

## 1-A Dual-HBD (Dual-Half-Bridge Driver)

TLE4207G



### Features

- Delivers up to 0.8 A continuous
- Optimized for DC motor management applications
- Very low current consumption in stand-by (Inhibit) mode
- Low saturation voltage; typ.1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Error flag diagnosis
- Overvoltage lockout and diagnosis
- Undervoltage lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal clamp diodes
- Overtemperature protection with hysteresis and diagnosis
- Enhanced power PG-DSO-Package
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-14

Type	Ordering Code	Package
TLE4207G	on request	PG-DSO-14

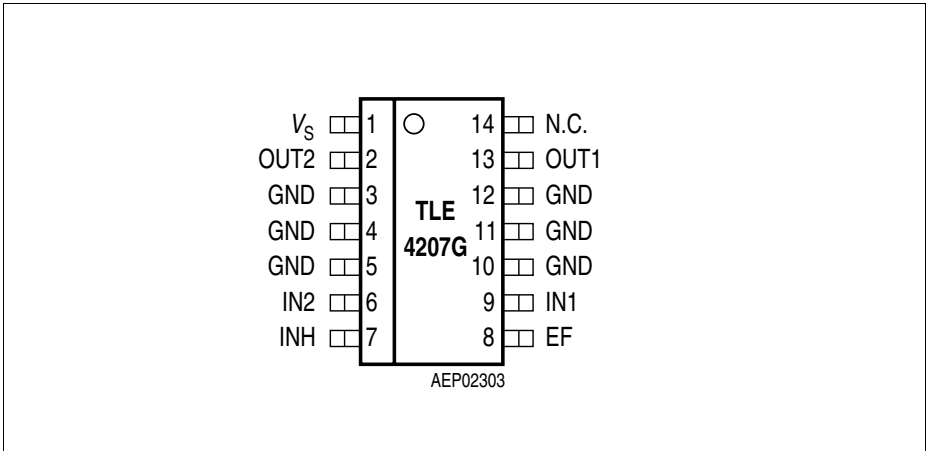
### Description

The TLE4207G is a protected **Dual-Half-Bridge-Driver** designed specially for automotive and industrial motion control applications.

The part is built using the Infineon bipolar high voltage power technology DOPL.

The actuator (DC motor) can be connected direct between the halfbridges. Operation modes forward (cw), reverse (ccw), brake and high impedance are invoked from a standard interface. The standard enhanced power PG-DSO-14 package meets the application requirements and saves PCB-board space and costs.

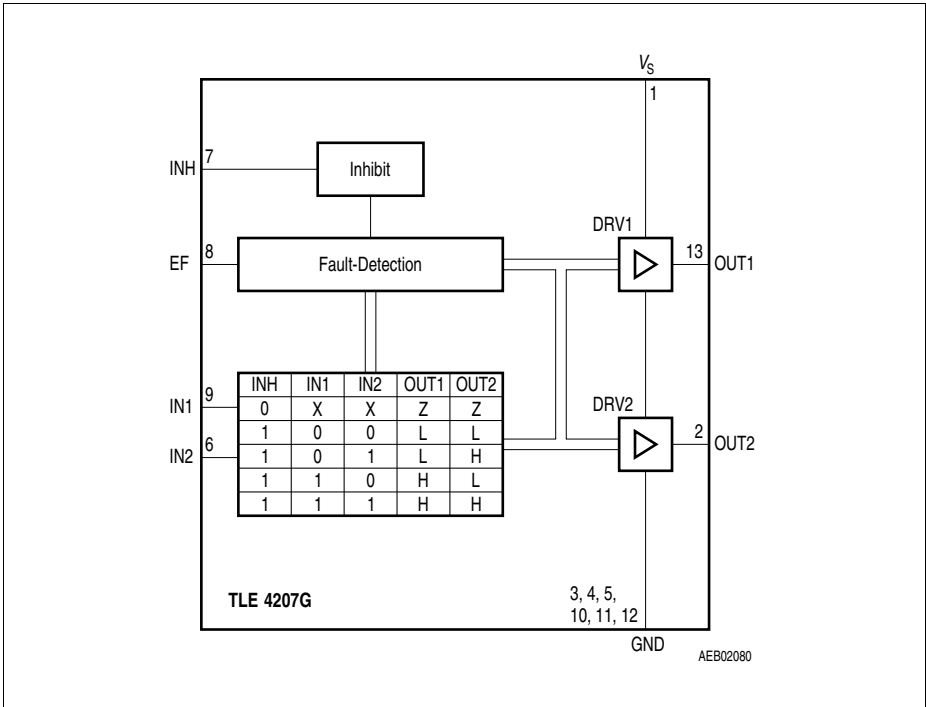
Furthermore the built in features like diagnosis, over- and undervoltage-lockout, short-circuit-protection, over-temperature-protection and the very low quiescent current in stand-by mode will open a wide range of automotive and industrial applications.



**Figure 1 Pin Configuration (top view)**

**Pin Definitions and Functions**

Pin No. PG-DSO-14	Symbol	Function
1	$V_S$	<b>Power supply voltage;</b> positive reference potential for blocking capacitor
2	OUT2	<b>Power output 2;</b> short circuit protected; with integrated clamp diodes
3, 4, 5, 10, 11, 12	GND	<b>Ground;</b> <b>negative</b> reference potential for blocking capacitor
6	IN2	<b>Input channel 2;</b> controls OUT2 (not inverted)
7	INH	<b>Inhibit input;</b> low = IC in stand-by
8	EF	<b>Error Flag output;</b> open collector; low = error
9	IN1	<b>Input channel 1;</b> controls OUT1 (not inverted)
13	OUT1	<b>Power output 1;</b> short circuit protected; with integrated clamp diodes
14	N.C.	<b>Not connected</b>



**Figure 2** Block Diagram

**Functional Truth Table**

<b>INH</b>	<b>IN1</b>	<b>IN2</b>	<b>OUT1</b>	<b>OUT2</b>	<b>Mode</b>
0	X	X	Z	Z	Stand-By
1	0	0	L	L	Brake LL
1	0	1	L	H	CW
1	1	0	H	L	CCW
1	1	1	H	H	Brake HH

IN: 0 = Logic LOW  
 1 = Logic HIGH  
 X = don't care

OUT: Z = Output in tristate condition  
 L = Output in sink condition  
 H = Output in source condition

**Diagnosis**

<b>EF</b>	<b>Error</b>
1	no error
0	over temperature
0	over voltage

**Electrical Characteristics**
**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

**Voltages**

Supply voltage	$V_S$	- 0.3	45	V	-
Supply voltage	$V_S$	- 1	-	V	$t < 0.5 \text{ s}; I_S > - 2 \text{ A}$
Logic input voltages (IN1; IN2; INH)	$V_I$	- 5	20	V	$0 \text{ V} < V_S < 45 \text{ V}$
Logic output voltage (EF)	$V_{EF}$	- 0.3	20	V	$0 \text{ V} < V_S < 45 \text{ V}$

**Currents**

Output current (cont.)	$I_{OUT1-2}$	-	-	A	internally limited
Output current (peak)	$I_{OUT1-2}$	-	-	A	internally limited
Output current (diode)	$I_{OUT1-2}$	- 1	1	A	-
Output current (EF)	$I_{OUT1-2}$	- 2	5	mA	-

**Temperatures**

Junction temperature	$T_j$	- 40	150	°C	-
Storage temperature	$T_{stg}$	- 50	150	°C	-

**Thermal Resistances**

Junction pin	$R_{thj-pin}$	-	25	K/W	measured to pin 5
Junction ambient	$R_{thjA}$	-	65	K/W	-

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

**Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	$V_{UV\ OFF}$	18	V	After $V_S$ rising above $V_{UV\ ON}$
Supply voltage increasing	$V_S$	- 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	$V_S$	- 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (IN1; IN2; INH)	$V_I$	- 2	18	V	-
Junction temperature	$T_j$	- 40	150	°C	-

*Note: In the operating range the functions given in the circuit description are fulfilled.*

**Electrical Characteristics**

8 V <  $V_S$  < 18 V; INH = High;  $I_{OUT1-2} = 0$  A;  $-40\text{ °C} < T_j < 150\text{ °C}$ ;  
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Current Consumption**

Quiescent current	$I_S$	–	20	50	$\mu$ A	INH = LOW
Quiescent current	$I_S$	–	20	30	$\mu$ A	INH = LOW; $V_S = 13.2$ V; $T_j = 25\text{ °C}$
Supply current	$I_S$	–	10	20	mA	–
Supply current	$I_S$	–	–	30	mA	$I_{OUT1} = 0.4$ A $I_{OUT2} = -0.4$ A
Supply current	$I_S$	–	–	50	mA	$I_{OUT1} = 0.8$ A $I_{OUT2} = -0.8$ A

**Over- and Under Voltage Lockout**

UV Switch ON voltage	$V_{UV\ ON}$	–	6.5	7.5	V	$V_S$ increasing
UV Switch OFF voltage	$V_{UV\ OFF}$	5.0	6	–	V	$V_S$ decreasing
UV ON/OFF hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
OV Switch OFF voltage	$V_{OV\ OFF}$	–	20	24	V	$V_S$ increasing
OV Switch ON voltage	$V_{OV\ ON}$	18.0	19.5	–	V	$V_S$ decreasing
OV ON/OFF hysteresis	$V_{OV\ HY}$	–	0.5	–	V	$V_{OV\ OFF} - V_{OV\ ON}$

**Electrical Characteristics (cont'd)**

8 V <  $V_S$  < 18 V; INH = High;  $I_{OUT1-2} = 0$  A;  $-40\text{ °C} < T_j < 150\text{ °C}$ ;  
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Outputs OUT1-2**
**Saturation Voltages**

Source (upper) $I_{OUT} = -0.2$ A	$V_{SAT U}$	–	0.85	1.15	V	$T_j = 25\text{ °C}$
Source (upper) $I_{OUT} = -0.4$ A	$V_{SAT U}$	–	0.90	1.20	V	$T_j = 25\text{ °C}$
Sink (upper) $I_{OUT} = -0.8$ A	$V_{SAT U}$	–	1.10	1.50	V	$T_j = 25\text{ °C}$
Sink (lower) $I_{OUT} = 0.2$ A	$V_{SAT L}$	–	0.15	0.23	V	$T_j = 25\text{ °C}$
Sink (lower) $I_{OUT} = 0.4$ A	$V_{SAT L}$	–	0.25	0.40	V	$T_j = 25\text{ °C}$
Sink (lower) $I_{OUT} = 0.8$ A	$V_{SAT L}$	–	0.45	0.75	V	$T_j = 25\text{ °C}$

Total Drop	$I_{OUT} = 0.2$ A	$V_{SAT}$	–	1	1.4	V	$V_{SAT} = V_{SAT U} + V_{SAT L}$
Total Drop	$I_{OUT} = 0.4$ A	$V_{SAT}$	–	1.2	1.7	V	$V_{SAT} = V_{SAT U} + V_{SAT L}$
Total Drop	$I_{OUT} = 0.8$ A	$V_{SAT}$	–	1.6	2.5	V	$V_{SAT} = V_{SAT U} + V_{SAT L}$

**Clamp Diodes**

Forward voltage; upper	$V_{FU}$	–	1	1.5	V	$I_F = 0.4$ A
Upper leakage current	$I_{L KU}$	–	–	5	mA	$I_F = 0.4$ A <sup>1)</sup>
Forward voltage; lower	$V_{FL}$	–	0.9	1.4	V	$I_F = 0.4$ A

Notes see page 10.



**Electrical Characteristics (cont'd)**

8 V <  $V_S$  < 18 V; INH = High;  $I_{OUT1-2} = 0$  A;  $-40$  °C <  $T_j$  < 150 °C;  
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input-Interface**
**Logic Inputs IN1; IN2**

H-input voltage	$V_{IH}$	–	2	3	V	–
L-input voltage	$V_{IL}$	1	1.5	–	V	–
Hysteresis of input voltage	$V_{IHY}$	–	0.5	–	V	–
H-input current	$I_{IH}$	– 2	–	10	μA	$V_I = 5$ V
L-input current	$I_{IL}$	– 100	– 20	– 5	μA	$V_I = 0$ V

**Logic Input INH**

H-input voltage	$V_{IH}$	–	2.7	3.5	V	–
L-input voltage	$V_{IL}$	1	2	–	V	–
Hysteresis of input voltage	$V_{IHY}$	–	0.7	–	V	–
H-input current	$I_{IH}$	–	100	250	μA	$V_{INH} = 5$ V
L-input current	$I_{IL}$	– 10	–	10	μA	$V_{INH} = 0$ V

**Error-Flag EF**

L-output voltage level	$V_{EFL}$	–	0.2	0.4	V	$I_{EF} = 2$ mA
Leakage current	$I_{EFLK}$	–	–	10	μA	$0$ V < $V_{EF}$ < 7 V

**Electrical Characteristics (cont'd)**

8 V <  $V_S$  < 18 V; INH = High;  $I_{OUT1-2} = 0$  A;  $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$ ;  
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Thermal Shutdown**

Thermal shutdown junction temperature	$T_{jSD}$	150	175	200	$^\circ\text{C}$	–
Thermal switch-on junction temperature	$T_{jSO}$	120	–	170	$^\circ\text{C}$	–
Temperature hysteresis	$\Delta T$	–	30	–	K	–

1) Guaranteed by design.

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ }^\circ\text{C}$  and the given supply voltage.*

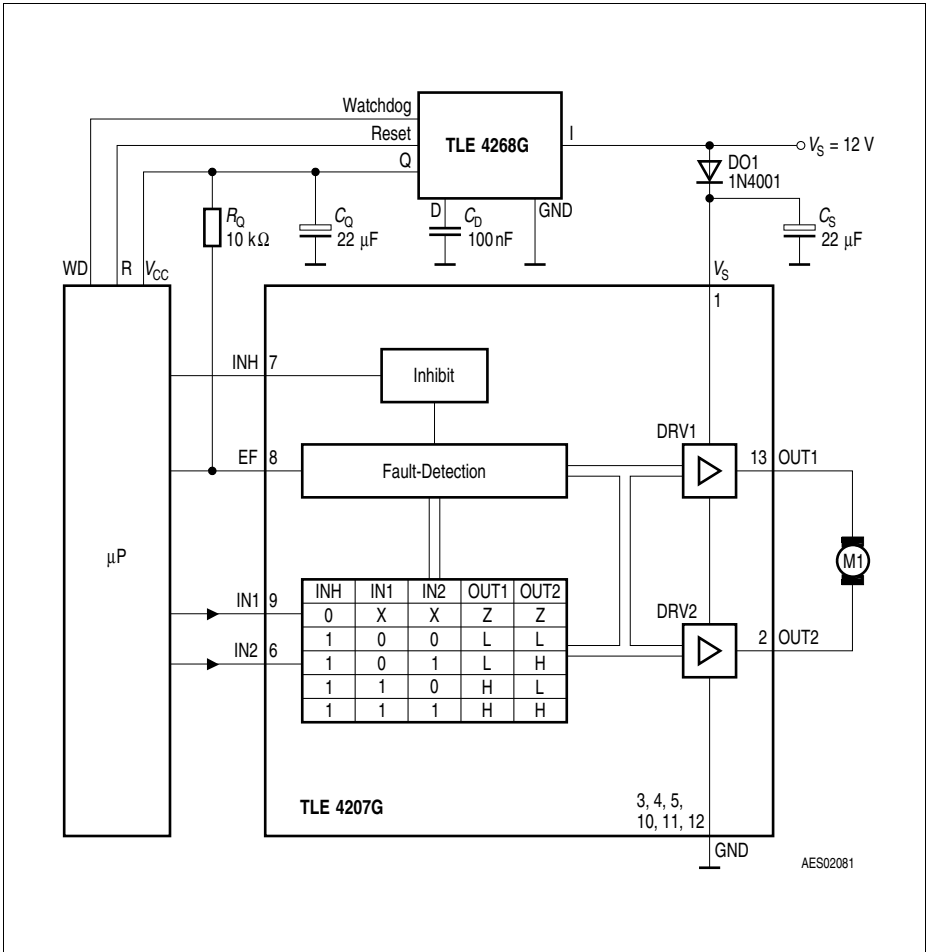
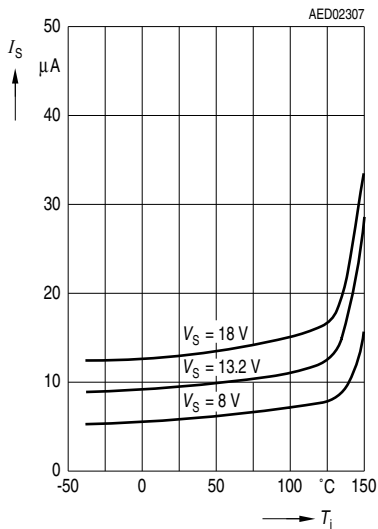


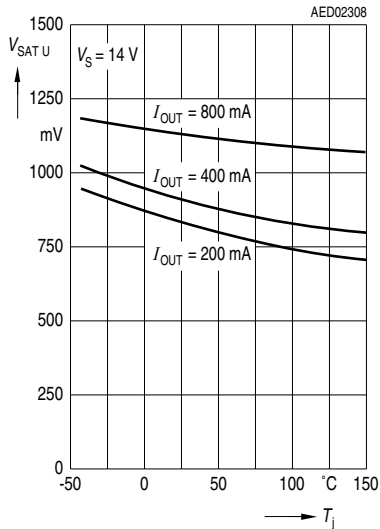
Figure 3 Application Circuit

Diagrams

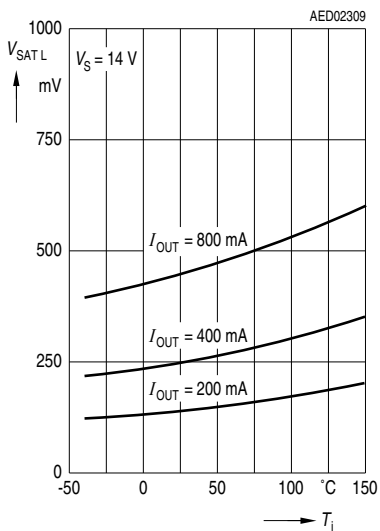
Quiescent current  $I_S$  over Temperature



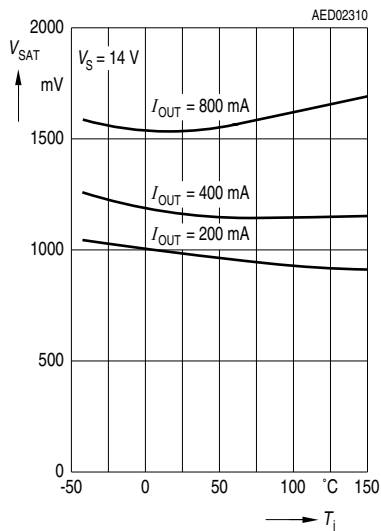
Saturation Voltage of Source  $V_{SAT U}$  over Temperature



Saturation Voltage of Sink  $V_{SAT L}$  over Temperature



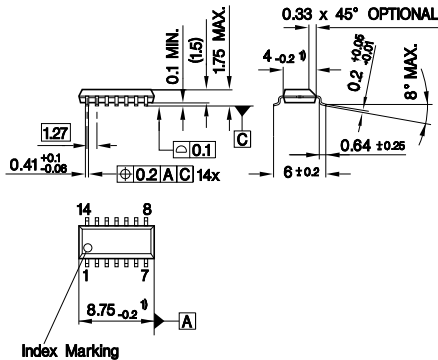
Total Drop at outputs  $V_{SAT}$  over Temperature



Package Outlines

**PG-DSO-14**

(Plastic Green - Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

**Green Product** (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Sorts of Packing, Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

**Revision History**

<b>Version</b>	<b>Date</b>	<b>Changes</b>
Rev. 1.1	2008-01-08	Initial version of RoHS-compliant derivate of TLE4207G Page 1: added AEC certified statement Page 1 and 13: added RoHS compliance statement and Green product feature Page 1+2: Editorial change: deleted "fully" (The term "fully protected" often leads to misunderstandings as it is unclear with respect to which parameters). Page 1 and 13: Package changed to RoHS compliant version Page 14 and 15: added Revision History, updated Legal Disclaimer
Rev. 1.2	2017-05-19	Removal of package suffix: PG-DSO-14-22 replaced by PG-DSO-14
Rev. 1.3	2018.07.02	Page 13: Modified package drawing

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