

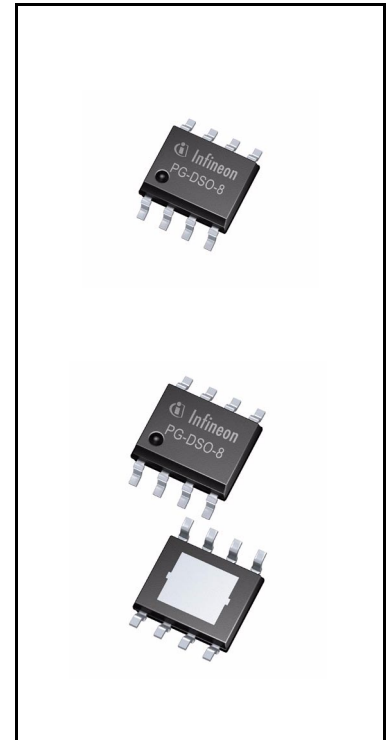
# OPTIREG™ linear TLE4253

## High precision voltage tracker



### Features

- Tight output tracking tolerance to reference
- Output voltage adjust down to 2.0 V
- Stable with ceramic output capacitor
- Flexibility of output voltage adjust higher or lower than reference, proportional to the reference voltage
- 250 mA output current capability
- Low dropout voltage
- Combined tracking / enable input
- Very low current consumption in OFF mode
- PG-DSO-8 packages with lowest thermal resistance
- Wide input voltage range  $-42\text{ V} \leq V_i \leq 45\text{ V}$
- Wide temperature range:  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$
- Output protected against short circuit to GND and battery
- Overtemperature protection
- Reverse polarity proof
- Suitable for use in automotive electronics
- Green product (RoHS compliant)



### Potential applications

- General automotive applications.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The OPTIREG™ linear TLE4253 is a monolithic integrated low-dropout voltage tracking regulator in small PG-DSO-8 packages. The exposed pad (EP) package variant PG-DSO-8 exposed pad offers extremely low thermal resistance. The IC is designed to supply off-board systems, e. g. sensors in engine management systems under the severe conditions of automotive applications. Therefore, the IC is equipped with additional protection functions against reverse polarity and short circuit to GND and battery.

With supply voltages up to 40 V, the output voltage follows a reference voltage applied at the adjust input with high accuracy. The reference voltage applied directly to the adjust input or by an e. g. external resistor divider can be 2.0 V at minimum.

The output is able to drive loads up to 250 mA at minimum while the device follows the e. g. 5 V output of a main voltage regulator acting as reference with high accuracy.

The TLE4253 tracker can be set into shutdown mode in order to reduce the quiescent current to an extremely low value. This makes the IC suitable to low power battery applications.

| <b>Type</b> | <b>Package</b>       | <b>Marking</b> |
|-------------|----------------------|----------------|
| TLE4253GS   | PG-DSO-8             | 4253           |
| TLE4253E    | PG-DSO-8 exposed pad | 4253E          |

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Block diagram

1 Block diagram

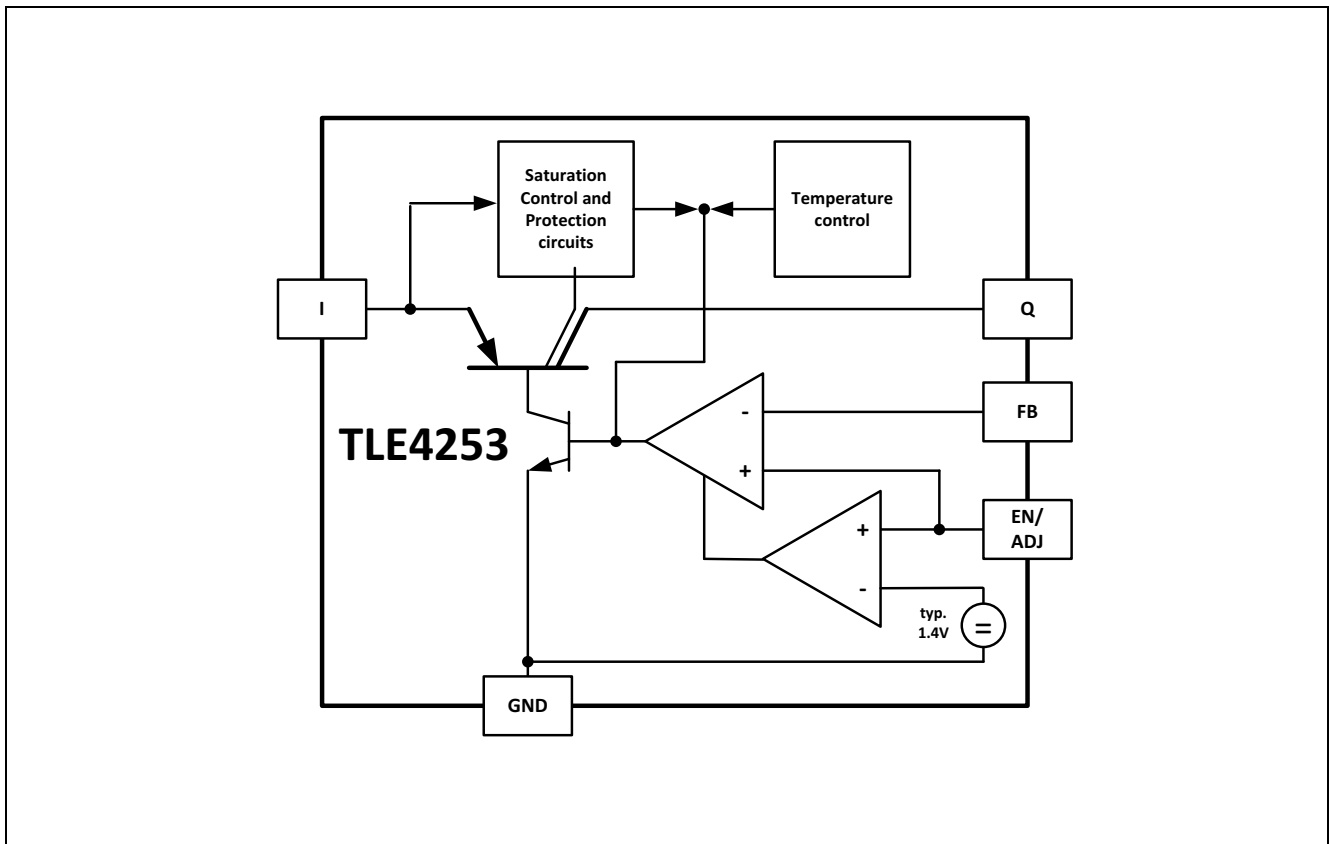
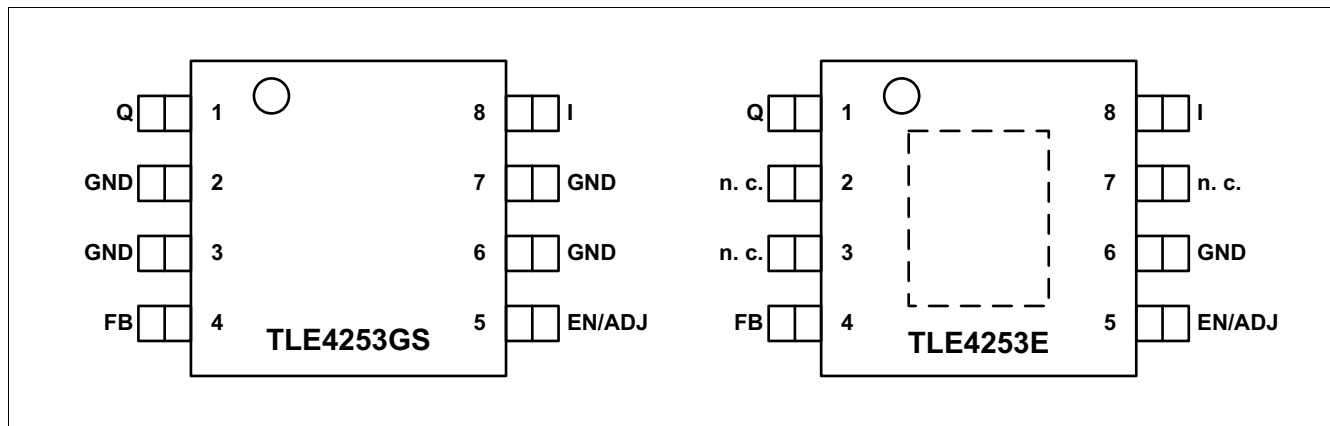


Figure 1 Block diagram

**Pin configuration**

## 2 Pin configuration

### 2.1 Pin assignment



**Figure 2 Pin configuration and block diagram**

### 2.2 Pin definitions and functions

| Pin        | Symbol | Function  |
|------------|--------|---|
| 1          | Q      | <b>Tracker output.</b><br>Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table “Functional Range”.   |
| 2, 3, 6, 7 | GND    | <b>Ground reference</b> (version TLE4253GS only).<br>Interconnect the pins on PCB. Connect to heatsink area.  |
| 6          | GND    | <b>Ground</b> (version TLE4253E only).<br>Connect to exposed pad.   |
| 2, 3, 7    | n. c.  | <b>Not connected</b> (version TLE4253E only).<br>Connect to GND externally.   |
| 4          | FB     | <b>Feedback input for tracker.</b><br>Inverting input of the internal error amplifier to control the output voltage. Connect this pin directly to the output pin in order to obtain lower or equal output voltages with respect to the reference voltage and connect a voltage divider for higher output voltages than the reference (see application information). |
| 5          | EN/ADJ | <b>Adjust / enable.</b><br>Connect the reference to this pin. The active high signal of the reference turns on the device, with active low the tracker is disabled. The reference voltage can be connected directly or by a voltage divider for lower output voltages (see application information).  |
| 8          | I      | <b>Input.</b><br>IC supply. For compensating line influences, a capacitor close to the IC terminals is recommended.   |
| –          | EP     | <b>Exposed pad</b> (version TLE4253E only).<br>Attach the exposed pad on package bottom to the heatsink area on circuit board. Connect to GND.  |

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 1 Absolute maximum ratings** <sup>1)</sup>

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified).

| Parameter             | Symbol        | Values |      |      | Unit | Note or Test Condition | Number  |
|-----------------------|---------------|--------|------|------|------|------------------------|---------|
|                       |               | Min.   | Typ. | Max. |      |                        |         |
| <b>Voltages</b>       |               |        |      |      |      |                        |         |
| Input voltage         | $V_I$         | -42    | –    | 45   | V    | –                      | P_4.1.1 |
| Output voltage        | $V_Q$         | -2     | –    | 45   | V    | –                      | P_4.1.2 |
| Adjust / enable input | $V_{ADJ/EN}$  | -42    | –    | 45   | V    | –                      | P_4.1.3 |
| Feedback input        | $V_{FB}$      | -42    | –    | 45   | V    | –                      | P_4.1.4 |
| <b>Temperature</b>    |               |        |      |      |      |                        |         |
| Junction temperature  | $T_j$         | -40    | –    | 150  | °C   | –                      | P_4.1.5 |
| Storage temperature   | $T_{stg}$     | -50    | –    | 150  | °C   | –                      | P_4.1.6 |
| <b>ESD rating</b>     |               |        |      |      |      |                        |         |
| ESD susceptibility    | $V_{ESD,HBM}$ | -4     | –    | 4    | kV   | HBM <sup>2)</sup>      | P_4.1.7 |
|                       | $V_{ESD,CDM}$ | -1     | –    | 1    | kV   | CDM <sup>3)</sup>      | P_4.1.8 |

1) Not subject to production test, specified by design.

2) ESD susceptibility Human Body Model “HBM” according to EIA/JESD 22-A 114B.

3) ESD susceptibility Charged Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1.

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**General product characteristics**

**3.2 Functional range**

**Table 2 Functional range**

| Parameter  | Symbol       | Values |      |      | Unit | Note or Test Condition  | Number  |
|--|--------------|--------|------|------|------|-------------------------|---------|
|  |              | Min.   | Typ. | Max. |      |                         |         |
| Input voltage  | $V_I$        | 3.5    | –    | 40   | V    | $V_I \geq V_Q + V_{dr}$ | P_4.2.1 |
| Adjust / enable input voltage (voltage tracking range) | $V_{ADJ/EN}$ | 2.0    | –    | –    | V    | –                       | P_4.2.5 |
| Junction temperature                                   | $T_j$        | -40    | –    | 150  | °C   | –                       | P_4.2.2 |
| Output capacitor requirements                          | $C_Q$        | 10     | –    | –    | μF   | <sup>1)</sup>           | P_4.2.3 |
|  | $ESR_{CQ}$   | –      | –    | 5    | Ω    | <sup>2)</sup>           | P_4.2.4 |

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

2) Relevant ESR value at  $f = 10$  kHz.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

**General product characteristics**

**3.3 Thermal resistance**

**Table 3 Thermal resistance**

| Parameter                   | Symbol      | Values |      |      | Unit | Note or Test Condition                              | Number   |
|-----------------------------|-------------|--------|------|------|------|---|----------|
|                             |             | Min.   | Typ. | Max. |      |   |          |
| <b>PG-DSO-8</b>             |             |        |      |      |      |   |          |
| Junction to soldering point | $R_{thJSP}$ | –      | 39   | –    | K/W  | Pins 2 - 3 and 6 - 7 fixed to $T_A$                 | P_4.3.1  |
| Junction to ambient         | $R_{thJA}$  | –      | 150  | –    | K/W  | Footprint only <sup>1)</sup>                        | P_4.3.2  |
|                             | –           | –      | 91   | –    | K/W  | 300 mm <sup>2</sup> PCB heatsink area <sup>1)</sup> | P_4.3.3  |
|                             | –           | –      | 81   | –    | K/W  | 600 mm <sup>2</sup> PCB heatsink area <sup>1)</sup> | P_4.3.4  |
|                             | –           | –      | 65   | –    | K/W  | 2s2p board <sup>2)</sup>                            | P_4.3.5  |
| <b>PG-DSO-8 exposed pad</b> |             |        |      |      |      |   |          |
| Junction to case bottom     | $R_{thJC}$  | –      | 9    | –    | K/W  | Measured to exposed bottom pad                      | P_4.3.6  |
| Junction to ambient         | $R_{thJA}$  | –      | 169  | –    | K/W  | Footprint only <sup>1)</sup>                        | P_4.3.7  |
|                             | –           | –      | 64   | –    | K/W  | 300 mm <sup>2</sup> PCB heatsink area <sup>1)</sup> | P_4.3.8  |
|                             | –           | –      | 55   | –    | K/W  | 600 mm <sup>2</sup> PCB heatsink area <sup>1)</sup> | P_4.3.9  |
|                             | –           | –      | 49   | –    | K/W  | 2s2p board <sup>2)</sup>                            | P_4.3.10 |

1) Package mounted on PCB FR4; 80 × 80 × 1.5 mm<sup>3</sup>; 35 μm Cu, 5 μm Sn; horizontal position; zero airflow. Not subject to production test; specified by design.

2) Specified  $R_{thJA}$  value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the package contacted the first inner copper layer.



## **4 Electrical characteristics**

### **4.1 Tracking regulator**

The output voltage  $V_Q$  is controlled by comparing it to the voltage applied at pin ADJ/EN and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "Functional Range" have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor  $ESR_{CQ}$  vs. Output Current  $I_Q$ ". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor  $C_I$  is strongly recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at high input voltages.

An overtemperature protection circuit prevents the IC from immediate destruction under fault conditions (e. g. output continuously short-circuited to GND) by reducing the output current. A thermal balance below 200°C junction temperature is established. Please note that a junction temperature above 150°C is outside the maximum ratings and reduces the IC lifetime.

The TLE4253 allows a negative supply voltage. However, several small currents are flowing into the IC. For details see electrical characteristics table and typical performance graph. The thermal protection circuit is not operating during reverse polarity condition.

**Electrical characteristics**

**Table 4 Electrical characteristics tracking regulator**

$V_I = 13.5\text{ V}$ ;  $V_{\text{ADJ/EN}} \geq 2.0\text{ V}$ ;  $V_{\text{FB}} = V_Q$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ;  
 all voltages with respect to ground (unless otherwise specified).

| Parameter  | Symbol                       | Values |      |      | Unit | Note or Test Condition  | Number   |
|--|------------------------------|--------|------|------|------|---|----------|
|  |                              | Min.   | Typ. | Max. |      |   |          |
| Output voltage tracking accuracy<br>$\Delta V_Q = V_{\text{EN/ADJ}} - V_Q$ | $\Delta V_Q$                 | -5     | -    | 5    | mV   | $I_Q = 30\text{ mA}$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$  | P_5.1.1  |
|  | -                            | -10    | -    | 10   | mV   | $0.1\text{ mA} \leq I_Q \leq 200\text{ mA}$ ;<br>$3.5\text{ V} \leq V_I \leq 32\text{ V}$<br>$V_{\text{ADJ/EN}} = 2\text{ V}$             | P_5.1.2  |
|  | -                            | -15    | -    | 15   | mV   | $0.1\text{ mA} \leq I_Q \leq 250\text{ mA}$ ;<br>$9\text{ V} \leq V_I \leq 32\text{ V}$<br>$V_{\text{ADJ/EN}} = 5\text{ V}$               | P_5.1.3  |
| Load regulation steady-state   | $ \Delta V_{Q,\text{load}} $ | -      | -    | 10   | mV   | $0.1\text{ mA} \leq I_Q \leq 200\text{ mA}$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$   | P_5.1.4  |
| Line regulation steady-state   | $ \Delta V_{Q,\text{line}} $ | -      | -    | 10   | mV   | $V_I = 6\text{ V}$ to $32\text{ V}$ ;<br>$I_Q = 10\text{ mA}$<br>$V_{\text{ADJ/EN}} = 5\text{ V}$   | P_5.1.5  |
| Power supply ripple rejection  | <i>PSRR</i>                  | 60     | -    | -    | dB   | $f_{\text{ripple}} = 100\text{ Hz}$ ;<br>$V_{\text{ripple}} = 1\text{ Vpp}$<br>$C_Q = 10\text{ }\mu\text{F}$ , ceramic type <sup>1)</sup> | P_5.1.6  |
| Dropout voltage<br>$V_{\text{dr}} = V_I - V_Q$                             | $V_{\text{dr}}$              | -      | 280  | 600  | mV   | $I_Q = 200\text{ mA}$ <sup>2)</sup>   | P_5.1.7  |
| Output current limitation  | $I_{Q,\text{max}}$           | 251    | 400  | 600  | mA   | $V_Q = (V_{\text{ADJ}} - 0.1\text{ V})$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$   | P_5.1.8  |
| Reverse current  | $I_Q$                        | -10    | -5.5 | -    | mA   | $V_I = 0\text{ V}$ ;<br>$V_Q = 16\text{ V}$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$   | P_5.1.9  |
| Reverse current at negative input voltage                                  | $I_I$                        | -5     | -2   | -    | mA   | $V_I = -16\text{ V}$ ;<br>$V_Q = 0\text{ V}$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$  | P_5.1.10 |

**Feedback input FB**

|                                |                 |   |     |     |               |                              |          |
|--------------------------------|-----------------|---|-----|-----|---------------|------------------------------|----------|
| Feedback input biasing current | $I_{\text{FB}}$ | - | 0.1 | 0.5 | $\mu\text{A}$ | $V_{\text{FB}} = 5\text{ V}$ | P_5.1.11 |
|--------------------------------|-----------------|---|-----|-----|---------------|------------------------------|----------|

**Overtemperature protection**

|                                  |                   |     |   |     |                  |   |          |
|----------------------------------|-------------------|-----|---|-----|------------------|---|----------|
| Junction temperature equilibrium | $T_{j,\text{eq}}$ | 151 | - | 200 | $^\circ\text{C}$ | $T_j$ increasing due to power dissipation generated by the IC <sup>1)</sup> | P_5.1.12 |
|----------------------------------|-------------------|-----|---|-----|------------------|---|----------|

1) Parameter not subject to production test; specified by design.

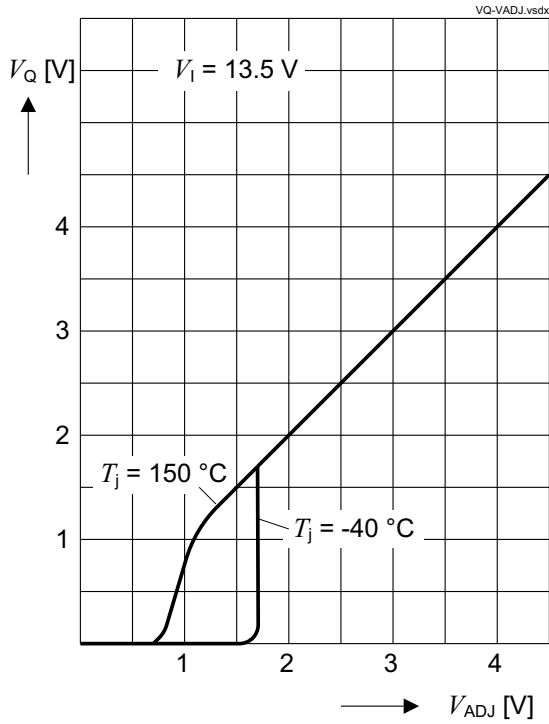
2) Measured when the output voltage  $V_Q$  has dropped 100 mV from its nominal value.

**Electrical characteristics**

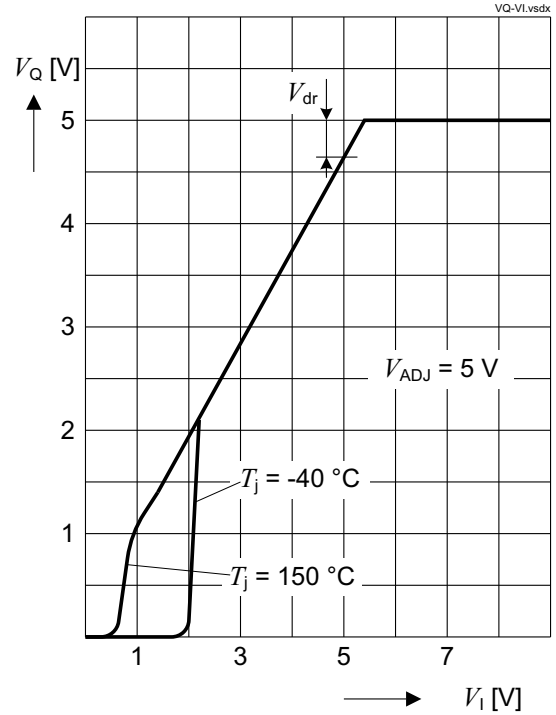
**Typical performance characteristics tracking regulator**

$V_{ADJ/EN} = 5\text{ V}$ ;  $V_{FB} = V_Q$  (unless otherwise noted)

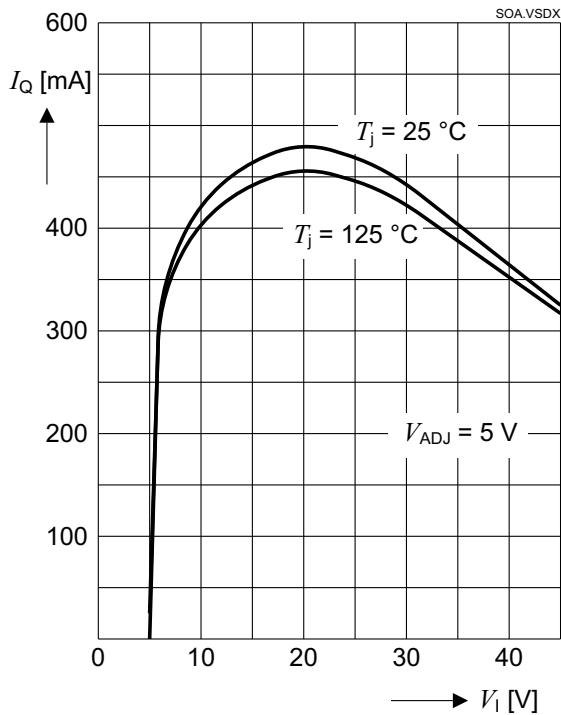
**Output voltage  $V_Q$  vs. adjust voltage  $V_{ADJ}$**



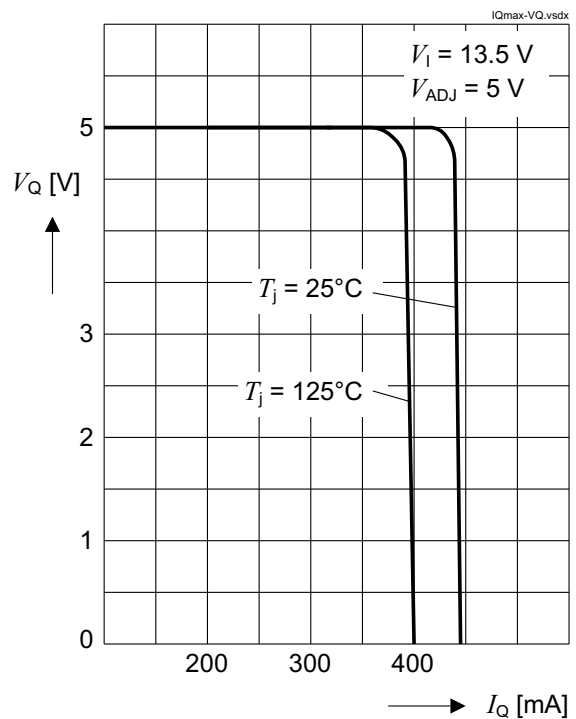
**Output voltage  $V_Q$  vs. input voltage  $V_I$**



**Output current limitation  $I_{Q,max}$  vs. input voltage  $V_I$**



**Output current limitation  $I_{Q,max}$  vs. output voltage  $V_Q$**

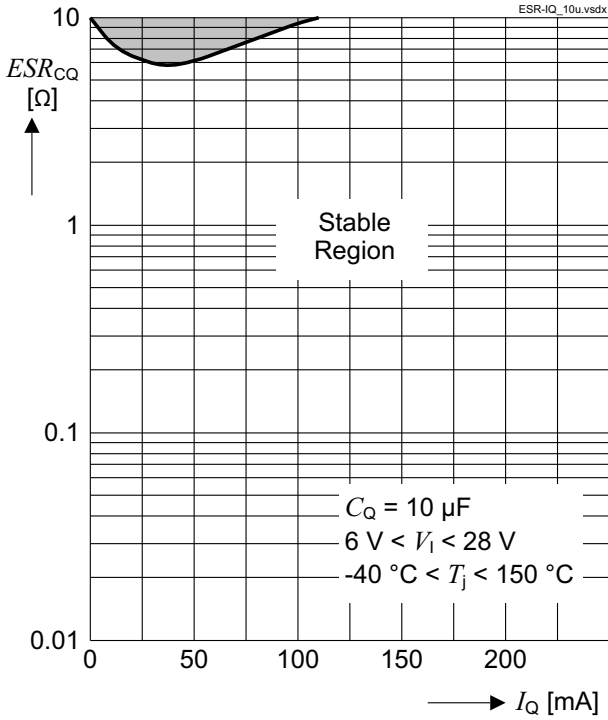


**Electrical characteristics**

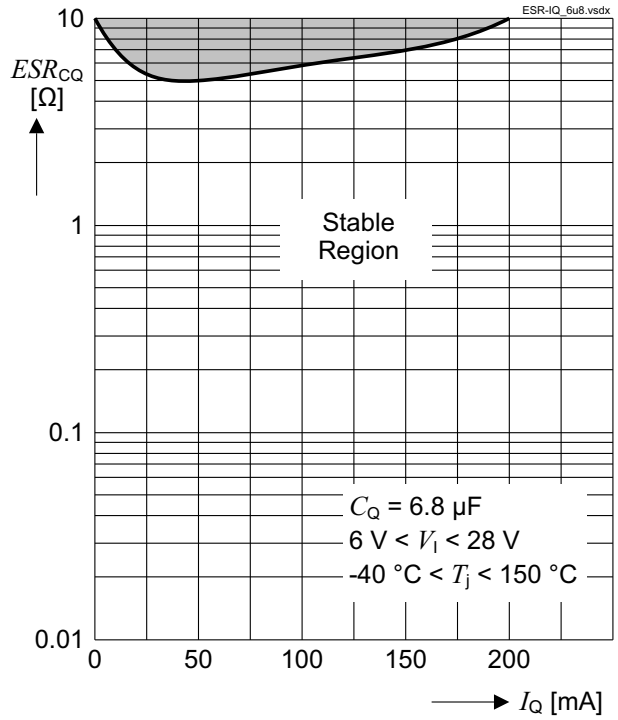
**Typical performance characteristics tracking regulator**

$V_{ADJ/EN} = 5\text{ V}$ ;  $V_{FB} = V_Q$  (unless otherwise noted)

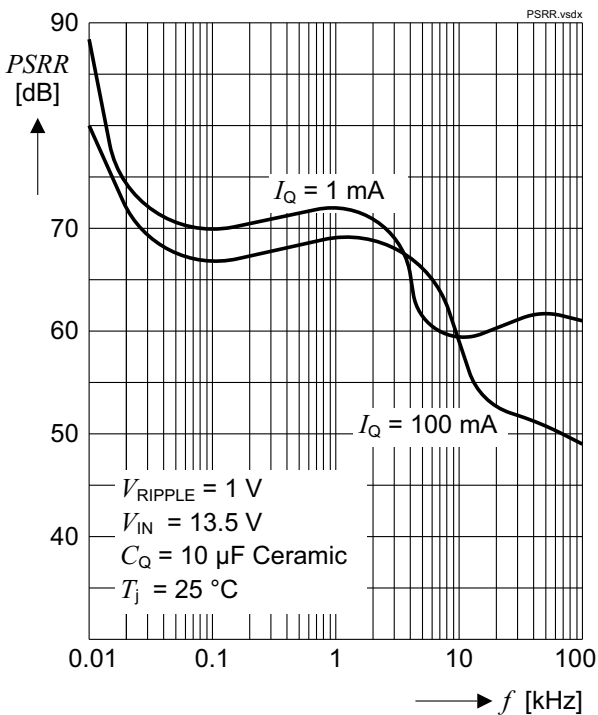
**Output capacitor series resistor  $ESR_{CQ}$  vs. output current  $I_Q$**



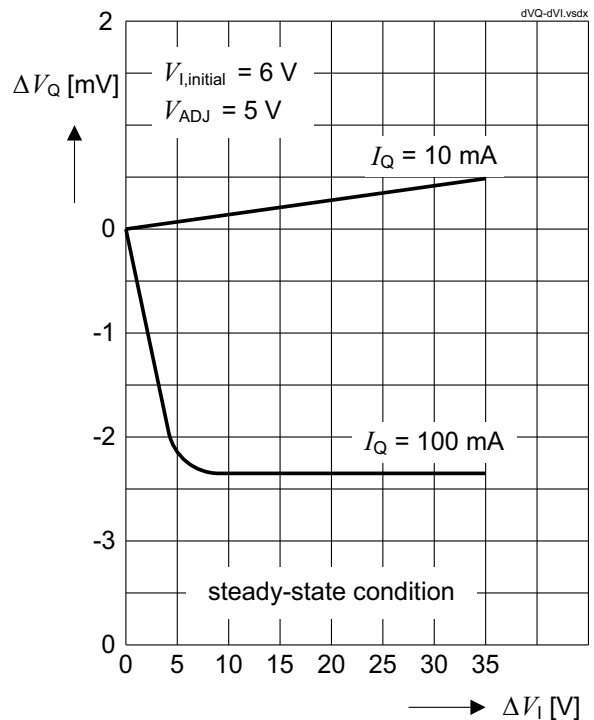
**Output capacitor series resistor  $ESR_{CQ}$  vs. output current  $I_Q$**



**Power supply ripple rejection  $PSRR$**



**Line regulation  $dV_{Q,line}$  vs. input voltage change  $dV_I$**

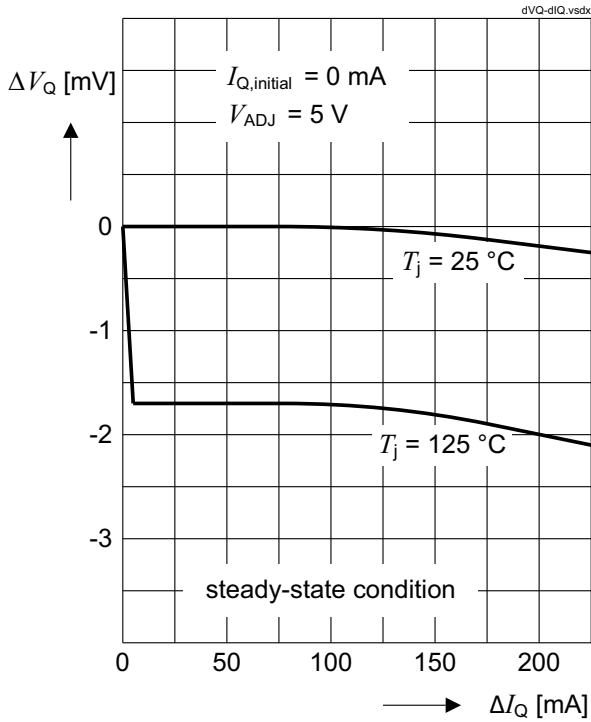


**Electrical characteristics**

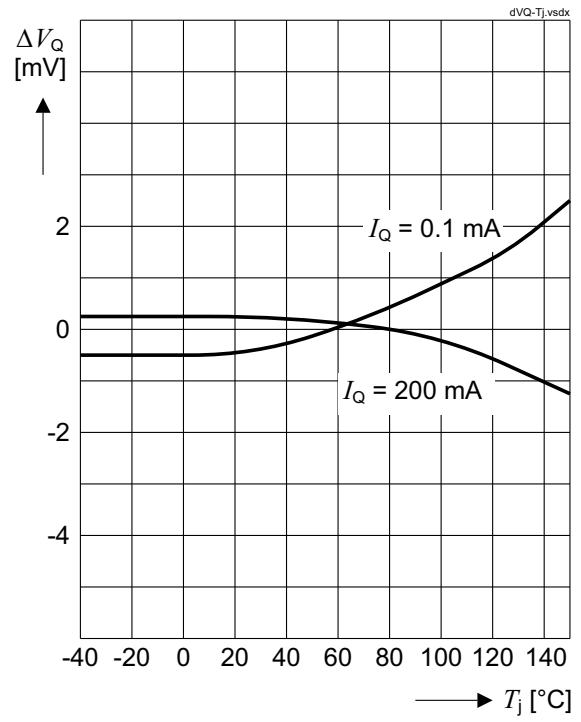
**Typical performance characteristics tracking regulator**

$V_{ADJ/EN} = 5\text{ V}$ ;  $V_{FB} = V_Q$  (unless otherwise noted)

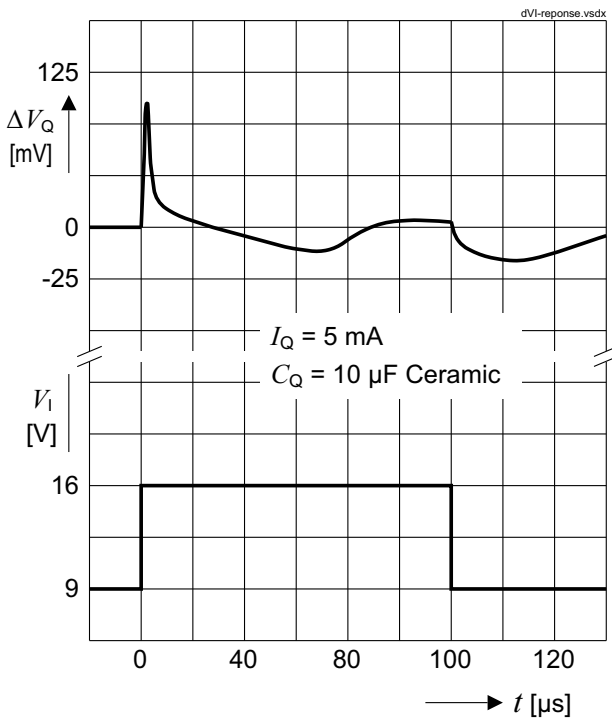
**Load regulation  $dV_{Q,line}$  vs. output current change  $dI_Q$**



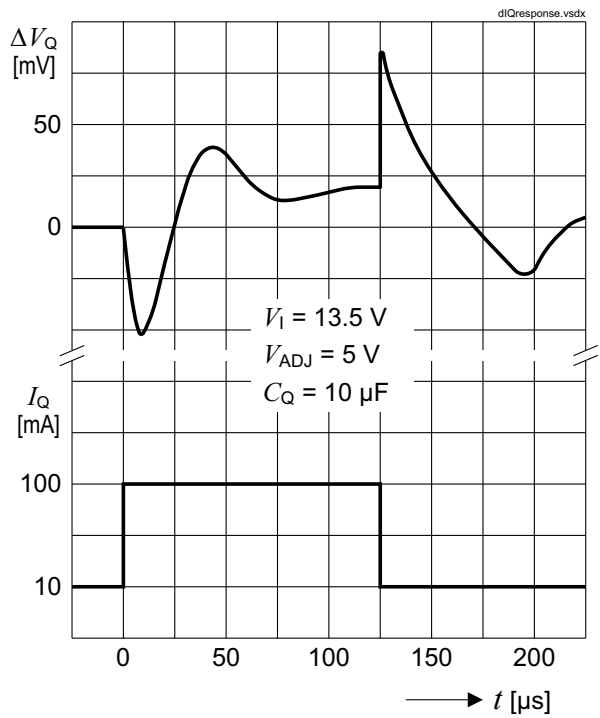
**Tracking accuracy  $\Delta V_Q$  vs. junction temperature  $T_j$**



**Line transient response**



**Load transient response**

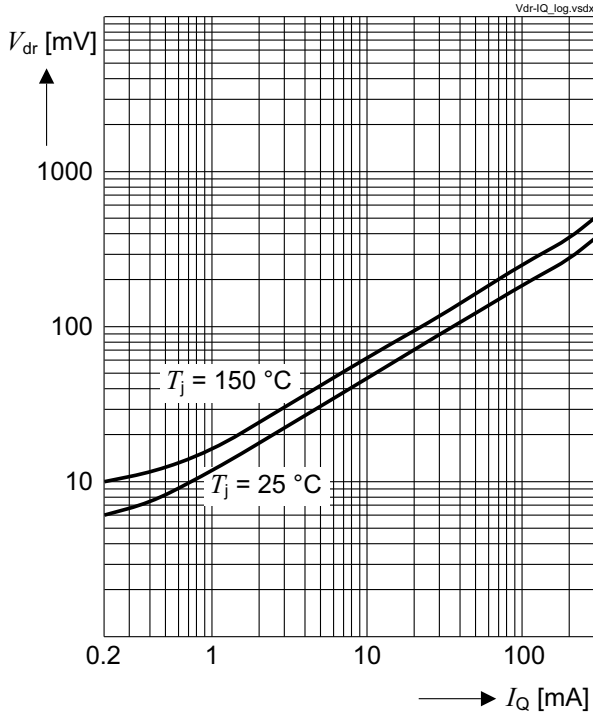


**Electrical characteristics**

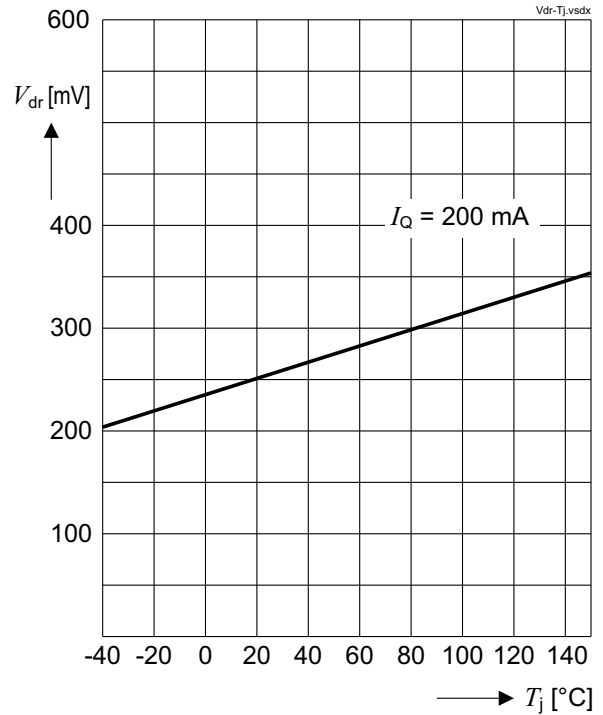
**Typical performance characteristics tracking regulator**

$V_{ADJ/EN} = 5\text{ V}$ ;  $V_{FB} = V_Q$  (unless otherwise noted)

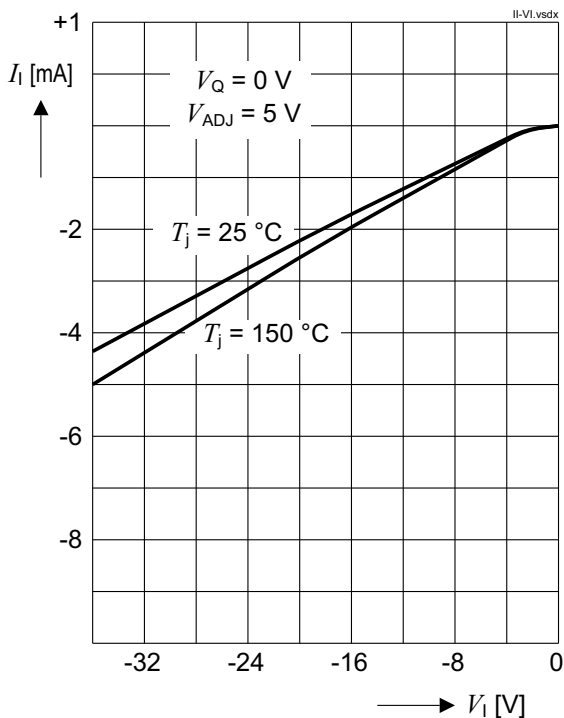
**Dropout voltage  $V_{dr}$  vs. output current  $I_Q$**



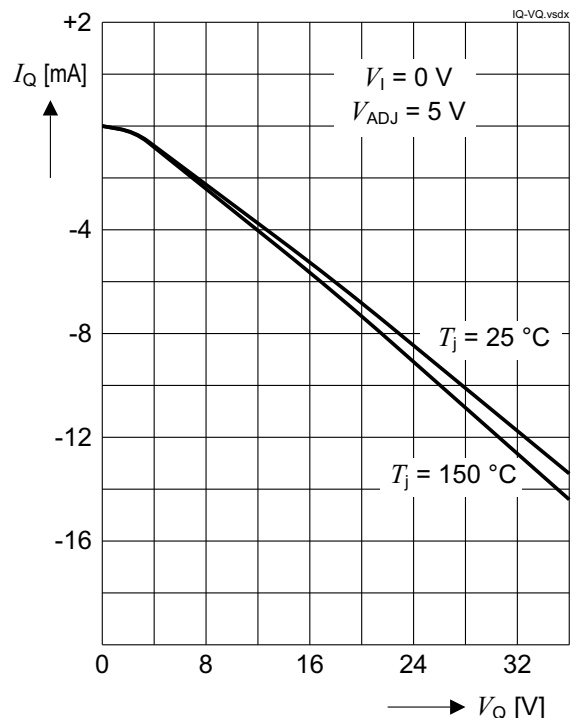
**Dropout voltage  $V_{dr}$  vs. junction temperature  $T_j$**



**Reverse current  $I_I$  vs. input voltage  $V_I$**



**Reverse output current  $I_Q$  vs. output voltage  $V_Q$**



**Electrical characteristics**

**4.2 Current consumption**

**Table 5 Electrical characteristics current consumption**

$V_I = 13.5\text{ V}$ ;  $V_{\text{ADJ/EN}} \geq 2.0\text{ V}$ ;  $V_{\text{FB}} = V_Q$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ;  
 all voltages with respect to ground (unless otherwise specified).

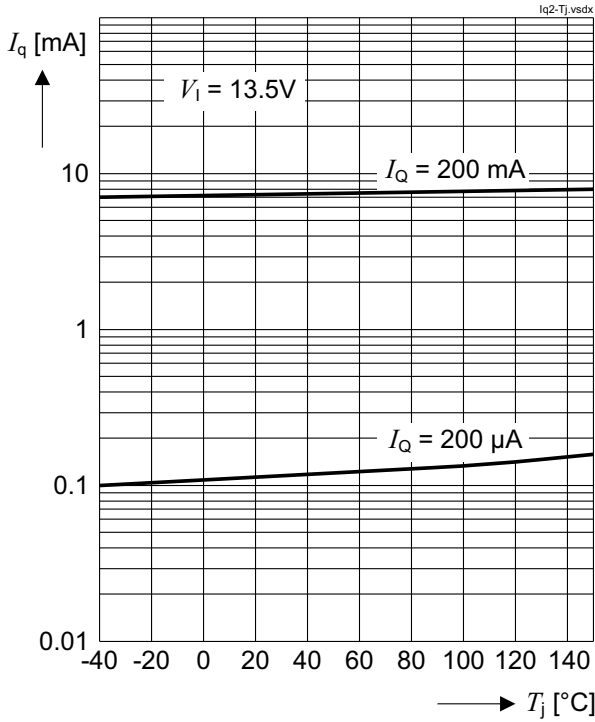
| Parameter   | Symbol   | Values |      |      | Unit          | Note or Test Condition   | Number  |
|---|----------|--------|------|------|---------------|--|---------|
|   |          | Min.   | Typ. | Max. |               |  |         |
| Quiescent current stand-by mode                       | $I_{q1}$ | –      | 0    | 2    | $\mu\text{A}$ | $V_Q = 0\text{ V}$ ;<br>$V_{\text{ADJ/EN}} \leq 0.4\text{ V}$ ;<br>$T_j \leq 85^\circ\text{C}$     | P_5.2.1 |
| Current consumption<br>$I_q = I_I - I_Q$              | $I_{q2}$ | –      | 120  | 150  | $\mu\text{A}$ | $I_Q \leq 100\ \mu\text{A}$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$ ;<br>$T_j \leq 85^\circ\text{C}$ | P_5.2.2 |
|   | –        | –      | 7    | 15   | $\text{mA}$   | $I_Q \leq 200\ \text{mA}$ ;<br>$V_{\text{ADJ/EN}} = 5\text{ V}$                                    | P_5.2.3 |
| Current consumption dropout region; $I_q = I_I - I_Q$ | $I_{q3}$ | –      | 1    | 3    | $\text{mA}$   | $V_{\text{ADJ}} = V_I = 5\text{ V}$ ;<br>$I_Q = 0\ \text{mA}$                                      | P_5.2.4 |

**Electrical characteristics**

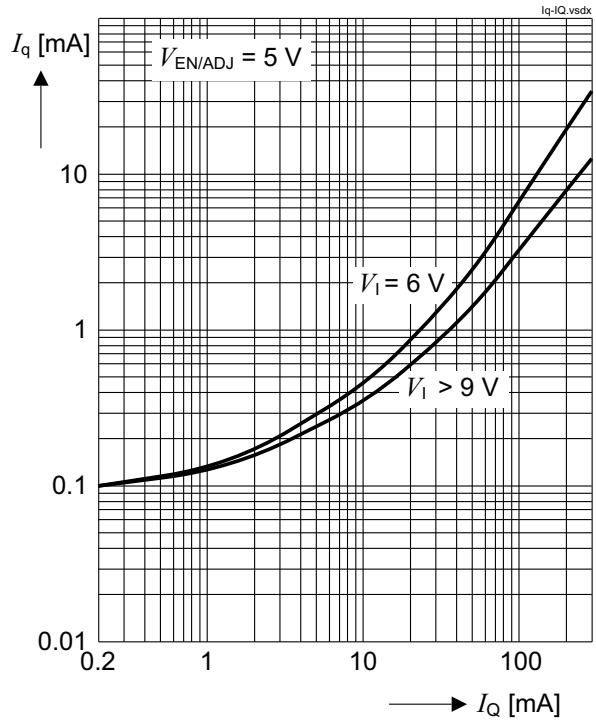
**Typical performance characteristics tracking regulator**

$V_{ADJ/EN} = 5\text{ V}$ ;  $V_{FB} = V_Q$  (unless otherwise noted)

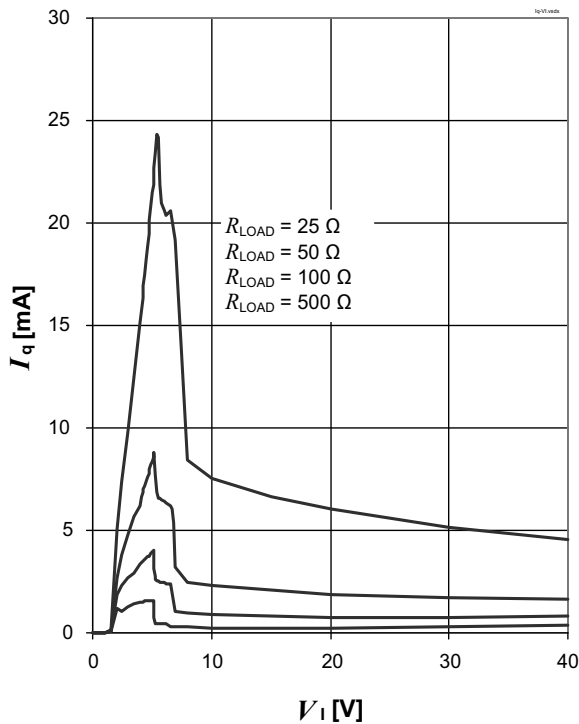
**Current consumption  $I_{q2}$  vs. junction temperature  $T_j$**



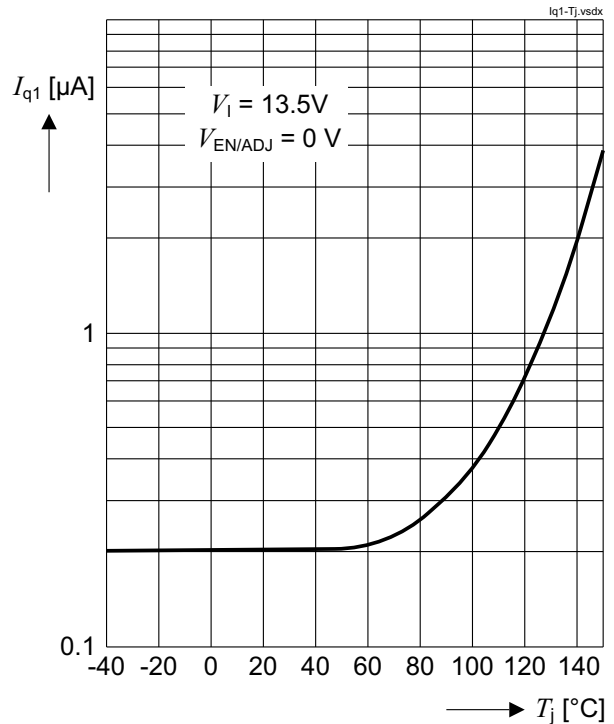
**Current consumption  $I_q$  vs. output current  $I_Q$**



**Current consumption  $I_q$  vs. input voltage  $V_i$**



**Quiescent current  $I_{q1}$  vs. junction temperature  $T_j$**





**Electrical characteristics**

**4.3 Adjust / enable input**

In order to reduce the quiescent current to a minimum, the TLE4253 can be switched to stand-by mode by setting the adjust/enable input “ADJ/EN” to “low”.

In case the pin “ADJ/EN” is left open, an internal pull-down resistor keeps the voltage at the pin low and therefore ensures that the regulator is switched off.

**Table 6 Electrical characteristics adjust / enable**

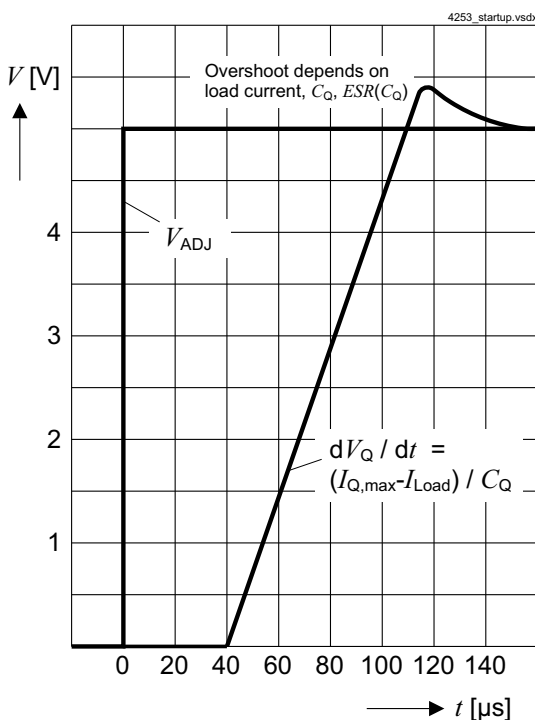
$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.0\text{ V}$ ;  $V_{FB} = V_Q$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ;  
 all voltages with respect to ground (unless otherwise specified).

| Parameter   | Symbol            | Values |      |      | Unit             | Note or Test Condition  | Number  |
|---|-------------------|--------|------|------|------------------|---|---------|
|   |                   | Min.   | Typ. | Max. |                  |   |         |
| Adjust / enable low signal valid                    | $V_{ADJ/EN,low}$  | –      | –    | 0.4  | V                | $V_Q = 0\text{ V}$ ;<br>$I_I < 2\ \mu\text{A}$ ;<br>$T_j \leq 85^\circ\text{C}$ | P_5.3.1 |
| Adjust / enable high signal valid (tracking region) | $V_{ADJ/EN,high}$ | 2      | –    | –    | V                | $V_Q$ settled:<br>$ V_Q - V_{ADJ/EN}  < 10\text{ mV}$ ;<br>$I_Q = 10\text{ mA}$ | P_5.3.2 |
| Adjust / enable input current                       | $I_{ADJ/EN}$      | –      | 3.8  | 5.5  | $\mu\text{A}$    | $V_{ADJ/EN} = 5\text{ V}$ ;   | P_5.3.3 |
| Adjust / enable internal pull-down resistor         | $R_{ADJ/EN}$      | 1      | 1.5  | 2    | $\text{M}\Omega$ | –   | P_5.3.4 |

**Typical performance characteristics tracking regulator**

$V_{ADJ/EN} = 5\text{ V}$ ;  $V_{FB} = V_Q$  (unless otherwise noted)

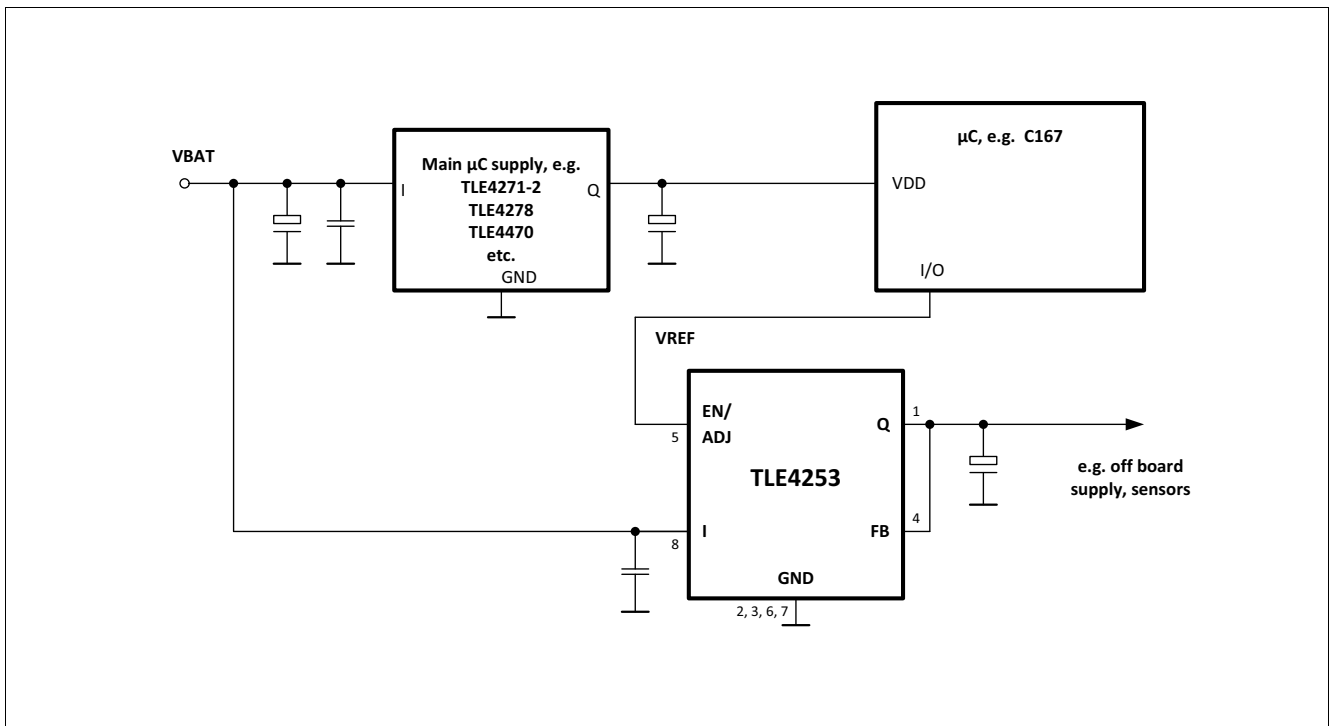
**Startup sequence**



**Application information**

**5 Application information**

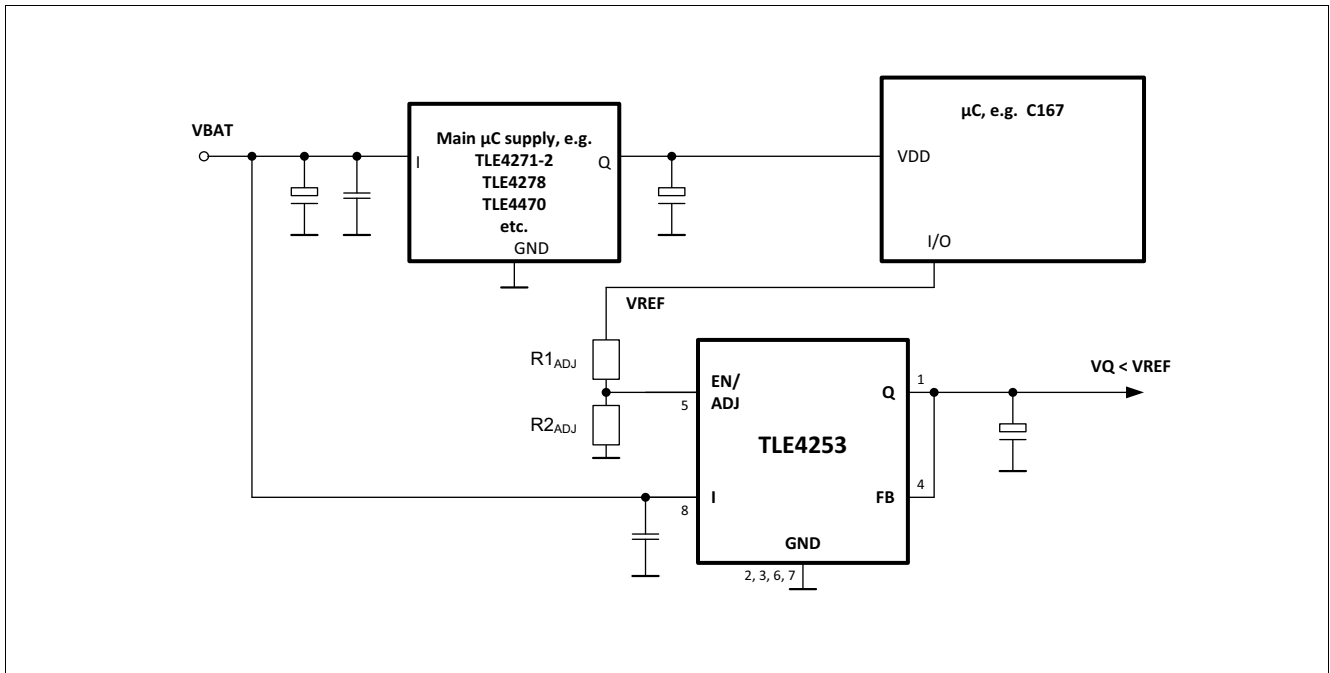
*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The application circuits shown are simplified examples. The function must be verified in the real application.*



**Figure 3 Application circuit: Output voltage  $V_Q$  equal to reference voltage  $V_{REF}$**

**Figure 3** shows the typical schematic for applications where the tracker output voltage equals the reference voltage  $V_{REF}$  applied to the pin “EN/ADJ”. The pin “FB” is connected directly to the output. The reference voltage is directly applied “EN/ADJ”.

**Application information**



**Figure 4 Application circuit: Output voltage  $V_Q$  lower than reference voltage  $V_{REF}$**

In order to obtain a lower output voltage  $V_Q$  at the tracker output than the reference voltage  $V_{REF}$ , a voltage divider according to **Figure 4** has to be used. The output voltage  $V_Q$  then calculates:

$$V_Q = V_{REF} \cdot \left( \frac{R2_{ADJ}}{R1_{ADJ} + R2_{ADJ}} \right) \quad (5.1)$$

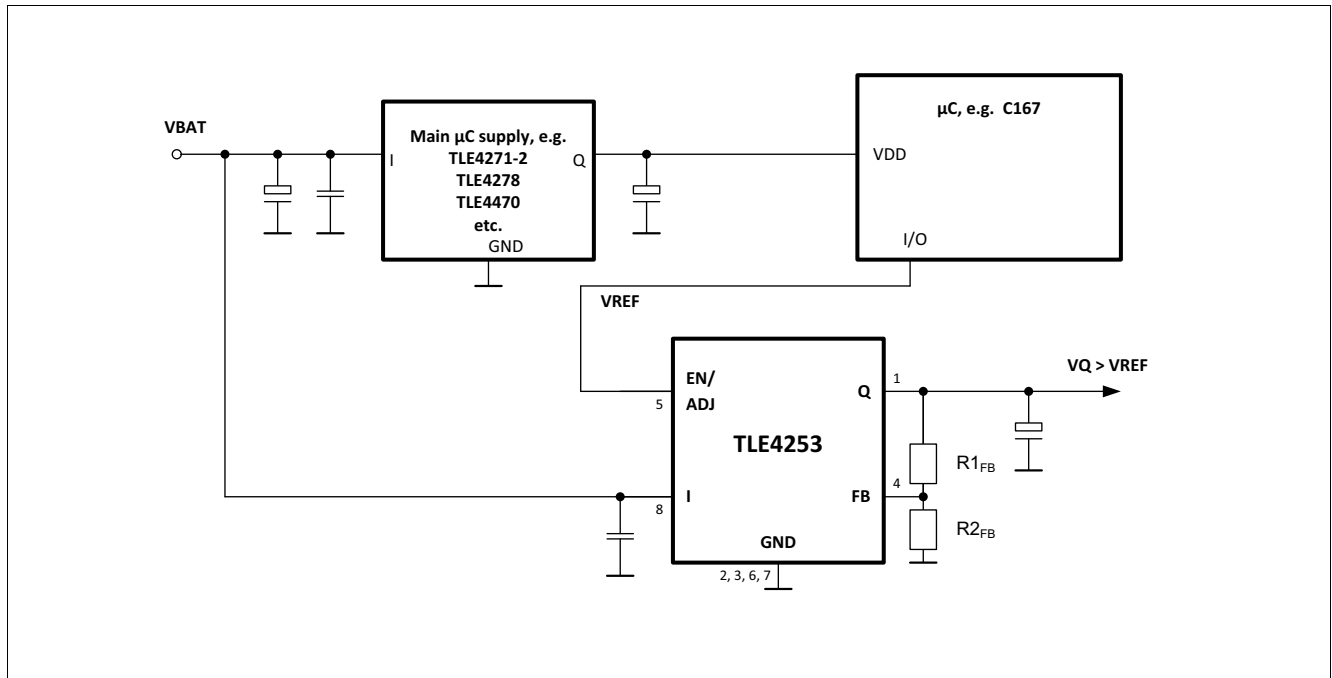
With a given reference voltage  $V_{REF}$ , the desired output voltage  $V_Q$  and the resistor value  $R1_{ADJ}$ , the resistor value for  $R2_{ADJ}$  is given by:

$$R2_{ADJ} = R1_{ADJ} \cdot \left( \frac{V_Q}{V_{REF} - V_Q} \right) \quad (5.2)$$

Taking into consideration also the effect of the internal EN/ADJ pull-down resistor, the external resistor divider's  $R2_{ADJ}$  has to be selected to:

$$R2_{ADJ,select} = \left( \frac{R2_{ADJ} \cdot R_{PullDown,min}}{R_{PullDown,min} - R2_{ADJ}} \right) \quad (5.3)$$

**Application information**



**Figure 5 Application circuit: Output voltage  $V_Q$  higher than reference voltage  $V_{REF}$**

For output voltages higher than the reference voltage, the voltage divider has to be applied between the feedback and the output according to **Figure 5**. The equation for the output voltage with respect to the reference voltage is given by:

(5.4)

$$V_Q = V_{REF} \cdot \left( \frac{R1_{FB} + R2_{FB}}{R2_{FB}} \right)$$

Keep in mind that the input voltage has to be at minimum equal to the output voltage plus the dropout voltage of the regulator.

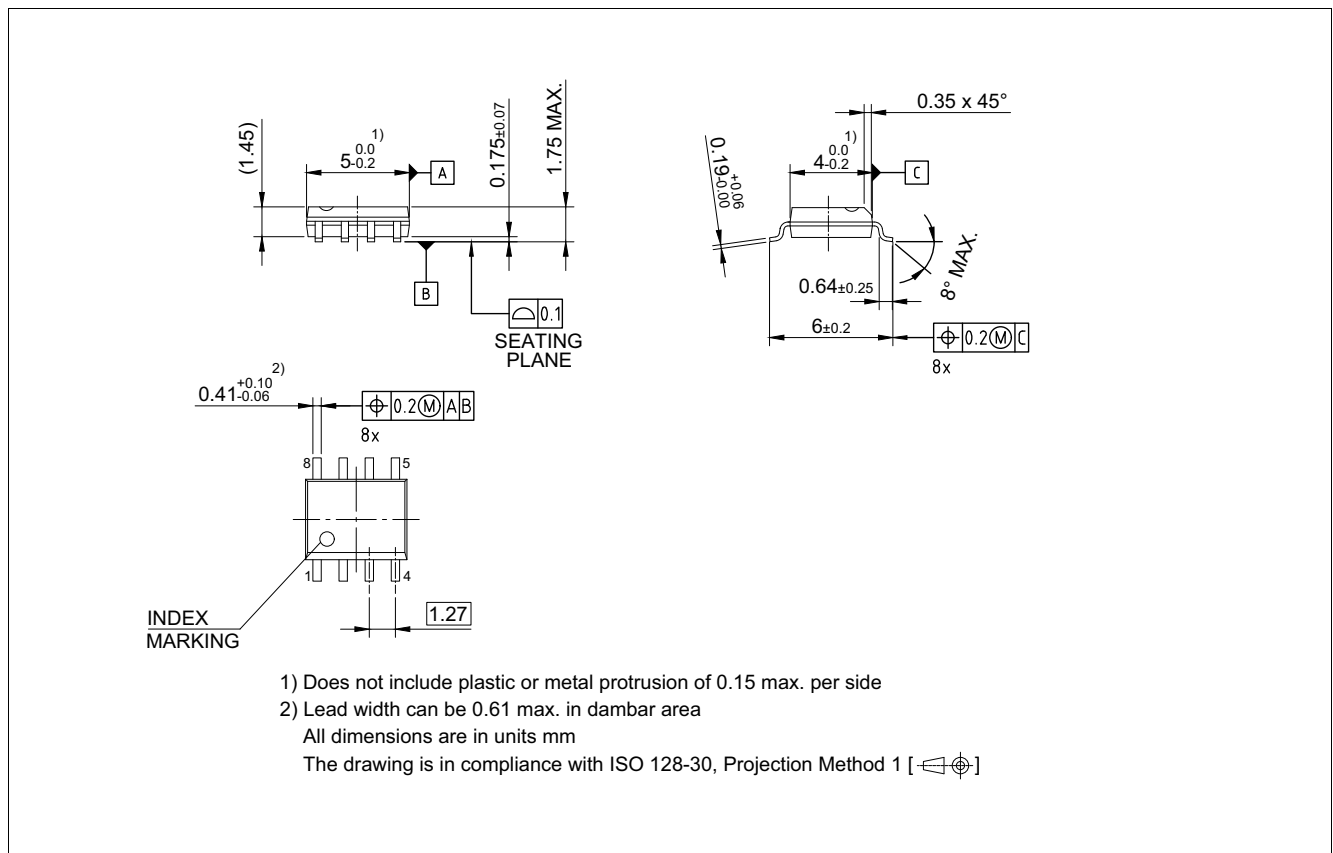
With a given reference voltage  $V_{REF}$ , the desired output voltage  $V_Q$  and the resistor value  $R1_{FB}$ , the resistor value for  $R2_{FB}$  is given by:

(5.5)

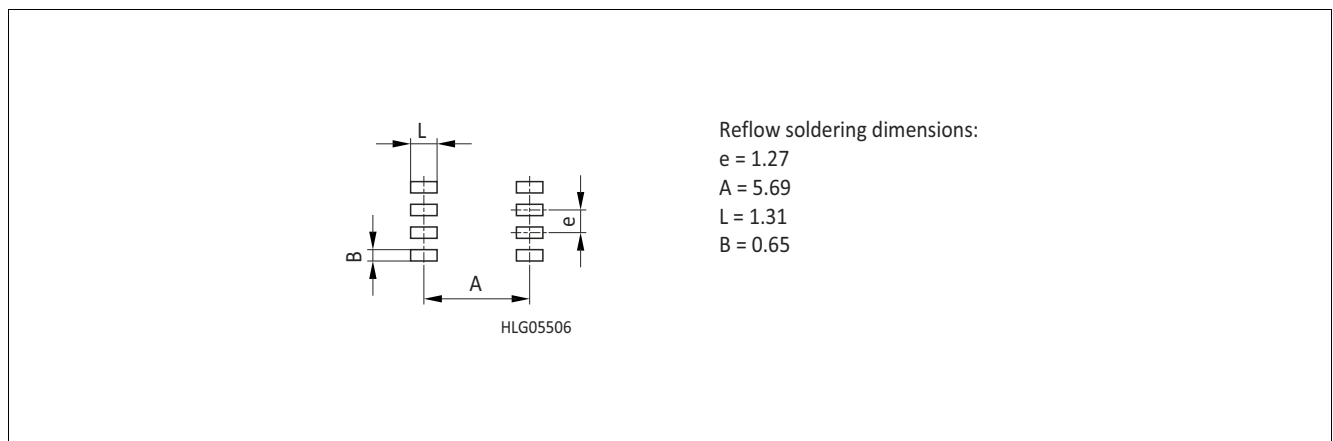
$$R2_{FB} = R1_{FB} \cdot \left( \frac{V_{REF}}{V_Q - V_{REF}} \right)$$

**Package outlines**

**6 Package outlines**



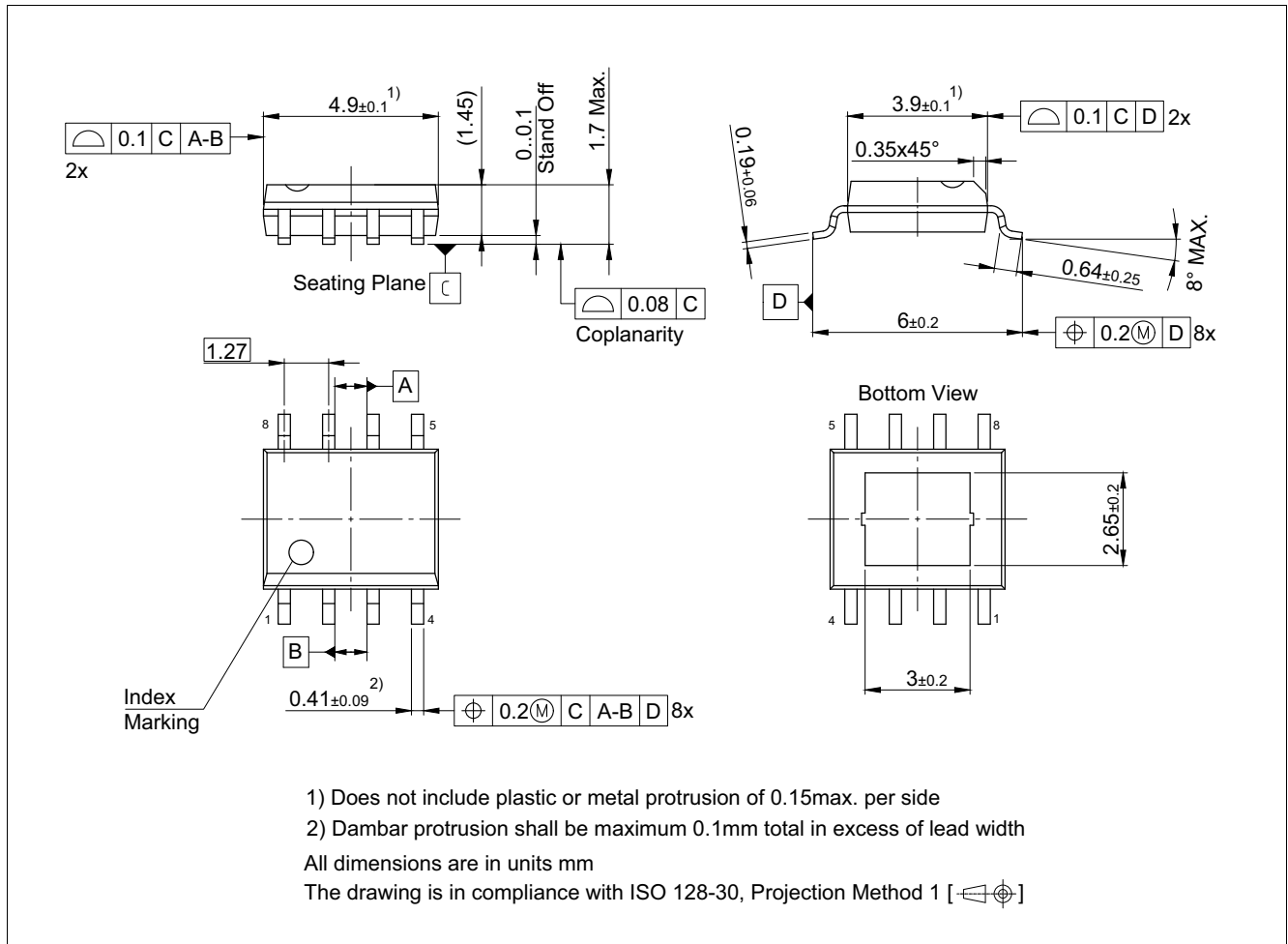
**Figure 6 Outline PG-DSO-8<sup>1)</sup>**



**Figure 7 Footprint PG-DSO-8<sup>1)</sup>**

1) Dimensions in mm.

**Package outlines**



**Figure 8 Outline and footprint PG-DSO-8 exposed pad (exposed pad)<sup>1)</sup>**

**Green product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Further information on packages**

<https://www.infineon.com/packages>

1) Dimensions in mm.

Revision history

## 7 Revision history

| Revision | Date       | Changes  |
|----------|------------|--|
| 1.21     | 2021-04-20 | <p>Editorial changes.</p> <p>Correct “Non inverting” to “Inverting” in the description of the <b>FB</b> pin in <b>“Pin definitions and functions” on Page 5</b>.</p> <p>Assigned the parameter <b>“Adjust / enable input voltage (voltage tracking range)” on Page 7</b> the number P_4.2.5.</p> <p>Split the previous figure 6 into <b>Figure 6 “Outline PG-DSO-8” on Page 21</b> and <b>Figure 7 “Footprint PG-DSO-81” on Page 21</b>. (The old figure 7 is now <b>Figure 8 “Outline and footprint PG-DSO-8 exposed pad (exposed pad)” on Page 22</b>.)</p>  |
| 1.2      | 2009-11-09 | <p>Updated Version Data Sheet, version TLE4253E in PG-DSO-8 exposed pad and all related description added:</p> <p>In <b>“Features” on Page 1</b> picture for package PG-DSO-8 updated</p> <p>In <b>“Features” on Page 1</b> “package” replaced by “packages”</p> <p>In <b>“Description” on Page 1</b> “a small PG-DSO-8 package” replaced by “small PG-DSO-8 packages”; “The exposed pad (EP) package variant PG-DSO-8 exposed pad offers extremely low thermal resistance.” added; “suits” replaces by “makes”</p> <p>In <b>“Pin assignment” on Page 5</b>, package PG-DSO-8 exposed pad added</p> <p>In <b>“Pin definitions and functions” on Page 5</b> all definition for package PG-DSO-8 exposed pad added</p> <p>In <b>“Thermal resistance” on Page 8</b> all values for package PG-DSO-8 exposed pad added (P_4.3.6 - P_4.3.10)</p> <p>In <b>“Adjust / enable input” on Page 17</b> typo corrected: “resistors” replaced by “resistor”</p> <p>In <b>“Package outlines” on Page 21</b> package PG-DSO-8 exposed pad added</p> |
| 1.1      | 2008-08-19 | <p>Updated Version Final Datasheet for TLE4253GS:</p> <p><b>“Package outlines” on Page 21</b> updated;</p> <p>In <b>“Typical performance characteristics tracking regulator” on Page 16</b> Graph <b>“Current consumption Iq vs. input voltageVI” on Page 16</b> added</p>   |
| 1.0      | 2007-07-10 | <p>Initial Final Datasheet for TLE4253GS.</p> <p>For the TLE4253ES (exposed pad) product variant, please refer to the respective datasheet</p>   |

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**Z8F55248541**

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