

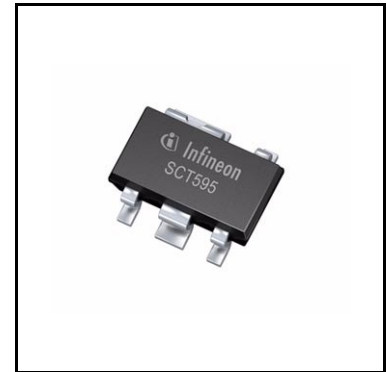
# OPTIREG™ linear TLE4294GV50

## Low dropout voltage regulator



### Features

- Output voltage tolerance  $\leq \pm 4\%$
- Very low drop out voltage
- Output current: 30 mA
- Low quiescent current consumption
- Wide operating range up to 45 V
- Wide temperature range:  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$
- Output protected against short circuit
- Overtemperature protection
- Reverse polarity protection
- Very small SMD package PG-SCT595-5
- Green Product (RoHS compliant)



### Potential applications

General automotive applications.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The OPTIREG™ linear TLE4294GV50 is a monolithic integrated low drop out voltage regulator in a very small SMD package PG-SCT595-5. It is designed to supply e.g. microcontroller systems under severe conditions. Therefore the device is equipped with additional protection functions against overload, short circuit and reverse polarity. In case of an overtemperature condition the regulator is automatically turned off by the integrated thermal protection circuit.

Input voltages up to 40 V are regulated to  $V_{Q,nom} = 5.0\text{ V}$ . The output is able to drive a load of more than 30 mA, while it regulates the output voltage within a 4% accuracy.

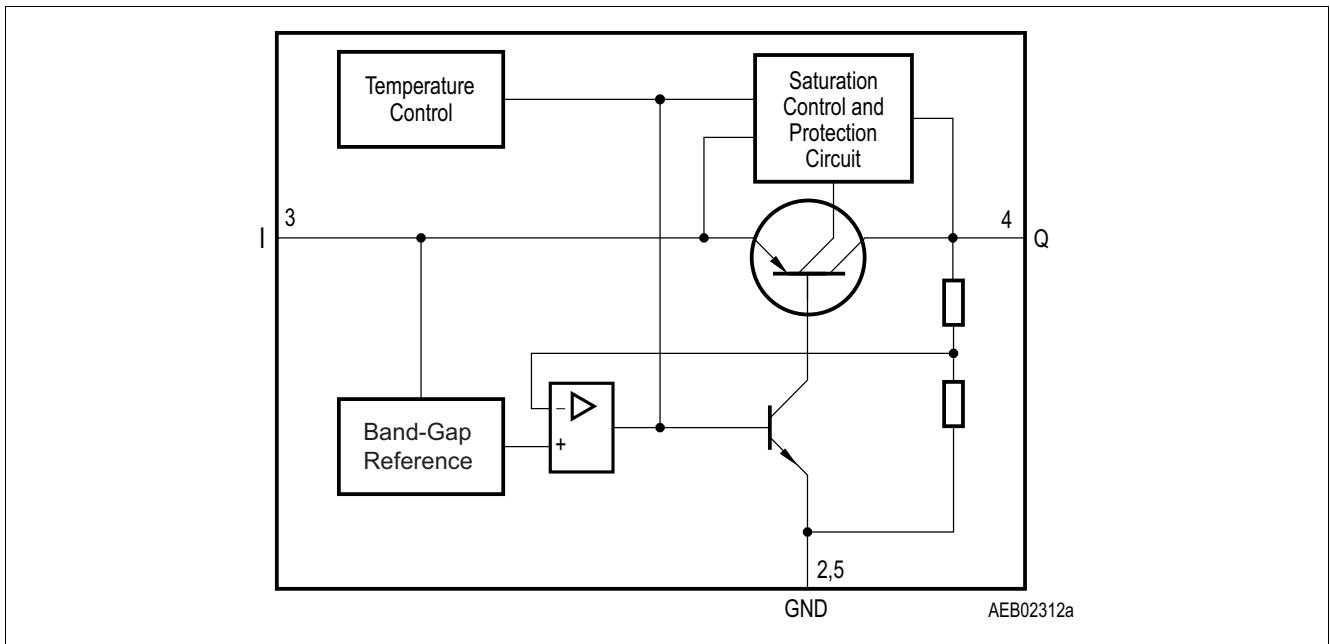
Type	Package	Marking
TLE4294GV50	PG-SCT595-5	F1

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**Block diagram**

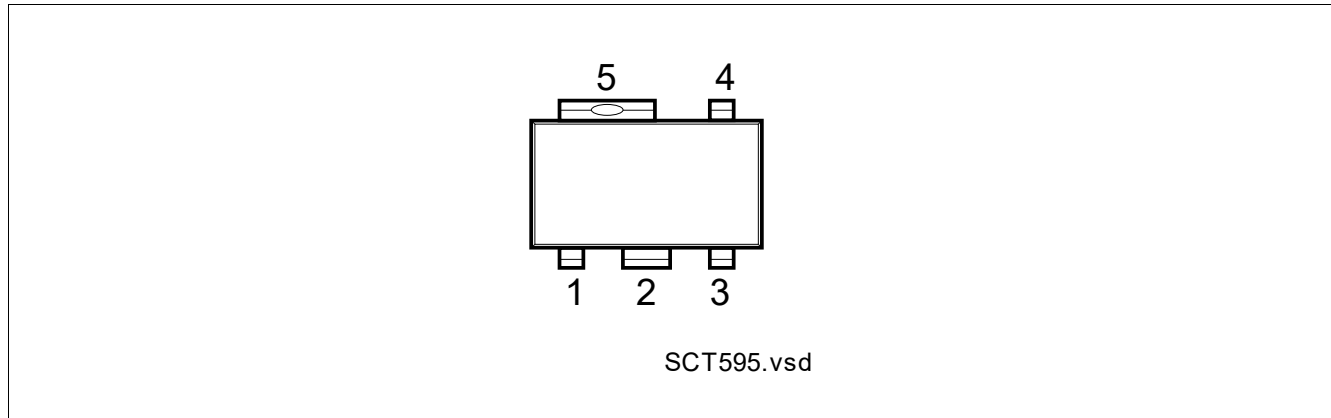
**1 Block diagram**



**Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment**



**Figure 2 Pin configuration (top view)**

**2.2 Pin definitions and functions**

**Table 1 Pin definitions and functions**

Pin	Symbol	Function
1	N.C.	<b>Not connected</b> Internally not connected. Connect to GND.
2	GND	<b>Ground</b> Connected to pin 5.
3	I	<b>Input voltage</b> For compensating line influences, a capacitor to GND close to the IC terminals is recommended.
4	Q	<b>Output voltage</b> Block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C <sub>Q</sub> and ESR in the <a href="#">Table 3 “Functional range” on Page 6</a> (Tantalum capacitor recommended as output capacitor).
5	GND	<b>Ground</b> Connect to heatsink area; Connected to pin 2.

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground, direction of currents as shown in **Figure 3** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input</b>							
Voltage	$V_I$	-42	–	45	V	–	P_3.1.1
Current	$I_I$	–	–	–	mA	<sup>2)</sup>	P_3.1.2
<b>Output</b>							
Voltage	$V_Q$	-6	–	30	V	–	P_3.1.3
Current	$I_Q$	–	–	–	mA	<sup>2)</sup>	P_3.1.4
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	–	150	°C	–	P_3.1.5
Storage temperature	$T_{stg}$	-50	–	150	°C	–	P_3.1.6
<b>ESD susceptibility</b>							
ESD resistivity	$V_{ESD}$	-2	–	2	kV	HBM <sup>3)</sup>	P_3.1.7
ESD resistivity to GND	$V_{ESD}$	-750	–	750	V	CDM <sup>4)</sup>	P_3.1.8

1) Not subject to production test, specified by design.

2) Internally limited.

3) ESD susceptibility, Human Body Model “HBM” according to EIA/JESD 22-A114B.

4) ESD susceptibility, Charged Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1.

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**General product characteristics**

**3.2 Functional range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Inhibit voltage	$V_I$	5.5	–	45	V	–	P_3.2.1
Output capacitor requirements	$C_Q$	2.2	–	–	$\mu\text{F}$	–	P_3.2.2
	$ESR_{CQ}$	1.5	–	8	$\Omega$	1)	P_3.2.3
Junction temperature	$T_j$	-40	–	150	$^{\circ}\text{C}$	–	P_3.2.4

1) Equivalent series resistance measured at a frequency of 10 kHz.

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

**3.3 Thermal resistance**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to ambient <sup>1)</sup>	$R_{thJA}$	–	179	–	K/W	Footprint only <sup>2)</sup>	P_3.3.1
		–	99	–	K/W	300 mm <sup>2</sup> heat sink area on PCB <sup>2)</sup>	P_3.3.2
		–	87	–	K/W	600 mm <sup>2</sup> heat sink area on PCB <sup>2)</sup>	P_3.3.3
		–	80	–	K/W	2s2p PCB <sup>3)</sup>	P_3.3.4
Junction to soldering point	$R_{thJSP}$	–	26	–	K/W	Measured to pin 5	P_3.3.5

1) Not subject to production test, specified by design.

2) EIA/JESD 52\_2, FR4, 80 x 80 x 1.5 mm; 35 $\mu$  Cu, 5 $\mu$  Sn.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70  $\mu\text{m}$  Cu, 2 x 35 $\mu\text{m}$  Cu).

**Electrical characteristics**

**4 Electrical characteristics**

**4.1 Electrical characteristics**

**Table 5 Electrical characteristics**

$V_I = 13.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground, direction of currents as shown in **Figure 3** (unless otherwise specified)

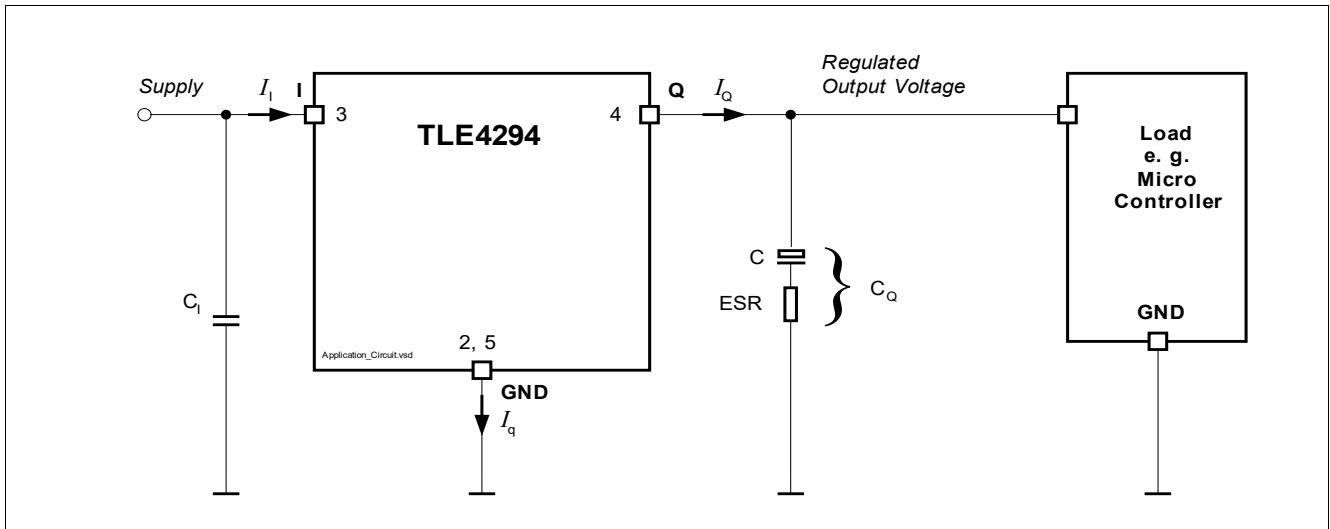
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Output</b>							
Output voltage	$V_Q$	4.80	5.00	5.20	V	$1\text{ mA} \leq I_Q < 30\text{ mA}$ ; $V_I < 13.5\text{ V}$	P_4.1.1
Output voltage	$V_Q$	4.80	5.00	5.20	V	$I_Q = 10\text{ mA}$ ; $6\text{ V} < V_I < 40\text{ V}$	P_4.1.2
Output current limitation	$I_Q$	30	–	–	mA	<sup>1)</sup>	P_4.1.3
Drop out voltage	$V_{dr}$	–	0.25	0.40	V	$I_Q = 20\text{ mA}^{1)}$	P_4.1.4
<b>Current consumption</b>							
Current consumption $I_q = I_I - I_Q$	$I_q$	–	2	4	mA	$I_Q < 30\text{ mA}$	P_4.1.5
Current consumption $I_q = I_I - I_Q$	$I_q$	–	120	200	$\mu\text{A}$	$I_Q < 1\text{ mA}$	P_4.1.6
<b>Regulator performance</b>							
Load regulation	$ \Delta V_Q $	–	10	25	mV	$1\text{ mA} < I_Q < 25\text{ mA}$ ; $T_j = 25^\circ\text{C}$ ;	P_4.1.7
Load regulation	$ \Delta V_Q $	–	10	30	mV	$1\text{ mA} < I_Q < 25\text{ mA}$ ;	P_4.1.8
Line regulation	$ \Delta V_Q $	–	5	25	mV	$\Delta V_I = V_{I,min}$ to $36\text{ V}$ ; $I_Q = 5\text{ mA}$ ; $T_j = 25^\circ\text{C}$	P_4.1.9
Line regulation	$ \Delta V_Q $	–	10	30	mV	$\Delta V_I = V_{I,min}$ to $36\text{ V}$ ; $I_Q = 5\text{ mA}$ ;	P_4.1.10
Power supply ripple rejection	$PSRR$	–	60	–	dB	$f_r = 100\text{ Hz}$ ; $V_r = 0.5\text{ Vpp}$	P_4.1.11

1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value.

**Application information**

**5 Application information**

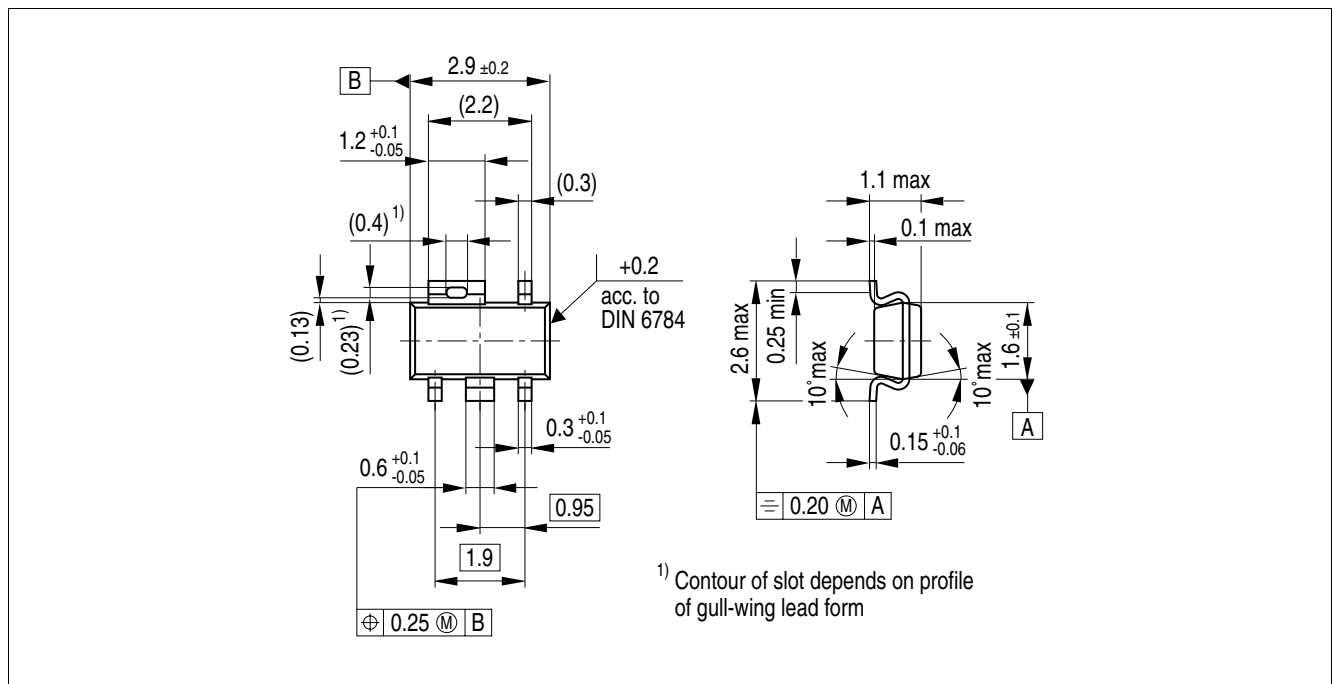
*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 3 Application diagram**



## 6 Package information



**Figure 4 PG-SCT595-5<sup>1)</sup>**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.2	2021-04-28	Updated layout and structure Editorial changes added TOC
1.1	2008-02-26	Device marking changed to F1
1.0	2004-01-01	Initial release

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