

# OPTIREG™ Linear TLE4299V33

## Low drop fixed voltage regulator



### Features

- Output voltage  $3.3\text{ V} \pm 2\%$
- 150 mA Output current
- Extreme low current consumption in ON state
- Inhibit function: Below  $1\ \mu\text{A}$  current consumption in off mode
- Early warning
- Reset output low down to  $V_Q = 1\text{ V}$
- Overtemperature protection
- Reverse polarity proof
- Wide temperature range
- Green Product (RoHS compliant)

### Potential applications

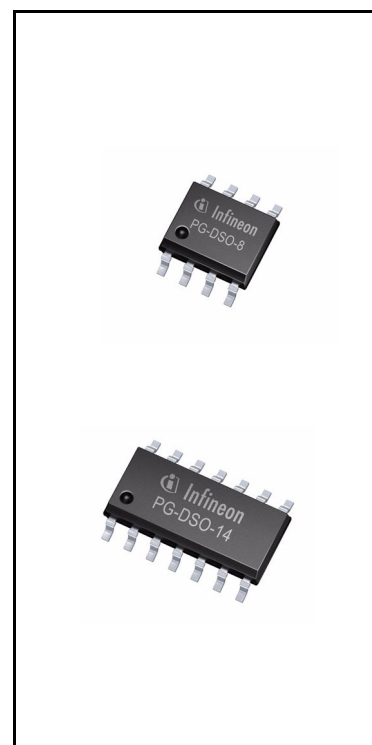
General automotive applications.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The OPTIREG™ Linear TLE4299V33 is a monolithic voltage regulator with fixed 3.3 V output, supplying loads up to 150 mA. It is especially designed for applications that may not be powered down while the motor is off. In addition the TLE4299GMV33 includes an inhibit function. When the inhibit signal is removed, the device is switched off and the quiescent current is less than  $1\ \mu\text{A}$ . To achieve proper operation of the  $\mu$ -controller, the device supplies a reset signal. The reset delay time is selected application-specific by an external delay capacitor. The reset threshold is adjustable. An early warning signal supervises the voltage at pin SI. The TLE4299V33 is pin-compatible to the TLE4269 and functional similar with the additional inhibit function. The TLE4299V33 is designed to supply microcontroller systems even under automotive environment conditions. Therefore it is protected against overload, short circuit and overtemperature.



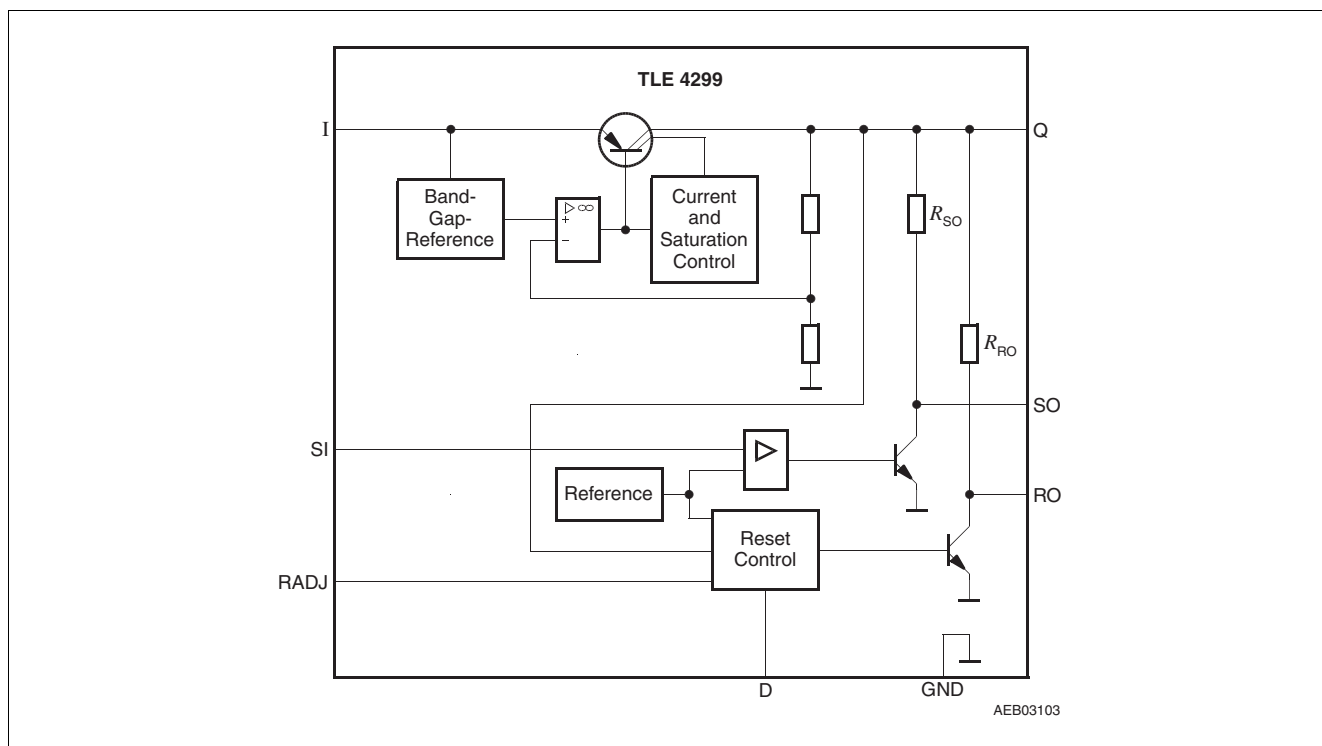
Type	Package	Marking
TLE4299GV33	PG-DSO-8	4299V33
TLE4299GMV33	PG-DSO-14	4299V33

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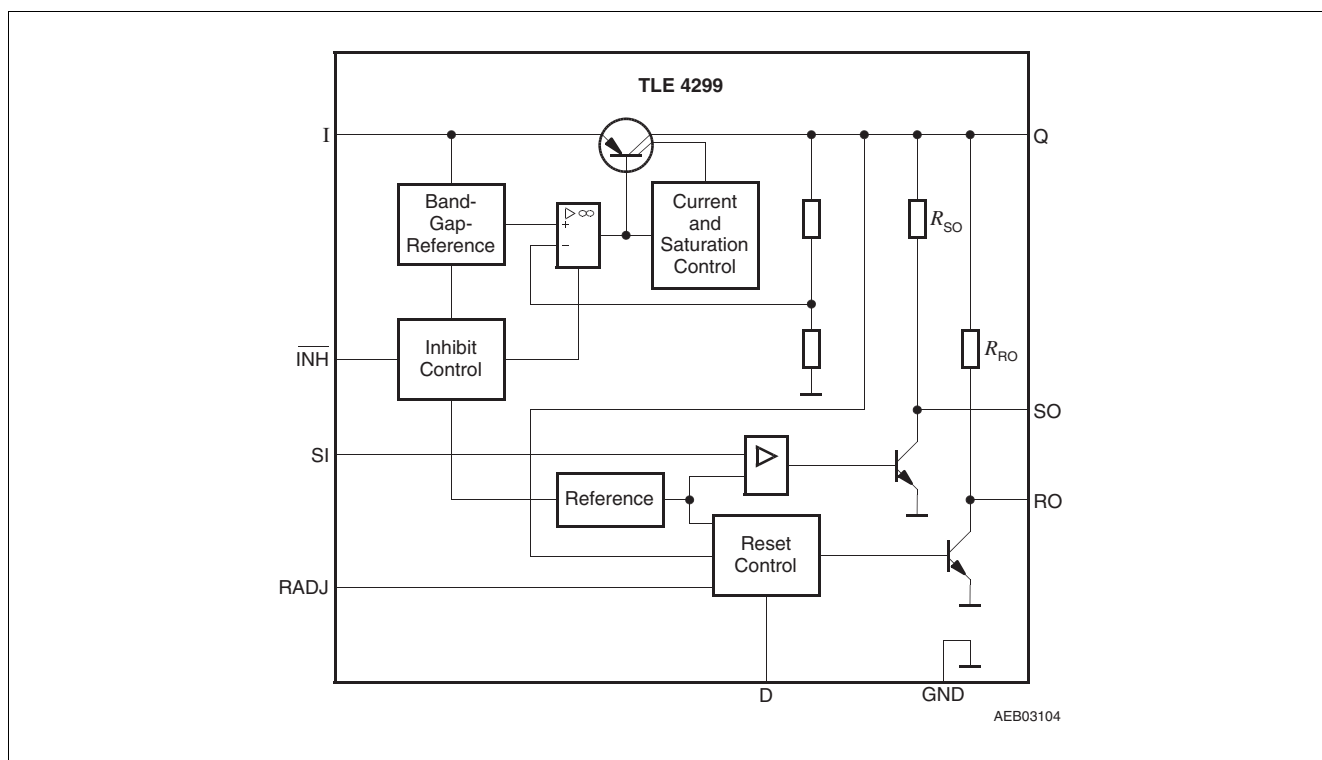
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**Block diagram**

**1 Block diagram**



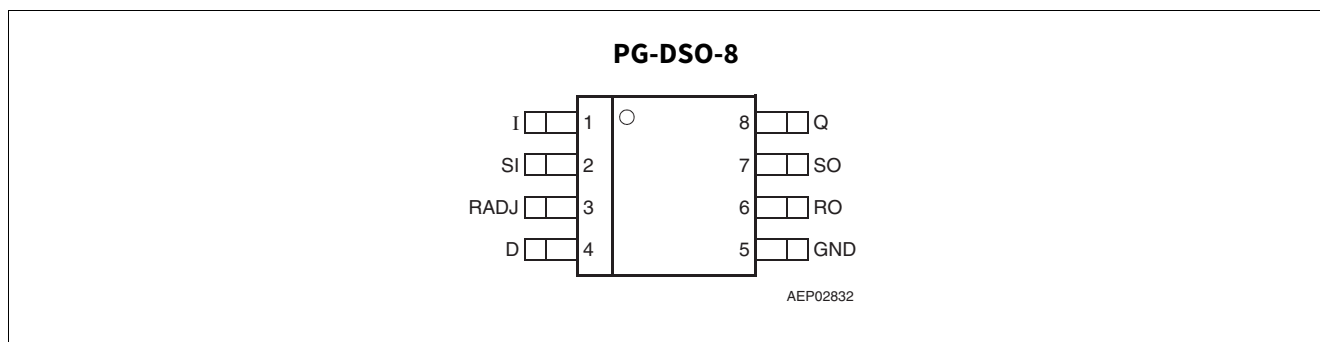
**Figure 1 Block diagram TLE4299GV33**



**Figure 2 Block diagram TLE4299GMV33**

**Pin configuration**

**2 Pin configuration**



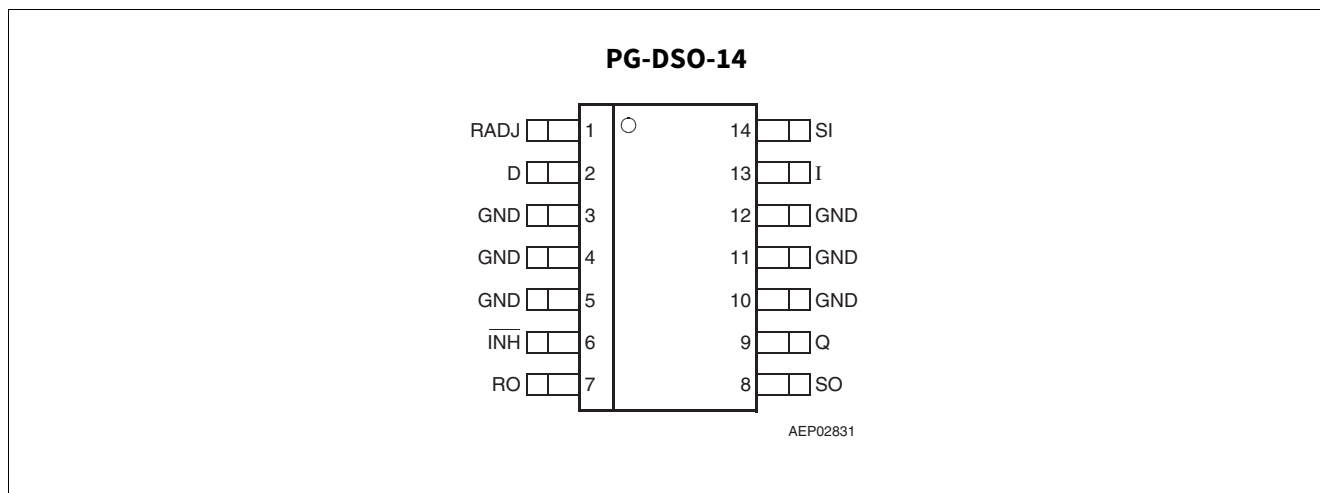
**Figure 3** Pin configuration PG-DSO-8 (top view)

**Table 1** Pin definitions and functions (TLE4299GV33)

Pin No.	Symbol	Function
1	I	<b>Input;</b> block directly to GND on the IC with a ceramic capacitor.
2	SI	<b>Sense input;</b> if not needed connect to Q.
3	RADJ	<b>Reset threshold adjust;</b> if not needed connect to GND.
4	D	<b>Reset delay;</b> to select delay time, connect to GND via external capacitor.
5	GND	<b>Ground</b>
6	RO	<b>Reset output;</b> the open-collector output is linked internally to Q via a 20 kΩ pull-up resistor. Keep open, if the pin is not needed.
7	SO	<b>Sense output;</b> open-collector output. Keep open, if the pin is not needed.
8	Q	<b>Output;</b> connect to GND with a 22 μF capacitor, $0.4 \Omega < \text{ESR} < 3.7 \Omega$ . <sup>1)</sup>

1) See characteristic curves.

**Pin configuration**



**Figure 4** Pin configuration PG-DSO-14 (top view)

**Table 2** Pin definitions and functions (TLE4299GMV33)

Pin No.	Symbol	Function
1	RADJ	<b>Reset threshold adjust</b> ; if not needed connect to GND.
2	D	<b>Reset delay</b> ; connect to GND via external delay capacitor for setting delay time.
3, 4, 5	GND	<b>Ground</b>
6	$\overline{\text{INH}}$	<b>Inhibit</b> ; if not needed connect to Input pin I; A high signal switches the regulator ON.
7	RO	<b>Reset output</b> ; the open-collector output is linked internally to Q via a 20 k $\Omega$ pull-up resistor. Keep open, if the pin is not needed.
8	SO	<b>Sense Output</b> ; open-collector output. Keep open, if the pin is not needed.
9	Q	<b>Output</b> ; connect to GND with a 22 $\mu\text{F}$ capacitor, $0.4 \Omega < \text{ESR} < 3.7 \Omega$ . <sup>1)</sup>
10, 11, 12	GND	<b>Ground</b>
13	I	<b>Input</b> ; block to GND directly at the IC by a ceramic capacitor.
14	SI	<b>Sense input</b> ; if not needed connect to Q.

1) See characteristic curves.

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 3 Absolute maximum ratings**

-40°C ≤ T<sub>j</sub> ≤ 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>Input I</b>						
Input voltage	V <sub>I</sub>	-40	-	45	V	-
<b>Inhibit input <math>\overline{\text{INH}}</math></b>						
Input voltage	V <sub>INH</sub>	-40	-	45	V	-
<b>Sense input SI</b>						
Input voltage	V <sub>SI</sub>	-0.3	-	45	V	-
Input current	I <sub>SI</sub>	-1	-	1	mA	-
<b>Reset threshold adjust RADJ</b>						
Input voltage	V <sub>RADJ</sub>	-0.3	-	7	V	-
Input current	I <sub>RADJ</sub>	-10	-	10	mA	-
<b>Reset delay D</b>						
Voltage	V <sub>D</sub>	-0.3	-	7	V	-
<b>Reset output RO</b>						
Voltage	V <sub>R</sub>	-0.3	-	7	V	-
<b>Sense output SO</b>						
Voltage	V <sub>SO</sub>	-0.3	-	7	V	-
<b>Output Q</b>						
Output voltage	V <sub>Q</sub>	-0.3	-	7	V	-
Output current	I <sub>Q</sub>	-5	-	-	mA	-
<b>Temperature</b>						
Junction temperature	T <sub>j</sub>	-	-	150	°C	-
Storage temperature	T <sub>Stg</sub>	-50	-	150	°C	-
<b>Operating range</b>						
Input voltage	V <sub>I</sub>	4.4	-	45	V	-
Junction temperature	T <sub>j</sub>	-40	-	150	°C	-

**General product characteristics**

**Table 3 Absolute maximum ratings (cont'd)**

$-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>Thermal data</b>						
Junction-ambient for foot print only <sup>1)</sup>	$R_{thja}$	–	–	200	K/W	PG-DSO-8
				130	K/W	PG-DSO-14
Junction-ambient for 300 mm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thja}$	–	–	164	K/W	PG-DSO-8
				70	K/W	PG-DSO-14
Junction-pin	$R_{thjp}$	–	–	60	K/W	PG-DSO-8 <sup>3)</sup>
				30	K/W	PG-DSO-14 <sup>4)</sup>

1) FR4, 80 × 80 × 1,5 mm; 35 μm Cu, 5 μm Sn; Footprint only.

2) FR4, 80 × 80 × 1,5 mm; 35 μm Cu, 5 μm Sn; 300 mm<sup>2</sup>.

3) Measured to pin 5.

4) Measured to pin 4.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. In the operating range, the functions given in the circuit description are fulfilled.*

**Functional description**

## **4 Functional description**

The TLE4299V33 is a PNP based very low drop linear voltage regulator. It regulates the output voltage to  $V_Q = 3.3\text{ V}$  for an input voltage range of  $4.4\text{ V} \leq V_I \leq 45\text{ V}$ . The control circuit protects the device against potential damages caused by overcurrent and overtemperature. The internal control circuit achieves a 3.3 V output voltage with a tolerance of  $\pm 2\%$ .

The device includes a power on reset and an undervoltage reset function with adjustable reset delay time and adjustable reset switching threshold as well as a sense control/early warning function. The device includes an inhibit function to disable it when the ECU is not used for example while the motor is off.

The reset logic compares the output voltage  $V_Q$  to an internal threshold. If the output voltage drops below this level, the external reset delay capacitor  $C_D$  is discharged. When  $V_D$  is lower than  $V_{ST}$ , the reset output RO is switched “low”. If the output voltage drop is very short, the  $V_{ST}$  level is not reached and no reset-signal is asserted. This feature avoids resets at short negative spikes at the output voltage e.g. caused by load changes. As soon as the output voltage is more positive than the reset threshold, the delay capacitor is charged with constant current. When the voltage reaches  $V_{DT}$  the reset output RO is set “high” again.

The reset delay time and the reset reaction time are defined by the external capacitor  $C_D$ . The reset function is active down to  $V_I = 1\text{ V}$ .

In addition to the normal reset function, the device gives an early warning. When the SI voltage drops below  $V_{SI,low}$ , the device asserts the SI output “low” to indicate the logic and the  $\mu$ -processor that this voltage has dropped. The sense function uses a hysteresis: When the SI-voltage reaches the  $V_{SI,high}$  level, SO is set “high” again. This feature can be used as early warning function to notice the  $\mu$ -controller about a battery voltage drop and a possible reset in a short time. Of course also any other voltage can be observed by this feature.

The user defines the threshold by the resistor-values  $R_{SI1}$  and  $R_{SI2}$ .

For the exact timing and calculation of the reset and sense timing and thresholds, please refer to the application section.



**Functional description**

**4.1 Electrical characteristics**

**Table 4 Electrical characteristics**

$V_1 = 13.5\text{ V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage	$V_Q$	3.23	3.30	3.37	V	$1\text{ mA} \leq I_Q \leq 100\text{ mA}$ ; $5.5\text{ V} \leq V_1 \leq 16\text{ V}$
Output voltage	$V_Q$	3.20	3.30	3.40	V	$I_Q \leq 150\text{ mA}$ ; $5.5\text{ V} \leq V_1 \leq 16\text{ V}$
Current limit	$I_Q$	250	400	500	mA	–
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	65	105	$\mu\text{A}$	Inhibit ON; $I_Q \leq 1\text{ mA}$ , $T_j < 85^\circ\text{C}$
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	170	500	$\mu\text{A}$	Inhibit ON; $I_Q = 10\text{ mA}$
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	0.7	2	mA	Inhibit ON; $I_Q = 50\text{ mA}$
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	–	1	$\mu\text{A}$	$V_{\text{INH}} = 0\text{ V}$ ; $T_j = 25^\circ\text{C}$
Load regulation	$\Delta V_Q$	–	5	30	mV	$I_Q = 1\text{ mA}$ to $100\text{ mA}$
Line regulation	$\Delta V_Q$	–	10	25	mV	$V_1 = 6\text{ V}$ to $28\text{ V}$ ; $I_Q = 1\text{ mA}$
Power supply ripple rejection	$PSRR$	–	66	–	dB	$f_r = 100\text{ Hz}$ ; $V_r = 1\text{ V}_{\text{SS}}$ ; $I_Q = 100\text{ mA}$

**Inhibit (TLE4299GMV33 only)**

Inhibit OFF voltage range	$V_{\text{INH OFF}}$	–	–	0.8	V	$V_Q$ off
Inhibit ON voltage range	$V_{\text{INH ON}}$	3.5	–	–	V	$V_Q$ on
High input current	$I_{\text{INH ON}}$	–	3	5	$\mu\text{A}$	$V_{\text{INH}} = 5\text{ V}$
Low input current	$I_{\text{INH OFF}}$	–	0.5	2	$\mu\text{A}$	$V_{\text{INH}} = 0.8\text{ V}$

**Reset generator**

Switching threshold	$V_{\text{rt}}$	3.00	3.10	3.20	V	–
Reset threshold headroom	$V_{\text{RTHEAD}}$	50	200	300	mV	–
Reset pull up	$R_{\text{RO}}$	10	20	40	k $\Omega$	–
Reset low voltage	$V_{\text{R}}$	–	0.17	0.40	V	$V_Q < 3.0\text{ V}$ ; internal $R_{\text{RO}}$ ; $I_{\text{R}} = 1\text{ mA}$
External reset pull up	$V_{\text{R ext}}$	5.6	–	–	k $\Omega$	Pull up resistor Q
Delay switching threshold	$V_{\text{DT}}$	1.6	1.85	2.35	V	–
Switching threshold	$V_{\text{ST}}$	0.35	0.50	0.60	V	–
Reset delay low voltage	$V_{\text{D}}$	–	–	0.1	V	$V_Q < V_{\text{RT}}$
Charge current	$I_{\text{ch}}$	2.0	3.5	6.0	$\mu\text{A}$	$V_{\text{D}} = 1\text{ V}$
Power-up reset delay time	$t_{\text{d}}$	36	51	60	ms	$C_{\text{D}} = 100\text{ nF}$
Reset reaction time	$t_{\text{rr}}$	0.5	1.2	3.0	$\mu\text{s}$	$C_{\text{D}} = 100\text{ nF}$

**Functional description**

**Table 4 Electrical characteristics (cont'd)**

$V_i = 13.5\text{ V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reset adjust switching threshold	VRADJ TH	1.26	1.36	1.44	V	$V_Q < 3.5\text{ V}$

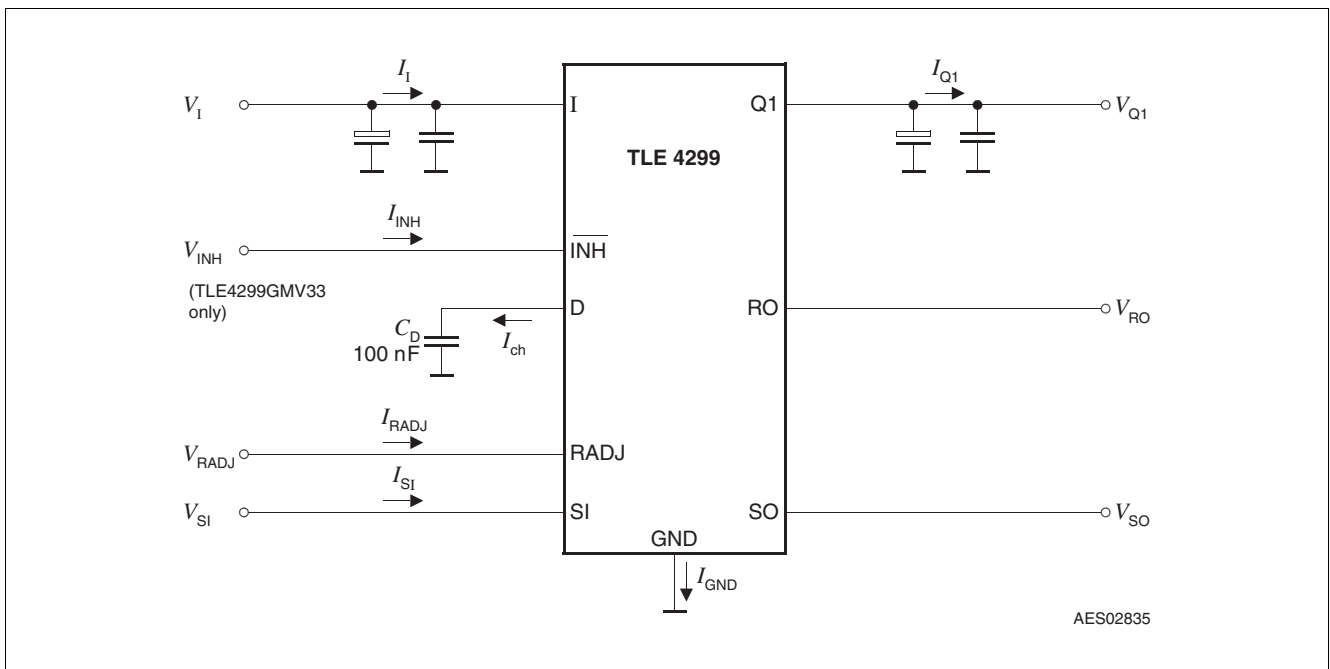
**Input voltage sense**

Sense threshold high	$V_{SI\ high}$	1.34	1.45	1.54	V	–
Sense threshold low	$V_{SI\ low}$	1.26	1.36	1.44	V	–
Sense input switching hysteresis	$V_{SI\ HYST}$	50	90	130	mV	$V_{SI\ HYST} = V_{SI\ high} - V_{SI\ low}$
Sense output low voltage	$V_{SO\ low}$	–	0.1	0.4	V	$V_{SI} < 1.20\text{ V}$ ; $V_i > 4.2\text{ V}$ ; $I_{SO} = 1\text{ mA}$
External SO pull up resistor	$R_{SO\ ext}$	5.6	–	–	k $\Omega$	–
Sense input current	$I_{SI}$	-1	0.1	1	$\mu\text{A}$	$S_i > 1.0\text{ V}$
Sense high reaction time	$t_{pd\ SO\ LH}$	–	2.4	4.0	$\mu\text{s}$	$R_{SO\ ext} = 5.6\text{ k}\Omega$
Sense low reaction time	$t_{pd\ SO\ HL}$	–	2.5	6.0	$\mu\text{s}$	$R_{SO\ ext} = 5.6\text{ k}\Omega$

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ\text{C}$  and the given supply voltage.*

**Functional description**

**4.2 Test circuit**

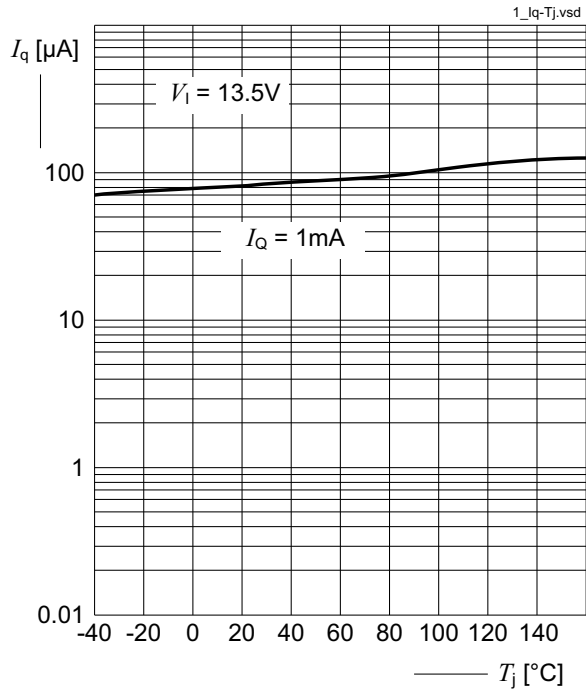


**Figure 5 Measurement circuit**

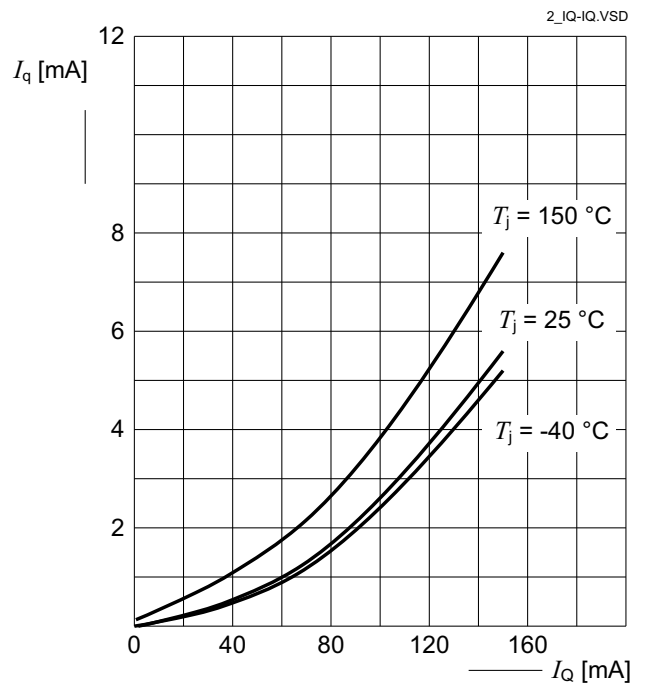
**Functional description**

**4.3 Typical performance characteristics**

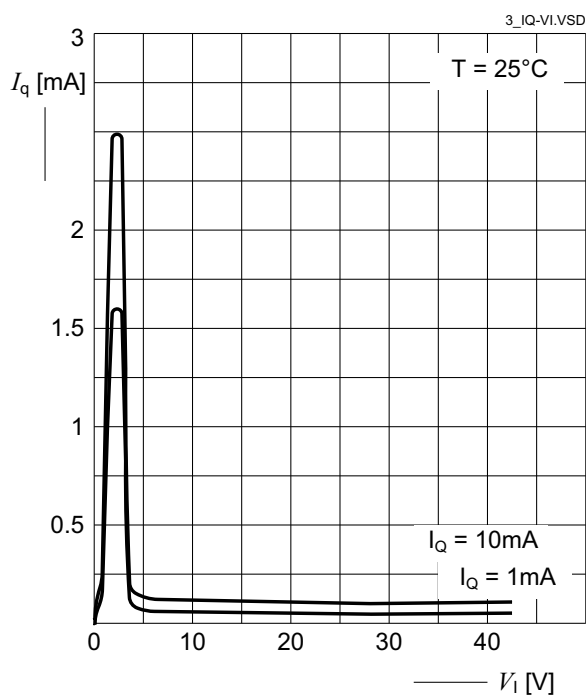
**Current consumption  $I_q$  versus junction temperature  $T_j$**



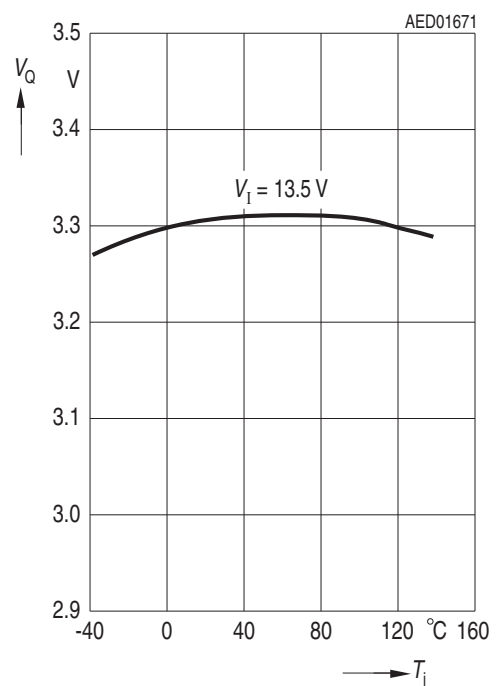
**Current consumption  $I_q$  versus output current  $I_Q$**



**Current consumption  $I_q$  versus input voltage  $V_i$**

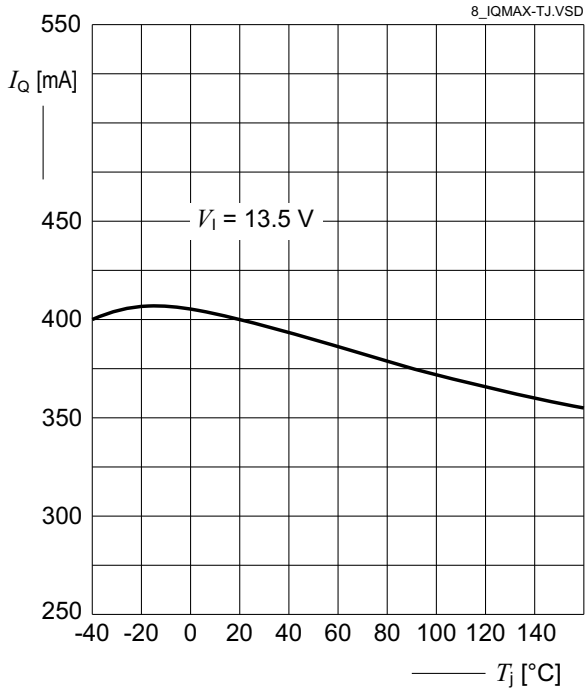


**Output voltage  $V_Q$  versus junction temperature  $T_j$**

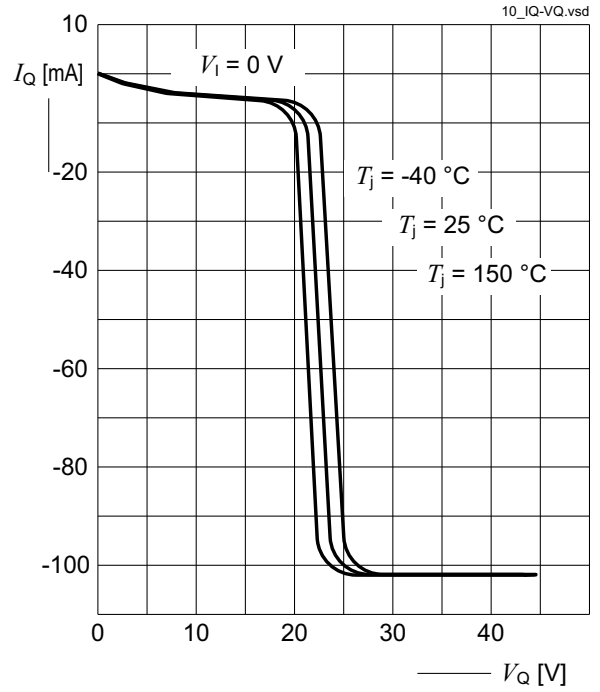


**Functional description**

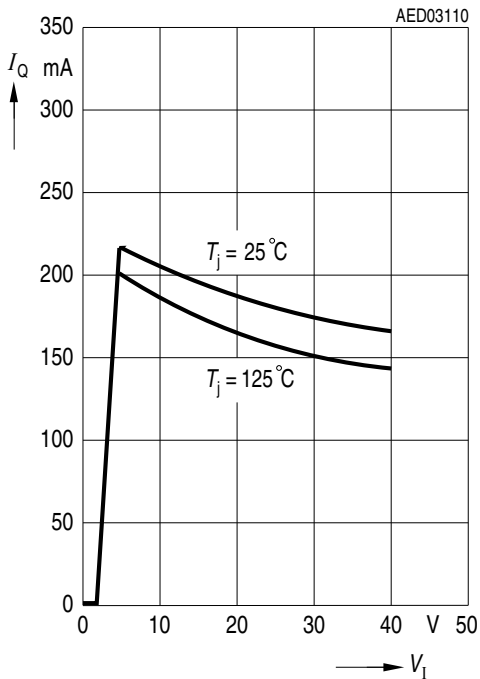
**Maximum output current  $I_Q$  versus junction temperature  $T_j$**



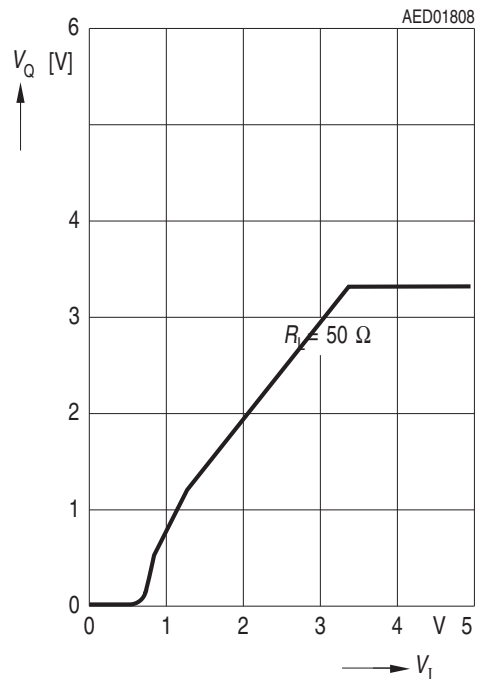
**Reverse output current  $I_Q$  versus output voltage  $V_Q$**



**Maximum output current  $I_Q$  versus input voltage  $V_I$**

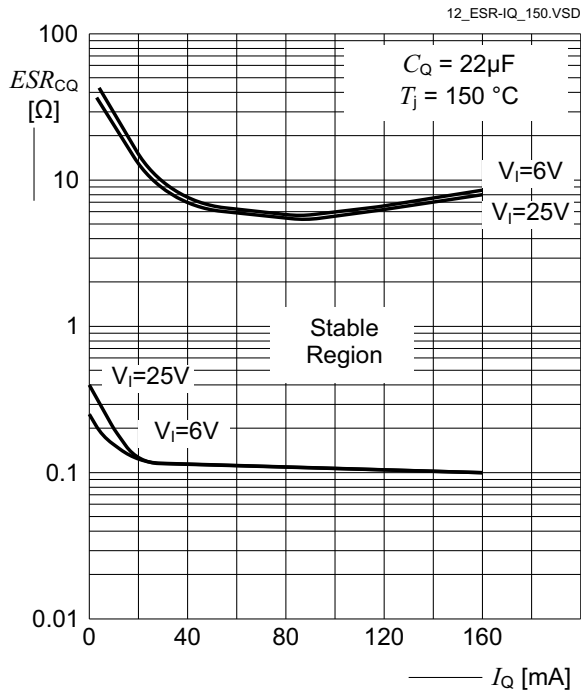


**Output voltage  $V_Q$  at input voltage extremes**

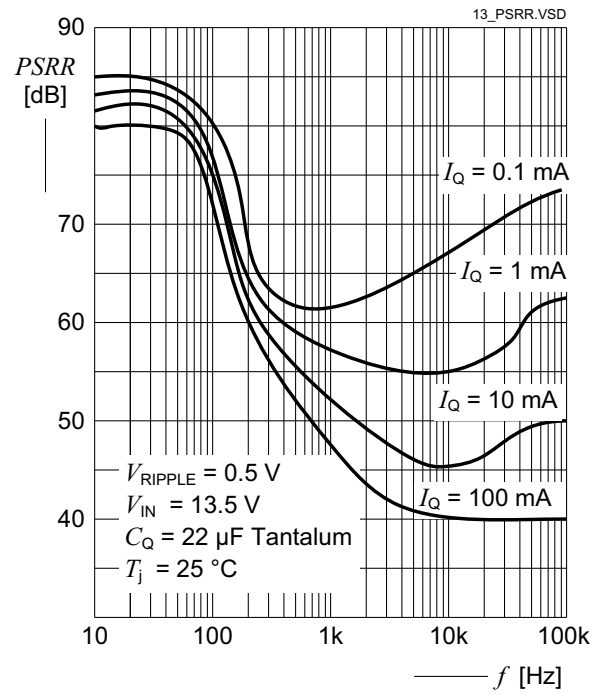


**Functional description**

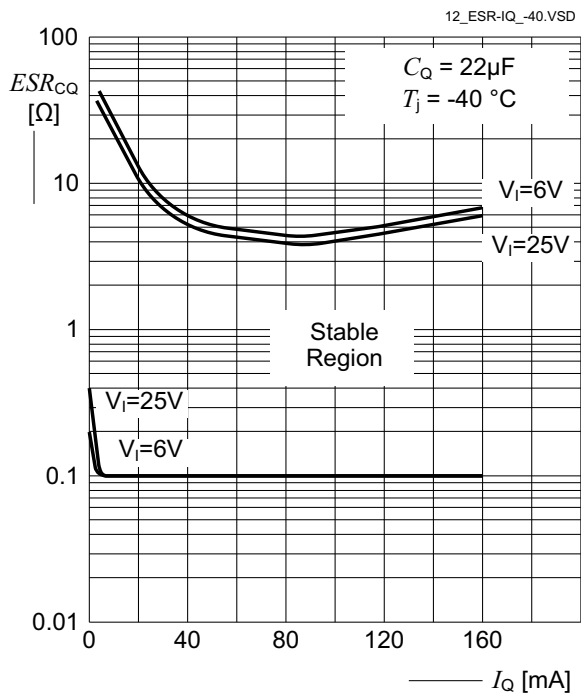
**Region of stability**



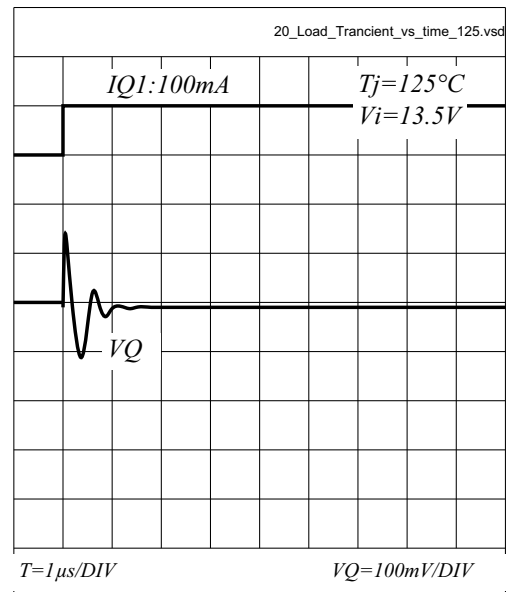
**Power supply ripple rejection PSRR versus Frequency  $f$**



**Region of stability**

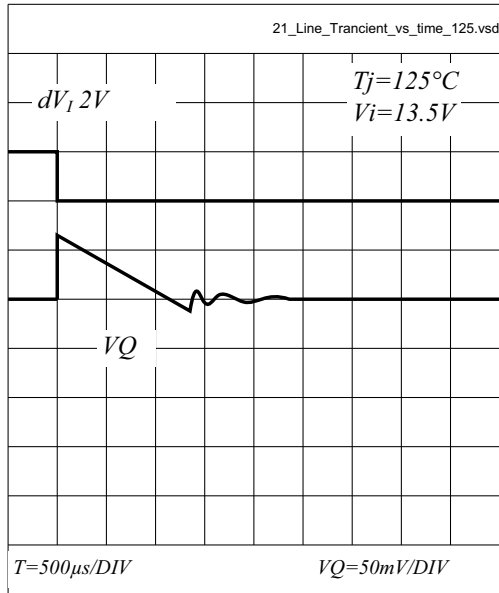


**Load transient response peak voltage  $D_{VQ}$**

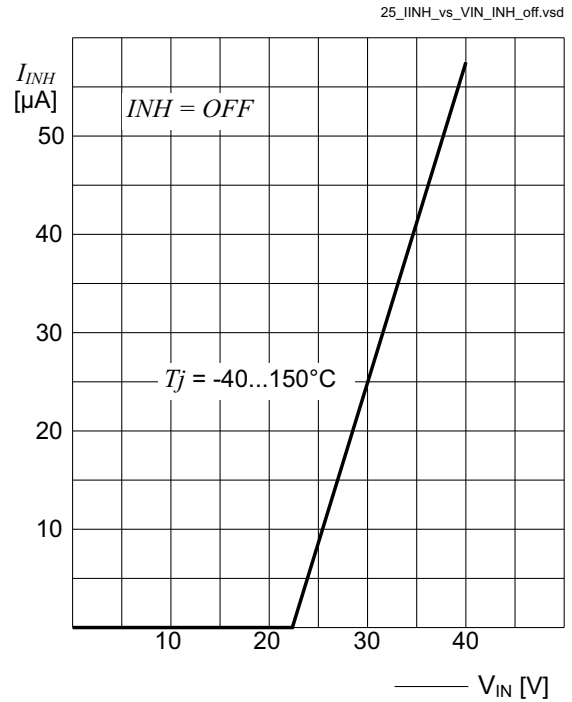


**Functional description**

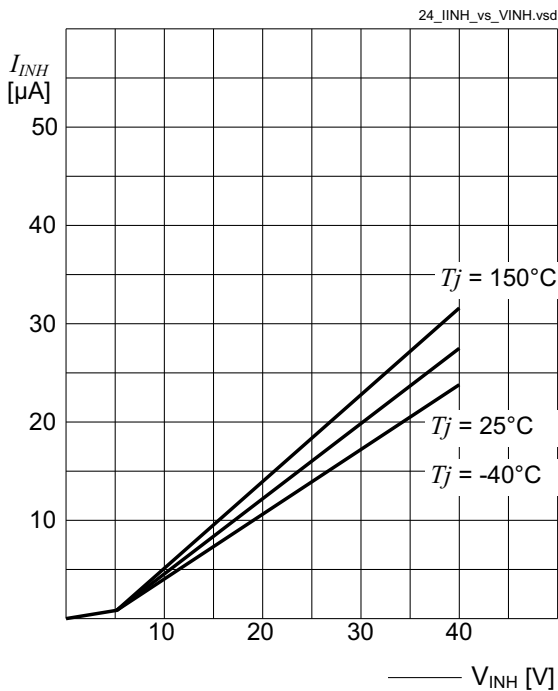
**Line transient response peak voltage  $D_{VQ}$**



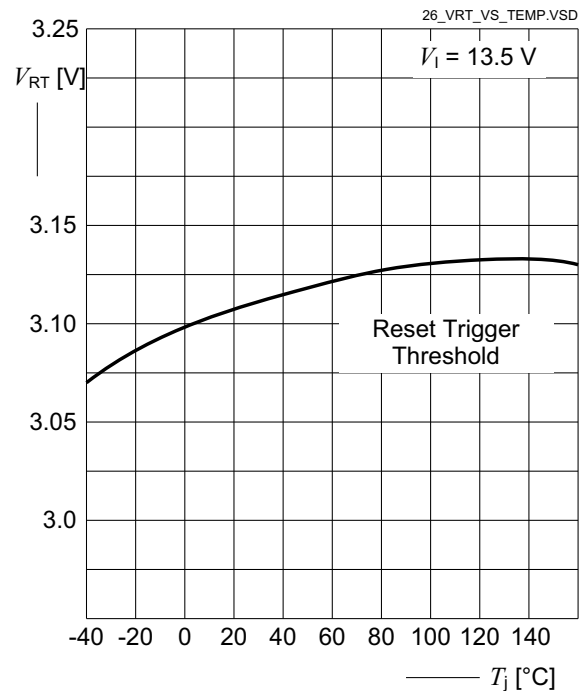
**Inhibit input current at input voltage extremes (INH = OFF)**



**Inhibit input current  $I_{INH}$  at inhibit input voltage extremes**

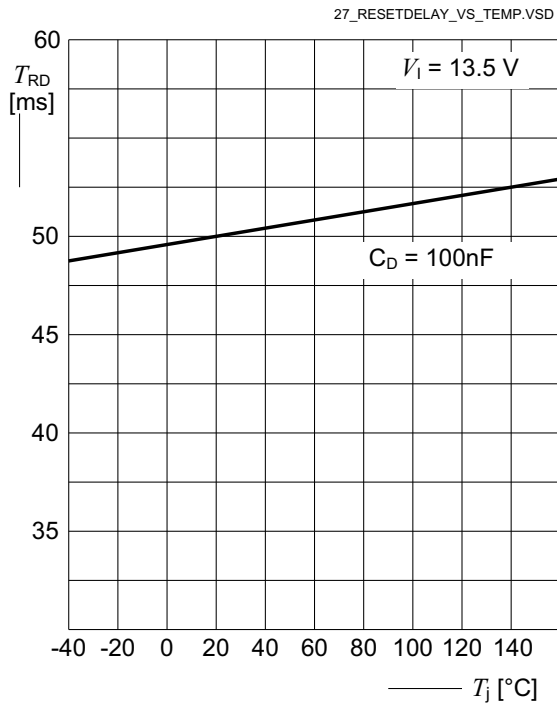


**Reset trigger threshold  $V_{RT}$  versus junction temperature  $T_j$**

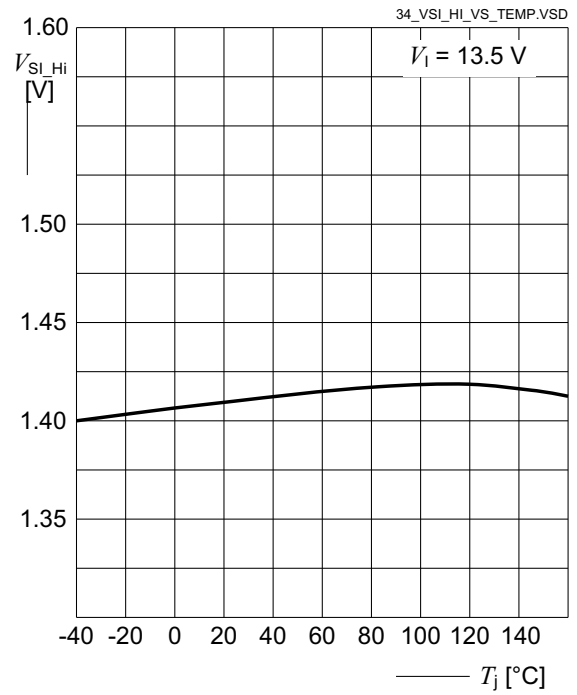


**Functional description**

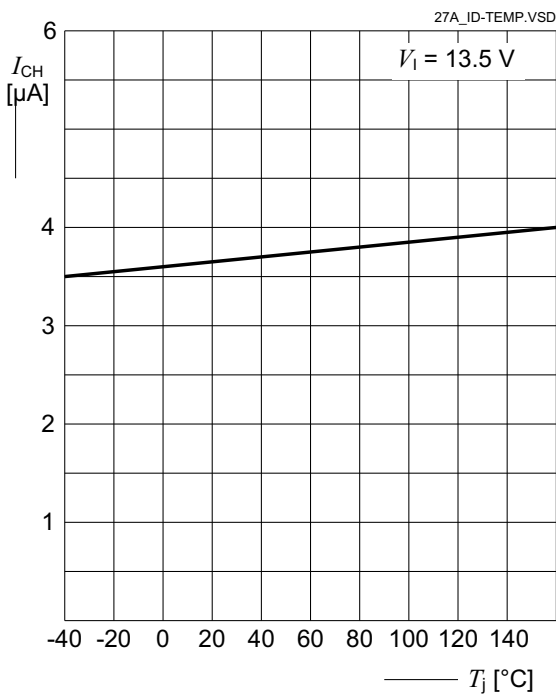
**Reset delay time  $T_{RD}$  versus junction temperature  $T_j$**



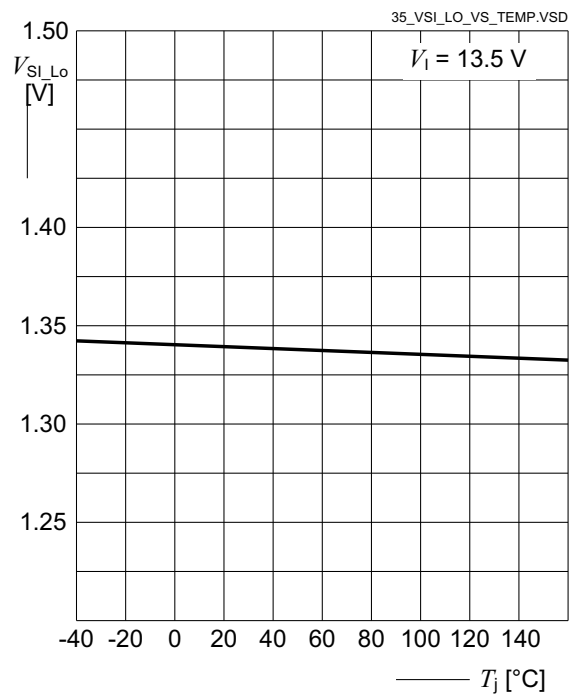
**Sense threshold high versus junction temperature  $T_j$**



**Delay capacitor charge current versus junction temperature  $T_j$**

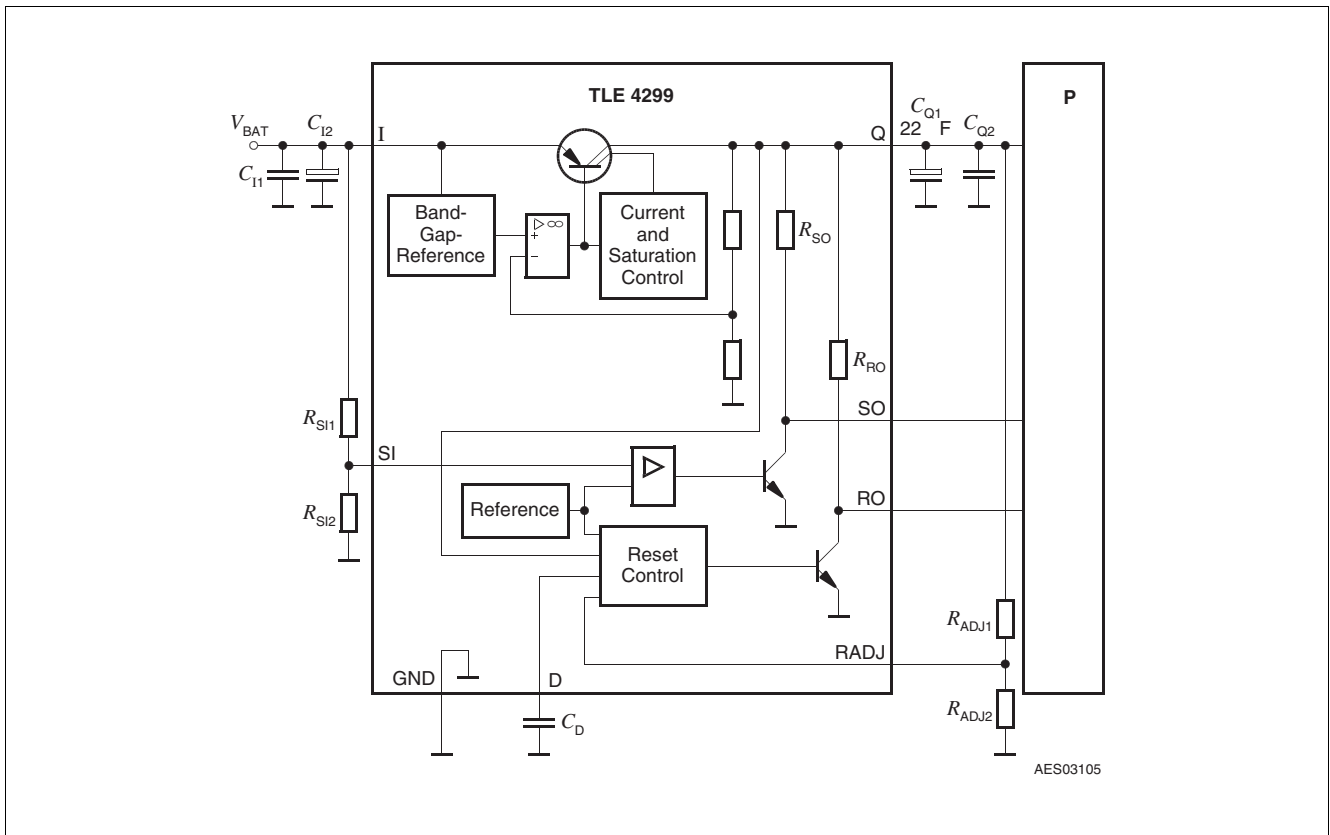


**Sense threshold low versus junction temperature  $T_j$**



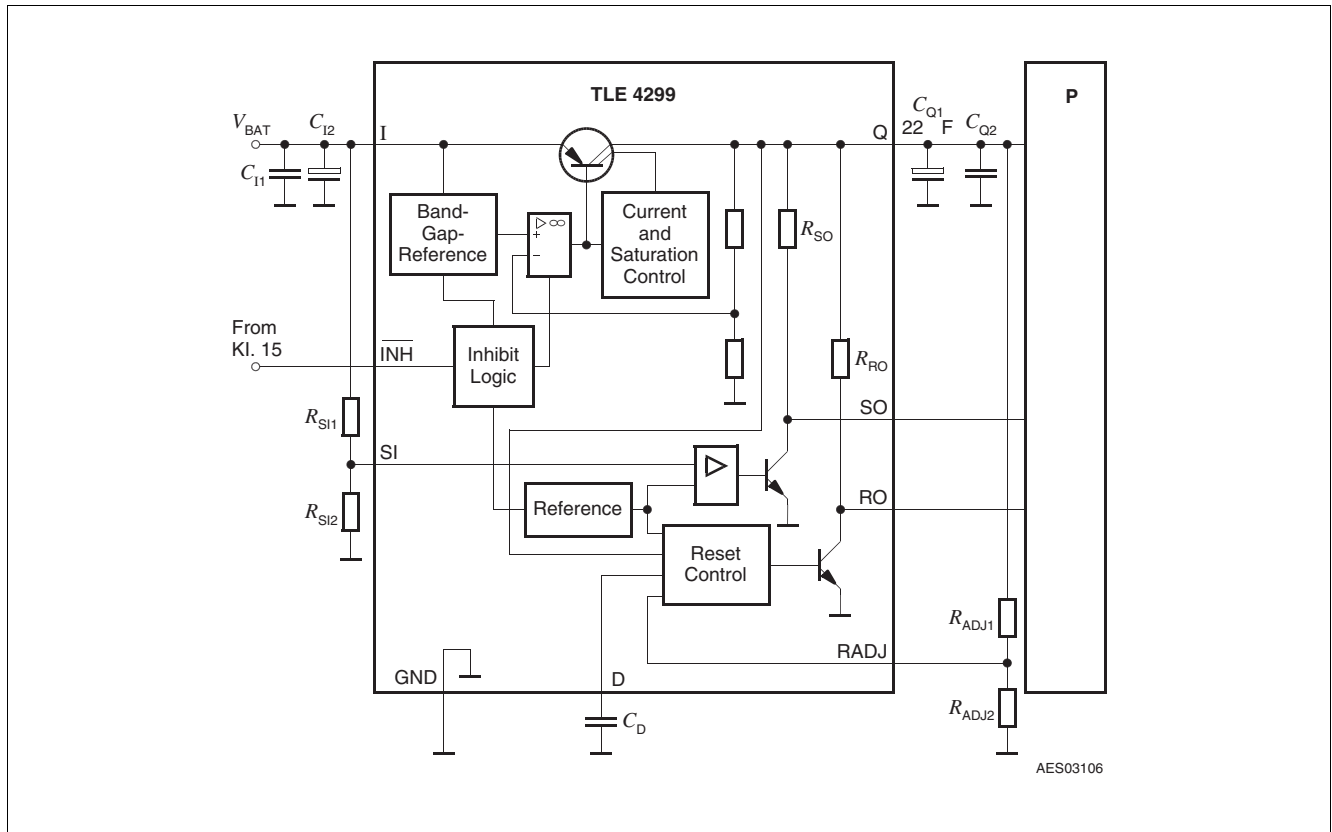


## 5 Application information



**Figure 6 Application diagram TLE4299GV33**

**Application information**



**Figure 7 Application diagram with inhibit function TLE4299GMV33**

The TLE4299V33 supplies a regulated 3.3 V output voltage with an accuracy of 2% for an input voltage between 4.4 V and 45 V in the temperature range of  $T_j = -40$  to  $150^\circ\text{C}$ , in an output current range of 1 mA to 100 mA.

The device is capable to supply 150 mA with an accuracy of 3%. For protection at high input voltage above 25 V, the output current is reduced (SOA protection).

An input capacitor is necessary for compensating line influences and to limit steep input edges. A resistor of approx.  $1\ \Omega$  in series with  $C_I$ , can damp the LC of the input inductivity and the input capacitor.

The voltage regulator requires for stability an output capacitor  $C_Q$  of at least  $22\ \mu\text{F}$  with an  $0.4\ \Omega < \text{ESR} < 3.7\ \Omega$  for the whole load- and temperature range. For more detailed information, refer to the characteristic curves.

**Application information**

**5.1 Reset**

The power on reset feature is necessary for a defined start of the microprocessor when switching on the application. For the reset delay time after the output voltage of the regulator is above the reset threshold, the reset signal is set “high” again. The reset delay time is defined by the reset delay capacitor  $C_D$  at pin D.

The undervoltage reset circuitry supervises the output voltage. In case  $V_Q$  decreases below the reset threshold the reset output is set “low” after the reset reaction time. The reset “low” signal is generated down to an output voltage  $V_Q$  to 1 V. Both the reset reaction time and the reset delay time is defined by the capacitor value.

The power on reset delay time is defined by the charging time of an external delay capacitor  $C_D$ .

(5.1)

$$C_D = (t_d \times I_D) / (\Delta V)$$

(5.2)

$$t_d = C_D \times \Delta V / I_D$$

With	$C_D$	Reset delay capacitor
	$t_d$	Reset delay time
	$\Delta V = V_{DT}$	Typical 1.8 V for power up reset
	$I_{ch}$	Charge current typical 3.5 $\mu A$

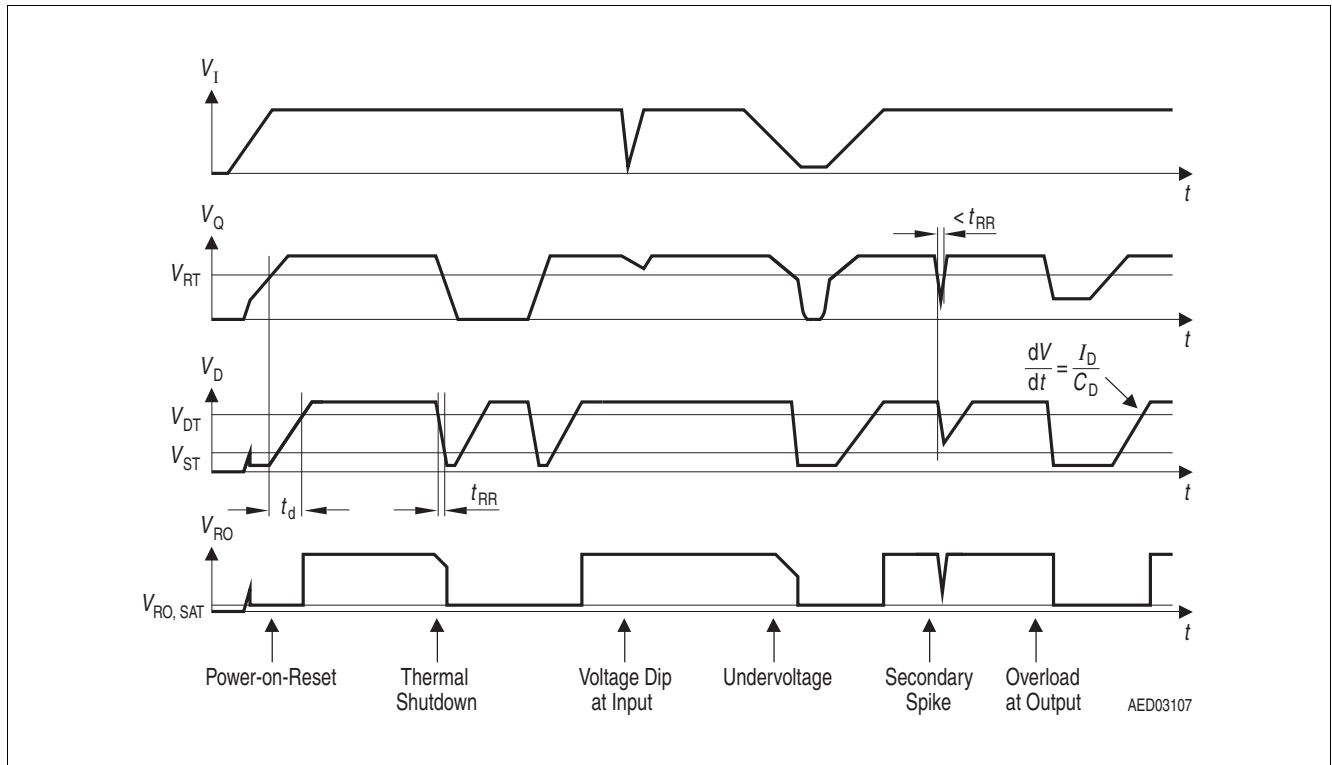
For a delay capacitor  $C_D = 100$  nF the typical power on reset delay time is 51 ms.

The reset reaction time  $t_{RR}$  is the time it takes the voltage regulator to set reset output “low” after the output voltage has dropped below the reset threshold. It is typically 1.2  $\mu s$  for delay capacitor of 100 nF. For other values for  $C_D$  the reaction time can be estimated using the following equation:

(5.3)

$$t_{RR} \sim (10ns) / (nF \times C_D)$$

**Application information**



**Figure 8 Reset timing diagram**

The reset output is an open collector output. An external pull-up can be added with a resistor value of at least 5.6 kΩ.

In addition the reset switching threshold can be adjusted by an external voltage divider.

The feature is useful for microprocessors which ensure safe operation down to voltages below the internally set reset threshold of 3.10 V typical. If the internal used reset threshold of typical 3.10 V is used, the pin  $R_{ADJ}$  must be connected to GND.

If a lower reset threshold is required by the system, a voltage divider defines the reset threshold  $V_{Rth}$  between 2.5 V and 3.10 V as long as the Input Voltage  $V_I > 4.4$  V

(5.4)

$$V_{Rth} = V_{RADJTH} \times (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2}$$

$V_{RADJTH}$  is typical 1.36 V.

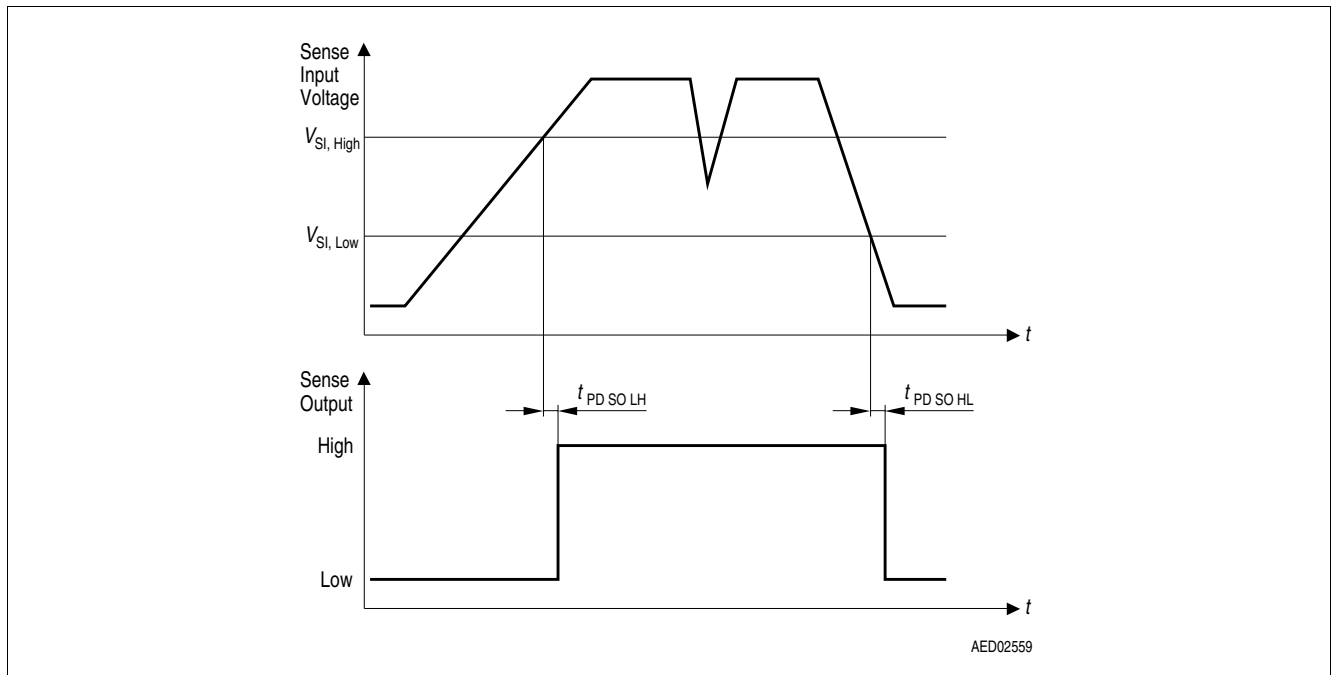
**Application information**

**5.2 Early warning**

The early warning function compares a voltage defined by the user to an internal reference voltage. Therefore the supervised voltage must be scaled down by an external voltage divider in order to compare it to the internal sense threshold of typical 1.36 V. The sense output pin is set “low”, when the voltage at SI falls below this threshold.

A typical example where the circuit can be used is to supervise the input voltage  $V_I$  to give the microcontroller a prewarning of low battery condition.

Calculation to the voltage divider can be easily done since the sense input current can be neglected.



**Figure 9 Sense timing diagram**

(5.5)

$$V_{thHL} = (R_{SI1} + R_{SI2})/R_{SI2} \times V_{SIlow}$$

(5.6)

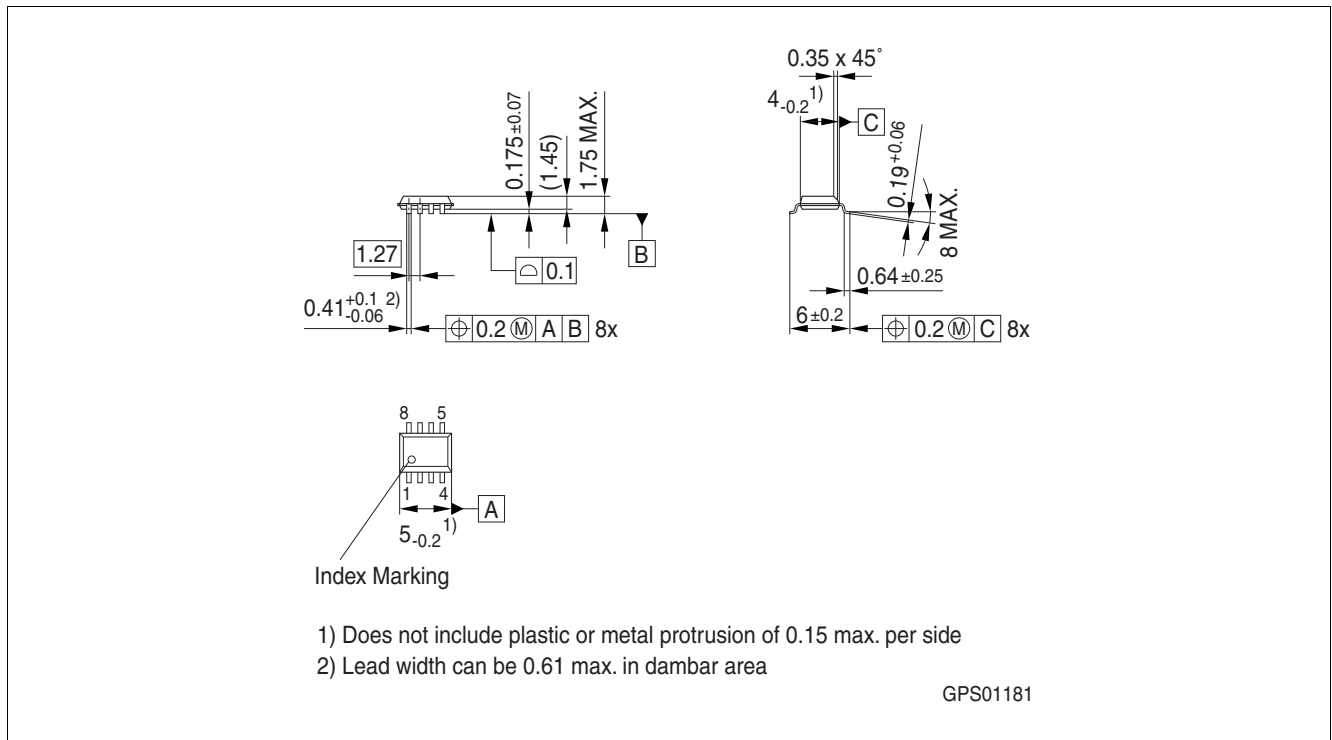
$$V_{thLH} = (R_{SI1} + R_{SI2})/R_{SI2} \times V_{SIhigh}$$

The sense in comparator uses a hysteresis of typical 90 mV. This hysteresis of the supervised threshold is multiplied by the resistor dividers amplification  $(R_{SI1} + R_{SI2})/R_{SI1}$ .

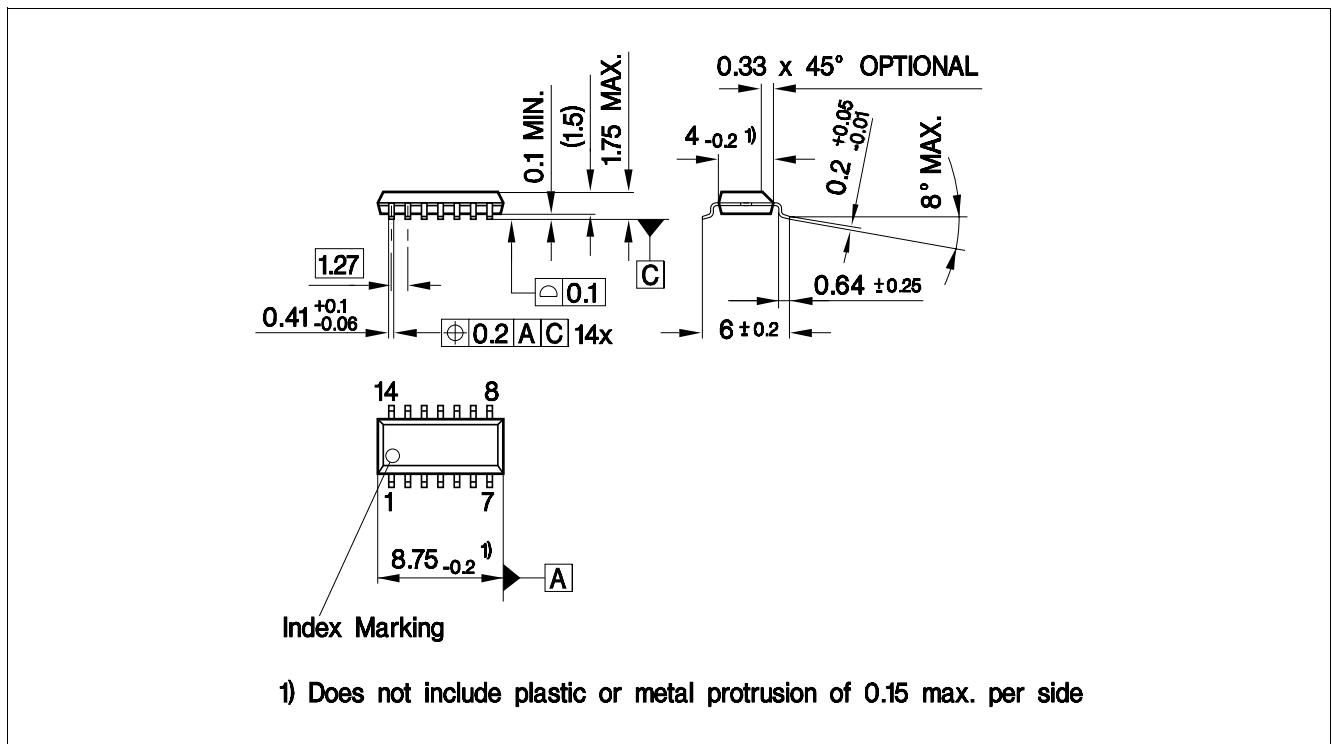
The sense in comparator can also be used for receiving data with a threshold of typical 1.36 V and a hysteresis of 90 mV. Of course also the data signal can be scaled down with a resistive divider as shown above. With a typical delay time of 2.5  $\mu$ s for positive transitions and 2.4  $\mu$ s for negative transitions receiving data of up to 100 kBaud are possible. The sense output is an open collector output.

**Package information**

**6 Package information**



**Figure 10 PG-DSO-8<sup>1)</sup>**



**Figure 11 PG-DSO-14<sup>1)</sup>**

1) Dimensions in mm

# OPTIREG™ Linear TLE4299V33

## Low drop fixed voltage regulator

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### Package information

#### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.2	2018-11-22	Update layout and structure Updated packaged drawing “PG-DSO-14” Editorial changes
1.1	2007-10-17	Initial version of RoHS-compliant derivate of TLE4299 <b>Page 1</b> : AEC certified statement added <b>Page 1</b> and <b>Page 22</b> ff: RoHS compliance statement and Green product feature added <b>Page 1</b> and <b>Page 22</b> ff: Package drawing changed to RoHS compliant version Legal Disclaimer updated



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