

# TLE4968-1K

High Precision Automotive Hall Effect Latch

## Technical Product Description

Rev. 1.0, 2012-01-17

**Edition 2012-01-17**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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Page or Item	Subjects (major changes since previous revision)
<b>Rev. 1.0, 2012-01-17</b>	

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## 1 Product Description



### 1.1 Overview

The TLE4968-1 is a high precision Hall effect bipolar switch with highly accurate switching thresholds for operating temperatures up to 170°C.



Figure 1-1 Image of TLE4968-1 in the PG-SC59-3-5 package

### 1.2 Features

- 3.0V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent & overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35µs)
- High ESD performance
- SOT23 like SMD package PG-SC59-3-5

### 1.3 Target Applications

Target applications for the TLE496x Hall switch family are all applications which require a high precision Hall switch with a operating temperature range from -40°C to 170°C. Its superior supply voltage range from 3.0 V to 32V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor makes it ideally suited for automotive and industrial applications.

The TLE4968-1 has very low magnetic thresholds and a bipolar switching behavior. It is therefore especially suited for applications which require a high sensitivity device and an output switching close to zero magnetic field values. Possible applications are BLDC rotor position measurement or speed and position measurements in camshaft or transmission applications.

Table 1-1 Ordering Information

Product Name	Product Type	Ordering Code	Package
TLE4968-1K	Bipolar Hall Latch	SP000847992	PG-SC59-3-5

## 2 Functional Description

### 2.1 General

The TLE4968-1 is an integrated Hall effect switch designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

### 2.2 Pin Configuration (top view)

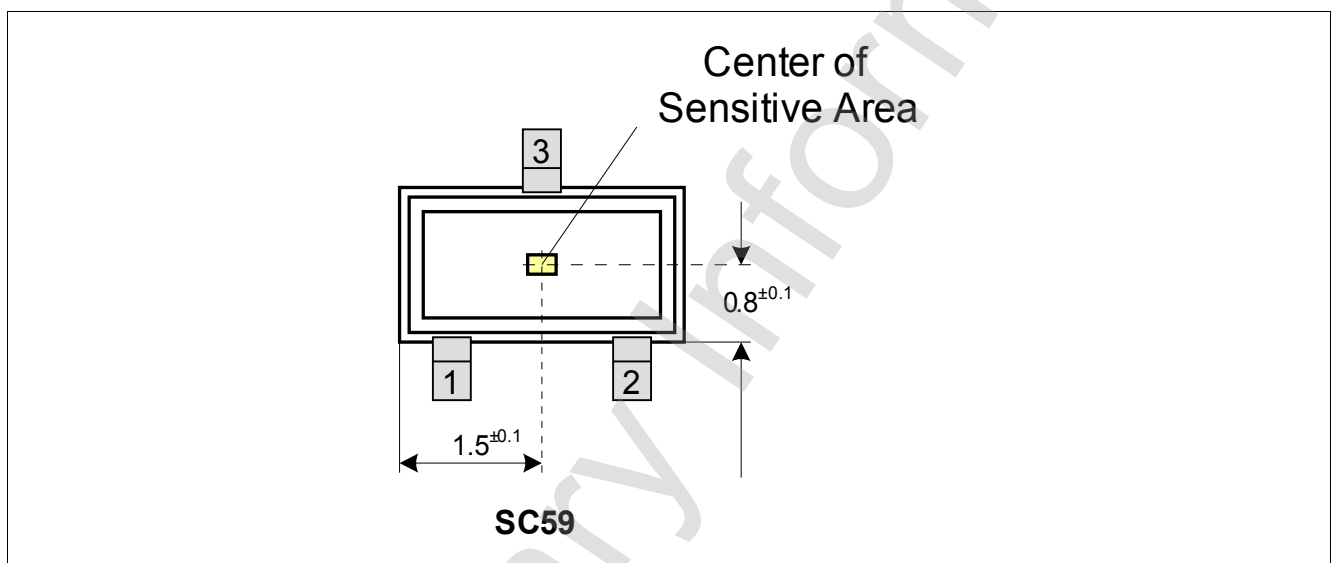


Figure 2-1 Pin Configuration and Center of Sensitive Area

### 2.3 Pin Description

Table 2-1 Pin Description PG-SC59-3-5

Pin No.	Symbol	Function
1	VDD	Supply voltage
2	Q	Output
3	GND	Ground

## 2.4 Block Diagram

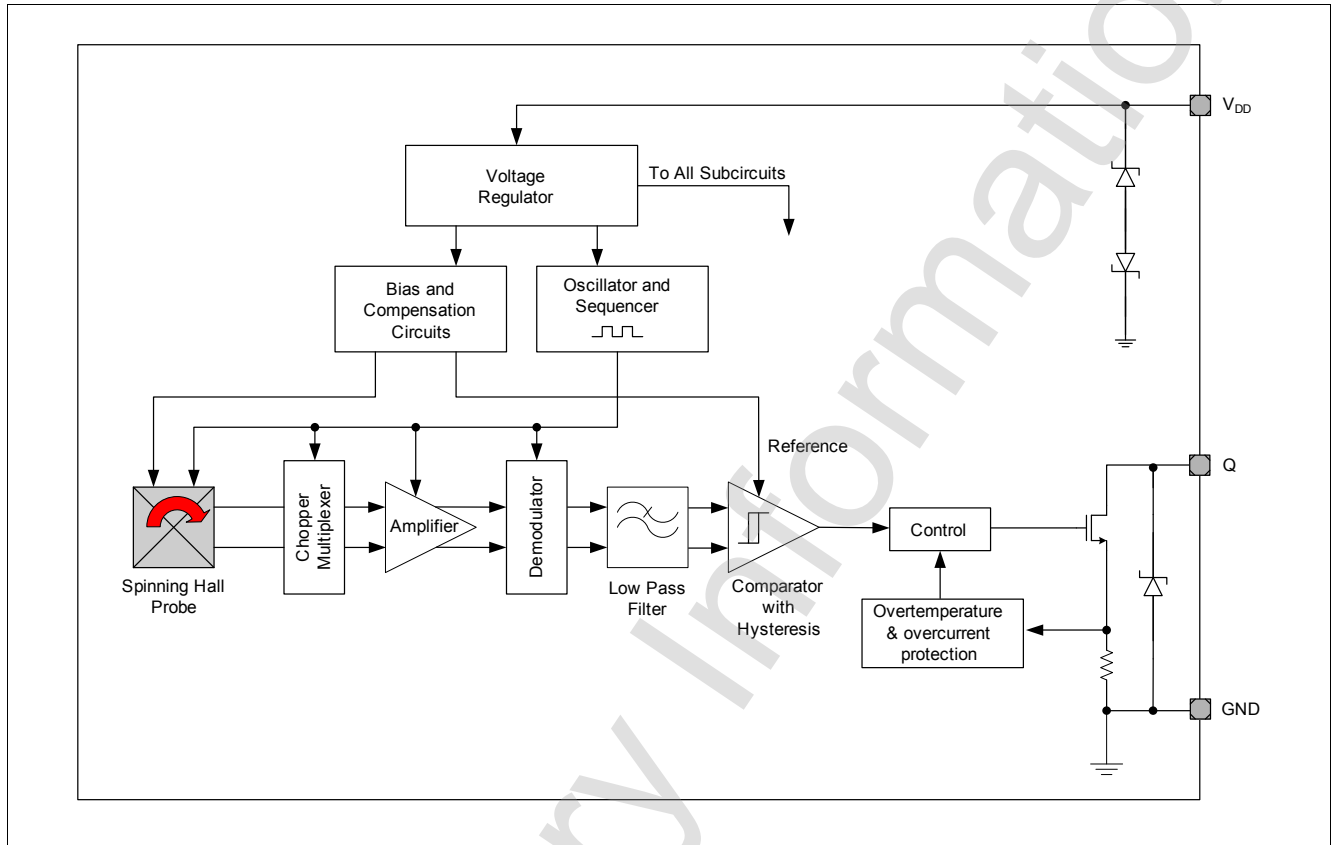


Figure 2-2 Functional Block Diagram TLE4968-1

## 2.5 Functional Block Description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

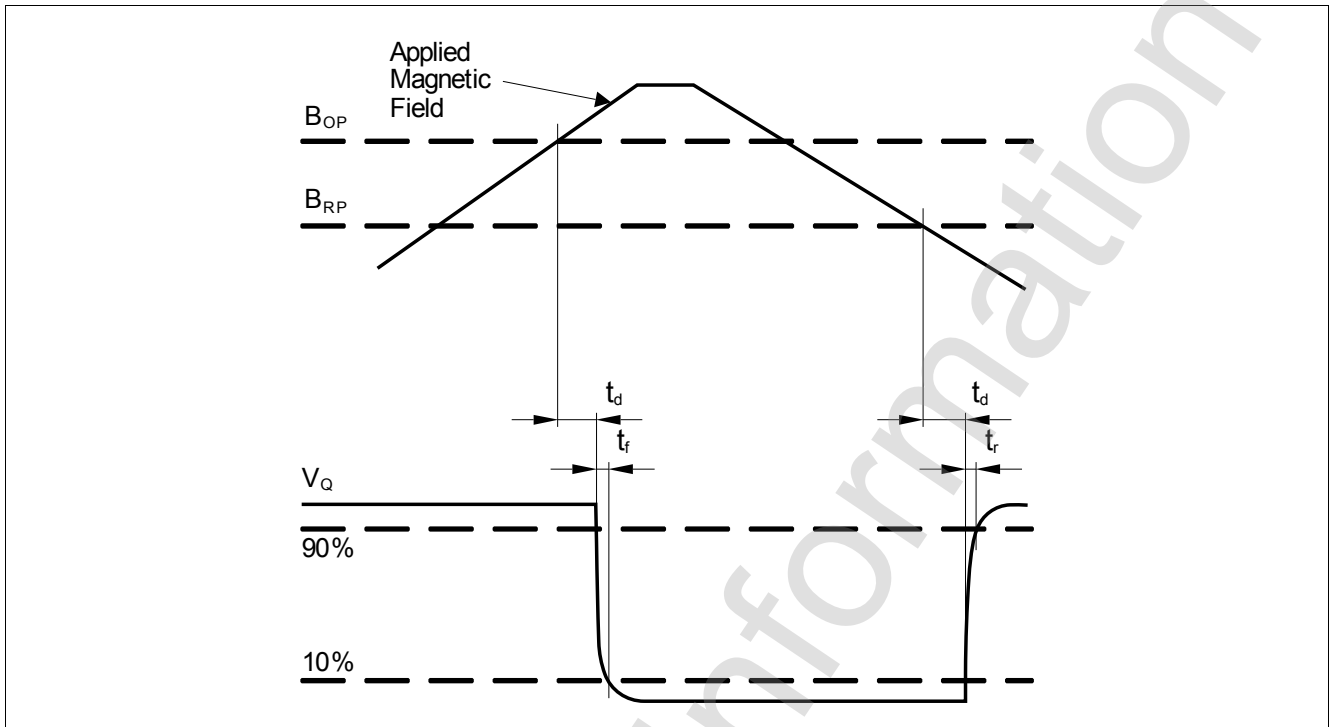


Figure 2-3 Timing Diagram TLE4968-1

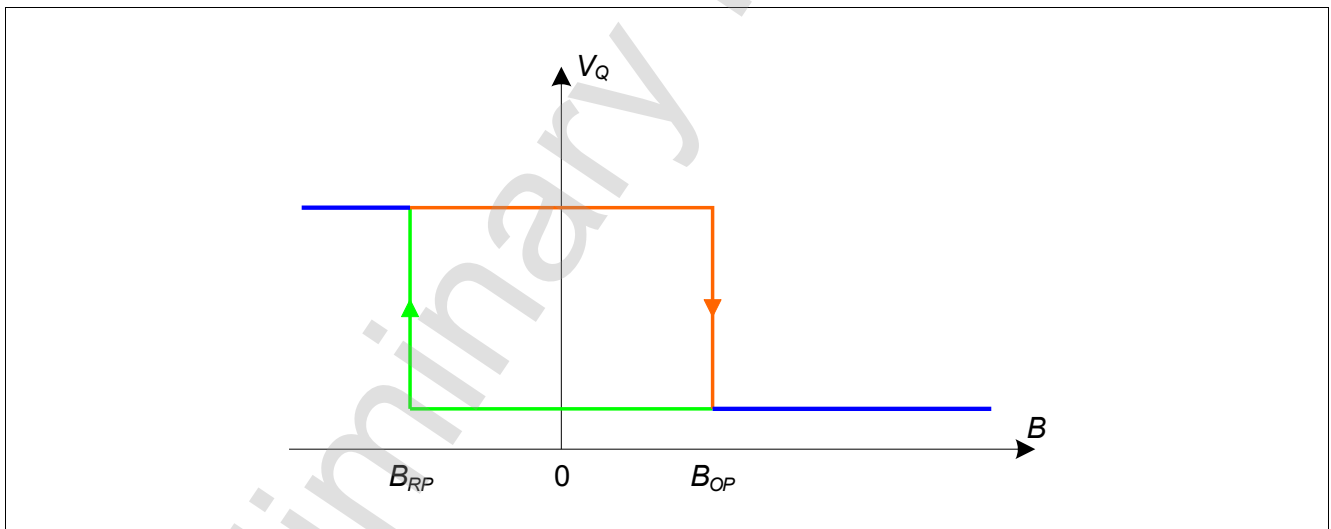


Figure 2-4 Output Signal TLE4968-1



### 3 Specification

#### 3.1 Application Circuit

The following **Figure 3-1** shows one option of an application circuit. As explained above the resistor  $R_S$  can be left out (see **Figure 3-2**). The resistor  $R_Q$  has to be in a dimension to match the applied  $V_S$  to keep  $I_Q$  limited to the operating range of maximal 25mA.

e.g.:

$$V_S = 12 \text{ V}$$

$$I_Q = 12 \text{ V} / 1200\Omega = 10\text{mA}$$

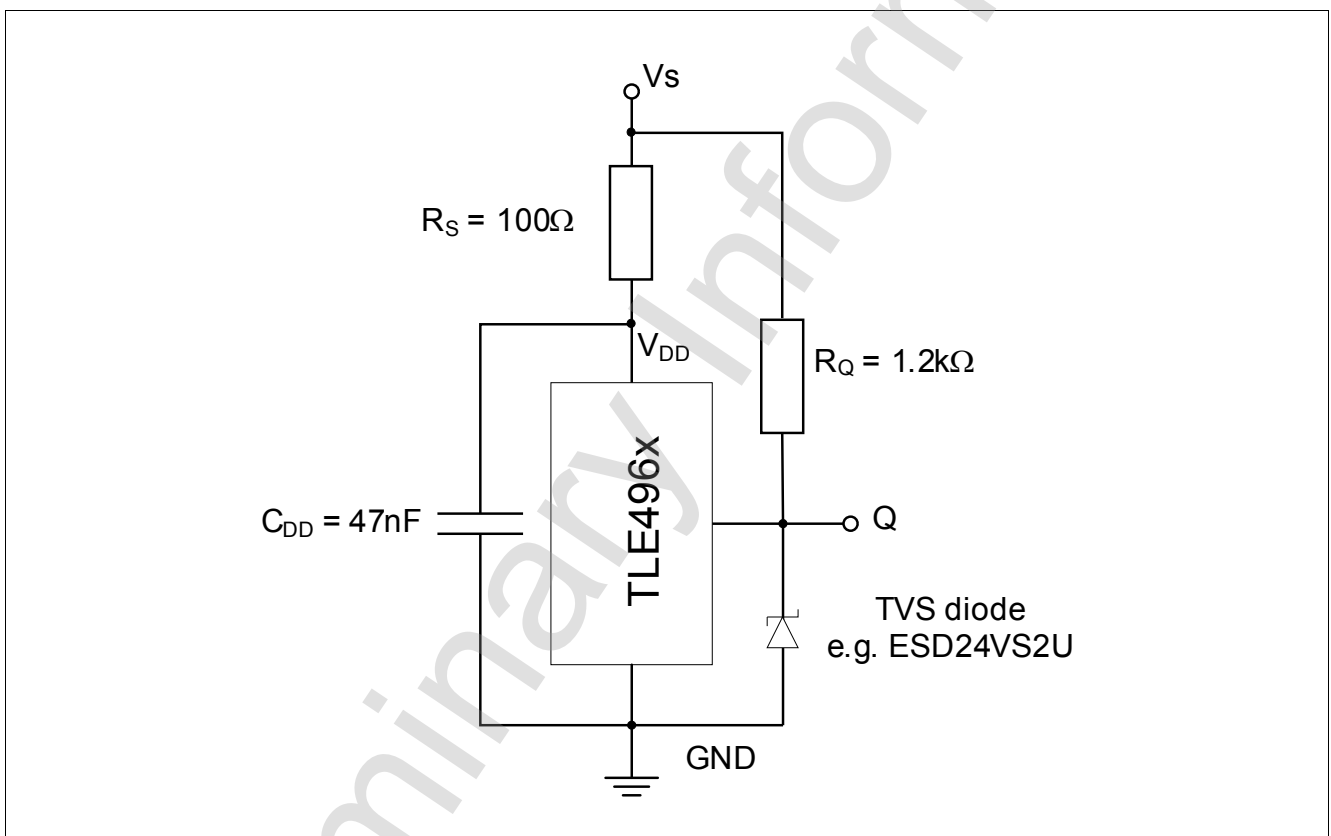


Figure 3-1 Application Circuit 1: with external resistor

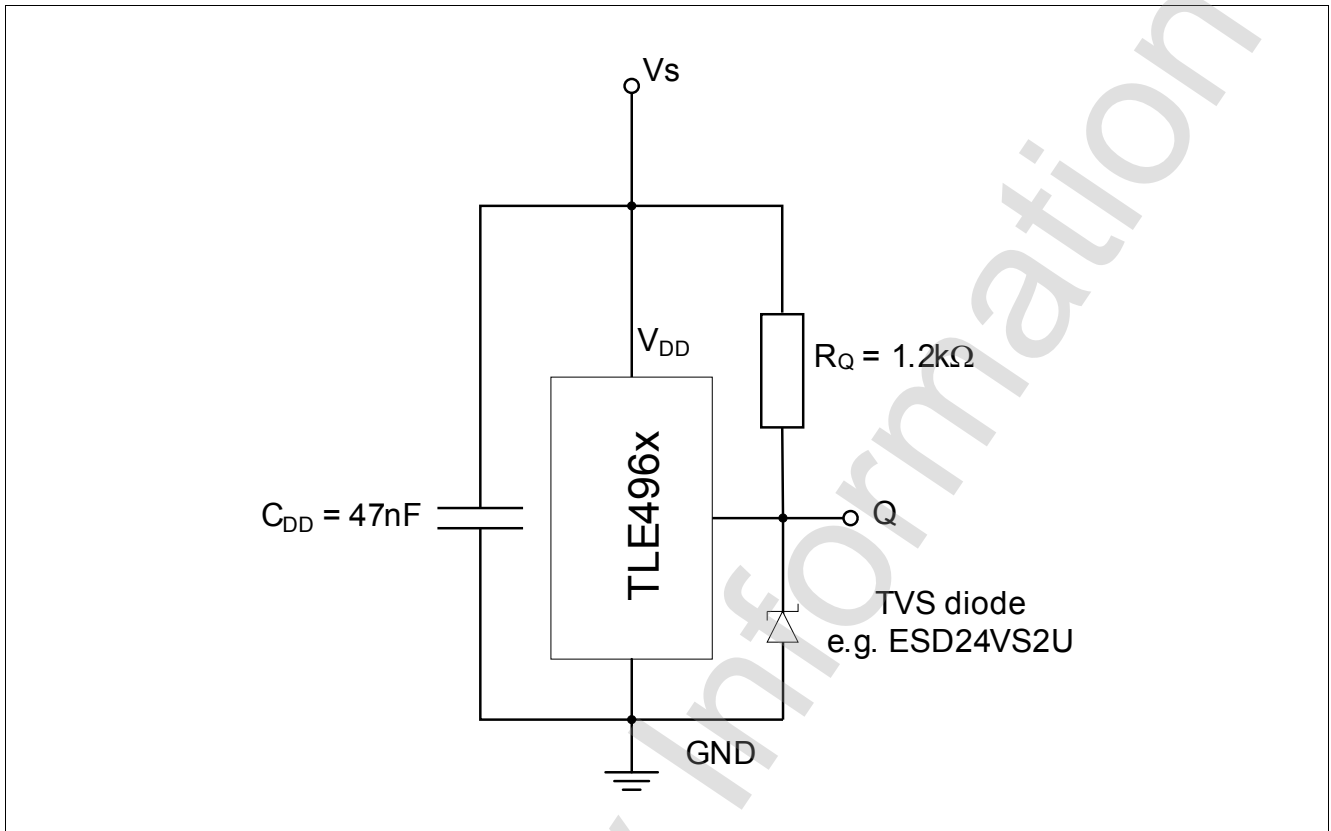


Figure 3-2 Application Circuit 2: without external resistor

### 3.2 Absolute Maximum Ratings

**Table 3-1 Absolute Maximum Rating Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	-18		32 42	V	10h, no external resistor required
Output voltage	$V_Q$	0		32	V	
Reverse output current	$I_Q$	-70			mA	
Junction temperature	$T_J$	-40		155 165 175 195	°C	for 2000h (not additive) for 1000h (not additive) for 168h (not additive) for 3 x 1h (additive)
Thermal resistance Junction ambient	$R_{thJA}$			300	K/W	for PG-SC59-3-5
Thermal resistance Junction lead	$R_{thJL}$			100	K/W	for PG-SC59-3-5

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

Calculation of the dissipated power  $P_{DIS}$  and junction temperature  $T_J$  of the chip (SC59 example):

e.g for:  $V_{DD} = 12\text{ V}$ ,  $I_S = 2.5\text{ mA}$ ,  $V_{QSAT} = 0.5\text{ V}$ ,  $I_Q = 20\text{ mA}$

Power dissipation:  $P_{DIS} = 12\text{ V} \times 2.5\text{ mA} + 0.5\text{ V} \times 20\text{ mA} = 30\text{ mW} + 10\text{ mW} = 40\text{ mW}$

Temperature  $\Delta T = R_{thJA} \times P_{DIS} = 300\text{ K/W} \times 40\text{ mW} = 12\text{ K}$

For  $T_A = 150^\circ\text{C}$ :  $T_J = T_A + \Delta T = 150^\circ\text{C} + 12\text{ K} = 162^\circ\text{C}$

**Table 3-2 ESD Protection<sup>1)</sup> (TA = 25°C)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) <sup>2)</sup>	$V_{ESD}$	-7		7	kV	R = 1.5kΩ, C = 100pF
ESD voltage (SDM) <sup>3)</sup>		-1		1		
ESD voltage (system level) <sup>4)</sup>		-15		15		with circuit shown in <a href="#">Figure 3-1</a> & <a href="#">Figure 3-2</a>

- 1) Characterization of ESD is carried out on a sample basis.
- 2) Human Body Model (HBM) tests according to EIA/JESD22-A114
- 3) Socket device model (SDM) tests according to EOS/ESD-DS5.3-1993
- 4) Gun test (2kΩ / 330pF or 330Ω / 150pF) according to ISO 10605-2008

### 3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4968-1K. All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

**Table 3-3 Operating Conditions Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	3.0		32 <sup>1)</sup>	V	
Output voltage	$V_Q$	0		32	V	
Junction temperature	$T_j$	-40		170	°C	
Output current	$I_Q$	0		25	mA	
Magnetic signal input frequency <sup>2)</sup>	$f_{SW}$	0		10	kHz	

- 1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.
- 2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

### 3.4 Electrical and Magnetic Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to  $V_{DD} = 12\text{ V}$  and  $T_A = 25^\circ\text{C}$ . The below listed specification is valid in combination with the application circuit shown in [Figure 3-1](#) and [Figure 3-2](#)

**Table 3-4 General Electrical Characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	$I_S$	1.1	1.6	2.5	mA	
Reverse current	$I_{SR}$		0.05	1	mA	for $V_{DD} = -18\text{V}$
Output saturation voltage	$V_{QSAT}$		0.2	0.5	V	$I_Q = 20\text{mA}$
			0.24	0.6	V	$I_Q = 25\text{mA}$
Output leakage current	$I_{QLEAK}$			10	$\mu\text{A}$	
Output current limitation	$I_{QLIMIT}$	30	56	70	mA	internally limited & thermal shutdown
Output fall time <sup>1)</sup>	$t_f$	0.17	0.4	1	$\mu\text{s}$	1.2k $\Omega$ / 50pF, see <a href="#">Figure 2-3</a>
Output rise time <sup>1)</sup>	$t_r$	0.4	0.5	1	$\mu\text{s}$	1.2k $\Omega$ / 50pF, see <a href="#">Figure 2-3</a>
Output jitter <sup>1)2)</sup>	$t_{QJ}$		0.35	1	$\mu\text{s}$	For square wave signal with 1kHz
Delay time <sup>1)3)</sup>	$t_d$	12	15	30	$\mu\text{s}$	see <a href="#">Figure 2-3</a>
Power-on time <sup>1)4)</sup>	$t_{PON}$		80	150	$\mu\text{s}$	$V_{DD} = 3\text{ V}$ , $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$
Chopper frequency <sup>1)</sup>	$f_{OSC}$		350		kHz	

- 1) Not subject to production test, verified by design/characterization
- 2) Output jitter is the  $1\sigma$  value of the output switching distribution
- 3) Systematic delay between magnetic threshold reached and output switching
- 4) Time from applying  $V_{DD} = 3.0\text{ V}$  to the sensor until the output is valid

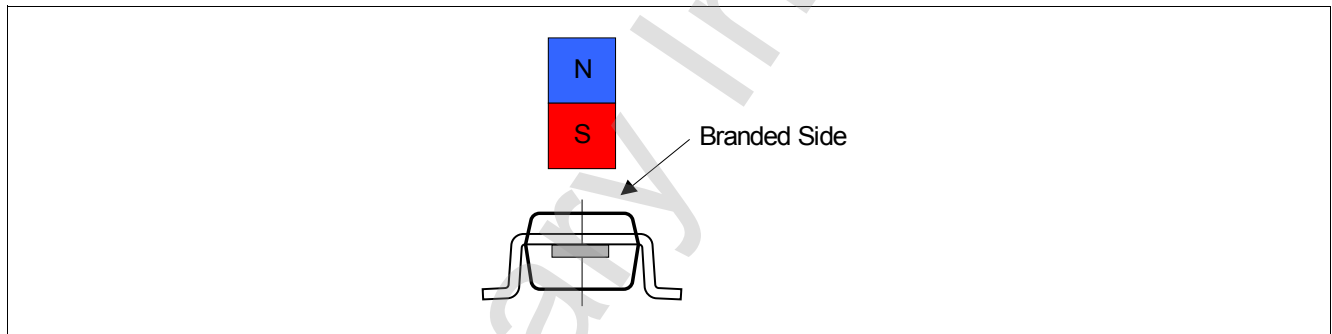
**Table 3-5 Magnetic Characteristics**

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B <sub>OP</sub>	-40...170	-0.2	1.0	2.25	mT	
Release point	B <sub>RP</sub>	-40...170	-2.25	-1.0	0.2	mT	
Hysteresis	B <sub>HYS</sub>	-40...170	1.5	2.0	2.5	mT	
Effective noise value of the magnetic switching points <sup>1)</sup>	B <sub>Neff</sub>	25		62		μT	
Temperature compensation of magnetic thresholds <sup>2)</sup>	T <sub>C</sub>			0		ppm/K	

- 1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents a the rms-value and corresponds therefore to a 1 σ probability of normal distribution. Consequently a 3 σ value corresponds to 99.7% probability of appearance.
- 2) Not subject to production test, verified by design/characterization

**Field Direction Definition**

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.



**Figure 3-3 Definition of magnetic field direction PG-SC59-3-5**

## 4 Package Information

The TLE4968-1 is available in the SMD package PG-SC59-3-5 with a SOT23 like pinout and footprint.

### 4.1 Package Outline PG-SC59-3-5

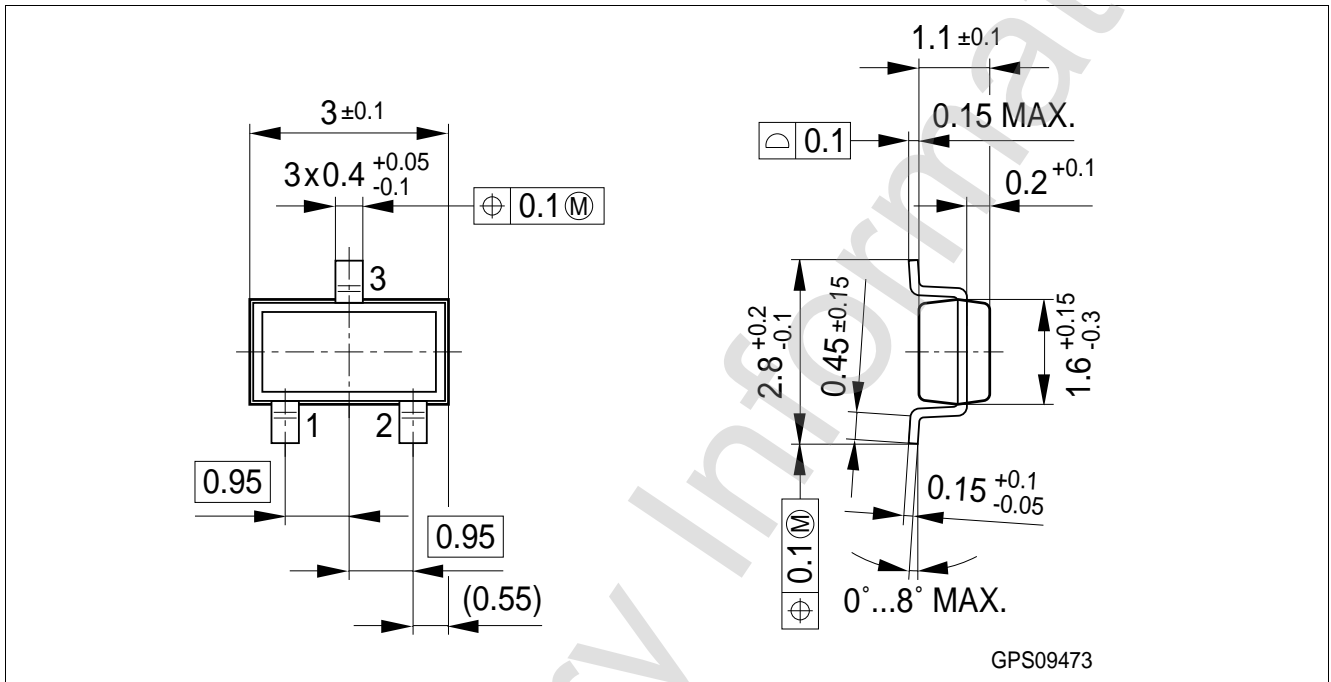


Figure 4-1 PG-SC59-3-5 Package Outline (All dimensions in mm)

### 4.2 Footprint

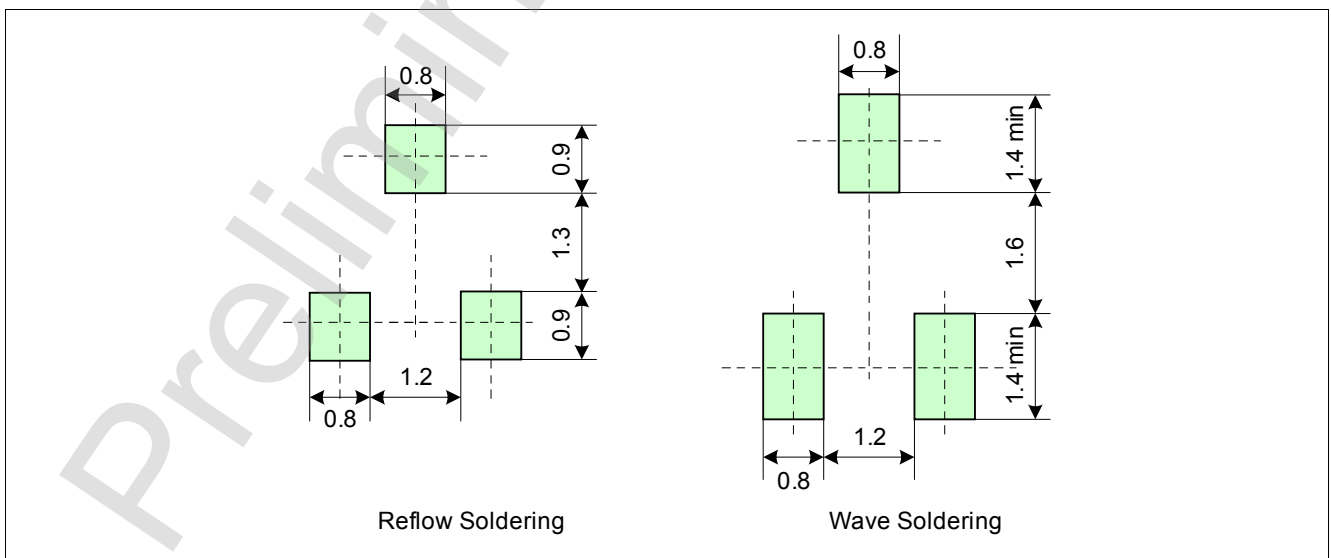


Figure 4-2 Footprint PG-SC59-3-5 and PG-SOT23

### 4.3 PG-SC59-3-5 Distance between Chip and Package

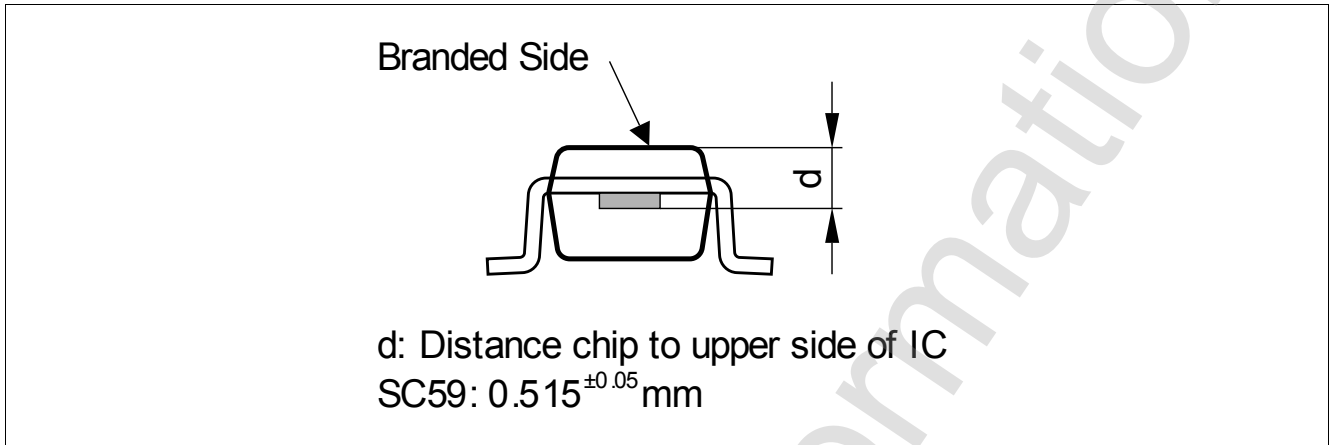


Figure 4-3 Distance between chip and package

### 4.4 Package Marking

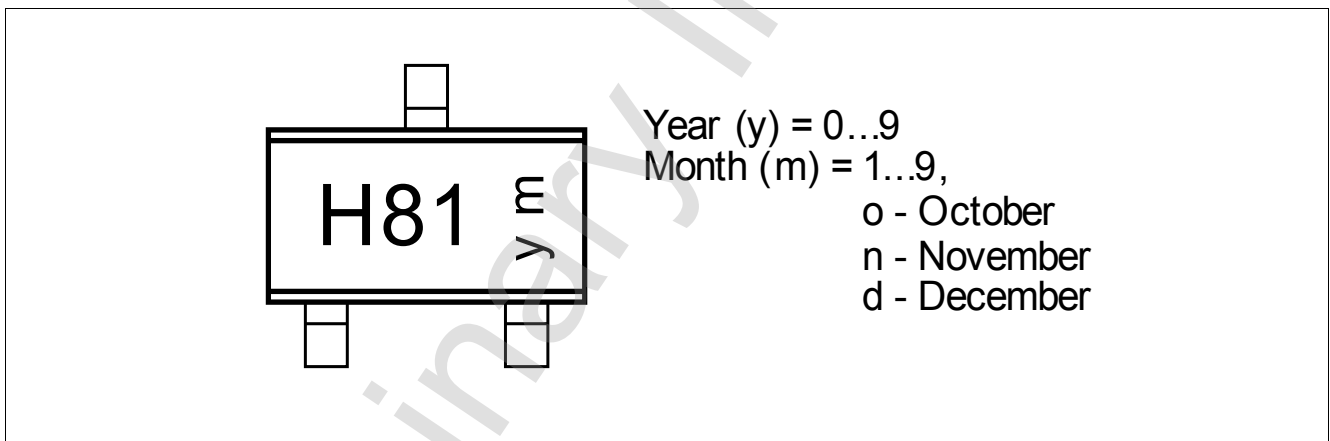


Figure 4-4 Marking of TLE4968-1K

Preliminary Information

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