

# TLE4997A8(D)

Programmable Single/Dual Die Linear Hall Sensor

## Data Sheet

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Sense & Control

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# 1 Overview



| Characteristic                                   | Supply Voltage | Supply Current | Magnetic Range            | Interface                 | Temperature    |
|--|----------------|----------------|---------------------------|---------------------------|----------------|
| Programmable Single/ Dual Die Linear Hall Sensor | 4.5~5.5 V      | 7.5 mA         | ±50mT<br>±100mT<br>±200mT | Analog Ratiometric Output | -40°C to 125°C |

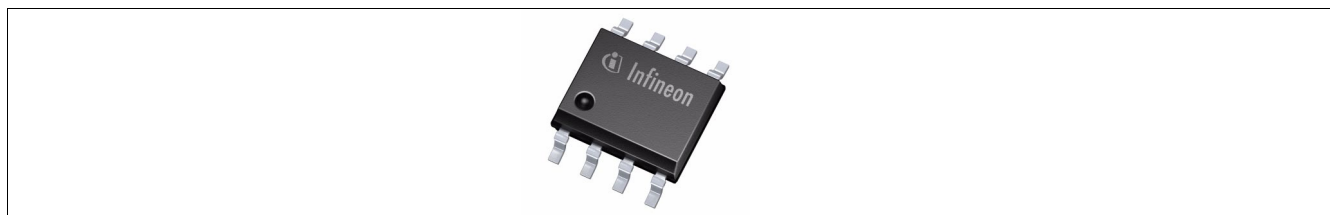


Figure 1-1 SMD package PG-TDSO-8 for the TLE4997A8(D)

## 1.1 Features

- Integration of two individual programmable Linear Hall sensor IC's with ratiometric analog output signal.
- 20-bit Digital Signal Processing (DSP)
- Digital temperature compensation
- 12-bit overall resolution
- Operating automotive temperature range -40°C to 125°C
- Low drift of output signal over temperature and lifetime
- Programmable parameters stored in EEPROM with single-bit error correction:
  - Magnetic range and sensitivity (gain), polarity of the output slope
  - Offset
  - Bandwidth
  - Clamping levels
  - Temperature compensation coefficients to accomodate most common magnet materials
  - Memory lock
- Supply voltage 4.5-5.5 V (4-7 V extended range)
- Configurable magnetic range : ±50mT, ±100mT or ±200mT
- Reverse-polarity and overvoltage protection for all pins
- Output short-circuit protection
- On-board diagnostics (wire breakage detection, EEPROM error, overvoltage)
- Digital readout of internal temperature and magnetic field values in calibration mode
- Programming and operation of multiple sensors with common power supply
- Two-point calibration of magnetic transfer function

*Note: Product qualification is based on "AEC Q100" grade 1 (Automotive Electronics Council - Stress test qualification for integrated circuits)*

Table 1-1 Ordering Information

| Product Name | Marking | Ordering Code | Package                  |
|--------------|---------|---------------|--------------------------|
| TLE4997A8    | A8S     | SP001215464   | single sensor, PG-TDSO-8 |
| TLE4997A8D   | A8D     | SP000902760   | dual sensor, PG-TDSO-8   |

## 1.2 Target Applications

- Robust replacement of potentiometers: No mechanical abrasion, resistant to humidity, temperature, pollution and vibration
- Linear and angular position sensing in automotive and industrial applications with highest accuracy requirements
- Suited for ASIL applications such as pedal position, throttle position and steering torque sensing

## 1.3 Pin Configuration

Figure 1-2 shows the location of the Hall elements in the chip pin configuration of the package.

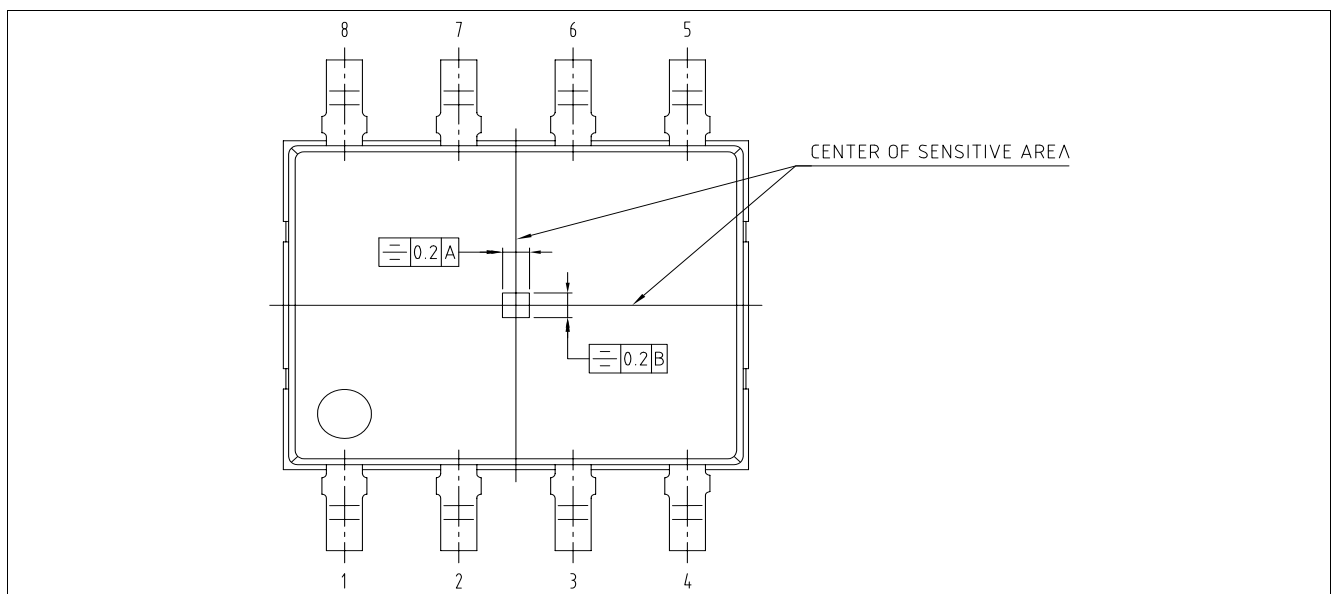


Figure 1-2 Pin Configuration of PG-TDSO-8 package

Table 1-2 TLE4997A8(D) Pin Definitions and Functions

| Pin No. | Symbol   | TLE4997A8 Function                               | TLE4997A8D Function                                 |
|---------|----------|--|---|
| 1       | n/c      | not connected (connection to GND is recommended) | not connected (connection to GND is recommended)    |
| 2       | $V_{DD}$ | Supply voltage / programming interface           | Supply voltage / programming interface (top die)    |
| 3       | GND      | Ground   | Ground (top die)                                    |
| 4       | OUT      | Output / programming interface                   | Output / programming interface (top die)            |
| 5       | OUT      | not connected                                    | Output / programming interface (bottom die)         |
| 6       | GND      | not connected                                    | Ground (bottom die)                                 |
| 7       | $V_{DD}$ | not connected                                    | Supply voltage / programming interface (bottom die) |
| 8       | n/c      | not connected                                    | not connected (connection to GND is recommended)    |

## 2 General

All further specifications are regarded to both implemented sensor IC's, or otherwise noted.

### 2.1 Block Diagram

Figure 2-1 shows is a simplified block diagram.

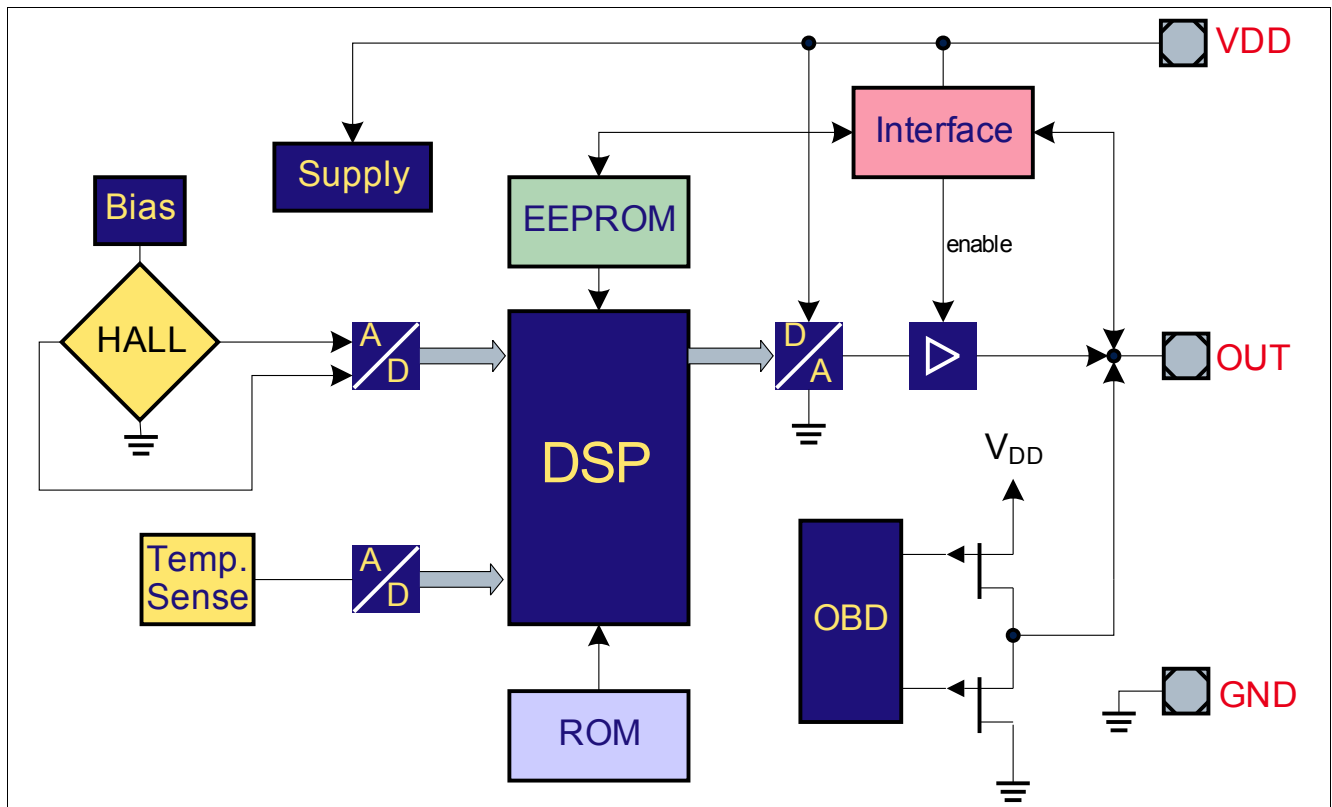


Figure 2-1 Block Diagram of the TLE4997A8(D) with the ratiometric analog output interface

### 2.2 Functional Description

The linear Hall IC TLE4997A8(D) has been specifically designed for highly accurate angle and position detection. The sensor provides a ratiometric analog output voltage, which is ideally suited to Analog-to-Digital (A/D) conversion with the supply voltage as a reference.

The IC is produced in BiCMOS technology with high voltage capability and also provides reverse polarity protection.

Digital signal processing using a 16-bit DSP architecture together with digital temperature and analog stress compensation guarantees excellent stability over the whole temperature range and life time.

## 2.3 Principle of Operation

- A magnetic flux is measured by a Hall-effect cell
- The output signal from the Hall-effect cell is converted from analog to digital signals
- The chopped Hall-effect cell and continuous-time A/D conversion ensure a very low and stable magnetic offset
- A programmable low-pass filter to reduce noise
- The temperature is measured and A/D converted
- Temperature compensation is done digitally using a second-order function
- Digital processing of the output value is based on zero field and sensitivity value
- The output value range can be clamped by digital limiters
- The final output value is D/A converted
- The output voltage is proportional to the supply voltage (ratiometric DAC)
- An On-Board-Diagnostics (OBD) circuit connects the output to  $V_{DD}$  or GND in case of errors

## 2.4 Transfer Functions

The examples in [Figure 2-2](#) show how different magnetic field ranges can be mapped to the desired output value ranges.

- Polarity Mode:
  - **Bipolar:** Magnetic fields can be measured in both orientations. The limit points do not necessarily have to be symmetrical around the zero field point
  - **Unipolar:** Only north- or south-oriented magnetic fields are measured
- Inversion: The gain value of either die can be set independently, to be positive or negative.

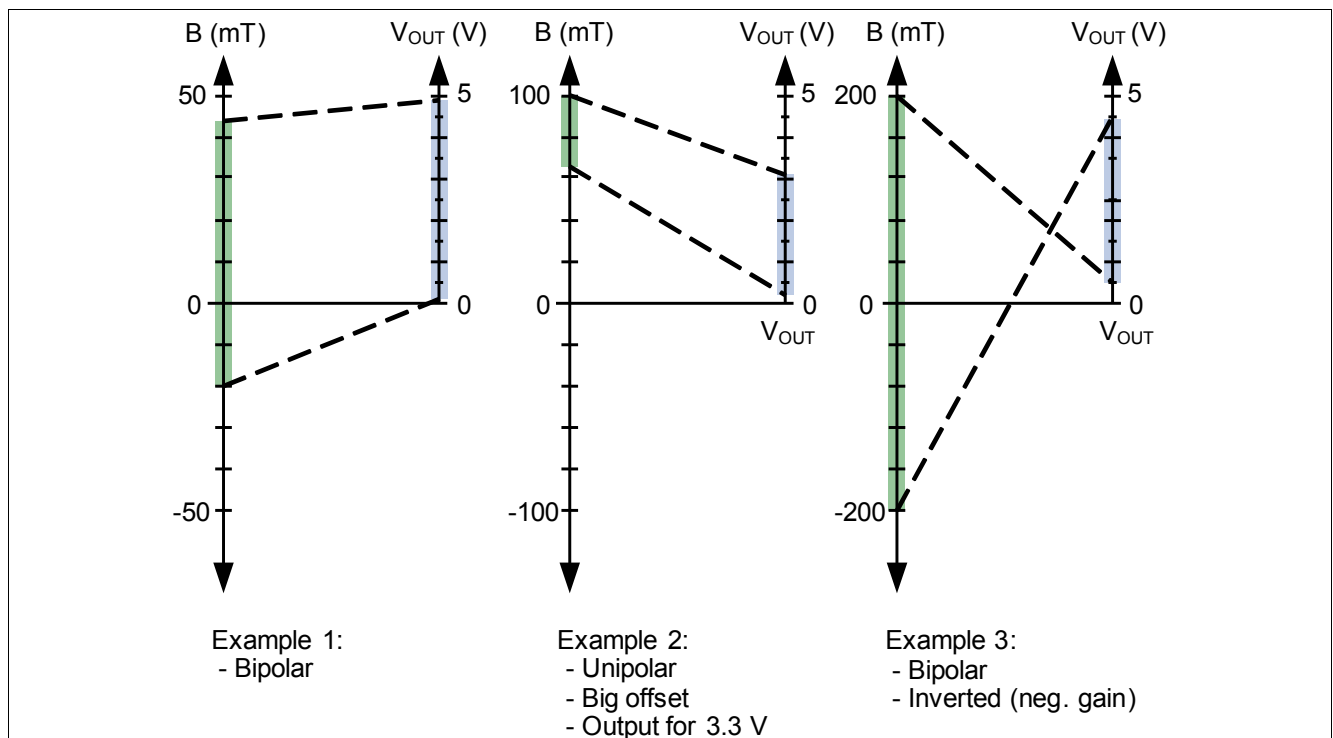


Figure 2-2 Examples of Operation



### 3 Maximum Ratings

**Table 3-1 Absolute Maximum Ratings**

| Parameter   | Symbol      | Values            |      |                   | Unit | Note / Test Condition  |
|---|-------------|-------------------|------|-------------------|------|--|
|   |             | Min.              | Typ. | Max.              |      |  |
| Junction temperature  | $T_J$       | - 40              | –    | 160 <sup>1)</sup> | °C   | -  |
| Voltage on $V_{DD}$ pin with respect to ground ( $V_{SS}$ ) | $V_{DD}$    | -20 <sup>2)</sup> | –    | 20 <sup>3)</sup>  | V    | $R_{THja} \leq 150 \text{ K/W}$                                |
| Supply current @ overvoltage                                | $I_{DDov}$  | –                 | –    | 52                | mA   | -  |
| Supply current @ reverse voltage                            | $I_{DDrev}$ | -75               | –    | –                 | mA   | -  |
| Voltage on output pin with respect to ground ( $V_{SS}$ )   | $V_{OUTov}$ | -16 <sup>4)</sup> | –    | 16 <sup>3)</sup>  | V    | $R_{THja} \leq 150 \text{ K/W}$<br>$V_{OUT}$ may be $> V_{DD}$ |
| Magnetic field  | $B_{MAX}$   | -                 | –    | 1                 | T    | -  |
| ESD protection  | $V_{ESD}$   | -                 |      | $\pm 2$           | kV   | According HBM<br>ANSI/ESDA/JEDEC<br>JS-001 <sup>5)</sup>       |

1) For limited time of 96 h. Depends on application temperature lifetime cycles. Please ask for support by Infineon.

2) max 24 h @  $-40^\circ\text{C} \leq T_a < 30^\circ\text{C}$   
 max 10 min. @  $30^\circ\text{C} \leq T_a < 80^\circ\text{C}$   
 max 30 sec. @  $80^\circ\text{C} \leq T_a < 125^\circ\text{C}$ .

3) max. 24 h @  $T_J < 80^\circ\text{C}$ .

4) Max. 1 ms @  $T_J < 30^\circ\text{C}$ ; -8.5 V for 100 h @  $T_J < 80^\circ\text{C}$ .

5) 100 pF and 1.5 k $\Omega$

**Attention: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device.**

**Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on VDD pins with respect to ground (VSS) must not exceed the values defined by the absolute maximum ratings. Lifetime statements are an anticipation based on an extrapolation of Infineon’s qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.**



## 4 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4997A8(D). All parameters specified in the following sections refer to these operating conditions, if applicable or unless otherwise indicated.

**Table 4-1 Operating Range**

| Parameter                         | Symbol    | Values |      |      | Unit               | Note / Test Condition                               |
|-----------------------------------|-----------|--------|------|------|--------------------|---|
|                                   |           | Min.   | Typ. | Max. |                    |   |
| Supply voltage                    | $V_{DD}$  | 4.5    | –    | 5.5  | V                  |   |
|                                   |           | 4      | –    | 7    | V                  | Extended range                                      |
| Output current                    | $I_{OUT}$ | -1     | –    | 1    | mA                 | <sup>1)</sup>                                       |
| Load resistance                   | $R_L$     | 10     | –    | –    | k $\Omega$         | Pull-down to GND                                    |
|                                   |           | 10     | –    | –    |                    | Pull-up to $V_{DD}$                                 |
| Load capacitance                  | $C_L$     | 0      | –    | 210  | nF                 |   |
| Ambient temperature <sup>2)</sup> | $T_A$     | - 40   | –    | 125  | $^{\circ}\text{C}$ | max. 1200 h at 125 $^{\circ}\text{C}$ <sup>3)</sup> |

1) For  $V_{OUT}$  within the range of 5% ... 95% of  $V_{DD}$ .

2)  $R_{THja} \leq 150 \text{ K/W}$ .

3) Maximum exposure time at other ambient temperatures between -40 $^{\circ}\text{C}$  and 125 $^{\circ}\text{C}$  shall be calculated based on the values specified in this table using the Arrhenius model.

*Note: Keeping signal levels within the limits specified in this table ensures operation without overload conditions.*

## 5 Electrical, Thermal and Magnetic Parameters

All specification values are valid over temperature and lifetime, unless noted otherwise.

### 5.1 Electrical Characteristics

**Table 5-1 Electrical Characteristics**

| Parameter                                     | Symbol            | Values |      |          | Unit          | Note / Test Condition   |
|---|-------------------|--------|------|----------|---------------|---|
|   |                   | Min.   | Typ. | Max.     |               |   |
| Output voltage range                          | $V_{OUT}$         | 5<br>6 | –    | 95<br>94 | % of $V_{DD}$ | for $T_A \leq 120^\circ\text{C}$<br>for $T_A > 120^\circ\text{C}$ |
| Supply current                                | $I_{DD}$          | 3      | 7.5  | 10       | mA            | <sup>1)</sup>   |
| Output current @ OUT shorted to supply lines  | $I_{OUTsh}$       | -30    | –    | 30       | mA            | for operating supply voltage range only                           |
| Zero field voltage                            | $V_{ZERO}$        | -100   | –    | 100      | %             | internal offset range   |
| Zero field voltage drift                      | $\Delta V_{ZERO}$ | -10    | –    | 10       | mV            | In lifetime <sup>2)</sup>   |
|   |                   | -10    | –    | 10       | mV            | error band over temp. <sup>3)</sup>                               |
| Ratiometry error                              | $E_{RAT}$         | -0.25  | –    | 0.25     | %             | of $V_{DD}$ <sup>3)4)</sup>                                       |
| Thermal resistance<br>PG-TDSO-8 <sup>5)</sup> | $R_{thJA}$        | –      | 150  | –        | K/W           | junction to air   |
|   | $R_{thJC}$        | –      | 50   | –        |               | junction to case  |
| Power-on time <sup>6)</sup>                   | $t_{Pon}$         | –      | –    | 1        | ms            | $\Delta V_{OUT} \leq \pm 5\%$ of $V_{DD}$                         |
|   |                   | –      | –    | 10       |               | $\Delta V_{OUT} \leq \pm 1\%$ of $V_{DD}$                         |
| Power-on reset level                          | $V_{DDpon}$       | 2      | –    | 4        | V             |   |
| Output DAC quantization                       | $\Delta V_{OUT}$  |        | 1.22 |          | mV            | @ $V_{DD} = 5\text{ V}$   |
| Output DAC resolution                         | –                 |        | 12   |          | bit           |   |
| Output DAC bandwidth                          | $f_{DAC}$         | –      | 3.2  | –        | kHz           | interpolation filter <sup>7)</sup>                                |
| Differential non-linearity                    | DNL               | -1     | –    | 1        | LSB           | of output DAC   |
| Output noise (rms)                            | $V_{noise}$       | –      | –    | 3        | mV            | <sup>8)</sup>   |
| Signal delay                                  | $t_{SD}$          | –      | –    | 250      | $\mu\text{s}$ | @ 100 Hz <sup>9)</sup>  |

1) Also in extended  $V_{DD}$  range. For  $V_{OUT}$  within the range of 5%... 95% of  $V_{DD}$ ,  $I_{OUT} = 0\text{ mA}$ .

2) For Sensitivity  $S \leq 25\text{ mV/mT}$ . For higher sensitivities the magnetic offset drift is dominant.

3) For  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  and within nominal  $V_{OUT}$  range; see “[Ratiometry](#)” on Page 11 for details on  $E_{RAT}$ .

4) For the maximum error in the extended voltage range, see “[Ratiometry](#)” on Page 11.

5) values derived from simulation with a 4 layer PCB

6) Response time to set up output data at power on when a constant field is applied. The first value given has a  $\pm 5\%$  error, the second value has a  $\pm 1\%$  error.

7) More information, see [Figure 7-2 “DAC Input Filter \(Magnitude Plot\)”](#) on Page 16.

8) 50 mT range (also valid for 100 mT range), LP filter setting 1320 Hz or less, gain 1.0 (scales linearly with gain)

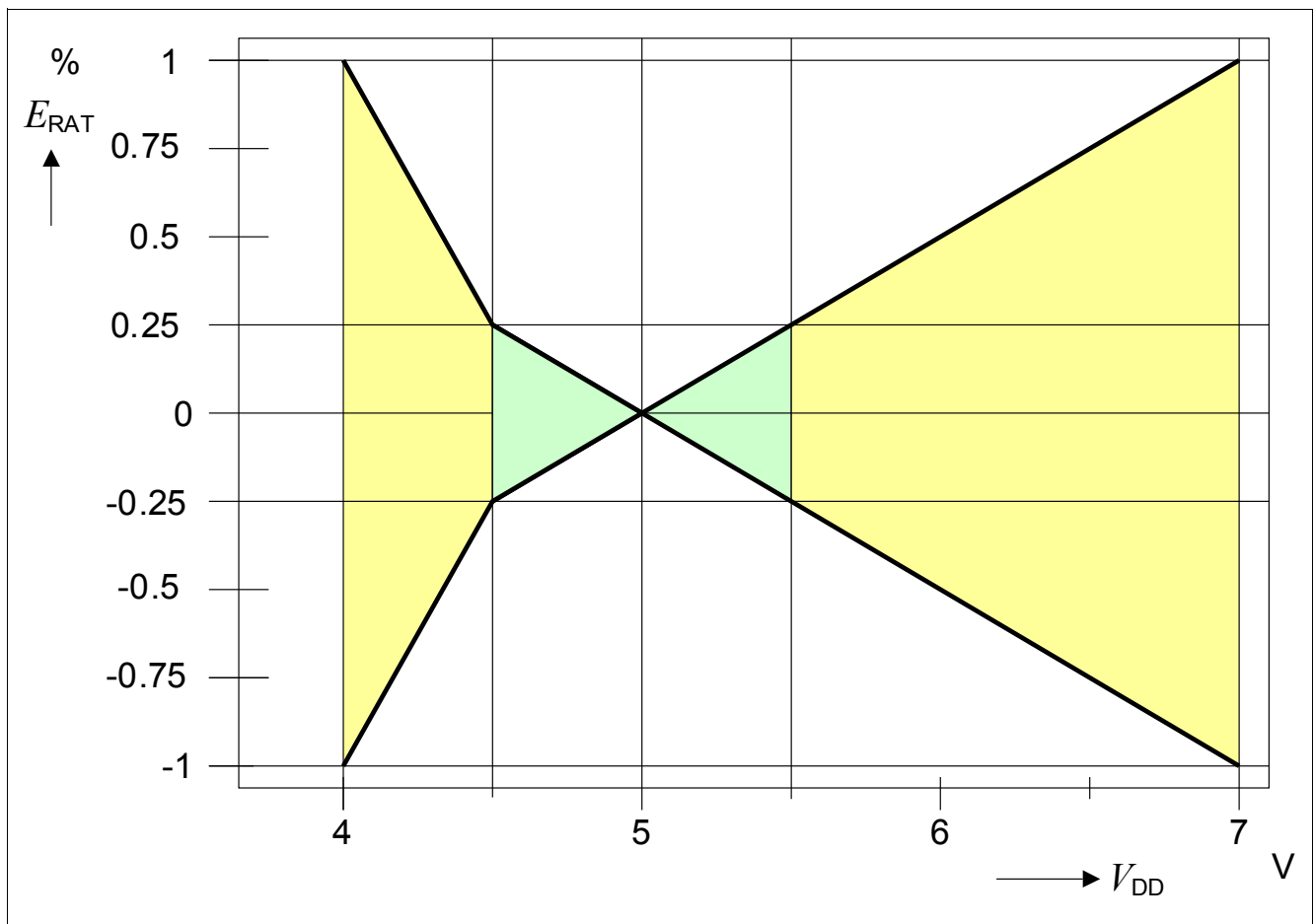
9) A sinusoidal magnetic field is applied,  $V_{OUT}$  shows amplitude of 20% of  $V_{DD}$ , LP filter is disabled.

**Ratiometry**

The linear Hall sensor works like a potentiometer. The output voltage is proportional to the supply voltage. The division factor depends on the magnetic field strength. This behavior is called “ratiometric”. The supply voltage  $V_{DD}$  should be used as the reference for the A/D Converter of the micro controller. In this case, variations of  $V_{DD}$  are compensated. The ratiometry error is defined as follows:

$$E_{RAT} = \left( \frac{V_{OUT}(V_{DD})}{V_{DD}} - \frac{V_{OUT}(5V)}{5V} \right) \times 100\% \tag{5.1}$$

The ratiometry error band displays as a “Butterfly Curve”.



**Figure 5-1 Ratiometry Error Band**

*Note: Take care of possible voltage drops on the  $V_{DD}$  and  $V_{OUT}$  line degrading the result. Ideally, both values are acquired and their ratio is calculated to gain the highest accuracy. This method should be used especially during calibration.*

**Calculation of the Junction Temperature**

The internal power dissipation  $P_{TOT}$  of the sensor increases the chip junction temperature above the ambient temperature.

The power multiplied by the total thermal resistance  $R_{thJA}$  (Junction to Ambient) added to  $T_A$  leads to the final junction temperature.  $R_{thJA}$  is the sum of the addition of the two components, Junction to Case and Case to Ambient.

$$R_{thJA} = R_{thJC} + R_{thCA}$$

$$T_J = T_A + \Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}); I_{DD}, I_{OUT} > 0, \text{ if direction is into IC}$$

Example (assuming no load on  $V_{OUT}$  and TLE4997A8 type):

- $V_{DD} = 5 \text{ V}$
- $I_{DD} = 8 \text{ mA}$
- $\Delta T = 150[\text{K/W}] \times (5 [\text{V}] \times 0.008 [\text{A}] + 0 [\text{VA}]) = 6 \text{ K}$

For molded sensors, the calculation with  $R_{thJC}$  is more applicable.

**5.2 Magnetic Characteristics**
**Table 5-2 Magnetic Characteristics**

| Parameter                               | Symbol          | Values     |           |           | Unit                         | Note / Test Condition                   |
|---|-----------------|------------|-----------|-----------|------------------------------|---|
|   |                 | Min.       | Typ.      | Max.      |                              |   |
| Sensitivity                             | $S^{1)}$        | $\pm 12.5$ | –         | $\pm 300$ | mV/mT                        | programmable <sup>2)</sup>              |
| Sensitivity error band over temperature | $S_E$           | -3         |           | 3         | %                            | <sup>3)</sup>                           |
| Magnetic field range                    | MFR             | $\pm 50$   | $\pm 100$ | $\pm 200$ | mT                           | programmable <sup>4)</sup>              |
| Integral nonlinearity                   | INL             | –          | –         | $\pm 15$  | mV                           | $= \pm 0.3\%$ of $V_{DD}$ <sup>5)</sup> |
| Magnetic offset                         | $B_{OS}$        | –          | $\pm 100$ | $\pm 400$ | $\mu\text{T}$                | <sup>6)</sup>                           |
| Magnetic offset drift                   | $\Delta B_{OS}$ | –          | $\pm 1$   | $\pm 5$   | $\mu\text{T}/^\circ\text{C}$ | error band <sup>6)</sup>                |

1) Defined as  $\Delta V_{OUT} / \Delta B$ .

2) Programmable in steps of 0.024%.

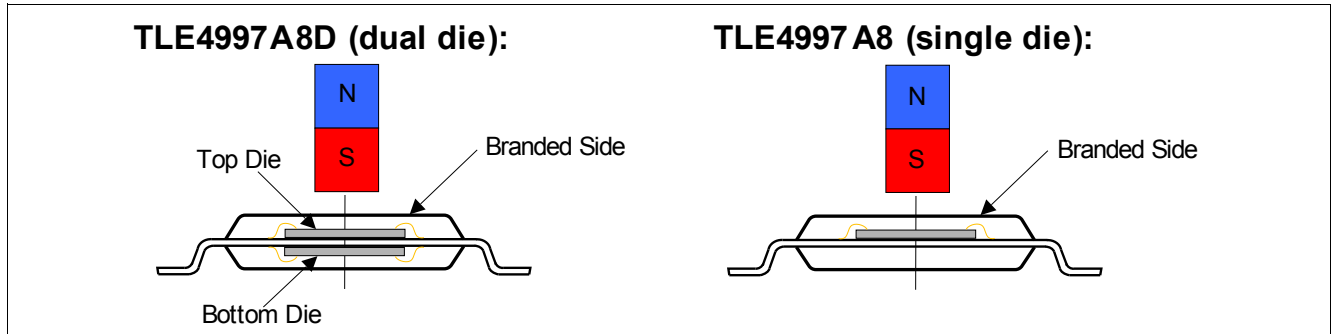
3) Residual sensitivity error band over temperature when using minimum 2 temperatures. Valid in dry state only. Dry is defined after following baking process: 60minutes at  $T=125^\circ\text{C}$

4) Depending on offset and gain settings, the output may already be saturated at lower fields.

5) Range  $\pm 50\text{mT}$  (also valid for ranges  $\pm 100 \text{ mT}$  and  $\pm 200 \text{ mT}$ ). Gain= 1.0 (scales linearly with gain).

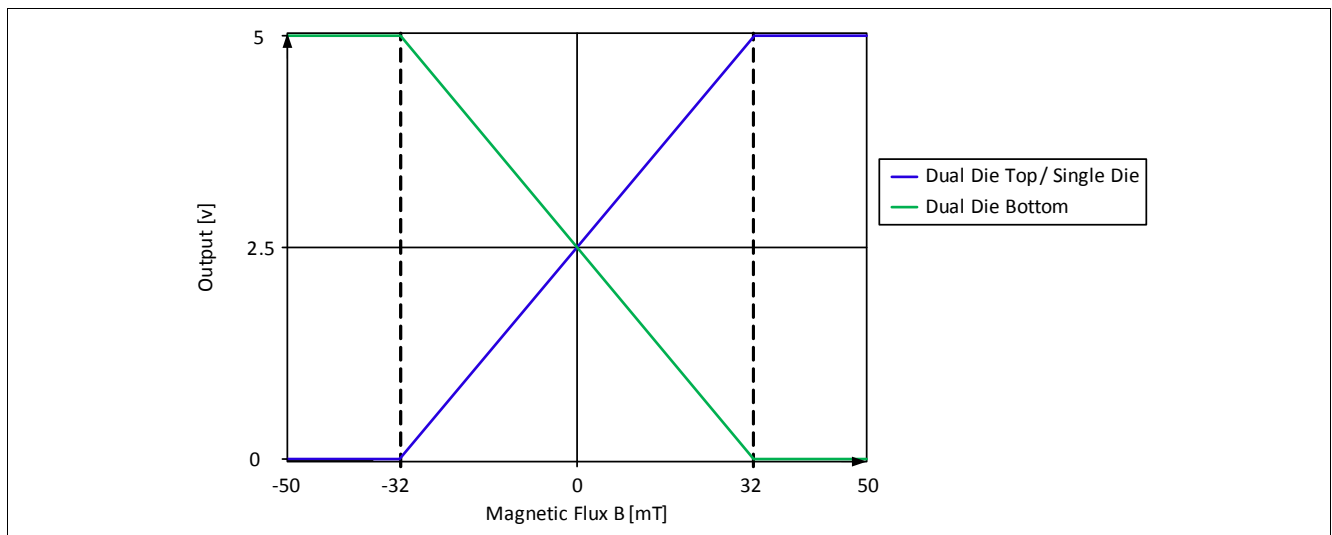
6) For Sensitivity  $S > 25 \text{ mV} / \text{mT}$ . For lower sensitivities, the zero field voltage drift is dominant.

### 5.3 Magnetic Field Direction Definition



**Figure 5-2** Definition of magnetic field direction of the TLE4997A8(D)

Without reconfiguration the bottom die measures the inverted field value of the top die. This leads to the characteristic shown in [Figure 5-3](#).



**Figure 5-3** Example of the dual die output signaling

## 6 Application Circuit

Figure 6-1 shows the connection of two Linear Hall sensors to a micro controller.

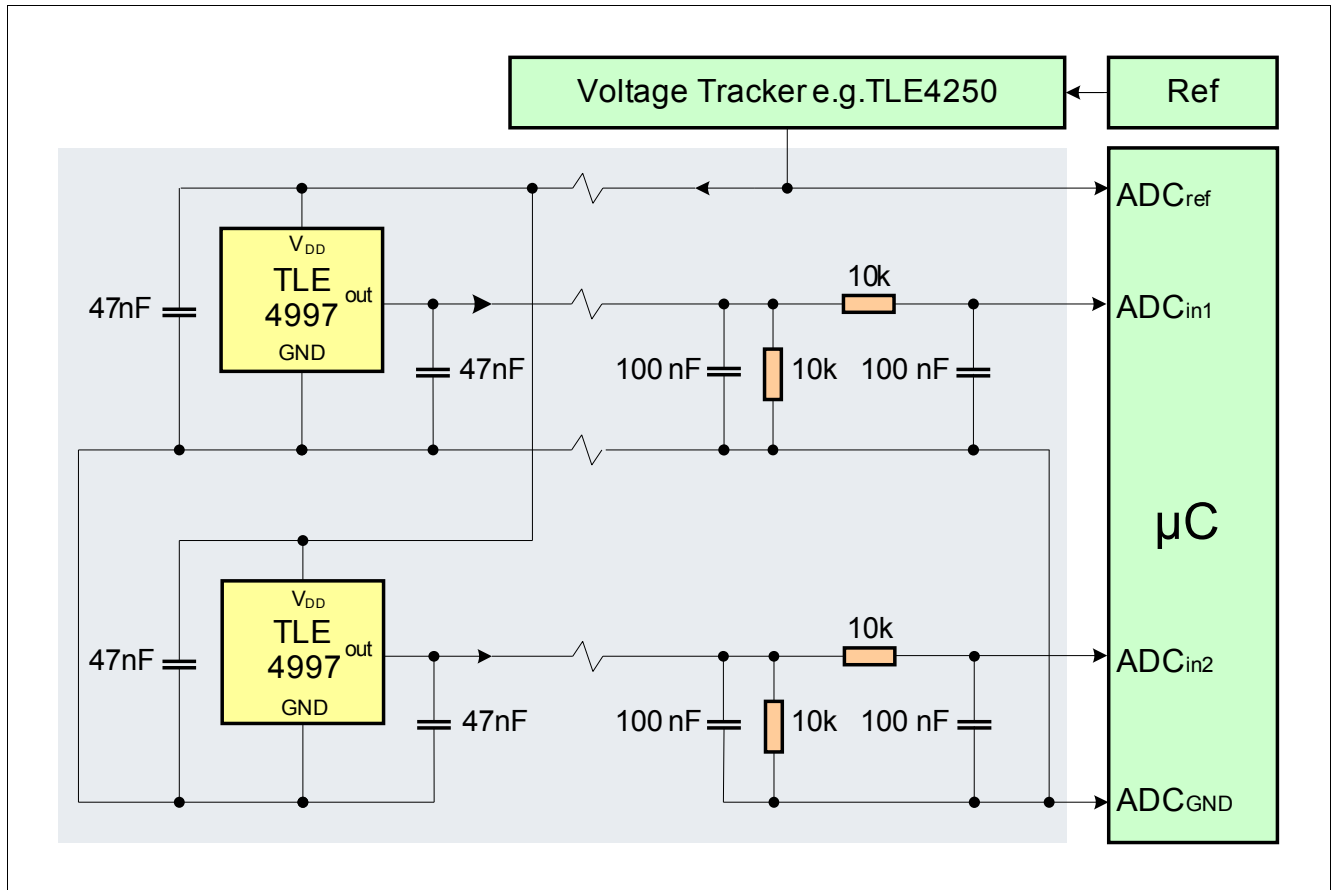


Figure 6-1 Application Circuit

Note: For calibration and programming, the interface has to be connected directly to the OUT pin.

## 7 Configuration and Calibration Parameters

The TLE4997A8(D) has several configurable parameters which are stored in the EEPROM. These parameters affect the internal data processing and compensation and the output protocol. This chapter gives an overview of the parameters. A detailed description of all the parameters and the programming procedure is given in the [TLE4997 User's Manual](#).

**Table 7-1 TLE4997A8(D) Parameters**

| Parameter   | Setting range  | Note   |
|---|--|--|
| Magnetic range  | ±50 mT<br>±100 mT<br>±200 mT   | Magnetic input range of Hall ADC   |
| Gain  | -4.0....3.9998 <sup>1)2)</sup>   | Quantization step: 244.14 ppm  |
| Offset  | -400 %V <sub>DD</sub> ... 399 %V <sub>DD</sub> <sup>3)</sup>               | Quantization step: 1.22mV@V <sub>DD</sub> = 5V                           |
| Clamping low level  | 0 %V <sub>DD</sub> ... 99.98% V <sub>DD</sub>                              | Quantization step: 1.22mV@V <sub>DD</sub> = 5V                           |
| Clamping high level   | 0 %V <sub>DD</sub> ... 99.98% V <sub>DD</sub>                              | Quantization step: 1.22mV@V <sub>DD</sub> = 5V                           |
| Bandwidth <sup>4)</sup>   | 78 Hz<br>244 Hz<br>421 Hz<br>615 Hz<br>826 Hz<br>1060 Hz<br>1320 Hz<br>Off | Low-pass filter cut-off (-3 dB) frequency see <a href="#">Figure 7-1</a> |
| 1 <sup>st</sup> order temperature coefficient TC <sub>1</sub> <sup>5)</sup> | -1000 ppm/°C ... 3000 ppm/°C   | Quantization step: 15.26 ppm/°C  |
| 2 <sup>nd</sup> order temperature coefficient TC <sub>2</sub> <sup>6)</sup> | -6 ppm/°C <sup>2</sup> ... 6 ppm/°C <sup>2</sup>                           | Quantization step: 0.119 ppm/°C <sup>2</sup>                             |

- 1) For gain values between -0.5 and +0.5, the numeric accuracy decreases.
- 2) Gain value of +1.0 corresponds to typical 40mV/mT sensitivity in 100 mT range. Infineon pre-calibrates the samples to 60mV/mT (100mT range).
- 3) Infineon pre-calibrates the samples at zero field to 50% of V<sub>DD</sub> (100mT range)
- 4) Subject to oscillator variation ±25%
- 5) Relative range to Infineon TC<sub>1</sub> temperature pre-calibration, the maximum adjustable range is limited by the register-size and depends on specific pre-calibrated TL setting, full adjustable range: -2441 to +5355 ppm/°C
- 6) Relative range to Infineon TC<sub>2</sub> temperature pre-calibration, the maximum adjustable range is limited by the register-size and depends on specific pre-calibrated TQ setting, full adjustable range: -15 to +15 ppm/°C<sup>2</sup>.



Figure 7-1 shows the filter characteristics as a magnitude plot (the highest setting is marked).

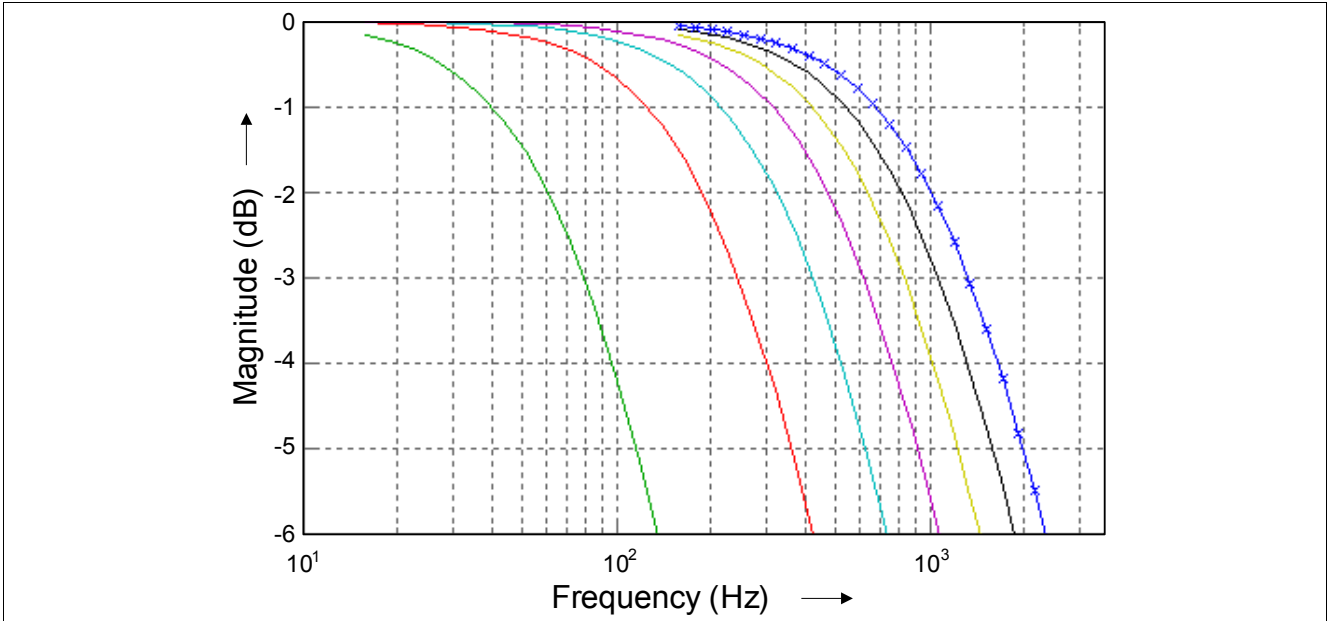


Figure 7-1 DSP Input Filter (Magnitude Plot)

An interpolation filter is placed between the DSP and the output DAC.

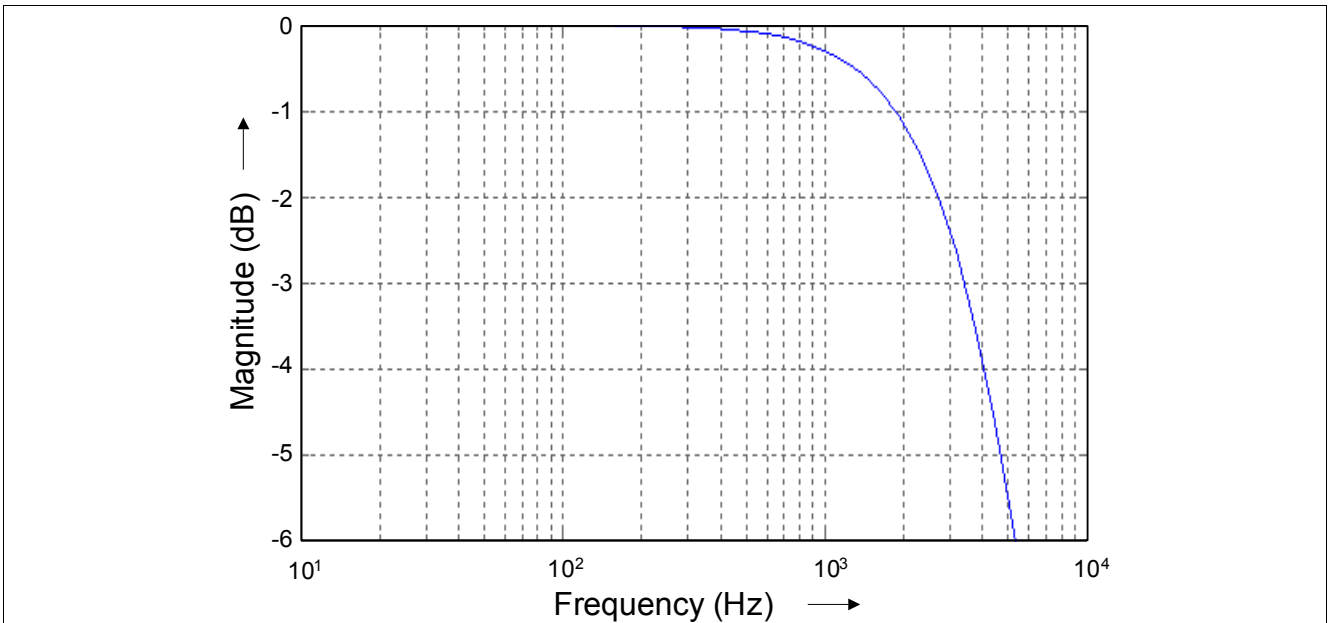


Figure 7-2 DAC Input Filter (Magnitude Plot)

Note: As this is a digital filter running with an RC-based oscillator, the cutoff frequency may vary within  $\pm 25\%$ .

Configuration and Calibration Parameters

Figure 7-3 shows an example in which the magnetic field range between  $B_{min}$  and  $B_{max}$  is mapped to output values between 0.8 V and 4.2 V. If it is not necessary to signal errors, the maximum output voltage range between 0.3 V and 4.7 V can be used.

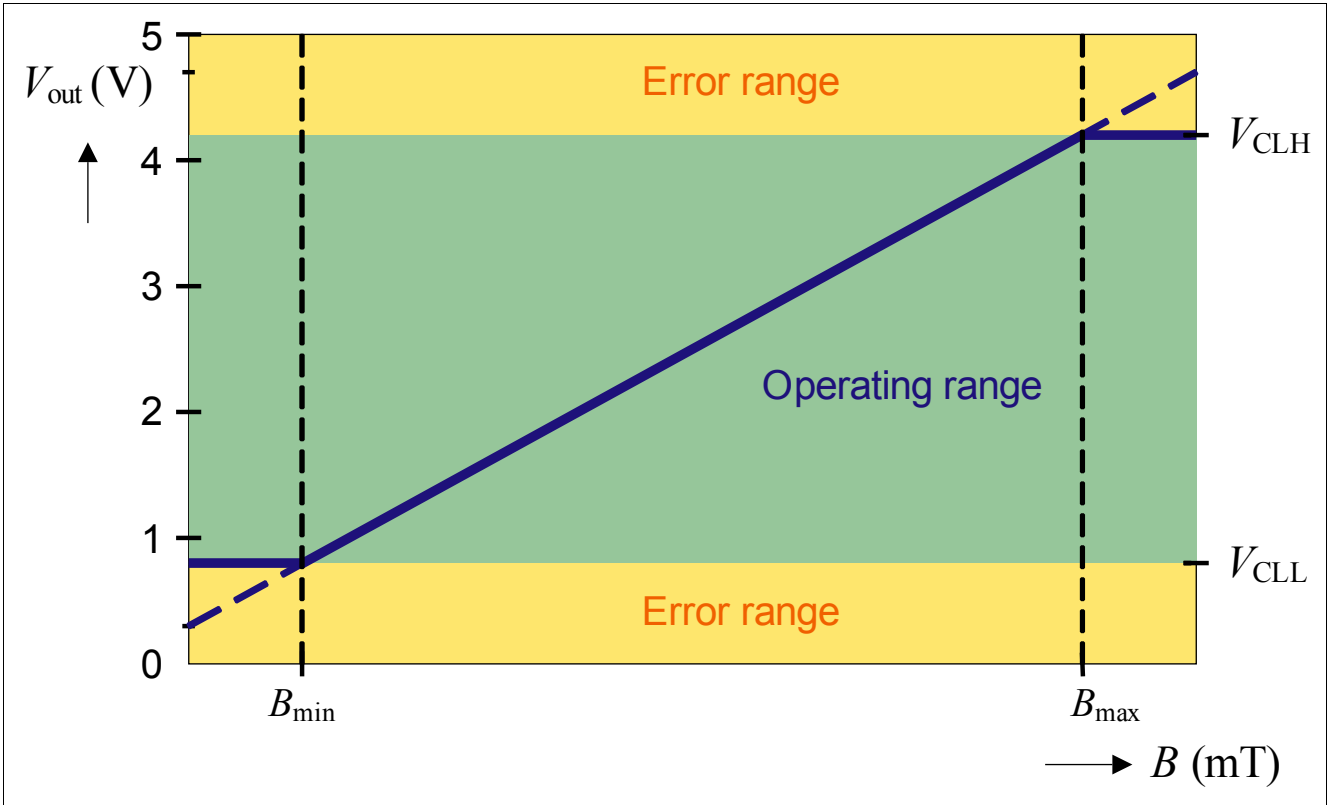


Figure 7-3 Clamping Example

Note: The clamping high value must be above the low value.

## 8 Error Detection

Different error cases can be detected by the On-Board-Diagnostics (OBD) and reported to the micro controller. The OBD is useful only when the clamping function is enabled. It is important to set the clamping threshold values inside the error voltage values shown in [Table 8-1](#) and [Table 8-2](#) to ensure that it is possible to distinguish between correct output voltages and error signals.

### 8.1 Voltages Outside the Operating Range

The output signals an error condition, if  $V_{DD}$  lies:

- Inside the ratings specified in [Table 3-1 “Absolute Maximum Ratings” on Page 8](#)
- Outside the range specified in [Table 4-1 “Operating Range” on Page 9](#)

**Table 8-1 Undervoltage and Overvoltage (All values with  $R_L \geq 10k$ )**

| Parameter                    | Symbol      | Values               |      |      | Unit | Note / Test Condition          |
|------------------------------|-------------|----------------------|------|------|------|--------------------------------|
|                              |             | Min.                 | Typ. | Max. |      |                                |
| Undervoltage threshold       | $V_{DDuv}$  | 3                    | -    | 4    | V    |                                |
| Overvoltage threshold        | $V_{DDov}$  | 7                    | -    | 8.3  | V    |                                |
| Output voltage@ undervoltage | $V_{OUTuv}$ | $0.95 \times V_{DD}$ | -    | -    | V    | $3V \leq V_{DD} \leq V_{DDuv}$ |
| Output voltage@ overvoltage  | $V_{OUTov}$ | $0.97 \times V_{DD}$ | -    | -    | V    | $V_{DDov} < V_{DD} \leq 16 V$  |
| Supply current <sup>1)</sup> | $I_{DDuv}$  | -                    | -    | 10   | mA   | @ undervoltage                 |

1) For overvoltage and reverse voltage, see [Table 3-1 “Absolute Maximum Ratings” on Page 8](#).

### 8.2 Open Circuit of Supply Lines

In the case of interrupted supply lines, the data acquisition device can alert the user. If two sensors are placed in parallel, the output of the remaining working sensor may be still used for an emergency operation.

**Table 8-2 Open Circuit (OBD Parameters)<sup>1)</sup>**

| Parameter                          | Symbol    | Values |      |      | Unit | Note / Test Condition  |
|------------------------------------|-----------|--------|------|------|------|------------------------|
|                                    |           | Min.   | Typ. | Max. |      |                        |
| Output voltage@ open $V_{DD}$ line | $V_{OUT}$ | 0      | -    | 0.18 | V    | $T_J \leq 120^\circ C$ |
| Output voltage@ open GND line      | $V_{OUT}$ | 4.82   | -    | 5    | V    | $T_J \leq 120^\circ C$ |

1) With  $V_{DD} = 5 V$  and  $R_L \geq 10 k\Omega$  pull-down or  $R_L \geq 20 k\Omega$  pull-up.

### 8.3 Not Correctable EEPROM Errors

The parity method is able to correct one single bit in one EEPROM line. One other single bit error in another line can also be detected. As this situation is not correctable, this status is represented at the output pin by clamping the output value to  $V_{DD}$ .

**Table 8-3 EEPROM Error Signalling**

| Parameter                     | Symbol    | Values               |      |          | Unit | Note / Test Condition |
|-------------------------------|-----------|----------------------|------|----------|------|-----------------------|
|                               |           | Min.                 | Typ. | Max.     |      |                       |
| Output voltage @ EEPROM error | $V_{OUT}$ | $0.97 \times V_{DD}$ | -    | $V_{DD}$ | V    |                       |

## 9 PG-TDSO-8 Package Outlines

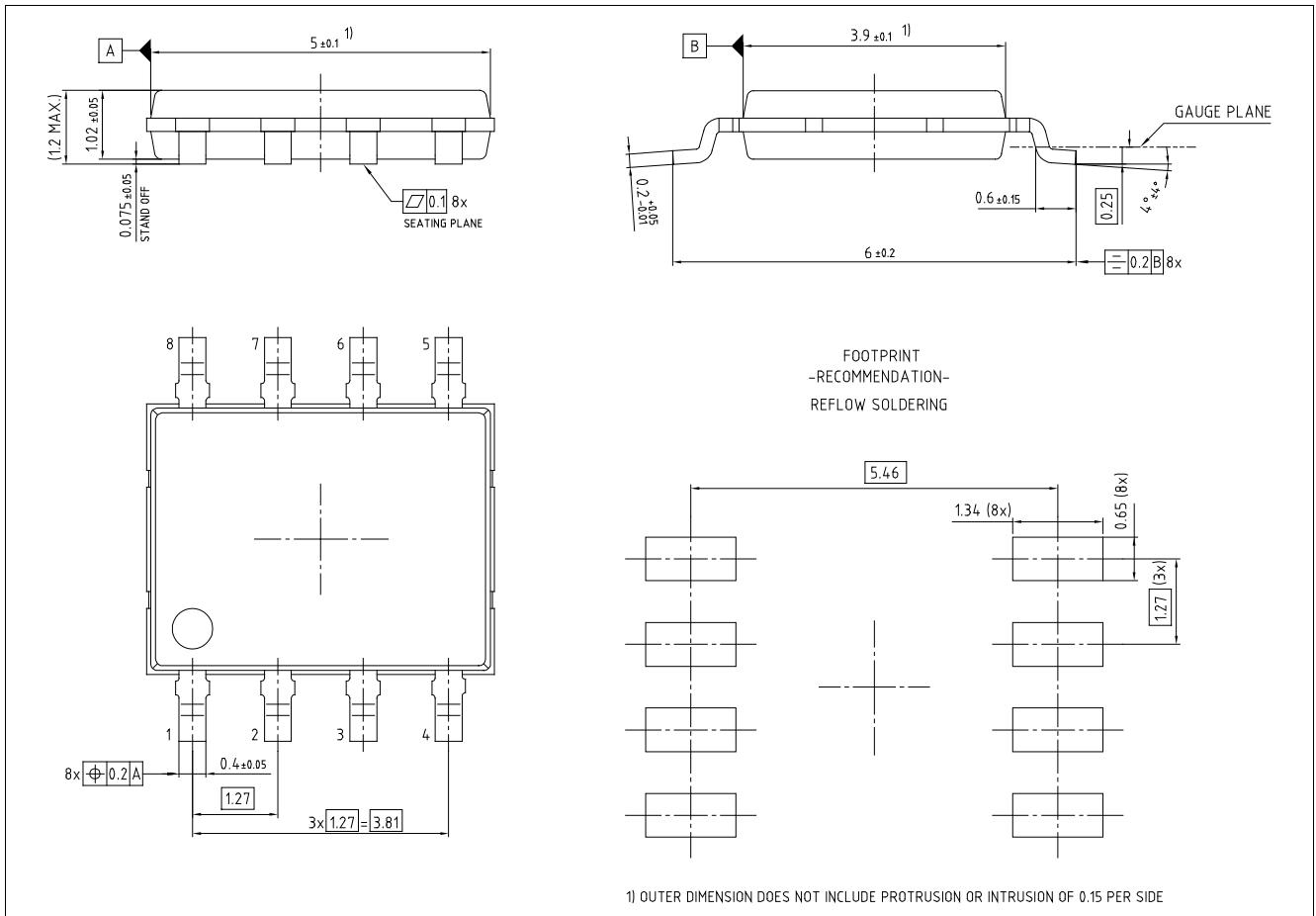


Figure 9-1 PG-TDSO-8 (PG-TDSO-Plastic Green Thin Dual Small Outline), Package Dimensions

### 9.1 Distance Chip to package

Figure 9-2 shows the distance of the chip surface to the PG-TDSO-8 surface.

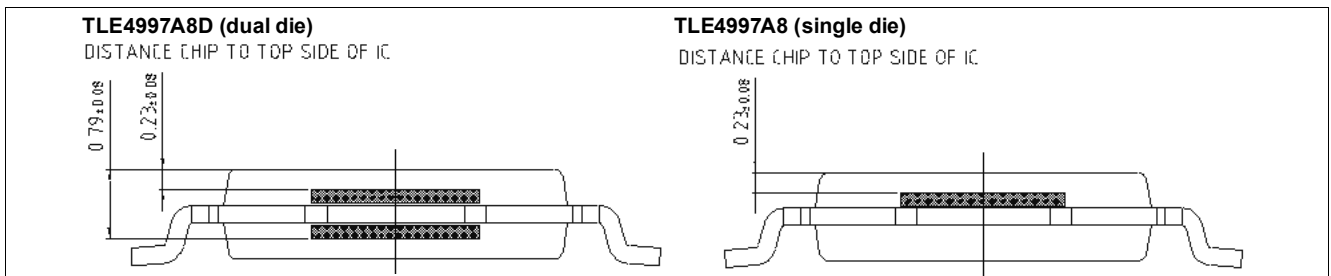


Figure 9-2 Distance of chip surface to package surface

### 9.2 Moisture Sensitivity Level (MSL)

The PG-TDSO-8 fulfills the MSL level 3 according to IPC/JEDEC J-STD-033B.1.

10 PG-TDSO-8 Package Marking

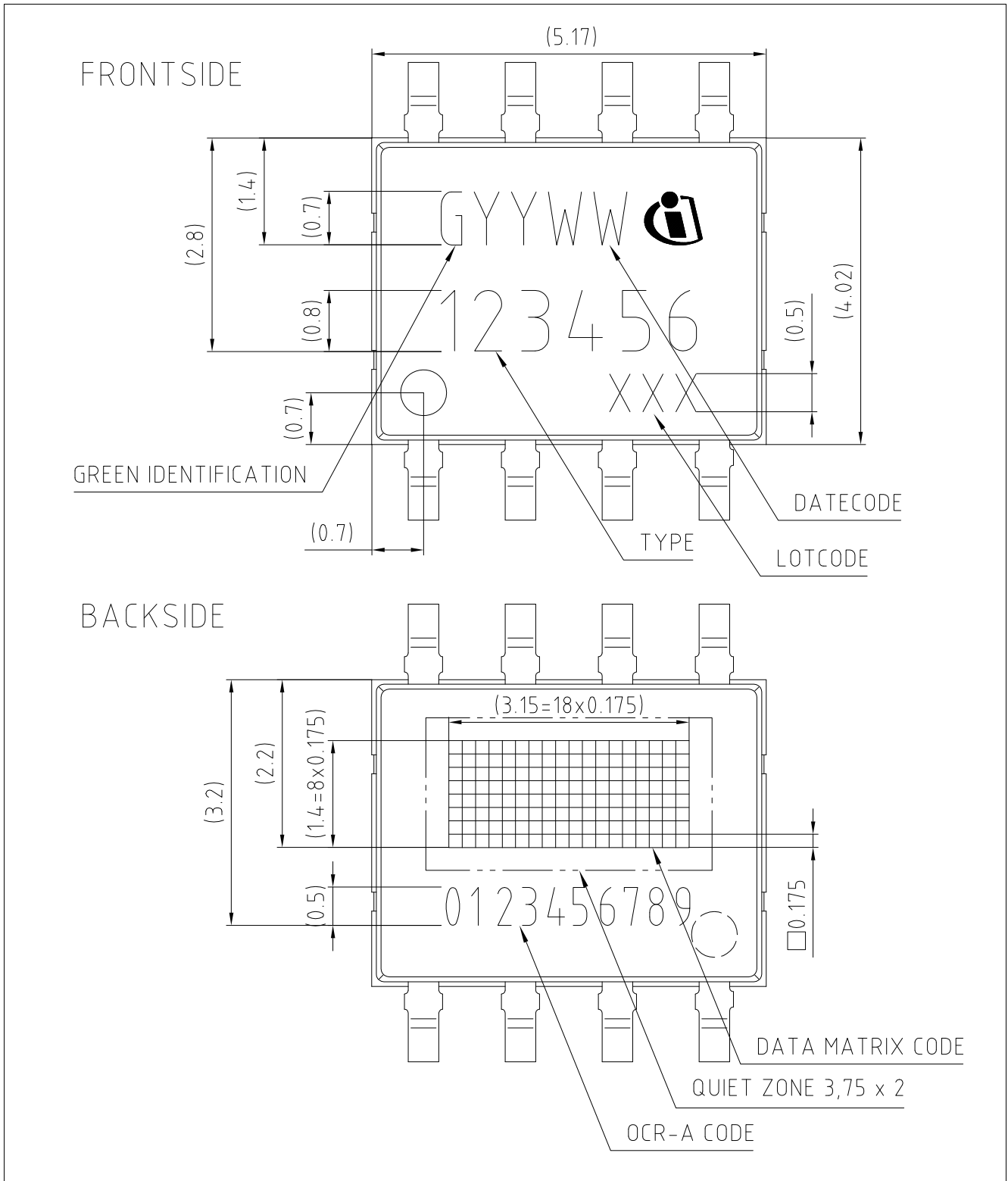


Figure 10-1 PG-TDSO-8 (PG-TDSO-Plastic Green Thin Dual Small Outline), Package Marking

**Revision History**

| Page or Item                 | Subjects (major changes since previous revision) |
|------------------------------|--|
| <b>Revision 1.1, 2018-01</b> |  |
| <b>Page 4</b>                | Removed AEC Q100 revision version                |

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