## Product Summary

| Supply voltage | $\mathrm{V}_{\mathrm{S}}$ | $4.5-32$ | V |
| :--- | :--- | :--- | ---: |
| Drain source voltage | $\mathrm{V}_{\mathrm{DS}(\mathrm{AZ)} \text { max }}$ | 60 | V |
| On resistance | $\mathrm{R}_{\mathrm{ON}}$ | 1.7 | $\Omega$ |
| Output current(each) | $\mathrm{I}_{\mathrm{D}(\mathrm{NOM})}$ | 350 | mA |
| $\quad$ (individ.) |  | 500 | mA |

## Smart Quad Low-Side Switch

## Features

- Shorted circuit protection
- Overtemperature protection
- Overvoltage protection
- Open Load Detection
- Direct parallel control of the inputs
- Inputs high or low active programmable
- General fault flag
- Very low standby quiescent current
- Compatible with 3 V microcontrollers
- Electostatic discharge (ESD) protection


## Application

- $\mu \mathrm{C}$ compatible power switch for 12 V applications
- Switch for automotive and industrial systems
- Line, relay or lamp driver

P-DSO 20-6
Ordering Code:
Q 67006 A9373

## General description

Quad channel Low-Side Switch in Smart Power Technology (SPT) with four separate inputs and four open drain DMOS output stages. The TLE 6225 G is protected by embedded protection functions and designed for automotive and industrial applications, to drive lines, lamps and relays.

## Block Diagram



Pin Description

| Pin | Symbol | Function |
| :---: | :---: | :---: |
| 1 | IN1 | Input Channel 1 |
| 2 | IN2 | Input Channel 2 |
| 3 | FAULT | General Fault Flag |
| 4 | GND | Ground |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 | GND | Ground |
| 8 | VS | Supply Voltage |
| 9 | IN3 | Input Channel 3 |
| 10 | IN4 | Input Channel 4 |
| 11 | ENA | Enable for all channels/Standby |
| 12 | OUT4 | Power Output channel 4 |
| 13 | OUT3 | Power Output channel 3 |
| 14 | GND | Ground |
| 15 | GND | Ground |
| 16 | GND | Ground |
| 17 | GND | Ground |
| 18 | OUT2 | Power Output channel 2 |
| 19 | OUT1 | Power Output channel 1 |
| 20 | PRG | Program (inputs high or low active) |

Pin Configuration (Top view)

| IN1 | $1 \bullet$ | 20 | PRG |
| :--- | :--- | :--- | :--- | :--- |
| IN2 | 2 | 19 | OUT1 |
| FAULT | 3 | 18 | OUT2 |
| GND | 4 | 17 | GND |
| GND | 5 | 16 | GND |
| GND | 6 | 15 | GND |
| GND | 7 | 14 | GND |
| VS | 8 | 13 | OUT3 |
| IN3 | 9 | 12 | OUT4 |
| IN4 | 10 | 11 | ENA |

$\qquad$

## Maximum Ratings for $\mathrm{T}_{\mathrm{j}}=-40^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$

| Parameter | Symbol | Values | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage | $V_{\text {S }}$ | $-0.3 \ldots+40$ | V |
| Continuous Drain Source Voltage (OUT1...OUT4) | $V_{\text {DS }}$ | $-0.7 \ldots+45$ | V |
| Input Voltage, IN1 - IN4 | $V_{\text {IN }}$ | -0.3... + 7 | V |
| Input Voltage, PRG, ENA | $V_{\text {IN }}$ | -0.3 ... +40 | V |
| Output Load Dump Protection $V_{\text {Load Dump }}=U_{P}+U_{S} ; U_{P}=13.5 \mathrm{~V}$ With Automotive Relay Load $R_{\mathrm{L}}=70 \Omega$ $R_{\mid}{ }^{1}=2 \Omega ; t_{\mathrm{d}}=400 \mathrm{~ms} ; \operatorname{IN}=$ low or high | $V_{\text {Load Dump }}{ }^{2}$ ) | 75 | V |
| $\overline{\text { FAULT Output Voltage }}$ | $V_{\text {Fault }}$ | $-0.3 \ldots+40$ | V |
| Operating Temperature Range <br> Storage Temperature Range | $\begin{aligned} & \hline T_{\mathrm{j}} \\ & T_{\mathrm{stg}} \end{aligned}$ | $\begin{aligned} & -40 \ldots+150 \\ & -55 \ldots+150 \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ |
| Output Current per Channel (see electrical characteristics) | $I_{\text {D (im) }}$ | $I_{\text {D(im) min }}$ | A |
| Output Clamping Energy $I_{D}=0.2 \mathrm{~A}$ | $E_{\text {AS }}$ | 10 | mJ |
| Power Dissipation (DC) @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (on PCB $6 \mathrm{~cm}^{2}$ cooling area) | $P_{\text {tot }}$ | 2.5 | W |
| Electrostatic Discharge Voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1-1993 | $V_{\text {ESD }}$ | 2000 | V |
| DIN Humidity Category, DIN 40040 |  | E |  |
| IEC Climatic Category, DIN IEC 68-1 |  | 40/150/56 |  |
| ```Thermal Resistance junction - pin junction - ambient @ min. footprint junction - ambient @ 6 cm``` | $R_{\text {thJP }}$ <br> $R_{\text {thJA }}$ <br> $R_{\text {thJA }}$ | 23 80 45 | K/W |

[^0]
## Electrical Characteristics

## Parameter and Conditions

$\mathrm{V}_{\mathrm{S}}=4.5$ to $32 \mathrm{~V} ; \mathrm{T}_{\mathrm{j}}=-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ (unless otherwise specified)

| Symbol | Values |  |  | Unit |
| :---: | :---: | :---: | :---: | :--- |
|  | min | typ | $\max$ |  |

## 1. Power Supply

| Supply Voltage | $V_{\mathrm{S}}$ | 4.5 |  | 32 | V |
| :--- | :--- | ---: | ---: | ---: | ---: |
| Supply Current (ENA $=\mathrm{H}$, Outputs ON) | $I_{(O \mathrm{ON})}$ |  | 1 | 2 | mA |
| Supply Current in Standby Mode (ENA $=\mathrm{L})$ | $I_{S(\text { stby })}$ |  |  | 10 | $\mu \mathrm{~A}$ |

## 2. Power Outputs

| ON Resistance $\mathrm{V}_{\mathrm{S}} \geq 6 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=300 \mathrm{~mA}$ $\mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ <br>  $\mathrm{T}_{\mathrm{J}}=150^{\circ} \mathrm{C}$ | $R_{\text {DS(ON) }}$ |  | 1.7 3 | 2 3.6 | $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Clamping Voltage Output OFF | $V_{\text {DS(AZ) }}$ | 45 | 50 | 60 | V |
| Current Limit | $I_{\text {D(im) }}$ | 500 | 750 | 1000 | mA |
| Output Leakage Current $\quad \mathrm{V}_{\text {ENA }}=\mathrm{L}$ | $I_{\text {D(kg) }}$ |  |  | 5 | $\mu \mathrm{A}$ |
| Turn-On Time $\quad \mathrm{I}_{\mathrm{D}}=200 \mathrm{~mA}$, resistive load | $t_{\text {ON }}$ |  | 5 | 10 | $\mu \mathrm{s}$ |
| Turn-Off Time $\quad \mathrm{I}_{\mathrm{D}}=200 \mathrm{~mA}$, resistive load | $t_{\text {OFF }}$ |  | 5 | 10 | $\mu \mathrm{s}$ |

## 3. Digital Inputs (IN1 - IN4, ENA, PRG)

| Input Low Voltage (IN1 - IN4, PRG) | $V_{\text {INL }}$ | -0.3 |  | 1 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Low Voltage (ENA) | $V_{\text {INL }}$ | -0.3 |  | 0.8 | V |
| Input High Voltage | $V_{\text {INH }}$ | 2.0 |  |  | V |
| Input Voltage Hysteresis (IN1 - IN4, PRG) | $V_{\text {INHys }}$ | 50 | 100 |  | mV |
| Input Voltage Hysteresis (ENA) | $V_{\text {INHys }}$ | 20 | 100 |  | mV |
| Input Pull Up Current (IN1...IN4) @ PRG = L, $\mathrm{V}_{\mathbb{I N}}=0 \mathrm{~V}$ | $I_{\text {IN( } 1.4) \mathrm{PU}}$ | 20 | 50 | 100 | $\mu \mathrm{A}$ |
| Input Pull Down Current (IN1...IN4) @ PRG = H, $\mathrm{V}_{\text {IN }}<\mathrm{V}_{\mathrm{S}} ; \mathrm{V}_{\text {IN }}<6$ | $I_{1 N(1.4) \mathrm{PD}}$ | 20 | 50 | 100 | $\mu \mathrm{A}$ |
| PRG, ENA Pull Down Current $\quad \mathrm{V}_{\text {IN }}=5 \mathrm{~V}$ | $I_{\text {IN(PRG, ENA })}$ | 20 | 50 | 100 | $\mu \mathrm{A}$ |
| PRG, ENA Pull Down Current $\quad \mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ | $I_{\text {IN(PRG, ENA })}$ |  |  | 200 | $\mu \mathrm{A}$ |

## 4. Digital Output ( $\overline{\text { FAULT }}$ )

| FAULT Output Low Voltage | $\mathrm{I}_{\text {FAULT }}=1.6 \mathrm{~mA}$ | $V_{\text {FAULTL }}$ |  |  | 0.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

5. Diagnostic Functions

| Open Load/Short to Ground Detection Voltage | $V_{\mathrm{DS}(\mathrm{OL})}$ | $0.4^{*} \mathrm{~V}_{\mathrm{S}}$ | $0.5^{*} \mathrm{~V}_{\mathrm{S}}$ | $0.6^{*} \mathrm{~V}_{\mathrm{S}}$ | V |
| :--- | :--- | ---: | ---: | ---: | ---: |
| Output Pull Down Current | $I_{\mathrm{PD}(\mathrm{OL})}$ | 20 | 50 | 200 | $\mu \mathrm{~A}$ |
| Fault Delay Time; $\mathrm{V}_{\mathrm{S}}=12 \mathrm{~V}$ | $t_{\mathrm{d}(\text { faut })}$ | 50 | 100 | 200 | $\mu \mathrm{~s}$ |
| Overtemperature Shutdown Threshold | $T_{\text {th(sd) }}$ | 170 |  | 200 | ${ }^{\circ} \mathrm{C}$ |
| Hysteresis | $T_{\text {hys }}$ |  | 10 |  | K |

## Functional Description

The TLE 6225 G is a quad channel low-side switch with four power DMOS stages. The power transistors are protected against short to $\mathrm{V}_{\mathrm{BB}}$, overload, overtemperature and against overvoltage by zenerclamp.
The diagnostic logic recognises a fault condition which is indicated by a fault flag.

## Circuit Description

## Output Stage Control

Each output is independently controlled by an input pin and a common enable line, which enables/disables all four outputs. The parallel inputs are high or low active depending on the PRG pin. If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the outputs 1 to 4 are switched OFF. ENA - and PRG - pin itself are internally pulled down when they are not connected.

| ENA - Enable pin. | ENA $=$ High: <br> ENA $=$ Low (GND): |
| :--- | :--- |
| Active mode. Channels are enabled |  |
| Sleep mode. Channels are switched off. Less than |  |
| $1 \mu$ A current consumption. |  |

## Power Transistors

Each of the four output stages has its own zenerclamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. The outputs are provided with a current limitation set to a minimum of 500 mA .
Each output is protected by embedded protection functions ${ }^{3)}$. In the event of an overload or short to supply, the current is internally limited. If this operation leads to an overtemperature condition, a second protection level (about $170^{\circ} \mathrm{C}$ ) will turn the effected output into a PWMmode (selective thermal shutdown with restart) to prevent critical chip temperatures. The temperature hysteresis is typically 10 K .

## Diagnostic

The FAULT pin is an open drain output. The logic status depends on the programming pin PRG.

$$
\begin{array}{lll}
\hline \text { FAULT }- \text { pin. } & \overline{\text { FAULT }}=\text { High } & \text { no fault @ PRG }=\text { High } \\
& \overline{\text { FAULT }}=\text { Low } & \text { no fault @ PRG }=\text { Low }
\end{array}
$$

[^1]Diagnostic Table

| Operating Condition | Enable <br> Input | Program <br> Input | Control <br> Input | Power <br> Output | Diagnostic <br> Output |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | ENA | PRG | IN | OUT | $\overline{\text { FAULT }}$ |
| Standby | L | X | X | OFF | H |
| Normal function | H | L | L | ON | L |
|  | H | L | H | OFF | L |
|  | H | H | L | OFF | H |
| Overtemperature | H | H | H | ON | H |
| Open load or short to ground | H | L | L | ON | L |
|  | H | L | L | OFF * | H |
|  | H | L | H | OFF | H |
|  | H | H | L | OFF | L |
|  | H | H | H | ON | H |

$X=$ not relevant
*selective thermal shutdown for each channel at overtemperature

## Fault Distinction

Open load/short to ground is recognised in OFF-state. Overtemperature as a result of an overload or short to battery can only arise in ON-state. If there is only one fault at a time, it is possible to distinguish which channel is affected with which fault.
$\qquad$

## Typical electrical Characteristics

## Drain-Source on-resistance

$R_{D S(O N)}=f\left(T_{j}\right) ; V_{s}=5 \mathrm{~V}$


Figure 6 : Typical ON Resistance versus Junction-Temperature Channel 1-4

## Output Clamping Voltage

$V_{D S(A Z)}=f\left(T_{j}\right) ; V_{s}=5 \mathrm{~V}$


Figure 7 : Typical Clamp Voltage versus Junction-Temperature Channel 1-4
$\qquad$

## Timing Diagrams

## Power Outputs



## Application Circuit



## Package and ordering code

all dimensions in $\mathbf{m m}$

| P- DSO-20-6 | Ordering code |
| :---: | :---: |
| TLE 6225 G | Q 67006 A9373 |



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[^0]:    ${ }^{\text {1) }} R_{1}$ =internal resistance of the load dump test pulse generator LD200
    ${ }^{2}$ ) $V_{\text {LoadDump }}$ is setup without DUT connected to the generator per ISO 7637-1 and DIN 40839.

[^1]:    ${ }^{3)}$ The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently

