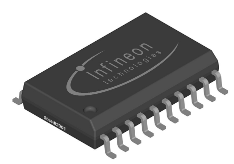
Smart Quad Low-Side Switch

Features

- Shorted circuit protection
- Overtemperature protection
- Overvoltage protection
- Open Load Detection
- Direct parallel control of the inputs
- Inputs high or low active programmable
- General fault flag
- Very low standby quiescent current
- Compatible with 3V microcontrollers
- **E**lecto**st**atic **d**ischarge (ESD) protection

Product Summary

Supply voltage	V_S	4.5 – 32	V
Drain source voltage	$V_{DS(AZ)max}$	60	V
On resistance	R_{ON}	1.7	Ω
Output current (each)	$I_{D(NOM)}$	350	mA
(individ.)		500	mA



P-DSO 20-6
Ordering Code:
Q 67006 A9373

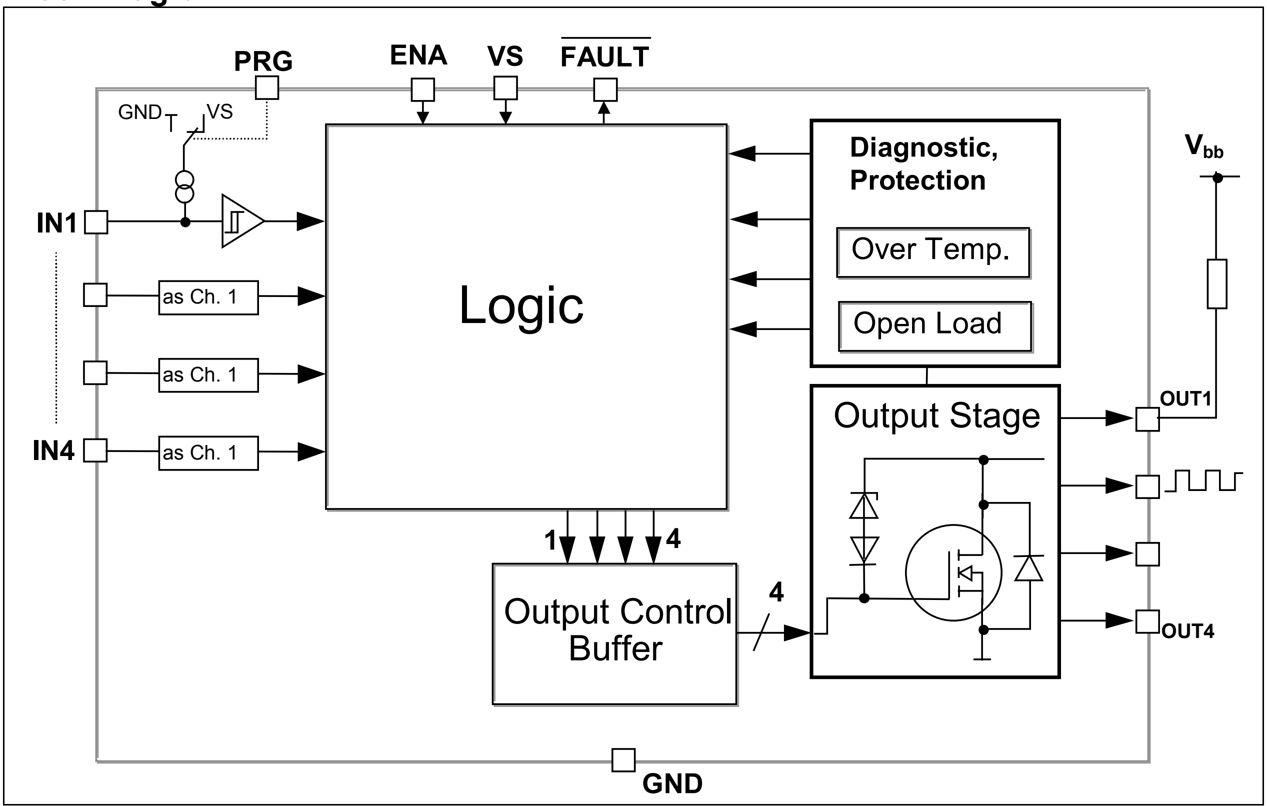
Application

- µC compatible power switch for 12 V applications
- Switch for automotive and industrial systems
- Line, relay or lamp driver

General description

Quad channel Low-Side Switch in Smart Power Technology (SPT) with four separate inputs and four open drain DMOS output stages. The TLE 6225 G is protected by embedded protection functions and designed for automotive and industrial applications, to drive lines, lamps and relays.

Block Diagram



Pin Description

Pin	Symbol	Function
1	IN1	Input Channel 1
2	IN2	Input Channel 2
3	$\overline{\text{FAULT}}$	General Fault Flag
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	VS	Supply Voltage
9	IN3	Input Channel 3
10	IN4	Input Channel 4
11	ENA	Enable for all channels/Standby
12	OUT4	Power Output channel 4
13	OUT3	Power Output channel 3
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	OUT2	Power Output channel 2
19	OUT1	Power Output channel 1
20	PRG	Program (inputs high or low active)

Pin Configuration (Top view)

IN1	1•	20	PRG
IN2	2	19	OUT1
$\overline{\text{FAULT}}$	3	18	OUT2
GND	4	17	GND
GND	5	16	GND
GND	6	15	GND
GND	7	14	GND
VS	8	13	OUT3
IN3	9	12	OUT4
IN4	10	11	ENA

P-DSO-20-6

Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply Voltage	V_S	-0.3 ... +40	V
Continuous Drain Source Voltage (OUT1...OUT4)	V_{DS}	-0.7 ... +45	V
Input Voltage, IN1 - IN4	V_{IN}	- 0.3 ... + 7	V
Input Voltage, PRG, ENA	V_{IN}	- 0.3 ... + 40	V
Output Load Dump Protection $V_{Load\ Dump}=U_P+U_S$; U_P=13.5 V With Automotive Relay Load R_L = 70 Ω R_I[1]=2 Ω; t_d=400ms; IN = low or high	$V_{Load\ Dump}$[2]	75	V
$\overline{\text{FAULT}}$ Output Voltage	V_{Fault}	- 0.3 ... + 40	V
Operating Temperature Range Storage Temperature Range	T_j T_{stg}	- 40 ... + 150 - 55 ... + 150	°C
Output Current per Channel (see electrical characteristics)	$I_{D(lim)}$	$I_{D(lim)\ min}$	A
Output Clamping Energy I_D= 0.2 A	E_{AS}	10	mJ
Power Dissipation (DC) @ T_A = 25 °C (on PCB 6 cm^2 cooling area)	P_{tot}	2.5	W
Electro**s**tatic **D**ischarge Voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2000	V
DIN Humidity Category, DIN 40 040		E	
IEC Climatic Category, DIN IEC 68-1		40/150/56	
Thermal Resistance junction - pin junction - ambient @ min. footprint junction - ambient @ 6 cm^2 cooling area	 R_{thJP} R_{thJA} R_{thJA}	 23 80 45	 K/W

[1] R_I=internal resistance of the load dump test pulse generator LD200
[2] $V_{LoadDump}$ is setup without DUT connected to the generator per ISO 7637-1 and DIN 40 839.

Electrical Characteristics

Parameter and Conditions V_S = 4.5 to 32 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
1. Power Supply						
Supply Voltage		V_S	4.5		32	V
Supply Current (ENA = H, Outputs ON)		$I_{S(ON)}$		1	2	mA
Supply Current in Standby Mode (ENA = L)		$I_{S(stby)}$			10	µA
2. Power Outputs						
ON Resistance $V_S \geq 6$ V; I_D = 300 mA	T_J = 25°C T_J = 150°C	$R_{DS(ON)}$		1.7 3	2 3.6	Ω
Output Clamping Voltage	Output OFF	$V_{DS(AZ)}$	45	50	60	V
Current Limit		$I_{D(lim)}$	500	750	1000	mA
Output Leakage Current	V_{ENA} = L	$I_{D(lkg)}$			5	µA
Turn-On Time	I_D = 200 mA, resistive load	t_{ON}		5	10	µs
Turn-Off Time	I_D = 200 mA, resistive load	t_{OFF}		5	10	µs
3. Digital Inputs (IN1 – IN4, ENA, PRG)						
Input Low Voltage (IN1 – IN4, PRG)		V_{INL}	- 0.3		1	V
Input Low Voltage (ENA)		V_{INL}	- 0.3		0.8	V
Input High Voltage		V_{INH}	2.0			V
Input Voltage Hysteresis (IN1 – IN4, PRG)		V_{INHys}	50	100		mV
Input Voltage Hysteresis (ENA)		V_{INHys}	20	100		mV
Input Pull Up Current (IN1...IN4) @ PRG = L, V_{IN} = 0V		$I_{IN(1..4)PU}$	20	50	100	µA
Input Pull Down Current (IN1...IN4) @ PRG = H, $V_{IN} < V_S$; $V_{IN} < 6$		$I_{IN(1..4)PD}$	20	50	100	µA
PRG, ENA Pull Down Current	V_{IN} = 5 V	$I_{IN(PRG,ENA)}$	20	50	100	µA
PRG, ENA Pull Down Current	V_{IN} = 14 V	$I_{IN(PRG,ENA)}$			200	µA
4. Digital Output ($\overline{\text{FAULT}}$)						
$\overline{\text{FAULT}}$ Output Low Voltage	I_{FAULT} = 1.6 mA	V_{FAULTL}			0.4	V
5. Diagnostic Functions						
Open Load/Short to Ground Detection Voltage		$V_{DS(OL)}$	0.4*V_S	0.5*V_S	0.6*V_S	V
Output Pull Down Current		$I_{PD(OL)}$	20	50	200	µA
Fault Delay Time; V_S = 12V		$t_{d(fault)}$	50	100	200	µs
Overtemperature Shutdown Threshold Hysteresis		$T_{th(sd)}$ T_{hys}	170	 10	200	°C K

Functional Description

The TLE 6225 G is a quad channel low-side switch with four power DMOS stages. The power transistors are protected against short to V_{BB}, overload, overtemperature and against overvoltage by zenerclamp.
The diagnostic logic recognises a fault condition which is indicated by a fault flag.

Circuit Description

Output Stage Control

Each output is independently controlled by an input pin and a common enable line, which enables/disables all four outputs. The parallel inputs are high or low active depending on the PRG pin. If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the outputs 1 to 4 are switched OFF. ENA - and PRG - pin itself are internally pulled down when they are not connected.

ENA - Enable pin.	ENA = High:	Active mode. Channels are enabled
	ENA = Low (GND):	Sleep mode. Channels are switched off. Less than 1 µA current consumption.
PRG - Program pin.	PRG = High:	Parallel inputs Channel 1 to 4 are high active
	PRG = Low (GND):	Parallel inputs Channel 1 to 4 are low active.

Power Transistors

Each of the four output stages has its own zenerclamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. The outputs are provided with a current limitation set to a minimum of 500 mA.
Each output is protected by embedded protection functions[3)]. In the event of an overload or short to supply, the current is internally limited. If this operation leads to an overtemperature condition, a second protection level (about 170 °C) will turn the effected output into a PWM-mode (selective thermal shutdown with restart) to prevent critical chip temperatures. The temperature hysteresis is typically 10K.

Diagnostic

The $\overline{\text{FAULT}}$ pin is an open drain output. The logic status depends on the programming pin PRG.

$\overline{\text{FAULT}}$ - pin.	$\overline{\text{FAULT}}$ = High	no fault @ PRG = High
	$\overline{\text{FAULT}}$ = Low	no fault @ PRG = Low

[3)] The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently

Diagnostic Table

Operating Condition	Enable Input **ENA**	Program Input **PRG**	Control Input **IN**	Power Output **OUT**	Diagnostic Output $\overline{\textbf{FAULT}}$
Standby	L	X	X	OFF	H
Normal function	H H H H	L L H H	L H L H	ON OFF OFF ON	L L H H
Overtemperature	H H	L H	L H	OFF * OFF *	H L
Open load or short to ground	H H H H	L L H H	L H L H	ON OFF OFF ON	L H L H

X = not relevant

*selective thermal shutdown for each channel at overtemperature

Fault Distinction
Open load/short to ground is recognised in OFF-state. Overtemperature as a result of an overload or short to battery can only arise in ON-state. If there is only one fault at a time, it is possible to distinguish which channel is affected with which fault.

Typical electrical Characteristics

Drain-Source on-resistance

$R_{DS(ON)} = f(T_j)$; $V_s = 5V$

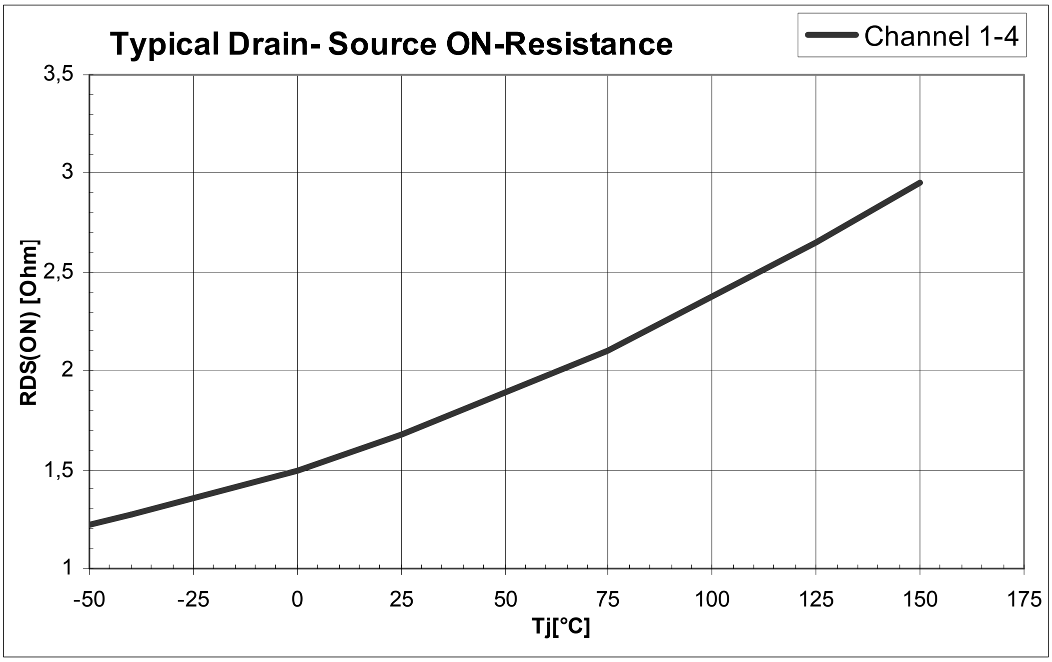


Figure 6 : Typical ON Resistance versus Junction-Temperature Channel 1-4

Output Clamping Voltage

$V_{DS(AZ)} = f(T_j)$; $V_s = 5V$

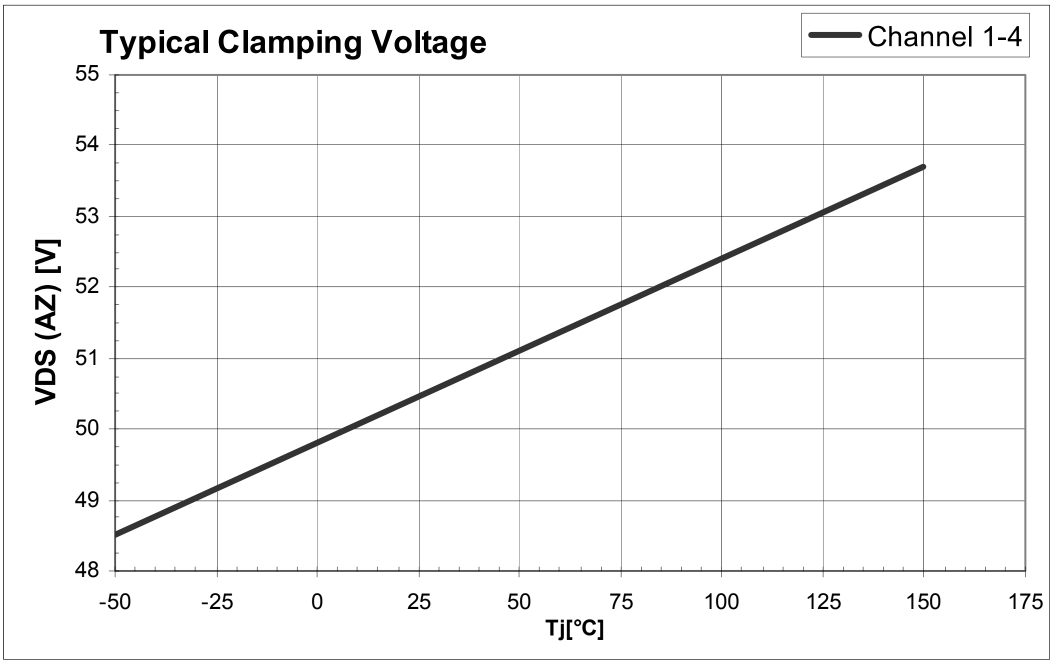
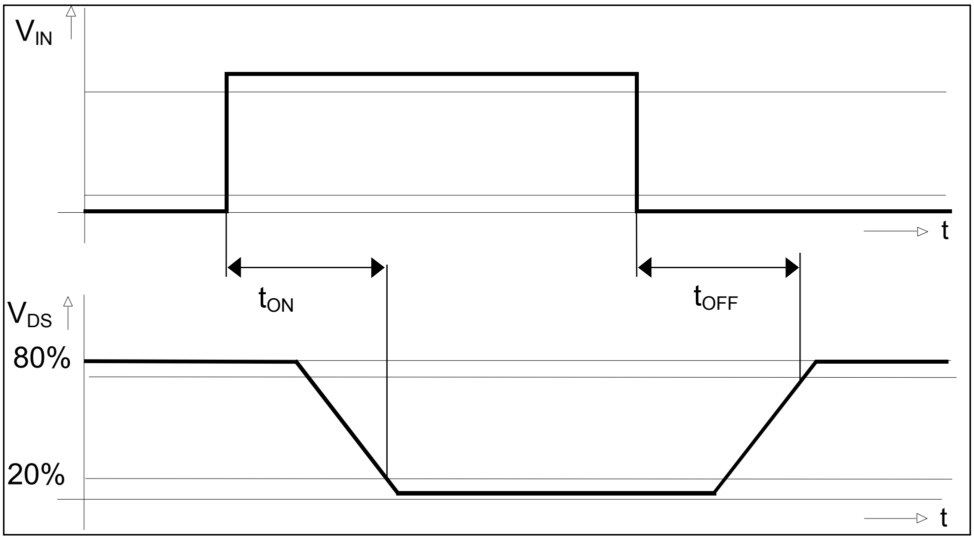


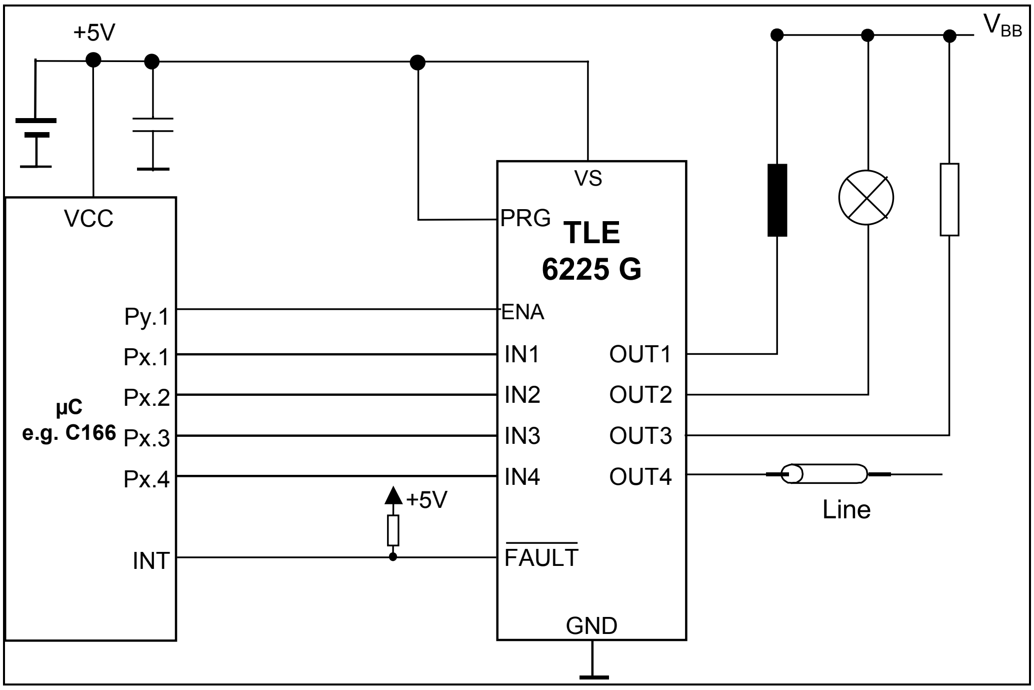
Figure 7 : Typical Clamp Voltage versus Junction-Temperature Channel 1-4

Timing Diagrams

Power Outputs



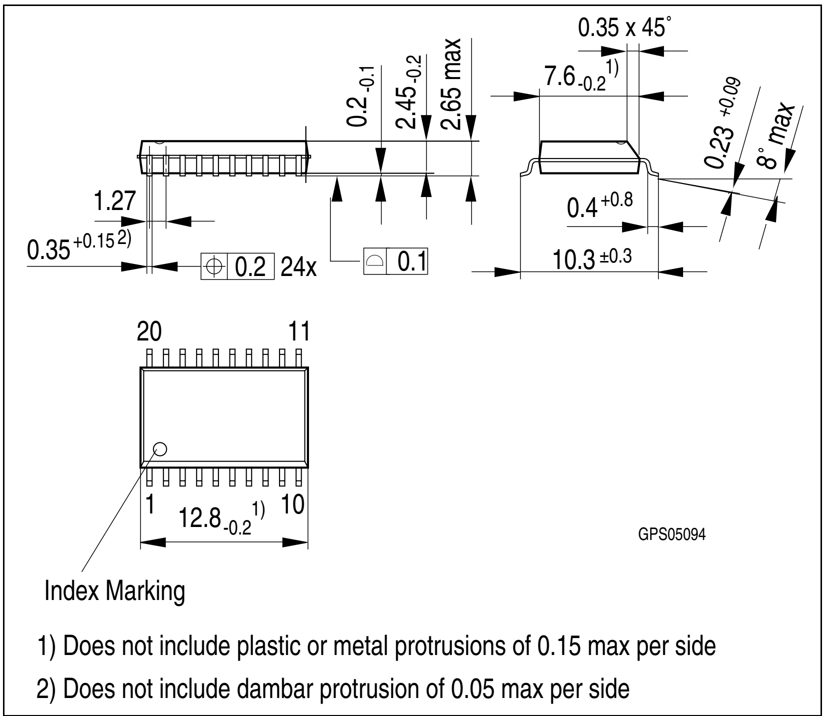
Application Circuit



Package and ordering code

all dimensions in mm

P - DSO - 20 - 6	Ordering code
TLE 6225 G	Q 67006 A9373



Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 76,
D-81541 München