Never stop thinking

TLE6240GP

Smart 16-Channel Low-Side Switch
coreFLEX

Data Sheet

Rev.3.3, 2010-02-15

Automotive Power

Table of Contents

1 Overview

PG-DSO-36

Features

- Short Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- 16 bit Serial Data Input and Diagnostic Output
  (2 bit/channel for Open Load- and Short to GND detection)
- Direct Parallel Control of eight channels for PWM Applications
- Parallel Inputs High or Low Active programmable
- General Fault Flag
- Low Quiescent Current
- Compatible with 3 V Microcontrollers
- Electrostatic discharge (ESD) Protection
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Automotive and Industrial Systems
- Solenoids, Relays and Resistive Loads

General Description

16-fold Low-Side Switch in Smart Power Technology (SPT) with a Serial Peripheral Interface (SPI) and 16 open drain DMOS output stages. The TLE6240GP is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via SPI Interface. Additionally 8 channels can be controlled direct in parallel for PWM applications. Therefore the TLE6240GP is particularly suitable for engine management and powertrain systems, safety and body applications.

Type	Package	Marking
TLE6240GP	PG-DSO-36	TLE6240GP

Product Summary

Parameter	Symbol	Value	Unit
Supply voltage	V_S	4.5 … 5.5	V
Drain source clamping voltage	$V_{DS(AZ)max}$	45 60	V
On resistance	$R_{ON1\text{-}8\ (max\ @\ 150°C)}$	2.2	Ω
	$R_{ON10,11,14,15\ (max\ @\ 150°C)}$	0.7	Ω
	$R_{ON9,12,13,16\ (max\ @\ 150°C)}$	0.6	Ω
Nominal Output current (channel 1 - 8)	I_D	0.5	A
Nominal Output current (channel 9 - 16)	I_D	1	A
Minimum Output current Limit (channel 1 - 8)	$I_{D(lim)\_min}$	1	A
Minimum Output current Limit (channel 9 - 16)	$I_{D(lim)\_min}$	3	A

Block Diagram

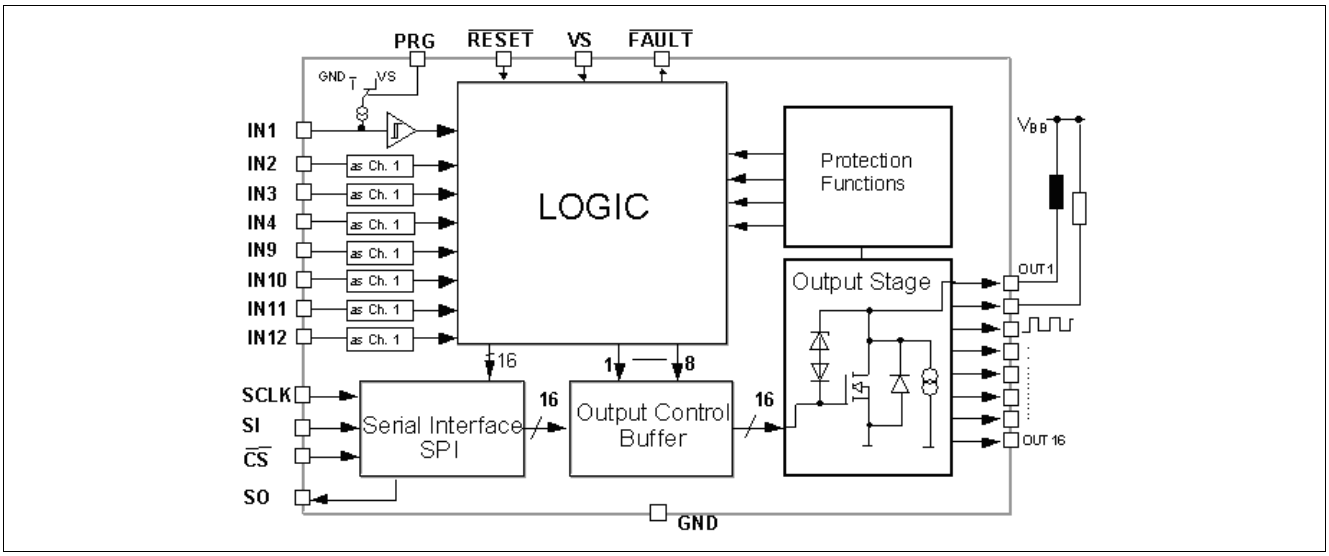


Figure 1 Application Block Diagram

2 Block Diagram

2.1 Detailed Block Diagram

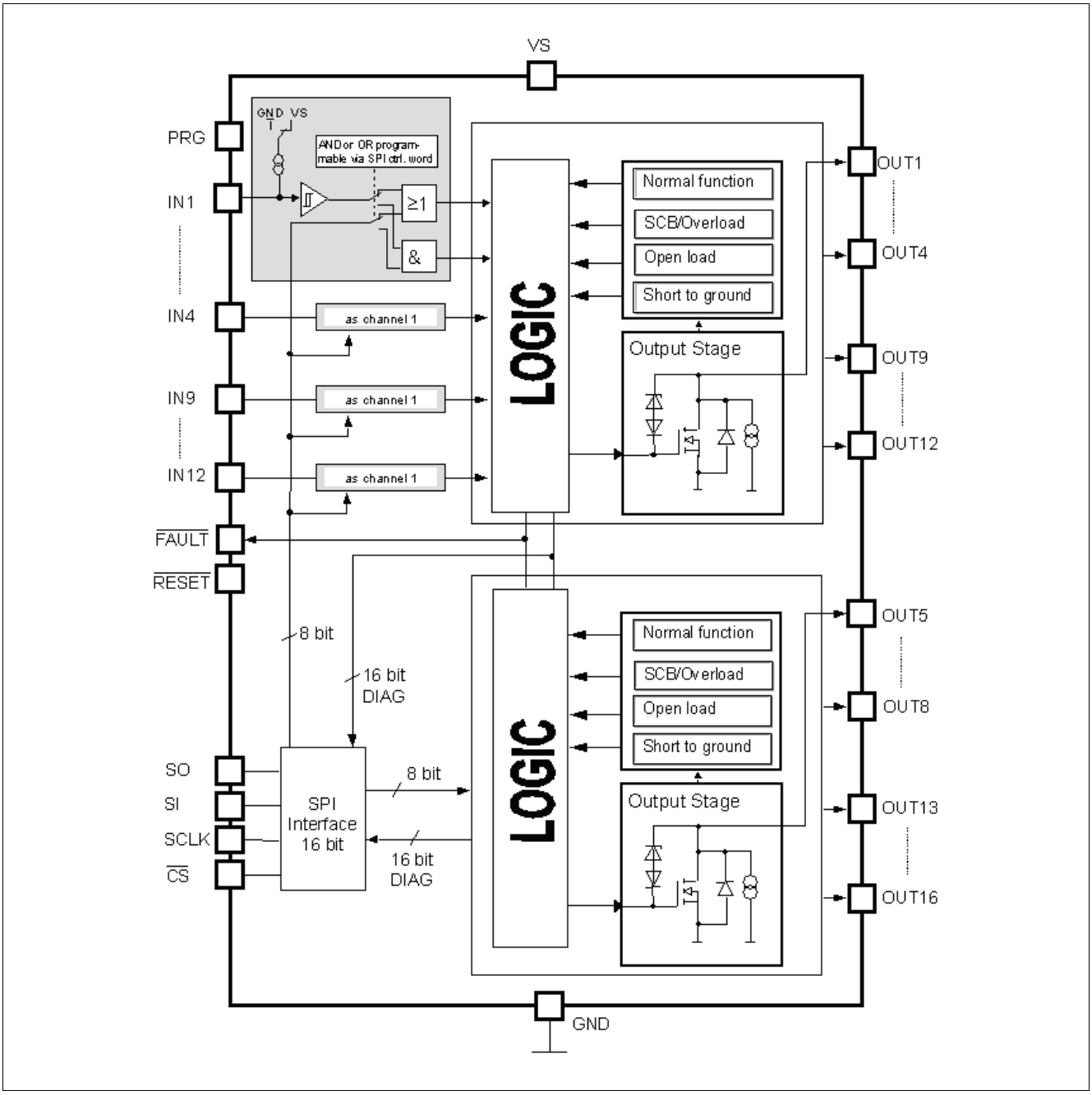


Figure 2 Detailed Block Diagram

2.2 Description of Block Diagram

All 16 channels can be controlled via the serial interface (SPI). In addition to the serial control it is possible to control channel 1 to 4 and 9 to 12 direct in parallel with a separate input pin. The parallel input signal is either OR - operated or AND - operated with the respective SPI data bit. This boolean operation can be programmed via SPI control byte (see **Chapter 5**). The SPI interface also performs a diagnostic information for each channel.

2.3 Terms

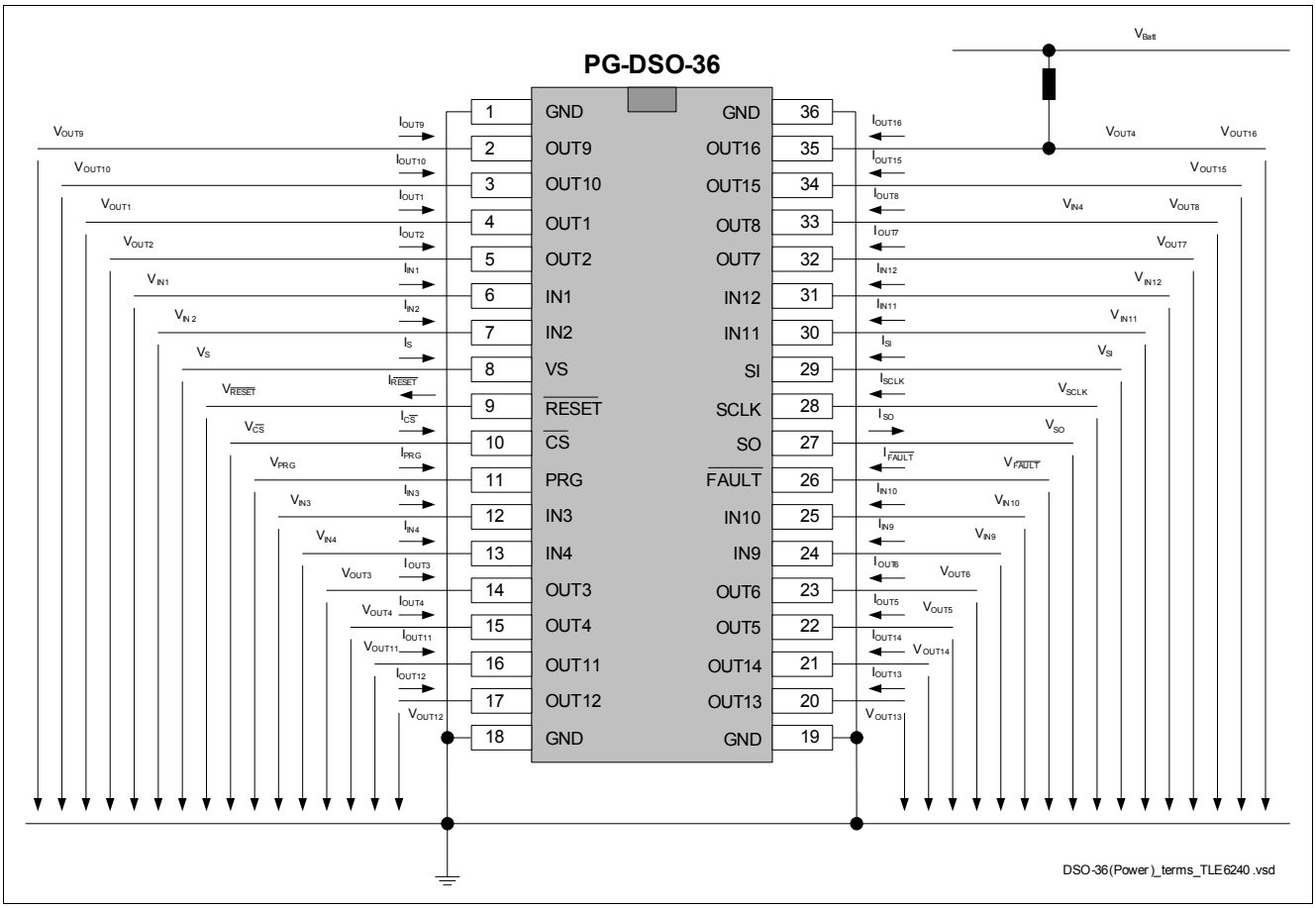


Figure 3 Terms for Voltages and Currents

3 Pin Configuration

3.1 Pin Assignment

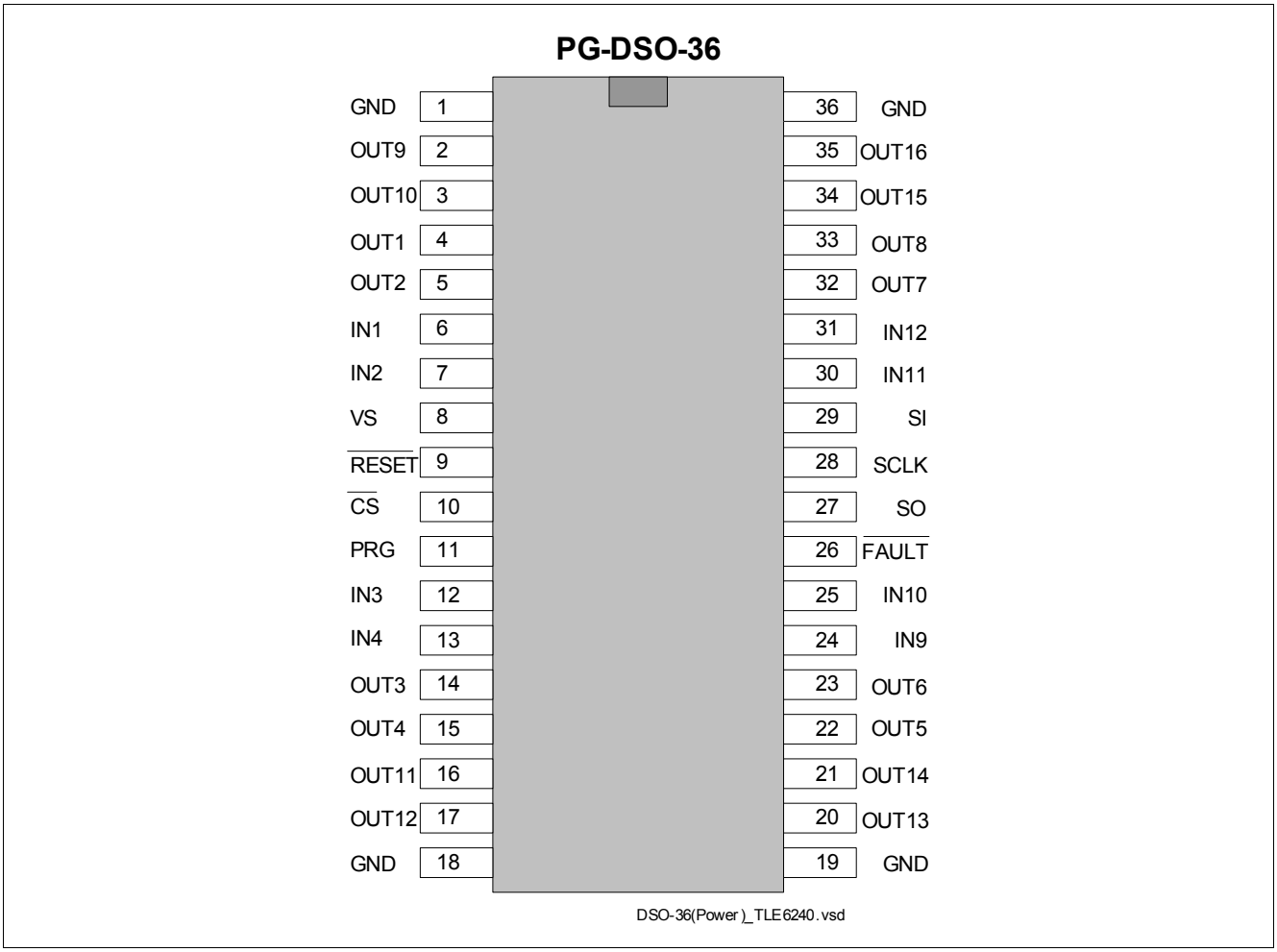


Figure 4 Pin Configuration (top view)

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground**
2	OUT9	**Power Output Channel 9**
3	OUT10	**Power Output Channel 10**
4	OUT1	**Power Output Channel 1**
5	OUT2	**Power Output Channel 2**
6	IN1	**Input Channel 1**
7	IN2	**Input Channel 2**
8	V_S	**Supply Voltage**
9	$\overline{\text{RESET}}$	**Reset**
10	$\overline{\text{CS}}$	**Chip Select**

Pin	Symbol	Function
11	PRG	**Program** (inputs high or low-active)
12	IN3	**Input Channel 3**
13	IN4	**Input Channel 4**
14	OUT3	**Power Output Channel 3**
15	OUT4	**Power Output Channel 4**
16	OUT11	**Power Output Channel 11**
17	OUT12	**Power Output Channel 12**
18	GND	**Ground**
19	GND	**Ground**
20	OUT13	**Power Output Channel 13**
21	OUT14	**Power Output Channel 14**
22	OUT5	**Power Output Channel 5**
23	OUT6	**Power Output Channel 6**
24	IN9	**Input Channel 9**
25	IN10	**Input Channel 10**
26	$\overline{\text{FAULT}}$	**General Fault Flag**
27	SO	**Serial Data Output**
28	SCLK	**Serial Clock**
29	SI	**Serial Data Input**
30	IN11	**Input Channel 11**
31	IN12	**Input Channel 12**
32	OUT7	**Power Output Channel 7**
33	OUT8	**Power Output Channel 8**
34	OUT15	**Power Output Channel 15**
35	OUT16	**Power Output Channel 16**
36	GND	**Ground**

Heat Slug internally connected to ground pins

4 Maximum Ratings and Operating Conditions

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-0.3	7	V	–
4.1.2	Continuous Drain Source Voltage (OUT1 to OUT16)	V_{DS}	–	45	V	–
4.1.3	Input Voltage, All Inputs and Data Lines	V_{IN}	-0.3	7	V	–
Currents						
4.1.4	Output current per Channel (see **Chapter 5**)	$I_{D(lim)}$	–	$I_{D(lim)\ min}$	A	–
4.1.5	Output current per Channel (All 16 Channels ON; Mounted on PCB)[2)]	$I_{D\ 1\text{-}8}$	–	0.3	A	T_A = 25 °C
		$I_{D\ 9\text{-}16}$	–	0.5	A	T_A = 25 °C
4.1.6	Output current (Max. total current of all channels on; Heat Sink required)	I_{Dmax}	–	14	A	–
ESD Susceptibility						
4.1.7	Electrostatic Discharge Voltage	V_{ESD}	–	2000	V	HBM[3)]

1) Not subject to production test, specified by design.

2) Output current rating so long as maximum junction temperature is not exceeded. At T_A = 125 °C the output current has to be calculated using R_{thJA} according mounting conditions.

3) Human Body Model according to EIA/JESD22-A114-E.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Temperature Range							
4.2.1	Operating Temperature Range	T_j	-40	–	150	°C	–
4.2.2	Storage Temperature Range	T_{stg}	-55	–	150	°C	–
Single Pulse Inductive Energy							
4.2.3	Single pulse inductive Energy (internal clamping)	E_{AS}	–	–	50	mJ	T_J = 25 °C; I_{D1-8} = 0.5 A; I_{D9-16} = 1 A
Power Dissipation							
4.2.4	Power Dissipation (mounted on PCB)	P_{tot}	–	3.3	–	W	T_A = 25 °C all Channel active

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case (die soldered on heat slug)[1)]	R_{thJSp}	–	0.5	1	K/W	Pv = 3W
4.3.2	Junction to ambient (see **Figure 5**[1)]); all channels active	R_{thjA}	–	12	–	K/W	Pv = 3W

1) Not subject to production test, specified by design.

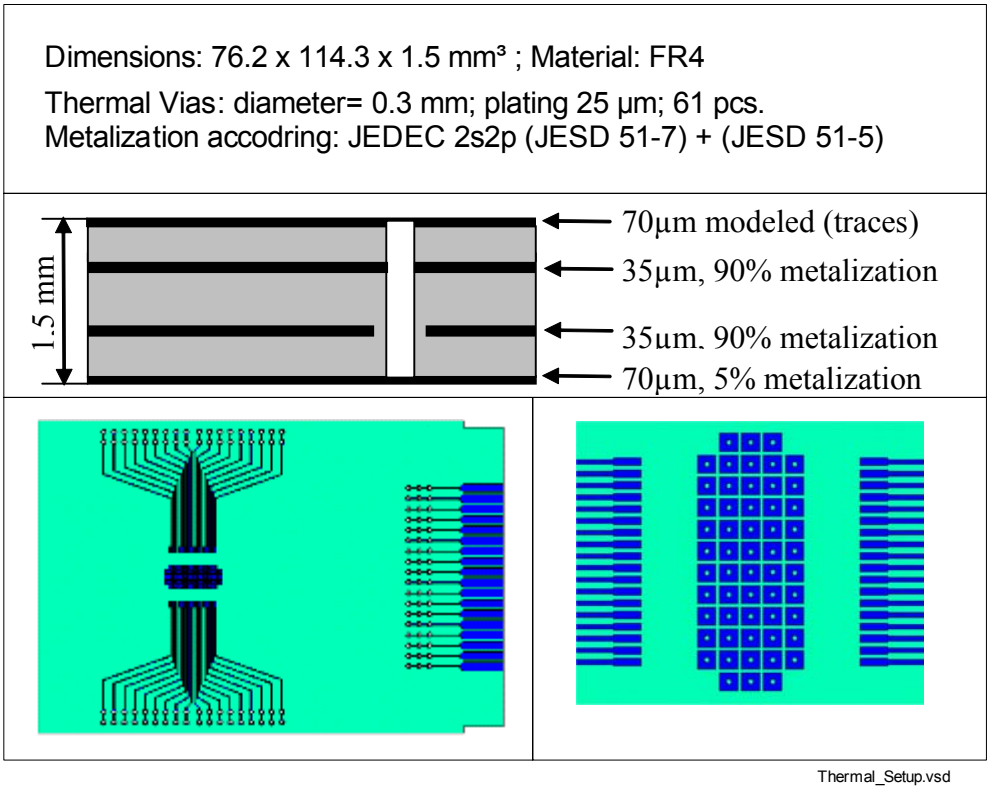


Figure 5 Thermal Simulation - PCB set-up

5 Electrical and Functional Description of Blocks

The TLE6240GP is an 16-fold low-side power switch which provides a serial peripheral interface (SPI) to control the 16 power DMOS switches, and diagnostic feedback. The power transistors are protected against short to V_{BB}, overload, overtemperature and against overvoltage by active zener clamp.

The diagnostic logic recognizes a fault condition which can be read out via the serial diagnostic output (SO).

5.1 Power Supply & Reset

RESET - Reset pin. If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip. In case the RESET Pin is pulled down statically, the device remains in Stand-by Mode

Electrical Characteristics: Power Supply

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, Reset = H (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Supply Voltage[1)]	V_S	4.5	–	5.5	V	–
5.1.2	Supply Current	I_S	–	5	10	mA	–
5.1.3	Supply Current in Standby Mode	$I_{S(stdy)}$	–	10	50	µA	(RESET = L)

1) For V_S < 4.5 V the power stages are switched according the input signals and data bits or are definitely switched off. This undervoltage reset gets active at V_S = 3 V (typ. value) and is specified by design and not subject to production test.

5.2 Digital Inputs

In this chapter is the electrical behavior of the following Digital Input Pins described:

- parallel Input Pin INx
- Reset Pin RESET
- Program Pin PRG

Electrical Characteristics: Digital Inputs

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, Reset = H (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Input Low Voltage	V_{INL}	-0.3	–	1.0	V	–
5.2.2	Input High Voltage	V_{INH}	2.0	–	–	V	–
5.2.3	Input Voltage Hysteresis	V_{INHys}	50	100	200	mV	–
5.2.4	Input Pull-down/up Current (IN1 to IN4, IN9 to IN12)	$I_{IN(1..4,9..12)}$	20	50	100	µA	V_{IN} = 5 V
5.2.5	PRG, Reset Pull-up Current	$I_{IN(PRG,Res)}$	20	50	100	µA	–
5.2.6	Minimum Reset Duration (After a reset all parallel inputs are ORed with the SPI data bits)	$t_{Reset,min}$	10	–	–	µs	–

5.3 Power Outputs

Power Transistor Protection Functions[1)]

Each of the 16 output stages has its own zener clamp, which causes a voltage limitation at the power transistor when solenoid loads are switched off. The outputs are provided with a current limitation set to a minimum of 1 A for channels 1 to 8 and 3 A for channels 9 to 16.

In the event of an overload or short to supply, the current is internally limited and the corresponding diagnosis bit combination is set. If this operation leads to an overtemperature condition, a second protection level will change the output into a low duty cycle PWM (selective thermal shut-down with restart) to prevent critical chip temperatures.

Electrical Characteristics: Power Outputs

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, Reset = H (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	ON Resistance V_S = 5 V; Channel 1-8	$R_{DS(ON)}$	–	1	–	Ω	T_J = 25 °C[1)]
			–	1.7	2.2	Ω	T_J = 150 °C
5.3.2	ON Resistance V_S = 5 V; Channel 10, 11, 14, 15	$R_{DS(ON)}$	–	0.35	–	Ω	T_J = 25 °C[1)]
			–	0.60	0.70	Ω	T_J = 150 °C
5.3.3	ON Resistance V_S = 5 V; Channel 9, 12, 13, 16	$R_{DS(ON)}$	–	0.30	–	Ω	T_J = 25 °C[1)]
			–	0.50	0.60	Ω	T_J = 150 °C
5.3.4	Output Clamping Voltage Channel 1-8	$V_{DS(AZ)}$	45	50	60	V	Output OFF
5.3.5	Output Clamping Voltage Channel 9-16	$V_{DS(AZ)}$	45	52.5	60	V	Output OFF
5.3.6	Current Limit Channel 1-8	$I_{D(lim)}$	1	1.5	2	A	–
5.3.7	Current Limit Channel 9-16	$I_{D(lim)}$	3	4.5	6	A	–
5.3.8	Output Leakage Current	$I_{D(lkg)}$	–	–	10	µA	V_{Reset} = L
5.3.9	Turn-On Time	t_{ON}	–	6	12	µs	I_D = 0.5 A, resistive load
5.3.10	Turn-Off Time	t_{OFF}	–	6	12	µs	

1) Specified by design and not subject to production test.

1) The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently.

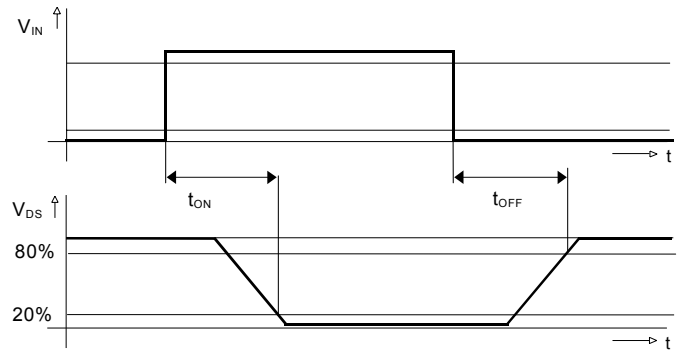


Figure 6 Timing

5.3.1 Typical Characteristics

Drain-Source On-Resistance

$R_{DS(ON)} = f(T_j)$; V_S = 5 V

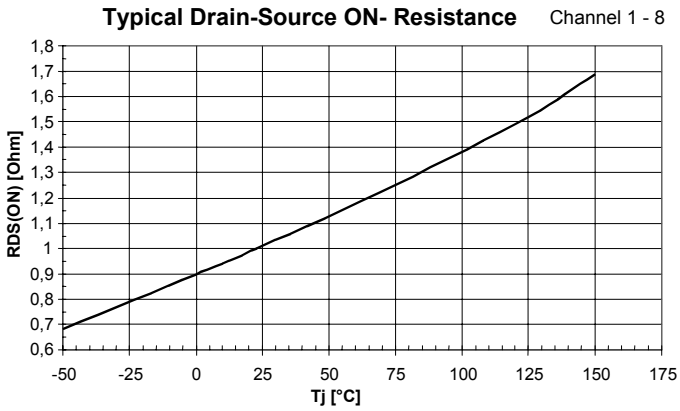


Figure 7 Typical ON Resistance versus Junction-Temperature (Channel 1-8)

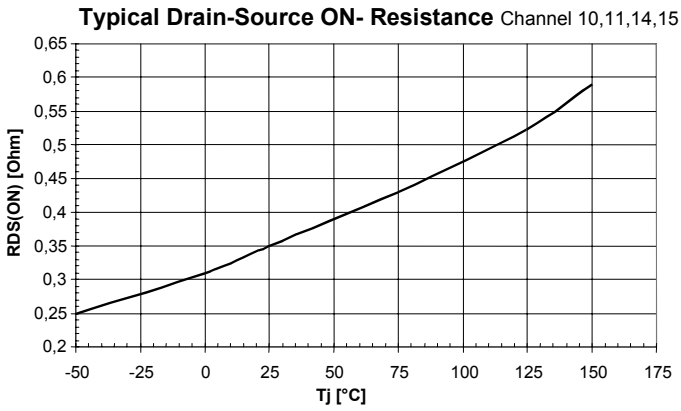


Figure 8 Typical ON Resistance versus Junction-Temperature (Channel 10, 11, 14, 15)

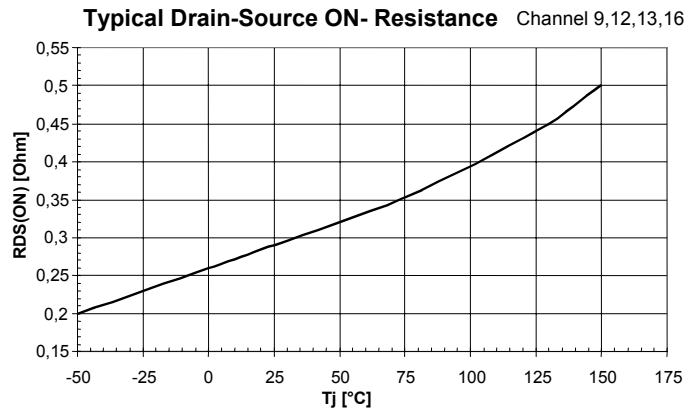


Figure 9 Typical ON Resistance versus Junction-Temperature (Channel 9, 12, 13, 16)

Output Clamping Voltage

$V_{DS(AZ)} = f(T_j)$; V_S = 5 V

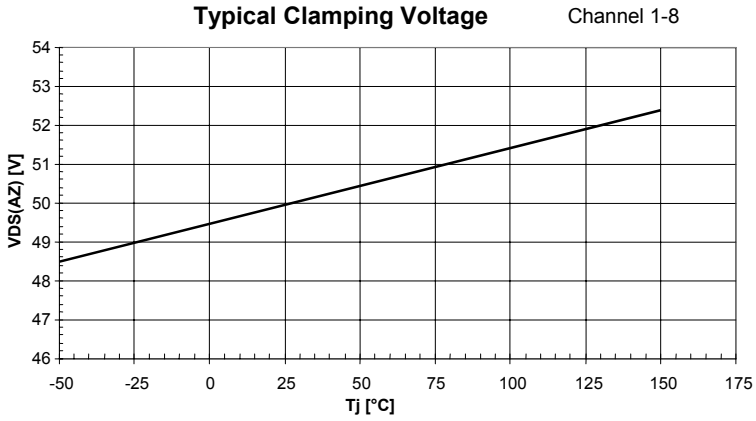


Figure 10 Typical Clamping Voltage versus Junction Temperature (Channel 1-8)

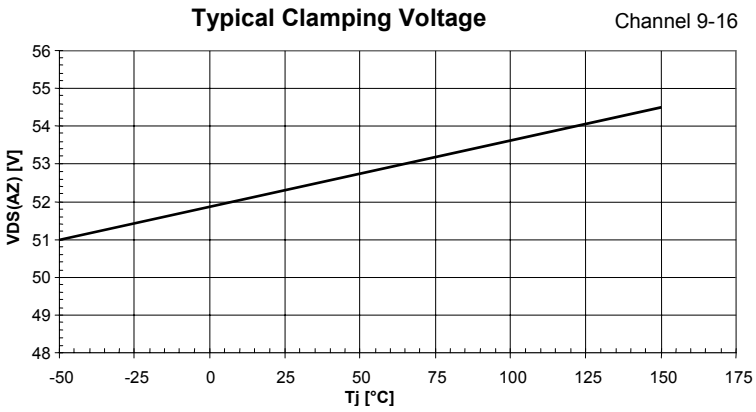


Figure 11 Typical Clamping Voltage versus Junction Temperature (Channel 9-16)

5.4 Diagnostic Functions and FAULT-Pin

The device provides diagnosis information about the device and about the load. There are following diagnosis flags implemented for each channel:

- The diagnosis information of the protective functions, such as “over current” and “over temperature”
- The open load diagnosis
- The short to ground information.

For further details, refer to the Chapter “Control of the device”

$\overline{\text{FAULT}}$ - Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error occurs for any one of the sixteen channels. This fault indication can be used to generate a µC interrupt. Therefore a ‘diagnosis’ interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.

As soon as a fault occurs, the fault information is latched into the diagnosis register. A new error will overwrite the old error report. Serial data out pin (SO) is in a high impedance state when $\overline{\text{CS}}$ is high. If $\overline{\text{CS}}$ receives a LOW signal, all diagnosis bits can be shifted out serially.

Electrical Characteristics: Diagnostic Functions

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, Reset = H (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Open Load Detection Voltage	$V_{DS(OL)}$	V_S - 2.5	V_S - 2	V_S - 1.3	V	–
5.4.2	Output Pull-down Current	$I_{PD(OL)}$	50	90	150	µA	V_{Reset} = H
5.4.3	Fault Delay Time	$t_{d(fault)}$	50	100	200	µs	–
5.4.4	Short to Ground Detection Voltage	$V_{DS(SHG)}$	V_S - 3.3	V_S - 2.9	V_S - 2.5	V	–
5.4.5	Short to Ground Detection Current	I_{SHG}	-50	-100	-150	µA	V_{Reset} = H
5.4.6	Overload Detection Threshold	$I_{D(lim)\ 1\text{-}8}$	1	1.3	2	A	–
		$I_{D(lim)\ 9\text{-}16}$	3	4	6	A	–
5.4.7	Overtemperature Shutdown Threshold[1)]	$T_{th(sd)}$	170	–	200	°C	–
5.4.8	Overtemperature Hysteresis[1)]	T_{hys}	–	10	–	K	–
5.4.9	FAULT Output Low Voltage	V_{faultL}	–	–	0.4	V	I_{faultL} = 1.6 mA

1) Specified by design and not subject to production test.

5.5 SPI Interface

Electrical Characteristics: SPI Interface

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, Reset = H (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.1	Input Pull-down Current (SI, SCLK)	$I_{IN(SI,SCLK)}$	10	20	50	µA	–
5.5.2	Input Pull-up Current ($\overline{CS}$)	$I_{IN(CS)}$	10	20	50	µA	–
5.5.3	SO High State Output Voltage	V_{SOH}	V_S - 0.4	–	–	V	I_{SOH} = 2 mA
5.5.4	SO Low State Output Voltage	V_{SOL}	–	–	0.4	V	I_{SOL} = 2.5 mA
5.5.5	Output Tri-state Leakage Current	I_{SOlkg}	-10	0	10	µA	$\overline{CS}$ = H; $0 \le V_{SO} \le V_S$
5.5.6	Serial Clock Frequency (depending on SO load)	f_{SCK}	DC	–	5	MHz	–
5.5.7	Serial Clock Period ($1/f_{clk}$)	$t_{p(SCK)}$	200	–	–	ns	–
5.5.8	Serial Clock High Time	t_{SCKH}	50	–	–	ns	–
5.5.9	Serial Clock Low Time	t_{SCKL}	50	–	–	ns	–
5.5.10	Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of CLK)	t_{lead}	200	–	–	ns	–
5.5.11	Enable Lag Time (falling edge of CLK to rising edge of $\overline{CS}$)	t_{lag}	200	–	–	ns	–
5.5.12	Data Setup Time (required time SI to falling of CLK)	t_{SU}	20	–	–	ns	–
5.5.13	Data Hold Time (falling edge of CLK to SI)	t_H	20	–	–	ns	–
5.5.14	Disable Time (@ C_L = 50 pF)[1]	t_{DIS}	–	–	150	ns	–
5.5.15	Transfer Delay Time[2] ($\overline{CS}$ high time between two accesses)	t_{dt}	200	–	–	ns	–
5.5.16	Data Valid Time	t_{valid}	–	–	100	ns	C_L = 50 pF[1]
			–	–	120	ns	C_L = 100 pF[1]
			–	–	150	ns	C_L = 220 pF[1]

1) This parameter will not be tested but specified by design

2) This time is necessary between two write accesses to control e.g. channel 1 to 8 during the first access and channel 9 to 16 during the second access. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200 µs.

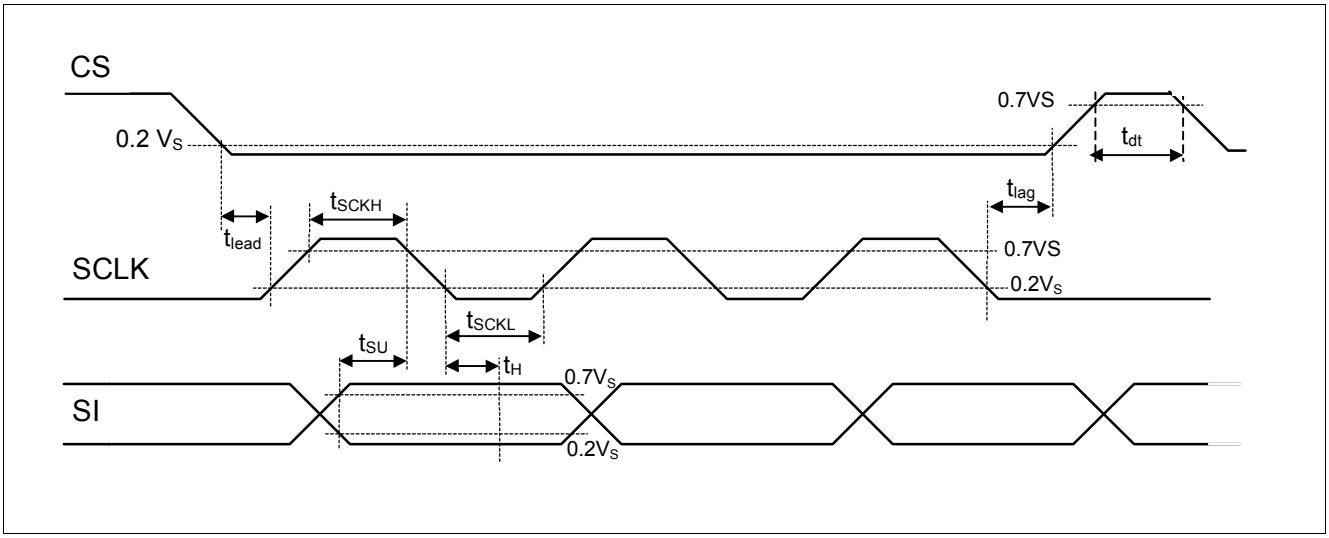


Figure 12 Input Timing Diagram

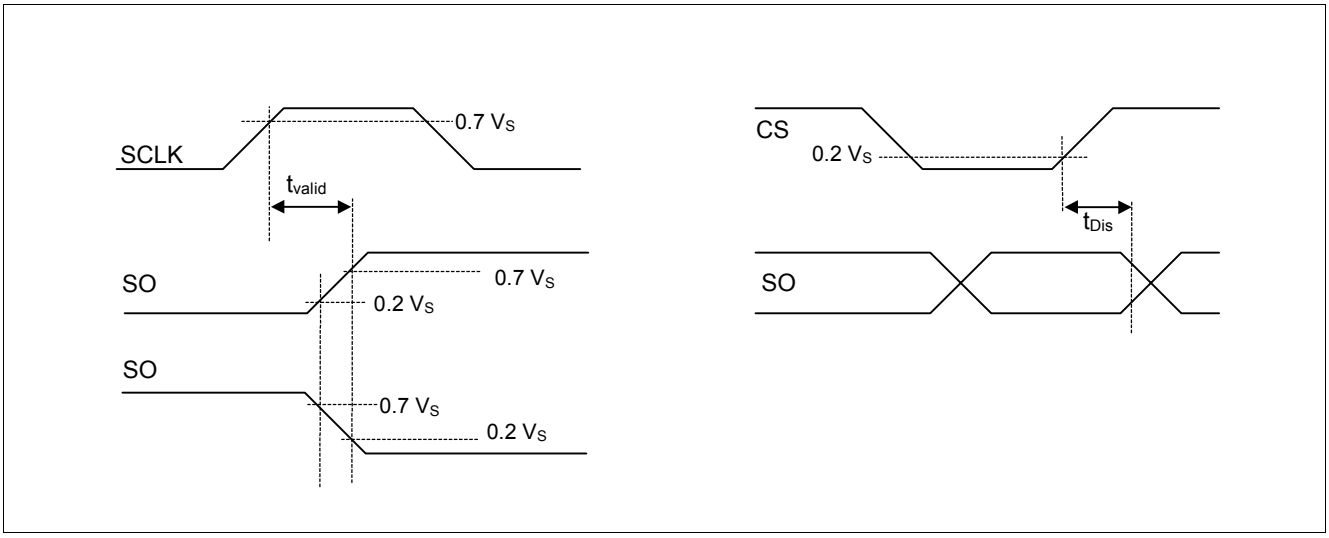


Figure 13 SO Valid Time Waveforms and Enable and Disable Time Waveforms

SPI Signal Description

$\overline{\text{CS}}$ - Chip Select. The system microcontroller selects the TLE6240GP by means of the $\overline{\text{CS}}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.

- **$\overline{\text{CS}}$ High to Low Transition:**
  - diagnostic status information is transferred from the power outputs into the shift register
  - serial input data can be clocked in from then on
  - SO changes from high impedance state to logic high or low state corresponding to the SO bits
- **$\overline{\text{CS}}$ Low to High Transition:**
  - transfer of SI bits from shift register into output buffers

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

SCLK - Serial Clock. The system clock pin clocks the internal shift register of the TLE6240GP. The serial input (SI) accepts data into the input shift register on the falling edge of SCLK while the serial output (SO) shifts

diagnostic information out of the shift register on the rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the falling edge of SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.

The input data consist of 16 bit, made up of one control byte and one data byte. The control byte is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see **Chapter 6.2**). The eight data bits contain the input information for the eight channels, and are high active.

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge of SCLK.

6 Control of the Device

6.1 Output Stage Control

The 16 outputs of the TLE6240GP can be controlled via serial interface. Additionally eight of these 16 channels can alternatively be controlled in parallel (Channel 1 to 4 and 9 to 12) for PWM applications.

6.1.1 Parallel Control and PRG - Pin

A Boolean operation (either AND or OR) is performed on each of the parallel inputs and respective SPI data bits, in order to determine the states of the respective outputs. The type of Boolean operation performed is programmed via the serial interface.

The parallel inputs are high or low active depending on the PRG pin. If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the outputs 1 to 4 and 9 to 12 are switched off. The PRG pin itself is internally pulled up when it is not connected.

PRG - Program pin.

- PRG = High (V_S): Parallel inputs Channel 1 to 4 and 9 to 12 are high active
- PRG = Low (GND): Parallel inputs Channel 1 to 4 and 9 to 12 are low active

6.1.2 Serial Control of the Outputs: SPI Protocol

6.1.3 Overview

Each output is independently controlled by an output latch and a common reset line, which disables all outputs. The Serial Input (SI) is read on the falling edge of the serial clock. A logic high input ‘data bit’ turns the respective output channel ON, a logic low ‘data bit’ turns it OFF.

$\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output control buffer.

The 16 channels of the TLE6240GP are divided up into two parts for the control of the outputs (ON, OFF) and the diagnosis information.

Serial Input (SI) information consists of 16 bit. 8 bit contain the input driver information for channel 1 to 8 or for channel 9 to 16. The remaining 8 bits are used to program a certain operation mode.

Serial Output (SO) data consists of 16 bit containing the diagnosis information for channels 1 to 8 or channels 9 to 16 with two bits per channel.

Channel 1 to 8:

- **Control Byte 1:** Operation mode and diagnosis select for channels 1 to 8
- **Data Byte1:** ON/OFF information for channel 1 to 8
- **DIAG_1:** Diagnosis data for channels 1 to 8

Channel 9 to 16:

- **Control Byte 2:** Operation mode and diagnosis select for channels 9 to 16
- **Data Byte2:** ON/OFF information for channel 9 to 16
- **DIAG_2:** Diagnosis data for channels 9 to 16

To drive all 16 channels and to get the complete diagnosis data of the TLE6240GP a two step access has to be performed as follows:

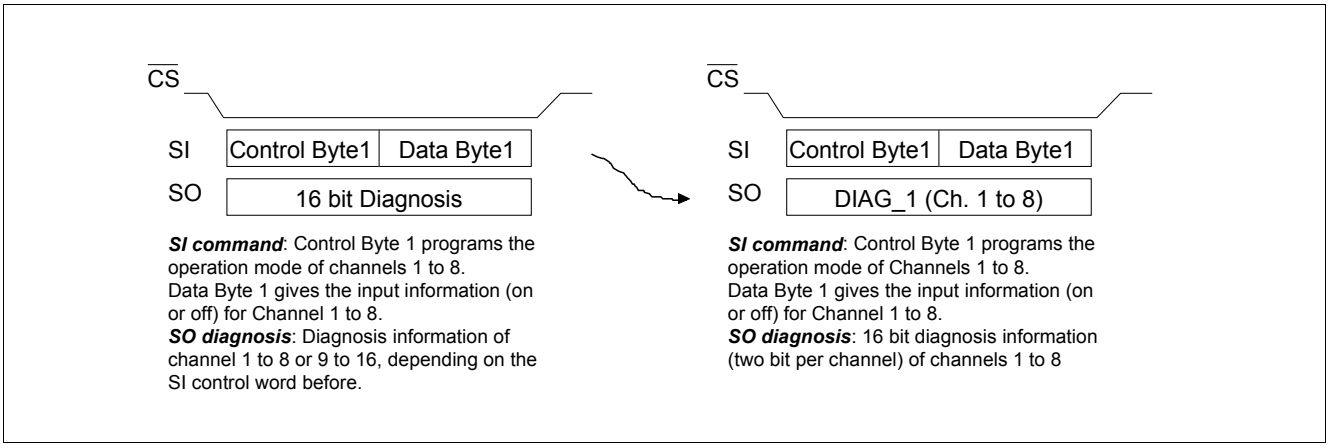


Figure 14 First Access

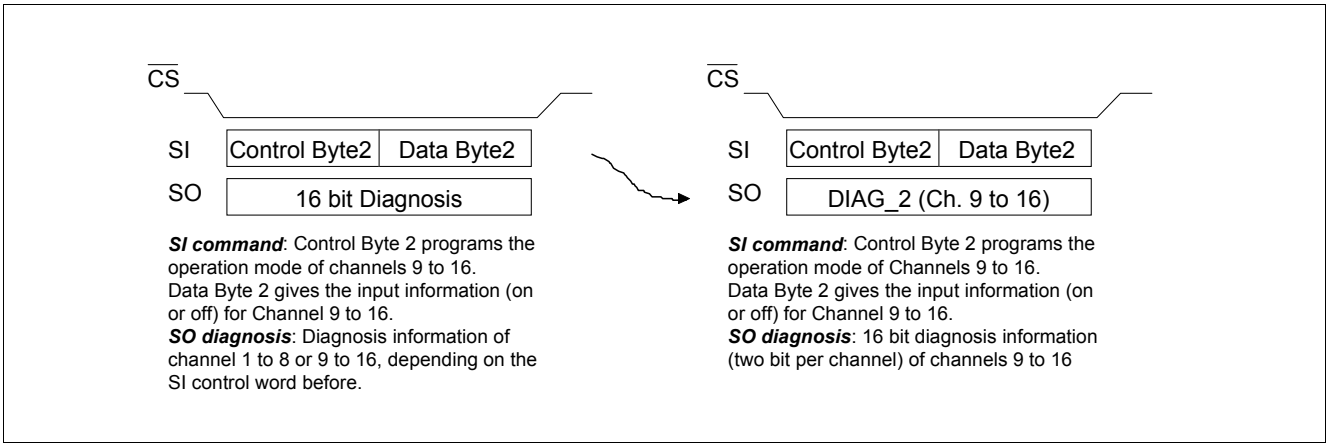


Figure 15 Second Access

6.1.4 Control- and Data Byte

As mentioned above, the serial input information consist of a control byte and a data byte. Via the control byte, the specific mode of the device is programmable.

Table 1 Control and Data Byte

MSB															LSB
C	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D
Control Byte								Data Byte							

Ten specific control words are recognized, having the following functions:

Table 2 Commands

No.	Control Byte	Data Byte	Function
Channel 1 to 8			
1	LLLL LLLL[1)]	XXXX XXXX[2)]	'Full Diagnosis' (two bits per channel) performed for channels 1 to 8. No change to output states.
2	HHLL LLLL	XXXX XXXX	State of the eight parallel inputs and '1-bit Diagnosis' for channel 1 to 8 is provided.
3	HLHL LLLL	XXXX XXXX	Echo-function of SPI; SI direct connected to SO.
4	LLHH LLLL	DDDDDDDD[2)]	IN1 … 4 and serial data bits 'OR'ed. 'Full Diagnosis' performed for channels 1 to 8.
5	HHHH LLLL	DDDDDDDD	IN1 … 4 and serial data bits 'AND'ed. 'Full Diagnosis' performed for channels 1 to 8.
Channel 9 to 16			
6	LLLL HHHH[1)]	XXXX XXXX	'Full Diagnosis' (two bits per channel) performed for channels 9 to 16. No change to output states.
7	HHLL HHHH	XXXX XXXX	State of the eight parallel inputs and '1-bit Diagnosis' for channel 9 to 16 is provided.
8	HLHL HHHH	XXXX XXXX	Echo-function of SPI; SI direct connected to SO.
9	LLHH HHHH	DDDDDDDD	IN9 … 12 and serial data bits 'OR'ed. 'Full Diagnosis' performed for channels 9 to 16.
10	HHHH HHHH	DDDDDDDD	IN9 … 12 and serial data bits 'AND'ed. 'Full Diagnosis' performed for channels 9 to 16.

1) Control Byte: Channel Selection via Bit 0 to 3
Bits 0 to 3 = L, Channels 1 to 8 selected
Bits 0 to 3 = H, Channels 9 to 16 selected

2) Data Byte: 'X' means 'don't care', because this data bits will be ignored.
'D' represents the data bits, either being H (= ON) or L (= OFF).

Control words beside No. 1- 10

Not specified Control words are not executed (cause no function) and the shift register (SO Data) is reset after the $\overline{CS}$ signal (all '0').

6.1.5 Control Byte - Detailed description

In the following section the different control bytes will be described. X used within the control byte means:

Table 3 Control Byte - Channel Group selection

MSB								Comment
X	**X**	**X**	**X**	**L**	**L**	**L**	**L**	**Command is valid for Channels 1 to 8**
X	**X**	**X**	**X**	**H**	**H**	**H**	**H**	**Command is valid for Channels 9 to 16**
				Control Byte				

The following Control Byte descriptions are referring to the Overview **Table 2**.

6.1.5.1 Control Byte No.1 and 6

Table 4 Control Byte No. 1 to 6

MSB								Comment
L	**L**	**L**	**L**	**X**	**X**	**X**	**X**	**Diagnosis only**
				Control Byte				

By clocking in this control byte, it is possible to get pure diagnostic information (two bits per channel) in accordance with **Figure 21**. The data bits are ignored, so that the state of the outputs are not influenced. This command is only active once unless the next control command is again “Diagnosis only”. Diagnostic information can be read out at any time with no change of the switching conditions.

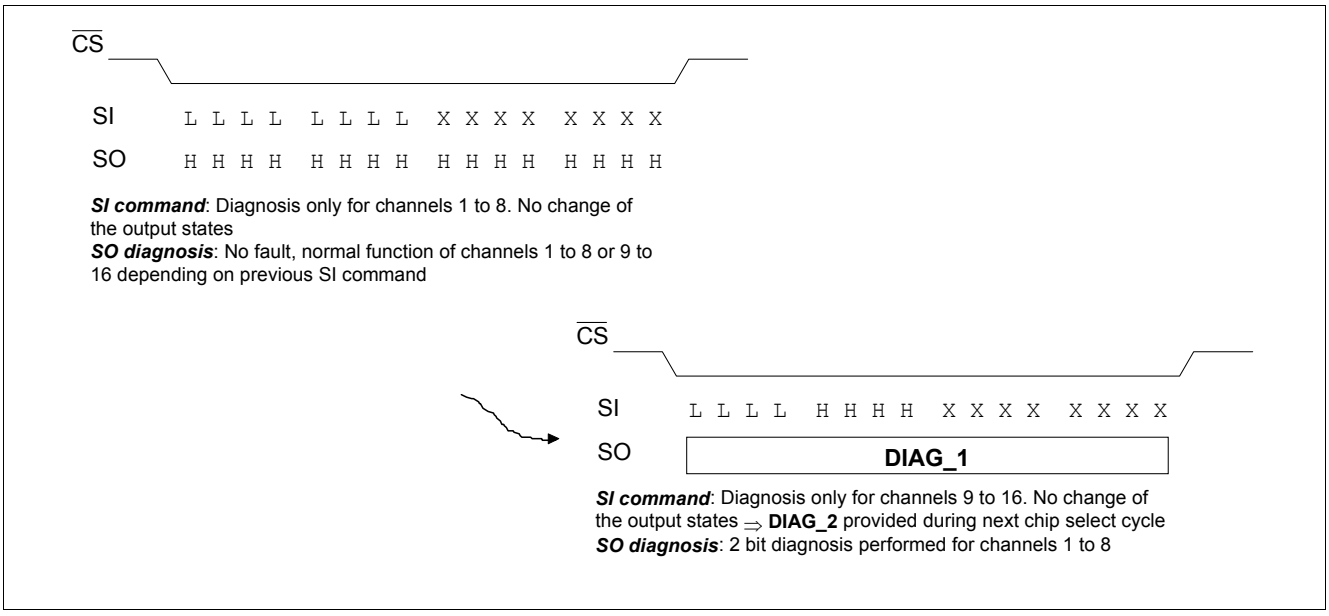


Figure 16 Example for two Consecutive Chip Select Cycles

6.1.5.2 Control Byte No. 2 and 7

Table 5 Control Byte No. 2 and 7

MSB								Comment
H	**H**	**L**	**L**	**X**	**X**	**X**	**X**	**Reading back of the eight inputs and '1-bit Diagnosis' provided**
Control Byte								

If the TLE6240GP is used as bare die in a hybrid application, it is necessary to know if proper connections exist between the µC-port and parallel inputs. By entering 'HHLL' as the control word, the first eight bits of the SO give the state of the parallel inputs, depending on the µC signals. By comparing the IN-bits with the corresponding µC-port signal, the necessary connection between the µC and the TLE6240GP can be verified - i.e. 'read back of the inputs'.

The second 8-bits fed out at the serial output contains '1-bit' fault information of the outputs (H = no fault, L = fault). In the expression given below for the output byte, 'FX' is the fault bit for channel X.

Table 6 Serial Output

MSB															LSB
IN12	**IN11**	**IN10**	**IN9**	**IN4**	**IN3**	**IN2**	**IN1**	**FX**	**FX**	**FX**	**FX**	**FX**	**FX**	**FX**	**FX**
Parallel Input Signals								Fault Bits Channel 1 to 8 or 9 to 16							

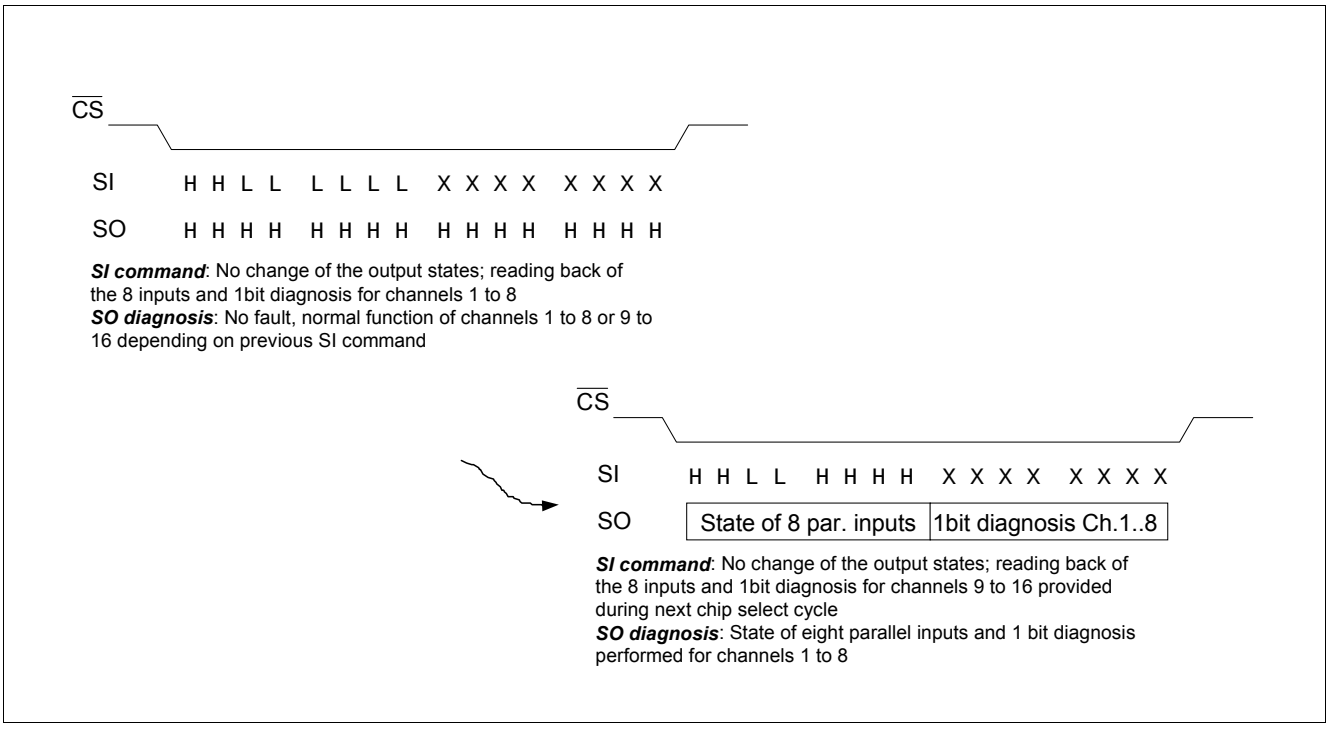


Figure 17 Example for two Consecutive Chip Select Cycles

6.1.5.3 Control Byte No. 3 and 8

Table 7 Control Byte No. 3 and 8

MSB								Comment
H	**L**	**H**	**L**	**X**	**X**	**X**	**X**	**Echo-function of SPI**
Control Byte								

To check the proper function of the serial interface the TLE6240GP provides a “SPI Echo Function”. By entering HLHL as control word, SI and SO are connected during the next $\overline{CS}$ period. By comparing the bits clocked in with the serial output bits, the proper function of the SPI interface can be verified. This internal loop is **only closed once** (for one $\overline{CS}$ period). The “Echo Function” does not cause any internal processing of data and after the next $\overline{CS}$ signal the SO data is ‘0’ (all registers reset).

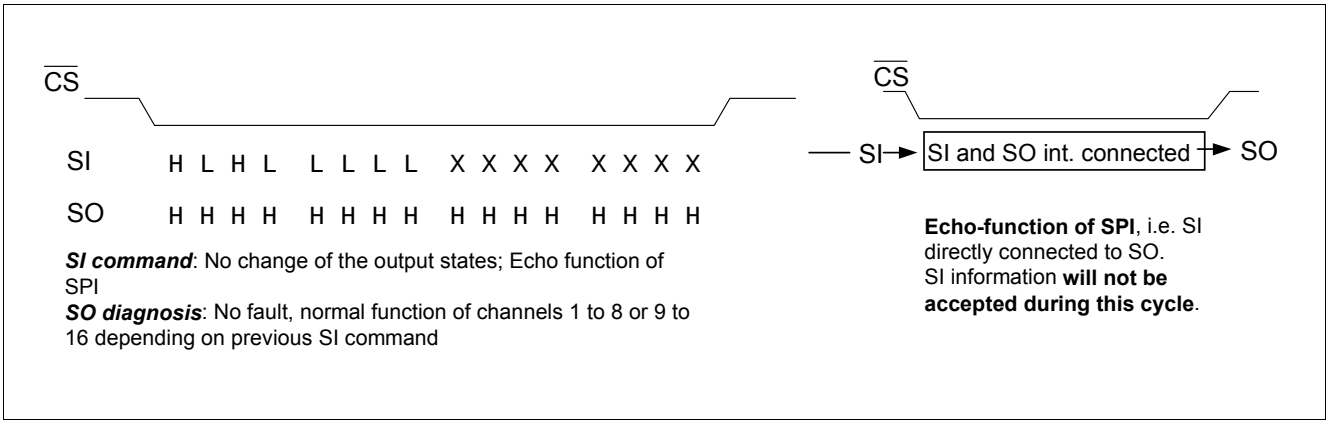


Figure 18 Echo-function of SPI

6.1.5.4 Control Byte No. 4 and 9

Table 8 Control Byte No. 4 and 9

MSB								Comment
L	**L**	**H**	**H**	**X**	**X**	**X**	**X**	**OR operation, and ‘full diagnosis’**
Control Byte								

With LLHH LLLL as the control word, each of the input signals IN1 to IN4 are ‘OR’ed with the corresponding SI data bits.

With LLHH HHHH as the control word, each of the input signals IN9 to IN12 are ‘OR’ed with the corresponding SI data bits.

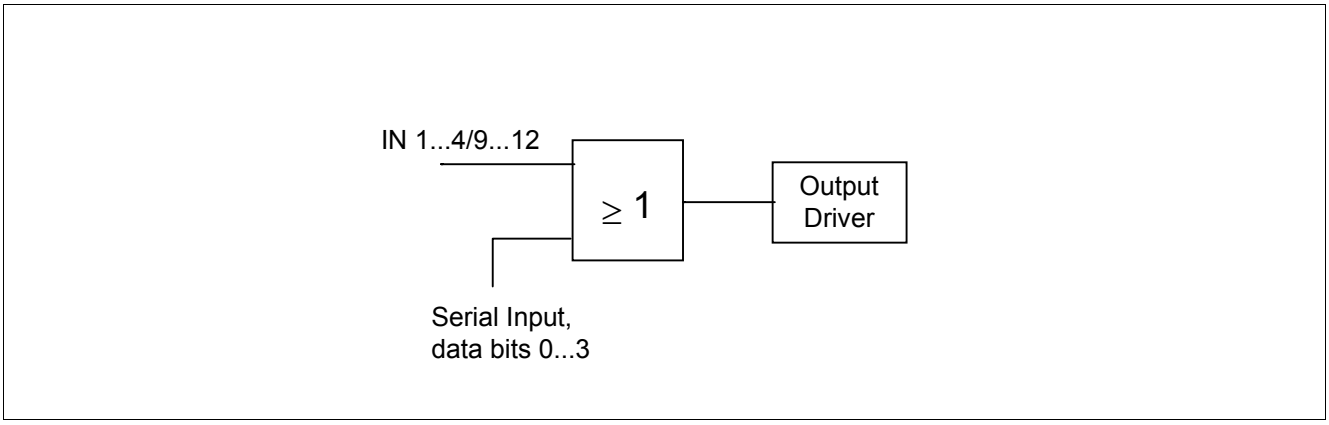


Figure 19 OR Operation between IN and Serial Input

This OR operation enables the serial interface to switch the channel ON, even though the corresponding parallel input might be in the off state.

SPI Priority for ON-State

Also parallel control of the outputs is possible without an SPI input.

The OR-function is the default Boolean operation if the device restarts after a Reset, or when the supply voltage is switched on for the first time.

If the OR operation is programmed it is latched until it is overwritten by the AND operation.

6.1.5.5 Control Byte No. 5 and 10

Table 9 Control Byte No. 5 and 10

MSB								Comment
H	**H**	**H**	**H**	**X**	**X**	**X**	**X**	**AND operation, and 'full diagnosis'**
Control Byte								

With HHHH LLLL as the control word, each of the input signals IN1 to IN4 are 'AND'ed with the corresponding SI data bits.

With HHHH HHHH as the control word, each of the input signals IN9 to IN12 are 'AND'ed with the corresponding SI data bits.

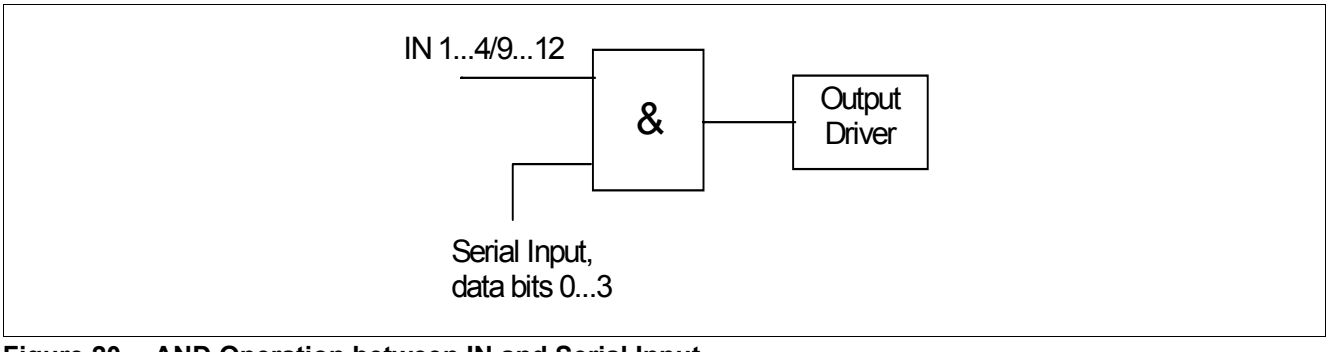


Figure 20 AND Operation between IN and Serial Input

The AND operation implies that the output can be switched off by the SPI data bit input, even if the corresponding parallel input is in the ON state.

SPI Priority for OFF-State

This also implies that the serial input data bit can only switch the output channel ON if the corresponding parallel input is in the ON state.

If the AND operation is programmed it is latched until it is overwritten by the OR operation.

6.1.5.6 Example for an access to channel 1 to 8

LLHH LLLL HLLH LLLH: OR operation between parallel inputs and data bits, i.e channel 1, 5 and 8 will be switched on.

The next command is now: LHHH LLLL HHHH LLLL

LHHH LLLL as command word has no special meaning and will not be accepted. The output states will not be changed and the shift register will be reset (at the next $\overline{CS}$ SO Data all ‘0’).

6.2 Diagnostics

For full diagnosis there are two diagnostic bits per channel configured as shown in **Figure 21**.

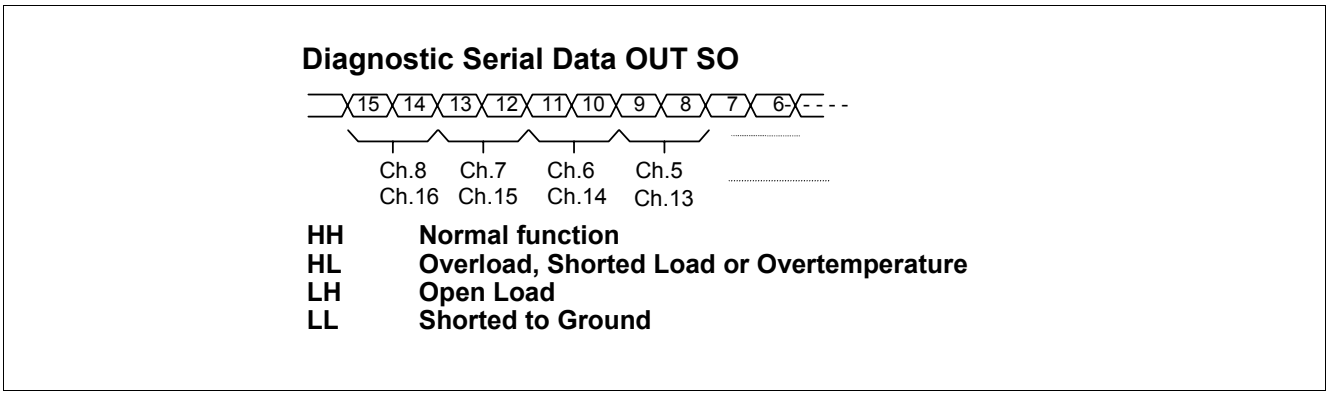


Figure 21 Two Bits per Channel Diagnostic Feedback

- **Normal function:** The bit combination **HH** indicates that there is no fault condition, i.e. normal function.
- **Overload, Short Circuit to Battery (SCB) or Overtemperature: HL** is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition.
- **Open load:** An open load condition is detected when the drain voltage decreases below 3 V (typ.). **LH** bit combination is set.
- **Short Circuit to GND:** If a drain to ground short circuit exists and the drain to ground current exceeds 100 µA, short to ground is detected and the **LL** bit combination is set.

A definite distinction between open load and short to ground is specified by design.

The standard way of obtaining diagnostic information is as follows:

Clock in serial information into SI pin and wait approximately 150 µs to allow the outputs to settle. Clock in the identical serial information once again - during this process the data coming out at SO contains the bit combinations representing the diagnosis conditions as described in **Figure 21**.

Reset of the Diagnosis Register

The diagnosis register is reset after reading the diagnosis data (after the falling $\overline{CS}$ edge). This is done for channels 1-8 and channels 9-16 separately depending on the previous command.

6.2.1 Diagnosis Read-out options

By means of the control byte it is possible either to:

1. control the outputs according to the data byte, as well as being able to read the diagnostic information (two bits per channel)
2. or purely get diagnostic information without changing the state of the outputs
3. or read back the parallel inputs plus a simple diagnosis (one bit per channel)
4. or SPI “Echo Function” as a diagnosis of proper SPI function.

Diagnosis Read-Out Option 1): Serial Control of Outputs

Table 10 OR-operation valid for channels 1 to 8

MSB															LSB
L	**L**	**H**	**H**	**L**	**L**	**L**	**L**	**L**	**H**	**L**	**H**	**H**	**L**	**L**	**L**
			Control Byte								Data Byte				

SI information: OR-operation valid for channels 1 to 8
SO: 16 bit diagnosis for channels 1 to 8 performed during next chip select cycle

Table 11 OR-operation valid for channels 9 to 16

MSB															LSB
L	**L**	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**L**	**H**	**L**	**H**	**L**	**L**	**L**
			Control Byte								Data Byte				

SI information: OR-operation valid for channels 9 to 16
SO: 16 bit diagnosis for channels 9 to 16 performed during next chip select cycle

Table 12 AND-operation valid for channels 1 to 8

MSB															LSB
H	**H**	**H**	**H**	**L**	**L**	**L**	**L**	**L**	**H**	**L**	**H**	**H**	**L**	**L**	**L**
			Control Byte								Data Byte				

SI information: AND-operation valid for channels 1 to 8
SO: 16 bit diagnosis for channels 1 to 8 performed during next chip select cycle

Table 13 AND-operation valid channels 9 to 16

MSB															LSB
H	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**L**	**H**	**L**	**H**	**H**	**L**	**L**	**L**
			Control Byte								Data Byte				

SI information: AND-operation valid for channels 9 to 16
SO: 16 bit diagnosis for channels 9 to 16 performed during next chip select cycle

Diagnosis Read-Out Option 2): Diagnosis only

Table 14 diagnosis - No change of output states

MSB															LSB
L	L	L	L	L	L	L	L	X	X	X	X	X	X	X	X
Control Byte								Data Byte							

SI information: Full diagnosis for channels 1 to 8. No change of output states
SO: 16 bit diagnosis for channels 1 to 8 performed during next chip select cycle

Table 15 diagnosis - No change of output states

MSB															LSB
L	L	L	L	H	H	H	H	X	X	X	X	X	X	X	X
Control Byte								Data Byte							

SI information: Full diagnosis for channels 9 to 16. No change of output states
SO: 16 bit diagnosis for channels 9 to 16 performed during next chip select cycle

Diagnosis Read-Out Option 3): Read back of parallel inputs plus simple diagnosis

Table 16 No change of output states - read

MSB															LSB
H	H	L	L	L	L	L	L	X	X	X	X	X	X	X	X
Control Byte								Data Byte							

SI information: No change of the output states. Read back of parallel inputs and 1 bit diagnosis for channels 1 to 8
SO: State of eight inputs plus 1 bit diagnosis for channel 1 to 8 during next chip select cycle

Table 17 No change of output states - read

MSB															LSB
H	H	L	L	H	H	H	H	X	X	X	X	X	X	X	X
Control Byte								Data Byte							

SI information: No change of the output states. Read back of parallel inputs and 1 bit diagnosis for channels 9 to 16
SO: State of eight inputs plus 1 bit diagnosis for channel 9 to 16 during next chip select cycle

Diagnosis Read-Out Option 4): SPI Echo function

Table 18 No change of output states - Echo

MSB															LSB
H	L	H	L	L	L	L	L	X	X	X	X	X	X	X	X
Control Byte								Data Byte							

SI information: Echo function of SPI interface. No change of the output states
SO: During next chip select cycle the SI bits clocked in appear directly at SO because of an internal connection for this cycle

Table 19 No change of output states - Echo

MSB															LSB
H	**L**	**H**	**L**	**H**	**H**	**H**	**H**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
			Control Byte								Data Byte				

SI information: Echo function of SPI interface. No change of the output states
SO: During next chip select cycle the SI bits clocked in appear directly at SO because of an internal connection for this cycle

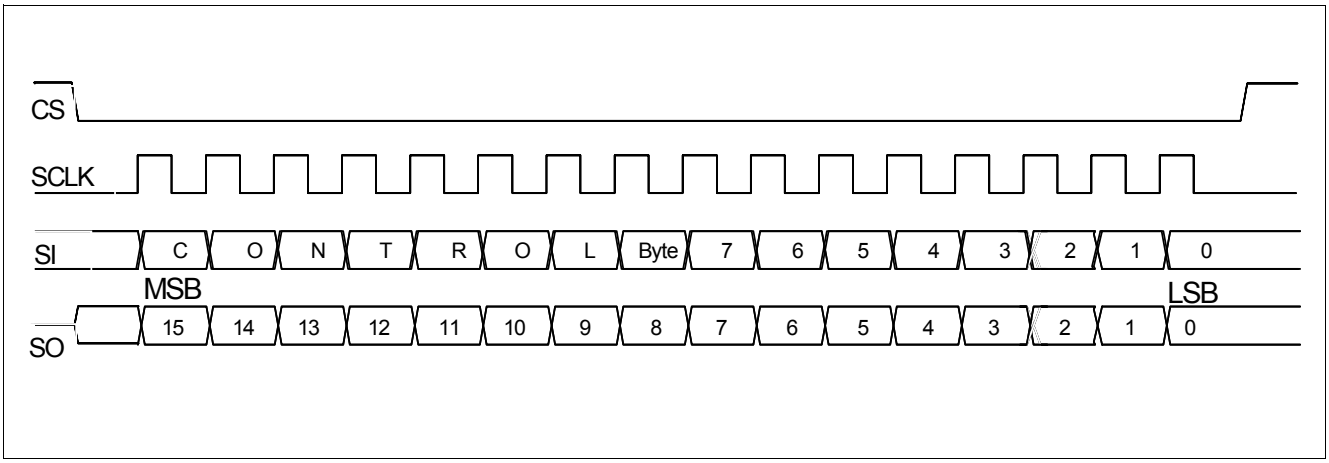


Figure 22 Serial Interface

7 Application Hints

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

7.1 Application Circuits

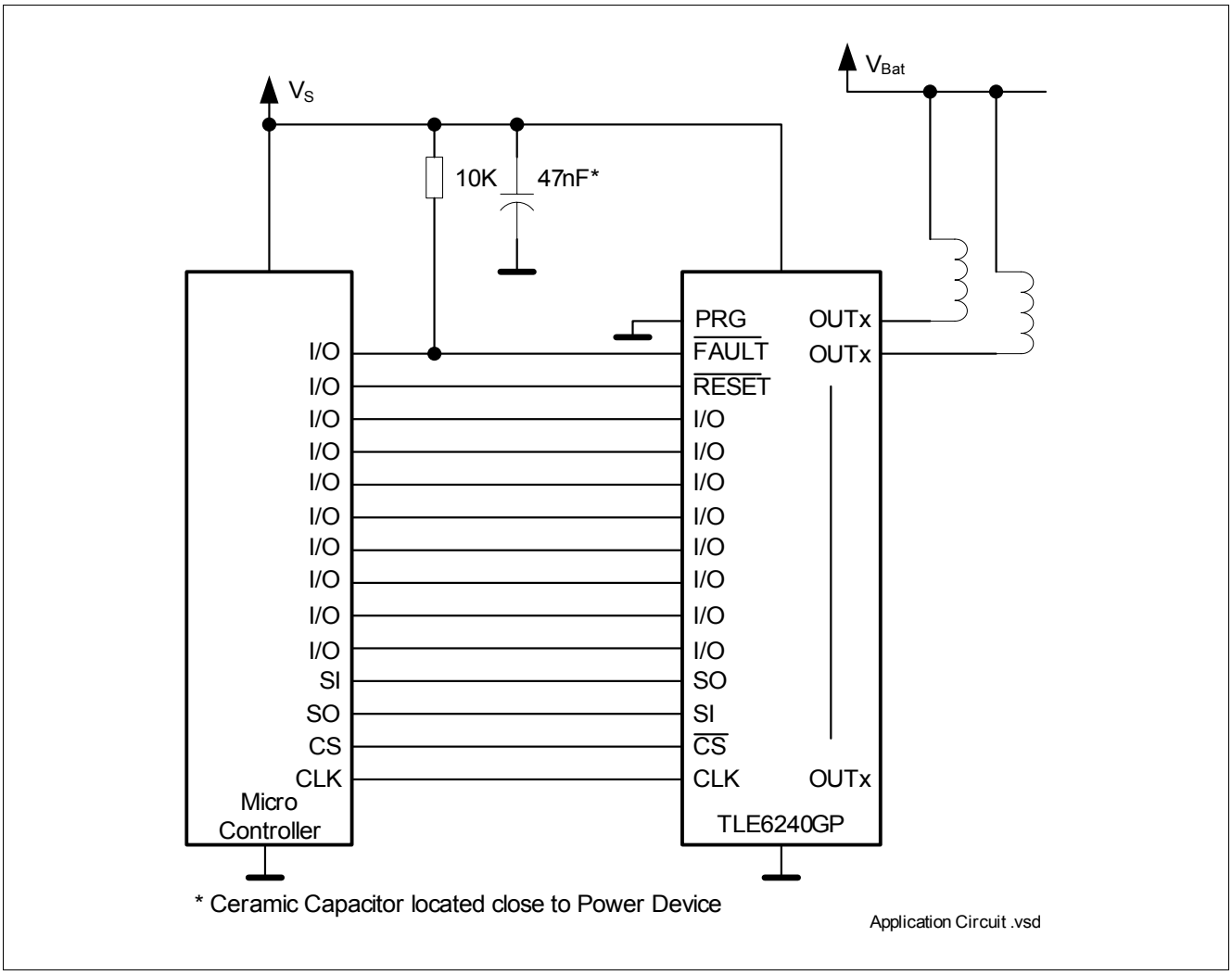


Figure 23 Application Circuit

7.2 Engine Management Application

TLE6240GP can be used in combination with Multichannel Switches for relays and general purpose loads. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 28 channels in sum 16 can be controlled direct in parallel for PWM applications.

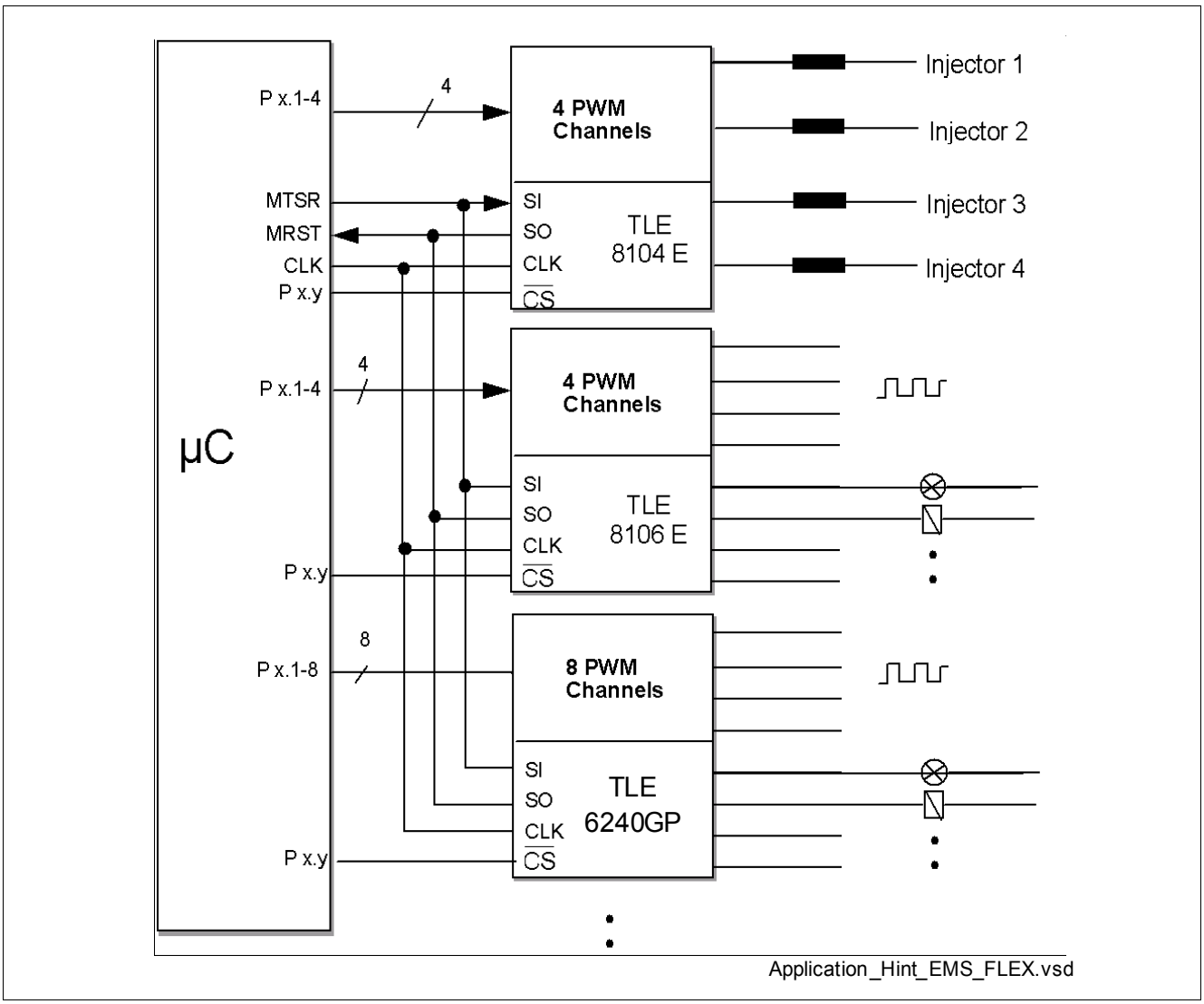


Figure 24 Engine Management Application

7.3 Daisy Chain Application

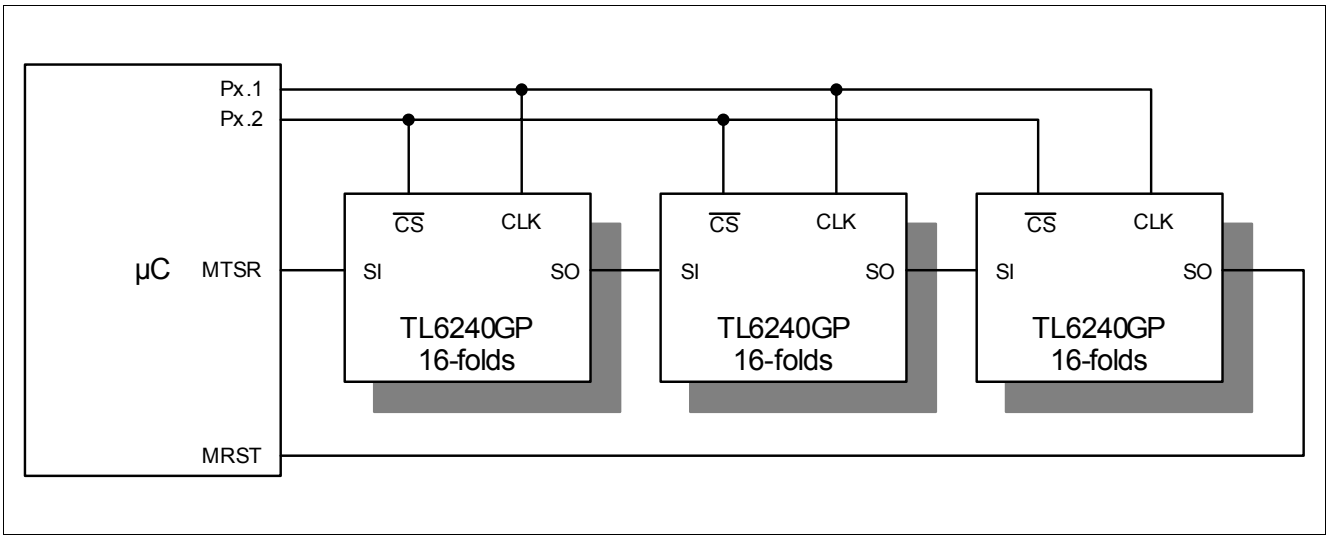
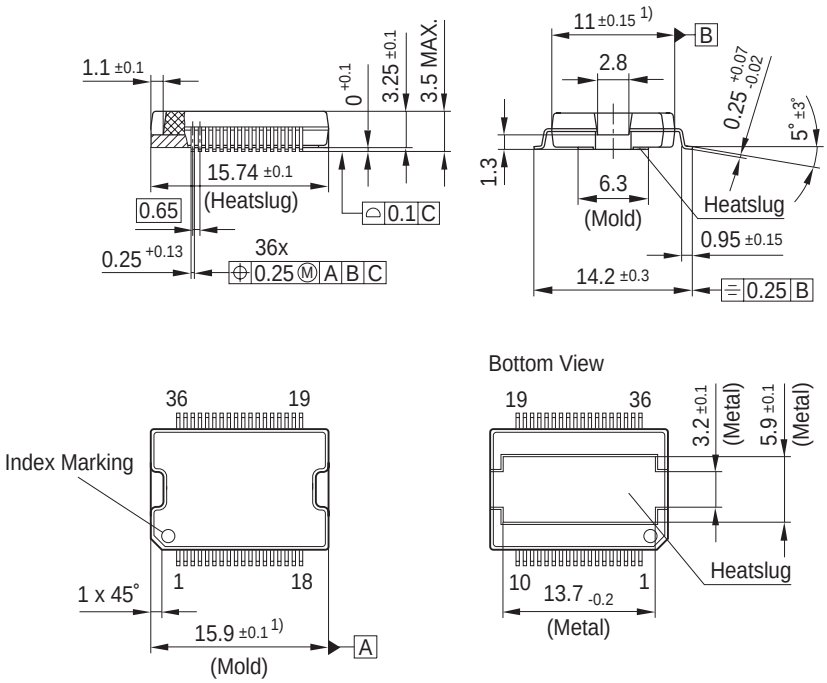


Figure 25 Daisy Chain Application

8 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09181

Figure 26 PG-DSO-36 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

9 Revision History

Version	Date	Changes
V3.3, 2010-02-15, up-date		
V3.3	2010-02-15	Template up-date
		ESD standard up-date
		Thermal Resistance parameters up-date
		Temperature range for functional range added
		Package name modified

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