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TLE6258-2G

LIN Transceiver

Automotive Power

Never stop thinking

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Infineon Technologies AG
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LIN Transceiver TLE6258-2G

Features

- Single-wire transceiver, suitable for **LIN** protocol
- Compatible to LIN specification 1.2, 1.3 and 2.0
- Compatible to ISO 9141 functions
- Transmission rate up to 20 kBaud
- Very low current consumption in stand-by mode
- Wake-up from Bus
- Short circuit proof to ground and battery
- Overtemperature protection
- Green Product (RoHS compliant)
- AEC Qualified

Description

The single wire transceiver TLE6258-2G is a monolithic integrated circuit in a PG-DSO-8 package. It works as an interface between the protocol controller and the physical bus. The TLE6258-2G is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the TLE6258-2G offers a stand-by mode. A wake-up caused by a message on the bus sets the RxD output low until the device is switched to normal operation mode.

The IC is based on the Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

The TLE6258-2G is designed to withstand the severe conditions of automotive applications.

Type	Package
TLE6258-2G	PG-DSO-8

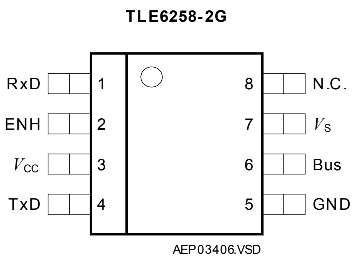

Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	RxD	**Receive data output;** integrated pull-up, LOW in dominant state
2	ENN	**Enable not input;** integrated 30 kΩ pull-up, transceiver in normal operation mode when LOW
3	V_{CC}	**5 V supply input**
4	TxD	**Transmit data input;** integrated pull-up, LOW in dominant state
5	GND	**Ground**
6	Bus	**Bus output/input;** internal 30 kΩ pull-up, LOW in dominant state
7	V_S	**Battery supply input**
8	n.c.	**Not connected**

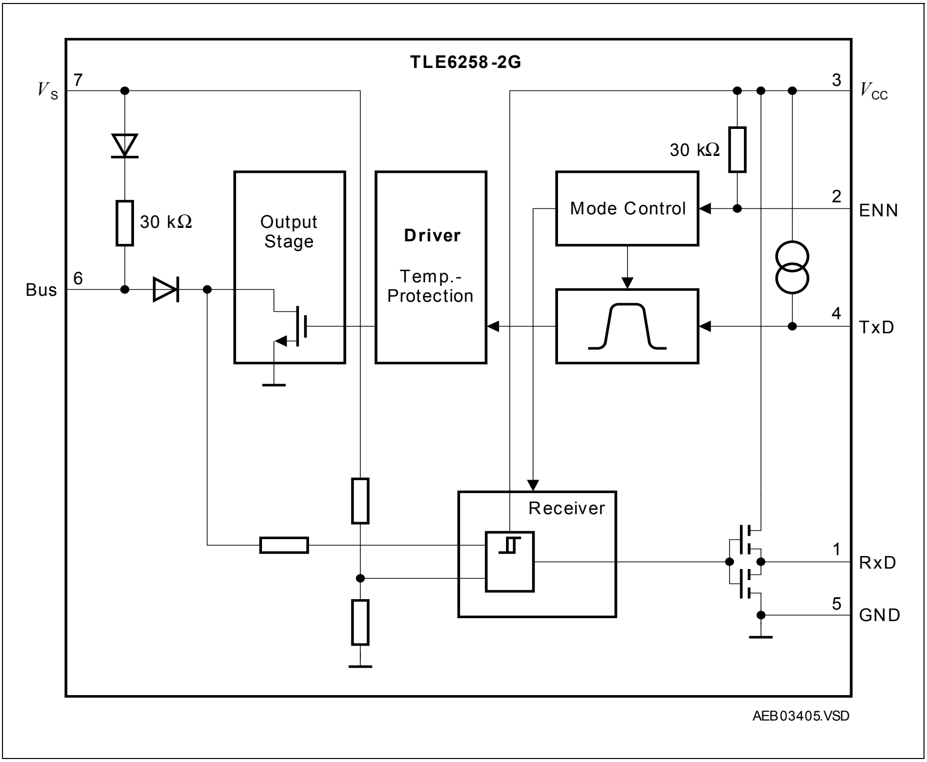

Figure 2 Functional Block Diagram

Application Information

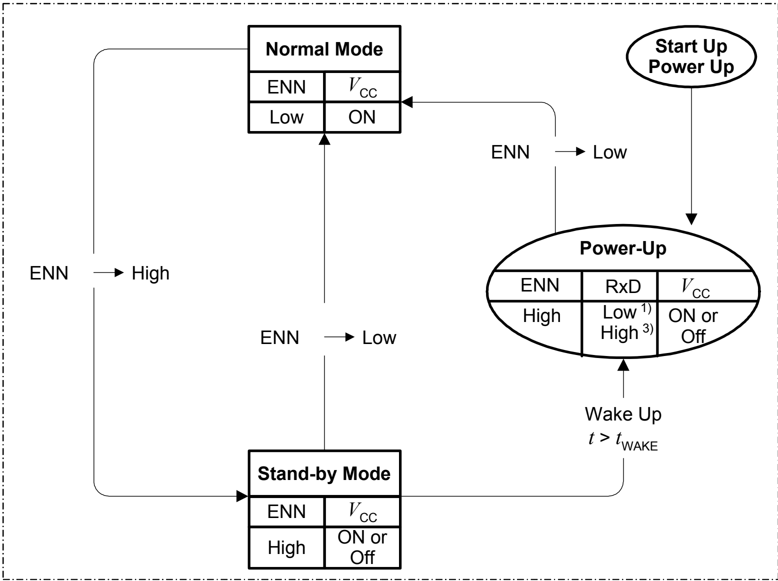

Figure 3 State Diagram

For fail safe reasons the TLE6258-2G has already a pull-up resistor of 30 kΩ implemented. To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is required. It is recommended to place this resistor in the master node. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is recommended to place a diode in series to the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF in the master node (see **Figure 6**).

In order to reduce the current consumption the TLE6258-2G offers a stand-by mode. This mode is selected by switching the Enable Not (ENN) input high (see **Figure 3**). In the stand-by mode a wake-up caused by a message on the bus is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Supply voltage	V_{CC}	-0.3	6	V	–
Battery supply voltage	V_S	-0.3	40	V	–
Bus input voltage	V_{bus}	-20	32	V	–
Bus input voltage	V_{bus}	-20	40	V	t < 1 s
Logic voltages at EN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Electrostatic discharge voltage at V_S, Bus	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{CC}	4.5	5.5	V	–
Battery Supply Voltage	V_S	6	35	V	–
Junction temperature	T_j	-40	150	°C	–
Thermal Shutdown (junction temperature)					
Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K
Thermal Resistances					
Junction ambient	$R_{thj\text{-}a}$	–	185	K/W	–

Table 4 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L = 500 Ω; V_{ENN} < $V_{ENN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
Current Consumption						
Current consumption	I_{CC}	–	0.4	0.7	mA	recessive state; V_{TxD} = V_{CC}
Current consumption	I_S	–	0.5	1.0	mA	recessive state; V_{TxD} = V_{CC}
Current consumption	I_{CC}	–	0.4	0.8	mA	dominant state; V_{TxD} = 0 V; without R_L
Current consumption	I_S	–	1.3	2.0	mA	dominant state; V_{TxD} = 0 V; without R_L
Current consumption	I_{CC}		0.4	0.7	mA	power-up mode
Current consumption	I_S	–	0.5	1.0	mA	power-up mode, V_{CC} = 0 V, V_S = 13.5 V
Current consumption	I_{CC}	1	3	10	µA	stand-by mode
Current consumption	I_S	–	18	40	µA	stand-by mode

Table 4 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L = 500 Ω; V_{ENN} < $V_{ENN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
Enable Not Input (pin ENN)						
HIGH level input voltage threshold	$V_{ENN,off}$	–	2.8	0.7 × V_{CC}	V	low power mode
LOW level input voltage threshold	$V_{ENN,on}$	0.3 × V_{CC}	2.2	–	V	normal operation mode
ENN input hysteresis	$V_{ENN,hys}$	300	600	900	mV	–
ENN pull-up resistance	R_{ENN}	15	30	60	kΩ	–
Receiver Output RxD						
HIGH level output current	$I_{RD,H}$	-1.2	-0.8	-0.5	mA	$V_{RD} = 0.8 \times V_{CC}$
LOW level output current	$I_{RD,L}$	0.5	0.8	1.2	mA	$V_{RD} = 0.2 \times V_{CC}$
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TD,H}$	–	2.9	0.7 × V_{CC}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	700	900	mV	–
LOW level input voltage threshold	$V_{TD,L}$	0.3 × V_{CC}	2.1	–	V	dominant state
TxD pull-up current	I_{TD}	-150	-110	-70	µA	$V_{TxD} < 0.3 \times V_{CC}$

Table 4 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L = 500 Ω; V_{ENN} < $V_{ENN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
Bus Receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 × V_S	0.48 × V_S	–	V	-8 V < V_{bus} < $V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$	–	0.56 × V_S	0.6 × V_S	V	$V_{bus,rec}$ < V_{bus} < 20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 × V_S	0.04 × V_S	0.1 × V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
Receiver threshold center voltage	$V_{bus,cnt}$	0.475 × V_S	0.5 × V_S	0.525 × V_S		LIN2.0 table 3.1
Input leakage current	$I_{bus,lek}$	-1			mA	V_{bus} = 0V, V_{bat} = 12V, pull-up resistor as specified in LIN2.0
Wake-up threshold voltage	V_{wake}	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–
Bus Transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 × V_S	–	V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$	0	–	2	V	V_{TxD} = 0 V 7.3V<V_S<27V
		0	–	1.2	V	V_{TxD} = 0 V 6V<V_S<7.3V
Bus short circuit current	$I_{bus,sc}$	40	100	150	mA	$V_{bus,short}$ = 13.5 V
Leakage current	$I_{bus,lk}$	-1	-	–	mA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V,
		–	10	20	µA	V_{CC} = 0 V, V_S = 13.5V, V_{bus} = 20 V,
Bus pull-up resistance	R_{bus}	20	30	47	kΩ	–

Table 4 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L = 500 Ω; V_{ENN} < $V_{ENN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
Dynamic Transceiver Characteristics						
Falling edge slew rate	$S_{bus(L)}$	-3	-2.0	-1	V/µs	[1] 60% > V_{bus} > 40% 1 µs < (τ = $R_L \times C_{BUS}$) < 5 µs; V_{CC} = 5 V; V_S = 13.5 V
Rising edge slew rate	$S_{bus(H)}$	1	1.5	3	V/µs	[1] 40% < V_{bus} < 60% 1 µs < (τ = $R_L \times C_{BUS}$) < 5 µs; V_{CC} = 5 V; V_S = 13.5 V
Slope symmetry	$t_{slopesym}$	5		-5	µs	t_{fslope} - t_{rslope} V_S = 18 V
Propagation delay TxD LOW to bus	$t_{d(L),T}$	–	1	3	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$	–	1	3	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T} = t_{d(L),T} - t_{d(H),T}$
Duty cycle D1	t_{duty1}	0.396	–	–	µs	duty cycle 1 [1] TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit};
Duty cycle D2	t_{duty2}	–	–	0.581	µs	duty cycle 2 [1] TH_{Rec}(max) = 0.422× V_S; TH_{Dom}(max) = 0.264 × V_S V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit};

Table 4 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L = 500 Ω; V_{ENN} < $V_{ENN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remark
		Min.	Typ.	Max.		
Wake-up delay time	t_{wake}	30	100	150	µs	T_j < 125 °C
				170	µs	T_j < 150 °C
Delay time for mode change	t_{snorm}			50	µs	

1) Bus load conditions concerning LIN spec 2.0 C_{bus}, R_{bus} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω

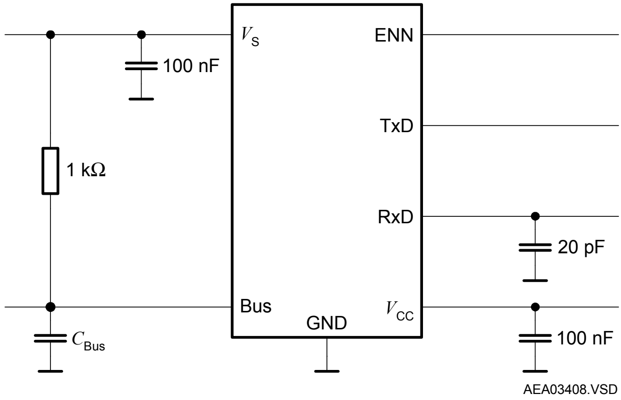

Figure 4 Test Circuits

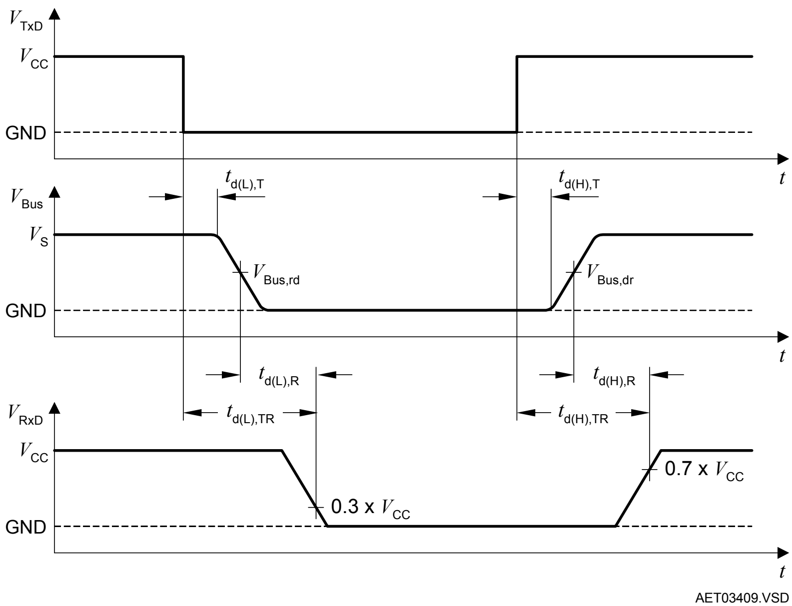

Figure 5 Timing Diagram for Dynamic Characteristics

Application

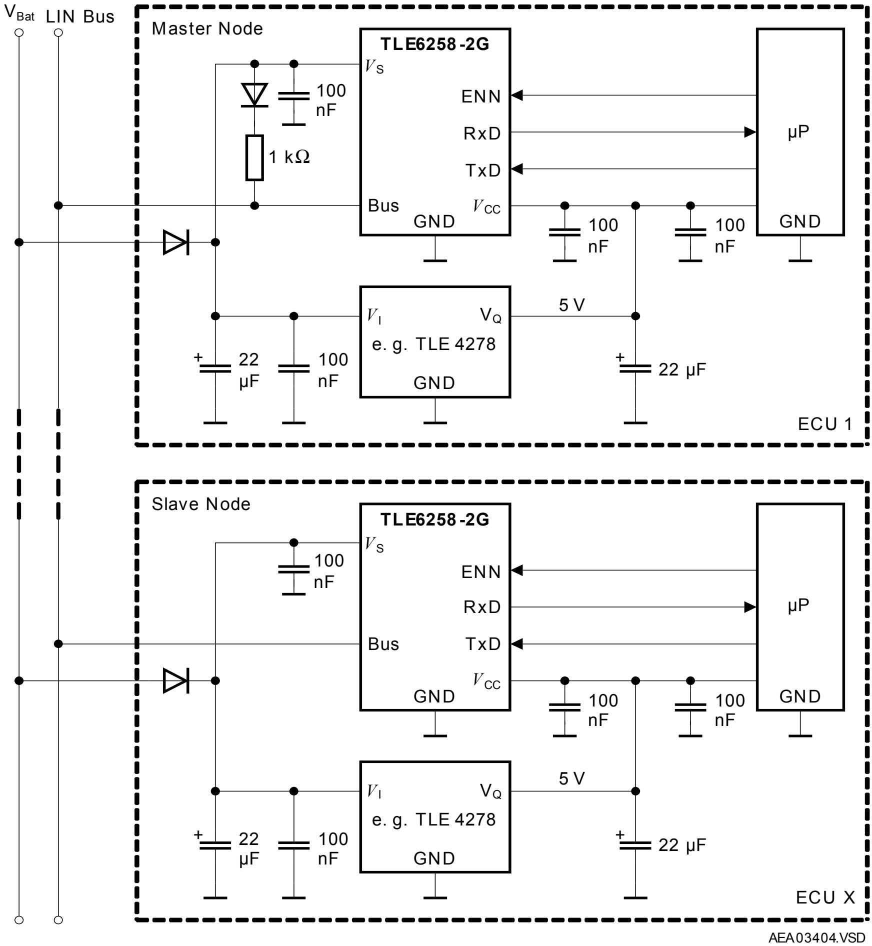

Figure 6 Application Circuit

Package Outlines

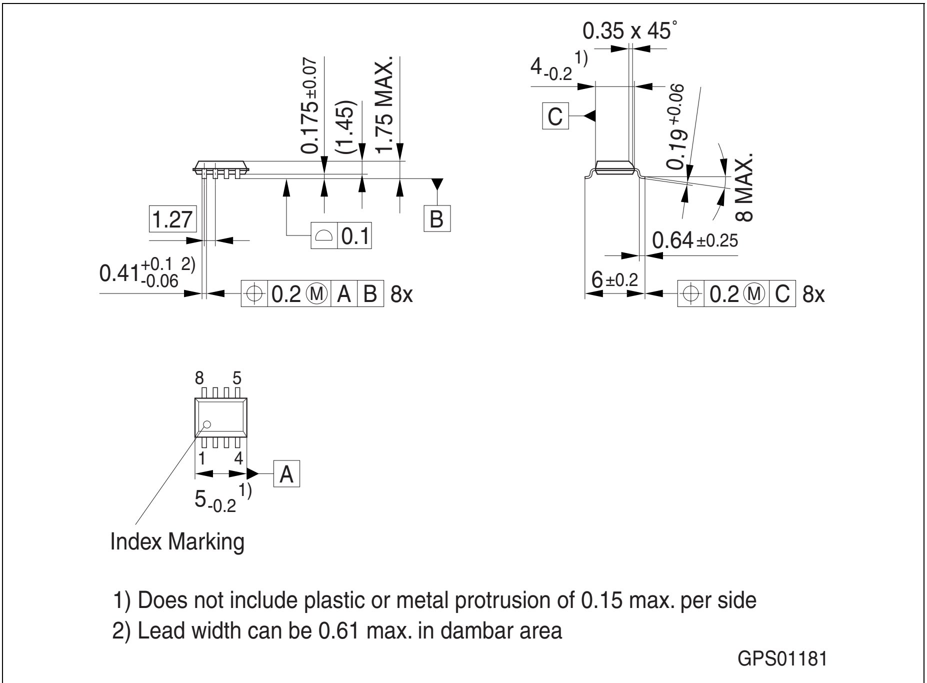

Figure 7 **PG-DSO-8** (PG-DSO-8-16 Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

Revision History

Version	Date	Changes
Rev. 2.1	2007-08-08	RoHS-compliant version of the TLE6258-2G • All pages: Infineon logo updated • Page 3: added "AEC qualified" and "RoHS" logo, "Green Product (RoHS compliant)" and "AEC qualified" statement added to feature list, package name changed to RoHS compliant versions, package picture updated, ordering code removed • Page 15: Changed package drawing to GPS01181 Package name changed to RoHS compliant versions, "Green Product" description added • added Revision History • updated Legal Disclaimer