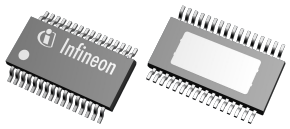
MOTIX™ 48 V/24 V bridge driver

Features



- Drive B6-bridge for BLDC motors in 24 V/48 V platforms with protection features
- Compatible with general microcontroller and MOTIX™ MCU
- High voltage capability/robustness up to 100 V helps to simplify PCB design
- 16-bit serial peripheral interface
- Charge pump concept to support 100% duty cycle
- Undervoltage shutdown
- Overvoltage shutdown
- Overtemperature protection
- Drain-source monitoring
- Timeout watchdog
- Cross-current protection
- Off-state diagnostic
- Adaptive MOSFET control

RoHS

AEC Qualified

ISO 26262 compliant

Potential applications

- Can be used to drive B6-bridge for BLDC motors with battery voltage up to 72 V (load dump) for 24 V/48 V applications for example engine cooling fan, water pump and oil pump
- Can be used together with general microcontroller to transfer the applications to 24 V/48 V platforms
- Can be used together with MOTIX™ MCU to transfer the applications to 24V/48V platforms with minor software development effort

Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100.

Description

This device is a 48 V MOSFET gate driver compatible with general microcontrollers and MOTIX™ MCU to drive max. 3 half-bridges in 24 V/48 V platform. It provides protection features and the possibility to use the diagnosis features integrated in the MOTIX™ MCU.

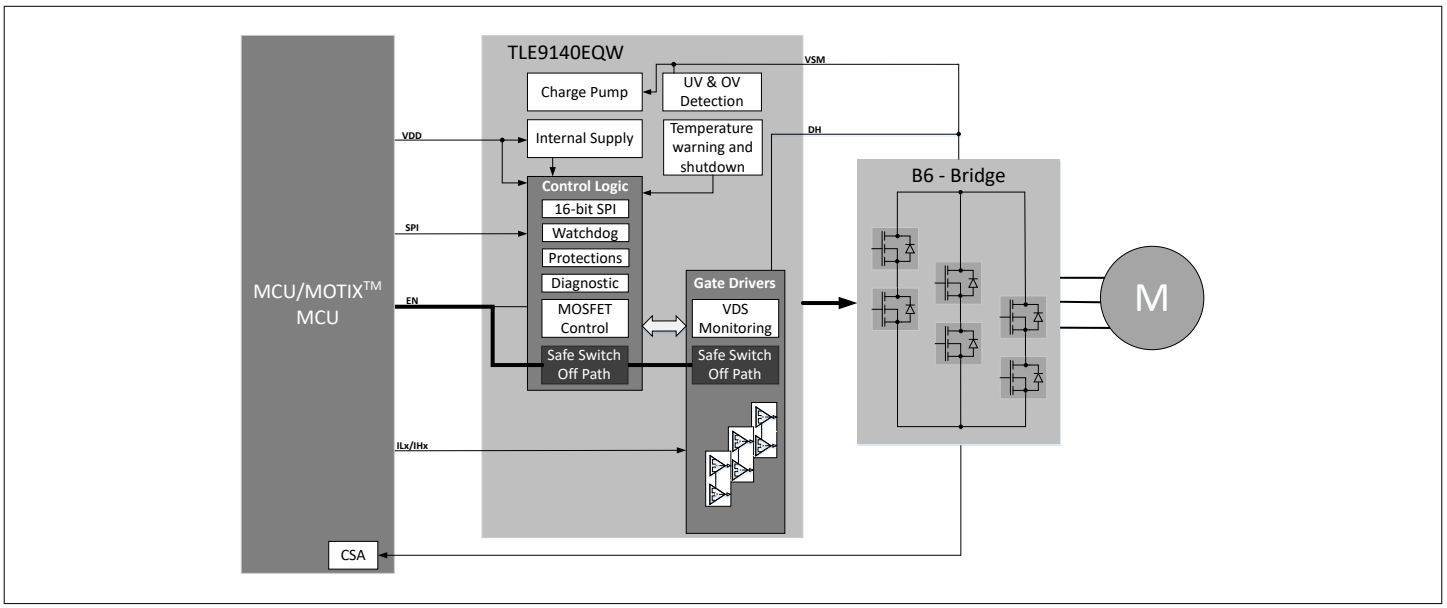


Table 1 Product summary

Parameter	Symbol	Value
Specified supply voltage range	$V_{S(nor)}$	8.0 V to 72 V
Max. total charge driver capability	Q_{tot_max}	290 nC * 6 @ 20 kHz
Max. undervoltage threshold	V_{SUV_ON}	20.0 V/8.0 V
Min. overvoltage threshold	V_{SOV_ON}	72.0 V/48.0 V
Max. total quiescent current	$I_{DDQ} + I_{SQ}$	26 µA
Product type	**Package**	**Marking**
TLE9140EQW	PG-TSDSO-32	TLE9140EQW

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1 Block diagram

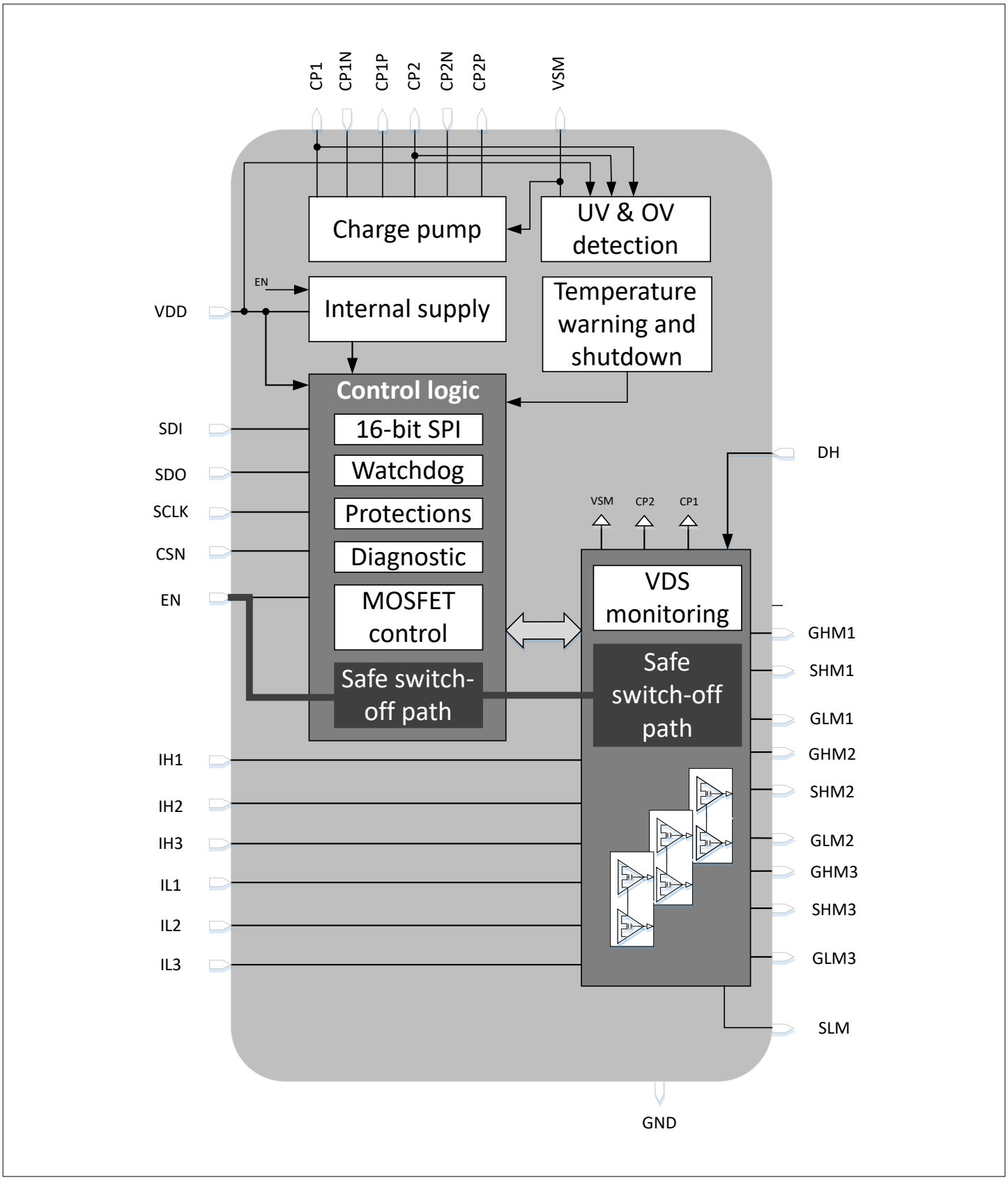

Figure 1 Block diagram

2 Pin configuration

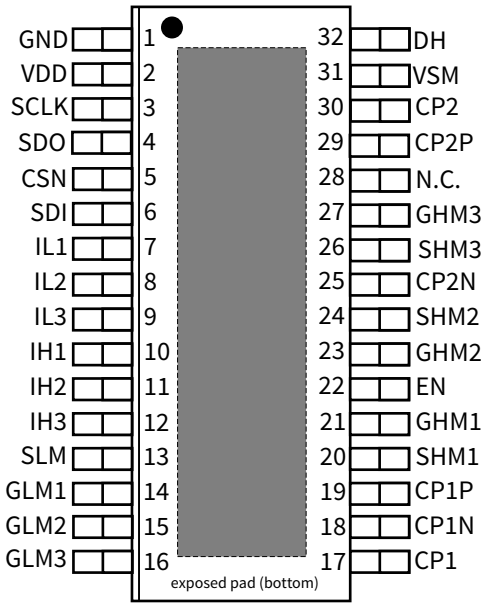

Figure 2 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	Function
1	GND	**Ground**
2	VDD	**VDD supply voltage** (connect to MCU/MOTIX™ MCU) Power supply for digital circuits
3	SCLK	**Serial clock input** (connect to MCU/MOTIX™ MCU)
4	SDO	**Serial data output** (connect to MCU/MOTIX™ MCU)
5	CSN	**Chip select not** (connect to MCU/MOTIX™ MCU)
6	SDI	**Serial data input** (connect to MCU/MOTIX™ MCU)
7	IL1	**Low-side 1 gate control** (connect to MCU/MOTIX™ MCU)
8	IL2	**Low-side 2 gate control** (connect to MCU/MOTIX™ MCU)
9	IL3	**Low-side 3 gate control** (connect to MCU/MOTIX™ MCU)
10	IH1	**High-side 1 gate control** ((connect to MCU/MOTIX™ MCU)
11	IH2	**High-side 2 gate control** (connect to MCU/MOTIX™ MCU)
12	IH3	**High-side 3 gate control** (connect to MCU/MOTIX™ MCU)
13	SLM	**Source low-side** Common connection to the source of the low-side MOSFETs
14	GLM1	**Gate low-side 1**
15	GLM2	**Gate low-side 2**

(table continues...)

Table 2 (continued) Pin definitions and functions

Pin	Symbol	Function
16	GLM3	**Gate low-side 3**
17	CP1	**Output of charge pump 1**
18	CP1N	**Negative connection to charge pump capacitor 1**
19	CP1P	**Positive connection to charge pump capacitor 1**
20	SHM1	**Source high-side 1**
21	GHM1	**Gate high-side 1**
22	EN	**Enable**
23	GHM2	**Gate high-side 2**
24	SHM2	**Source high-side 2**
25	CP2N	**Negative connection to charge pump capacitor 2**
26	SHM3	**Source high-side 3**
27	GHM3	**Gate high-side 3**
28	N.C.	**Unconnected pin**
29	CP2P	**Positive connection to charge pump capacitor 2**
30	CP2	**Output of charge pump 2**
31	VSM	**Voltage supply** Connect to supply voltage (battery) with reverse polarity protection circuit
32	DH	**Drain high-side** Connect to the drain of high-side MOSFETs

3 General product characteristics

3.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

T_j = -40°C to 175°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_{SM}	-0.3	–	90	V	–	P_GPC_01_01
Logic supply voltage	V_{DD}	-0.3	–	5.5	V	–	P_GPC_01_02
Logic input voltages (IHx, ILx)	V_{ILX}, V_{IHX}	-0.3	–	20	V	–	P_GPC_01_03
Logic input voltages (SCLK, CSN)	V_{SCLK}, V_{CSN}	-0.3	–	V_{DD} + 0.3	V	–	P_GPC_01_04
Logic input voltages (SDI)	V_{SDI}	-0.3	–	V_{DD} + 0.3	V	I < 10mA	P_GPC_01_05
Logic input voltages (EN)	V_{EN}	-0.3	–	V_{DD} + 0.3	V	I < 10 mA	P_GPC_01_06
Voltage at SDO	V_{SDO}	-0.3	–	V_{DD} + 0.3	V	–	P_GPC_01_07
Voltage range at DH	V_{DH}	-0.3	–	90	V	–	P_GPC_01_08
Voltage range at GHMx	V_{GHMx}	-10.0	–	100	V	–	P_GPC_01_09
Dynamic voltage range at GHMx	V_{GHMx}	–	–	110	V	< 500 ns	P_GPC_01_10
Voltage range at SHMx	V_{SHMx}	-10.0	–	100	V	–	P_GPC_01_11
Dynamic voltage range at SHMx	V_{SHMx}	–	–	110	V	< 500 ns	P_GPC_01_12
Voltage range at GLMx	V_{GLMx}	-7.0	–	20	V	–	P_GPC_01_13
Voltage range at SLM	V_{SLM}	-7.0	–	6.0	V	–	P_GPC_01_14
Voltage difference between GHMx-SHMx and GLMx-SLM	V_{GSM}	-0.3	–	13	V	Bridge drivers are active.	P_GPC_01_15
Voltage difference between GHMx-SHMx and GLMx-SLM	V_{GSM}	-0.3	–	7		Bridges drivers are off.	P_GPC_01_30

(table continues...)

Table 3 (continued) Absolute maximum ratings

T_j = -40°C to 175°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage range at charge pump pin CP1	V_{CP1}	-0.3	–	20	V	–	P_GPC_01_16
Voltage range at charge pump pin CP1N	V_{CP1N}	-0.3	–	V_{CP1} + 0.3	V	–	P_GPC_01_17
Voltage range at charge pump pin CP1P	V_{CP1P}	-0.3	–	90	V	–	P_GPC_01_25
Voltage difference between VSM and CP1N pins	V_{SM} - V_{CP1N}	-0.3	–	V_{SM}	V	–	P_GPC_01_26
Voltage range at charge pump pin CP2P	V_{CP2P}	V_{SM} - 0.3	–	100	V	–	P_GPC_01_18
Voltage range at charge pump pin CP2	V_{CP2}	V_{SM} - 0.6	–	100	V	–	P_GPC_01_19
Voltage range at charge pump pin CP2N	V_{CP2N}	-0.3	–	100	V	–	P_GPC_01_20
Temperatures							
Junction temperature	T_j	-40	–	175	°C	–	P_GPC_01_21
ESD susceptibility							
ESD susceptibility all pins 1	$V_{ESDHBM1}$	-2	–	2	kV	HBM [1)]	P_GPC_01_22
ESD susceptibility all pins 2	$V_{ESDCDM1}$	-500	–	500	V	CDM [2)]	P_GPC_01_23
ESD susceptibility pin corner pins	$V_{ESDCDM2}$	-750	–	750	V	CDM [2)]	P_GPC_01_24

1) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
2) ESD susceptibility, Charged device model (CDM) according JEDEC JESD22-C101.

3.2 Functional range

Table 4 Functional range

T_j = -40°C to 175°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{SM(nor)}$	8.0	–	60	V	–	P_GPC_02_01
Extended supply voltage range	$V_{SM(ext)}$	8.0	–	75	V	Note: All parameters are specified with the condition 8.0 V < VSM < 60 V. They may have deviations in extended supply voltage range.	P_GPC_02_02
Voltage range at DH	V_{DH}	8.0	–	85	V	–	P_GPC_02_03
Logic supply voltage	V_{DD}	3.0	–	5.5	V	–	P_GPC_02_04
Junction temperature	T_j	-40	–	150	°C	–	P_GPC_02_05
Extended junction temperature	T_{j_ext}	-40	–	175	°C	–	P_GPC_02_06

3.3 Thermal resistance

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	1.93	–	k/W	T_a = 85°C	P_GPC_03_01
Junction to ambient	R_{thJA}	–	27.12	–	k/W	T_a = 85°C; Package on JEDEC 2s2p with thermal VIAs	P_GPC_03_02

4 General description

4.1 Operation modes

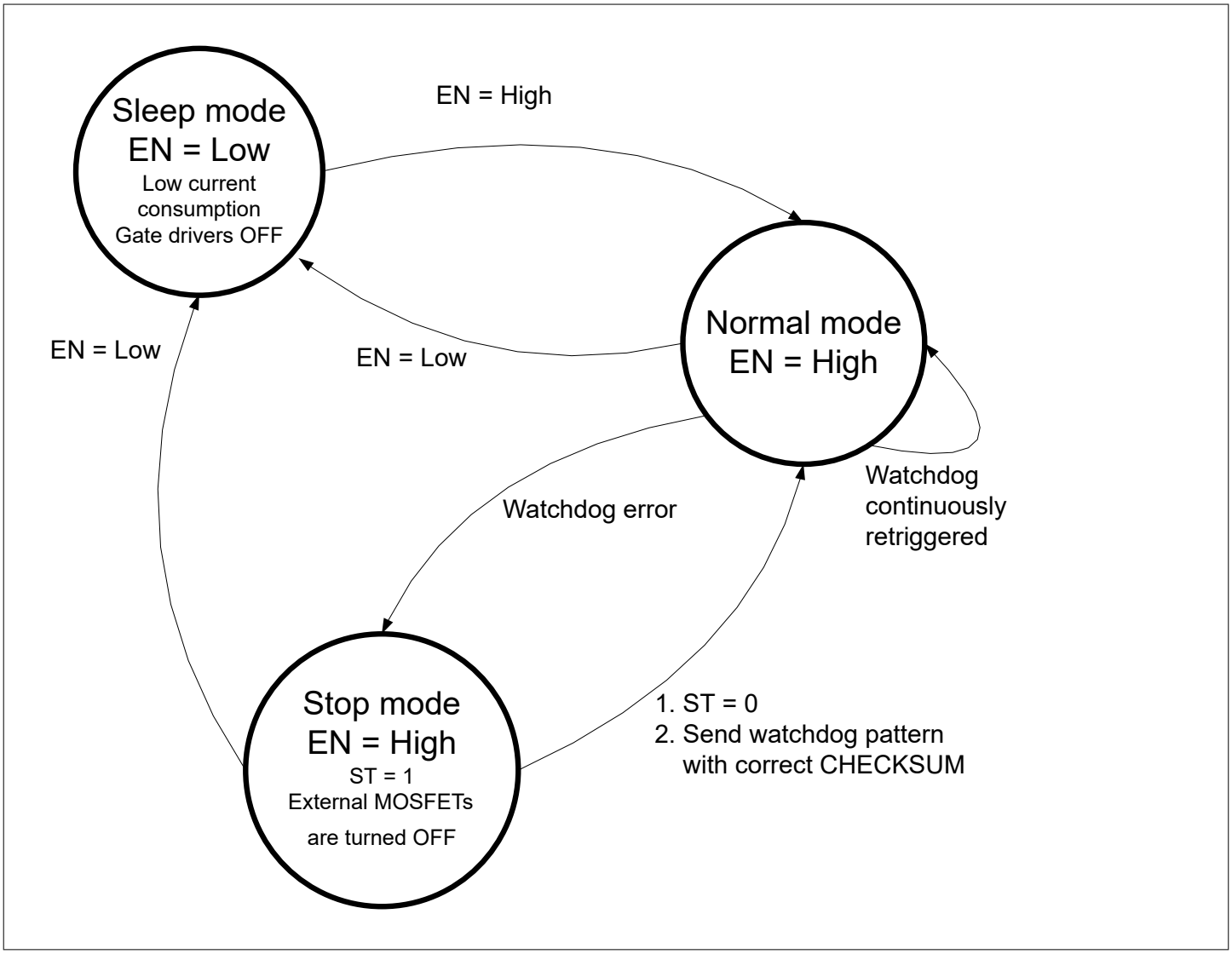

Figure 3 State diagram

4.1.1 Normal mode

The device enters normal operation mode if EN pin is set to high for a duration longer than SPI setup time t_{SET_SPI}.

The device will stay in the normal operation mode if the watchdog is retriggered in the defined watchdog period and the EN is kept to high.

In normal operation mode, the device behaves as follows:

- All functions and all diagnostics are available
- The output drivers can be enabled and configured through the SPI in error free condition

Note: In case of SPI error, the SPI frame which contains an error will be ignored and the SPIE bit will be set. The next valid SPI frame will be accepted, but the SPIE bit remains until it is cleared by the SPI command.

4.1.2 Sleep mode

Sleep mode is a low power mode with quiescent current of V_{DD} and V_{SM} reduced respectively to I_{DD_Q} and I_{SMQ}.
If EN is set to low for a duration longer than EN filter time t_{EN_FILT}, the device will:

- Turn-off the external MOSFETs actively
- Enter sleep mode with a delay defined by t_{DSLEEP}

In sleep mode, the device behaves as follows:

- Turn-off the external MOSFETs with pull down resistors
- Deactivate the internal circuits and the power supply structure
- Reset the SPI registers

4.1.3 Stop mode

In case of watchdog error, the device will:

- Turn-off external MOSFETs
- Set ST bit (see STAT and Global status byte)
- Enter stop mode

In stop mode, the device behaves as follows:

- The control registers are reset to default values
- Any write command or clear command (except ST bit in STAT) will be discarded
- A clear command to status registers does not reset any failure flag except ST bit in STAT
- Control and status registers are allowed to be read in this mode

The device will resume normal mode from stop mode if the microcontroller executes the following sequence:

1. Clear the ST bit in STAT
2. Send watchdog pattern with correct CHECKSUM bit

Note: Only a correct SPI protocol transaction in between can interrupt the exit sequence.

4.2 Reset behavior

The device resumes normal operation mode, and the nPOR bit in STAT and Global status byte is reset to 0 to report the reset condition if the following conditions are fulfilled:

- EN is set to high for a duration longer than t_{SET_SPI}
- $V_{DD} > V_{DD\_POR}$

In case of V_{DD} undervoltage, if V_{DD} is rising above V_{DD_POR} again, the device behaves as follows:

- Reset the digital block
- Set NPOR bit to 0 to report the reset condition
- Resume normal operation mode

4.3 Power supply

The device is supplied by V_{DD} and V_{SM}. The V_{DD} supplies the digital I/O ports, and V_{SM} supplies the buck/boost charge pump (charge pump 1) and the single stage charge pump (charge pump 2).

The output of the buck/boost charge pump (CP1) is regulated at V_{CP1}, and supplies:

- The low side gate drivers
- The single stage charge pump

The output voltage of the single stage CP2 is used to supply the high side gate drivers.

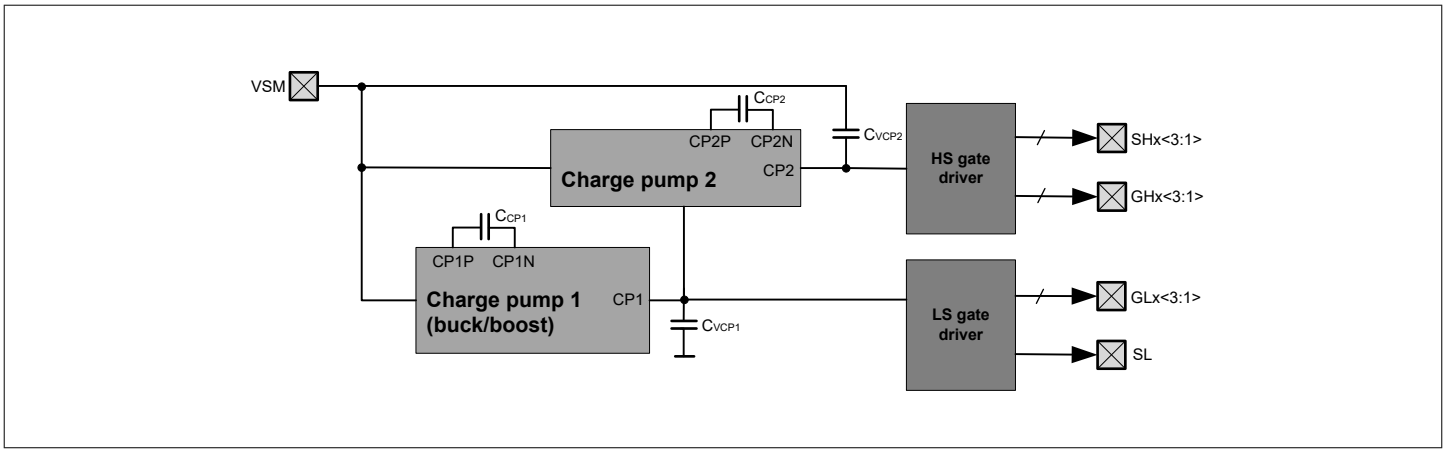

Figure 4 Power supply

4.4 Electrical characteristics

Table 6 Supply

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption, EN = low							
Supply quiescent current	I_{SMQ}	–	7	15	µA	T_j < 85 °C	P_GEN_01_01
Supply quiescent current extended	I_{SMQ_EXT}	–	–	40	µA	150°C < T_j ≤ 175°C	P_GEN_01_03
Logic supply quiescent current	I_{DDQ}	–	3	10	µA	T_j < 85 °C	P_GEN_01_04
Logic supply quiescent current extended	I_{DDQ_EXT}	–	–	120	µA	150° < T_j ≤ 175°C	P_GEN_01_06
Total quiescent current	I_{DDQ} + I_{SMQ}	–	8.5	26	µA	T_j < 85 °C	P_GEN_01_07
Sleep mode delay	t_{DSLEEP}	2.5	4.4	10	µs	–	P_GEN_01_08
EN low filter time	t_{EN_FILT}	1	2.4	4.5	µs	–	P_GEN_01_09
Current consumption, EN = high							
Supply current	I_{SM_NOR1}	–	125	150	mA	13 V < V_{SM} < 19 V, BD_EN = 1b, I_{Load_CP1} = 19.1mA, I_{Load_CP2} = 19.1mA	P_GEN_01_20

(table continues...)

Table 6 (continued) Supply

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply current	I_{SM_NOR2}	–	62	85	mA	19 V < V_{SM} < 60 V, BD_EN = 1b, I_{Load_CP1} = 19.1 mA, I_{Load_CP2} = 19.1 mA	P_GEN_01_21
Logic supply current	I_{DD1}	–	3.75	6	mA	$T_j \leq$ 150 °C; CP_EN = 0b; BD_EN = 0b	P_GEN_01_22
V_S							
UV switch ON voltage (VSM_COVUVTH = 000B, 001B,010B or 011B)	V_{SMUV_ON1}	18	19	20	V	V_{SM} increasing	P_GEN_01_23
UV switch ON voltage (VSM_COVUVTH = 100B)	V_{SMUV_ON2}	7.0	7.5	8.0	V	V_{SM} increasing	P_GEN_01_24
UV switch OFF voltage (VSM_COVUVTH = 000B, 001B,010B or 011B)	V_{SMUV_OFF1}	17.5	18.5	19.5	V	V_{SM} decreasing	P_GEN_01_25
UV switch OFF voltage (VSM_COVUVTH = 100B)	V_{SMUV_OFF2}	6.5	7.0	7.5	V	V_{SM} decreasing	P_GEN_01_26
UV ON/OFF hysteresis	V_{SMUV_HY}	0.3	0.5	0.7	V	V_{SMUV_ON} - V_{SMUV_OFF}	P_GEN_01_27
OV switch ON voltage (VSM_COVUVTH = 000B)	V_{SMCOV_ON1}	53	55	57	V	V_{SM} decreasing	P_GEN_01_28
OV switch ON voltage (VSM_COVUVTH = 001B)	V_{SMCOV_ON2}	55	57	59	V	V_{SM} decreasing	P_GEN_01_29

(table continues...)

Table 6 (continued) Supply

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OV switch ON voltage (VSM_COVUVTH = 010B)	V_{SMCOV_ON3}	57	59	61	V	V_{SM} decreasing	P_GEN_01_30
OV switch ON voltage (VSM_COVUVTH = 011B)	V_{SMCOV_ON4}	59	61	63	V	V_{SM} decreasing	P_GEN_01_31
OV switch ON voltage (VSM_COVUVTH = 100B)	V_{SMCOV_ON5}	48	50	52	V	V_{SM} decreasing	P_GEN_01_32
Hard OV switch ON voltage	V_{SMOV_ON}	71	74	76	V	V_{SM} decreasing	P_GEN_01_33
OV switch OFF voltage (VSM_COVUVTH = 000B)	V_{SMCOV_OFF1}	54	56	58	V	V_{SM} increasing	P_GEN_01_34
OV switch OFF voltage (VSM_COVUVTH = 001B)	V_{SMCOV_OFF2}	56	58	60	V	V_{SM} increasing	P_GEN_01_35
OV switch OFF voltage (VSM_COVUVTH = 010B)	V_{SMCOV_OFF3}	58	60	62	V	V_{SM} increasing	P_GEN_01_36
OV switch OFF voltage (VSM_COVUVTH = 011B)	V_{SMCOV_OFF4}	60	62	64	V	V_{SM} increasing	P_GEN_01_37
OV switch OFF voltage (VSM_COVUVTH = 100B)	V_{SMCOV_OFF5}	49	51	53	V	V_{SM} increasing	P_GEN_01_38
Hard OV switch OFF voltage	V_{SMOV_OFF}	72	75	77	V	V_{SM} increasing	P_GEN_01_39
OV ON/OFF hysteresis	V_{SMOV_HY}	0.5	1	2	V	V_{SMOV_ON} - V_{SMOV_OFF} or V_{SMCOV_ONx} - V_{SMCOV_OFFx}	P_GEN_01_40

(table continues...)

Table 6 (continued) Supply

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
V_{DD}							
VDD Power-On-Reset	V_{DD_POR}	2.50	2.70	2.90	V	V_{DD} increasing	P_GEN_01_41
VDD Power-Off-Reset	V_{DD_POFFR}	2.40	2.60	2.80	V	V_{DD} decreasing	P_GEN_01_42
VDD Power-On-Reset hysteresis	$V_{DD\_POR\_HY}$	30	–	–	mV	V_{DD_POR} - V_{DD_POFFR}	P_GEN_01_43

Table 7 EN

V_{SM} = 8.0 V to 60 V, T_j = -40°C to + 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
EN high level	V_{ENH}	0.75∗V_{DD}	–	V_{DD}	V	–	P_GEN_02_01
EN low level	V_{ENL}	–	–	0.25∗V_{DD}	V	–	P_GEN_02_02
EN hysteresis	V_{ENHY}	50	400	–	mV	–	P_GEN_02_03
EN pull-down resistor	R_{PD_EN}	25	40	60	kΩ	–	P_GEN_02_04

Table 8 Charge pumps

V_{SM} = 8.0 V to 60 V, T_j = -40°C to + 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Charge pump 1							
Charge pump 1 frequency	f_{CP1}	225	250	275	kHz	–	P_GEN_03_01
Output voltage (13 V < VSM < 60 V): CP1 vs. GND	V_{CP1}	16	18	19.5	V	13 V < V_{SM} < 60 V, I_{CP1} = 19.1 mA, I_{CP2} = 19.1 mA, BD_EN = 1b -40°C ≤ T_j ≤ 150°C	P_GEN_03_02

(table continues...)

Table 8 (continued) Charge pumps

V_{SM} = 8.0 V to 60 V, T_j = -40°C to + 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage HT (13 V < VSM < 60 V): CP1 vs. GND	V_{CP1}	14	16.5	19	V	13 V < V_{SM} < 60 V, I_{CP1} = 19.1 mA, I_{CP2} = 19.1 mA, BD_EN = 1b 150°C < T_j ≤ 175°C	P_GEN_03_03
Output voltage (VSM = 8 V): CP1 vs. GND	V_{CP1}	11	12.5	14	V	V_{SM} = 8 V, I_{CP1} = 5.6 mA, I_{CP2} = 5.6 mA, CPEN = 1b, BD_EN = 1b -40°C ≤ T_j ≤ 150°C	P_GEN_03_08
Output voltage HT (VSM = 8V): CP1 vs. GND	V_{CP1}	10.7	11.5	12.5	V	V_{SM} = 8 V, I_{CP1} = 5.6 mA, I_{CP2} = 5.6 mA, BD_EN = 1b 150°C < T_j ≤ 175°C	P_GEN_03_09
CP1 blanking time	t_{BLK_VCP1}	400	500	600	µs	8.0 V < V_{SM} < 60 V, C_{VCP1}= 1 µF, C_{CP1} = 470 nF, I_{CP1} = 0 [1)]	P_GEN_03_10
Rise time of CP1	t_{RISE_VCP1}	–	105	300	µs	8.0 V < V_{SM} < 60 V (25% to 75%), C_{CP1} = 470 nF, I_{CP1} = 0 [1)]	P_GEN_03_11
Charge pump 1 undervoltage threshold	V_{CP1UV}	9.0	10.0	12.0	V	–	P_GEN_03_12
Charge pump 1 undervoltage filter time	t_{CP1UV}	51	64	77	µs	–	P_GEN_03_13
Charge pump 2							
Charge pump 2 frequency	f_{CP2}	225	250	275	kHz	–	P_GEN_03_14
Output voltage (13 V < VSM < 60 V): CP2 vs. VSM	V_{CP2}	11.5	13.5	15.5	V	13 V < V_{SM} < 60 V, I_{CP1} = 19.1 mA, I_{CP2} = 19.1 mA, BD_EN = 1b -40°C ≤ T_j ≤ 150°C	P_GEN_03_15
Output voltage HT (13 V < VSM < 60 V): CP2 vs. VSM	V_{CP2}	10.5	12.5	14	V	13 V < V_{SM} < 60 V, I_{CP1} = 19.1 mA, I_{CP2} = 19,1 mA, BD_EN = 1b 150°C < T_j ≤ 175°C	P_GEN_03_16

(table continues...)

Table 8 (continued) Charge pumps

V_{SM} = 8.0 V to 60 V, T_j = -40°C to + 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage (VSM = 8 V): CP2 vs. VSM	V_{CP2}	8	9.2	10	–	V_{SM} = 8 V, I_{CP1} = 5.6 mA, I_{CP2} = 5.6 mA, CPEN = 1b, BD_EN = 1b -40°C ≤ T_j ≤ 150°C	P_GEN_03_21
Output voltage HT (VSM = 8 V): CP2 vs. VSM	V_{CP2}	7.0	7.5	9.0	–	V_{SM} = 8 V, I_{CP1} = 5.6 mA, I_{CP2} = 5.6 mA, CPEN = 1b, BD_EN = 1b 150°C < T_j ≤ 175°C	P_GEN_03_22
Turn-on time of CP2	t_{ON_VCP2}	–	450	600	µs	8.0 V < V_{SM} < 60 V (25%), C_{CP2} = 220 nF, I_{CP2} = 0 [1)] Typ. value at 48V	P_GEN_03_23
Rise time of CP2	t_{RISE_VCP2}	–	150	350	µs	8.0 V < V_{SM} < 60 V (25% to 75%), C_{CP2} = 220 nF, I_{CP2} = 0 [1)]	P_GEN_03_24
CP2 blanking time	t_{BLK_VCP2}	720	900	1080	µs	8.0 V < V_{SM} < 60 V, C_{VCP2}= 470 nF, C_{CP2} = 220 nF, I_{CP1} = 0 [1)]	P_GEN_03_25
Charge pump 2 undervoltage	V_{CP2UV}	6	7	8	V	–	P_GEN_03_26
Charge pump 2 undervoltage filter time	t_{CP2UV}	51	64	77	µs	–	P_GEN_03_27

1) Parameter dependent on the capacitance.

5 Protections and diagnostics

This device provides protection and monitoring functions. All detected errors will be sent back to the general microcontroller or the MOTIX™ MCU via SPI.

5.1 Reverse polarity protection

Although reverse polarity protection is 48 V standard, it could be required by the applications. In case it is required, the following structures can be used:

- For 48 V applications, a simple reverse polarity protection including one diode and one resistor can also be used. Refer to Figure 5
- The output of the charge pump 2 (CP2) can be used to supply an external n-channel MOSFET, building an active reverse polarity protection. Refer to Figure 6

For 24 V applications the solution in Figure 5 is not recommended due to the voltage drop of the resistance.

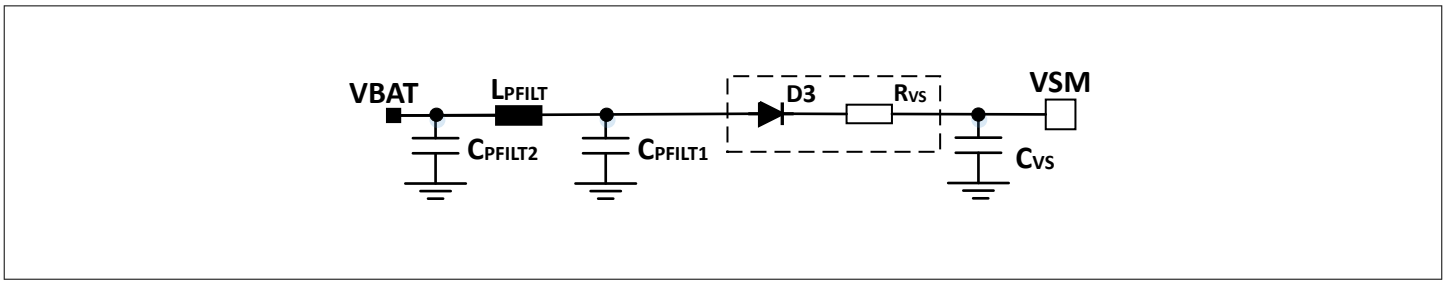

Figure 5 Reverse polarity for 48 V applications

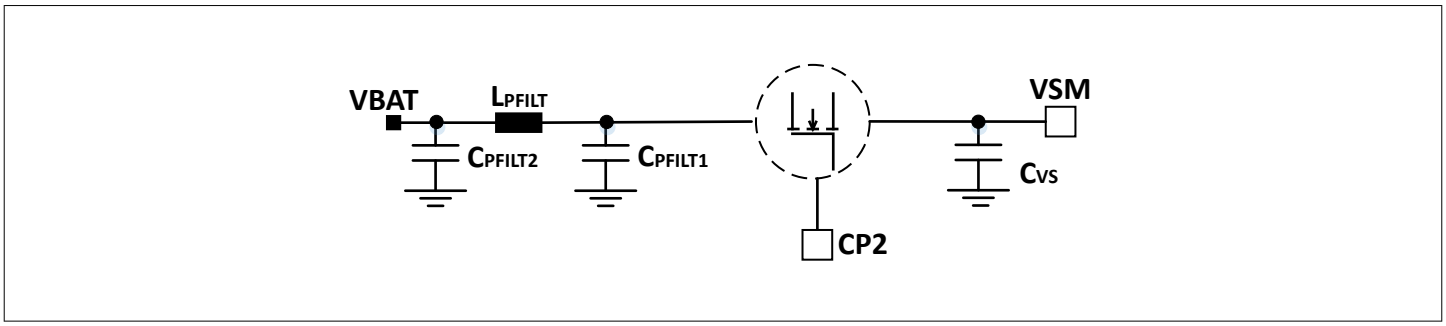

Figure 6 Reverse polarity

5.2 Drain-source voltage monitoring

MOSFETs are protected by V_{DS} monitoring from a short circuit respectively to ground and to battery during on-state:

- HSxDSOV is set to high if the voltage difference between DH and SHMx exceeds the threshold voltage configured by VDSTH (see Table 9)
- LSxDSOV is set to high if the voltage difference between SHMx and SL exceeds the threshold voltage configured by VDSTH (see Table 9)

If a drain-source overvoltage is detected by a voltage comparator when HSLSOV_DIS = 1, the following actions will be performed:

- The gate driver discharge the gate capacitance of the corresponding half-bridge with configured discharge current IDISCHG_ST during TCCP
- The gate capacitance is discharged by IHOLD after TCCP
- The corresponding half bridge will be latched off
- The corresponding bit (LSxDSOV/HSxDSOV) in STAT2 is set

- The DSOV bit in STAT and Global status byte is set
- The error signal (GEF) will be sent back to the general microcontroller or the MOTIX™ MCUhttps://www.infineon.com/cms/en/product/microcontroller/embedded-power-ics-system-on-chip-/3-phase-bridge-driver-integrated-arm-cortex-m3/via the SPI

If a drain-source overvoltage is detected by a voltage comparator when HSLSOV_DIS = 0, the following actions will be performed:

- The gate driver discharge the gate capacitance of the all half-bridges with configured discharge current IDISCHG_ST during TCCP
- The gate capacitance is discharged by IHOLD after TCCP
- All half bridge will be latched off
- The corresponding bit (LSxDSOV/HSxDSOV) in STAT2 is set
- The DSOV bit in STAT and Global status byte is set
- The error signal (GEF) will be sent back to the general microcontroller or the MOTIX™ MCU via the SPI

The device reports a drain-source voltage error if both conditions are met:

- After expiration of the blank time
- Drain-source voltage exceeds the configured threshold for a duration longer than the configured filter time

Table 9 Drain-source overvoltage threshold

HBxVDSTH[2:0]	Drain-source overvoltage threshold
000_B	145 mV
001_B	195 mV (default)
010_B	245 mV
011_B	295 mV
100_B	390 mV
101_B	490 mV
110_B	590 mV
111_B	2 V

The gate drive resume normal operation once the corresponding bit in STAT2 is cleared by the microcontroller.

5.3 Overtemperature protection

If the temperature sensor reaches T_{jW} and the TWDIS is set to 0, then TW bit in STAT1, TE bit in STAT and Global status byte will be set and latched.

The outputs stages however remain activated. Refer to Figure 7.

The TW bit is reset by clearing STAT1 if the thermal warning condition has disappeared.

If the temperature sensor reaches T_{jSD}, the device behaves as follows:

- Discharge the gate capacitances of the MOSFETs with configured discharge current IDISCHG_ST
- All gate drivers are latched off
- Deactivate the charge pump
- Set TSD bit in STAT1
- Set TE bit in STAT and Global status byte

All outputs remain deactivated until the temperature shutdown condition has disappeared and STAT1 is cleared. See Figure 7.

To resume normal functionality of the gate drivers, the following conditions need to be met:

- The temperature shutdown condition has disappeared

- The the general microcontroller or the MOTIX™ MCU clears TSD bit in STAT1
- The charge pump blanking time t_{BLK_VCPX} and the gate driver filter time t_{GD_filt} expire

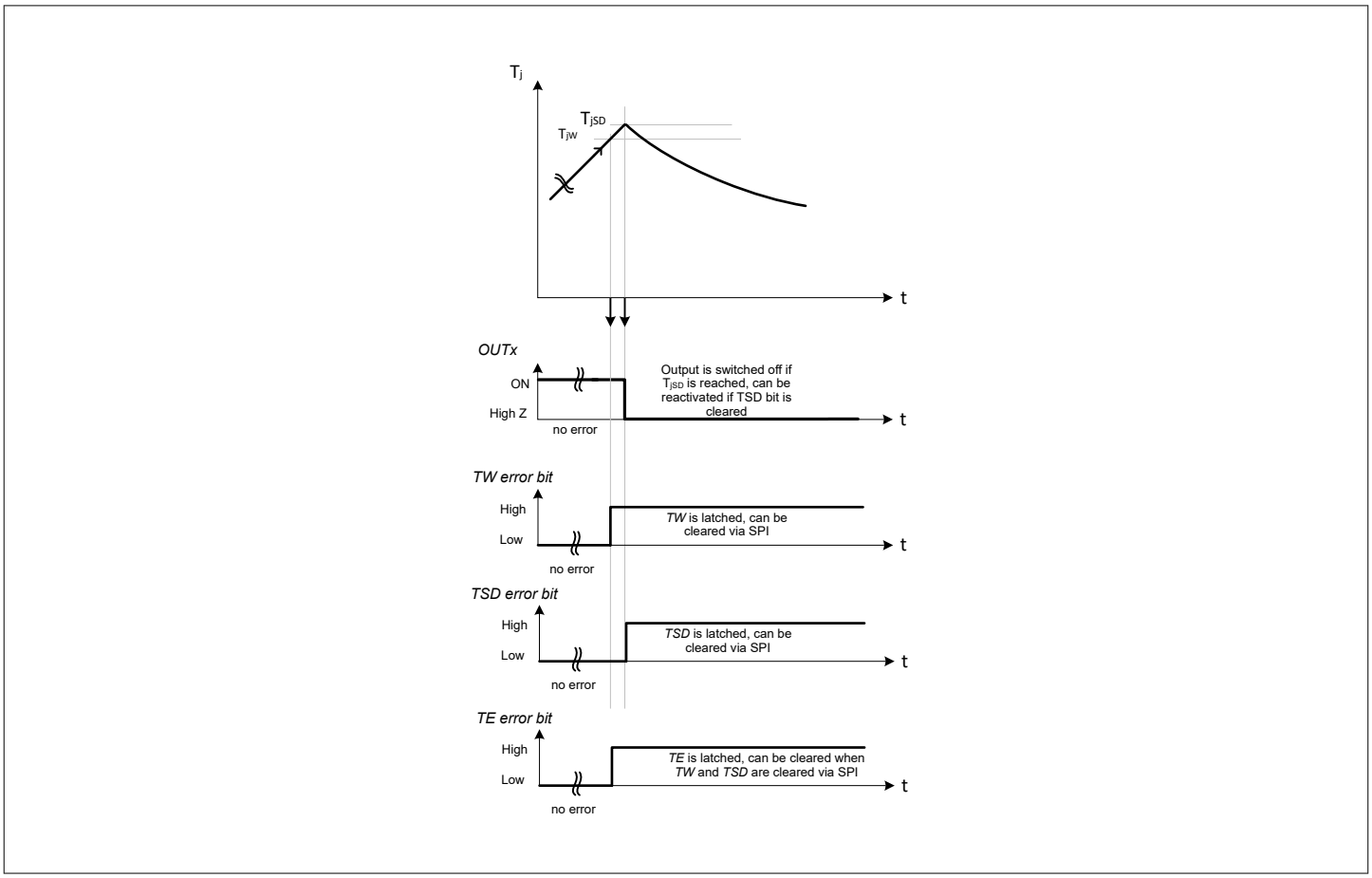

Figure 7 Overtemperature behavior

5.4 Input error

The MOSFETs are protected by input monitoring. When both IHx and ILx of the same bridge are set to high at the same time:

- All external MOSFETs are actively discharged for the duration TCCP
- All external MOSFETs are discharged by IHOLD after TCCP
- INEx bits in STAT3, STAT and Global status byte are set and latched

The gate drivers resume normal operation once the input error disappears and the INEx bits are reset by clearing STAT3.

The INE bit is reset by clearing STAT3.

5.5 Off-state diagnostic

In order to support the off-state diagnostic, the gate driver of each MOSFET provides pull-up and pull-down currents at the SHx pins.

The pull-up current sources are always active when BD_EN = 1 and CPEN = 1 in normal operation mode.

The pull-down currents of each gate driver are activated by the control bits HBxIDIAG in GENCTRL3. During the off-state diagnostic routine performed by the general microcontroller or the MOTIX™ MCU, the drain-source overvoltage threshold of the relevant half-bridges must be set to 2 V nominal. Refer to Table 9. Once the routine is finished, it is highly recommended to decrease the drain-source overvoltage threshold to a lower value, to have a proper VDS monitoring threshold and avoid additional current consumption from the VSM input.

The corresponding HBxVOUT bit in STAT3 is set if any of the following failures are detected:

- MOSFET short circuit to GND
- MOSFET short circuit the battery
- Open load (disconnected motor)

In normal operation mode the status of the output voltage SHx can be read back with status bit HBxVOUT in STAT3 when BD_EN = 1, CPEN = 1 and the corresponding half-bridge is in off-state ((IHx, ILx) = (0, 0))

Note: HBxVOUT = 0 if the half-bridge x is not in off-state ((IHx, ILx) = (1, 0) or (0, 1)). INE is reported if ((IHx, ILx) = (1, 1)).

5.6 Timeout watchdog

An integrated timeout watchdog supervises the integrity of the communication with the general microcontroller or the MOTIX™ MCU. The watchdog period is programmable by setting the WDPER bits in GENCTRL2 in the range of 2 ms to 512 ms.

After a power-on-reset, if the watchdog is not retriggered by receiving a valid SPI-write command to the watchdog configuration register (GENCTRL2) from the general microcontroller or the MOTIX™ MCU in the programmable watchdog period in GENCTRL2, the device will:

- Set and latch the ST bit in STAT and Global status byte
- Reset the control registers to their default values
- Actively switch off all external MOSFETs with IDISCHG_ST
- Enter the stop mode

The device resumes normal operation, if the general microcontroller or the MOTIX™ MCU device:

1. Clears the ST bit in STAT when the device is in stop mode
2. Sends watchdog pattern with correct CHECKSUM bit in normal mode

A checksum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting. The sum of the 8 data bits 7:0 in the register GENCTRL2 needs to have even parity. This is realized by either setting the bit CHECKSUM to 0 or 1. The checksum is calculated by taking all 8 data bits into account. The written value of the reserved bits of the register is also considered (even if read as 0 in the SPI output) for checksum calculation, that is if a 1 is written on the reserved bit position, then a 1 is used in the checksum calculation.

The SPI command is ignored and SPIE bit is set and latched in STAT and Global status byte, if the a watchdog trigger with an incorrect CHECKSUM is sent.

CHECKSUM = Bit7⊕...⊕Bit0

During normal operation the status bits WDMON[1:0] in STAT2 report the relative position of the watchdog timer to the watchdog period. Refer to Table 10 and Figure 8.

This allows the detection of a potential latent failure associated to the watchdog timer: the general microcontroller or the MOTIX™ MCU can indeed verify that the watchdog timer is running.

Table 10 Watchdog monitoring

WDMON[1:0]	Position of the watchdog timer
00_B	Watchdog timer is between [0%, 25%] of the watchdog period
01_B	Watchdog timer is between [25%, 50%] of the watchdog period
10_B	Watchdog timer is between [50%, 75%] of the watchdog period
11_B	Watchdog timer is between [75%, 100%] of the watchdog period

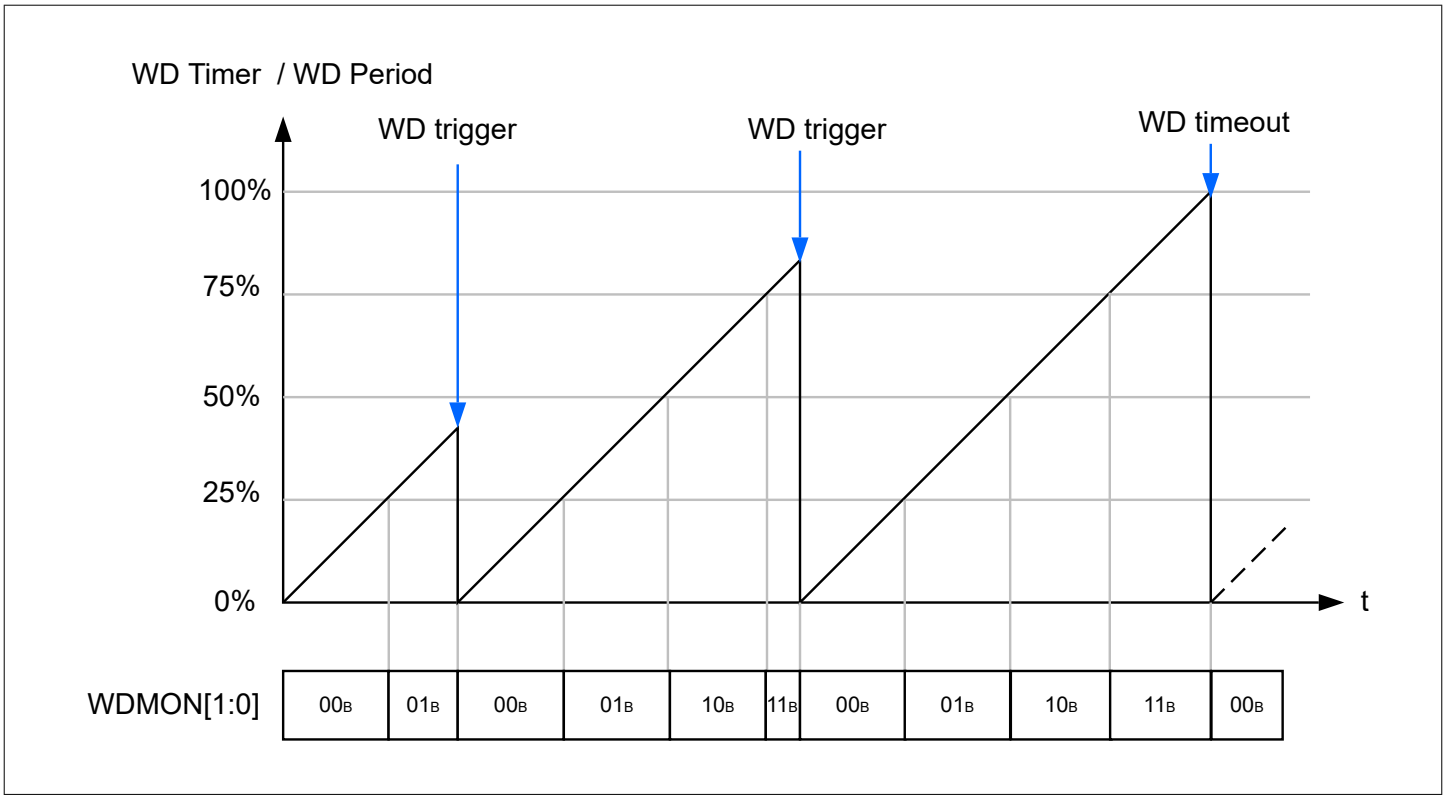

Figure 8 Example of watchdog monitoring and watchdog timeout

The watchdog is enabled by default.

It can be disabled only if the following SPI sequence is sent:

1. First frame: Set UNLOCK bit in GENCTRL1 to 1
   Note: UNLOCK is automatically reset to 0 at the end of the next frame.
2. Following frame: Set WDDIS bit in GENCTRL3 to 1

The watchdog is directly re-enabled by setting WDDIS to 0.

5.7 Cross-current protection and drain-source overvoltage blank time

All gate drivers feature a cross-current protection time and a drain-source overvoltage blank time. The cross-current protection avoids the simultaneous activation of the high-side and the low-side MOSFETs of the same half-bridge.

During the blank time, the drain-source overvoltage detection is disabled, to avoid a wrong fault detection during the activation phase of a MOSFET.

5.7.1 Cross-current protection

If IHx/ILx is set to high in the duration of the other input's TCCP, to avoid the cross current the device will:

- Switch on the corresponding MOSFET with a delay defined by cross-current protection time in GENCTRL12
- Discharge the other MOSFET in the same half bridge actively for a duration defined by the remaining cross-current protection time

Table 11 Cross-current protection time

TCCP[2:0]	Cross-current protection time t_{CCPx} (typical)
000_B	0.5 µs
001_B	1.0 µs

(table continues...)

Table 11 (continued) Cross-current protection time

TCCP[2:0]	Cross-current protection time t_{CCPx} (typical)
010_B	1.5 µs
011_B	2.0 µs
100_B	2.5 µs
101_B	3.0 µs
110_B	3.5 µs
111_B	4.0 µs

5.7.2 Drain-source overvoltage blank time

When the MOSFETs are switched on, after the expiration of the cross-current protection time, a drain-source overvoltage error will be masked during the blank time defined in GENCTRL12 for the drain-source monitoring.

Table 12 Drain-source overvoltage blank time

TBLK[2:0]	Drain-source overvoltage blank time t_{BLANKx} (nominal)
000_B	0.5 µs
001_B	1.0 µs
010_B	1.5 µs
011_B	2.0 µs
100_B	2.5 µs
101_B	3.0 µs
110_B	3.5 µs
111_B	4.0 µs

5.8 Overvoltage and undervoltage shutdown

5.8.1 VSM undervoltage

If VSM drops below V_{SMUV_OFFx} and VDD > V_{DD_POR}, the device will:

- Switch off the external MOSFETs actively for the duration TCCP with the discharge current corresponding to the settings of IDISCHG_ST
- Deactivate the charge pumps
- Activate passive discharge after TCCP
- Set and latch VSMUV bit in STAT1
- Set and latch SUPE bit in STAT and Global status byte
- Keep logic information

If VSM rises above V_{SMUV_ONx} as shown in Figure 9, after clearing the VSMUV bit the device resumes normal operation when t_{BLK_VCPX} and t_{GD_filt} expire.

The SUPE is reset if the following conditions are fulfilled:

- VSM > V_{SMUV_ONx} (see Figure 9)
- The device receives a clear command to STAT1

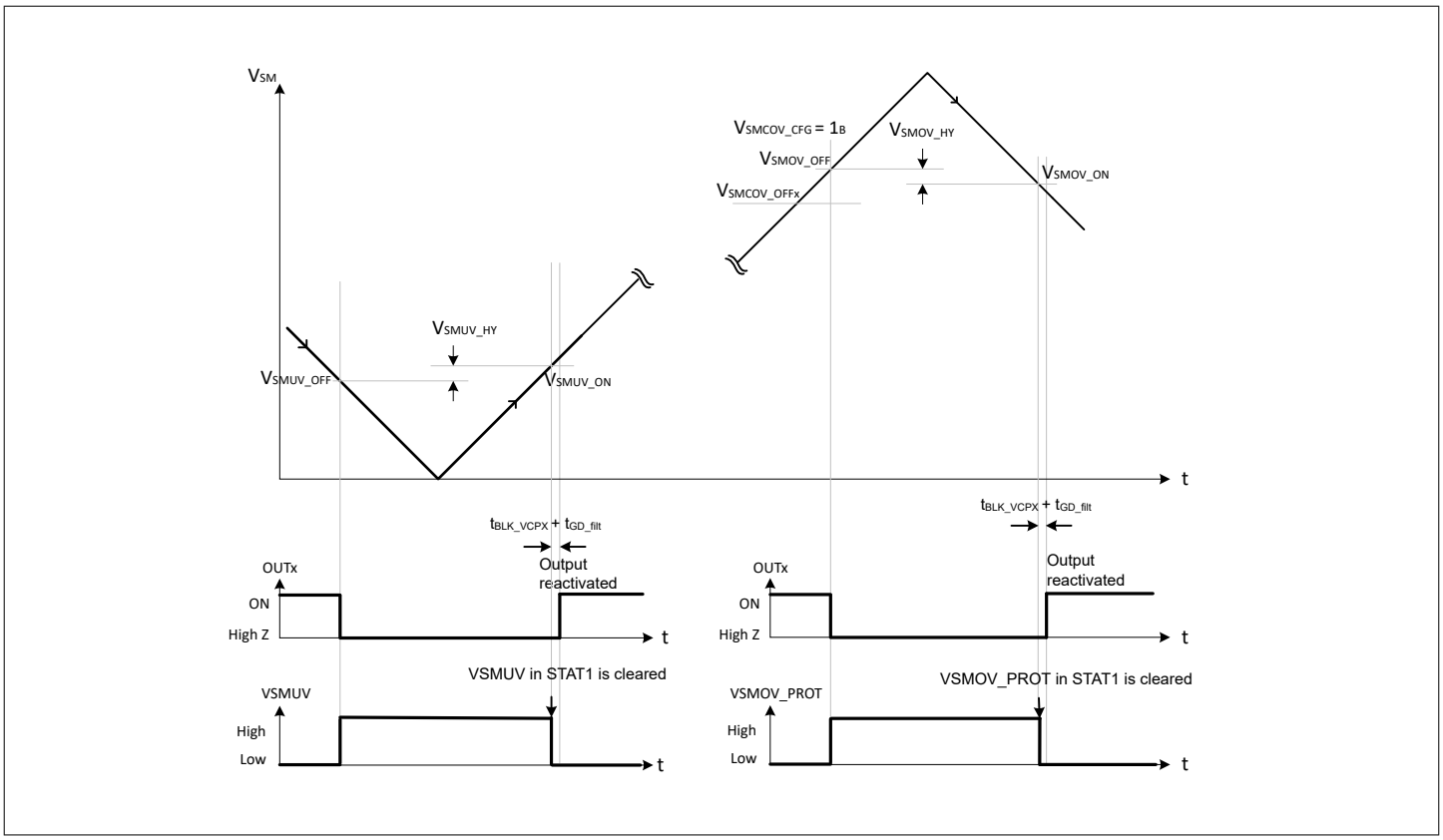

Figure 9 VSM monitoring

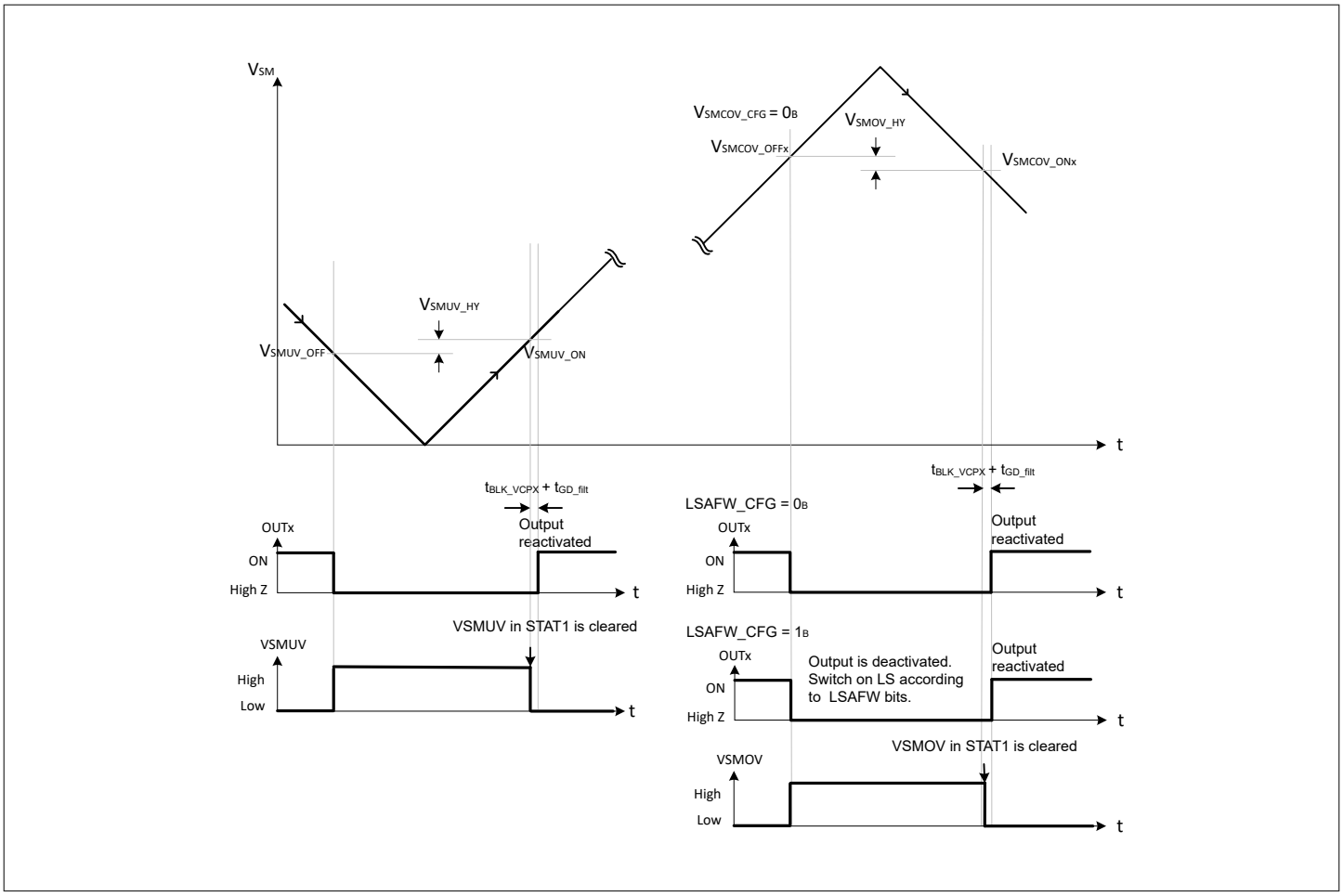

Figure 10 Configurable VSM monitoring

5.8.2 VSM overvoltage

If VSM rises above V_{SMOV_OFF}, VDD > V_{DD_POR}, the device will:

- Switch off the external MOSFETs actively for the duration TCCP with the discharge current corresponding to the settings of IDISCHG_ST
- Deactivate the charge pumps
- Activate passive discharge after TCCP
- Set and latch VSMOV_PROT bit in STAT1
- Set and latch SUPE bit in STAT and Global status byte
- Keep logic information

A configurable overvoltage threshold below V_{SMCOV_OFFx} can be selected by set VSM_COVUVTH bit in GENCTRL13.

When the conditions below are met:

- VSMOV_CFG is set to 0_B
- VSM rises above the selected V_{SMCOV_OFFx}
- VDD > V_{DD_POR}
- LSAFW_CFG = 0_B

The device will:

- Switch off the external MOSFETs actively for the duration TCCP with the discharge current corresponding to the settings of IDISCHG_ST
- Deactivate the charge pumps
- Activate passive discharge after TCCP

- Set and latch VSMOV bit in STAT1
- Set and latch SUPE bit in STAT and Global status byte
- Keep logic information

When the conditions below are met:

- VSMOV_CFG is set to 0_B
- VSM rises above the selected V_{SMCOV_OFFx}
- VDD > V_{DD_POR}
- LSAFW_CFG = 1_B

The device will:

- Set and latch VSMOV bit in STAT1
- Set and latch SUPE bit in STAT and Global status byte
- Switch off the external high-side MOSFETs actively for the duration TCCP
- Switch on the corresponding low-side MOSFET based on the LSAFW bits in GENCTRL13
- Switch on all low-side MOSFETs if LSAFW = 00_B (the one was in on-state will be kept switched on)
- The low-side MOSFETs will be latched on till the VSMOV bit is cleared
- Keep charge pumps activated with auto-recovery
- Ignore CPREC bit
- Keep logic information

Note: The low-side MOSFETs are switched on based on the same sequence for normal switching on.

When the conditions below are met:

- VSMOV_CFG is set to 1_B
- VSM rises above the selected V_{SMCOV_OFFx}
- VDD > V_{DD_POR}

The device will:

- Ignore the configurable overvoltage event
- Not set the VSMOV bit in STAT1
- Not set SUPE bit in STAT and Global status byte
- Keep charge pumps activated
- Keep logic information

If VSM drops below V_{SMOV_ON} / V_{SMCOV_ONx} as shown in Figure 9 and Figure 10, after clearing VSMOV _PROT bit and VSMOV bit the device will resume normal operation when t_{BLK_VCPX} nd t_{GD_filt} expires.

The SUPE is reset if the following conditions are fulfilled:

- VSM < V_{SMOV_ON} or VSM < V_{SMCOV_ONx} when VSMOV_CFG is 0_B (see Figure 9 and Figure 10)
- The device receives a clear command to STAT1

5.8.3 VDD undervoltage protection

If the VDD logic supply drops below the undervoltage threshold V_{DD_POFFR} (power off reset), the device behaves as follows:

- Deactivate the SPI interface
- Reset the digital block
- Switch off the gate driver
- Activate the passive discharge path for the external MOSFETs
- Switch off the charge pump

5.8.4 Charge pump undervoltage

The voltage of the buck/boost charge pump output (CP1) is monitored in order to ensure a correct control of the external MOSFETs.

If CP1 falls below the configured charge pump undervoltage threshold V_{CP1UV}, the device will:

- Discharge the external MOSFETs actively with IDISCHG_ST for the duration TCCP
- Turn-off the gate drivers
- Activate the passive discharge path
- Set and latch CP1UV bit in STAT1
- Set and latch SUPE bit in STAT and Global status byte

Note: The charge pump undervoltage event is ignored during blanking time, and will be reported after filter time as shown in Figure 11.

If STAT1 is cleared when VCP1 > VCP1UV, the device resets the SUPE bit and resumes normal operation after the charge pump blanking time and the filter time.

Note: CPREC setting bit is ignored for charge pump undervoltage event. It is only related to the VSM undervoltage and VSM overvoltage events.

The voltage of the charge pump output (CP2) is monitored in order to ensure a correct control of the external MOSFETs.

If CP2 falls below the configured charge pump undervoltage threshold V_{CP2UV}, the device will:

- Discharge the external MOSFETs actively with IDISCHG_ST for the duration TCCP
- Turn-off the gate drivers
- Activate the passive turn-off path
- Set and latch CP2UV bit in STAT1
- Set and latch SUPE bit in STAT and Global status byte

Note: The charge pump undervoltage event is ignored during blanking time, and will be reported after filter time as shown in Figure 11.

If STAT1 is cleared when VCP2 > VCP2UV, after charge pump blanking time and the filter time the device resumes normal operation and resets the SUPE bit.

Note: CPREC setting bit is ignored for the charge pump undervoltage event. It is only related to the VSM undervoltage and VSM overvoltage events.

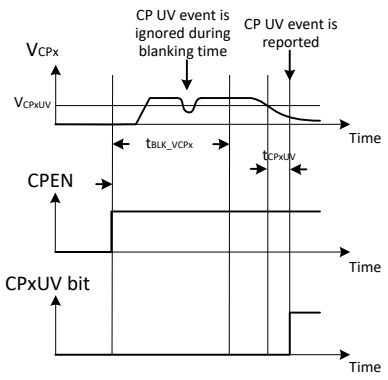

Figure 11 Charge pump undervoltage event

5.9 Electrical characteristics protection and diagnosis

Table 13 Electrical characteristics

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Watchdog							
Watchdog period	t_{WDPER}	–	2 4 8 16 64 128 256 512	–	ms	WDPER[2:0] = 000_B WDPER[2:0] = 001_B WDPER[2:0] = 010_B WDPER[2:0] = 011_B WDPER[2:0] = 100_B WDPER[2:0] = 101_B WDPER[2:0] = 110_B WDPER[2:0] = 111_B	P_PRO_01_01
Watchdog period accuracy	t_{WDPER_ACC}	-10	–	+10	%	–	P_PRO_01_02
Filter time to avoid false VDS error during recovery from the errors							
Gate driver filter time	t_{GD_filt}	60	72	86	µs	–	P_PRO_01_03
Off-state open load diagnosis							
Pull-up diagnosis current	I_{PUDiag}	-0.9	-2	-3.0	mA	8 V ≤ HBOUTx ≤ 60 V HBOUTx = VBAT	P_PRO_01_04
Pull-down diagnosis current	I_{PDDiag}	4.5	7	10.5	mA	8 V ≤ HBOUTx ≤ 60 V HBOUTx = VBAT	P_PRO_01_05
Pull-down pull-up diagnosis current ratio	IPDDiag / IPUDiag	2.7	–	–	–	–	P_PRO_01_06
Drain-source monitoring threshold							
Drain-source monitoring threshold	$V_{VDSMONTHx}$	–	0.145 0.195 0.245 0.295 0.39 0.49 0.59 2	–	V	HBxVDSTH[2:0] = 000_B HBxVDSTH[2:0] = 001_B HBxVDSTH[2:0] = 010_B HBxVDSTH[2:0] = 011_B HBxVDSTH[2:0] = 100_B HBxVDSTH[2:0] = 101_B HBxVDSTH[2:0] = 110_B HBxVDSTH[2:0] = 111_B	P_PRO_01_07

(table continues...)

Table 13 (continued) Electrical characteristics

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drain-source monitoring threshold accuracy low	$V_{VDSMONTH\_ACC1}$	-30	–	+30	%	VDSTH[2:0] = 000_B	P_PRO_01_08
Drain-source monitoring threshold accuracy high	$V_{VDSMONTH\_ACC2}$	-20	–	+20	%	VDSTH[2:0] = 001_B VDSTH[2:0] = 010_B VDSTH[2:0] = 011_B VDSTH[2:0] = 100_B VDSTH[2:0] = 101_B VDSTH[2:0] = 110_B VDSTH[2:0] = 111_B	P_PRO_01_09
Drain-source monitoring filter time							
VDS monitoring filter time	t_{DSMON_FILT}	–	0.25 0.50 0.75 1.00 1.25 1.50 1.75 2.00	–	µs	TFVDS[2:0] = 000_B TFVDS[2:0] = 001_B TFVDS[2:0] = 010_B TFVDS[2:0] = 011_B TFVDS[2:0] = 100_B TFVDS[2:0] = 101_B TFVDS[2:0] = 110_B TFVDS[2:0] = 111_B	P_PRO_01_10
VDS monitoring filter time accuracy	$t_{DSMONFILT\_ACC}$	-10	–	+10	%	–	P_PRO_01_11
Drain-source monitoring blank time							
Drain-source monitoring blank time	t_{DSMON_BLK}	–	0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0	–	µs	TBLK[2:0] = 000_B TBLK[2:0] = 001_B TBLK[2:0] = 010_B TBLK[2:0] = 011_B TBLK[2:0] = 100_B TBLK[2:0] = 101_B TBLK[2:0] = 110_B TBLK[2:0] = 111_B	P_PRO_01_12
Drain-source monitoring blank time accuracy	$t_{DSMONBLK\_ACC}$	-10	–	+10	%	–	P_PRO_01_13

(table continues...)

Table 13 (continued) Electrical characteristics

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cross current protection							
Cross current protection time	$t_{HBxCCPx}$	–	0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0	–	µs	TCCP[2:0] = 000_B TCCP[2:0] = 001_B TCCP[2:0] = 010_B TCCP[2:0] = 011_B TCCP[2:0] = 100_B TCCP[2:0] = 101_B TCCP[2:0] = 110_B TCCP[2:0] = 111_B	P_PRO_01_14
Cross current protection time accuracy	$t_{HBxCCPx\_ACC}$	-10	–	+10	%	–	P_PRO_01_15
Thermal warning and shutdown							
Thermal warning junction temperature	T_{jW}	156	170	185	°C	–	P_PRO_01_16
Thermal shutdown junction temperature	T_{jSD}	196	210	225	°C	–	P_PRO_01_17
Thermal shutdown hysteresis	T_{jHYS}	5	10	–	°C	–	P_PRO_01_18

6 Gate driver

6.1 Gate driver control

The device integrates six floating gate drivers capable of controlling a wide range of N-channel MOSFETs. They are configured as three high-sides and three low-sides, building for 3-phase BLDC.

The MOSFETs can be:

- Deactivated with BD_EN = 0
- Activated in PWM mode with BD_EN = 1 and CPEN = 1

The MOSFETs are controlled as shown in Figure 12, Figure 13, Figure 14 and Figure 15.

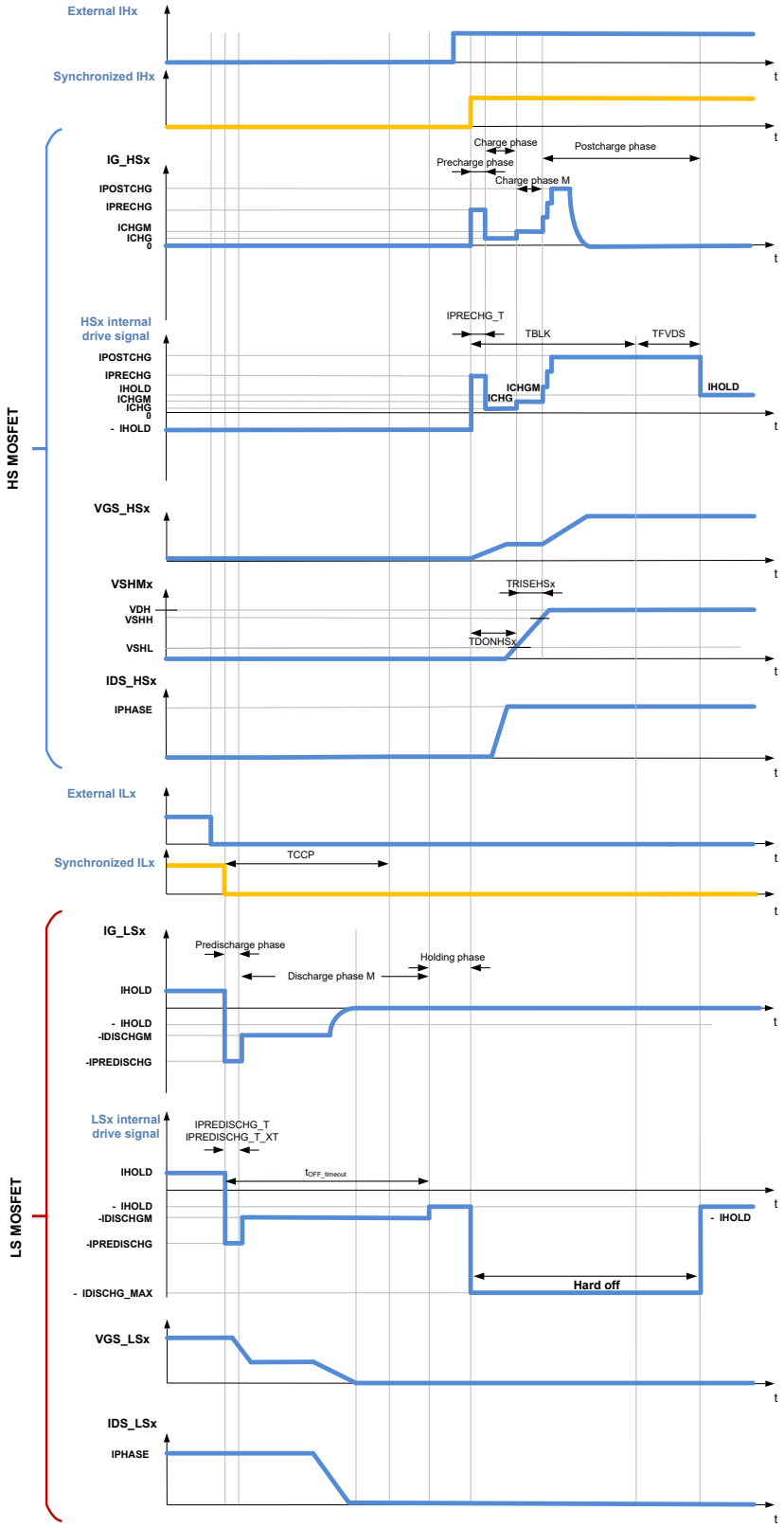

Figure 12 Turn-on of the high-side MOSFET

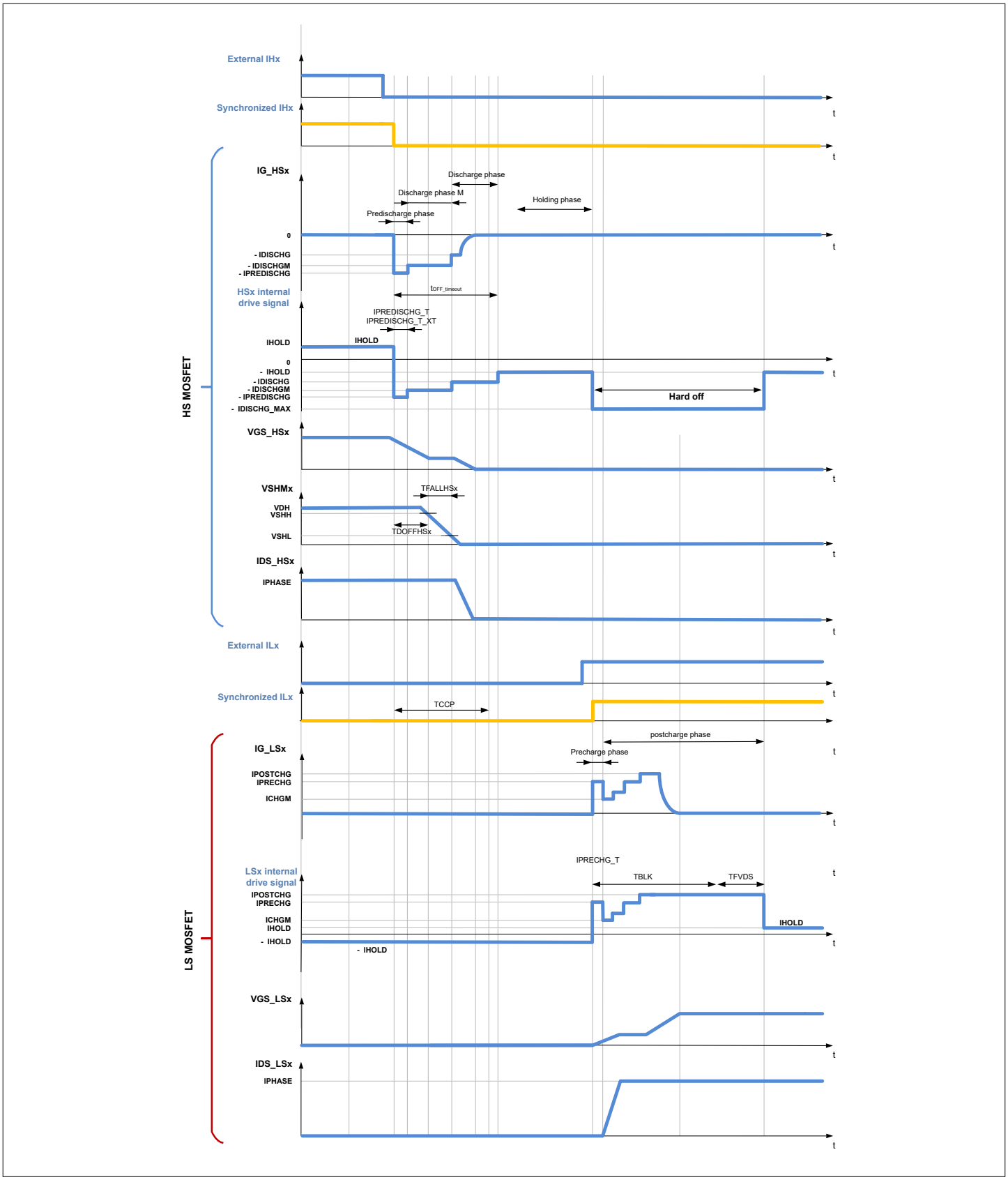

Figure 13 Turn-off of the high-side MOSFET

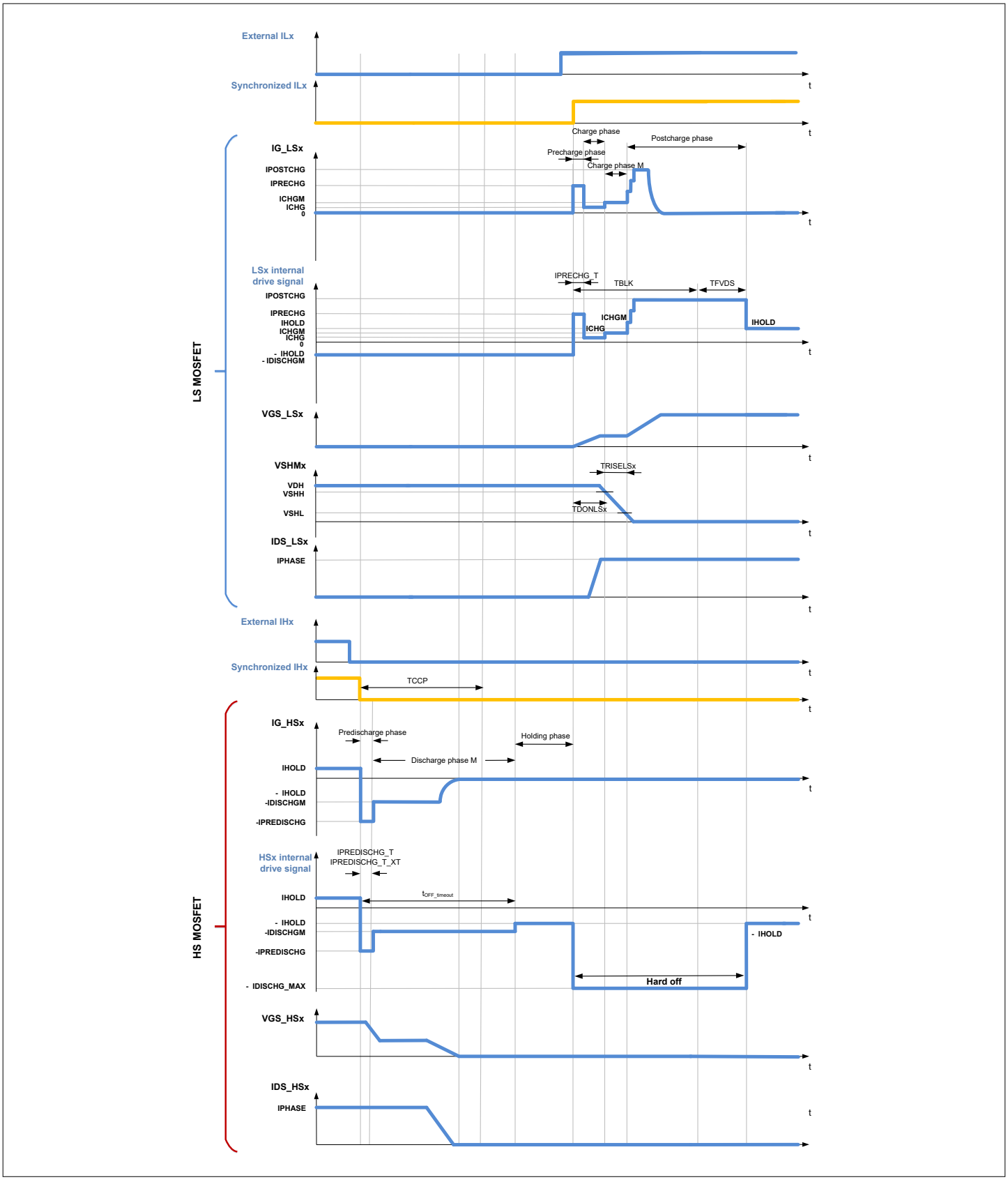

Figure 14 Turn-on of the low-side MOSFET

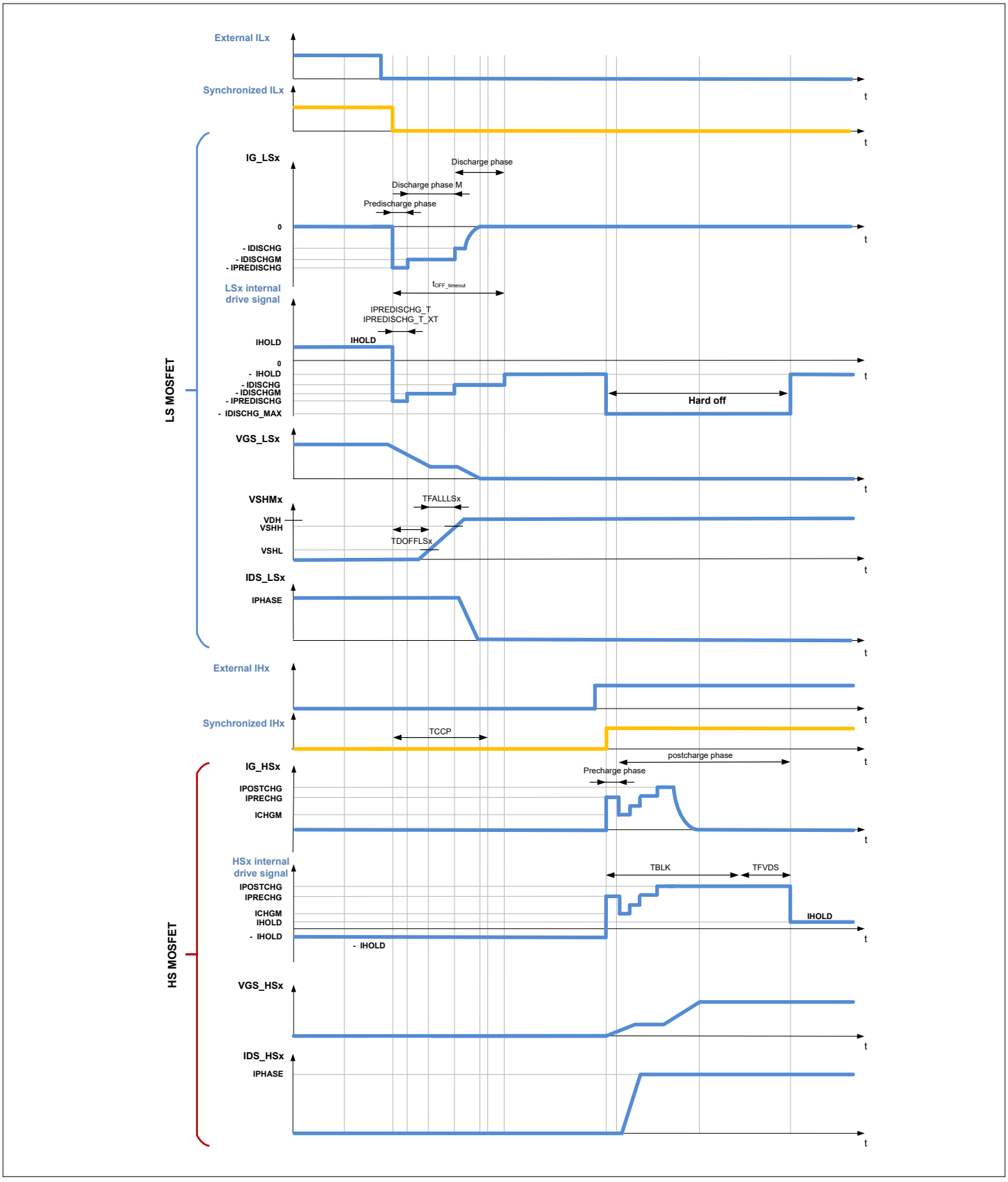

Figure 15 Turn-off of the low-side MOSFET

The turn-on of the high-side MOSFET is done in five phases (refer to Figure 12):

1. **Cross-current protection phase:** the cross-current protection time TCCP starts at the falling edge of ILx. During TCCP, the low-side MOSFET is turned off while the high-side is kept off with IHOLD. Only after TCCP IHx is allowed to set to high. The low-side will be kept off with hard off current until TFVDS has elapsed
2. **Pre-charge phase:** once the TCCP has elapsed and IHx is set to high, the gate of the high-side MOSFET is pre-charged with the current IPRECHG for a duration IPRECHG_T. When IPRECHG_T expires it will jump to charge phase
3. **Charge phase:** after the pre-charge phase the charge current is decreased from IPRECHG down to ICHG. The gate of the high-side MOSFET will be charged with ICHG until VSHMx reaches GND + 2 V. If VSHMx reaches VDH - 2 V during the charge phase, it will jump to post-charge phase
4. **Middle-charge phase:** after the charge phase the gate of the high-side MOSFET will be charged with ICHGM until VSHMx reaches VDH - 2 V
5. **Post-charge phase**: after the middle-charge phase the control signal for the charge current is set to IPOSTCHG until the end of TFVDS. If the device is still in the ramping phase of the post-charge current when TFVDS has expired, the ramp phase will be extended until it reaches IPOSTCHG. After TFVDS expires and IPOSTCHG is reached, the charge current will be switched to IHOLD

Cross-current protection time TCCP represents the time after which the complementary transistor in the same half-bridge can be activated. Therefore TCCP is the minimum discharge phase for the MOSFET. $t_{OFF\_timeout}$ is the maximum time for discharge.

The turn-off of the high-side MOSFET is done in four phases (refer to Figure 13):

1. **Pre-discharge phase:** once IHx is set to low, the gate of the high-side MOSFET is pre-discharged with the current IPREDISCHG for a duration based on IPREDISCHG_T and IPREDISCHG_T_XT. It will jump to middle-discharge phase after pre-discharge time expires
2. **Middle-discharge phase:** after the pre-discharge phase the gate current is decreased from IPREDISCHG down to IDISCHGM. The gate of the high-side MOSFET will be discharged with IDISCHGM until VSHMx reaches GND + 2 V
3. **Discharge phase:** after the middle-discharge phase the device will enter discharge phase. The gate of the high-side MOSFET will be discharged with IDISCHG until $t_{OFF\_timeout}$ expires
4. **Holding phase:** after the $t_{OFF\_timeout}$ expires the high-side MOSFET will be kept off with IHOLD

Note: If a INE failure comes, all MOSFETs will be discharged with IDISCHG_ST for a duration of TCCP.

The turn-on of the low-side MOSFET is done in five phases (refer to Figure 14):

1. **Cross-current protection phase:** the cross-current protection time TCCP starts at the falling edge of IHx. During TCCP, the high-side MOSFET is turned off while the low-side is kept off with IHOLD. Only after TCCP ILx is allowed to set to high. The high-side will be kept off with hard off current until TFVDS has elapsed
2. **Pre-charge phase:** once the TCCP has elapsed and ILx is set to high, the gate of the low-side MOSFET is pre-charged with the current IPRECHG for a duration IPRECHG_T. After IPRECHG_T expires, it will jump to charge phase
3. **Charge phase:** after the pre-charge phase the charge current is decreased from IPRECHG down to ICHG. The gate of the low-side MOSFET will be charged with ICHG until VSHMx reaches VDH - 2 V
4. **Middle-charge phase:** after the charge phase the gate of the low-side MOSFET will be charged with ICHGM until VSHx reaches GND + 2V
5. **Post-charge phase**: after the middle-charge phase the control signal for the charge current is set to IPOSTCHG until the end of TFVDS. If the device is still in the ramping phase of the post-charge current when TFVDS has expired, the ramp phase will be extended until it reaches IPOSTCHG. After TFVDS expires and IPOSTCHG is reached, the charge current will be switched to IHOLD

Cross-current protection time TCCP represents the time after which the complementary transistor in the same half-bridge can be activated. Therefore TCCP is the minimum discharge phase for the MOSFET. $t_{OFF\_timeout}$ is the maximum time for discharge.

The turn-off of the low-side MOSFET is done in four phases (refer to Figure 15):

1. **Pre-discharge phase:** once ILx is set to low, the gate of the low-side MOSFET is pre-discharged with the current IPREDISCHG for a duration based on IPREDISCHG_T and IPREDISCHG_T_XT. It will jump to middle-discharge phase after pre-discharge time expires

2. **Middle-discharge phase:** after the pre-discharge phase the discharge current is decreased from IPREDISCHG down to IDISCHGM. The gate of the low-side MOSFET will be discharged with IDISCHGM until VSHMx reaches VDH - 2 V
3. **Discharge phase:** after the middle-discharge phase the gate of the low-side MOSFET will be discharged with IDISCHG until $t_{OFF\_timeout}$ expires
4. **Holding phase:** after the $t_{OFF\_timeout}$ expires the high-side MOSFET will be kept off with IHOLD

Note: If a INE failure comes, all MOSFETs will be discharged with IDISCHG_ST for a duration of TCCP.

High-side MOSFET:

- TDONHSx is counted from the rising edge of the synchronized IHx until VSHMx reaches GND + 2 V
- TRISEHSx is counted from the VSHMx reaching GND + 2 V until it reaches VDH - 2 V
- If VSHMx does not reach GND + 2 V until TBLK is elapsed, 0xFF and 0x00 will be saved in effective high-side MOSFET turn-on delay register and effective high-side MOSFET rise time register respectively
- If VSHMx has reached VDH - 2 V when the rising edge of the synchronized IHx comes, 0x00 will be stored in both the effective high-side MOSFET turn-on delay register and the effective high-side MOSFET rise time register
- If VSHMx reaches GND + 2 V but does not reach VDH -2V when TBLK is elapsed, 0xFF will be saved in the effective high-side MOSFET rise time register
- TDOFFHSx is counted from the falling edge of the synchronized IHx until VSHMx reaches VDH - 2 V
- TFALLHSx is counted from the VSHMx reaching VDH - 2V until it reaches to GND + 2 V
- If VSHMx does not reach VDH - 2 V until TCCP is elapsed, 0xFF and 0x00 will be saved in effective high-side MOSFET turn-off delay register and effective high-side MOSFET fall time register respectively
- If VSHMx has reached GND + 2 V when the falling edge of the synchronized IHx comes, 0x00 will be stored in both the effective high-side MOSFET turn-off delay register and the effective high-side MOSFET fall time register
- If VSHMx reaches VDH - 2 V but does not reach GND + 2 V when TCCP is elapsed, 0xFF will be saved in the effective high-side MOSFET fall time register

Note:

- *If VDH - 2 V > VSHMx > GND + 2 V when the rising edge of the synchronized IHx comes, 0x00 will be saved in effective high-side MOSFET turn-on delay register and the time from the IHx rising edge to VSHMx reaching VDH - 2 V will be saved in the effective high-side MOSFET rise time register*
- *If 0x00 is saved as the turn-on delay time, the rise time TRISEHSx might not reflect the slew rate correctly. It is not recommended to use the TRISEHSx to adjust the switching behavior*
- *If IHx pulse is shorter than TBLK/TCCP, the registers will keep the last value and will not be updated*

Low-side MOSFET:

- TDONLSx is counted from the rising edge of the synchronized ILx until VSHMx reaches VDH - 2 V
- TRISELSx is counted from the VSHMx reaching VDH - 2 V until it reaches GND + 2 V
- If VSHMx does not reach VDH - 2 V until TBLK is elapsed, 0xFF and 0x00 will be saved in effective low-side MOSFET turn-on delay register and effective low-side MOSFET rise time register respectively
- If VSHMx has reached GND + 2 V when the rising edge of the synchronized ILx comes, 0x00 will be stored in both the effective low-side MOSFET turn-on delay register and the effective low-side MOSFET rise time register
- If VSHMx reaches VDH - 2 V but does not reach GND + 2 V when TBLK is elapsed, 0xFF will be saved in the effective low-side MOSFET rise time register
- TDOFFLSx is counted from the falling edge of the synchronized ILx until VSH reaches GND + 2 V
- TFALLLSx is counted from the VSHMx reaching GND + 2 V until it reaches to VDH - 2 V
- If VSHMx does not reach GND + 2 V until TCCP is elapsed, and 0xFF and 0x00 will be saved in effective low-side MOSFET turn-off delay register and effective low-side MOSFET fall time register respectively
- If VSHMx has reached VDH - 2 V when the falling edge of the synchronized ILx comes, 0x00 will be stored in both the effective low-side MOSFET turn-off delay register and the effective low-side MOSFET fall time register
- If VSHMx reaches GND + 2 V but does not reach VDH - 2 V when TCCP is elapsed, 0xFF will be saved in the effective low-side MOSFET fall time register

Note:

- *If VDH - 2 V > VSHMx > GND + 2 V when the rising edge of the synchronized ILx comes, 0x00 will be saved in effective low-side MOSFET turn-on delay register and the time from the ILx rising edge to VSHMx reaching GND + 2 V will be saved in the effective low-side MOSFET rise time register*
- *If 0x00 is saved as the turn-on delay time, the rise time TRISELSx might not reflect the slew rate correctly. It is not recommended to use the TRISELSx to adjust the switching behavior*
- *The values in the registers are invalid if IHx/ILx pulse is active shorter than TBLK or inactive shorter than TCCP*

6.2 Electrical characteristics of gate driver

Table 14 Electrical characteristics gate driver

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High input voltage threshold of ILx, IHx (VDD = 5 V)	V_{IH1_IN}	2.5	–	–	V	VDD = 5 V	P_BDRV_01_01
High input voltage threshold of ILx, IHx (VDD = 3.3 V)	V_{IH2_IN}	1.5	–	–	V	VDD = 3.3 V	P_BDRV_01_02
Low input voltage threshold of ILx, IHx (VDD = 5 V)	V_{IL1_IN}	–	–	0.8	V	VDD = 5 V	P_BDRV_01_03
Low input voltage threshold of ILx, IHx (VDD = 3.3 V)	V_{IL2_IN}	–	–	0.6	V	VDD = 3.3 V	P_BDRV_01_04
Hysteresis of ILx, IHx (VDD = 5 V)	V_{IHY1_IN}	100	400	–	mV	VDD = 5 V	P_BDRV_01_05
Hysteresis of ILx, IHx (VDD = 3.3 V)	V_{IHY2_IN}	100	150	–	mV	VDD = 3.3 V	P_BDRV_01_06
Maximum total charge driver capability	Q_{tot_max}	–	–	1400	nC	Due to charge pump current capability only 6 ∗ MOSFETs + additional external capacitors with a total charge of max. 1400 nC can be driven simultaneous at a PWM frequency of 25 kHz.	P_BDRV_01_07
High level output voltage low: GHMx vs. SHMx	V_{GSHMx}	6.5	–	12.8	V	V_{SM} = 8 V, I_{CP1} = 5.6 mA, I_{CP2} = 5.6 mA, CPEN = 1b, BD_EN = 1b	P_BDRV_01_08
High level output voltage high: GHMx vs. SHMx	V_{GSHMx}	10	11	12.8	V	V_{SM} > 13 V, I_{CP1} = 19.1 mA, I_{CP2} = 19.1 mA, CPEN = 1b, BD_EN = 1b	P_BDRV_01_09

(table continues...)

Table 14 (continued) Electrical characteristics gate driver

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level output voltage low: GLMx vs. SLMx	V_{GSLMx}	8	–	12.8	V	VSM = 8 V, I_{CP1} = 5.6 mA, I_{CP2} = 5.6 mA, CPEN = 1b, BD_EN = 1b	P_BDRV_01_10
High level output voltage high: GLMx vs. SLMx	V_{GSLMx}	10	11	12.8	V	V_{SM} > 13 V, I_{CP1} = 19.1 mA, I_{CP2} = 19.1 mA, CPEN = 1b, BD_EN = 1b	P_BDRV_01_11
Gate driver current turn-on rise time	$t_{GDRV\_RISE(ON)}$	20	75	120	ns	From 20% of ICHG to 80% of ICHG, x = 0 to 63, C_{Load} = 20 nF	P_BDRV_01_12
Gate driver current turn-off rise time	$t_{GDRV\_RISE(OFF)}$	20	75	120	ns	From 20% of IDISCHG to 80% of IDISCHG, x = 0 to 63, C_{Load} = 20 nF	P_BDRV_01_13
HS delay on time low	$t_{delay\_on(HS)}$	220	280	360	ns	HBFREQ = 0_B From IHx reaching high voltage threshold to 20% of ICHGx, x = 0 to 63	P_BDRV_01_14
HS delay on time high	$t_{delay\_on(HS)}$	250	320	400	ns	HBFREQ = 1_B From IHx reaching high voltage threshold to 20% of ICHGx, x = 0 to 63	P_BDRV_01_15
HS delay off time low	$t_{delay\_off(HS)}$	220	280	360	ns	HBFREQ = 0_B From IHx reaching low voltage threshold to 20% of IDISCHGx, x = 0 to 63	P_BDRV_01_16
HS delay off time high	$t_{delay\_off(HS)}$	250	320	400	ns	HBFREQ = 1_B From IHx reaching low voltage threshold to 20% of IDISCHGx, x = 0 to 63	P_BDRV_01_17
LS delay on time low	$t_{delay\_on(LS)}$	220	280	360	ns	HBFREQ = 0_B From ILx reaching high voltage threshold to 20% of ICHGx, x = 0 to 63	P_BDRV_01_18

(table continues...)

Table 14 (continued) Electrical characteristics gate driver

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
LS delay on time high	$t_{delay\_on(LS)}$	250	320	400	ns	HBFREQ = 1_B From ILx reaching high voltage threshold to 20% of ICHGx, x = 0 to 63	P_BDRV_01_19
LS delay off time low	$t_{delay\_off(LSx)}$	220	280	360	ns	HBFREQ = 0_B From ILx reaching low voltage threshold to 20% of IDISCHGx, x = 0 to 63	P_BDRV_01_20
LS delay off time high	$t_{delay\_off(LSx)}$	250	320	400	ns	HBFREQ = 1_B From ILx reaching low voltage threshold to 20% of IDISCHGx, x = 0 to 63	P_BDRV_01_21
Charge/discharge current accuracy (00 0000B)	I_{ACC0}	-60	–	+75	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $00\ 0000_B$	P_BDRV_01_22
Charge/discharge current accuracy (00 1111B)	I_{ACC15}	-40	–	+40	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $00\ 1111_B$	P_BDRV_01_23
Charge/discharge current accuracy (01 1111B)	I_{ACC31}	-30	–	+30	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $01\ 1111_B$	P_BDRV_01_24
Charge/discharge current accuracy (10 1111B)	I_{ACC31}	-20	–	+20	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $10\ 1111_B$, IGx_SEL = 0_B	P_BDRV_01_25

(table continues...)

Table 14 (continued) Electrical characteristics gate driver

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Charge/discharge current accuracy (10 1111B)	I_{ACC31_H}	-25	–	+25	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $10\ 1111_B$, IGx_SEL = 1_B	P_BDRV_01_43
Charge/discharge current accuracy (11 1111B)	I_{ACC63}	-20	–	+20	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $11\ 1111_B$, IGx_SEL = 0_B	P_BDRV_01_26
Charge/discharge current accuracy (11 1111B)	I_{ACC63_H}	-25	–	+25	%	ICHG / IDISCHG / IPRECHG / IPREDISCHG / IPOSTCHG / ICHGM / IDISCHGM = $11\ 1111_B$, IGx_SEL = 1_B	P_BDRV_01_44
Discharge_ST current accuracy (0 0000B)	I_{ACC_ST0}	-60	–	+75	%	IDISCHG_ST = $0\ 0000_B$	P_BDRV_01_27
Discharge_ST current accuracy (0 0111B)	I_{ACC_ST7}	-40	–	+40	%	IDISCHG_ST = $0\ 0111_B$	P_BDRV_01_28
Discharge_ST current accuracy (0 1111B)	I_{ACC_ST15}	-30	–	+30	%	IDISCHG_ST = $0\ 1111_B$	P_BDRV_01_29
Discharge_ST current accuracy (1 0111B)	I_{ACC_ST23}	-20	–	+20	%	IDISCHG_ST = $1\ 0111_B$, IGx_SEL = 0_B	P_BDRV_01_30
Discharge_ST current accuracy (1 0111B)	$I_{ACC\_ST23\_H}$	-25	–	+25	%	IDISCHG_ST = $1\ 0111_B$, IGx_SEL = 1_B	P_BDRV_01_45
Discharge_ST current accuracy (1 1111B)	I_{ACC_ST31}	-20	–	+20	%	IDISCHG_ST = $1\ 1111_B$, IGx_SEL = 0_B	P_BDRV_01_31
Discharge_ST current accuracy (1 1111B)	$I_{ACC\_ST31\_H}$	-25	–	+25	%	IDISCHG_ST = $1\ 1111_B$, IGx_SEL = 1_B	P_BDRV_01_46

(table continues...)

Table 14 (continued) Electrical characteristics gate driver

V_{SM} = 8.0 V to 60 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SHMx comparator delay	t_{SHMx}	–	5	40	ns	–	P_BDRV_01_35
Discharge timeout	$t_{OFF\_timeout}$	3.2	4	4.8	µs	–	P_BDRV_01_32
SHMx High Threshold	V_{SHMH}	V_{DH} - 3.0	–	V_{DH} - 2.0	V	–	P_BDRV_01_33
SHMx Low Threshold	V_{SHL}	1.8	–	3.0	V	Referred to GND	P_BDRV_01_34
On resistance of gate current source	R_{ONGX}	2	–	11	Ω	–	P_BDRV_01_36
BEMF comparator accuracy	V_{BEMF_ACC}	-100	–	+100	mV	V_{SM} = 48V	P_BDRV_01_37
BEMF hysteresis	V_{BEMF_HYS}	–	100	–	mV	–	P_BDRV_01_38

7 BEMF comparator

The device has 3 BEMF comparators integrated. GEF can be configured to show the output of each BEMF comparator and sent back via SDO as shown in Figure 16 below.

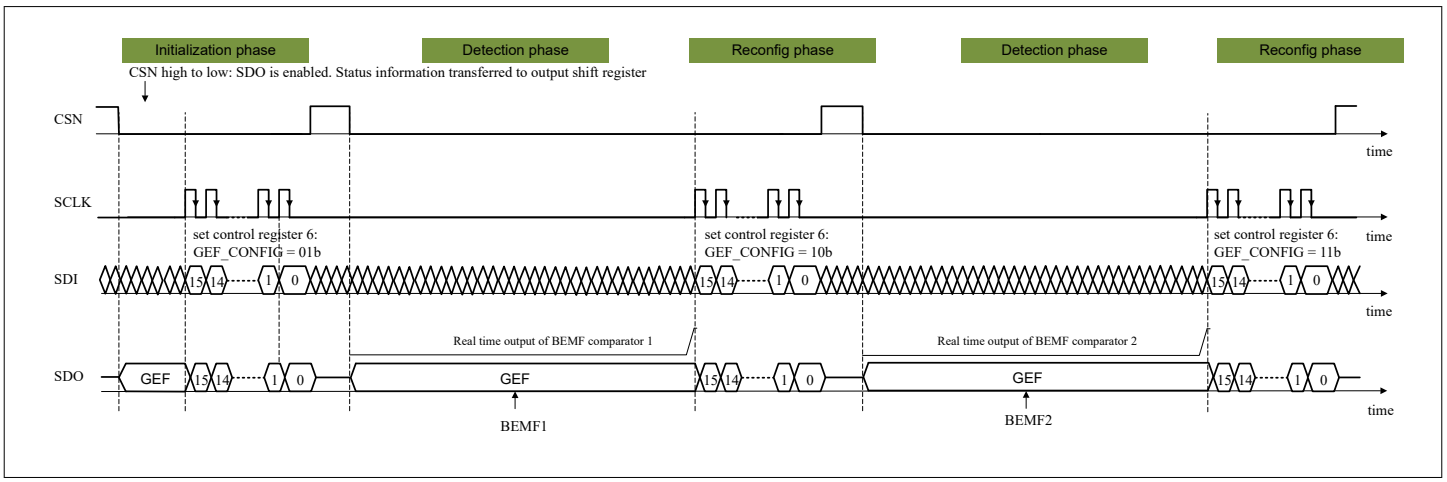

Figure 16 BEMF signal is sent back via SDO

When BEMF_POCESSING_EN bit is set to 0_B, the real time signal of the outputs of the BEMF comparators can be read from STAT4:

If the voltage at SHMx is higher than the average voltage of the other two SHM pins (SHMy + SHMz) / 2, the output of the corresponding BEMF comparator will be set to 1, and the corresponding bit in the status register will be set to 1.

If the voltage at SHMx is lower than the average voltage of the other two SHM pins (SHMy + SHMz) / 2, the output of the corresponding BEMF comparator will be set to 0, and the corresponding bit in the status register will be set to 0.

If the BEMF_POCESSING_EN bit is set to 1_B, the BEMF signal read from STAT4 will be the output signal with the post-processing algorithm.

8 Serial Peripheral Interface - SPI

8.1 SPI description

The control input word is read via the data input SDI, which is synchronized with the clock input SCLK provided by the general microcontroller or the MOTIX™ MCU. The output word appears synchronously at the data output SDO, see Figure 17.

The transmission cycle begins when the chip is selected by the input CSN (chip select not), low active. After the CSN input returns from low to high, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (high impedance) at this point, thereby releasing the SDO bus for other use. The state of SDI is shifted into the input register with every falling edge on SCLK. The state of SDO is shifted out of the output register after every rising edge on SCLK. The SPI of the device is not daisy chain capable.

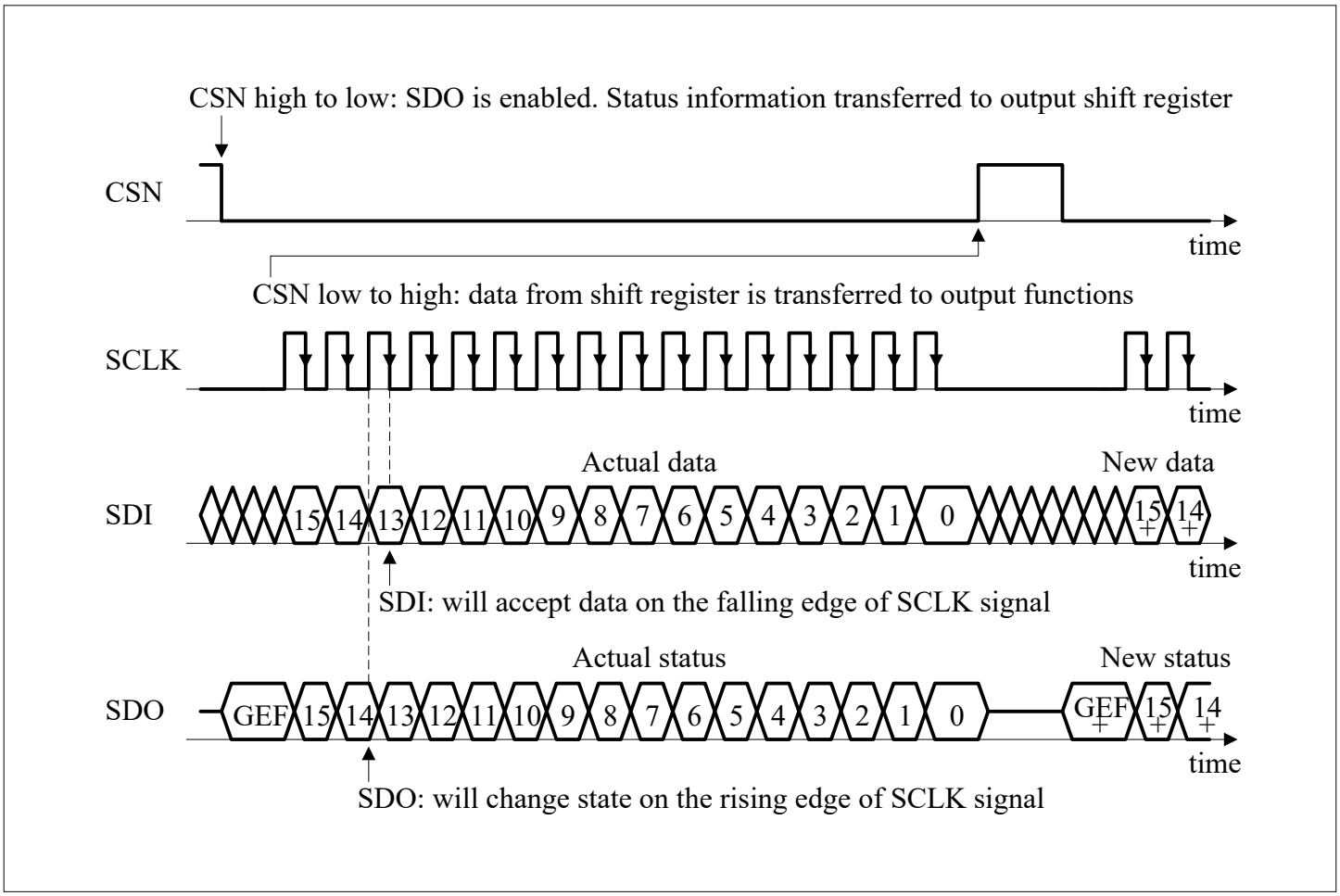

Figure 17 SPI data transfer timing

A SPI communication consists of 16-bit frames:

- SDI receives one address byte followed by one data byte
- SDO transmits the Global error flag and the Global status byte followed by one response byte

The address byte specifies (see Figure 18):

- The target register (A[6:0])
- The type of operation:
  - For control registers:
    - Read only: OP bit = 0
    - Read and write: OP bit = 1
  - For status registers:
    - Read only: OP bit = 0
    - Read and clear: OP bit = 1

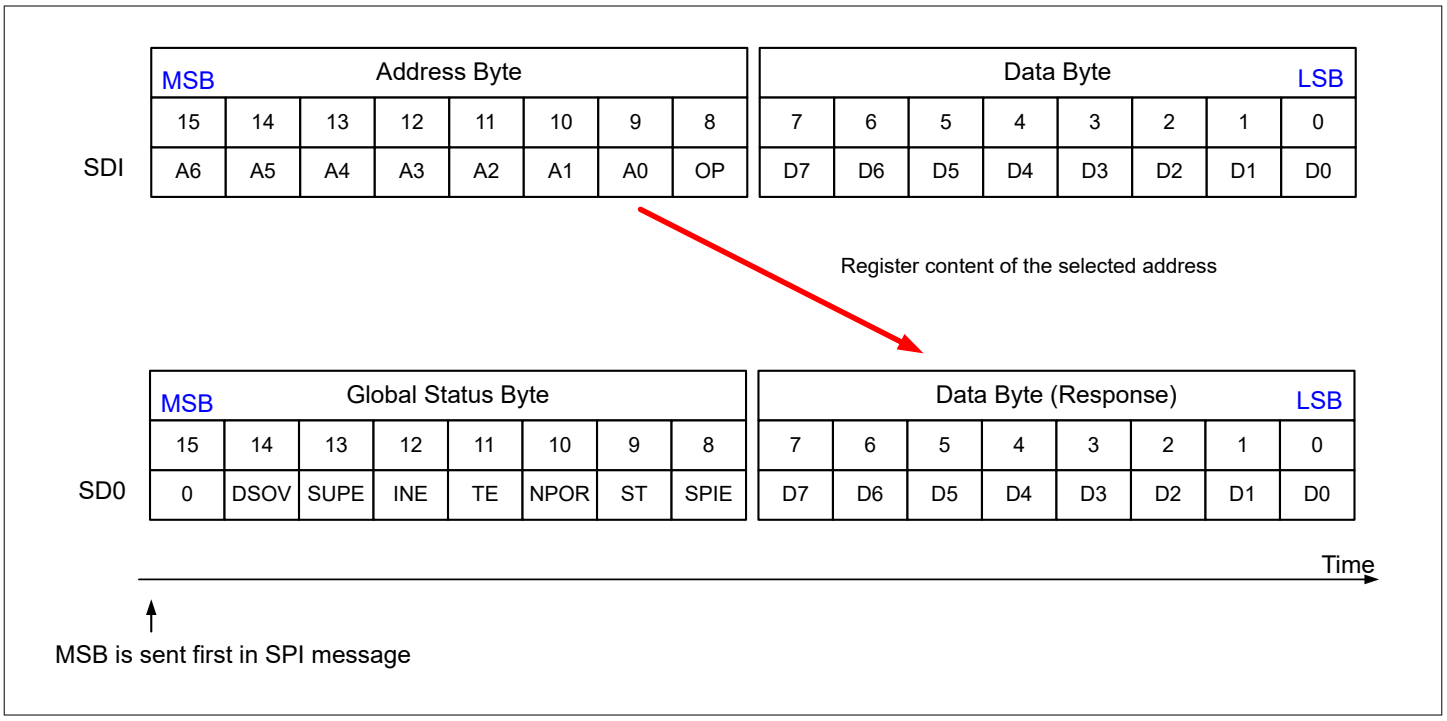

Figure 18 In-frame response

8.2 Global error flag

GEF bit can be configured by GEF_CONFIG in GENTRL6:

- 00_B global error flag
- 01_B back EMF1
- 10_B back EMF2
- 11_B back EMF3

The global error flag (GEF) bit is reported on SDO between the CSN falling edge and the first SCLK rising edge.

When the GEF bit is configured as a global error flag, the device is possible to have a quick diagnostic without any SPI clock pulse in following conditions:

- A fault condition is detected as in Table 15
- The device comes from a power-on-reset

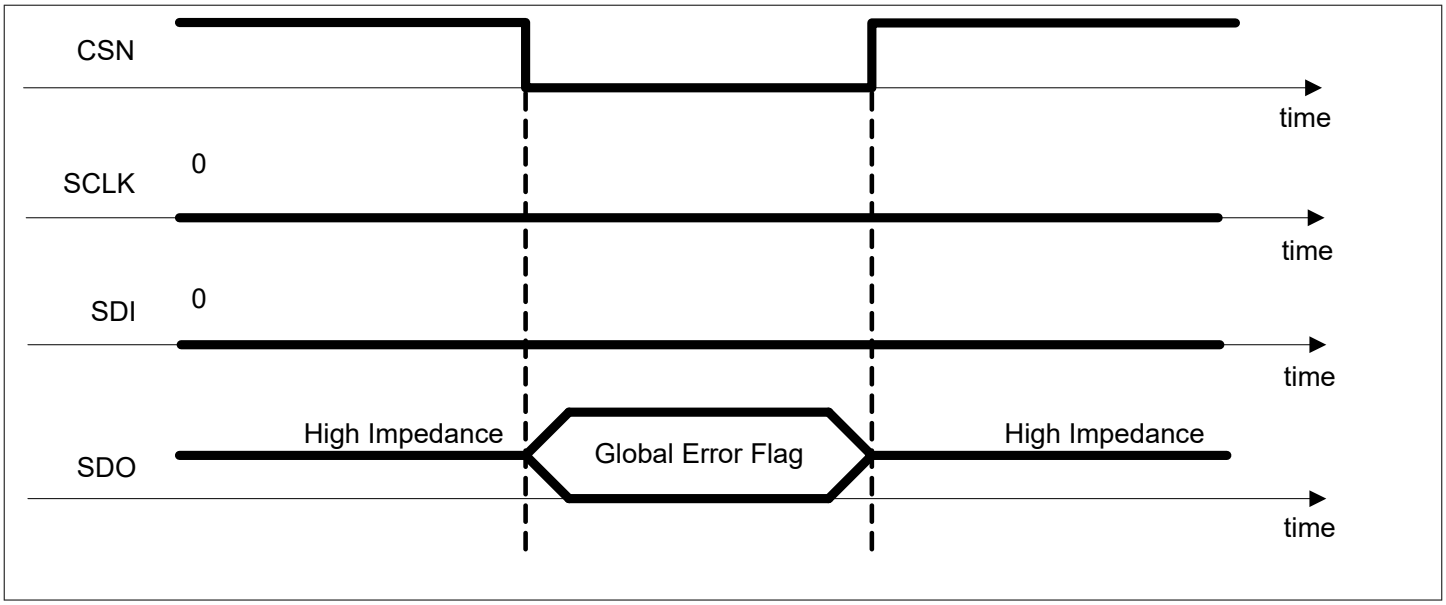

Figure 19 GEF - diagnostic with 0 - clock cycle

8.3 Global status byte

The SDO shifts out the general status register during the first eight SCLK cycles to provide an overview of the device status shown in Table 15 as following (in Figure 18):

- VDS monitoring error (DSOV bit): logical OR combination between HSxDSOV and LSxDSOV
- Supply error (SUPE bit): logical OR combination between VSM undervoltage shutdown (VSMUV), VSM overvoltage shutdown (VSMOV and VSMOV_PROT) and charge pump (CP1UV and CP2UV)
- Input error (INE bit): logical OR combination of INEx bits
- Temperature error (TE bit):
  - Logical OR combination between thermal warning (TW) and thermal shutdown (TSD) when TWDIS = 0
  - Thermal shutdown (TSD) when TSD = 1
- Negated power-on-reset (nPOR bit)
- Stop mode (ST bit)
- SPI protocol error (SPIE bit)

Note: The Global error flag is a logic OR combination of every bit of the global status byte: GEF = (DSOV) OR (SUPE) OR (INE) OR (TE) OR (NOT(nPOR)) OR (ST) OR (SPIE).

Table 15 Failure reported in the global status byte and global error flag

Type of error	Failure reported in the global status byte	Global error flag
VDS monitoring error	DSOV = 1	1
Supply error	SUPE = 1	1
Input error	INE = 1	1
Temperature error	TE = 1	1
Power-on-reset	**NPOR = 0**	1
Stop mode	ST = 1	1
SPI protocol error	SPIE = 1	1

(table continues...)

Table 15 (continued) Failure reported in the global status byte and global error flag

Type of error	Failure reported in the global status byte	Global error flag
No error and no power-on-reset	DSOV = 0 SUPE = 0 INE = 0 TE = 0 **NPOR = 1** ST = 0 SPIE = 0	0

8.4 SPI error detection

The SPI incorporates an error flag SPIE in STAT and Global status byte to supervise and preserve the data integrity.
The SPIE bit is set in the next SPI communication if following SPI errors are detected during a given frame:

- The number of SCLK clock pulses received for the duration CSN = 0 is (protocol error):
  - Not zero
  - Or less than 16
  - Or more than 16
- A watchdog trigger with an incorrect checksum bit is sent
- The microcontroller sends an SPI command to an unused address (protocol error)
- A clock polarity error is detected, see the Figure 22 below: the incoming clock signal was high during CSN rising or falling edges (protocol error)
- Any command to clear status registers in stop mode and not belonging to the exit sequence
- Any command to write control registers in stop mode and not belonging to the exit sequence

To ensure a correct SPI communication, the following conditions have to be fulfilled:

- SCLK must be low for a minimum t_{BEF} before CSN falling edge and t_{lead} after CSN falling edge
- SCLK must be low for a minimum t_{lag} before CSN rising edge and t_{BEH} after CSN rising edge

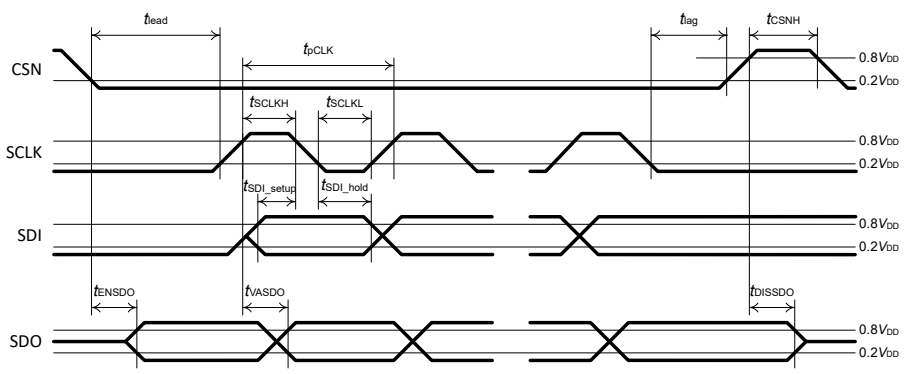

Figure 20 SPI timing parameters

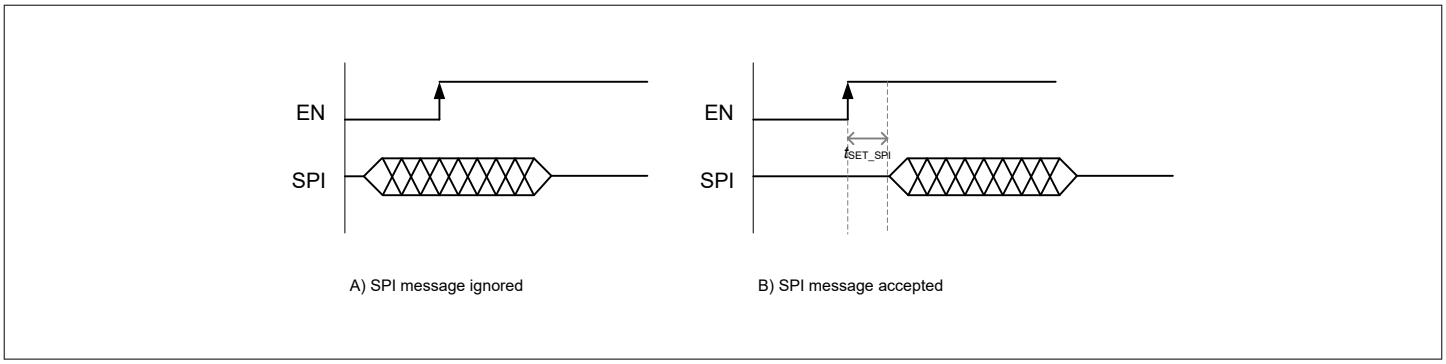

Figure 21 Setup time from EN rising edge to first SPI communication

The SPI error bit SPIE is reset under the following conditions:

- The SPI error bit SPIE can be reset only In normal mode when the microcontroller must clear the SPIE bit in STAT
- In stop mode the microcontroller must enter normal operation mode and clear the SPIE bit in STAT

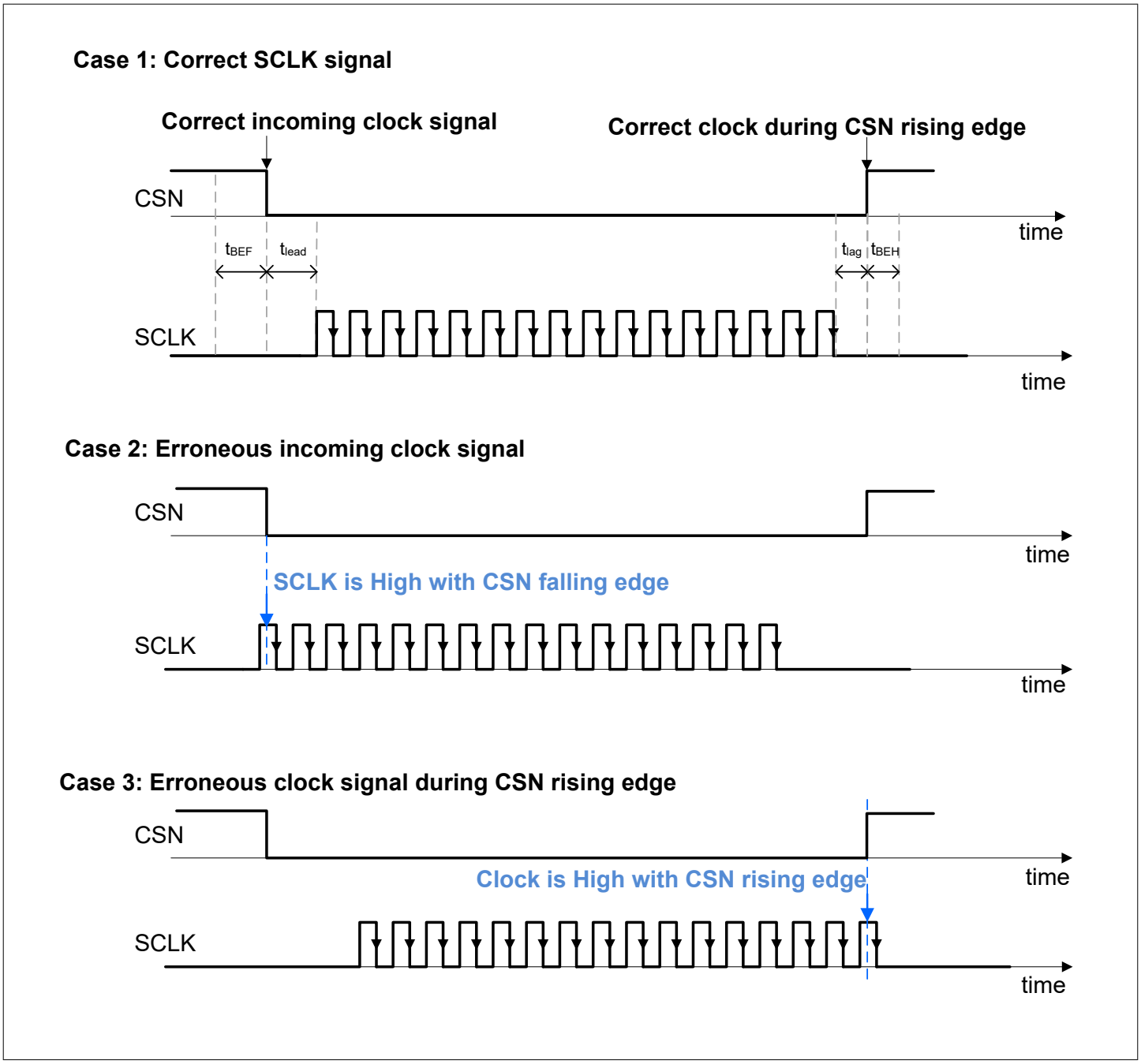

Figure 22 Polarity error

8.5 Electrical characteristics SPI

Table 16 SPI electrical characteristics

V_{SM} = 8.0 V to 60 V, V_{DD} = 3 V to 5.5 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4	MHz	–	P_SPI_01_01
Delay from EN rising edge to first SPI frame							
SPI interface setup time	t_{SET_SPI}	–	–	500	µs	–	P_SPI_01_02
SPI interface (SDI, SCLK, CSN)							
High input voltage threshold (VDD = 5 V)	V_{IH1}	2.5	–	–	V	V_{DD} = 5 V	P_SPI_01_03
High input voltage threshold (VDD = 3.3 V)	V_{IH2}	1.5	–	–	V	V_{DD} = 3.3 V	P_SPI_01_04
Low input voltage threshold (VDD = 5 V)	V_{IL1}	–	–	0.8	V	V_{DD} = 5 V	P_SPI_01_05
Low input voltage threshold (VDD = 3.3 V)	V_{IL2}	–	–	0.6	V	V_{DD} = 3.3 V	P_SPI_01_06
Hysteresis of input voltage (VDD = 5 V)	V_{IHY1}	100	–	–	mV	V_{DD} = 5 V	P_SPI_01_07
Hysteresis of input voltage (VDD = 3.3 V)	V_{IHY2}	100	–	–	mV	V_{DD} = 3.3 V	P_SPI_01_08
Pull down resistor at input pin ILx, IHx	R_{pd}	25	40	60	kΩ	V_{EN} = V_{DD} = 5 V or V_{EN} = V_{DD} = 3.3 V	P_SPI_01_09
Pull up resistor at pin CSN	R_{PU_CSN}	25	40	60	kΩ	–	P_SPI_01_10
Pull down resistor at pin SDI, SCLK	R_{PD_SDI}, R_{PD_SCLK}	25	40	60	kΩ	V_{EN} = V_{DD} = 5 V or V_{EN} = V_{DD} = 3.3 V	P_SPI_01_11
Input capacitance at pin CSN, SDI and SCLK	C_I	–	–	10	pF	0 V < V_{DD} < 5.5 V	P_SPI_01_12

(table continues...)

Table 16 (continued) SPI electrical characteristics

V_{SM} = 8.0 V to 60 V, V_{DD} = 3 V to 5.5 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input interface, logic outputs SDO							
High output voltage level	V_{SDOH}	V_{DD} - 0.4	–	–	V	$\|I_{SDOH}\|$ = 1.6 mA	P_SPI_01_13
Low output voltage level	V_{SDOL}	–	–	0.4	V	$\|I_{SDOL}\|$ = 1.6 mA	P_SPI_01_14
Tri-state leakage current	I_{SDOLK}	-10	–	10	µA	$V_{CSN} = V_{DD}$; 0 V < V_{SDO} < V_{DD}	P_SPI_01_15
Tri-state input capacitance	C_{SDO}	–	–	15	pF	–	P_SPI_01_16
Data input timing							
SCLK period	t_{pCLK}	250	–	–	ns	–	P_SPI_01_17
SCLK high time	t_{SCLKH}	0.45 * t_{pCLK}	–	0.55 * t_{pCLK}	ns	–	P_SPI_01_18
SCLK low time	t_{SCLKL}	0.45 * t_{pCLK}	–	0.55 * t_{pCLK}	ns	–	P_SPI_01_19
CSN setup time	t_{lead}	250	–	–	ns	–	P_SPI_01_21
SCLK setup time	t_{lag}	250	–	–	ns	–	P_SPI_01_22
SCLK low after CSN high	t_{BEH}	125	–	–	ns	–	P_SPI_01_23
SDI setup time	t_{SDI_setup}	100	–	–	ns	–	P_SPI_01_24
SDI hold time	t_{SDI_hold}	50	–	–	ns	–	P_SPI_01_25
Input signal rise time at pin SDI, SCLK, CSN	t_{rIN}	–	–	50	ns	–	P_SPI_01_26
Input signal fall time at pin SDI, SCLK, CSN	t_{fIN}	–	–	50	ns	–	P_SPI_01_27
Minimum CSN high time	t_{CSNH}	3	–	–	µs	–	P_SPI_01_28
Data output timing							
SDO rise time	t_{rSDO}	–	30	80	ns	C_{Load} = 100 pF	P_SPI_01_29
SDO fall time	t_{fSDO}	–	30	80	ns	C_{Load} = 100 pF	P_SPI_01_30
SDO enable time after CSN falling edge	t_{ENSDO}	–	–	80	ns	–	P_SPI_01_31

(table continues...)

Table 16 (continued) SPI electrical characteristics

V_{SM} = 8.0 V to 60 V, V_{DD} = 3 V to 5.5 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SDO disable time after CSN	t_{DISSDO}	–	–	50	ns	–	P_SPI_01_32
SDO valid time for VDD = 5 V	t_{VASDO}	–	–	80	ns	V_{SDO} < 0.2 * V_{DD}, V_{SDO} > 0.8 * V_{DD} C_{load} = 100 pF	P_SPI_01_33

9 Register specification

9.1 Register overview

Table 17 Register overview

Register short name	Register long name
GENCTRL1	General control register 1
GENCTRL2	General control register 2
GENCTRL3	General control register 3
GENCTRL4	General control register 4
GENCTRL5	General control register 5
GENCTRL6	General control register 6
GENCTRL7	General control register 7
GENCTRL8	General control register 8
GENCTRL9	General control register 9
GENCTRL10	General control register 10
GENCTRL11	General control register 11
GENCTRL12	General control register 12
GENCTRL13	General control register 13
STAT	General status register
STAT1	Global status register 1
STAT2	Global status register 2
STAT3	Global status register 3
STAT4	Global status register 4
STAT5	Effective high-side MOSFET turn-on delay PWM1
STAT6	Effective high-side MOSFET turn-off delay PWM1
STAT7	Effective low-side MOSFET turn-on delay PWM1
STAT8	Effective low-side MOSFET turn-off delay PWM1
STAT9	Effective high-side MOSFET turn-on delay PWM2
STAT10	Effective high-side MOSFET turn-off delay PWM2
STAT11	Effective low-side MOSFET turn-on delay PWM2
STAT12	Effective low-side MOSFET turn-off delay PWM2
STAT13	Effective high-side MOSFET turn-on delay PWM3
STAT14	Effective high-side MOSFET turn-off delay PWM3
STAT15	Effective low-side MOSFET turn-on delay PWM3
STAT16	Effective low-side MOSFET turn-off delay PWM3

(table continues...)

Table 17 (continued) Register overview

Register short name	Register long name
STAT17	Effective high-side MOSFET rise time PWM1
STAT18	Effective high-side MOSFET fall time PWM1
STAT19	Effective low-side MOSFET rise time PWM1
STAT20	Effective low-side MOSFET fall time PWM1
STAT21	Effective high-side MOSFET rise time PWM2
STAT22	Effective high-side MOSFET fall time PWM2
STAT23	Effective low-side MOSFET rise time PWM2
STAT24	Effective low-side MOSFET fall time PWM2
STAT25	Effective high-side MOSFET rise time PWM3
STAT26	Effective high-side MOSFET fall time PWM3
STAT27	Effective low-side MOSFET rise time PWM3
STAT28	Effective low-side MOSFET fall time PWM3

9.2 Control Registers

- The control registers will be reset to default values after power up or reset
- There are different bit types:
  - 'r' = READ: read only bits (or reserved bits)
  - 'rw' = READ/WRITE: readable and writable bits
- Reserved bits are marked as "Reserved" and always read as 0. The respective bits shall also be programmed as 0
- Reading a register is done word wise by setting the SPI bit OP to 0 (= read only)
- The SPI control registers are not cleared or changed automatically. It must be done by the microcontroller via SPI programming

9.2.1 General control register 1

Table 18 General control register 1 (000 0001B) Reset value: 0010 0001B

7	6	5	4	3	2	1	0
HBFREQ	**BD_EN**	**HSLSOV_DIS**	**DG**	**IGx_SEL**	**UNLOCK**	**FMODE_1**	**FMODE_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
HBFREQ	7	rw	**HB frequency** 0_B 37.5 MHz (default) 1_B 18.75 MHz
BD_EN	6	rw	**Bridge driver enable** 0_B the bridge driver is disabled 1_B the bridge driver in enabled

(table continues...)

Table 18 (continued) General control register 1 (000 0001B) Reset value: 0010 0001B

HSLSOV_DIS	5	rw	**Over-current protection** 0_B when VDS_HSx or VDS_LSx ≥ VDSTH, all gate drivers will be switched off 1_B when VDS_HSx or VDS_LSx ≥ VDSTH, the gate drivers of the same half - bridge will be switch off (default)
DG	4	rw	**Deglitch for high speed comparator** 0_B the deglitch feature is disabled (default) 1_B the deglitch feature is enabled Note: Enable deglitch feature can ignore small glitches at the comparator input.
IGx_SEL	3	rw	**Charge/discharge current extension bit:** 0_B keep the current set by corresponding bits (default) 1_B enlarge all currents to max. 480 mA Note: I represents the IPRECHG, ICHG, ICHGM, IHOLD, IPREDISCHG, IDISCHG, IDISCHGM, IPOSTCHG and IDISCHG_ST.
UNLOCK	2	rw	**Unlock bit to disable the watchdog** 0_B WDDIS cannot be reset (default) 1_B WDDIS can be reset in following SPI frame
FMODE	[1:0]	rw	**Frequency modulation** 00_B no modulation 01_B modulation frequency 15.6 kHz (default) 10_B modulation frequency 31.2 kHz 11_B modulation frequency 62.5 kHz

9.2.2 General control register 2

Table 19 General control register 2 ($000\ 0010_B$) Reset value: $x000\ 0100_B$

7	6	5	4	3	2	1	0
CHECKSUM	**RES**	**RES**	**RES**	**RES**	**WDPER**		
rw	r	r	r	r	rw		

Field	Bits	Type	Description
CHECKSUM	7	rw	**Watchdog Setting Check Sum Bit** The sum of bits 6:0 needs to have even parity 0_B counts as 0 for checksum calculation 1_B counts as 1 for checksum calculation
RES	6	r	**Reserved. Always read as 0**
RES	5	r	**Reserved. Always read as 0**

(table continues...)

Table 19 (continued) General control register 2 (000 0010_B) Reset value: x000 0100_B

RES	4	r	**Reserved. Always read as 0**
RES	3	r	**Reserved. Always read as 0**
WDPER	[2:0]	rw	**Watchdog period** 000_B 2 ms 001_B 4 ms 010_B 8 ms 011_B 16 ms 100_B 64 ms (default) 101_B 128 ms 110_B 256 ms 111_B 512 ms

9.2.3 General control register 3

Table 20 General control register 3 (000 0011_B) Reset value: 0000 0001_B

7	6	5	4	3	2	1	0
WDDIS	**TWDIS**	**HB3DIAG**	**HB2DIAG**	**HB1DIAG**	**VDSTH**		
rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
WDDIS	7	rw	**Watchdog disable bit** 0_B the watchdog is enabled (default) 1_B the watchdog is disabled if the previous SPI frame has set UNLOCK bit (**GENCTRL1**) Once the watchdog is disabled, it is directly re-enabled by resetting WDDIS.
TWDIS	6	rw	**Thermal warning disable** 0_B TW is reported in GEF and set in global status register (default) 1_B TW is not reported in GEF, but it is set in global status register
HB3DIAG	5	rw	**Control of HB3 off-state current source and current sink** 0_B pull-down deactivated (default) 1_B pull-down activated
HB2DIAG	4	rw	**Control of HB2 off-state current source and current sink** 0_B pull-down deactivated (default) 1_B pull-down activated
HB1DIAG	3	rw	**Control of HB1 off-state current source and current sink** 0_B pull-down deactivated (default) 1_B pull-down activated

(table continues...)

Table 20 (continued) General control register 3 (000 0011_B) Reset value: 0000 0001_B

VDSTH	[2:0]	rw	**Drain - source overvoltage threshold** 000_B : 145 mV 001_B : 195 mV(default) 010_B : 245 mV 011_B : 295 mV 100_B : 390 mV 101_B : 490 mV 110_B : 590 mV 111_B : 2 V

9.2.4 General control register 4

Table 21 General control register 4 (000 0100_B) Reset value: 0000 1111_B

7	6	5	4	3	2	1	0
IPRECHG_T		**IPRECHG**					
rw		rw					

Field	Bits	Type	Description		
IPRECHG_T	[7:6]	rw	**Pre - charge time of HB1 - HB3** 00_B 100 ns (default) 01_B 150 ns 10_B 200 ns 11_B 250 ns		
IPRECHG	[5:0]	rw	**Pre - charge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			00 0000_B	11.6 mA	11.6 mA
			00 0001_B	14.8 mA	15.8 mA
			00 0010_B	18.1 mA	20.1 mA
			00 0011_B	21.3 mA	24.3 mA
			00 0100_B	24.5 mA	28.5 mA
			00 0101_B	27.7 mA	32.7 mA
			00 0110_B	31.0 mA	37.0 mA
			00 0111_B	34.2 mA	41.2 mA
			00 1000_B	37.4 mA	45.4 mA
			00 1001_B	40.6 mA	49.7 mA
			00 1010_B	43.9 mA	53.9 mA
			00 1011_B	47.1 mA	58.1 mA

(table continues...)

Table 21 (continued) General control register 4 (000 0100_B) Reset value: $0000\ 1111_B$

			$00\ 1100_B$	50.3 mA	62.4 mA
			$00\ 1101_B$	53.6 mA	66.6 mA
			$00\ 1110_B$	56.8 mA	70.8 mA
			$00\ 1111_B$ (def.)	60.0 mA	75.0 mA
			$01\ 0000_B$	65.4 mA	82.1 mA
			$01\ 0001_B$	70.8 mA	89.3 mA
			$01\ 0010_B$	76.1 mA	96.4 mA
			$01\ 0011_B$	81.5 mA	103.5 mA
			$01\ 0100_B$	86.9 mA	111.6 mA
			$01\ 0101_B$	92.3 mA	117.8 mA
			$01\ 0110_B$	97.6 mA	124.9 mA
			$01\ 0111_B$	103.0 mA	132.0 mA
			$01\ 1000_B$	108.4 mA	139.1 mA
			$01\ 1001_B$	113.8 mA	146.3 mA
			$01\ 1010_B$	119.1 mA	153.4 mA
			$01\ 1011_B$	124.5 mA	160.5 mA
			$01\ 1100_B$	129.9 mA	167.6 mA
			$01\ 1101_B$	135.3 mA	174.8 mA
			$01\ 1110_B$	140.6 mA	181.9 mA
			$01\ 1111_B$	146.0 mA	189.0 mA
			$10\ 0000_B$	152.9 mA	197.8 mA
			$10\ 0001_B$	159.8 mA	206.6 mA
			$10\ 0010_B$	166.6 mA	215.4 mA
			$10\ 0011_B$	173.5 mA	224.2 mA
			$10\ 0100_B$	180.4 mA	233.1 mA
			$10\ 0101_B$	187.2 mA	241.9 mA
			$10\ 0110_B$	194.1 mA	250.7 mA
			$10\ 0111_B$	201.0 mA	259.5 mA
			$10\ 1000_B$	207.9 mA	268.3 mA
			$10\ 1001_B$	214.8 mA	277.1 mA
			$10\ 1010_B$	221.6 mA	285.9 mA
			$10\ 1011_B$	228.5 mA	294.7 mA
			$10\ 1100_B$	235.4 mA	303.5 mA
			$10\ 1101_B$	242.3 mA	312.3 mA

(table continues...)

Table 21 (continued) General control register 4 (000 0100_B) Reset value: 0000 1111_B

			$10\ 1110_B$	249.1 mA	321.2 mA
			$10\ 1111_B$	256.0 mA	330.0 mA
			$11\ 0000_B$	263.4 mA	339.4 mA
			$11\ 0001_B$	270.9 mA	348.8 mA
			$11\ 0010_B$	278.3 mA	358.1 mA
			$11\ 0011_B$	285.8 mA	367.5 mA
			$11\ 0100_B$	293.2 mA	376.8 mA
			$11\ 0101_B$	300.6 mA	386.2 mA
			$11\ 0110_B$	308.1 mA	395.6 mA
			$11\ 0111_B$	315.5 mA	405.0 mA
			$11\ 1000_B$	323.0 mA	414.4 mA
			$11\ 1001_B$	330.4 mA	423.8 mA
			$11\ 1010_B$	337.8 mA	433.1 mA
			$11\ 1011_B$	345.3 mA	442.5 mA
			$11\ 1100_B$	352.7 mA	451.9 mA
			$11\ 1101_B$	360.2 mA	461.3 mA
			$11\ 1110_B$	367.6 mA	470.6 mA
			$11\ 1111_B$	375.0 mA	480.0 mA

9.2.5 General control register 5

Table 22 General control register 5 (000 0101_B) Reset value: 0000 1111_B

7	6	5	4	3	2	1	0
ICHG_T		**ICHG**					
rw		rw					

Field	Bits	Type	Description		
ICHG_T	[7:6]	rw	**Charge time of HB1 - HB3** 00_B 200 ns (default) 01_B 400 ns 10_B 600 ns 11_B 800 ns		
ICHG	[5:0]	rw	**Charge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			$00\ 0000_B$	11.6 mA	11.6 mA
			$00\ 0001_B$	14.8 mA	15.8 mA

(table continues...)

Table 22 (continued) General control register 5 (000 0101$_B$) Reset value: 0000 1111$_B$

			00 0010$_B$	18.1 mA	20.1 mA
			00 0011$_B$	21.3 mA	24.3 mA
			00 0100$_B$	24.5 mA	28.5 mA
			00 0101$_B$	27.7 mA	32.7 mA
			00 0110$_B$	31.0 mA	37.0 mA
			00 0111$_B$	34.2 mA	41.2 mA
			00 1000$_B$	37.4 mA	45.4 mA
			00 1001$_B$	40.6 mA	49.7 mA
			00 1010$_B$	43.9 mA	53.9 mA
			00 1011$_B$	47.1 mA	58.1 mA
			00 1100$_B$	50.3 mA	62.4 mA
			00 1101$_B$	53.6 mA	66.6 mA
			00 1110$_B$	56.8 mA	70.8 mA
			00 1111$_B$ (def.)	60.0 mA	75.0 mA
			01 0000$_B$	65.4 mA	82.1 mA
			01 0001$_B$	70.8 mA	89.3 mA
			01 0010$_B$	76.1 mA	96.4 mA
			01 0011$_B$	81.5 mA	103.5 mA
			01 0100$_B$	86.9 mA	111.6 mA
			01 0101$_B$	92.3 mA	117.8 mA
			01 0110$_B$	97.6 mA	124.9 mA
			01 0111$_B$	103.0 mA	132.0 mA
			01 1000$_B$	108.4 mA	139.1 mA
			01 1001$_B$	113.8 mA	146.3 mA
			01 1010$_B$	119.1 mA	153.4 mA
			01 1011$_B$	124.5 mA	160.5 mA
			01 1100$_B$	129.9 mA	167.6 mA
			01 1101$_B$	135.3 mA	174.8 mA
			01 1110$_B$	140.6 mA	181.9 mA
			01 1111$_B$	146.0 mA	189.0 mA
			10 0000$_B$	152.9 mA	197.8 mA
			10 0001$_B$	159.8 mA	206.6 mA
			10 0010$_B$	166.6 mA	215.4 mA
			10 0011$_B$	173.5 mA	224.2 mA

(table continues...)

Table 22 (continued) General control register 5 (000 0101$_B$) Reset value: 0000 1111$_B$

			10 0100$_B$	180.4 mA	233.1 mA
			10 0101$_B$	187.2 mA	241.9 mA
			10 0110$_B$	194.1 mA	250.7 mA
			10 0111$_B$	201.0 mA	259.5 mA
			10 1000$_B$	207.9 mA	268.3 mA
			10 1001$_B$	214.8 mA	277.1 mA
			10 1010$_B$	221.6 mA	285.9 mA
			10 1011$_B$	228.5 mA	294.7 mA
			10 1100$_B$	235.4 mA	303.5 mA
			10 1101$_B$	242.3 mA	312.3 mA
			10 1110$_B$	249.1 mA	321.2 mA
			10 1111$_B$	256.0 mA	330.0 mA
			11 0000$_B$	263.4 mA	339.4 mA
			11 0001$_B$	270.9 mA	348.8 mA
			11 0010$_B$	278.3 mA	358.1 mA
			11 0011$_B$	285.8 mA	367.5 mA
			11 0100$_B$	293.2 mA	376.8 mA
			11 0101$_B$	300.6 mA	386.2 mA
			11 0110$_B$	308.1 mA	395.6 mA
			11 0111$_B$	315.5 mA	405.0 mA
			11 1000$_B$	323.0 mA	414.4 mA
			11 1001$_B$	330.4 mA	423.8 mA
			11 1010$_B$	337.8 mA	433.1 mA
			11 1011$_B$	345.3 mA	442.5 mA
			11 1100$_B$	352.7 mA	451.9 mA
			11 1101$_B$	360.2 mA	461.3 mA
			11 1110$_B$	367.6 mA	470.6 mA
			11 1111$_B$	375.0 mA	480.0 mA

9.2.6 General control register 6

Table 23 General control register 6 (000 0110$_B$) Reset value: 0000 1111$_B$

7	6	5	4	3	2	1	0
GEF_CONFIG		**IPOSTCHG**					
rw		rw					

(table continues...)

Table 23 (continued) General control register 6 (000 0110_B) Reset value: 0000 1111_B

Field	Bits	Type	Description		
GEF_CONFIG	[7:6]	rw	**Global Error Flag** 00_B GEF (default state) 01_B BEMF1 10_B BEMF2 11_B BEMF3		
IPOSTCHG	[5:0]	rw	**Post - charge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			00 0000_B	11.6 mA	11.6 mA
			00 0001_B	14.8 mA	15.8 mA
			00 0010_B	18.1 mA	20.1 mA
			00 0011_B	21.3 mA	24.3 mA
			00 0100_B	24.5 mA	28.5 mA
			00 0101_B	27.7 mA	32.7 mA
			00 0110_B	31.0 mA	37.0 mA
			00 0111_B	34.2 mA	41.2 mA
			00 1000_B	37.4 mA	45.4 mA
			00 1001_B	40.6 mA	49.7 mA
			00 1010_B	43.9 mA	53.9 mA
			00 1011_B	47.1 mA	58.1 mA
			00 1100_B	50.3 mA	62.4 mA
			00 1101_B	53.6 mA	66.6 mA
			00 1110_B	56.8 mA	70.8 mA
			00 1111_B (def.)	60.0 mA	75.0 mA
			01 0000_B	65.4 mA	82.1 mA
			01 0001_B	70.8 mA	89.3 mA
			01 0010_B	76.1 mA	96.4 mA
			01 0011_B	81.5 mA	103.5 mA
			01 0100_B	86.9 mA	111.6 mA
			01 0101_B	92.3 mA	117.8 mA
			01 0110_B	97.6 mA	124.9 mA
			01 0111_B	103.0 mA	132.0 mA
			01 1000_B	108.4 mA	139.1 mA
			01 1001_B	113.8 mA	146.3 mA

(table continues...)

Table 23 (continued) General control register 6 (000 0110_B) Reset value: $0000\ 1111_B$

			$01\ 1010_B$	119.1 mA	153.4 mA
			$01\ 1011_B$	124.5 mA	160.5 mA
			$01\ 1100_B$	129.9 mA	167.6 mA
			$01\ 1101_B$	135.3 mA	174.8 mA
			$01\ 1110_B$	140.6 mA	181.9 mA
			$01\ 1111_B$	146.0 mA	189.0 mA
			$10\ 0000_B$	152.9 mA	197.8 mA
			$10\ 0001_B$	159.8 mA	206.6 mA
			$10\ 0010_B$	166.6 mA	215.4 mA
			$10\ 0011_B$	173.5 mA	224.2 mA
			$10\ 0100_B$	180.4 mA	233.1 mA
			$10\ 0101_B$	187.2 mA	241.9 mA
			$10\ 0110_B$	194.1 mA	250.7 mA
			$10\ 0111_B$	201.0 mA	259.5 mA
			$10\ 1000_B$	207.9 mA	268.3 mA
			$10\ 1001_B$	214.8 mA	277.1 mA
			$10\ 1010_B$	221.6 mA	285.9 mA
			$10\ 1011_B$	228.5 mA	294.7 mA
			$10\ 1100_B$	235.4 mA	303.5 mA
			$10\ 1101_B$	242.3 mA	312.3 mA
			$10\ 1110_B$	249.1 mA	321.2 mA
			$10\ 1111_B$	256.0 mA	330.0 mA
			$11\ 0000_B$	263.4 mA	339.4 mA
			$11\ 0001_B$	270.9 mA	348.8 mA
			$11\ 0010_B$	278.3 mA	358.1 mA
			$11\ 0011_B$	285.8 mA	367.5 mA
			$11\ 0100_B$	293.2 mA	376.8 mA
			$11\ 0101_B$	300.6 mA	386.2 mA
			$11\ 0110_B$	308.1 mA	395.6 mA
			$11\ 0111_B$	315.5 mA	405.0 mA
			$11\ 1000_B$	323.0 mA	414.4 mA
			$11\ 1001_B$	330.4 mA	423.8 mA
			$11\ 1010_B$	337.8 mA	433.1 mA
			$11\ 1011_B$	345.3 mA	442.5 mA

(table continues...)

Table 23 (continued) General control register 6 (000 0110_B) Reset value: 0000 1111_B

			11 1100_B	352.7 mA	451.9 mA
			11 1101_B	360.2 mA	461.3 mA
			11 1110_B	367.6 mA	470.6 mA
			11 1111_B	375.0 mA	480.0 mA

9.2.7 General control register 7

Table 24 General control register 7 (000 0111_B) Reset value: 0000 1111_B

7	6	5	4	3	2	1	0
IPREDISCHG_T		**IPREDISCHG**					
rw		rw					

Field	Bits	Type	Description		
IPREDISCHG_T	[7:6]	rw	**Pre - discharge time of HB1 - HB3** 00_B 100 ns (default) 01_B 150 ns 10_B 200 ns 11_B 250 ns		
IPREDISCHG	[5:0]	rw	**Pre - discharge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			00 0000_B	11.6 mA	11.6 mA
			00 0001_B	14.8 mA	15.8 mA
			00 0010_B	18.1 mA	20.1 mA
			00 0011_B	21.3 mA	24.3 mA
			00 0100_B	24.5 mA	28.5 mA
			00 0101_B	27.7 mA	32.7 mA
			00 0110_B	31.0 mA	37.0 mA
			00 0111_B	34.2 mA	41.2 mA
			00 1000_B	37.4 mA	45.4 mA
			00 1001_B	40.6 mA	49.7 mA
			00 1010_B	43.9 mA	53.9 mA
			00 1011_B	47.1 mA	58.1 mA
			00 1100_B	50.3 mA	62.4 mA
			00 1101_B	53.6 mA	66.6 mA
			00 1110_B	56.8 mA	70.8 mA
			00 1111_B (def.)	60.0 mA	75.0 mA

(table continues...)

Table 24 (continued) General control register 7 (000 0111_B) Reset value: 0000 1111_B

			01 0000_B	65.4 mA	82.1 mA
			01 0001_B	70.8 mA	89.3 mA
			01 0010_B	76.1 mA	96.4 mA
			01 0011_B	81.5 mA	103.5 mA
			01 0100_B	86.9 mA	111.6 mA
			01 0101_B	92.3 mA	117.8 mA
			01 0110_B	97.6 mA	124.9 mA
			01 0111_B	103.0 mA	132.0 mA
			01 1000_B	108.4 mA	139.1 mA
			01 1001_B	113.8 mA	146.3 mA
			01 1010_B	119.1 mA	153.4 mA
			01 1011_B	124.5 mA	160.5 mA
			01 1100_B	129.9 mA	167.6 mA
			01 1101_B	135.3 mA	174.8 mA
			01 1110_B	140.6 mA	181.9 mA
			01 1111_B	146.0 mA	189.0 mA
			10 0000_B	152.9 mA	197.8 mA
			10 0001_B	159.8 mA	206.6 mA
			10 0010_B	166.6 mA	215.4 mA
			10 0011_B	173.5 mA	224.2 mA
			10 0100_B	180.4 mA	233.1 mA
			10 0101_B	187.2 mA	241.9 mA
			10 0110_B	194.1 mA	250.7 mA
			10 0111_B	201.0 mA	259.5 mA
			10 1000_B	207.9 mA	268.3 mA
			10 1001_B	214.8 mA	277.1 mA
			10 1010_B	221.6 mA	285.9 mA
			10 1011_B	228.5 mA	294.7 mA
			10 1100_B	235.4 mA	303.5 mA
			10 1101_B	242.3 mA	312.3 mA
			10 1110_B	249.1 mA	321.2 mA
			10 1111_B	256.0 mA	330.0 mA
			11 0000_B	263.4 mA	339.4 mA
			11 0001_B	270.9 mA	348.8 mA

(table continues...)

Table 24 (continued) General control register 7 (000 0111_B) Reset value: 0000 1111_B

			11 0010_B	278.3 mA	358.1 mA
			11 0011_B	285.8 mA	367.5 mA
			11 0100_B	293.2 mA	376.8 mA
			11 0101_B	300.6 mA	386.2 mA
			11 0110_B	308.1 mA	395.6 mA
			11 0111_B	315.5 mA	405.0 mA
			11 1000_B	323.0 mA	414.4 mA
			11 1001_B	330.4 mA	423.8 mA
			11 1010_B	337.8 mA	433.1 mA
			11 1011_B	345.3 mA	442.5 mA
			11 1100_B	352.7 mA	451.9 mA
			11 1101_B	360.2 mA	461.3 mA
			11 1110_B	367.6 mA	470.6 mA
			11 1111_B	375.0 mA	480.0 mA

9.2.8 General control register 8

Table 25 General control register 8 (000 1000_B) Reset value: 0000 1111_B

7	6	5	4	3	2	1	0
IHOLD		**IDISCHG**					
rw		rw					

Field	Bits	Type	Description		
IHOLD	[7:6]	rw	**Gate driver hold current IHOLD**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			00_B (def.)	11.6 mA	11.6 mA
			01_B	27.7 mA	32.7 mA
			10_B	40.6 mA	49.7 mA
			11_B	50.3 mA	62.4 mA
IDISCHG	[5:0]	rw	**Discharge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			00 0000_B	11.6 mA	11.6 mA
			00 0001_B	14.8 mA	15.8 mA
			00 0010_B	18.1 mA	20.1 mA
			00 0011_B	21.3 mA	24.3 mA

(table continues...)

Table 25 (continued) General control register 8 (000 1000_B) Reset value: 0000 1111_B

			$00\ 0100_B$	24.5 mA	28.5 mA
			$00\ 0101_B$	27.7 mA	32.7 mA
			$00\ 0110_B$	31.0 mA	37.0 mA
			$00\ 0111_B$	34.2 mA	41.2 mA
			$00\ 1000_B$	37.4 mA	45.4 mA
			$00\ 1001_B$	40.6 mA	49.7 mA
			$00\ 1010_B$	43.9 mA	53.9 mA
			$00\ 1011_B$	47.1 mA	58.1 mA
			$00\ 1100_B$	50.3 mA	62.4 mA
			$00\ 1101_B$	53.6 mA	66.6 mA
			$00\ 1110_B$	56.8 mA	70.8 mA
			$00\ 1111_B$ (def.)	60.0 mA	75.0 mA
			$01\ 0000_B$	65.4 mA	82.1 mA
			$01\ 0001_B$	70.8 mA	89.3 mA
			$01\ 0010_B$	76.1 mA	96.4 mA
			$01\ 0011_B$	81.5 mA	103.5 mA
			$01\ 0100_B$	86.9 mA	111.6 mA
			$01\ 0101_B$	92.3 mA	117.8 mA
			$01\ 0110_B$	97.6 mA	124.9 mA
			$01\ 0111_B$	103.0 mA	132.0 mA
			$01\ 1000_B$	108.4 mA	139.1 mA
			$01\ 1001_B$	113.8 mA	146.3 mA
			$01\ 1010_B$	119.1 mA	153.4 mA
			$01\ 1011_B$	124.5 mA	160.5 mA
			$01\ 1100_B$	129.9 mA	167.6 mA
			$01\ 1101_B$	135.3 mA	174.8 mA
			$01\ 1110_B$	140.6 mA	181.9 mA
			$01\ 1111_B$	146.0 mA	189.0 mA
			$10\ 0000_B$	152.9 mA	197.8 mA
			$10\ 0001_B$	159.8 mA	206.6 mA
			$10\ 0010_B$	166.6 mA	215.4 mA
			$10\ 0011_B$	173.5 mA	224.2 mA
			$10\ 0100_B$	180.4 mA	233.1 mA
			$10\ 0101_B$	187.2 mA	241.9 mA

(table continues...)

Table 25 (continued) General control register 8 (000 1000_B) Reset value: 0000 1111_B

			$10\ 0110_B$	194.1 mA	250.7 mA
			$10\ 0111_B$	201.0 mA	259.5 mA
			$10\ 1000_B$	207.9 mA	268.3 mA
			$10\ 1001_B$	214.8 mA	277.1 mA
			$10\ 1010_B$	221.6 mA	285.9 mA
			$10\ 1011_B$	228.5 mA	294.7 mA
			$10\ 1100_B$	235.4 mA	303.5 mA
			$10\ 1101_B$	242.3 mA	312.3 mA
			$10\ 1110_B$	249.1 mA	321.2 mA
			$10\ 1111_B$	256.0 mA	330.0 mA
			$11\ 0000_B$	263.4 mA	339.4 mA
			$11\ 0001_B$	270.9 mA	348.8 mA
			$11\ 0010_B$	278.3 mA	358.1 mA
			$11\ 0011_B$	285.8 mA	367.5 mA
			$11\ 0100_B$	293.2 mA	376.8 mA
			$11\ 0101_B$	300.6 mA	386.2 mA
			$11\ 0110_B$	308.1 mA	395.6 mA
			$11\ 0111_B$	315.5 mA	405.0 mA
			$11\ 1000_B$	323.0 mA	414.4 mA
			$11\ 1001_B$	330.4 mA	423.8 mA
			$11\ 1010_B$	337.8 mA	433.1 mA
			$11\ 1011_B$	345.3 mA	442.5 mA
			$11\ 1100_B$	352.7 mA	451.9 mA
			$11\ 1101_B$	360.2 mA	461.3 mA
			$11\ 1110_B$	367.6 mA	470.6 mA
			$11\ 1111_B$	375.0 mA	480.0 mA

9.2.9 General control register 9

Table 26 General control register 9 (000 1001_B) Reset value: 0000 1111_B

7	6	5	4	3	2	1	0
CPEN	**CPREC**	**ICHGM**					
rw	rw	rw					

Field	Bits	Type	Description

(table continues...)

Table 26 (continued) General control register 9 (000 1001_B) Reset value: $0000\ 1111_B$

CPEN	7	rw	**Charge pump enable** 0_B disable CP1 and CP2 modules (default) 1_B enable CP1 and CP2 modules		
CPREC	6	rw	**Charge pump automatic recovery enable** 0_B disable the automatic recovery for CP1 and CP2 when VSM left OV/UV conditions (default) 1_B enable the automatic recovery for CP1 and CP2 when VSM left OV/UV conditions		
ICHGM	[5:0]	rw	**Middle charge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			$00\ 0000_B$	11.6 mA	11.6 mA
			$00\ 0001_B$	14.8 mA	15.8 mA
			$00\ 0010_B$	18.1 mA	20.1 mA
			$00\ 0011_B$	21.3 mA	24.3 mA
			$00\ 0100_B$	24.5 mA	28.5 mA
			$00\ 0101_B$	27.7 mA	32.7 mA
			$00\ 0110_B$	31.0 mA	37.0 mA
			$00\ 0111_B$	34.2 mA	41.2 mA
			$00\ 1000_B$	37.4 mA	45.4 mA
			$00\ 1001_B$	40.6 mA	49.7 mA
			$00\ 1010_B$	43.9 mA	53.9 mA
			$00\ 1011_B$	47.1 mA	58.1 mA
			$00\ 1100_B$	50.3 mA	62.4 mA
			$00\ 1101_B$	53.6 mA	66.6 mA
			$00\ 1110_B$	56.8 mA	70.8 mA
			$00\ 1111_B$ (def.)	60.0 mA	75.0 mA
			$01\ 0000_B$	65.4 mA	82.1 mA
			$01\ 0001_B$	70.8 mA	89.3 mA
			$01\ 0010_B$	76.1 mA	96.4 mA
			$01\ 0011_B$	81.5 mA	103.5 mA
			$01\ 0100_B$	86.9 mA	111.6 mA
			$01\ 0101_B$	92.3 mA	117.8 mA
			$01\ 0110_B$	97.6 mA	124.9 mA
			$01\ 0111_B$	103.0 mA	132.0 mA
			$01\ 1000_B$	108.4 mA	139.1 mA
			$01\ 1001_B$	113.8 mA	146.3 mA

(table continues...)

Table 26 (continued) General control register 9 (000 1001_B) Reset value: 0000 1111_B

			01 1010_B	119.1 mA	153.4 mA
			01 1011_B	124.5 mA	160.5 mA
			01 1100_B	129.9 mA	167.6 mA
			01 1101_B	135.3 mA	174.8 mA
			01 1110_B	140.6 mA	181.9 mA
			01 1111_B	146.0 mA	189.0 mA
			10 0000_B	152.9 mA	197.8 mA
			10 0001_B	159.8 mA	206.6 mA
			10 0010_B	166.6 mA	215.4 mA
			10 0011_B	173.5 mA	224.2 mA
			10 0100_B	180.4 mA	233.1 mA
			10 0101_B	187.2 mA	241.9 mA
			10 0110_B	194.1 mA	250.7 mA
			10 0111_B	201.0 mA	259.5 mA
			10 1000_B	207.9 mA	268.3 mA
			10 1001_B	214.8 mA	277.1 mA
			10 1010_B	221.6 mA	285.9 mA
			10 1011_B	228.5 mA	294.7 mA
			10 1100_B	235.4 mA	303.5 mA
			10 1101_B	242.3 mA	312.3 mA
			10 1110_B	249.1 mA	321.2 mA
			10 1111_B	256.0 mA	330.0 mA
			11 0000_B	263.4 mA	339.4 mA
			11 0001_B	270.9 mA	348.8 mA
			11 0010_B	278.3 mA	358.1 mA
			11 0011_B	285.8 mA	367.5 mA
			11 0100_B	293.2 mA	376.8 mA
			11 0101_B	300.6 mA	386.2 mA
			11 0110_B	308.1 mA	395.6 mA
			11 0111_B	315.5 mA	405.0 mA
			11 1000_B	323.0 mA	414.4 mA
			11 1001_B	330.4 mA	423.8 mA
			11 1010_B	337.8 mA	433.1 mA
			11 1011_B	345.3 mA	442.5 mA

(table continues...)

Table 26 (continued) General control register 9 (000 1001_B) Reset value: 0000 1111_B

			11 1100_B	352.7 mA	451.9 mA
			11 1101_B	360.2 mA	461.3 mA
			11 1110_B	367.6 mA	470.6 mA
			11 1111_B	375.0 mA	480.0 mA

9.2.10 General control register 10

Table 27 General control register 10 (000 1010_B) Reset value: 0000 1111_B

7	6	5	4	3	2	1	0
TFBEMF		**IDISCHGM**					
rw		rw					

Field	Bits	Type	Description		
TFBEMF	[7:6]	rw	**Back EMF filter time** 00_B 0.5 µs (def.) 01_B 1 µs 10_B 2 µs 11_B 3 µs		
IDISCHGM	[5:0]	rw	**Middle discharge current of HB1 - HB3**		
				IGx_SEL = 0_B	IGx_SEL = 1_B
			00 0000_B	11.6 mA	11.6 mA
			00 0001_B	14.8 mA	15.8 mA
			00 0010_B	18.1 mA	20.1 mA
			00 0011_B	21.3 mA	24.3 mA
			00 0100_B	24.5 mA	28.5 mA
			00 0101_B	27.7 mA	32.7 mA
			00 0110_B	31.0 mA	37.0 mA
			00 0111_B	34.2 mA	41.2 mA
			00 1000_B	37.4 mA	45.4 mA
			00 1001_B	40.6 mA	49.7 mA
			00 1010_B	43.9 mA	53.9 mA
			00 1011_B	47.1 mA	58.1 mA
			00 1100_B	50.3 mA	62.4 mA
			00 1101_B	53.6 mA	66.6 mA
			00 1110_B	56.8 mA	70.8 mA
			00 1111_B (def.)	60.0 mA	75.0 mA

(table continues...)

Table 27 (continued) General control register 10 (000 1010_B) Reset value: 0000 1111_B

			01 0000_B	65.4 mA	82.1 mA
			01 0001_B	70.8 mA	89.3 mA
			01 0010_B	76.1 mA	96.4 mA
			01 0011_B	81.5 mA	103.5 mA
			01 0100_B	86.9 mA	111.6 mA
			01 0101_B	92.3 mA	117.8 mA
			01 0110_B	97.6 mA	124.9 mA
			01 0111_B	103.0 mA	132.0 mA
			01 1000_B	108.4 mA	139.1 mA
			01 1001_B	113.8 mA	146.3 mA
			01 1010_B	119.1 mA	153.4 mA
			01 1011_B	124.5 mA	160.5 mA
			01 1100_B	129.9 mA	167.6 mA
			01 1101_B	135.3 mA	174.8 mA
			01 1110_B	140.6 mA	181.9 mA
			01 1111_B	146.0 mA	189.0 mA
			10 0000_B	152.9 mA	197.8 mA
			10 0001_B	159.8 mA	206.6 mA
			10 0010_B	166.6 mA	215.4 mA
			10 0011_B	173.5 mA	224.2 mA
			10 0100_B	180.4 mA	233.1 mA
			10 0101_B	187.2 mA	241.9 mA
			10 0110_B	194.1 mA	250.7 mA
			10 0111_B	201.0 mA	259.5 mA
			10 1000_B	207.9 mA	268.3 mA
			10 1001_B	214.8 mA	277.1 mA
			10 1010_B	221.6 mA	285.9 mA
			10 1011_B	228.5 mA	294.7 mA
			10 1100_B	235.4 mA	303.5 mA
			10 1101_B	242.3 mA	312.3 mA
			10 1110_B	249.1 mA	321.2 mA
			10 1111_B	256.0 mA	330.0 mA
			11 0000_B	263.4 mA	339.4 mA
			11 0001_B	270.9 mA	348.8 mA

(table continues...)

Table 27 (continued) General control register 10 (000 1010$_B$) Reset value: 0000 1111$_B$

			11 0010$_B$	278.3 mA	358.1 mA
			11 0011$_B$	285.8 mA	367.5 mA
			11 0100$_B$	293.2 mA	376.8 mA
			11 0101$_B$	300.6 mA	386.2 mA
			11 0110$_B$	308.1 mA	395.6 mA
			11 0111$_B$	315.5 mA	405.0 mA
			11 1000$_B$	323.0 mA	414.4 mA
			11 1001$_B$	330.4 mA	423.8 mA
			11 1010$_B$	337.8 mA	433.1 mA
			11 1011$_B$	345.3 mA	442.5 mA
			11 1100$_B$	352.7 mA	451.9 mA
			11 1101$_B$	360.2 mA	461.3 mA
			11 1110$_B$	367.6 mA	470.6 mA
			11 1111$_B$	375.0 mA	480.0 mA

9.2.11 General control register 11

Table 28 General control register 11 (000 1011$_B$) Reset value: 0000 1111$_B$

7	6	5	4	3	2	1	0
TFVDS			**IDISCHG_ST**				
rw			rw				

Field	Bits	Type	Description		
TFVDS	[7:5]	rw	**Drain - source overvoltage filter time of HB1 - HB3**		
			000$_B$ 0.25 µs (def.)		
			001$_B$ 0.50 µs		
			010$_B$ 0.75 µs		
			011$_B$ 1.00 µs		
			100$_B$ 1.25 µs		
			101$_B$ 1.50 µs		
			110$_B$ 1.75 µs		
			111$_B$ 2.00 µs		
IDISCHG_ST	[4:0]	rw	**Static discharge current of HB1 - HB3**		
				IGx_SEL = 0$_B$	IGx_SEL = 1$_B$
			0 0000$_B$	14.8 mA	15.8 mA

(table continues...)

Table 28 (continued) General control register 11 (000 1011_B) Reset value: 0000 1111_B

			$0\ 0001_B$	21.3 mA	24.3 mA
			$0\ 0010_B$	27.7 mA	32.7 mA
			$0\ 0011_B$	34.3 mA	41.2 mA
			$0\ 0100_B$	40.6 mA	49.7 mA
			$0\ 0101_B$	47.1 mA	58.1 mA
			$0\ 0110_B$	53.6 mA	66.6 mA
			$0\ 0111_B$	60.0 mA	75.0 mA
			$0\ 1000_B$	70.8 mA	89.3 mA
			$0\ 1001_B$	81.5 mA	103.5 mA
			$0\ 1010_B$	92.3 mA	117.8 mA
			$0\ 1011_B$	103.0 mA	132.0 mA
			$0\ 1100_B$	113.8 mA	146.3 mA
			$0\ 1101_B$	124.5 mA	160.5 mA
			$0\ 1110_B$	135.3 mA	174.8 mA
			$0\ 1111_B$ (def.)	146.0 mA	189.0 mA
			$1\ 0000_B$	159.8 mA	206.6 mA
			$1\ 0001_B$	173.5 mA	224.2 mA
			$1\ 0010_B$	187.2 mA	241.9 mA
			$1\ 0011_B$	201.0 mA	259.5 mA
			$1\ 0100_B$	214.8 mA	277.1 mA
			$1\ 0101_B$	228.5 mA	294.7 mA
			$1\ 0110_B$	242.3 mA	312.3 mA
			$1\ 0111_B$	256.0 mA	330.0 mA
			$1\ 1000_B$	270.9 mA	348.8 mA
			$1\ 1001_B$	285.8 mA	367.5 mA
			$1\ 1010_B$	300.6 mA	386.2 mA
			$1\ 1011_B$	315.5 mA	405.0 mA
			$1\ 1100_B$	330.4 mA	423.8 mA
			$1\ 1101_B$	345.3 mA	442.5mA
			$1\ 1110_B$	360.20 mA	461.3 mA
			$1\ 1111_B$	375.0 mA	480.0 mA

9.2.12 General control register 12

Table 29 General control register 12 (000 1100$_B$) Reset value: 0001 1011$_B$

7	6	5	4	3	2	1	0
RES	**IPREDISCHG_T_XT**	**TBLK**			**TCCP**		
r	rw	rw			rw		

Field	Bits	Type	Description
RES	7	r	**Reserved. Always read as 0**
IPREDISCHG_T_XT	6	rw	**Extended pre-discharge time** 0_B keep the pre-discharge time defined by IPREDISCHG_T (default) 1_B extend the pre-discharge time to 300ns when IPREDISCHG_T = 00_B 350 ns when IPREDISCHG_T = 01_B 400 ns when IPREDISCHG_T = 10_B 450 ns when IPREDISCHG_T = 11_B
TBLK	[5:3]	rw	**Blank time tBLANK for HB1 - HB3** 000_B 0.5 µs 001_B 1.0 µs 010_B 1.5 µs 011_B 2.0 µs (def.) 100_B 2.5 µs 101_B 3.0 µs 110_B 3.5 µs 111_B 4.0 µs
TCCP	[2:0]	rw	**Cross current protection tCCP for HB1 - HB3** 000_B 0.5 µs 001_B 1.0 µs 010_B 1.5 µs 011_B 2.0 µs (def.) 100_B 2.5 µs 101_B 3.0 µs 110_B 3.5 µs 111_B 4.0 µs

9.2.13 General control register 13

Table 30 General control register 13 (000 1101$_B$) Reset value: 0000 0011$_B$

7	6	5	4	3	2	1	0
RES	**LSAFW_CFG**	**LSAFW**		**VSMOV_CFG**	**VSM_COVUVTH**		

(table continues...)

Table 30 (continued) General control register 13 (000 1101_B) Reset value: 0000 0011_B

r	rw	rw	rw	rw

Field	Bits	Type	Description
RES	7	r	**Reserved. Always read as 0**
LSAFW_CFG	6	rw	**Overvoltage low-side freewheeling enable bit** 0_B switch off MOSFETs if VSMOV = 1 (default) 1_B activate low-side freewheeling if VSMOV = 1
LSAFW	[5:4]	rw	**Low-side freewheeling set up bit:** 00_B all low-side MOSFETs are switched on for freewheeling if VSMOV = 1 (default) 01_B only LS1 is switched on for freewheeling if VSMOV = 1 10_B only LS2 is switched on for freewheeling if VSMOV = 1 11_B only LS3 is switched on for freewheeling if VSMOV = 1
VSMOV_CFG	3	rw	**Configurable overvoltage/undervoltage enable bit:** 0_B when VSM reaches VSM_COVUVTH, the VSMOV is set and the overvoltage event is reported in GEF (default) 1_B when VSM reaches VSM_COVUVTH, the overvoltage event is ignored
VSM_COVUVTH	[2:0]	rw	**Configurable overvoltage/undervoltage thresholds:** 000_B OV: 56 V, UV: 18.5 V 001_B OV: 58 V, UV: 18.5 V 010_B OV: 60 V, UV: 18.5 V 011_B OV: 62 V, UV: 18.5 V (default) 100_B OV: 51 V, UV: 7.0 V 101_B keep the latest configuration settings 110_B keep the latest configuration settings 111_B keep the latest configuration settings

9.3 Status registers

- One 16-bit SPI command consists of two bytes (see Figure 18):
  - The 7-bit address and one additional bit for the register access mode and
  - Following the data byte
- There are two different bit types:
  - 'r' = READ: read only bits (or reserved bits)
  - 'rc' = READ/CLEAR: readable and clearable bits
- Reading a register is done word wise by setting the SPI bit OP to 0 (= read only)
- Clearing a register is done word wise by setting the SPI bit OP to 1. No single bits can be cleared
- The SPI status registers are in general not cleared automatically. It must be done by the microcontroller via SPI command

Table 31 General control register 14 (010 1011B) Reset value: 0000 0000B

7	6	5	4	3	2	1	0
RES	**RES**	**RES**	**RES**	**RES**	**BEMF_PROCESSING_EN**	**BEMF_BT_TFILT_SEL**	
r	r	r	r	r	rw	rw	

Field	Bits	Type	Description
RES	7	r	**Reserved. Always read as 0**
RES	6	r	**Reserved. Always read as 0**
RES	5	r	**Reserved. Always read as 0**
RES	4	r	**Reserved. Always read as 0**
RES	3	r	**Reserved. Always read as 0**
BEMF_PROCESSING_EN	2	rw	**BEMF processing enable bit:** 0_B BEMF processing algorithm is disabled (default) 1_B BEMF processing algorithm is enabled
BEMF_BT_TFILT_SEL	[1:0]	rw	**HB Blanking time for BEMF comparator output signal** 00_B 6 µs (default) 01_B 8 µs 10_B 12 µs 11_B 16 µs

9.3.1 General status register

Table 32 General status register (000 1110_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
RES	**DSOV**	**SUPE**	**INE**	**TE**	**nPOR**	**ST**	**SPIE**
r	**r**	**r**	**r**	**r**	**rc**	**rc**	**rc**

Field	Bits	Type	Description
RES	7	r	**Reserved. Always read as 0**
DSOV	6	r	**VDS monitoring bit** 0_B no VDS error is detected (default) 1_B VDS error is detected
SUPE	5	r	**Supply error bit** 0_B no supply error is detected (default) 1_B supply error is detected

(table continues...)

Table 32 (continued) General status register (000 1110$_B$) Reset value: 0000 0000$_B$

INE	4	r	**Input error bit** 0_B no input error is detected (default) 1_B input error is detected
TE	3	r	**Temperature error bit** 0_B no thermal shutdown and no thermal warning is detected (default) 1_B a thermal shutdown or a thermal warning is detected
nPOR	2	rc	**Negative Power-On-Reset bit** 0_B a Power-On-Reset is detected (default) 1_B no Power-On-Reset (after clear)
ST	1	rc	**Stop mode bit** 0_B The device is not in stop mode state (default) 1_B The device is in stop mode state
SPIE	0	rc	**SPI protocol error bit** 0_B No SPI protocol error is detected (default) 1_B A SPI protocol error is detected

9.3.2 Global status register 1

Table 33 Global status register 1 (000 1111$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
RES	**TW**	**TSD**	**CP1UV**	**CP2UV**	**VSMOV_PROT**	**VSMOV**	**VSMUV**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
RES	7	rc	**Reserved. Always read as 0**
TW	6	rc	**Thermal warning** 0_B no thermal warning is detected (default) 1_B a thermal warning is detected
TSD	5	rc	**Thermal shutdown** 0_B no thermal shutdown is detected (default) 1_B a thermal shutdown is detected
CP1UV	4	rc	**Charge pump 1 undervoltage** 0_B no charge pump 1 undervoltage detected (default) 1_B charge pump 1 undervoltage detected
CP2UV	3	rc	**Charge pump 2 undervoltage** 0_B no charge pump 2 undervoltage detected (default) 1_B charge pump 2 undervoltage detected

(table continues...)

Table 33 (continued) Global status register 1 (000 1111_B) Reset value: 0000 0000_B

VSMOV_PROT	2	rc	**VSM overvoltage Bit** 0_B VSM doesn't reach the hard OV threshold (default) 1_B VSM reaches the hard OV threshold
VSMOV	1	rc	**VSM overvoltage Bit** 0_B no VSM Overvoltage is detected (default) 1_B VSM Overvoltage is detected
VSMUV	0	rc	**VSM undervoltage Bit** 0_B no VSM Undervoltage is detected (default) 1_B VSM Undervoltage is detected

9.3.3 Global status register 2

Table 34 Global status register 2 (001 0000_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
WDMON		**LS3DSOV**	**HS3DSOV**	**LS2DSOV**	**HS2DSOV**	**LS1DSOV**	**HS1DSOV**
r		rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
WDMON	[7:6]	r	**Watchdog monitoring** 00_B WD timer is between [0%;25%] of the WD period (default) 01_B WD timer is between [25%;50%] of the WD period 10_B WD timer is between [50%;75%] of the WD period 11_B WD timer is between [75%;100%] of the WD period
LS3DSOV	5	rc	**Drain-source overvoltage on low side 3** 0_B no overvoltage on DS of low side 3 (default) 1_B overvoltage on DS of low side 3 is detected
HS3DSOV	4	rc	**Drain-source overvoltage on high side 3** 0_B no overvoltage on DS of high side 3 (default) 1_B overvoltage on DS of high side 3 is detected
LS2DSOV	3	rc	**Drain-source overvoltage on low side 2** 0_B no overvoltage on DS of low side 2 (default) 1_B overvoltage on DS of low side 2 is detected
HS2DSOV	2	rc	**Drain-source overvoltage on high side 2** 0_B no overvoltage on DS of high side 2 (default) 1_B overvoltage on DS of high side 2 is detected
LS1DSOV	1	rc	**Drain-source overvoltage on low side 1** 0_B no overvoltage on DS of low side 1 (default) 1_B overvoltage on DS of low side 1 is detected

(table continues...)

Table 34 (continued) Global status register 2 (001 0000_B) Reset value: $0000\ 0000_B$

HS1DSOV	0	rc	**Drain-source overvoltage on high side 1** 0_B no overvoltage on DS of high side 1 (default) 1_B overvoltage on DS of high side 1 is detected

9.3.4 Global status register 3

Table 35 Global status register 3 (001 0001_B) Reset value: $0000\ 0000_B$

7	6	5	4	3	2	1	0
RES	**RES**	**INE1**	**INE2**	**INE3**	**HS3VOUT**	**HS2VOUT**	**HS1VOUT**
r	r	rc	rc	rc	r	r	r

Filed	Bits	Type	Description
RES	[7:6]	r	**Reserved. Always read as 0**
INE1	5	rc	**Input 1 error** 0_B no input 1 error is detected (default) 1_B IH1 and IL1 are high
INE2	4	rc	**Input 2 error** 0_B no input 2 error is detected (default) 1_B IH2 and IL2 are high
INE3	3	rc	**Input 3 error** 0_B no input 1 error is detected (default) 1_B IH3 and IL3 are high
HS3VOUT	2	r	**Voltage level at SH3 when (IH3, IL3) = (0,0)** 0_B low: |VSH3 - GND| < VSHL 1_B high: |VSH3 - GND| > VSHL Note: HB3VOUT = 0 if (IH3, IL3) = (1,0) or (0,1).
HS2VOUT	1	r	**Voltage level at SH2 when (IH2, IL2) = (0,0)** 0_B low: |VSH2 - GND| < VSHL 1_B high: |VSH2 - GND| > VSHL Note: HB2VOUT = 0 if (IH2, IL2) = (1,0) or (0,1).
HS1VOUT	0	r	**Voltage level at SH1 when (IH1, IL1) = (0,0)** 0_B low: |VSH1 - GND| < VSHL 1_B high: |VSH1 - GND| > VSHL Note: HB1VOUT = 0 if (IH1, IL1) = (1,0) or (0,1).

9.3.5 Global status register 4

Table 36 Global status register 4 (001 0010_B) Reset value: $0000\ 0000_B$

7	6	5	4	3	2	1	0

(table continues...)

Table 36 (continued) Global status register 4 (001 0010$_B$) Reset value: 0000 0000$_B$

RES	BEMF3	BEMF2	BEMF1
r	r	r	r

Field	Bits	Type	Description
RES	[7:3]	r	**Reserved. Always read as 0**
BEMF3	2	r	**Signal for BEMF3** 1_B VSHM3 > (VSHM1 + VSHM2)/2 0_B VSHM3 < (VSHM1 + VSHM2)/2 Note: If the BEMF_POCESSING_EN bit is set to 0_B, the BEMF3 will be real time signal. If the BEMF_POCESSING_EN bit is set to 1_B, the BEMF3 will be the output signal with the post-processing algorithm. When BD_EN = 0_B, the BEMF3 = 0_B
BEMF2	1	r	**Signal for BEMF2** 1_B VSHM2 > (VSHM1 + VSHM3)/2 0_B VSHM2 < (VSHM1 + VSHM3)/2 Note: If the BEMF_POCESSING_EN bit is set to 0_B, the BEMF2 will be real time signal. If the BEMF_POCESSING_EN bit is set to 1_B, the BEMF2 will be the output signal with the post-processing algorithm. When BD_EN = 0_B, the BEMF2 = 0_B
BEMF1	0	r	**Signal for BEMF1** 1_B VSHM1 > (VSHM2 + VSHM3)/2 0_B VSHM1 < (VSHM2 + VSHM3)/2 Note: If the BEMF_POCESSING_EN bit is set to 0_B, the BEMF1 will be real time signal. If the BEMF_POCESSING_EN bit is set to 1_B, the BEMF1 will be the output signal with the post-processing algorithm. When BD_EN = 0_B, the BEMF1 = 0_B

9.3.6 Effective MOSFET turn-on/-off delay

Table 37 Effective high-side MOSFET turn-on delay PWM1 (001 0011$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0

(table continues...)

Table 37 (continued) Effective high-side MOSFET turn-on delay PWM1 (001 0011_B) Reset value: 0000 0000_B

TDONHS1
r

Field	Bits	Type	Description
TDONHS1	[7:0]	r	**Effective high-side MOSFET turn-on delay of PWM channel 1** [1)] HBFREQ bit is 1: effective turn-on delay = 53.3 ∗ TDONHS1[7:0]$_D$ ns HBFREQ bit is 0: effective turn-on delay = 26.7 ∗ TDONHS1[7:0]$_D$ ns Default value: 0_B

Table 38 Effective high-side MOSFET turn-off delay PWM1 (001 0100_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TDOFFHS1							
r							

Field	Bits	Type	Description
TDOFFHS1	[7:0]	r	**Effective high-side MOSFET turn-off delay of PWM channel 1** [3)] HBFREQ bit is 1: effective turn-off delay = 53.3 ∗ TDOFFHS1[7:0]$_D$ ns HBFREQ bit is 0: effective turn-off delay = 26.7 ∗ TDOFFHS1[7:0]$_D$ ns Default value: 0_B

Table 39 Effective low-side MOSFET turn-on delay PWM1 (001 0101_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TDONLS1							
r							

Field	Bits	Type	Description
TDONLS1	[7:0]	r	**Effective low-side MOSFET turn-on delay of PWM channel 1** [2)] HBFREQ bit is 1: effective turn-on delay = 53.3 ∗ TDONLS1[7:0]$_D$ ns HBFREQ bit is 0: effective turn-on delay = 26.7 ∗ TDONLS1[7:0]$_D$ ns Default value: 0_B

Table 40 Effective low-side MOSFET turn-off delay PWM1 (001 0110_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TDOFFLS1							
r							

Field	Bits	Type	Description

(table continues...)

Table 40 (continued) Effective low-side MOSFET turn-off delay PWM1 (001 0110_B) Reset value: 0000 0000_B

TDOFFLS1	[7:0]	r	**Effective low-side MOSFET turn-off delay of PWM channel 1** [4] HBFREQ bit is 1: effective turn-off delay = 53.3 ∗ TDOFFLS1[7:0]$_D$ ns HBFREQ bit is 0: effective turn-off delay = 26.7 ∗ TDOFFLS1[7:0]$_D$ ns Default value: 0_B

Table 41 Effective high-side MOSFET turn-on delay PWM2 (001 0111_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TDONHS2							
r							

Field	Bits	Type	Description
TDONHS2	[7:0]	r	**Effective high-side MOSFET turn-on delay of PWM channel 2** [1] HBFREQ bit is 1: effective turn-on delay = 53.3 ∗ TDONHS2[7:0]$_D$ ns HBFREQ bit is 0: effective turn-on delay = 26.7 ∗ TDONHS2[7:0]$_D$ ns Default value: 0_B

Table 42 Effective high-side MOSFET turn-off delay PWM2 (001 1000_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TDOFFHS2							
r							

Field	Bits	Type	Description
TDOFFHS2	[7:0]	r	**Effective high-side MOSFET turn-off delay of PWM channel 2** [3] HBFREQ bit is 1: effective turn-off delay = 53.3 ∗ TDOFFHS2[7:0]$_D$ ns HBFREQ bit is 0: effective turn-off delay = 26.7 ∗ TDOFFHS2[7:0]$_D$ ns Default value: 0_B

Table 43 Effective low-side MOSFET turn-on delay PWM2 (001 1001_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TDONLS2							
r							

Field	Bits	Type	Description
TDONLS2	[7:0]	r	**Effective low-side MOSFET turn-on delay of PWM channel 2** [2] HBFREQ bit is 1: effective turn-on delay = 53.3 ∗ TDONLS2[7:0]$_D$ ns HBFREQ bit is 0: effective turn-on delay = 53.3 ∗ 127 + 26.7 ∗ TDONLS2[7:0]$_D$ ns Default value: 0_B

Table 44 Effective low-side MOSFET turn-off delay PWM2 (001 1010$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TDOFFLS2							
r							

Field	Bits	Type	Description
TDOFFLS2	[7:0]	r	**Effective low-side MOSFET turn-off delay of PWM channel 2** [4] HBFREQ bit is 1: effective turn-off delay = 53.3 ∗ TDOFFLS2[7:0]$_D$ ns HBFREQ bit is 0: effective turn-off delay = 26.7 ∗ TDOFFLS2[7:0]$_D$ ns Default value: 0$_B$

Table 45 Effective high-side MOSFET turn-on delay PWM3 (001 1011$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TDONHS3							
r							

Field	Bits	Type	Description
TDONHS3	[7:0]	r	**Effective high-side MOSFET turn-on delay of PWM channel 3** [1] HBFREQ bit is 1: effective turn-on delay = 53.3 ∗ TDONHS3[7:0]$_D$ ns HBFREQ bit is 0: effective turn-on delay = 26.7 ∗ TDONHS3[7:0]$_D$ ns Default value: 0$_B$

Table 46 Effective high-side MOSFET turn-off delay PWM3 (001 1100$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TDOFFHS3							
r							

Field	Bits	Type	Description
TDOFFHS3	[7:0]	r	**Effective high-side MOSFET turn-off delay of PWM channel 3** [3] HBFREQ bit is 1: effective turn-off delay = 53.3 ∗ TDOFFHS3[7:0]$_D$ ns HBFREQ bit is 0: effective turn-off delay = 26.7 ∗ TDOFFHS3[7:0]$_D$ ns Default value: 0$_B$

Table 47 Effective low-side MOSFET turn-on delay PWM3 (001 1101$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TDONLS3							
r							

(table continues...)

Table 47 (continued) Effective low-side MOSFET turn-on delay PWM3 (001 1101$_B$) Reset value: 0000 0000$_B$

Field	Bits	Type	Description
TDONLS3	[7:0]	r	**Effective low-side MOSFET turn-on delay of PWM channel 3** [2] HBFREQ bit is 1: effective turn-on delay = 53.3 ∗ TDONLS3[7:0]$_D$ ns HBFREQ bit is 0: effective turn-on delay = 26.7 ∗ TDONLS3[7:0]$_D$ ns Default value: 0$_B$

Table 48 Effective low-side MOSFET turn-off delay PWM3 (001 1110$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TDOFFLS3							
r							

Field	Bits	Type	Description
TDOFFLS3	[7:0]	r	**Effective low-side MOSFET turn-off delay of PWM channel 3** [4] HBFREQ bit is 1: effective turn-off delay = 53.3 ∗ TDOFFLS3[7:0]$_D$ ns HBFREQ bit is 0: effective turn-off delay = 26.7 ∗ TDOFFLS3[7:0]$_D$ ns Default value: 0$_B$

1) Effective high-side turn-on delay is reported if VSHMx rises above VSHL in the duration of TBLANK.
If VSHMx > VSHL when the precharge starts, TDONHSx will be set to 0000 0000$_B$.
If VSHMx < VSHL when TBLANK elapses, TDONHSx will be set to 1111 1111$_B$.
2) Effective low-side turn-on delay is reported if VSHMx drops below VSHH in the duration of TBLANK.
If VSHMx < VSHH when the precharge starts, TDONLSx will be set to 0000 0000$_B$.
If VSHMx > VSHH when TBLANK elapses, TDONLSx will be set to 1111 1111$_B$.
3) Effective high-side turn-off delay is reported if VSHMx drops below VSHH in the duration of TCCP.
If VSHMx >VSHH when TCCP elapses, TDOFFHSx will be set to 1111 1111$_B$.
If VSHMx < VSHH when the predischarge starts, TDOFFHSx will be set to 0000 0000$_B$.
4) Effective low-side turn-off delay is reported if VSHMx rises above VSHL in the duration of TCCP.
If VSHMx < VSHL when TCCP elapses, TDOFFLSx will be set to 1111 1111$_B$.
If VSHMx > VSHL when the predischarge starts, TDOFFLSx will be set to 0000 0000$_B$.

9.3.7 Effective MOSFET rise/fall times

Table 49 Effective high-side MOSFET rise time of PWM1 (001 1111$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TRISEHS1							
r							

Field	Bits	Type	Description

(table continues...)

Table 49 (continued) Effective high-side MOSFET rise time of PWM1 (001 1111_B) Reset value: 0000 0000_B

TRISEHS1	[7:0]	r	**Effective high-side MOSFET rise time of PWM channel 1** [1)] HBFREQ bit is 1: effective rise time = 53.3 ∗ TRISE_HS1[7:0]$_D$ ns HBFREQ bit is 0: effective rise time = 26.7 ∗ TRISE_HS1[7:0]$_D$ ns Default value: 0_B

Table 50 Effective high-side MOSFET fall time of PWM1 (010 0000_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TFALLHS1							
r							

Field	Bits	Type	Description
TFALLHS1	[7:0]	r	**Effective high-side MOSFET fall time of PWM channel 1** [3)] HBFREQ bit is 1: effective fall time = 53.3 ∗ TFALL_HS1[7:0]$_D$ ns HBFREQ bit is 0: effective fall time = 26.7 ∗ TFALL_HS1[7:0]$_D$ ns Default value: 0_B

Table 51 Effective low-side MOSFET rise time of PWM1 (010 0001_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TRISELS1							
r							

Field	Bits	Type	Description
TRISELS1	[7:0]	r	**Effective low-side MOSFET rise time of PWM channel 1** [2)] HBFREQ bit is 1: effective rise time = 53.3 ∗ TRISE_LS1[7:0]$_D$ ns HBFREQ bit is 0: effective rise time = 26.7 ∗ TRISE_LS1[7:0]$_D$ ns Default value: 0_B

Table 52 Effective low-side MOSFET fall time of PWM1 (010 0010_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TFALLLS1							
r							

Field	Bits	Type	Description
TFALLLS1	[7:0]	r	**Effective low-side MOSFET fall time of PWM channel 1** [4)] HBFREQ bit is 1: effective fall time = 53.3 ∗ TFALL_LS1[7:0]$_D$ ns HBFREQ bit is 0: effective fall time = 26.7 ∗ TFALL_LS1[7:0]$_D$ ns Default value: 0_B

Table 53 Effective high-side MOSFET rise time of PWM2 (010 0011_B) Reset value: $0000\ 0000_B$

7	6	5	4	3	2	1	0
TRISEHS2							
r							

Field	Bits	Type	Description
TRISEHS2	[7:0]	r	**Effective high-side MOSFET rise time of PWM channel 2** [1)] HBFREQ bit is 1: effective rise time = 53.3 ∗ TRISE_HS2[7:0]$_D$ ns HBFREQ bit is 0: effective rise time = 26.7 ∗ TRISE_HS2[7:0]$_D$ ns Default value: 0_B

Table 54 Effective high-side MOSFET fall time of PWM2 (010 0100_B) Reset value: $0000\ 0000_B$

7	6	5	4	3	2	1	0
TFALLHS2							
r							

Field	Bits	Type	Description
TFALLHS2	[7:0]	r	**Effective high-side MOSFET fall time of PWM channel 2** [3)] HBFREQ bit is 1: effective fall time = 53.3 ∗ TFALL_HS2[7:0]$_D$ ns HBFREQ bit is 0: effective fall time = 26.7 ∗ TFALL_HS2[7:0]$_D$ ns Default value: 0_B

Table 55 Effective low-side MOSFET rise time of PWM2 (010 0101_B) Reset value: $0000\ 0000_B$

7	6	5	4	3	2	1	0
TRISELS2							
r							

Field	Bits	Type	Description
TRISELS2	[7:0]	r	**Effective low-side MOSFET rise time of PWM channel 2** [2)] HBFREQ bit is 1: effective rise time = 53.3 ∗ TRISE_LS2[7:0]$_D$ ns HBFREQ bit is 0: effective rise time = 26.7 ∗ TRISE_LS2[7:0]$_D$ ns Default value: 0_B

Table 56 Effective low-side MOSFET fall time of PWM2 (010 0110_B) Reset value: $0000\ 0000_B$

7	6	5	4	3	2	1	0
TFALLLS2							
r							

(table continues...)

Table 56 (continued) Effective low-side MOSFET fall time of PWM2 (010 0110_B) Reset value: 0000 0000_B

Field	Bits	Type	Description
TFALLLS2	[7:0]	r	**Effective low-side MOSFET fall time of PWM channel 2** [4] HBFREQ bit is 1: effective fall time = 53.3 ∗ TFALL_LS2[7:0]$_D$ ns HBFREQ bit is 0: effective fall time = 26.7 ∗ TFALL_LS2[7:0]$_D$ ns Default value: 0_B

Table 57 Effective high-side MOSFET rise time of PWM3 (010 0111_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TRISEHS3							
r							

Field	Bits	Type	Description
TRISEHS3	[7:0]	r	**Effective high-side MOSFET rise time of PWM channel 3** [1] HBFREQ bit is 1: effective rise time = 53.3 ∗ TRISE_HS3[7:0]$_D$ ns HBFREQ bit is 0: effective rise time = 26.7 ∗ TRISE_HS3[7:0]$_D$ ns Default value: 0_B

Table 58 Effective high-side MOSFET fall time of PWM3 (010 1000_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TFALLHS3							
r							

Field	Bits	Type	Description
TFALLHS3	[7:0]	r	**Effective high-side MOSFET fall time of PWM channel 3** [3] HBFREQ bit is 1: effective fall time = 53.3 ∗ TFALL_HS3[7:0]$_D$ ns HBFREQ bit is 0: effective fall time = 26.7 ∗ TFALL_HS3[7:0]$_D$ ns Default value: 0_B

Table 59 Effective low-side MOSFET rise time of PWM3 (010 1001_B) Reset value: 0000 0000_B

7	6	5	4	3	2	1	0
TRISELS3							
r							

Field	Bits	Type	Description
TRISELS3	[7:0]	r	**Effective low-side MOSFET rise time of PWM channel 3** [2] HBFREQ bit is 1: effective rise time = 53.3 ∗ TRISE_LS3[7:0]$_D$ ns HBFREQ bit is 0: effective rise time = 26.7 ∗ TRISE_LS3[7:0]$_D$ ns Default value: 0_B

Table 60 Effective low-side MOSFET fall time of PWM3 (010 1010$_B$) Reset value: 0000 0000$_B$

7	6	5	4	3	2	1	0
TFALLLS3							
r							

Field	Bits	Type	Description
TFALLLS3	[7:0]	r	**Effective low-side MOSFET fall time of PWM channel 3** [4)] HBFREQ bit is 1: effective fall time = 53.3 ∗ TFALL_LS3[7:0]$_D$ ns HBFREQ bit is 0: effective fall time = 26.7 ∗ TFALL_LS3[7:0]$_D$ ns Default value: 0$_B$

1) Effective high-side rise time is reported if VSHMx rises above VSHH in the duration of TBLANK.
If VSHMx > VSHH when the precharge starts, TRISE_HSx will be set to 0000 0000$_B$.
If VSHL < VSHMx < VSHH when TBLANK elapses, TRISE_HSx will be set to 1111 1111$_B$.
2) Effective low-side rise time is reported if VSHMx drops blow VSHL in the duration of TBLANK.
If VSHMx < VSHL when the precharge starts, TRISE_LSx will be set to 0000 0000$_B$.
If VSHL < VSHMx < VSHH when TBLANK elapses, TRISE_LSx will be set to 1111 1111$_B$.
3) Effective high-side fall time is reported if VSHMx drops below VSHL in the duration of TCCP.
If VSHH > VSHMx > VSHL when TCCP elapses, TFALL_HSx will be set to 1111 1111$_B$.
If VSHMx < VSHL when the predischarge starts, TFALL_HSx will be set to 0000 0000$_B$.
4) Effective low-side fall time is reported if VSHMx rises above VSHH in the duration of TCCP.
If VSHH < VSHMx < VSHL when TCCP elapses, TFALL_LSx will be set to 1111 1111$_B$.
If VSHMx > VSHH when the predischarge starts, TFALL_LSx will be set to 0000 0000$_B$.

10 Application figure

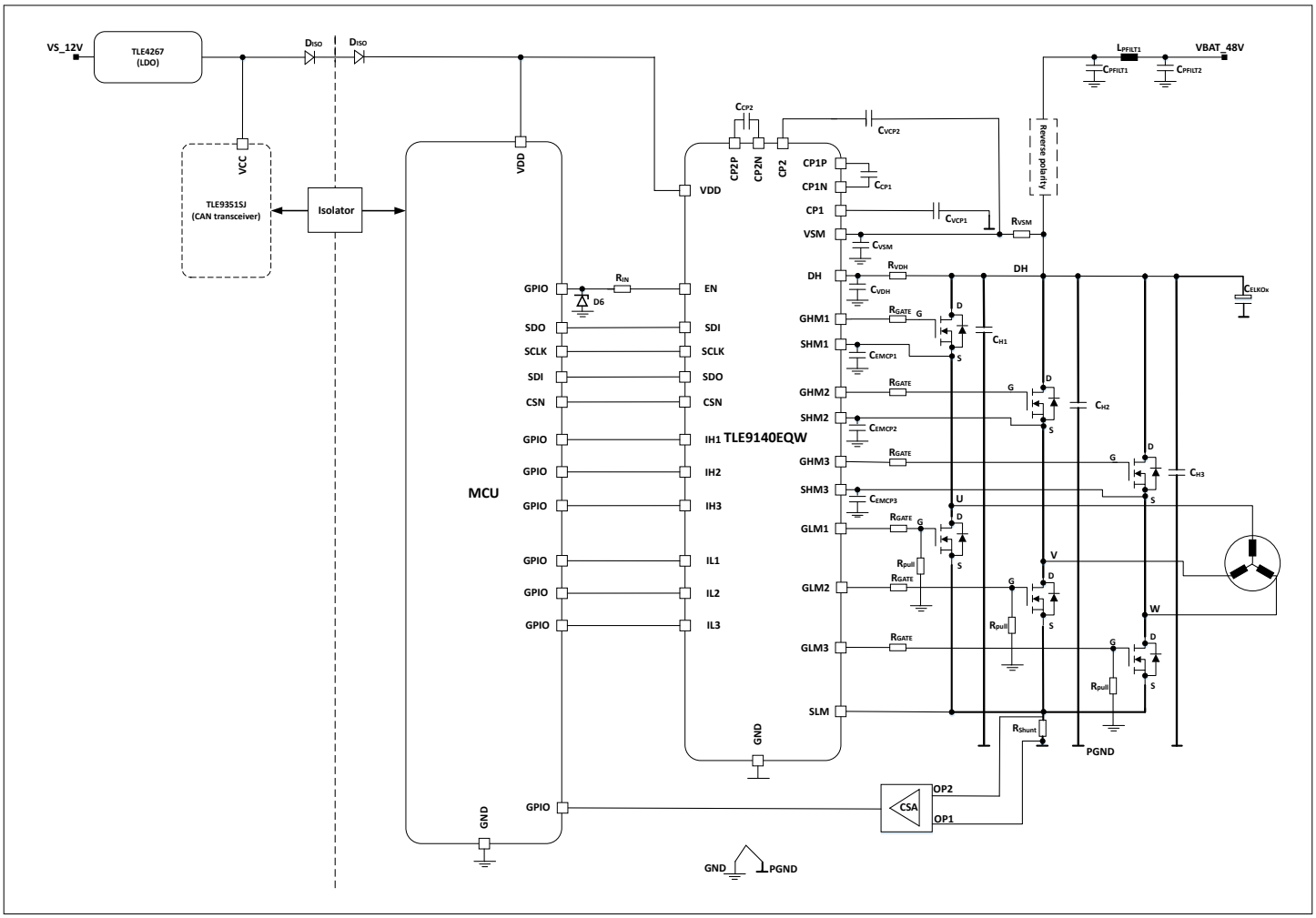

Figure 23 **TLE9140EQW is driven by the general microcontroller for 48 V applications supply concept: isolated 12 V supply for the general MCU with diodes**

10 Application figure

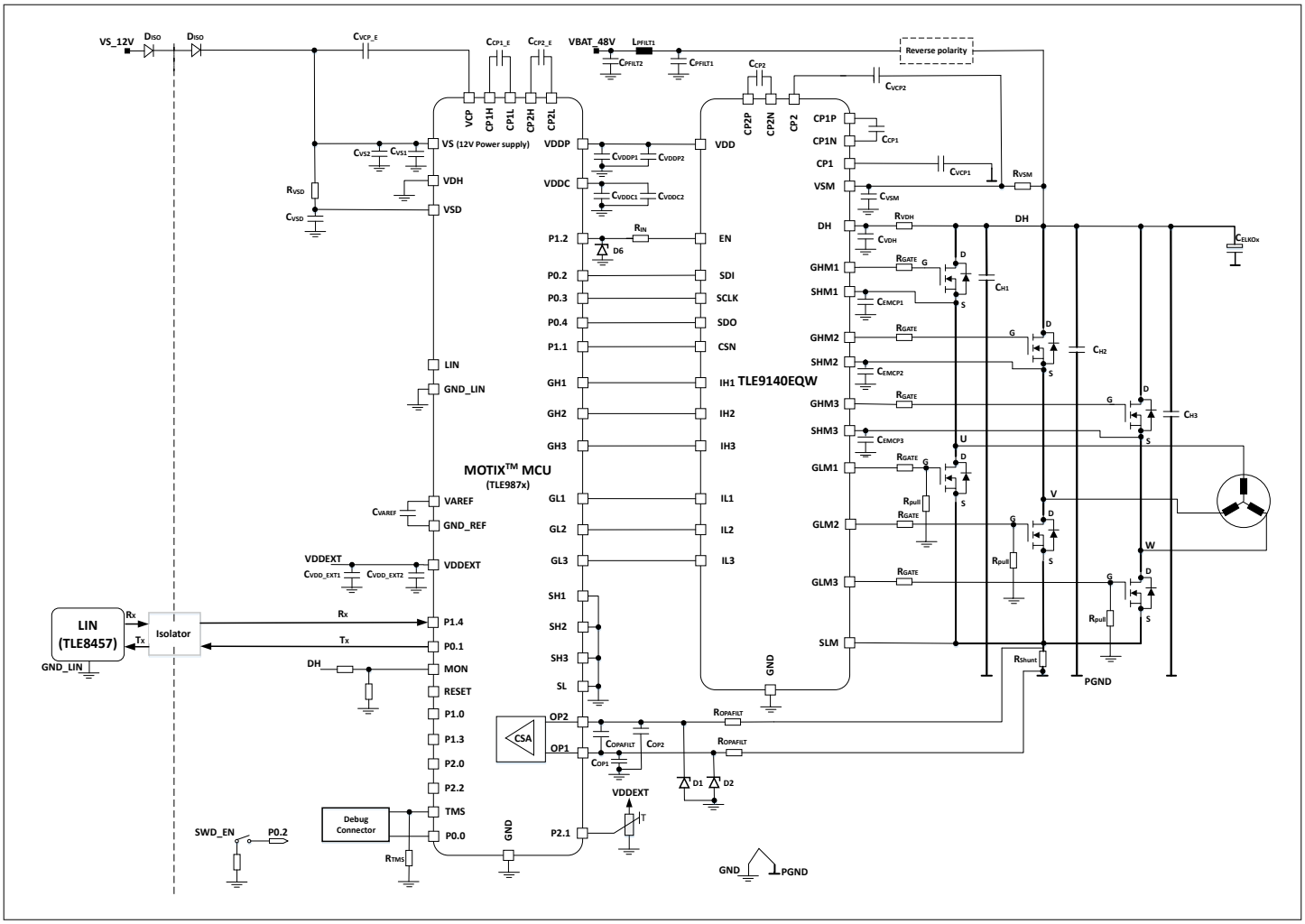

Figure 24 **TLE9140EQW is driven by the MOTIX™ MCU (TLE987x) device supply concept: isolated 12 V supply for the MOTIX™ MCU device with diodes**

10 Application figure

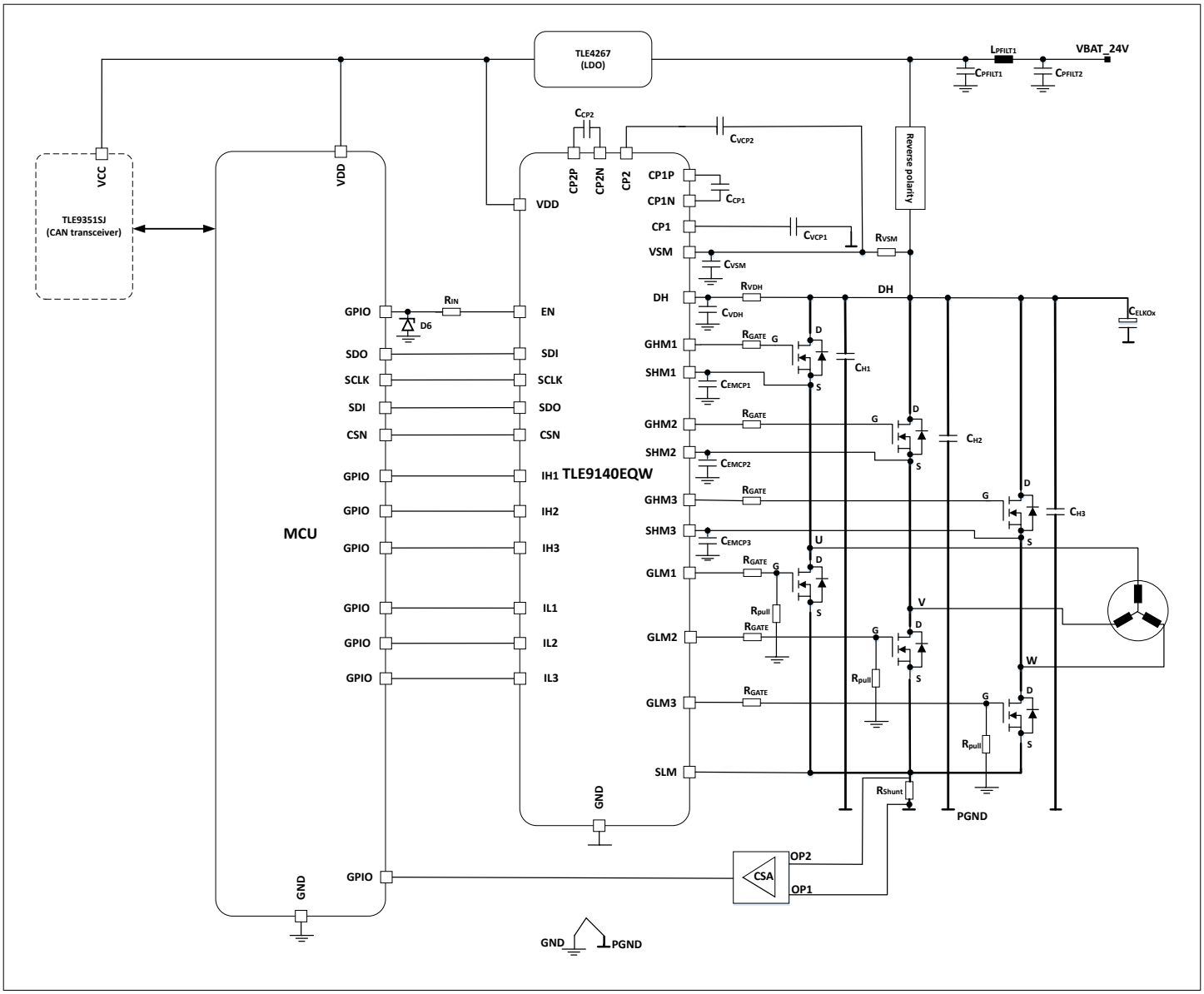

Figure 25 TLE9140EQW is driven by the general MCU for 24 V applications

10 Application figure

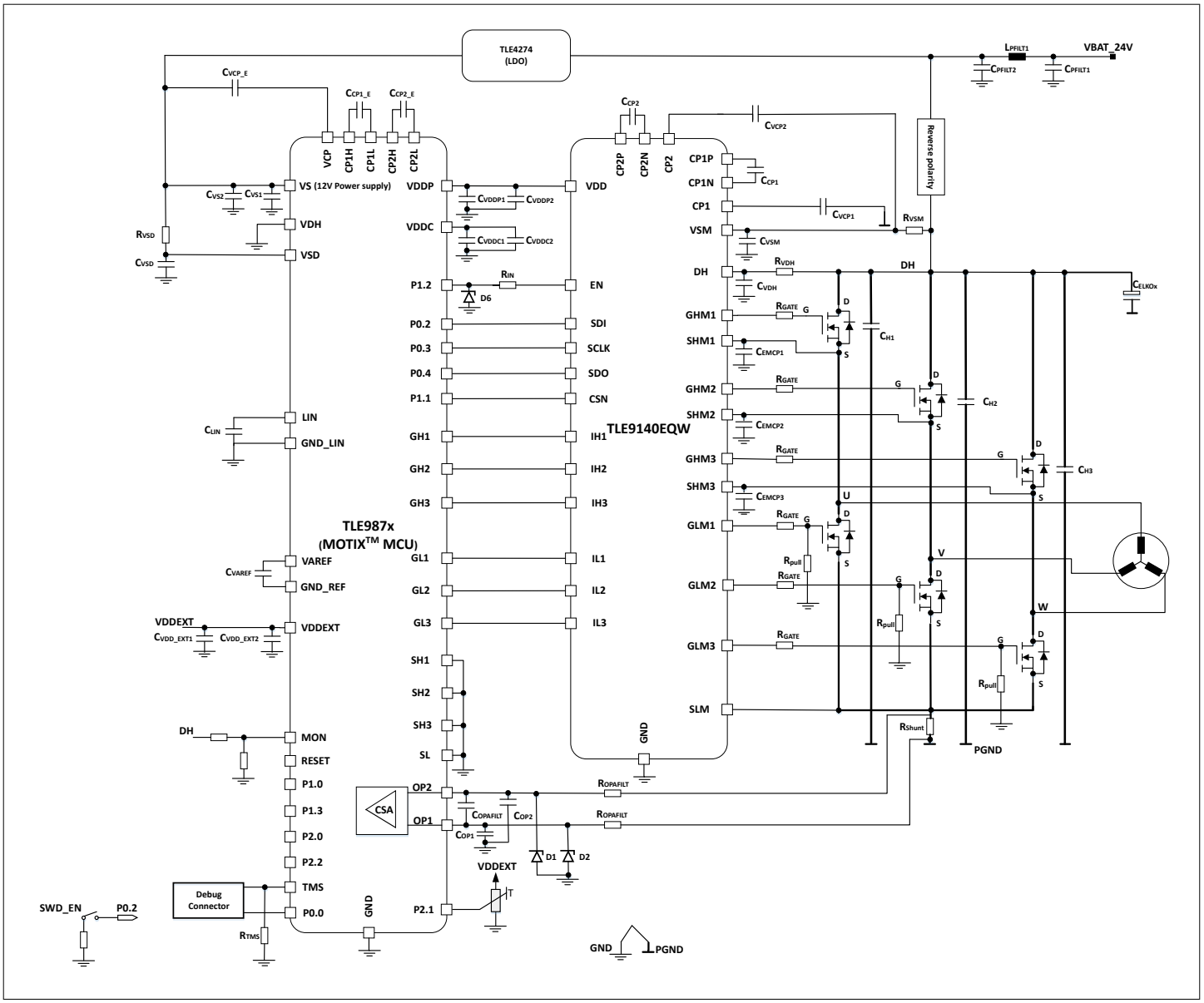

Figure 26 TLE9140EQW is driven by the MOTIX™ MCU (TLE987x) device for 24 V applications

11 Package outline

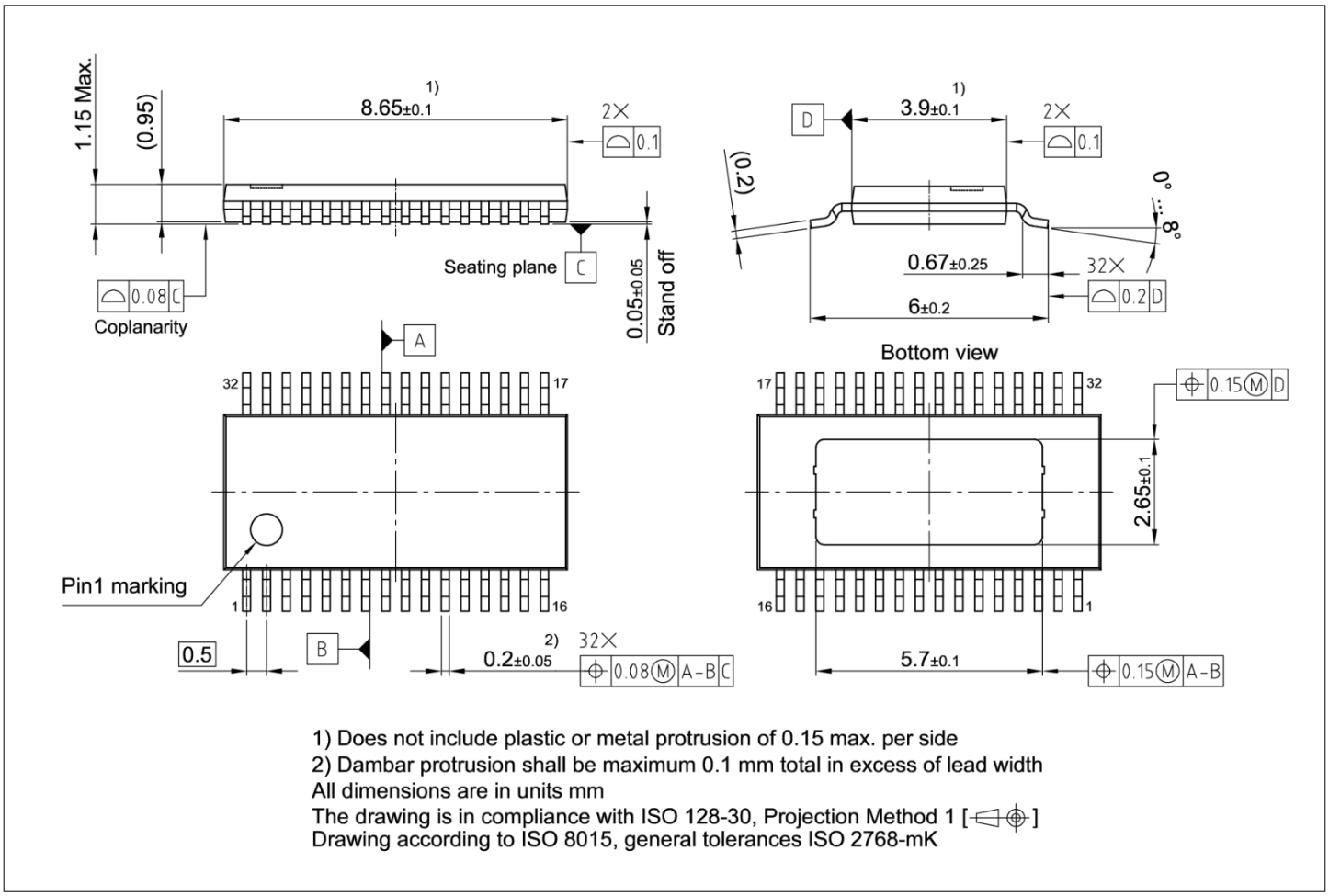

Figure 27 PG-TSDSO-32-1

To meet the world-wide customer requirements for environmental friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (this means lead-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

12 Revision history

Document version	Date of release	Description of changes
1.0	2023-08-07	Datasheet available

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