

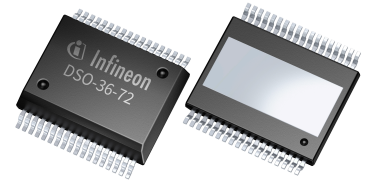
# TLE92464EDHP

## High accuracy four channel low-side solenoid driver IC

Quality Requirement Category: Automotive

### Features

- High current control accuracy
  - $\pm 3$  mA up to 1200 mA initially ( $T_J = -40 - 150^\circ\text{C}$ ,  $V_{\text{BAT}} = 9 - 16$  V)
  - $\pm 0.8\%$  up to 1200 mA including aging ( $T_J = -40 - 150^\circ\text{C}$ ,  $V_{\text{BAT}} = 9 - 16$  V)
  - $\pm 1\%$  up to 1500 mA including aging ( $T_J = -40 - 150^\circ\text{C}$ ,  $V_{\text{BAT}} = 6 - 18$  V)
- Four independent low side channels with integrated MOSFETs ( $R_{\text{DSon}} = 115$  m $\Omega$ )
- Programmable setpoint from 0 mA to 1.5 A
- Load current including dither 1.8 A
- Current in parallel channel mode 2.7 A
- Integrated dither generator with programmable amplitude, frequency and waveform
- 15 bit current setpoint resolution
- Integrated sense resistor  $R_{\text{SHUNT}} = 140$  m $\Omega$
- Excellent immunity to large load supply voltage changes
- Operation down to 3.5 V at VDD pin
- 32 bit SPI with 8 bit CRC and SPI watchdog
- Sophisticated protection and diagnostic functions for each channel in on and off state
  - Independent thermal shutdown for each channel
  - Diagnostic Function (Open Load, Short Circuit Ground, Overcurrent)
  - Voltage monitoring
  - Overtemperature protection
- Two independent current feedback paths
- Integrated system clock with clock watchdog
- Temperature range  $-40^\circ\text{C}$  to  $175^\circ\text{C}$
- Small power package PG-DSO-36-72
- Green Product (RoHS compliant)
- Pb-free (RoHS compliant) package
- AEC-Q100 Grade 0 qualified
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL C



### Potential applications

- Variable force solenoids (e.g. automatic transmission and e-Axle)
- Other constant current solenoids
  - Idle air control
  - Exhaust gas recirculation
  - Vapor management valve
  - Suspension control

## Product validation

Qualified for automotive applications with higher temperature requirements. Product validation according to AEC-Q100, Grade 0.

## Product type & package table

Product type	Package	Marking
TLE92464EDHP	PG-DSO-36 Dual-Gauge (300 mil)	TLE92464EDHP

## Description

The TLE92464EDHP is a flexible, monolithic solenoid driver IC designed for the control of linear solenoids in automatic transmissions, electronic stability control, active suspension and e-Axle applications.

The TLE92464EDHP is a four channel low-side solenoid driver IC with high current accuracy. The device provides an initial current accuracy of less than  $\pm 3$  mA up to 1200 mA current range. Including life time, the current accuracy is less than  $\pm 0.8\%$  up to 1200 mA. Over the full temperature, battery and current range (1500 mA in single channel mode, 2700 mA in parallel channel mode) the control error is less than  $\pm 1\%$ .

The device includes the drive transistors and the current sensing resistors to minimize the number of external components. Target currents from 0 to 1500 mA can be programmed with a resolution of 15 bit. The device supports dither currents up to 1800 mA. The dither generator superimposes a triangular or trapezoidal waveform with programmable amplitude, frequency and shape on the programmed current setpoint. A 32 bit SPI interface is used to control the 4 channels and monitor the status of the diagnostic functions. The SPI communication is secured with an 8 bit CRC and a programmable timeout watchdog.

An active low reset input (RESN) is used to disable all channels and reset the internal registers to the default values. An active high enable pin (EN) enables or disables the output channels without disabling the SPI interface. A fault output pin (FAULTN) signal can be used as external interrupt to the microcontroller whenever a fault is detected.

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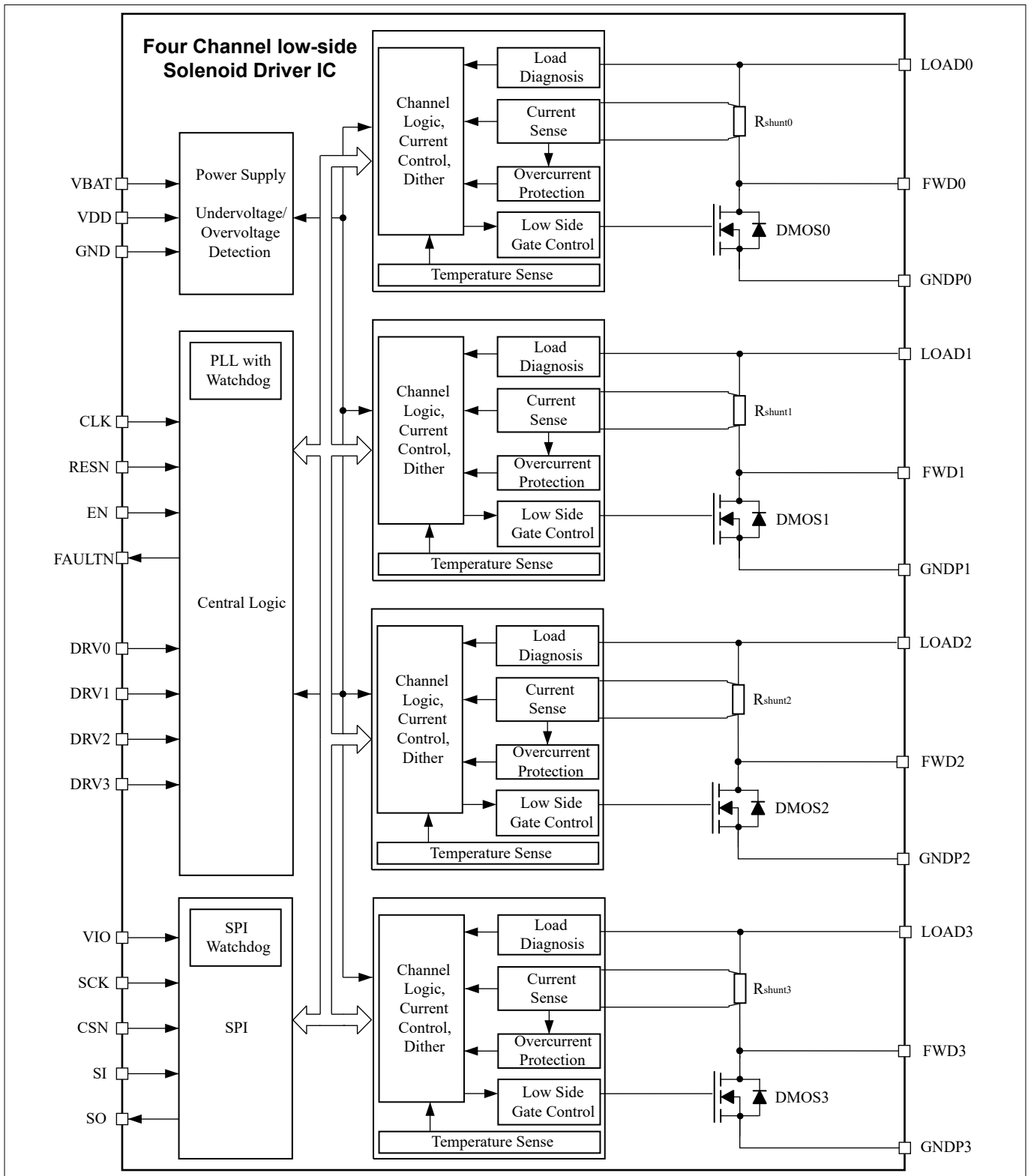
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**Block diagram**

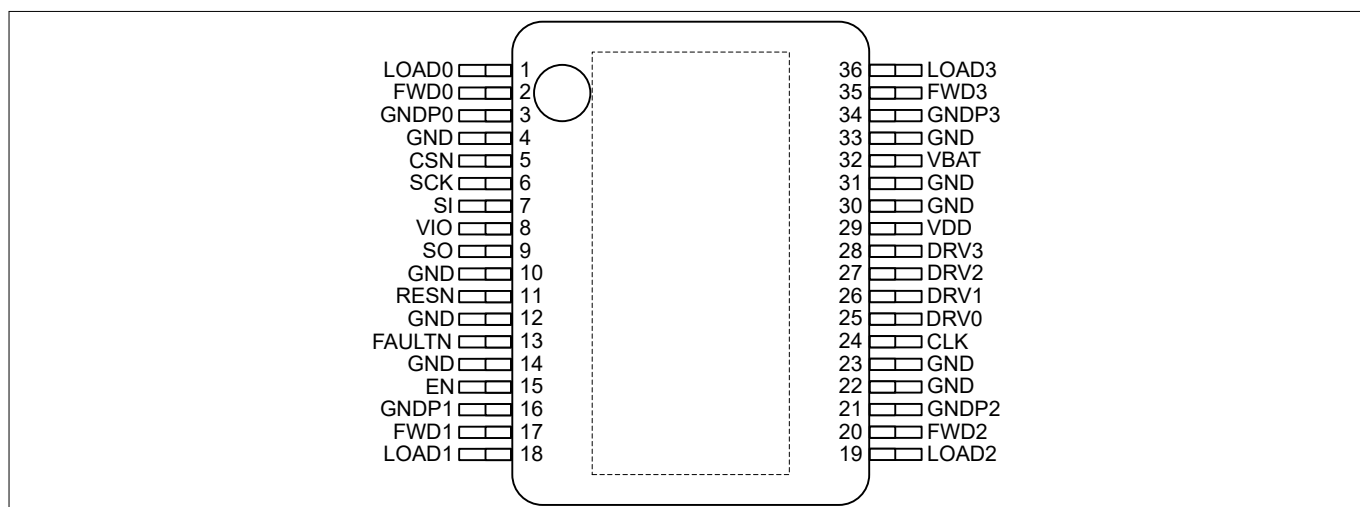
**1 Block diagram**



**Figure 1 Block diagram**

**Pin configuration**

## 2 Pin configuration



**Figure 2 Pin assignment**

### Pin definitions and functions

**Table 1 Pin definition and functions**

Pin	Symbol	Function
1	LOAD0	Output; for channel 0.
2	FWD0	Free wheeling diode; for channel 0.
3	GNDP0	Ground; for channel 0 power stage.
4	GND	Ground; connect to GND.
5	CSN	SPI chip select input; digital input: 3.3 V or 5.0 V logic levels.
6	SCK	SPI clock input; digital input: 3.3 V or 5.0 V logic levels.
7	SI	SPI input; digital input: 3.3 V or 5.0 V logic levels.
8	VIO	Supply SPI Slave Out (SO) pin; connected to 3.3 V or 5.0 V supply.
9	SO	SPI output; push pull output compatible to 3.3 V or 5.0 V logic levels.
10	GND	Ground; signal ground. Internally connected to cooling tab.
11	RESN	Control input; digital input: 3.3 V or 5.0 V logic levels. Active low reset input.
12	GND	Ground; signal ground. Internally connected to cooling tab.
13	FAULTN	Status output; open drain output. In case not used, keep open.
14	GND	Ground; connect to GND.
15	EN	Control input; digital input: 3.3 V or 5.0 V logic levels. Active high enable input.
16	GNDP1	Ground; ground connection for channel 1 power stage.
17	FWD1	Free wheeling diode; for channel 1.
18	LOAD1	Output; for channel 1.
19	LOAD2	Output; for channel 2.

**(table continues...)**

**Pin configuration**

**Table 1 (continued) Pin definition and functions**

<b>Pin</b>	<b>Symbol</b>	<b>Function</b>
20	FWD2	Free wheeling diode; for channel 2.
21	GNDP2	Ground; ground connection for channel 2 power stage.
22	GND	Ground; connect to GND.
23	GND	Ground; signal ground. Internally connected to cooling tab.
24	CLK	Clock input; Main system clock.
25	DRV0	Direct drive input for channel 0: 3.3 V or 5.0 V logical levels.
26	DRV1	Direct drive input for channel 1: 3.3 V or 5.0 V logical levels.
27	DRV2	Direct drive input for channel 2: 3.3 V or 5.0 V logical levels.
28	DRV3	Direct drive input for channel 3: 3.3 V or 5.0 V logical levels.
29	VDD	Supply voltage; supplies digital circuits. Connected to 5.0 V supply voltage.
30	GND	Ground; signal ground. Internally connected to cooling tab.
31	GND	Ground; connect to GND
32	VBAT	Supply voltage; connected to battery voltage with reverse protection diode and filter against EMC.
33	GND	Ground; connect to GND.
34	GNDP3	Ground; for channel 3 power stage.
35	FWD3	Free wheeling diode; for channel 3.
36	LOAD3	Output; for channel 3.
37	Cooling Tap	Connect externally to GND and heat sink area



### 3 Electrical characteristics and parameters

#### 3.1 Absolute maximum ratings

##### 3.1.1 Absolute maximum voltage ratings

**Table 2 Absolute maximum voltage ratings**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Max. supply voltage (VDD)	$V_{DD,max}$	-0.3	–	19	V	
Max. supply voltage (VBAT)	$V_{BAT,max}$	-0.3	–	40	V	
Max. supply voltage (VIO)	$V_{VIO,max}$	-0.3	–	19	V	
Max. digital input pin voltage (CLK, RESN, EN, DRVx, SCK, CSN, SI)	$V_{CLK,max}$ $V_{RESN,max}$ $V_{EN,max}$ $V_{DRVx,max}$ $V_{SCK,max}$ $V_{CSN,max}$ $V_{SI,max}$	-0.3	–	19	V	
Max. open drain output voltage (FAULTN)	$V_{FAULTN,max}$	-0.3	–	19	V	
Max. Push Pull Output (SO)	$V_{SO,max}$	-0.3	–	19	V	
Max. LOADx voltage	$V_{LOADx,max}$	-0.3 <sup>1)</sup>	–	40	V	<sup>1)</sup> During negative pulses ( $V_{LOADx} < -0.3$ V) the maximum energy of $E_{LOADx} =  V_{LOADx} * (I_{LOADx} + I_{FWDx}) * t_{pulse}  \leq 2$ mJ shall not be violated.
Max. FWDx voltage	$V_{FWDx,max}$	-0.3 <sup>1)</sup>	–	40	V	<sup>1)</sup> During negative pulses ( $V_{FWDx} < -0.3$ V) the maximum energy of $E_{FWDx} =  V_{FWDx} * (I_{LOADx} + I_{FWDx}) * t_{pulse}  \leq 2$ mJ shall not be violated.
Max. GNDPx voltage	$V_{GNDPx,max}$	-0.3	–	0.3	V	

**Electrical characteristics and parameters**

**3.1.2 Absolute maximum current ratings**

**Table 3 Absolute maximum current ratings**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Max. current range	$I_{FWDx,max}$ $I_{LOADx,max}$	-2	-	2	A	DC In the case of an active overcurrent shutdown the specification at the LOADx pin can be exceeded.
Max. Output Current (FAULTN)	$I_{FAULTN,max}$	-5	-	0	mA	
Max. output current (SO)	$I_{SO,max}$	-5	-	5	mA	DC
Max. input current (CLK, RESN, EN, DRVx, SCK, CSN, SI)	$I_{CLK,max}$ $I_{RESN,max}$ $I_{EN,max}$ $I_{DRVx,max}$ $I_{SCK,max}$ $I_{CSN,max}$ $I_{SI,max}$	-5	0	5	mA	Maximum allowed forward and reverse current through ESD structure.

**3.1.2.1 TDS\_max\_rating**

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

**3.1.3 Absolute maximum temperature ratings**

**Table 4 Absolute maximum temperature ratings**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction temperature (T <sub>J</sub> )	$T_J$	-40	-	150	°C	
Extended junction temperature (T <sub>J</sub> extended)	$T_{Jext}$	150	-	175	°C	parameter deviations are possible

**(table continues...)**

**Electrical characteristics and parameters**

**Table 4 (continued) Absolute maximum temperature ratings**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Storage temperature (TSTG)	$T_{STG}$	-55	–	150	°C	

### 3.1.4 ESD Robustness

**Table 5 ESD Robustness**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness HBM (all pins)	$V_{HBMall}$	-2	–	2	kV	ESD robustness Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001.
ESD robustness HBM (VBAT, LOADx)	$V_{HBMglobal}$	-4	–	4	kV	VBAT, LOADx vs. all Grounds shorted ESD robustness Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001.
ESD robustness CDM (all pins)	$V_{CDMall}$	-500	–	500	V	ESD robustness Charged Device Model (CDM) according to JEDEC JESD22-C101
ESD robustness CDM (corner pins)	$V_{CDMcorner}$	-750	–	750	V	ESD robustness Charged Device Model (CDM) according to JEDEC JESD22-C101

## 3.2 Functional range

### 3.2.1 Functional range

**Table 6 Functional range**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Functional range (VDD)	$V_{DD}$	4.5	–	5.5	V	
Extended Functional range (VDD)	$V_{DD,ext}$	3.5	–	19	V	Outside of the normal Functional Range of $V_{DD}$ : <ul style="list-style-type: none"> <li><math>V_{DD} &lt; V_{DD,UV,TH}</math>: SPI communication functional; Power-stage off</li> <li><math>V_{DD} &gt; V_{DD,OV,TH}</math>: SPI communication functional; Power-stage off</li> </ul>
Functional range (VBAT)	$V_{BAT}$	6	–	18	V	

**(table continues...)**

**Electrical characteristics and parameters**

**Table 6 (continued) Functional range**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Extended functional range (VBAT)	$V_{BAT,ext}$	4	–	38	V	Outside of the normal functional $V_{BAT}$ range parameter deviations are possible: <ul style="list-style-type: none"> <li><math>V_{BATL}</math> 4 V...6 V: Parameter deviation possible</li> <li><math>V_{BATH}</math> 18 V...38 V: Parameter deviation possible</li> </ul>
Functional range (VIO)	$V_{IO}$	3.0	–	5.5	V	
Extended functional range (VIO)	$V_{IO,ext}$	5.5	–	19	V	Parameter deviation possible
Functional range (FWDx)	$V_{FWDx}$	-0.3 <sup>1)</sup>	–	40	V	<sup>1)</sup> During negative pulses ( $V_{FWDx} < -0.3$ V) the maximum energy of $E_{FWDx} =   -V_{FWDx} * (I_{LOADx} + I_{FWDx}) * t_{pulse}   \leq 2$ mJ shall not be violated.
Functional range (LOADx)	$V_{LOADx}$	-0.3 <sup>1)</sup>	–	40	V	<sup>1)</sup> During negative pulses ( $V_{LOADx} < -0.3$ V) the maximum energy of $E_{LOADx} =   -V_{LOADx} * (I_{LOADx} + I_{FWDx}) * t_{pulse}   \leq 2$ mJ shall not be violated.
Functional range clock frequency (CLK)	$f_{CLK}$	1	–	8	MHz	
System clock frequency	$f_{SYS}$	27.5	28	28.5	MHz	For use of external clock, clock divider must be set accordingly
System clock watchdog	$f_{SYS,WD}$	27	–	29	MHz	
Target PWM frequency	$f_{PWM}$	110	-	4000	Hz	PWM frequency control configuration range
Junction temperature	$T_J$	-40	–	150	°C	
Extended junction temperature	$T_{J,ext}$	150	–	175	°C	In the temperature range of 150 - 175°C parameter deviations are possible

**3.2.1.1 TDS\_functional\_range**

*Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given by the related "electrical characteristics" table.*

**Electrical characteristics and parameters**

**3.2.2 Parameter above 150°C**

**Table 7 Parameter above 150°C**

$T_J = 150^\circ\text{C}$  to  $175^\circ\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Shunt resistance	$R_{shunt}$	-	-	190	mΩ	
ON resistance	$R_{DSON}$	-	-	215	mΩ	
Average current control error, absolut	$I_{err,absolut}$	-6	-	6	mA	$I_{set} = 10 - 500\text{mA}$ $V_{BAT} = 13\text{V}$ Single channel operation
Average current control error, absolut - parallel	$I_{err,absolut,par}$	-12	-	12	mA	$I_{set,par} = 20 - 1000\text{ mA}$ $V_{BAT} = 13\text{V}$ Parallel channel operation
Average current control error, relative	$I_{err.relative}$	-1.2	-	1.2	%	$I_{set} > 500\text{mA}$ ; single channel operation $I_{set,par} > 1000\text{mA}$ ; parallel channel operation $V_{BAT} = 13\text{V}$
Diagnosis Current 0	$I_{HS}$ $I_{LS}$	-	-	130	μA	<I_DIAG> = 00 <sub>B</sub>

**3.2.3 Thermal resistance**

**Table 8 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction to case	$R_{thJC}$	-	-	3	K/W	
Junction to ambient	$R_{thJA}$	-	18.5	-	K/W	Depending on the mounting conditions. Specified $R_{thJA}$ value is according to JEDEC JESD51 -5, -7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μm, 2 x 35 μm CU).

**Functional description**

## **4 Functional description**

### **4.1 Power supply**

#### **4.1.1 TDS\_Power Supply**

##### **VDD pin**

The VDD pin and GND pin are the supply and ground pins for the digital circuit blocks. The current through these pins contain high frequency components. Decoupling with ceramic capacitors and careful PCB layout are required to obtain good EMC performance.

##### **VIO pin**

The VIO pin supplies the SPI output pin (SO). It should be connected to the I/O supply of the microcontroller (3.3 V or 5.0 V). The VIO voltage level can be configured by the <VIO\_SEL> bit in the GLOBAL\_CONFIG register.

##### **VBAT pin**

The VBAT pin is an input pin used to measure and monitor the battery voltage and feed diagnosis current source. The pin should be connected to the reverse protected battery rail and decoupled with a ceramic capacitor.

##### **GND/GNDP pin**

GND pins are the ground pins for the logic while the GNDP pins are the power ground pins for the power stages. It is recommended to connect all GNDP pins to the GND net externally.

##### **Power On Reset**

An internal power on reset (POR) circuit holds the device in a reset state if the internal logic is not operational due to undervoltage. The power on reset is released after all supplies are within their functional range and the Reset Duration Time  $t_{POR}$  has elapsed. The SPI interface can be accessed after the power on reset time. Any power on reset will set the bit <POR\_EVENT> in the GLOBAL\_DIAG0 register to 1. This can be used to check whether a power on reset has happened since the bit was set to 0.

#### **4.1.2 TDS\_Voltage monitoring**

The voltage levels of the supply pins  $V_{BAT}$ ,  $V_{IO}$  and  $V_{DD}$  and all internal voltages (ADC reference voltages, internal supply voltages) are monitored. A voltage fault is detected if a voltage exceeds the corresponding overvoltage (OV) threshold or falls below the respective undervoltage (UV) threshold. Apart from a VBAT OV/UV, an under/overvoltage fault disables the output stages by setting all <EN\_CH> bits to "0". Apart from a  $V_{BAT}$  and internal pre-regulator (<VPRE\_OV>) fault, an OV/UV fault condition causes the device to enter the Operation State Config Mode.

External supply voltage ( $V_{BAT}$ ,  $V_{IO}$ ,  $V_{DD}$ ) faults are indicated by setting the corresponding indication bit in the GLOBAL\_DIAG0 register to 1 while IC internal voltage faults are listed in the GLOBAL\_DIAG1 register. Voltage fault indication bits are cleared on write only. The bit <SUP\_NOK\_INT> and <SUP\_NOK\_EXT> in the FB\_STAT register provide a summarized indication if any internal or external voltage fault has been detected.

The under and overvoltage thresholds of  $V_{BAT}$  can be adapted and be set in the VBAT\_TH register.

$$V_{BAT,UV,TH} = \langle VBAT\_UV\_TH \rangle \cdot 0.16208V$$
$$V_{BAT,OV,TH} = \langle VBAT\_OV\_TH \rangle \cdot 0.16208V$$

##### **Equation 1**

The measured voltages of  $V_{IO}$  and  $V_{DD}$  are provided in the FB\_VOLTAGE1 register. The  $V_{BAT}$  voltage level can be readout from the FB\_VOLTAGE2 register.

The voltage monitoring mechanism of external and internal voltages can be tested by setting the <UV\_OV\_SWAP> bit in the GLOBAL\_CONFIG register to "1". If the test is successful, the OV/UV detection bits <VDD\_OV/UV>, <VIO\_OV/UV>, <VBAT\_OV/UV>, <VDD2V5\_OV/UV>, <VR\_IREF\_OV/UV>, <VPRE\_OV> and

**Functional description**

<REF\_OV/UV> are set. The power on reset (POR) due to an under or overvoltage can be tested by setting the bits <V1V5\_OV\_TEST> or <V1V5\_UV\_TEST> in the GLOBAL\_CONFIG register to "1".

**4.1.3 Electrical characteristics power supply**

**Table 9 Electrical characteristics power supply**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBAT current consumption normal mode	$I_{VBAT}$	-	-	1	mA	$V_{BAT} = 18\text{ V}$ Diagnosis off
VBAT current consumption inactive mode	$I_{VBAT,inactive}$	-	-	10	$\mu\text{A}$	$V_{BAT} = 18\text{ V}$ $V_{DD} = 0\text{ V} = V_{IO}$
VDD current consumption	$I_{VDD}$	10	21	30	mA	$V_{DD} = 5.5\text{ V}$
VIO current consumption	$I_{VIO}$	-	-	1	mA	$V_{DD} = 5.5\text{ V}$ $V_{CSN} > V_{CSN,high}$
VBAT undervoltage threshold	$V_{BAT,UV,TH}$	$(x*8-17)*0.01965$	$x*0.16208$	$(x*8+17)*0.02087$	V	$x = \langle V_{BAT\_UV\_TH} \rangle$ $V_{BAT}$ voltage is falling.
VBAT overvoltage threshold	$V_{BAT,OV,TH}$	$(x*8-17)*0.01965$	$x*0.16208$	$(x*8+17)*0.02087$	V	$x = \langle V_{BAT\_OV\_TH} \rangle$ $V_{BAT}$ voltage rising.
VDD undervoltage threshold	$V_{DD,UV,TH}$	3.7	-	4.5	V	$V_{DD}$ falling
VDD overvoltage threshold	$V_{DD,OV,TH}$	5.5	-	6.4	V	$V_{DD}$ rising
VIO undervoltage threshold 3.3 V	$V_{IO,UV,3V3,TH}$	2.6	-	3	V	$V_{IO}$ falling
VIO overvoltage threshold 3.3 V	$V_{IO,OV,3V3,TH}$	3.6	-	4.1	V	$V_{IO}$ rising
VIO undervoltage threshold 5 V	$V_{IO,UV,5V,TH}$	3.7	-	4.5	V	$V_{IO}$ falling
VIO overvoltage threshold 5 V	$V_{IO,OV,5V,TH}$	5.5	-	6.4	V	$V_{IO}$ rising
Power on reset time initialized with RESN	$t_{RESN}$	-	-	0.1	ms	Logic circuits are functional after $t_{RESN}$

**(table continues...)**

**Functional description**

**Table 9 (continued) Electrical characteristics power supply**

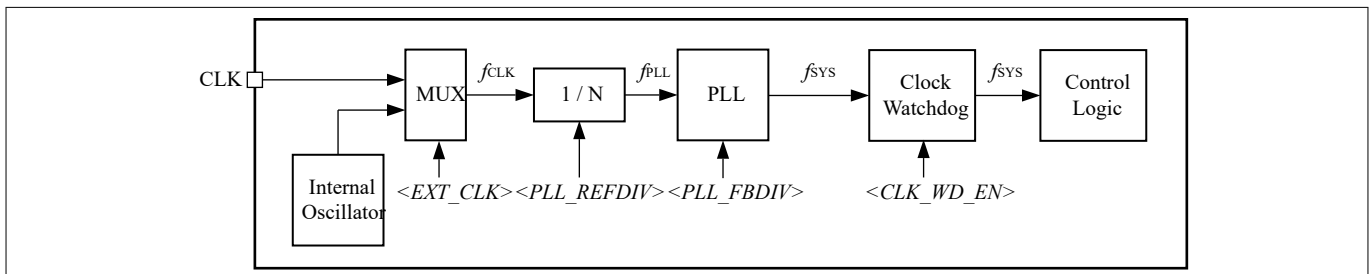
$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power on reset time initialized with undervoltage reset	$t_{POR}$	–	–	10	ms	Logic circuits are functional after $t_{POR}$

**4.2 Input / Output**

**4.2.1 TDS\_Clock**

The chip system clock  $f_{SYS}$  is generated by an integrated PLL (phase locked loop) and is used to clock the internal analog to digital converters and logic. The PLL can be either sourced by an internal oscillator or an external rectangular clock signal applied on the CLK-pin. The PLL clock source  $f_{CLK}$  can be selected by programming the <EXT\_CLK> bit in the CLK\_DIV register. Changing the clock source can only be done in Operation State Config Mode. During a change of the clock source, the clock watchdog is disabled and the <INIT\_DONE> bit is cleared. After a successful transition of the clock source, the <INIT\_DONE> bit in the FB\_STAT register is set to 1 and the clock watchdog is enabled.



**Figure 3 Clock Generation**

The system clock frequency  $f_{SYS}$  is given by

$$f_{SYS} = f_{CLK} \cdot \frac{\langle PLL\_FBDIV \rangle}{2 \cdot \langle PLL\_REFDIV \rangle}$$

**Equation 2**

By selecting an external clock input, the PLL divider must be set to meet the system clock frequency  $f_{SYS}$  (see table "Clock control register settings"). If the internal clock oscillator is used, the contents of the divider bit fields are ignored. The values of PLL reference divider <PLL\_REFDIV> and PLL feedback divider <PLL\_FBDIV> are located in the CLK\_DIV register.

$$\langle PLL\_REFDIV \rangle = \text{round}\left(\frac{f_{CLK}}{1\text{MHz}}\right)$$

$$\langle PLL\_FBDIV \rangle = \frac{56\text{MHz} \cdot \langle PLL\_REFDIV \rangle}{f_{CLK}}$$

**Equation 3**



**Functional description**

**Table 10**                    **Clock control register settings**

$f_{CLK}$ (MHz)	<PLL_REFDIV>	<PLL_FBDIV>	$f_{SYS}$ (MHz)	Error (%)
1	1	56	28	0.00
1.5	1	37	27.75	-0.89
2	2	56	28	0.00
2.5	2	45	28.13	0.45
3	3	56	28	0.00
3.5	3	48	28	0.00
4	4	56	28	0.00
4.5	4	50	28.13	0.45
5	5	56	28	0.00
5.5	5	51	28.05	0.18
6	6	56	28	0.00
6.5	6	52	28.17	0.60
7	7	56	28	0.00
7.5	7	52	27.86	-0.51
8	8	56	28	0.00

### 4.2.2                    **TDS\_Clock Watchdog**

The internal system clock  $f_{SYS}$  can be supervised by a separate clock watchdog. The clock watchdog can be disabled by setting the <CLK\_WD\_EN> bit in the GLOBAL\_CONFIG register to 0. A change of the clock watchdog configuration is only possible in Config Mode and if the <INIT\_DONE> bit in the FB\_STAT register is 1. If the system clock  $f_{SYS}$  is outside of the allowed frequency range  $f_{SYS,WD}$ , a clock watchdog fault is indicated by setting <CLK\_NOK> in the GLOBAL\_DIAG0 register to 1, all power stages are disabled and device enters the Config Mode. In case the clock watchdog detects a too fast clock, the device immediately enters the Critical Fault State.

### 4.2.3                    **TDS\_I/O Pins**

#### **RESN pin**

The RESN pin is an active low pin. If this pin is low, all channels are off, the device is in Reset State and all registers are set to their default values. The bit <RES\_EVENT> in the GLOBAL\_DIAG0 register indicates a reset triggered via the RESN pin. The RESN input pin is internally pulled low (GND).

#### **EN pin**

The EN pin is an active high pin. When this pin is low, all channels are turned off. The EN input pin is internally pulled low (GND).

#### **FAULTN pin**

The FAULTN pin is an open drain output. The FAULTN pin is initially high, if no fault is present after power up. The FAULTN pin is pulled low when the device transitions to the Critical Fault State, the RESN pin is low or an unmasked fault is detected. Fault indication on the FAULTN pin can be masked by setting the appropriate mask bit in the FAULT\_MASK registers.

- Channel specific:
  - CHx ICC regulation warning

**Functional description**

- CHx PWM regulation warning
- CHx overtemperature warning
- CHx open load
- CHx short circuit battery
- CHx short circuit ground
- Central overtemperature warning
- Central overtemperature error
- SPI watchdog error
- Clock too slow error
- Data error
- EN pin status indication
- Internal/External supply fault

**CLK pin**

A digital input clock signal  $f_{CLK}$  must be applied on the CLK pin if an external clock input is used. Using the internal clock, the pin should be connected to GND. The CLK input pin is internally pulled low (GND).

**DRV pins**

The DRV pins enable a direct control of the output stages, if the channel is configured to Direct Drive Mode via DRV pin. The DRV input pins are internally pulled low (GND). Unused DRV pins should be connected to GND.

**SI, SO, CSN, SCK pin**

The SI, SO, CSN, and SCK pins comprise the SPI interface. See SPI chapter for details.

**4.2.4 Electrical characteristics I/O**

**4.2.4.1 Control inputs EN, RESN, CLK, DRVx**

**Table 11 Control inputs EN, RESN, CLK, DRVx**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital high threshold voltage (EN, RESN, CLK, DRVx)	$V_{EN,high}$ $V_{RESN,high}$ $V_{CLK,high}$ $V_{DRVx,high}$	2	-	-	V	
Digital low threshold voltage (EN, RESN, CLK, DRVx)	$V_{EN,low}$ $V_{RESN,low}$ $V_{CLK,low}$ $V_{DRVx,low}$	-	-	0.8	V	
Digital input hysteresis (EN, RESN, CLK, DRVx)	$V_{IN\_HYS,EN}$ $V_{IN\_HYS,RESN}$ $V_{IN\_HYS,CLK}$ $V_{IN\_HYS,DRVx}$	-	50	-	mV	

(table continues...)

**Functional description**

**Table 11 (continued) Control inputs EN, RESN, CLK, DRVx**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull down current (EN, RESN, CLK, DRVx)	$I_{PD,EN}$ $I_{PD,RESN}$ $I_{PD,CLK}$ $I_{PD,DRVx}$	10	–	50	$\mu\text{A}$	$V_{IN} = 0.8\text{ V}$

**4.2.4.2 FAULTN**

**Table 12 FAULTN**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output low threshold voltage (FAULTN)	$V_{FAULTN,LOW}$	0	–	0.4	V	$I_{FAULTN} = 2\text{ mA}$
Output leakage current (FAULTN)	$I_{FAULTN,LGK}$	-100	–	100	$\mu\text{A}$	No fault present $0\text{ V} < V_{FAULTN} < V_{IO}$

**4.3 IC Operation states**

**4.3.1 TDS\_IC Operation states**

**Reset state:**

- The answer to an SPI command is the 16 bit reply frame.
- All SPI register values are being reset to default when the product leaves the Reset State.

**Config Mode:**

- All channels are disabled. <EN\_CH> bits are 0 and cannot be set.
- Channel diagnostic is disabled (HS and LS current source are disabled).
- The Channel Mode, the global configuration, the parallel channel operation and the PLL divider can only be configured in Config Mode.

**Mission Mode:**

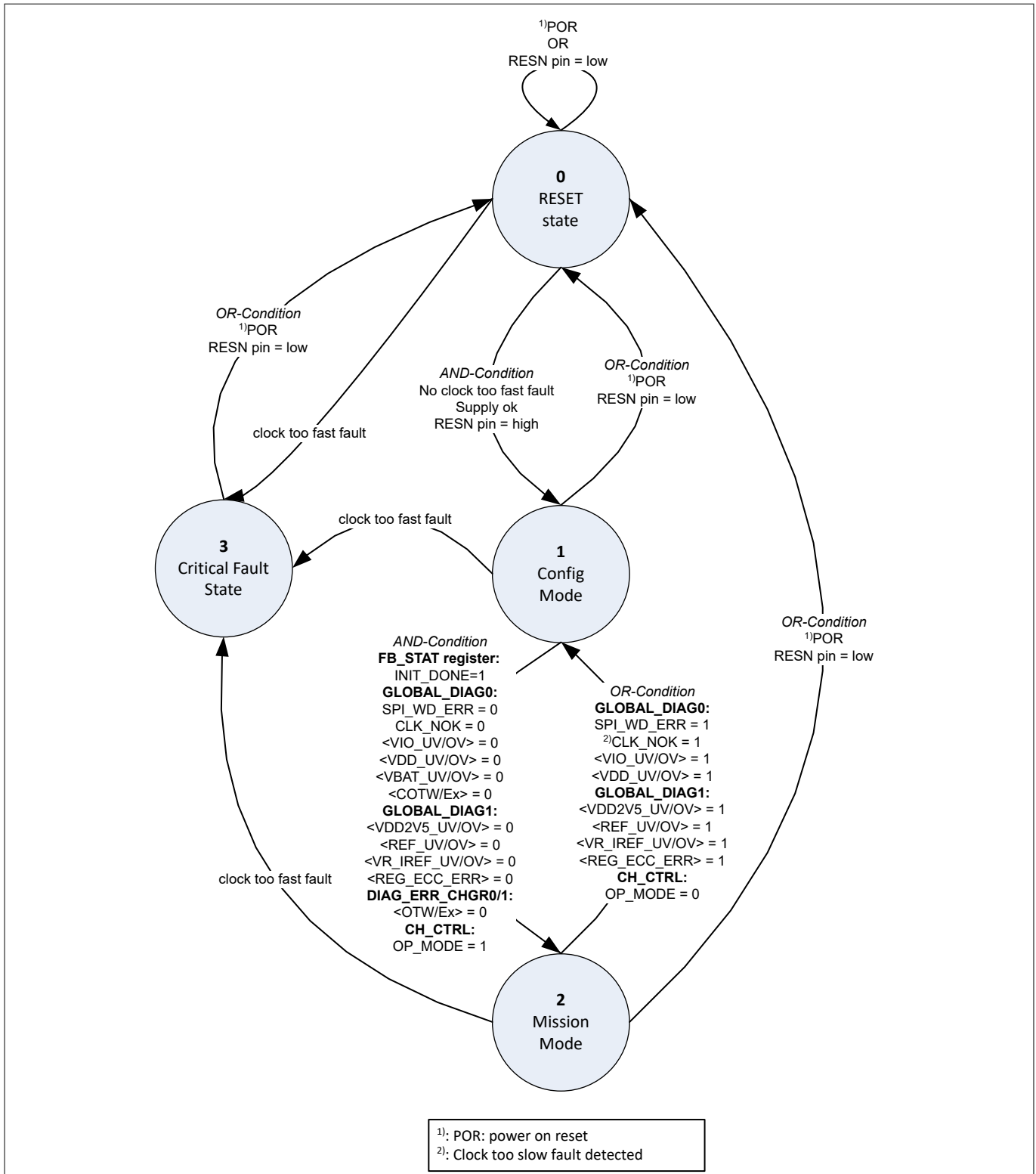
- The channels and their respective diagnosis are only functional in Mission Mode.

**Critical Fault state:**

- The IC will reply all SPI interactions with the Critical Fault frame.
- The FAULTN pin is pulled low.

The following State Diagram gives an overview on the transition conditions.

**Functional description**



**Figure 4**      **Operation States and Transitions**

**Functional description**

**4.4 Channel modes**

**4.4.1 TDS\_Channel Modes**

The IC offers different modes to control the output stage of a channel. The channel mode can be selected by programming the MODE register. A change of the channel mode is only possible in Config Mode. The measurement period  $T_{meas}$  for averaged feedback values depends on the selected channel mode (see chapter "current supervision").

**4.4.2 Channel Modes**

Channel Mode	Measurement Period $T_{meas}$ for Feedback Values
Channel off	No measurement active
Current Control ICC	Dither Period $T_{Dither}$
Direct Drive via on-time (TON register)	Dither Period $T_{Dither}$
Direct Drive via DRV pin	<ul style="list-style-type: none"> <li>If configured Dither Period <math>T_{Dither}</math>, else</li> <li>Time between two rising edges at DRV pin</li> </ul>
Measurement Mode*	Dither Period $T_{Dither}$

**4.4.3 TDS\_Measurement Mode - (4/6CHx)**

*Note: The current measurement over the shunt can be used for high-precision current measurement applications. In measurement mode the internal low-side switch is non-conductive.*

**4.4.4 TDS\_Additional Information Channel Modes**

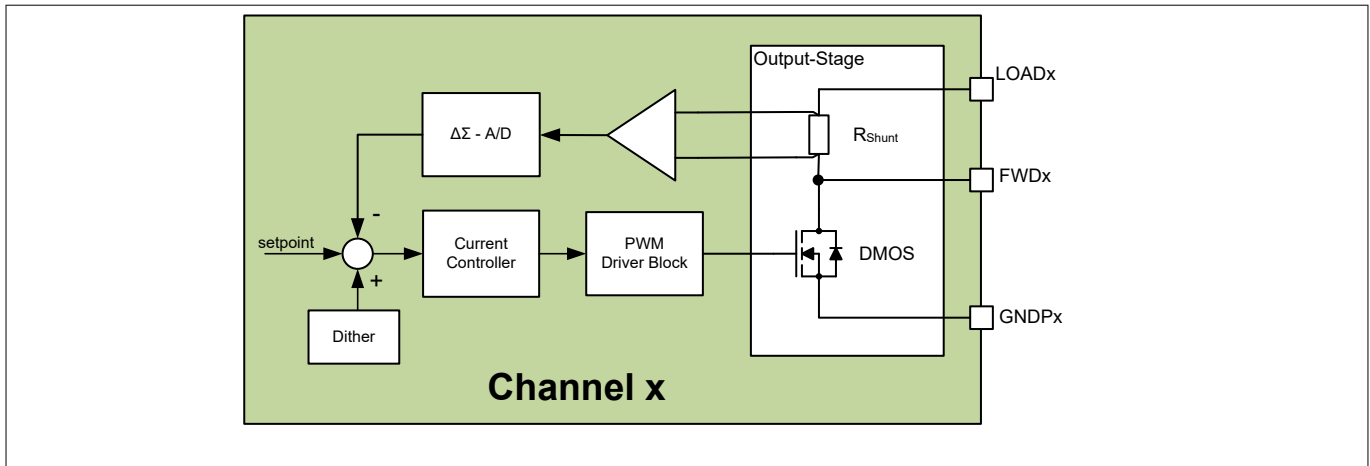
*Note: For more details on the "Current Control" and "Direct Drive" Mode please refer to the respective chapters.*

**4.5 Power stages**

**4.5.1 TDS\_Channel overview - (4CHx)**

There are four independent output channels implemented in this device. The output powerstage of each channel consists of a low side n-channel DMOS transistor and a current sensing resistor. The switch and shunt resistor are protected from external failures by built in overcurrent and overtemperature detection circuits. A high-side load can be connected to the LOADx pin. For inductive loads a diode must be applied at the FWDx pin for external freewheeling. The output voltage slew rate of the power stages can be programmed in the CH\_CONFIG register.

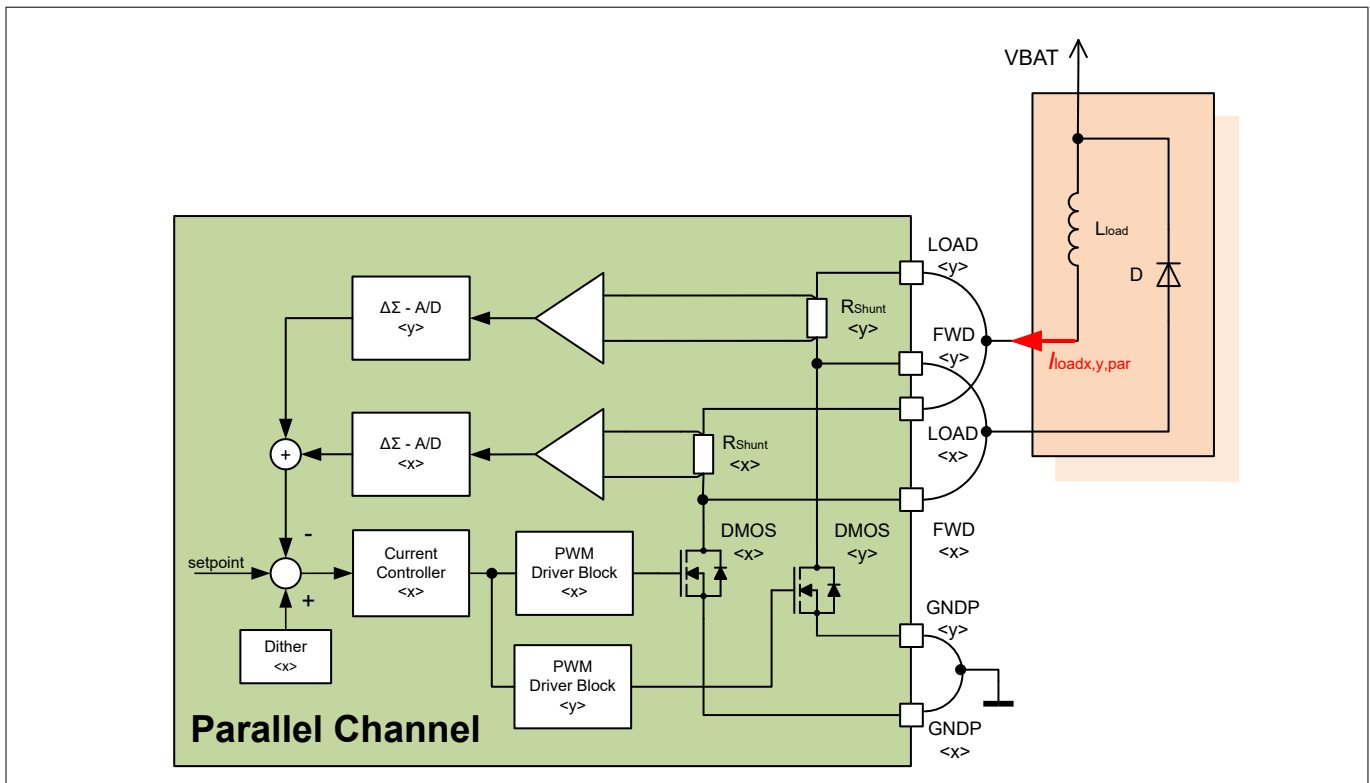
**Functional description**



**Figure 5 Channel Block Diagram**

**4.5.2 TDS\_Parallel channel operation - (4CHx)**

The IC features a parallel mode of output stages to increase the maximum current capability of the device. The channels 0 and 3 and the channels 1 and 2 can be connected in parallel. Channel 0 and 1 are the master channels and channel 2 and 3 are the slave channels. Only the master channels can be configured via SPI. The parallel channel mode can be enabled or disabled in the CH\_CTRL register when the device is in Config Mode.



**Figure 6 Parallel Channel Configuration**

**Slave channel**

The current controller and the OFF-state diagnosis of the slave channel are disabled. A write access to the MODE register of the slave channel is ignored and reads back zero. The slave channel's SETPOINT register cannot be set and is read back as zero. All feedback registers of the slave channel have to be disregarded. A write to a slave <EN\_CH> bit is ignored and 0 is read back. After disabling the parallel channel mode the slave channel must be re-configured to the desired channel behaviour.

**Setpoint**

**Functional description**

In parallel channel mode, the programmed setpoint of the master channel is used. Hence the LSB (least significant bit) of the setpoint is doubled.

**Diagnostic functions**

The LSB of the fixed OLSG (open load/short to GND) threshold is scaled by a factor of two. The OC (overcurrent) protection feature is active on the master as well as on the slave channel. If either the master or the slave channel detects an OC fault, both channels are disabled.

**Feedback functions**

The current feedback in the FB\_I\_AVG register represent the summed up current over the shunt resistors of the master and slave channel. The duty cycle feedback can be read from the master channel.

**4.5.3 Electrical characteristics power stages**

**Table 13 Electrical characteristics power stages**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

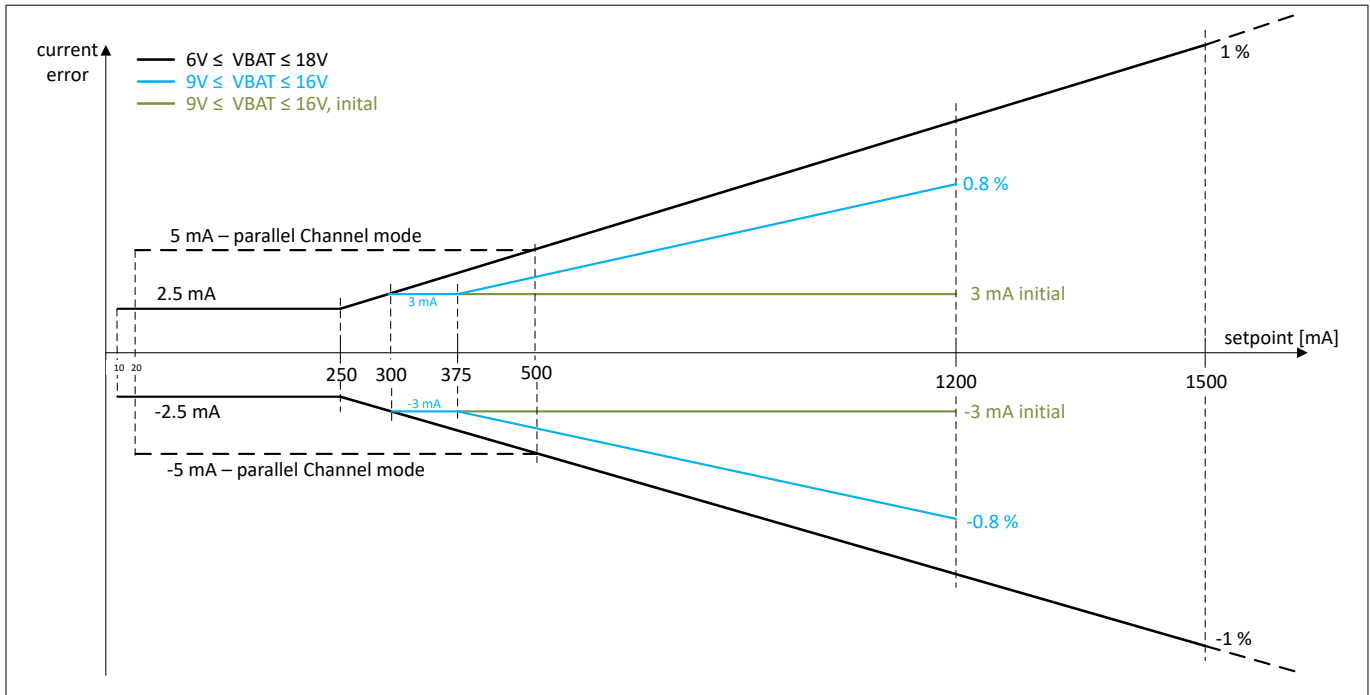
Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Shunt resistance	$R_{shunt}$	-	140	185	m $\Omega$	
ON resistance	$R_{DSON}$	-	115	200 <sup>1)</sup>	m $\Omega$	<sup>1)</sup> $T_J = 150^{\circ}\text{C}$ , $I_{LOADx} = 2.0\text{ A}$
Leakage current (LOADx, FWDx)	$I_{LOADx,LKG}$ $I_{FWDx,LKG}$	-100	-	100	$\mu\text{A}$	$V_{BAT} = 18\text{ V}$ ; Setpoint = 0 mA; Diagnosis off
Slew rate 0	SR0	0.5	1	2	V/ $\mu\text{s}$	$V_{BAT}=14\text{V}$ ; $R_{LOAD}=10\Omega$ 20% to 80% of applied load voltage <SLEWR> = 00 <sub>B</sub>
Slew rate 1	SR1	1.25	2.5	5	V/ $\mu\text{s}$	$V_{BAT}=14\text{V}$ ; $R_{LOAD}=10\Omega$ 20% to 80% of applied load voltage <SLEWR> = 01 <sub>B</sub>
Slew rate 2	SR2	2.5	5	10	V/ $\mu\text{s}$	$V_{BAT}=14\text{V}$ ; $R_{LOAD}=10\Omega$ 20% to 80% of applied load voltage <SLEWR> = 10 <sub>B</sub>
Slew rate 3	SR3	5	10	20	V/ $\mu\text{s}$	$V_{BAT}=14\text{V}$ ; $R_{LOAD}=10\Omega$ 20% to 80% of applied load voltage <SLEWR> = 11 <sub>B</sub>

**4.6 Current control**

**4.6.1 Current accuracy overview**

The average current setpoint is determined by the content of <TARGET> in the SETPOINT register. The accuracy band of the current regulation is illustrated in the figure below. The current accuracy includes the junction temperature range  $T_J$ , battery voltage range  $V_{BAT}$  and device aging (AEC-Q100 HTOL, TC). The device supports a high precision current accuracy within a reduced battery range. For more details refer to [Table 14](#).

**Functional description**



**Figure 7** Current accuracy specification overview

**4.6.2 Integrating Current Controller (ICC)**

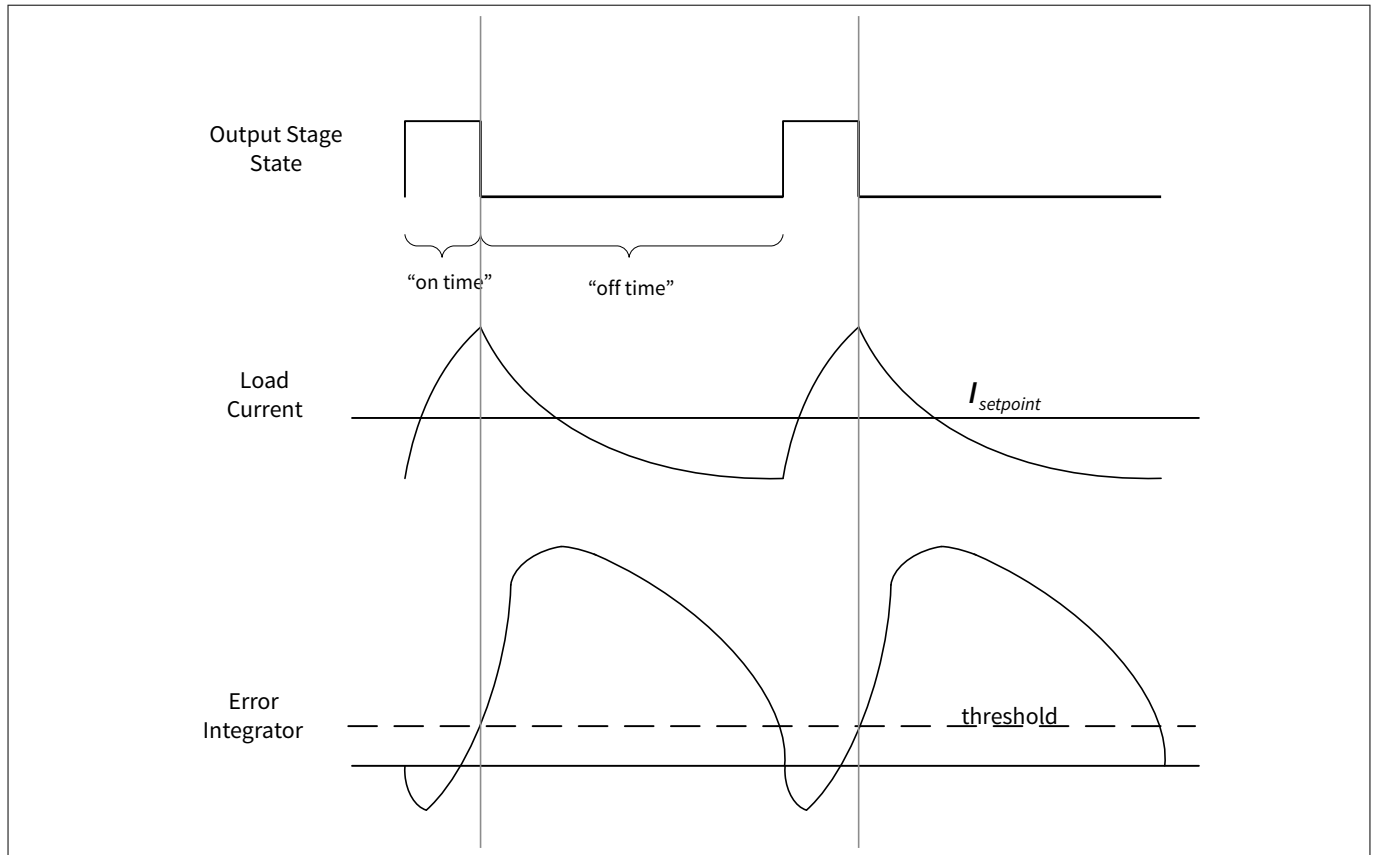
**4.6.2.1 TDS\_Integrating Current Controller (ICC)**

The current controller regulates the load current automatically to a user defined setpoint by turning on and off the internal transistor. If the internal transistor is switched on, the current through the inductive load will increase. If the internal transistor is turned off, the current will continue to flow through the recirculation diode gradually decay.

The Integrating Current Controller (ICC) is based on the requirement that the integrated current error over one PWM cycle is zero. This means that the average current after one PWM cycle exactly equals the targeted current. The controller integrates the current deviation (difference between load current and the setpoint) and switches the output stage accordingly: While the integrated current deviation is below a configurable integrator threshold, the power stage is turned on. In this phase the load current will increase. When the integrated current error exceeds the determined integrator threshold the power stage is turned off and the current recirculates through the freewheeling diode. The average current is reached when the integrated current deviation crosses zero which determines the start of a new PWM cycle. The ICC switching characteristic provides the physically fastest current response which makes it very robust against load voltage dips.



**Functional description**



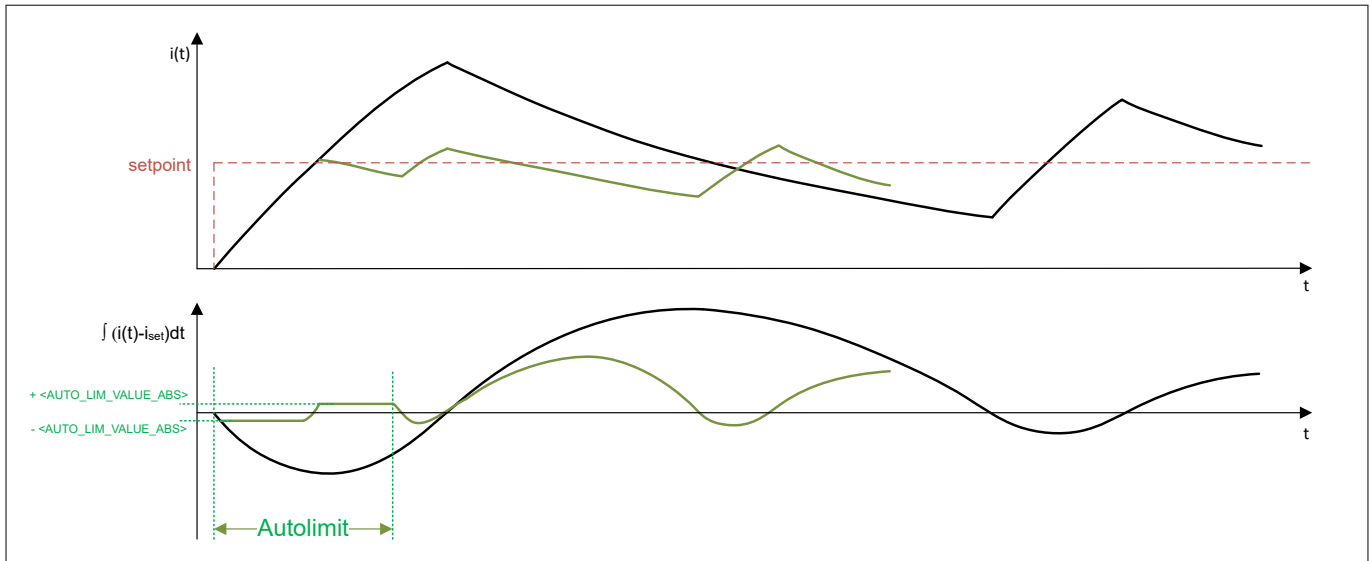
**Figure 8** Current Control Waveform

### 4.6.2.2 TDS\_Integrator Limits

The ICC integrator can be saturated in order to avoid an integrator windup. The integrator limits are configurable via +/-<LIM\_VALUE\_ABS> in the INTEGRATOR\_LIMIT register.

In order to avoid current overshoots after setpoint changes the Autolimit feature is introduced. The device limits the integrator value to +/-<AUTO\_LIM\_VALUE\_ABS> (INTEGRATOR\_LIMIT register) for a maximum of two PWM cycles after a setpoint change. After the completion of Autolimit, the ICC automatically revert back to the normal integrator limit values +/-<LIM\_VALUE\_ABS>. The Autolimit feature is disabled by writing a 1 to the <AUTO\_LIMIT\_DIS> bit in the SETPOINT register.

**Functional description**



**Figure 9**                    **Autolimit feature**

**4.6.2.3**                    **TDS\_PWM Frequency Control**

The load characteristic and load supply voltage affecting the PWM output frequency of the ICC controller. The on-time of the LS-FET and therefore the PWM cycle can be adjusted by modifying the integrator threshold value. A greater integrator threshold ends up in a longer on-time. Although the configured integrator threshold value is positive, the actual threshold can get negative since it is referenced to the lowest current deviation integral value captured during the on-phase. This means very short on-time configurations are possible. The shortest on-time is determined by limiting the integrator threshold to a minimum value configurable via <MIN\_INT\_THRESH> in the CTRL register.

There are two options to set the integrator threshold to adjust the PWM frequency.

**Manual setting of On-time**

The driver on-time and therefore a target PWM period can be set manually by programming a fixed integrator threshold <INT\_THRESH> in the CTRL\_INT\_THRESH register. The PWM frequency controller has to be disabled by setting <PERIOD\_MANT> in the PERIOD register to 0.

**Automatic PWM control**

The PWM frequency controller regulates the PWM frequency using an “Integral” control loop with a programmable gain, KI. This control loop monitors the actual PWM period and compares subtracts it from the PWM period target setting in the PWM period register. The error in the PWM period is multiplied by the gain KI and then integrated at each PWM cycle. The output of the controller adjusts the on-time of the PWM signal until the actual PWM period matches the programmed PWM period. The internal PWM frequency controller can be activated by setting a target PWM period  $T_{period}$  in the PERIOD register.

$$T_{period} = \frac{\langle PERIOD\_MANT \rangle \cdot 2^{\langle PERIOD\_EXP \rangle}}{f_{SYS}}$$

**Equation 4**

By setting the bit <LOW\_FREQ\_RANGE\_EN> the range of the configurable target PWM frequency is lower and can be calculated as follow.

$$T_{period} = \frac{\langle PERIOD\_MANT \rangle \cdot 8 \cdot 2^{\langle PERIOD\_EXP \rangle}}{f_{SYS}}$$

**Equation 5**

**Functional description**

The bitfield <INT\_THRESH> in the CTRL\_INT\_THRESH register determines the integrator threshold used after setpoint changes or activation of the PWM controller. The <INT\_THRESH> value must be configured before applying the new setpoint. The resulting threshold calculated by the PWM frequency controller can be retrieved from the FB\_INT\_THRESH register. The threshold calculated by the PWM frequency controller can be read back from the FB\_INT\_THRESH register. The threshold value can be used to program <INT\_THRESH> to reduce the settling time of the PWM frequency controller e.g. after a setpoint change.

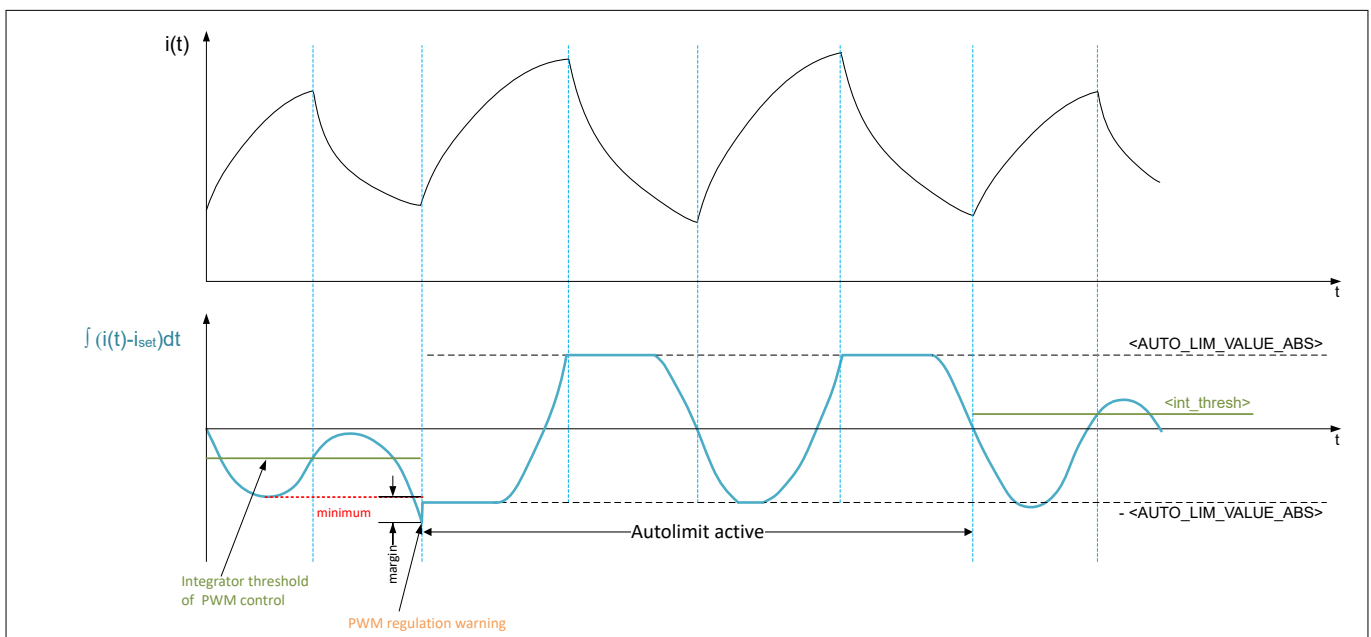
*Note: The Autolimit threshold must be greater than the lower threshold limit configuration for a correct ICC functioning (<AUTO\_LIM\_VALUE\_ABS> > <MIN\_INT\_THRESH>+0x3).*

The PWM frequency control parameter KI can be set by <PWM\_CTRL\_PARAM> in the PERIOD register. The integrator parameter KI determines the gain and therefore the speed of the PWM frequency control loop. A KI value of 0 results in a slower but more stable PWM control.

During steep dither settings, long off-times can appear which end up in high frequencies in the next rising dither slope. The frequency controller does not consider falling dither slopes by setting the <PWM\_PERIOD\_CALC\_MODE> in the CTRL register.

**4.6.2.4 TDS\_PWM regulation warning**

An ICC PWM regulation warning is issued if the ICC integrator value drops below the minimum integral value, which was captured during the on-phase. This can happen i.e. if a negative absolute integrator threshold is calculated from the PWM control and the inertia of the load is too large. This means the integrated current deviation could not exceed the zero level and therefore the power stage would not switch on anymore. A negative integrator threshold can be avoided by programming <MIN\_INT\_THRESH> in the CTRL register to a value greater than 1. A recovery process maintains the current regulation by triggering the Autolimit feature. After finishing Autolimit, the integrator threshold configured in <INT\_THRESH> bitfield is used. The PWM regulation warning is signaled by asserting the <PWM\_REG\_WARN> bit in the DIAG\_WARN\_CHGR register.

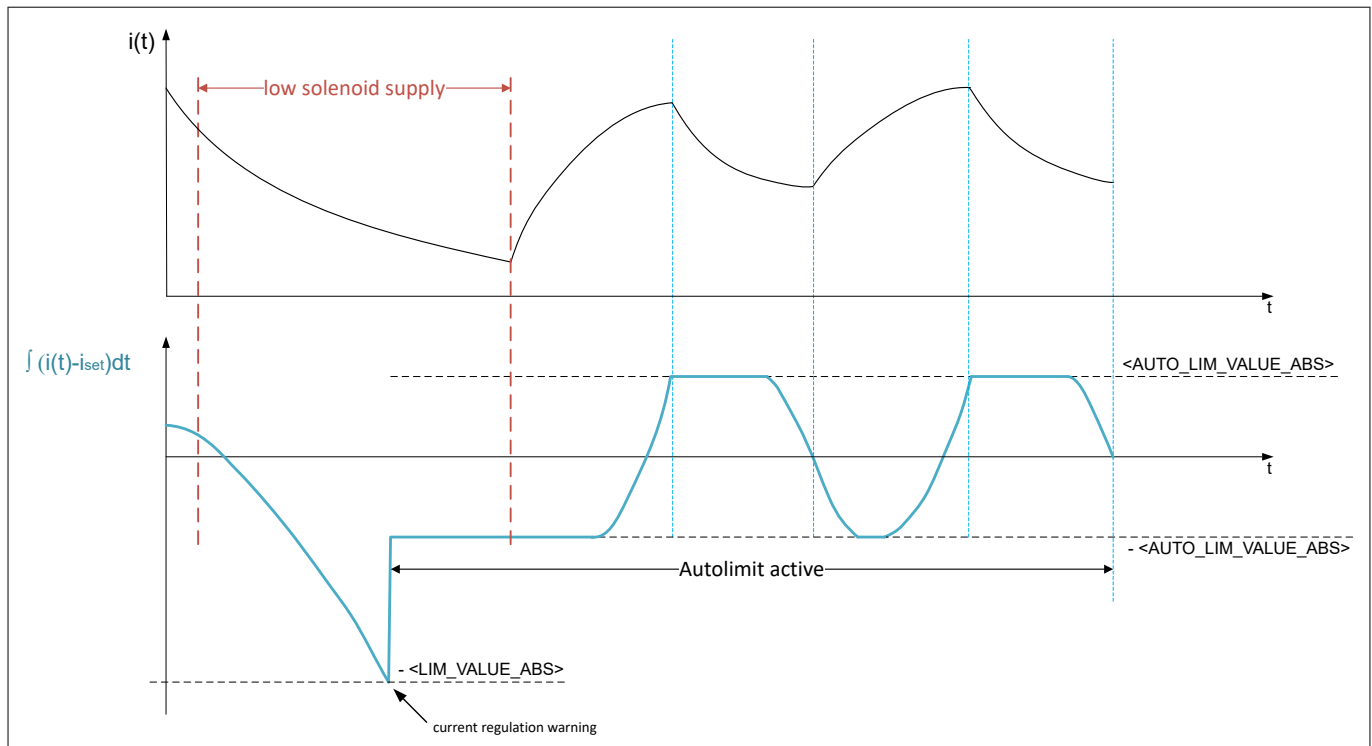


**Figure 10** ICC PWM regulation warning

**4.6.2.5 TDS\_Current regulation warning**

An ICC current regulation warning occurs if the ICC integrator value reaches the absolute integrator limit <LIM\_VALUE\_ABS> located in the INTEGRATOR\_LIMIT register. This can happen for example during a voltage supply dip. A recovery process maintains the current regulation by triggering the Autolimit feature. The integrator threshold will be reset to <INT\_THRESH> located in the CTRL\_INT\_THRESH register. The warning is signaled by asserting the respective <I\_REG\_WARN> bit in the DIAG\_WARN\_CHGR register.

**Functional description**



**Figure 11** ICC current regulation warning

**4.6.3 Electrical characteristics current control**

**Table 14** Electrical characteristics current control

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Average current control error, absolute	$I_{err,abs,1}$	-2.5	-	2.5	mA	$I_{set} = 10 - 250\text{ mA}$ includes aging single channel operation
Average current control error, absolute - parallel	$I_{err,abs,1,par}$	-5	-	5	mA	$I_{set} = 20 - 500\text{ mA}$ includes aging parallel channel operation
Average current control error, relative	$I_{err,rel,1}$	-1	-	1	%	$250\text{ mA} < I_{set} \leq 1500\text{ mA}$ ; single channel operation $500\text{ mA} < I_{set} \leq 2700\text{ mA}$ ; parallel channel operation includes aging
Average current control error, absolute - reduced battery	$I_{err,abs,2}$	-3	-	3	mA	$300\text{ mA} < I_{set} \leq 375\text{ mA}$ $9.0\text{ V} \leq V_{BAT} \leq 16\text{ V}$ includes aging single channel operation

**(table continues...)**

**Functional description**

**Table 14 (continued) Electrical characteristics current control**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Initial average current control error, absolute - reduced battery	$I_{err,abs,2,init}$	-3	-	3	mA	$375\text{ mA} < I_{set} \leq 1200\text{ mA}$ $9.0\text{ V} \leq V_{BAT} \leq 16\text{ V}$ single channel operation
Average current control error, relative - reduced battery	$I_{err,rel,2}$	-0.8	-	0.8	%	$375\text{ mA} < I_{set} \leq 1200\text{ mA}$ $9.0\text{ V} \leq V_{BAT} \leq 16\text{ V}$ includes aging single channel operation
Load current	$I_{set}$	0	-	1500	mA	DC setpoint current Single channel operation
Dither current	$I_{set} + I_{Dither}$	0	-	1800	mA	DC setpoint current incl. dither current amplitude Single channel operation
Measurement current	$I_{LOADx}$	0	-	2000	mA	DC setpoint incl. dither current amplitude and overshoot Single channel operation The user must take care that the maximum value is not exceeded
Measurement current - parallel	$I_{LOADx,y,par}$	0	-	2700	mA	DC setpoint current incl. dither current amplitude and overshoot Parallel channel operation Single channel measurement range $I_{LOADx}$ of each Channel shall not be violated

## 4.7 Dither

### 4.7.1 TDS\_Dither configuration

A configurable dither waveform can be added to the average current setpoint in order to reduce the hysteresis of a driven solenoid valve. The dither operation is an overlay of a triangular or trapezoidal waveform over the current setpoint. The dither waveform is generated by permanently changing the setpoint according to the programmed shape.

The dither shape can be configured by setting the <STEPS>, <STEP\_SIZE> and <FLAT> values in the DITHER\_STEP and DITHER\_CTRL register. The <STEP\_SIZE> value scales the height of each dither step where the LSB is equal to <TARGET> in the setpoint register. The value of <STEPS> determines the number of steps for the rising and falling edge of each half cycle of the dither waveform. The value of <FLAT> determines the number of flat steps at the minimum and maximum plateau of the dither waveform.

The amplitude of the dither waveform overlay  $I_{Dither}$  can be calculated as follows.

**Functional description**

$$I_{Dither} = \langle \text{STEPS} \rangle \cdot \langle \text{STEP\_SIZE} \rangle \cdot \frac{2A}{2^{15} - 1}$$

**Equation 6**

Care should be taken that no negative dither amplitude ( $I_{set} - I_{Dither} > 0$ ) is configured and possible overshoots are not violating the specified measurement current range  $I_{LOADx}$  or  $I_{LOADx,par}$  (parallel channel operation). The dither overlay  $I_{Dither}$  is deactivated if the target setpoint is set to 0.

The Dither period  $T_{Dither}$  is a multiple of the Dither reference clock determined by the values of  $\langle \text{MANT} \rangle$ ,  $\langle \text{EXP} \rangle$  of the DITHER\_CLK\_DIV register. The dither period  $T_{Dither}$  and dither reference clock  $t_{ref\_clk}$  can be calculated as follows.

$$T_{Dither} = (4 \cdot \langle \text{STEPS} \rangle + 2 \cdot \langle \text{FLAT} \rangle) \cdot t_{ref\_clk}$$

**Equation 7**

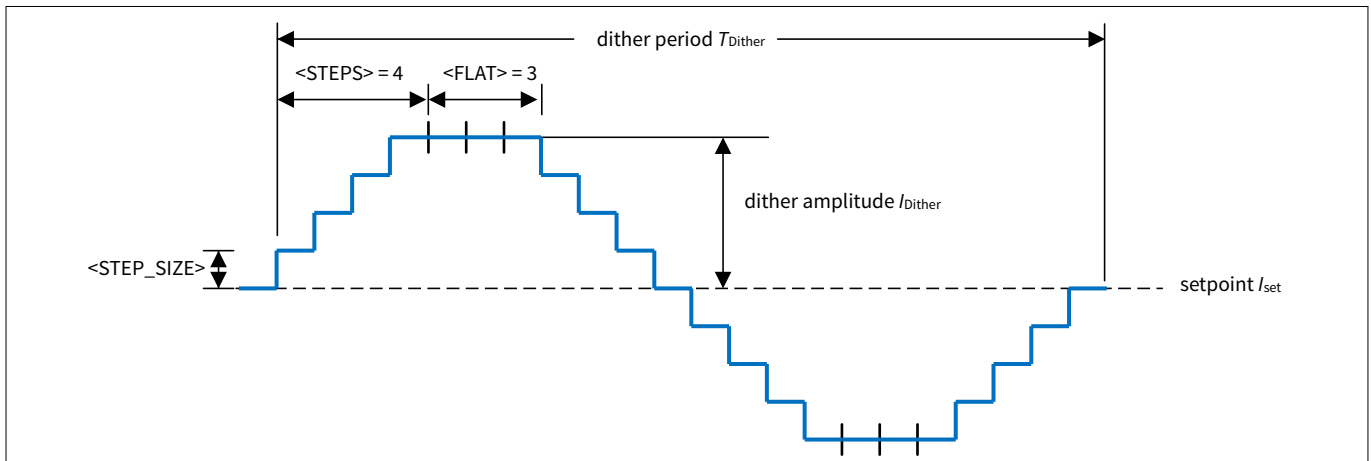
$$t_{ref\_clk} = \frac{\langle \text{MANT} \rangle \cdot 2^{\langle \text{EXP} \rangle}}{f_{SYS}}$$

**Equation 8**

$$t_{flat} = \langle \text{FLAT} \rangle \cdot t_{ref\_clk}$$

**Equation 9**

Note: If  $\langle \text{STEPS} \rangle = 0$  and  $\langle \text{FLAT} \rangle = 0$ , the dither period  $T_{Dither} = t_{ref\_clk}$



**Figure 12 Dither Waveform Configuration**

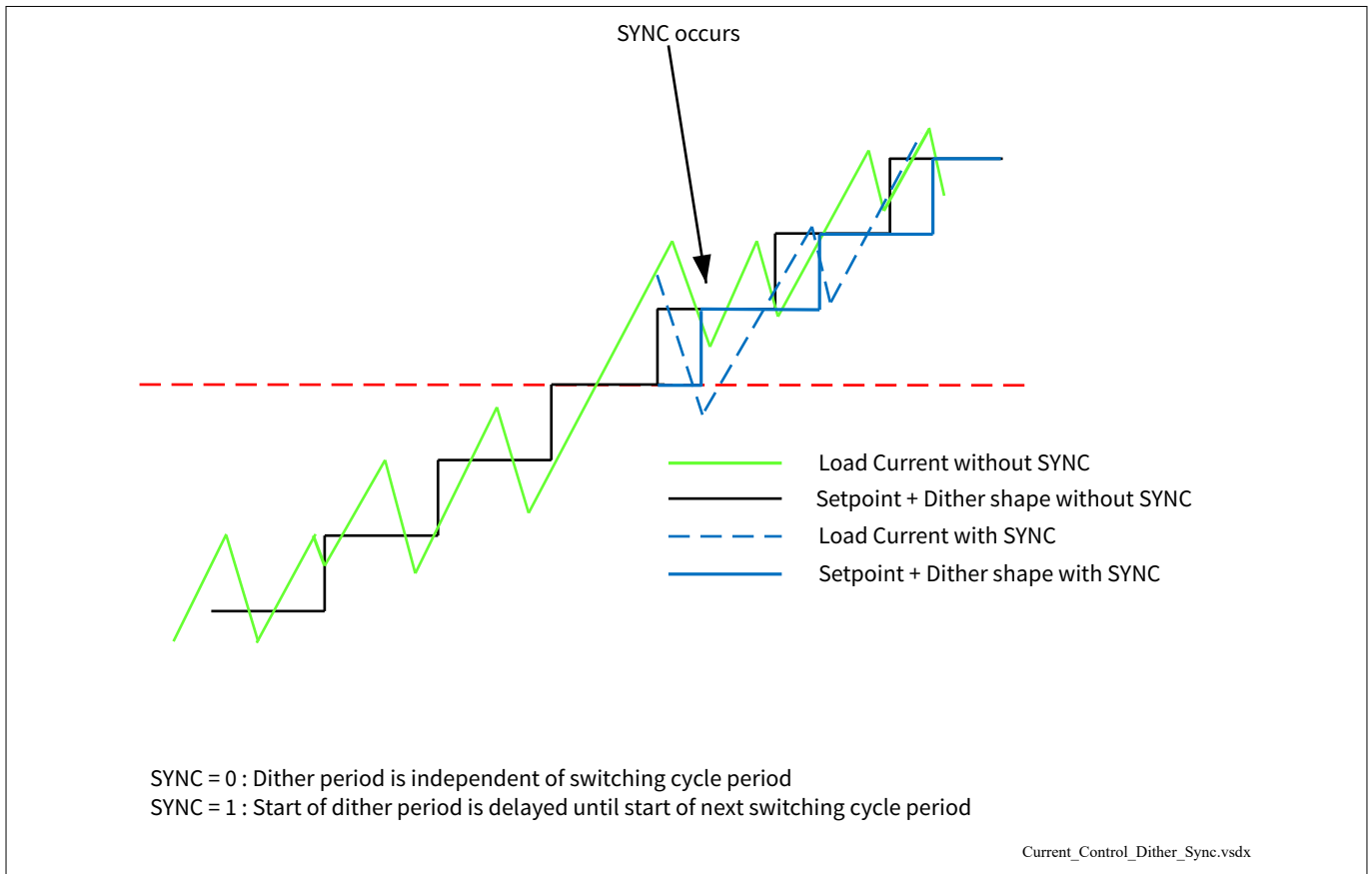
**4.7.2 TDS\_Dither parameter update**

All dither parameters located in registers DITHER\_STEP and DITHER\_CTRL become active at the start of the next dither period after writing to the DITHER\_CTRL register. After triggering an update event (write to DITHER\_CTRL) within the active dither period, the dither configuration ( DITHER\_STEP/ DITHER\_CTRL) that was transmitted last within the active dither period is taken over. An update of the reference clock  $t_{ref\_clk}$  controlled by the DITHER\_CLK\_DIV register takes immediate effect. If the dither amplitude is disabled by clearing  $\langle \text{STEP\_SIZE} \rangle$ , the active dither period will be completed. The configured dither period and overlay is immediately (re)-started if the  $\langle \text{EN\_CH} \rangle$  bit transitions to 1.

**Functional description**

**4.7.3 TDS\_Dither PWM synchronization**

The dither-PWM synchronization starts a new dither period synchron with the start of the next PWM cycle to enable the same starting conditions for each dither period. The start of a PWM cycle period is defined as a turn on of the output stage. The start of a dither period is defined to be when the dither increases one step above zero on this rising slope of the dither waveform. The dither-PWM synchronization can be enabled by setting the <DITHER\_PWM\_SYNC\_EN> bit in the DITHER\_CLK\_DIV register. When the <DITHER\_PWM\_SYNC\_EN> bit is set to 0, the dither waveform is free-running and asynchronous to the PWM frequency.



**Figure 13 Dither sync**

**4.7.4 TDS\_Only ICC**

Note: This feature is only available in ICC Channel Mode.

**4.7.5 TDS\_Dither setpoint synchronization**

The dither-setpoint synchronization feature updates the averaged feedback values of a channel (FB\_DC, FB\_I\_AVG, FB\_VBAT) after a change in setpoint in the shortest possible time. The dither-setpoint synchronization restarts the dither period when the newly applied setpoint has been reached. Therefore, the measurement period  $T_{meas}$  (dither period) for the feedback values is always in lockstep with a setpoint change and no latency of the averaged feedback values (FB\_DC, FB\_I\_AVG, FB\_VBAT) is present. The synchronization of the dither period to a setpoint change can be enabled by programming the <DITHER\_SETPOINT\_SYNC\_EN> bit in the DITHER\_CLK\_DIV register. An enabled setpoint synchronization freezes the average feedback registers (FB\_DC, FB\_I\_AVG, FB\_VBAT) with the last valid measurement result if the channel is disabled with setpoint "0".

**Functional description**

### 4.7.6 TDS\_Only ICC

*Note:* This feature is only available in ICC Channel Mode.

### 4.7.7 TDS\_Deep dither

A steep and deep dither command is comparable to great changes of setpoint. The deep dither function reduces the over- and undershoot of very steep dither overlays by permanently enabling the Autolimit feature. The deep dither feature can be enabled by setting the <DEEP\_DITHER> bit in DITHER\_CTRL register.

### 4.7.8 TDS\_ICC only

*Note:* This feature is only available in ICC Channel Mode.

## 4.8 Direct Drive

### 4.8.1 TDS\_Direct Drive

In Direct Drive, the channel's output stage is controlled directly by the user. To enable a output stage switching, the respective channel must be activated by setting <EN\_CH> bit to 1 and a target current setpoint value different to zero. The Direct Drive mode must be selected by programming the MODE register.

#### Direct Drive mode via DRV pin

In Direct Drive mode via DRV pin the channel's output stage is switched according to the logic level at the corresponding DRV pin. The channel is turned on if the DRV pin is high and is switched off if the DRV pin is low.

#### Direct Drive mode via SPI on-Time

In Direct Drive mode via SPI on-Time, the channel's output stage is switched according to a configurable period. The period  $T_{period}$  is set in the DITHER\_CLK\_DIV register by the bit fields <MANT> and <EXP>. The on-time  $t_{on}$  during a period can be configured with the <TON\_MANT> bit field in the TON register.

$$T_{period} = \frac{\langle MANT \rangle \cdot 2^{\langle EXP \rangle}}{f_{SYS}}$$
$$t_{on} = \frac{\langle TON\_MANT \rangle \cdot 2^{\langle EXP \rangle}}{f_{SYS}}$$

**Equation 10**

## 4.9 Diagnostic functions

### 4.9.1 TDS\_Overview

Each IC channel has an independent open load (OL), overcurrent (OC) and short circuit to ground (SG) diagnosis.

The following points should be considered:

- All failure modes are only considered to occur on the off board routed LOAD-pin.
- The diagnosis indication bits are clear on write.
- The diagnosis is only enabled if the device is in Mission Mode

The diagnosis consists of an ON-state diagnosis and an OFF-state diagnosis. Both diagnosis states shall be used to enable a full fault analysis coverage.

#### ON-state diagnosis



**Functional description**

A channel is in ON-state if the <EN\_CH> bit is set and the setpoint value is different to 0 mA. All diagnostic functions in ON-state rely on measuring the current through the shunt resistor. The ON-state diagnosis cannot distinguish between a short circuit to ground (SG) and an open load (OL) fault. Those faults are summarized to an Open Load/Short to Ground fault (OLSG) in the ON-state. A distinction whether an OL or SG is present needs to be done by the OFF-state diagnosis.

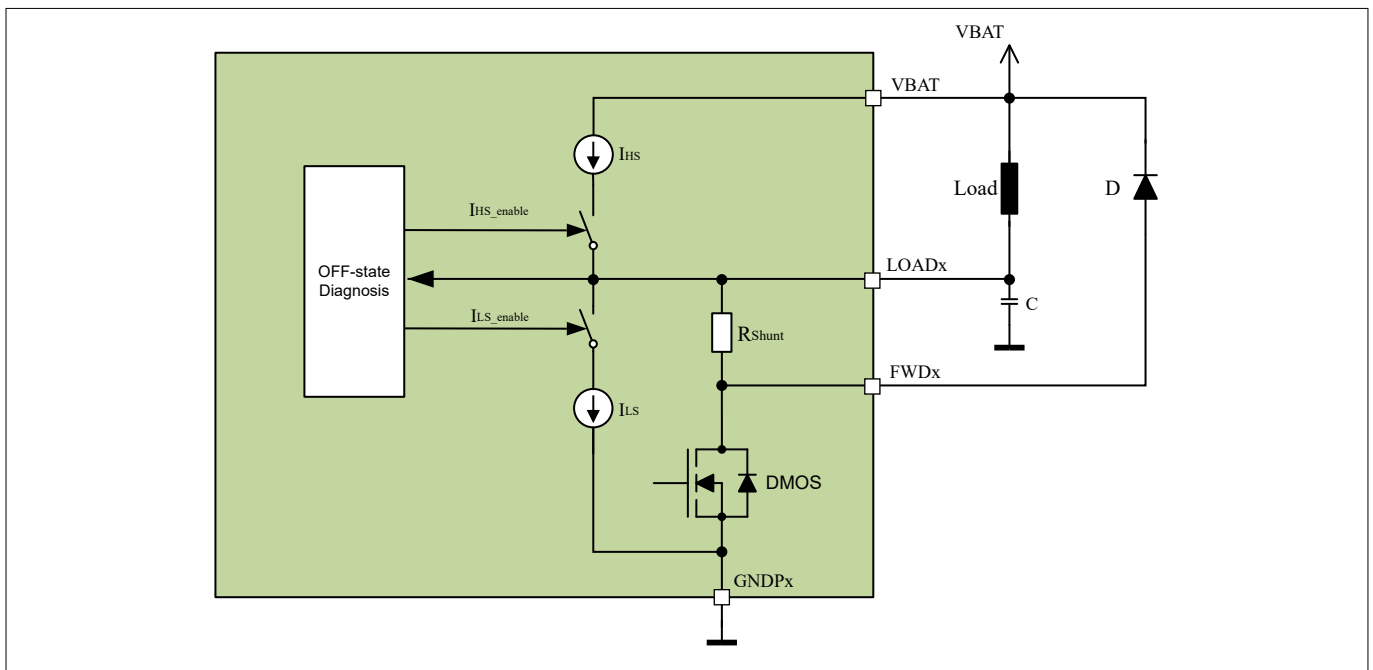
**OFF-state diagnosis**

A channel is in OFF-state if

1. the setpoint is 0 and the <EN\_CH> bit is set to 1 (EN-pin must be high for use of OFF-state diagnosis state machine)
2. the setpoint is non-zero and the <EN\_CH> bit is set to 0.

The first condition can be used to initially test the application circuit. The second condition is present after the ON-state diagnosis has detected a fault.

In OFF-state, the internal high and low side current sources  $I_{HS}$  and  $I_{LS}$  at the LOADx pin are active. The switching configuration and current strength of  $I_{HS}$  and  $I_{LS}$  can be configured in the CH\_CONFIG register.



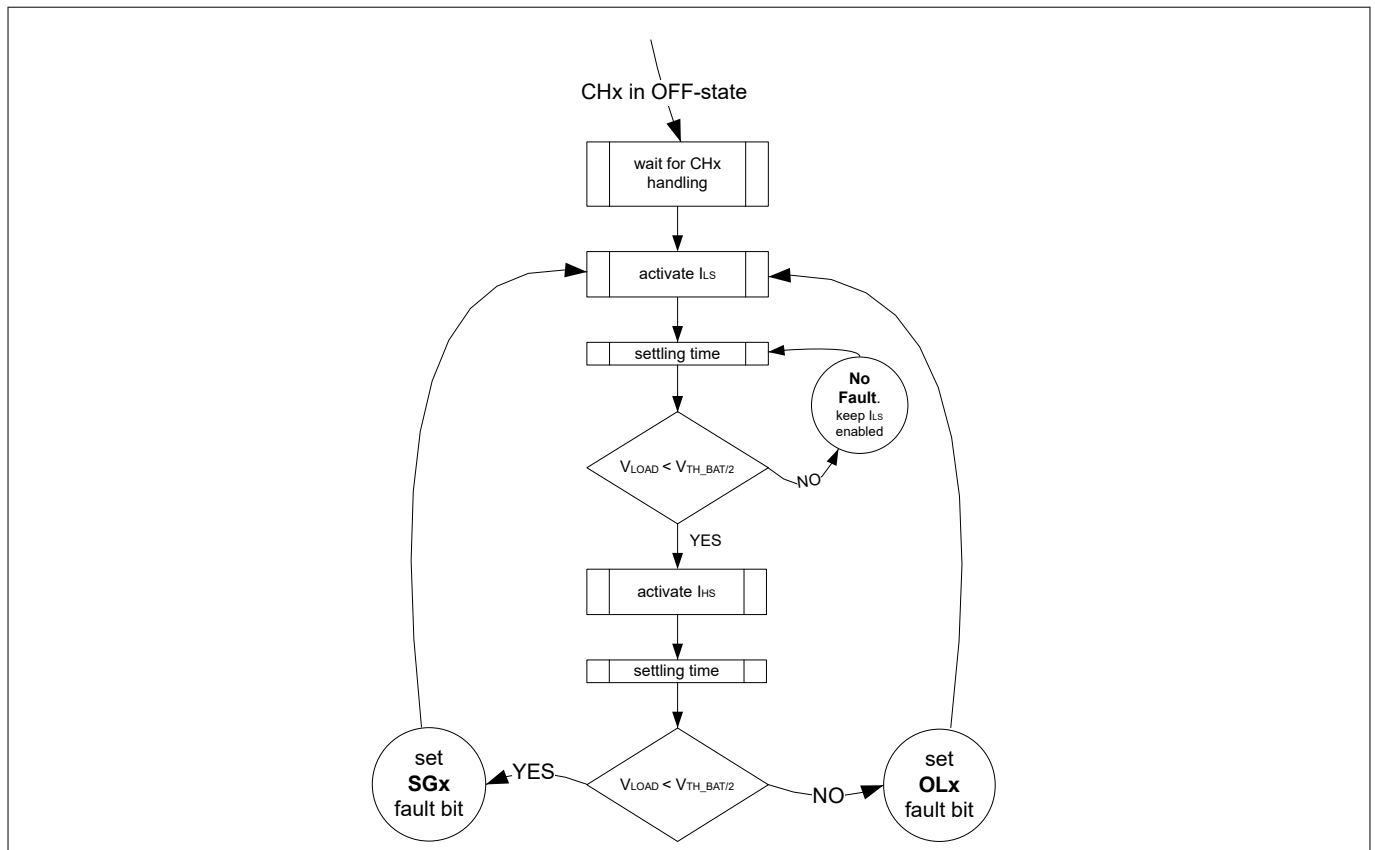
**Figure 14** OFF-state diagnosis circuit

Setting <OFF\_DIAG\_CH> bit in the CH\_CONFIG register to "0", activates the OFF-state diagnosis. The OFF-state diagnosis detects and indicates open load (OL) or short circuit to ground (SG) faults by performing following LOAD pin voltage checks.

1. The low side diagnostic current  $I_{LS}$  is enabled and the high side diagnostic current  $I_{HS}$  is disabled.
  - If  $V_{LOAD} > V_{TH\_BAT/2}$  no fault is detected.
  - If  $V_{LOAD} < V_{TH\_BAT/2}$  the sequence continues.
2. The high side diagnostic current  $I_{HS}$  is enabled and the low side diagnostic current  $I_{LS}$  is disabled.
  - If  $V_{LOAD} > V_{TH\_BAT/2}$  an OL is detected and indicated in the DIAG\_ERR\_CHGR register.
  - If  $V_{LOAD} < V_{TH\_BAT/2}$  a SG is detected and indicated in the DIAG\_ERR\_CHGR register.

The OFF-state diagnosis handles all channels sequentially. The OFF-state diagnosis sequence takes  $T_{off,sequence}$ .

**Functional description**

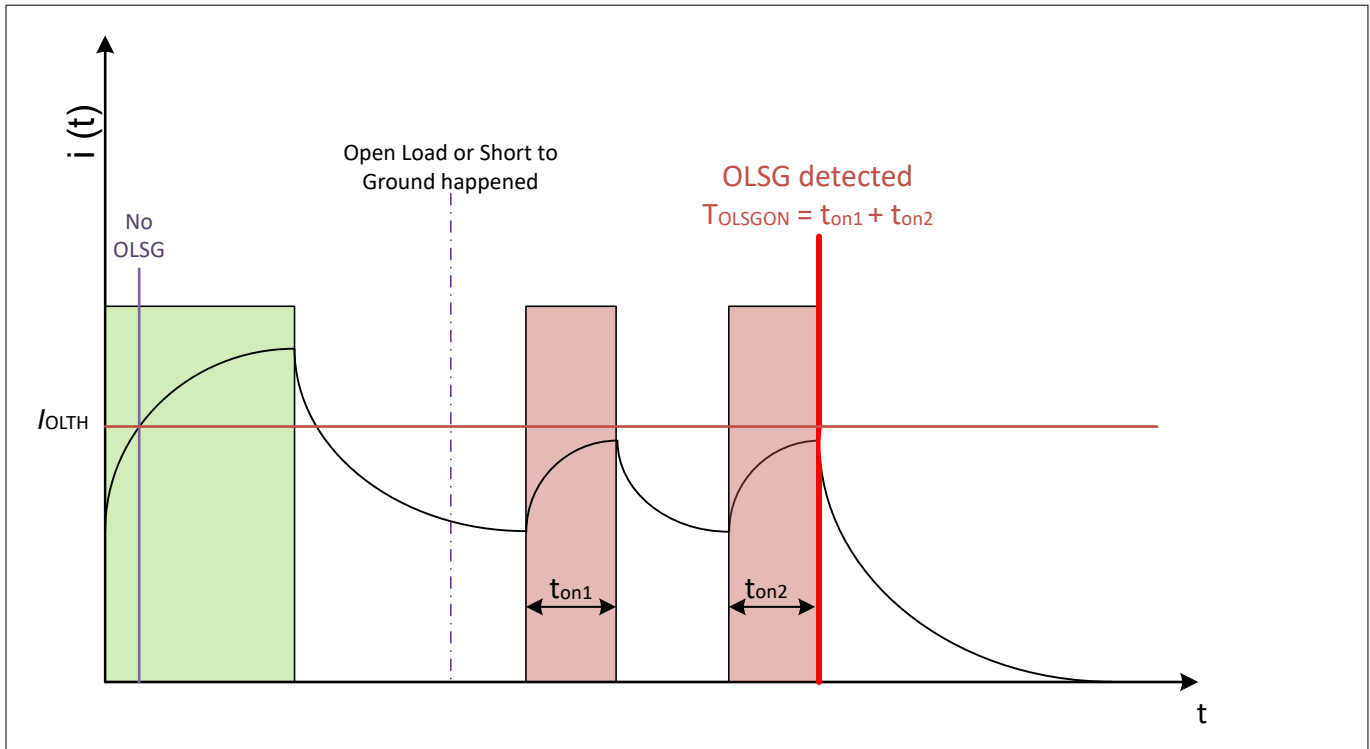


**Figure 15** OFF-state diagnosis sequence

**4.9.2 TDS\_Open Load/Short to Ground (OLSG)**

An open load (OL) and a short circuit to ground (SG) are both reducing the current flowing through the shunt resistor. Therefore the faults cannot be distinguished in ON-state and are summarized as OLSG fault. An OLSG is detected if the cumulated driver on-time equals  $T_{OLSGON}$  and the load current  $I_{LOAD}$  is below the open load threshold  $I_{OLTH}$ .

**Functional description**



**Figure 16** Simplified OLSG detection mechanism

An OLSG fault switches off the respective power stage and is indicated by setting the respective OLSG bit in the DIAG\_ERR\_CHGR register. The device keeps the channel disabled until the fault is removed, the diagnosis bit is cleared and the <EN\_CH> bit is set to “1” again.

$R_{OLmin}$  is the minimum impedance to detect an OL in ON-state via an OLSG fault.

$$R_{OLmin} = \frac{V_{BAT}}{I_{OLTH}} - (R_{LOAD} + R_{shunt} + R_{DSon})$$

**Equation 11**

$R_{SGmax}$  is the maximum impedance to detect an SG in ON-state via an OLSG fault.

$$R_{SGmax} = \frac{R_{LOAD} \cdot (R_{shunt} + R_{DSon})}{R_{OLmin}}$$

**Equation 12**

**4.9.2.1 TDS\_OL-Threshold configuration**

The open load threshold  $I_{OLTH}$  can be set to a fixed threshold and/or a threshold relative to the setpoint via the CH\_CONFIG register. The OLSG diagnosis is disabled by setting both OL-thresholds to 0.

**Fixed OL-Threshold**

A fixed open load threshold is programmable via bitfield <OL\_TH\_FIXED>.

**Functional description**

$$I_{OLTH} = \frac{\langle OL\_TH\_FIXED \rangle \cdot 128 \cdot 2000\text{mA}}{2^{15} - 1}$$

$$I_{OLTH, parallel} = \frac{\langle OL\_TH\_FIXED \rangle \cdot 128 \cdot 4000\text{mA}}{2^{15} - 1}$$

**Equation 13**

Note: The OL detection in direct drive mode is only possible with the fixed threshold configuration.

**Relative OL-Threshold**

The relative threshold refers to the actual setpoint  $I_{set}$  including the dither amplitude  $I_{Dither}$ . A relative open load threshold is adjustable in bitfield  $\langle OL\_TH \rangle$ . The relative open load threshold is disabled by setting  $\langle OL\_TH \rangle$  to 0.

$$I_{OLTH} = (I_{set} + I_{Dither}) \cdot \frac{\langle OL\_TH \rangle}{8}$$

**Equation 14**

Note: The relative threshold is only available in a current control mode.

**Transition phase**

During a transition phase, the fixed OL-threshold is always used. A transition phase takes place after a channel activation or setpoint change. A transition phase lasts for one PWM cycle or maximum for a driver on-time of  $T_{OLSGON}$  (PWM cycle  $> T_{OLSGON}$ ). The transition phase time out can be extended or shortened by configuring  $t_{OLSG\_TIMEOUT}$  in the TON register. After the transition phase has been finished, the OLSG detection swaps from fixed to relative OL-threshold. If the  $\langle OL\_TH\_FIXED \rangle$  bitfield is set to 0, no OLSG will be detected during a transition phase.

$$t_{OLSG\_TIMEOUT} = \frac{(\langle OLSG\_TIMEOUT \rangle \cdot 256 + 255) \cdot 64}{f_{SYS}}$$

**Equation 15**

**4.9.3 TDS\_OLSG Warning**

An additional OLSG-Warning checks if the voltage at the LOAD pin is greater than  $V_{TH\_BAT/2}$  at the end of the freewheeling phase. The blanking time  $t_{OLwindow}$  is triggered every time the outputstage is switched off. If the output stage is switched on within  $t_{OLwindow}$ , no voltage check is possible. This is indicated by setting  $\langle OLSG\_WARN\_CHK\_NOK \rangle$  in the DIAG\_WARN\_CHGR register to 1. The  $\langle OLSG\_WARN\_CHK\_NOK \rangle$  bit is cleared by reading.

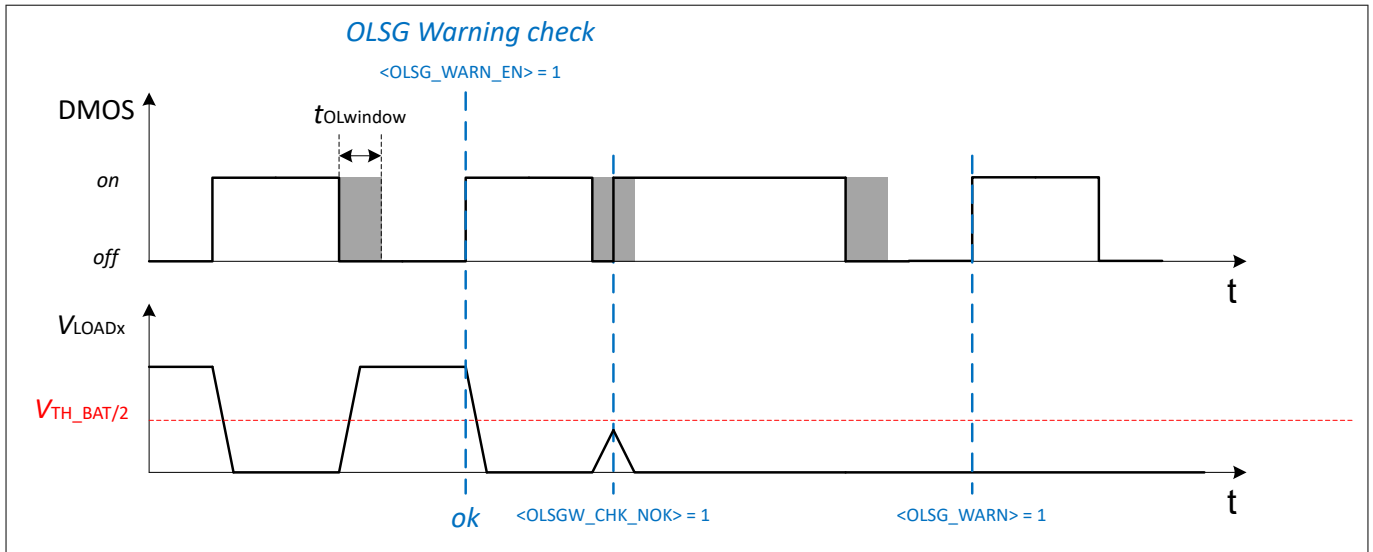
If the check was successful, a detected OLSG-warning is indicated by setting  $\langle OLSG\_WARN \rangle$  in the DIAG\_WARN\_CHGR register to 1. The OLSG-warning is initially enabled and can be disabled by clearing the bit  $\langle OLSG\_WARN\_EN \rangle$  in the CTRL register. The OLSG-warning check bit  $\langle OLSG\_WARN\_CHK\_NOK \rangle$  is set to 1 after clearing  $\langle OLSG\_WARN \rangle$  in the DIAG\_WARN\_CHGR register.

$t_{OLwindow}$  can be configured in the CTRL register.

$$t_{OLwindow} = \frac{(\langle OLSG\_WARN\_WINDOW \rangle + 1) \cdot 64}{f_{SYS}}$$

**Equation 16**

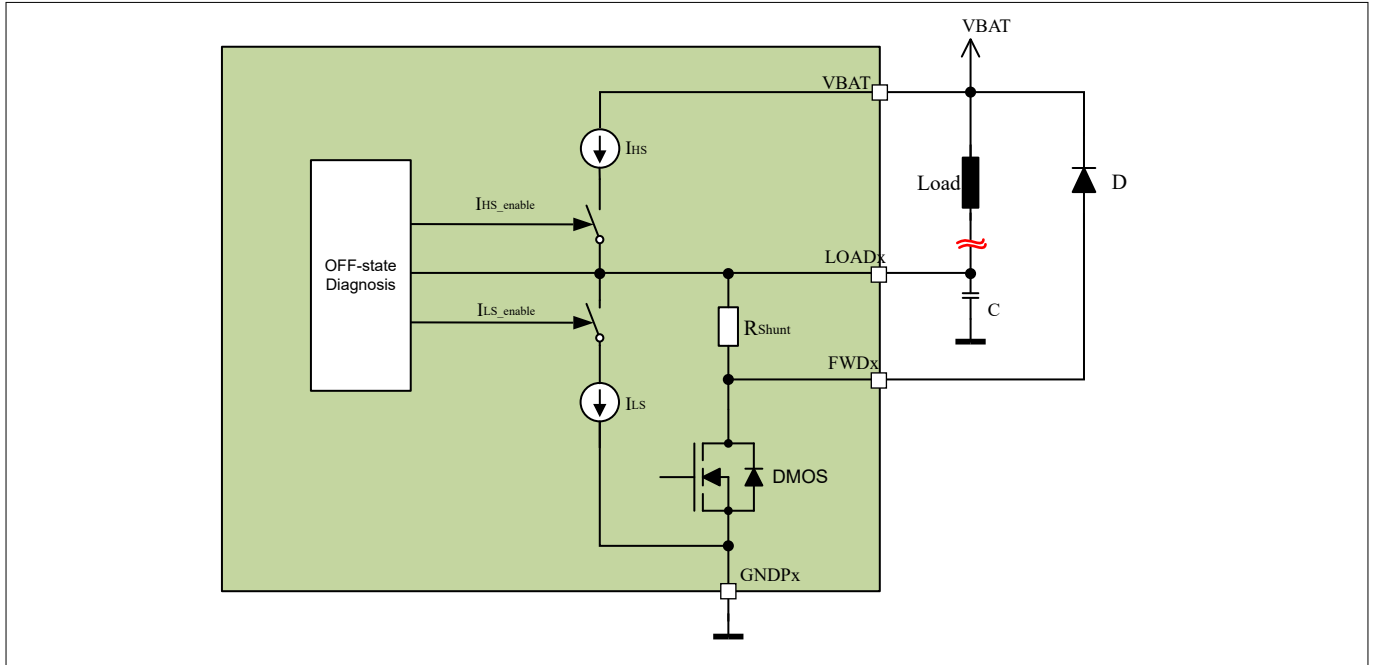
**Functional description**



**Figure 17** OLSG-Warning and OLSG warning check overview

**4.9.4 TDS\_Open load (OL)**

In ON-state, an open load is indicated via the <OLSG> bit in the DIAG\_ERR\_CHGR register. The final fault discrimination to identify an open load is done by the OFF-state diagnostic. The device indicates the fault by setting the respective <OL> bit in the DIAG\_ERR\_CHGR register. The device keeps the channel disabled until the fault is removed, the diagnosis bit is cleared and the <EN\_CH> bit is set to “1” again.

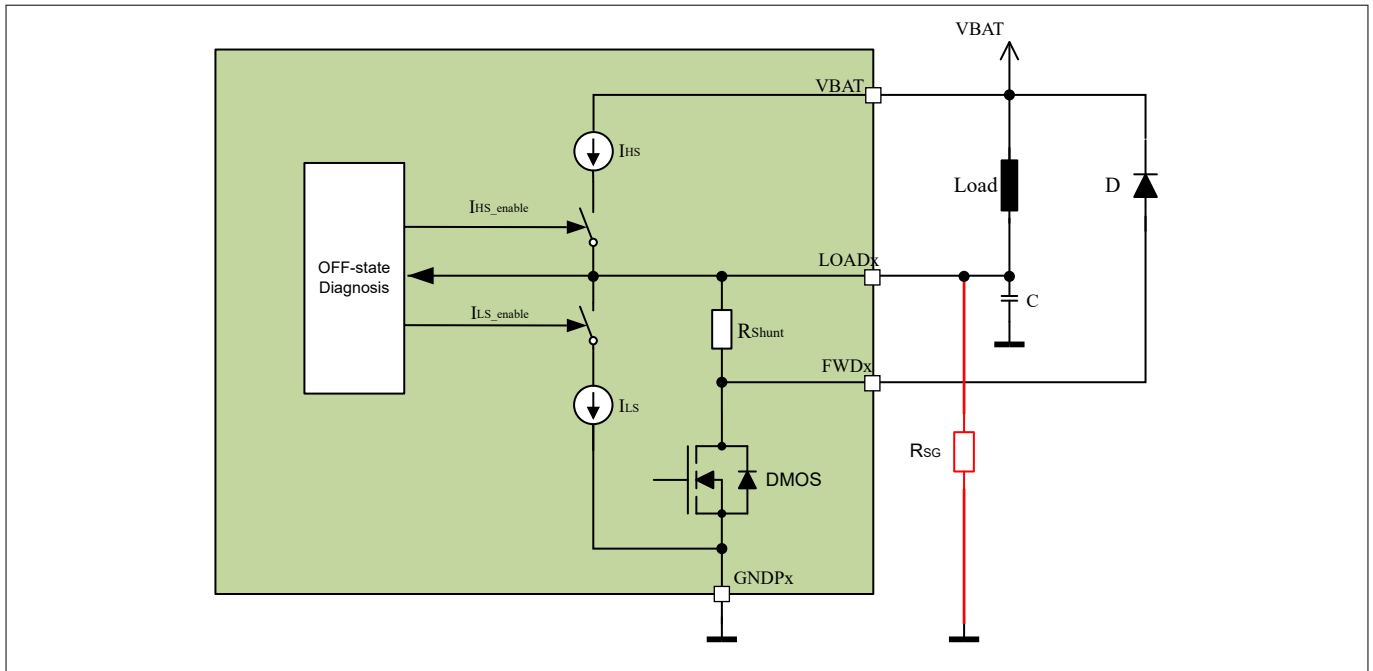


**Figure 18** Open load

**4.9.5 TDS\_Short circuit ground (SG)**

In the ON-state, a short circuit to ground is detected via the <OLSG> bit in the DIAG\_ERR\_CHGR register. The final fault discrimination to identify a short circuit to ground is done by the OFF-state diagnostic. The device indicates the fault by setting the respective <SG> bit in the DIAG\_ERR\_CHGR register. The device keeps the channel disabled until the fault is removed, the diagnosis bit is cleared and the <EN\_CH> bit is set to “1” again.

**Functional description**



**Figure 19 Short to Ground**

**4.9.6 TDS\_Overcurrent (OC)**

An overcurrent fault (OC) is an unintended low impedance connection between the LOAD terminal and the battery rail, therefore bypassing the load impedance.

An overcurrent is detected if a current flow through the power stage exceeds  $I_{OC}$ . Therefore the power stage must be turned on for a short period of time  $t_{OCOn}$  to detect an OC in OFF-state. The driver on-time  $t_{OCOn}$  can be triggered by setting the <OC\_DIAG\_EN> bit in the CH\_CONFIG register and the respective <EN\_CH> bit in the CH\_CTRL register to 1. The driver on-time  $t_{OCOn}$  must be configured before executing the OC detection.

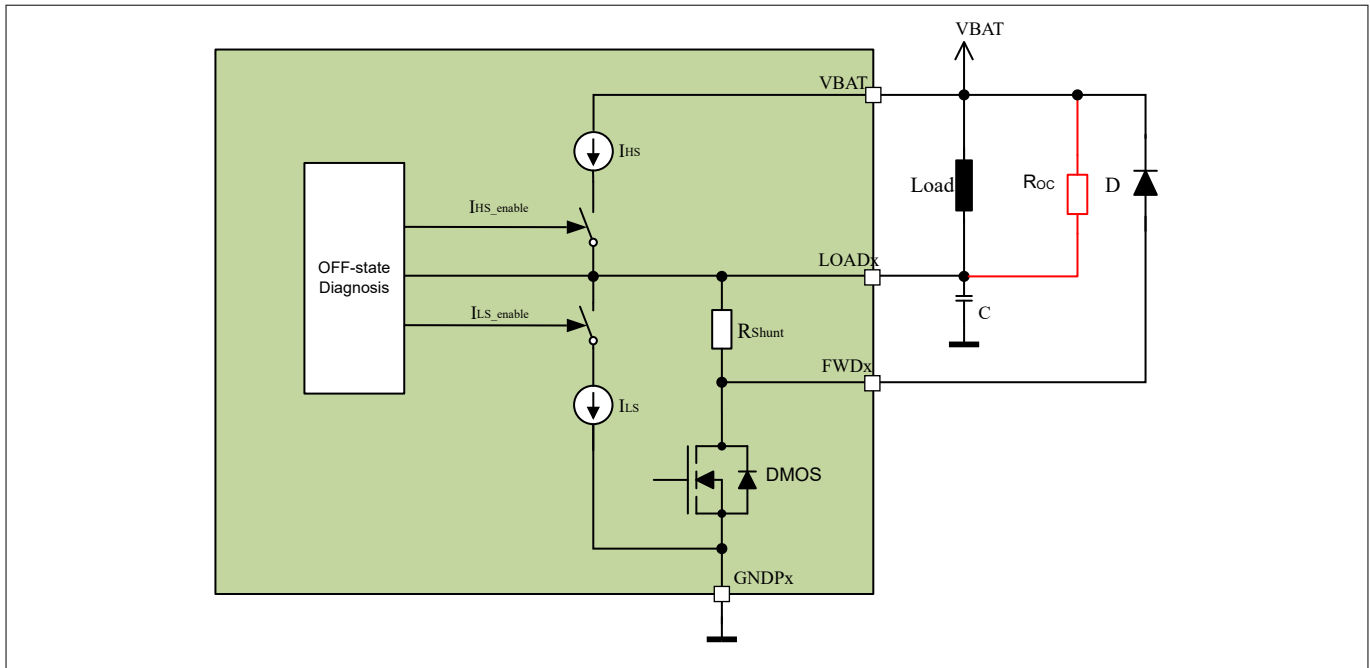
$$t_{OCOn} = \frac{(<TON\_MANT> + 1) \cdot 2^{<EXP>}}{f_{SYS}}$$

**Equation 17**

The mantissa <TON\_MANT> is located in the TON register and the exponent <EXP> is located in DITHER\_CLK\_DIV. An enabled OFF-state diagnosis is kept active during  $t_{OCOn}$ .

<OC\_DIAG\_EN> is reset after  $t_{OCOn}$  has expired. If an overcurrent is present, the <EN\_CH> bit is cleared and the indication bit <OC> in the DIAG\_ERR\_CHGR register is set to 1. The device keeps the channel disabled until the fault is removed, the diagnosis bits are cleared by two clear commands and the <EN\_CH> bit is set to “1” again.

**Functional description**



**Figure 20**      **Overcurrent**

**4.9.7**      **TDS\_Register/OTP ECC**

A register/OTP (one time programmable memory) error will be detected by a continuous error checking and correction (ECC) mechanism. If a correction is not possible, a register/OTP ECC error is present and the  $\langle REG\_ECC\_ERR \rangle / \langle OTP\_ECC\_ERR \rangle$  bit in the GLOBAL\_DIAG2 register will be set. The  $\langle OTP\_ECC\_ERR \rangle$  can only be cleared by sending two clear commands. A register ECC error disables all power stages and the product enters the Operation State "Config Mode". The  $\langle OTP\_VIRGIN \rangle$  bit in the GLOBAL\_DIAG2 indicates a non programmed OTP-memory. This bit must always be 0.

**4.9.8**      **TDS\_Built in Self Test (BIST)**

The device provides a self-test in order to check the built in error detection and correction feature for safety critical registers. The BIST tests the ability to detect correctable and uncorrectable errors. The BIST can only be triggered in Config Mode by writing a '1' to the  $\langle SMU\_SLF\_TST\_EN \rangle$  bit in the SFF\_BIST register. After the safety flip-flop BIST sequence is completed, the bits  $\langle SMU\_SLF\_TST\_DONE \rangle$ ,  $\langle SMU\_SLF\_TST\_UERR \rangle$  and  $\langle SMU\_SLF\_TST\_CERR \rangle$  are set to indicate a finished test sequence.

The safety flip-flop BIST result is stored in the  $\langle SMU\_SLF\_TST\_FAIL \rangle$  bit in SFF\_BIST register. All result and status bits in the SFF\_BIST register are cleared on writing 0. A successfully tested safety flip-flop error (uncorrectable fault) sets the respective error bits  $\langle REG\_ECC\_ERR \rangle$  in the GLOBAL\_DIAG2 register.

**4.9.9**      **Electrical characteristics diagnostic functions**

**Table 15**      **Electrical characteristics diagnostic functions**

$T_J = -40^\circ C$  to  $150^\circ C$ ;  $V_{DD} = 4.5 - 5.5 V$ ;  $V_{IO} = 3.0 - 5.5 V$ ;  $V_{BAT} = 6 - 18 V$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OLSG threshold single	$I_{OLTH}$	0	-	492	mA	fixed OLSG threshold in single channel mode

**(table continues...)**

**Functional description**

**Table 15 (continued) Electrical characteristics diagnostic functions**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OLSG threshold parallel	$I_{OLTH,parallel}$	0	-	984	mA	fixed OLSG threshold in parallel mode
OLSG filter detection time	$T_{OLSGON}$	-	$2^{15}$	-	cycles	$f_{SYS}$ cycles
OFF-state LOADx threshold voltage	$V_{TH\_BAT/2}$	-	$V_{BAT}/2$	-	V	
OFF-state sequence time	$T_{off,sequence}$	1.2	-	4.8	ms	
Diagnosis Current 0	$I_{HS}$ $I_{LS}$	30	80	120	$\mu\text{A}$	$\langle I\_DIAG \rangle = 00_B$
Diagnosis Current 1	$I_{HS}$ $I_{LS}$	105	190	275	$\mu\text{A}$	$\langle I\_DIAG \rangle = 01_B$
Diagnosis Current 2	$I_{HS}$ $I_{LS}$	510	720	910	$\mu\text{A}$	$\langle I\_DIAG \rangle = 10_B$
Diagnosis Current 3	$I_{HS}$ $I_{LS}$	910	1250	1520	$\mu\text{A}$	$\langle I\_DIAG \rangle = 11_B$

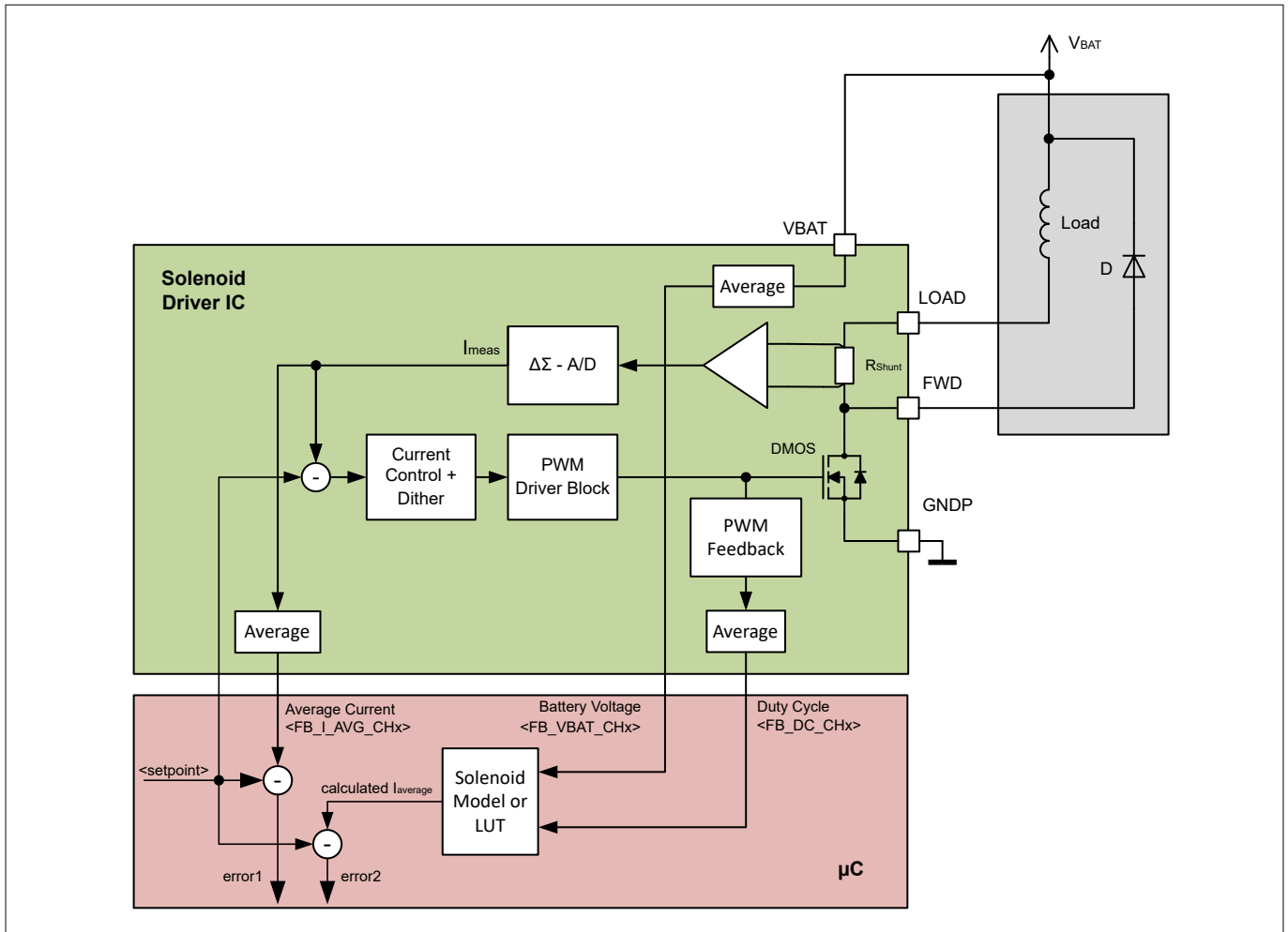
## 4.10 Current supervision

### 4.10.1 TDS\_Independent current feedback

The device provides independent current feedback paths to the microcontroller for plausibility checks on the load current. The average load current measured via the internal shunt can be read back directly. The independently measured duty cycle and battery voltage can be used to calculate the average load current using a load model.



**Functional description**



**Figure 21** Current supervision

**4.10.2 TDS\_Average feedback values**

The feedback values are provided in the registers FB\_DC, FB\_VBAT, FB\_I\_AVG. The feedback values averaged over the configured measurement period  $T_{meas}$  (see "Channel modes"). The register contents are updated after each measurement period  $T_{meas}$ .

The feedback values can be calculated as follows:

- Measurement period:

$$T_{meas} = \frac{\langle TP\_MANT \rangle \cdot 2^{\langle EXP \rangle}}{f_{SYS}}$$

**Equation 18**

- PWM on time:

$$t_{on} = \frac{\langle TO\_MANT \rangle \cdot 2^{\langle EXP \rangle}}{f_{SYS}}$$

**Equation 19**

- Duty cycle:

**Functional description**

$$DC = \frac{\langle TO\_MANT \rangle}{\langle TP\_MANT \rangle}$$

**Equation 20**

- Battery voltage:

$$V_{BAT} = 41.47V \cdot \frac{\langle VBAT\_AVG\_MANT \rangle}{\langle TP\_MANT \rangle}$$

**Equation 21**

- Average load current (signed):

$$I_{avg} = 4A \cdot \frac{\langle I\_AVG\_MANT \rangle}{\langle TP\_MANT \rangle}$$

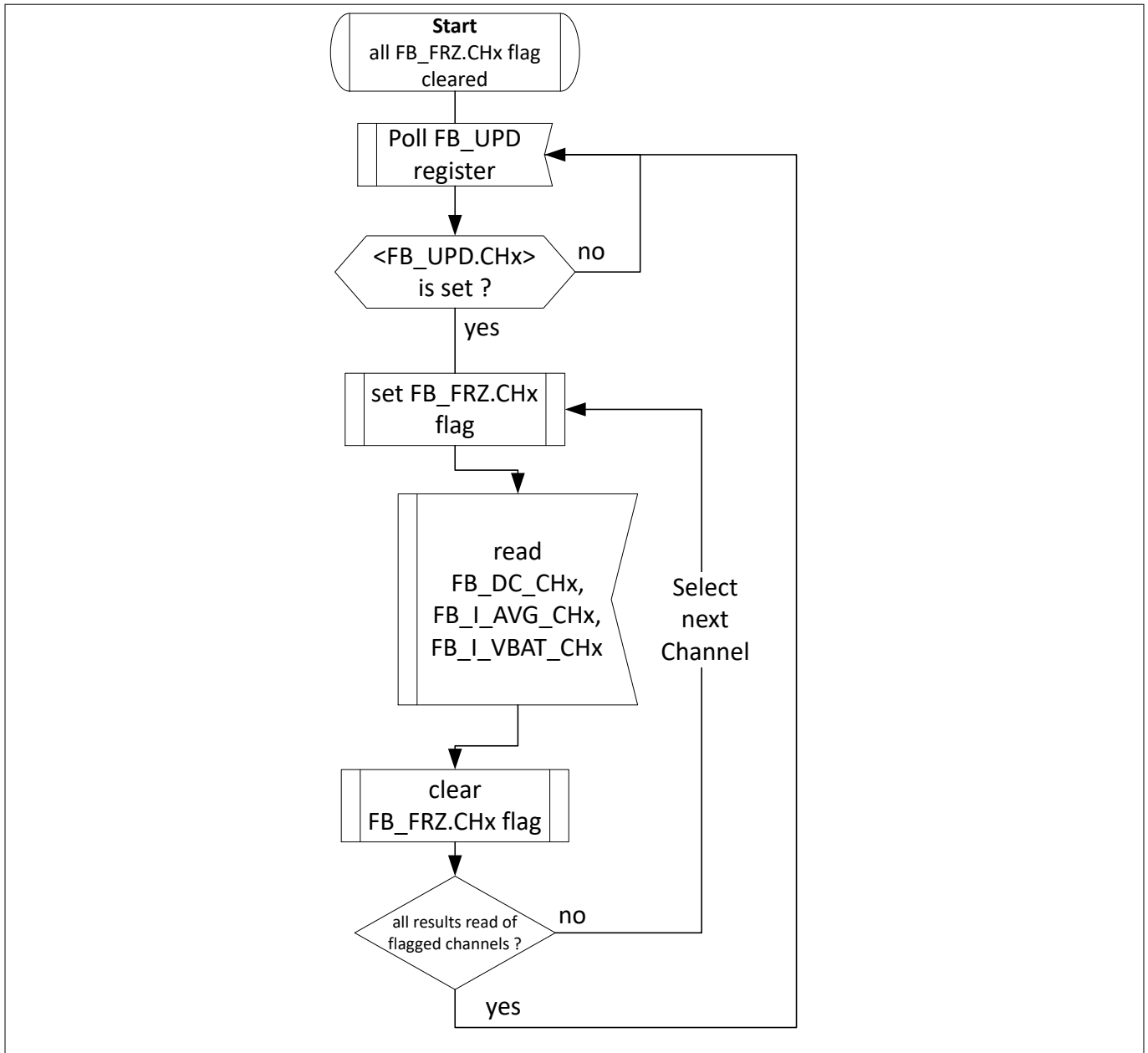
**Equation 22**

The bitfields <TP\_MANT> and <TO\_MANT> are located in the FB\_DC register. The bitfields <VBAT\_AVG\_MANT> and <EXP> are located in the FB\_VBAT register. The bitfield <I\_AVG\_MANT> is located in the FB\_I\_AVG register. The bitfield <I\_AVG\_MANT> represents a signed current value (two's complement).

### **4.10.3 TDS\_Update/Freeze Mechanism**

The Update/Freeze mechanism should be applied for a correct readout of each measurement sample set. The IC indicates new feedback data by setting the respective <CH> bit in the FB\_UPD register to 1. Setting <CH> bit in the FB\_FRZ register to 1, stops the updating and freezes the latest measurement results of the feedback registers FB\_DC, FB\_VBAT, FB\_I\_AVG, FB\_PERIOD\_MIN\_MAX, FB\_IMIN\_IMAX. Setting the <CH> bit in the FB\_FRZ register to 0, also clears the respective <CH> bit in the FB\_UPD register and enables the update of the feedback values. Following state diagram shows a recommendation for the readout of the feedback values.

**Functional description**



**Figure 22** Readout proposal for feedback values

**4.10.4 TDS\_lavg16, minimum/maximum current/PWM feedback**

The IC provides the average load current  $I_{avg16}$  over a free running period of  $2^{16}$  system clocks, as a signed 16 bit value in the FB\_I\_AVG\_s16 register. This value is not intended to be used while in closed loop operation or for current supervision. The value is provided as additional information and can be used for calibration purposes.

$$I_{avg16} = 4A \cdot \frac{\langle I_{AVG\_s16} \rangle}{2^{16} - 1}$$

**Equation 23**

The IC provides measurements of the minimum (min) and maximum (max) current and PWM period. The min/max values represent the highest/lowest current and shortest/longest PWM period captured during a measurement period  $T_{meas}$ . If no measurement period  $T_{meas}$  is defined, the min/max registers are

**Functional description**

permanently updated when a new minimum or maximum current/PWM has been measured. The current values are held in the FB\_IMIN\_IMAX register and the PWM values can be read out from the FB\_PERIOD\_MIN\_MAX register. The current values in the FB\_IMIN\_IMAX register are represented as a signed 9 bit value (two's complement).

$$I_{min} = 4A \cdot \frac{\langle IMIN \rangle}{2^9 - 1}$$

$$I_{max} = 4A \cdot \frac{\langle IMAX \rangle}{2^9 - 1}$$

**Equation 24**

$$T_{PWM\_min} = \langle PMIN \rangle \cdot \frac{256}{f_{SYS}}$$

$$T_{PWM\_max} = \langle PMAX \rangle \cdot \frac{256}{f_{SYS}}$$

**Equation 25**

**4.11 Protection functions**

**4.11.1 TDS\_Overtemperature protection**

The device provides protection against overtemperature by measuring the central IC temperature and every power stage temperature. If an overtemperature  $T_{J,ot}$  is measured, the respective power stage is switched off and the respective <OT> bit in the DIAG\_ERR\_CHGRx register is set. A central overtemperature of the IC disables all power stages and sets the <COTERR> bit in the GLOBAL\_DIAG0 register.

If the respective power stage has cooled down to  $T_{J,ot} - T_H$ , the power stage can be re-enabled. A pre-warning bit in the diagnostic register is set, if the power stage temperature exceeds the pre-warning threshold  $T_p$ .

The overtemperature detection can be tested by setting the <OT\_TEST> bit in the GLOBAL\_CONFIG register to "1". This test sets the overtemperature threshold to the lowest possible value and the according overtemperature indication bits should be asserted.

The device provides a temperature feedback  $T_{FB}$  which can be read out from the bitfield <TEMP\_VALUE> in the FB\_VOLTAGE2 register. The temperature feedback  $T_{FB}$  is given by

$$T_{FB} = \frac{\langle TEMP\_VALUE \rangle \cdot 0.000593 - 0.819^{*})}{-0.0016^{*})} \text{ } ^\circ\text{C}$$

**Equation 26**

If a higher accuracy of the temperature feedback  $T_{FB}$  is required, a calibration of the parameters <sup>\*)</sup> have to be done on system level.

**4.11.2 TDS\_Overcurrent protection**

The maximum current through every power stage of the device is limited. An overcurrent condition is detected if the load current exceeds  $I_{OC}$ . The detection of an overcurrent takes maximum  $t_{OC,DETECT}$ . An overcurrent causes the channel to be switched off and is indicated by setting the respective <OC> bit in the DIAG\_ERR\_CHGR register to 1. The <OC> bit must be cleared by two SPI write commands.

**Functional description**

**4.11.3 Electrical characteristics protection functions**

**4.11.3.1 Overtemperature protection**

**Table 16 Overtemperature protection**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature pre-warning threshold	$T_P$	150	-	175	$^{\circ}\text{C}$	
Overtemperature threshold	$T_{J,OT}$	175	-	200	$^{\circ}\text{C}$	
Thermal hysteresis	$T_H$	10	-	15	$^{\circ}\text{C}$	
Temperature feedback accuracy	$T_{FB}$	-20	-	20	$^{\circ}\text{C}$	

**4.11.3.2 Overcurrent protection**

**Table 17 Overcurrent protection**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

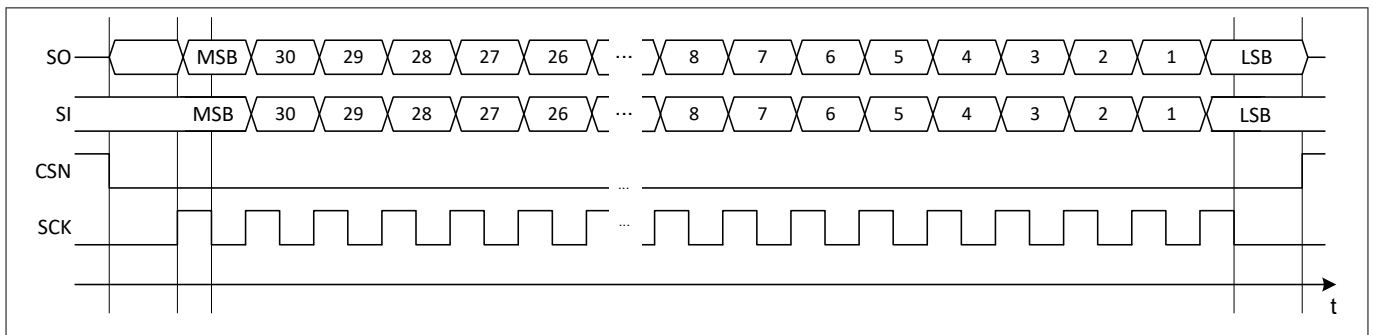
Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent protection threshold	$I_{OC}$	2.05	-	6	A	
Overcurrent protection filter time	$t_{OC,DETECT}$	-	-	1.5	$\mu\text{s}$	$f_{SYS} = 28\text{ MHz}$

## 5 Serial peripheral interface (SPI)

### 5.1 Description of interface

#### 5.1.1 TDS\_General information

The communication interface is based on a standard serial peripheral interface (SPI). The SPI is a full duplex synchronous serial slave interface which uses four signal lines: SO, SI, SCK, and CSN. Data is transferred by the lines SI and SO at the data rate given by SCK. The falling edge of CSN indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCK and shifted out on line SO at the rising edge of SCK. Each access must be terminated by a rising edge of CSN. A counter ensures that data is taken only when 32 bits have been transferred. If the number of bits transferred is not 32, the data frame is ignored.



**Figure 23** SPI signal overview

#### 5.1.2 TDS\_Cyclic redundancy check (CRC)

An 8-bits cyclic redundancy code (CRC-8 SAE-J1850) is added to all SPI communication frames to detect corrupt data and to avoid wrong configuration of the IC. The CRC-8 SAE-J1850 polynomial is used for the calculation:

$$x^8 + x^4 + x^3 + x^2 + 1 \text{ or } 0x1D$$

*Note: CRC is supported by the flexible CRC engine (FCE) of Aurix TC26x, TC27x and TC29x.*

The initial value of the CRC-byte is 0xFF. The CRC result is XOR operated with 0xFF. The CRC-byte is located in the most significant byte of the SPI frame. The byte-sequence for the CRC calculation is as follows:

1<sup>st</sup> byte: SPI frame[7:0]

2<sup>nd</sup> byte: SPI frame[15:8]

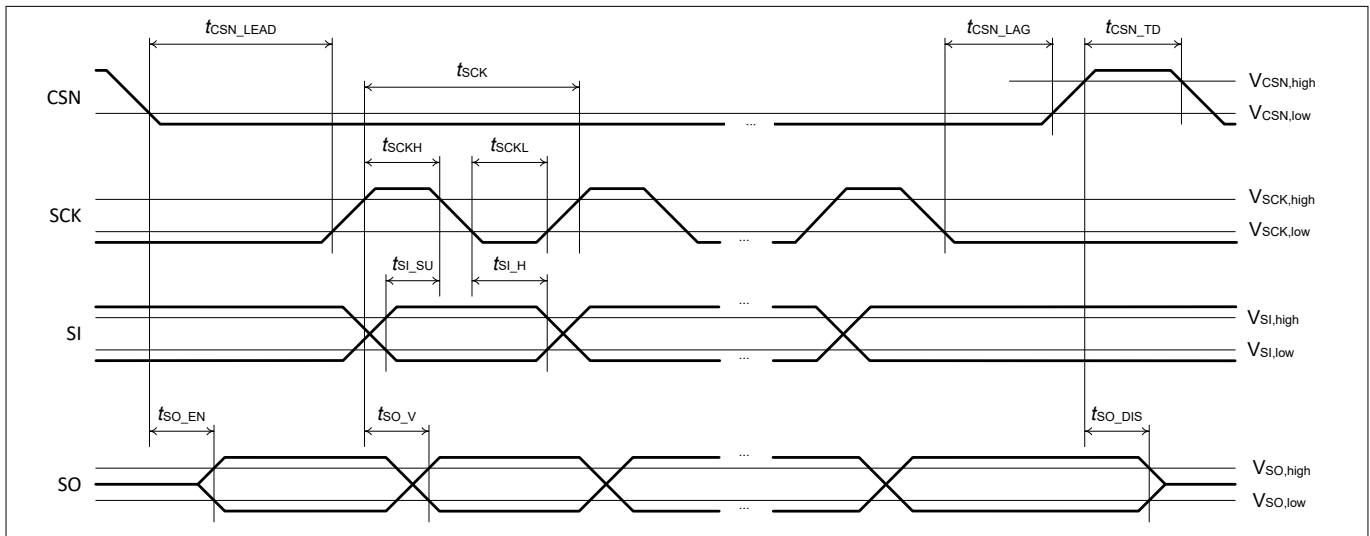
3<sup>rd</sup> byte: SPI frame[23:16]

Different generator polynomials are supported by the frame encoder/decoder entity definition, but the specific implementation is not part of the reuse module. The product designer has to modify the frame encoder/decoder source code within the project design environment accordingly.

The CRC byte is located in the most significant frame byte [31:24]. Whenever a SPI frame CRC error is detected, a SPI 16 bit reply frame indicating the SPI CRC error status is send in the subsequent SPI transaction.

The CRC check can be disabled by setting the <CRC\_EN> bit in the GLOBAL\_CONFIG register to "0".

### 5.1.3 TDS\_Timing Diagram



**Figure 24 SPI Signal Timing Diagram**

### 5.1.4 Electrical characteristics SPI interface

**Table 18 Electrical characteristics SPI interface**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Serial clock high time	$t_{SCKH}$	50	-	-	ns	
Serial clock low time	$t_{SCKL}$	50	-	-	ns	
Enable lead time	$t_{CSN\_LEAD}$	250	-	-	ns	falling CSN to rising SCK
Enable lag time	$t_{CSN\_LAG}$	250	-	-	ns	falling SCK to rising CSN
Transfer delay time	$t_{CSN\_TD}$	600	-	-	ns	rising CSN to falling CSN
Data setup time	$t_{SI\_SU}$	20	-	-	ns	required time SI to falling SCK
Data hold time	$t_{SI\_H}$	20	-	-	ns	required time falling SCK to SI
Output disable time	$t_{SO\_DIS}$	-	-	200	ns	rising CSN to SO tri-state $C_L = 150\text{ pF}$
Output enable time	$t_{SO\_EN}$	-	-	200	ns	falling CSN to SO valid $C_L = 150\text{ pF}$
Output data valid time	$t_{SO\_V}$	-	-	100	ns	$C_L = 150\text{ pF}$

**(table continues...)**

**Serial peripheral interface (SPI)**

**Table 18 (continued) Electrical characteristics SPI interface**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ;  $V_{DD} = 4.5 - 5.5\text{ V}$ ;  $V_{IO} = 3.0 - 5.5\text{ V}$ ;  $V_{BAT} = 6 - 18\text{ V}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Functional range SPI clock frequency (SCK)	$f_{SCK}$	-	-	8	MHz	
SPI watchdog decrement frequency	$f_{SPI,WD}$	-	$f_{SYS} / 2^{14}$	-	MHz	$f_{SYS} = 28\text{ MHz}$
Input pin capacitance (CSN, SCK, SI, CLK)	$C_{IN}$	-	-	10	pF	$V_{bias} = 2\text{ V}$ ; $V_{test} = 20\text{ mVpp}$ ; $f = 1\text{ MHz}$
Output pin capacitance (SO)	$C_{SO,HIZ}$	-	-	15	pF	Tri-state Output $V_{bias} = 2\text{ V}$ ; $V_{test} = 20\text{ mVpp}$ ; $f = 1\text{ MHz}$
SPI High Threshold Voltage (SI, SCK, CSN)	$V_{SI,high}$ $V_{SCK,high}$ $V_{CSN,high}$	-	-	2	V	
SPI Low Threshold Voltage (SI, SCK, CSN)	$V_{SI,low}$ $V_{SCK,low}$ $V_{CSN,low}$	0.8	-	-	V	
SPI Input hysteresis (SI, SCK, CSN)	$V_{IN,HYS,SI}$ $V_{IN,HYS,SCK}$ $V_{IN,HYS,CSN}$	-	50	-	mV	
SPI output high voltage (SO)	$V_{SO,high}$	$V_{IO} - 0.5$	-	$V_{IO}$	V	pull down current $I_{SO} = -0.5\text{ mA}$ / $3.0\text{ V} < V_{IO} < 5.5\text{ V}$
SPI output low voltage (SO)	$V_{SO,low}$	0	-	0.5	V	pull up current $I_{SO} = 0.5\text{ mA}$
SPI output leakage current (SO)	$I_{SO,OFF}$	-10	-	10	$\mu\text{A}$	$V_{CSN} > V_{CSN,high}$ $0\text{ V} < V_{SO} < V_{IO}$
Pull down current (SI, SCK)	$I_{PD,SI}$ $I_{PD,SCK}$	10	-	50	$\mu\text{A}$	$V_{IN} = 2\text{ V}$
Pull up current (CSN)	$I_{PU,CSN}$	-50	-	-10	$\mu\text{A}$	$V_{CSN} = 0.8\text{ V}$



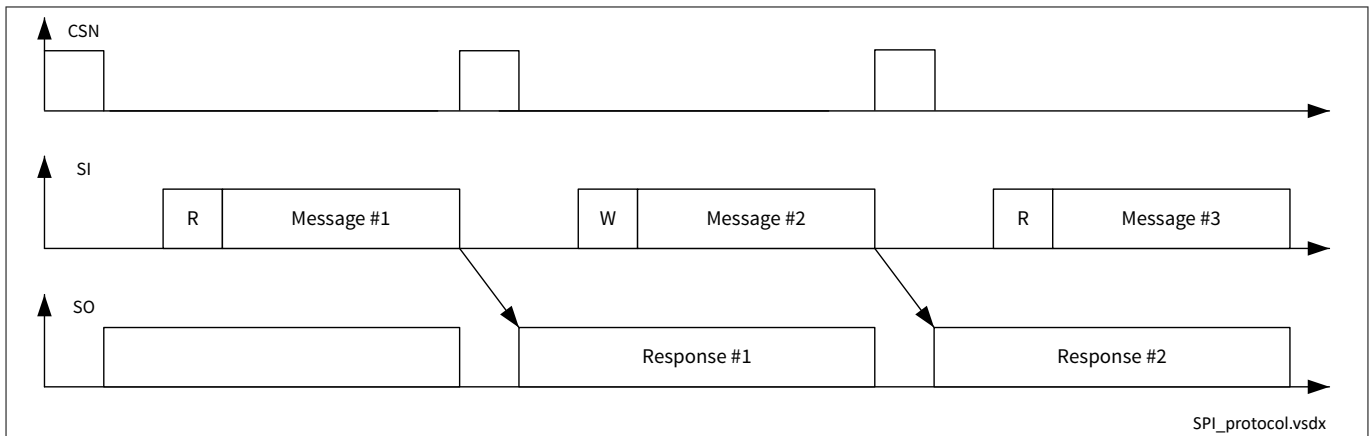
**Serial peripheral interface (SPI)**

**5.2 Description of protocol**

**5.2.1 TDS\_Data flow**

The message from the microcontroller must be sent MSB first. The data from the SO pin is sent MSB first. For each command received at the SI pin of the SPI interface, a serial data stream is returned at the same time on the SO pin. The content of the SO data frame is dependent on the command which was received on the SI pin during the previous frame. A READ command (R/W = 0) returns the contents of the addressed register one SPI frame later. The data bits in the READ command are ignored.

A WRITE command (R/W = 1) will write the data bits in the SPI word to the addressed register. The actual contents of addressed register will be returned to the SPI master (microcontroller) during the next SPI frame.



**Figure 25 SPI protocol**

**5.2.2 TDS\_SPI watchdog**

An SPI watchdog checks the communication on the SPI bus. The SPI watchdog can be enabled by setting <SPI\_WD\_EN> in the GLOBAL\_CONFIG register.

If the SPI watchdog is enabled, the <WD\_TIME> value in the WD\_RELOAD register is constantly decremented with  $f_{SPI,WD}$ . In order to avoid a SPI watchdog error, the WD\_RELOAD register must be permanently updated.

If the <WD\_TIME> value of the WD\_RELOAD register transitions from 1 to 0, the <SPI\_WD\_ERR> bit in the GLOBAL\_DIAG0 register is asserted and the IC transits to Config Mode.

As long as a SPI watchdog fault is present the device cannot enter Mission Mode. The SPI error indication bit <SPI\_WD\_ERR> is set to 0 if the WD\_RELOAD register contains a non-zero value.

The SPI watchdog timeout  $t_{SPI,WD}$  is given by:

$$t_{SPI,WD} = \frac{\langle WD\_TIME \rangle}{f_{SPI,WD}}$$

**Equation 27**

**5.2.3 SPI frame definition**

**5.2.3.1 TDS\_MOSI - Write frame**

MOSI SPI write frame

Data in frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

**Serial peripheral interface (SPI)**

CRC								Address							R/W	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0
Data																

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)
Address	23:17	Address field
R/W	16	MOSI Read/Write Indicator 0 <sub>B</sub> : Read operation 1 <sub>B</sub> : Write operation
Data	15:0	Data bits are defined in register description

**5.2.3.2 TDS\_MOSI - Read frame**

MOSI SPI read frame  
 Data in frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC								-							R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)
-	23:17	Don't care
R/W	16	MOSI Read/Write Indicator 0 <sub>B</sub> : Read operation 1 <sub>B</sub> : Write operation
Address	15:0	Read Address

**5.2.3.3 TDS\_MISO - 16 bit reply frame**

MISO SPI 16 bit reply frame  
 16 bit data out frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC								Reply Mode		Status					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)

**Serial peripheral interface (SPI)**

Field	Bits	Description
Reply Mode	23:22	Indicates type of reply frame: 00 <sub>B</sub> : 16 bit Reply Frame 01 <sub>B</sub> : 22 bit Reply Frame 10 <sub>B</sub> : Critical Fault Frame
Status	21:17	Status indication of the current Frame: 00 <sub>B</sub> : no error 01 <sub>B</sub> : SPI frame error 10 <sub>B</sub> : Parity/CRC error 11 <sub>B</sub> : Write to read only register 100 <sub>B</sub> /101 <sub>B</sub> /110 <sub>B</sub> : Internal bus fault <i>NOTE: The highest priority has the lowest encoding</i>
R/W	16	Indicator mirrored from previous MOSI frame 0 <sub>B</sub> : Read indicator 1 <sub>B</sub> : Write indicator
Data	15:0	Data bits are defined in register description

**5.2.3.4 TDS\_MISO - 22 bit reply frame**

MISO SPI 22 bit reply frame  
 22 bit data out frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC									0	1	Data				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data (cont'd)															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)
Reply Mode	23:22	Indicates type of reply frame: 00 <sub>B</sub> : 16 bit Reply Frame 01 <sub>B</sub> : 22 bit Reply Frame 10 <sub>B</sub> : Critical Fault Frame
Data	21:0	22 data bits used for feedback registers defined in register description

**5.2.3.5 TDS\_MISO - Critical fault reply frame**

MISO SPI critical fault reply frame  
 Critical fault frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	19	17	16
Don't care									1	0	Don't care				

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't care (cont'd)								1V5	2V5	BG	CLK_TOO_SLOW	CLK_TOO_FAST	DIG_CLK_TOO_SLOW	DIG_CLK_TOO_FAST	WD_REF_CLK

Field	Bits	Description
Don't care	31:24	-
Reply Mode	23:22	Indicates type of reply frame: 00 <sub>B</sub> : 16 bit Reply Frame 01 <sub>B</sub> : 22 bit Reply Frame 10 <sub>B</sub> : Critical Fault Frame
Don't care	21:8	-
1V5	7	0 <sub>B</sub> : 1V5 supply not ok 1 <sub>B</sub> : 1V5 supply ok
2V5	6	0 <sub>B</sub> : 2V5 supply not ok 1 <sub>B</sub> : 2V5 supply ok
BG	5	0 <sub>B</sub> : ADC Bandgap not ok 1 <sub>B</sub> : ADC Bandgap ok
CLK_TOO_SLOW	4	0 <sub>B</sub> : No clock fault detected 1 <sub>B</sub> : Clock is too slow for IC operation
CLK_TOO_FAST	3	0 <sub>B</sub> : No clock fault detected 1 <sub>B</sub> : Clock is too fast for IC operation
DIG_CLK_TOO_SLOW	2	0 <sub>B</sub> : No clock fault detected 1 <sub>B</sub> : Digital Clock is too slow <i>Note: clock watchdog must be enabled.</i>
DIG_CLK_TOO_FAST	1	0 <sub>B</sub> : No clock fault detected 1 <sub>B</sub> : Digital Clock is too fast <i>Note: clock watchdog must be enabled.</i>
WD_REF_CLK	0	0 <sub>B</sub> : Clock watchdog reference clock is ok 1 <sub>B</sub> : Clock watchdog reference clock is missing

## 5.3 Register description

### 5.3.1 Overview of Register Types

Bit type short name	Bit type description	Note
r	Bits are readable (read)	bitfields "RES" do not care
rh	Bits are readable (read) and modifiable by the IC (hardware)	bitfields "RES" do not care
rw	Bits are read- and writeable (read-write)	bitfields "RES" do not care, write "0"
rwh	Bits are read- and writeable (read-write) and modifiable by the IC (hardware)	bitfields "RES" do not care, write "0"

## 5.3.2 Central registers

### 5.3.2.1 Register overview - centralRegs (ascending offset address)

**Table 19** Register overview - centralRegs (ascending offset address)

Short name	Long name	Offset address	Page number
CH_CTRL	Channel Control Register	0000 <sub>H</sub>	55
GLOBAL_CONFIG	Global Configuration Register	0002 <sub>H</sub>	55
GLOBAL_DIAG0	Global Diagnosis Register 0	0003 <sub>H</sub>	56
GLOBAL_DIAG1	Global Diagnosis Register 1	0004 <sub>H</sub>	57
GLOBAL_DIAG2	Global Diagnosis Register 2	0005 <sub>H</sub>	58
VBAT_TH	VBAT Threshold Register	0006 <sub>H</sub>	59
FB_FRZ	Feedback Freeze Register	0007 <sub>H</sub>	59
FB_UPD	Feedback Update Register	0008 <sub>H</sub>	60
WD_RELOAD	SPI Watchdog Register	0009 <sub>H</sub>	61
DIAG_ERR_CHGR0	Diagnosis Error Register 0	000A <sub>H</sub>	61
DIAG_ERR_CHGR1	Diagnosis Error Register 1	000B <sub>H</sub>	62
DIAG_WARN_CHGR0	Diagnosis Warning Register 0	0010 <sub>H</sub>	63
DIAG_WARN_CHGR1	Diagnosis Warning Register 1	0011 <sub>H</sub>	64
FAULT_MASK0	Fault Mask Register 0	0016 <sub>H</sub>	66
FAULT_MASK1	Fault Mask Register 1	0017 <sub>H</sub>	66
FAULT_MASK2	Fault Mask Register 2	0018 <sub>H</sub>	67
CLK_DIV	Clock Control Register	0019 <sub>H</sub>	68
SFF_BIST	BIST Register	003F <sub>H</sub>	68
ICVID	Version Register	0200 <sub>H</sub>	69
PIN_STAT	Pin Status Register	0201 <sub>H</sub>	70
FB_STAT	Feedback Status Register	0202 <sub>H</sub>	70
FB_VOLTAGE1	Feedback Voltage Register 1	0203 <sub>H</sub>	72
FB_VOLTAGE2	Feedback Voltage Register 2	0204 <sub>H</sub>	73

### 5.3.2.2 Register address space - centralRegs

**Table 20** Registers address space - centralRegs

Module	Base address	End address	Note
apb	00000000 <sub>H</sub>	0000FFFE <sub>H</sub>	

**Serial peripheral interface (SPI)**

**5.3.2.3 Channel Control Register**

The channel enable bits EN\_CHx can only be set in Mission mode. The parallel mode configuration bits CH\_PAR\_x can only be set in Config mode.

**CH\_CTRL** Offset address: 0000<sub>H</sub>  
 Channel Control Register value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>OP_M ODE</b>	<b>CH_ PAR_ 1_2</b>	<b>CH_ PAR_ 0_3</b>	<b>Res</b>									<b>EN_C H3</b>	<b>EN_C H2</b>	<b>EN_C H1</b>	<b>EN_C H0</b>
undef	undef	undef	r									undef	undef	undef	undef

Field	Bits	Type	Description
EN_CH0	0	undef	<b>Enable Channel 0</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
EN_CH1	1	undef	<b>Enable Channel 1</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
EN_CH2	2	undef	<b>Enable Channel 2</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
EN_CH3	3	undef	<b>Enable Channel 3</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH_PAR_0_3	13	undef	<b>Parallel Operation Channel 0/3</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH_PAR_1_2	14	undef	<b>Parallel Operation Channel 1/2</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
OP_MODE	15	undef	<b>Chip Operation Mode</b> 0 <sub>B</sub> Config Mode 1 <sub>B</sub> Mission Mode

**5.3.2.4 Global Configuration Register**

Global Configuration Register: write access only possible in Config Mode

**GLOBAL\_CONFIG** Offset address: 0002<sub>H</sub>  
 Global Configuration Register value: 4005<sub>H</sub>

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	VIO_SEL	UV_OV_SWAP	OT_TEST	Res						V1V5_OV_TEST	V1V5_UV_TEST	Res	CRC_EN	SPI_WD_EN	CLK_WD_EN
r	undef	undef	undef	r						undef	undef	r	undef	undef	undef

Field	Bits	Type	Description
CLK_WD_EN	0	undef	<b>Clock Watchdog</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
SPI_WD_EN	1	undef	<b>SPI Watchdog</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CRC_EN	2	undef	<b>SPI CRC Check</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
V1V5_UV_TEST	4	undef	<b>Test Internal Supply Undervoltage Detection</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
V1V5_OV_TEST	5	undef	<b>Test Internal Supply Overvoltage Detection</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
OT_TEST	12	undef	<b>Test Overtemperature Detection</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
UV_OV_SWAP	13	undef	<b>Test Undervoltage/Overvoltage Detection</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
VIO_SEL	14	undef	<b>VIO voltage selection</b> 0 <sub>B</sub> 3.3 V 1 <sub>B</sub> 5.0 V

**5.3.2.5 Global Diagnosis Register 0**

Global Diagnosis Register 0

**GLOBAL\_DIAGO** Offset address: 0003<sub>H</sub>  
 Global Diagnosis Register 0 value: 0600<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	SPI_WD_ERR	Res			POR_EVENT	RES_EVENT	COT_WARN	COTERR	CLK_NOK	VDD_OV	VDD_UV	VIO_OV	VIO_UV	VBAT_OV	VBAT_UV
r	undef	r			undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef



**Serial peripheral interface (SPI)**

Field	Bits	Type	Description
VBAT_UV	0	undef	<b>VBAT Undervoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VBAT_OV	1	undef	<b>VBAT Overvoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VIO_UV	2	undef	<b>VIO Undervoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VIO_OV	3	undef	<b>VIO Overvoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VDD_UV	4	undef	<b>VDD Undervoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VDD_OV	5	undef	<b>VDD Overvoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
CLK_NOK	6	undef	<b>Clock Fault Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
COTERR	7	undef	<b>Central Overtemperature Error</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
COTWARN	8	undef	<b>Central Overtemperature Warning</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
RES_EVENT	9	undef	<b>Reset occurred due to RESN-pin low</b> 0 <sub>B</sub> No Event Occurred 1 <sub>B</sub> Event Occurred
POR_EVENT	10	undef	<b>Event Occurred</b> 0 <sub>B</sub> No Event Occurred 1 <sub>B</sub> A Power On Reset Event occurred since previous read out
SPI_WD_ERR	14	undef	<b>SPI Watchdog Fault Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected

**5.3.2.6 Global Diagnosis Register 1**

Global Diagnosis Register 1

**GLOBAL\_DIAG1**

Offset address:

0004<sub>H</sub>

**Serial peripheral interface (SPI)**

Global Diagnosis Register 1

value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>HVAD C_ER R</b>	<b>Res</b>								<b>VPRE _OV</b>	<b>REF_ OV</b>	<b>REF_ UV</b>	<b>VDD 2V5_ OV</b>	<b>VDD 2V5_ UV</b>	<b>VR_I REF_ OV</b>	<b>VR_I REF_ UV</b>
undef	r								undef	undef	undef	undef	undef	undef	undef

Field	Bits	Type	Description
VR_IREF_UV	0	undef	<b>Internal Bias Current too Low Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VR_IREF_OV	1	undef	<b>Internal Bias Current too High Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VDD2V5_UV	2	undef	<b>Internal 2V5 Supply Undervoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VDD2V5_OV	3	undef	<b>Internal 2V5 Supply Overvoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
REF_UV	4	undef	<b>Internal Reference Undervoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
REF_OV	5	undef	<b>Internal Reference Overvoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
VPRE_OV	6	undef	<b>Internal Pre-Regulator Overvoltage Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
HVADC_ERR	15	undef	<b>Internal Monitoring ADC Error Detection</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected

**5.3.2.7 Global Diagnosis Register 2**

Global Diagnosis Register 2

**GLOBAL\_DIAG2**

Offset address: 0005<sub>H</sub>

Global Diagnosis Register 2

value: 0000<sub>H</sub>

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>											<b>OTP_VIRG_IN</b>	<b>OTP_ECC_ERR</b>	<b>Res</b>	<b>REG_ECC_ERR</b>	<b>Res</b>
r											undef	undef	r	undef	r

Field	Bits	Type	Description
REG_ECC_ERR	1	undef	<b>Register ECC Error</b> 0 <sub>B</sub> No Error 1 <sub>B</sub> Multi Bit Flip Detected
OTP_ECC_ERR	3	undef	<b>OTP ECC Error</b> 0 <sub>B</sub> No Error 1 <sub>B</sub> None Repairable Multi Bit Flip Detected
OTP_VIRGIN	4	undef	<b>OTP Memory Configured Complete</b> 0 <sub>B</sub> OTP completely configured 1 <sub>B</sub> Virgin OTP Address Detected

### 5.3.2.8 VBAT Threshold Register

VBAT Over and Under Voltage Threshold Register

**VBAT\_TH**

VBAT Threshold Register

Offset address: 0006<sub>H</sub>

value: FF19<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>VBAT_OV_TH</b>								<b>VBAT_UV_TH</b>							
undef								undef							

Field	Bits	Type	Description
VBAT_UV_TH	7:0	undef	<b>VBAT Undervoltage Threshold</b> $V_{BAT\_UV} = <VBAT\_UV\_TH> * 0.16208 \text{ V}$
VBAT_OV_TH	15:8	undef	<b>VBAT Overvoltage Threshold</b> $V_{BAT\_OV} = <VBAT\_OV\_TH> * 0.16208 \text{ V}$

### 5.3.2.9 Feedback Freeze Register

Feedback Freeze Register

Feedback Values are provided in the registers FB\_DC, FB\_VBAT, FB\_I\_AVG

**FB\_FRZ**

Feedback Freeze Register

Offset address: 0007<sub>H</sub>

value: 0000<sub>H</sub>

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>												<b>FR_C H3</b>	<b>FR_C H2</b>	<b>FR_C H1</b>	<b>FR_C H0</b>
r												rw	rw	rw	rw

Field	Bits	Type	Description
FR_CH0	0	rw	<b>Freeze of CH0 Feedback Values</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
FR_CH1	1	rw	<b>Freeze of CH1 Feedback Values</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
FR_CH2	2	rw	<b>Freeze of CH2 Feedback Values</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
FR_CH3	3	rw	<b>Freeze of CH3 Feedback Values</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

**5.3.2.10 Feedback Update Register**

Feedback Update Register

Feedback Values are provided in the registers FB\_DC, FB\_VBAT, FB\_I\_AVG

**FB\_UPD** Offset address: 0008<sub>H</sub>  
 Feedback Update Register value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>												<b>UD_ CH3</b>	<b>UD_ CH2</b>	<b>UD_ CH1</b>	<b>UD_ CH0</b>
r												undef	undef	undef	undef

Field	Bits	Type	Description
UD_CH0	0	undef	<b>Indication of CH0 Feedback Values Update</b> 0 <sub>B</sub> No new Feedback Values available 1 <sub>B</sub> New Feedback Values available
UD_CH1	1	undef	<b>Indication of CH1 Feedback Values Update</b> 0 <sub>B</sub> No new Feedback Values available 1 <sub>B</sub> New Feedback Values available
UD_CH2	2	undef	<b>Indication of CH2 Feedback Values Update</b> 0 <sub>B</sub> No new Feedback Values available 1 <sub>B</sub> New Feedback Values available

**(table continues...)**

**Serial peripheral interface (SPI)**

(continued)

Field	Bits	Type	Description
UD_CH3	3	undef	<b>Indication of CH3 Feedback Values Update</b> 0 <sub>B</sub> No new Feedback Values available 1 <sub>B</sub> New Feedback Values available

**5.3.2.11 SPI Watchdog Register**

SPI Watchdog Counter Reload Register

**WD\_RELOAD** Offset address: 0009<sub>H</sub>  
 SPI Watchdog Register value: 0001<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>						<b>WD_TIME</b>									
r						undef									

Field	Bits	Type	Description
WD_TIME	10:0	undef	<b>Reload value of SPI watchdog timeout t<sub>SPI_WD</sub></b> $\langle \text{WD\_TIME} \rangle = \text{rounddown}(t_{\text{SPI\_WD}} * f_{\text{SYS}} / 2^{14})$

**5.3.2.12 Diagnosis Error Register 0**

Diagnosis Error Register Channel Group 0

**DIAG\_ERR\_CHGR0** Offset address: 000A<sub>H</sub>  
 Diagnosis Error Register 0 value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>			<b>OTE1</b>	<b>SG1</b>	<b>OC1</b>	<b>OL1</b>	<b>OLSG1</b>	<b>Res</b>			<b>OTE0</b>	<b>SG0</b>	<b>OC0</b>	<b>OL0</b>	<b>OLSG0</b>
r			undef	undef	undef	undef	undef	r			undef	undef	undef	undef	undef

Field	Bits	Type	Description
OLSG0	0	undef	<b>Open Load or Short to Ground Detection CH0</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OL0	1	undef	<b>Open Load Detection CH0</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OC0	2	undef	<b>Overcurrent Detection CH0</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected

(table continues...)

**Serial peripheral interface (SPI)**

(continued)

Field	Bits	Type	Description
SG0	3	undef	<b>Short to Ground Detection CH0</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OTE0	4	undef	<b>Overtemperature Error Detection CH0</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OLSG1	8	undef	<b>Open Load or Short to Ground Detection CH1</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OL1	9	undef	<b>Open Load Detection CH1</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OC1	10	undef	<b>Overcurrent Detection CH1</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
SG1	11	undef	<b>Short to Ground Detection CH1</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OTE1	12	undef	<b>Overtemperature Error Detection CH1</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected

**5.3.2.13 Diagnosis Error Register 1**

Diagnosis Error Register Channel Group 1

**DIAG\_ERR\_CHGR1**

Offset address: 000B<sub>H</sub>

Diagnosis Error Register 1

value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>		<b>OTE3</b>	<b>SG3</b>	<b>OC3</b>	<b>OL3</b>	<b>OLSG3</b>		<b>Res</b>		<b>OTE2</b>	<b>SG2</b>	<b>OC2</b>	<b>OL2</b>	<b>OLSG2</b>	
r		undef	undef	undef	undef	undef		r		undef	undef	undef	undef	undef	

Field	Bits	Type	Description
OLSG2	0	undef	<b>Open Load or Short to Ground Detection CH2</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OL2	1	undef	<b>Open Load Detection CH2</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected

(table continues...)

**Serial peripheral interface (SPI)**

(continued)

Field	Bits	Type	Description
OC2	2	undef	<b>Overcurrent Detection CH2</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
SG2	3	undef	<b>Short to Ground Detection CH2</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OTE2	4	undef	<b>Overtemperature Error Detection CH2</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OLSG3	8	undef	<b>Open Load or Short to Ground Detection CH3</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OL3	9	undef	<b>Open Load Detection CH3</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OC3	10	undef	<b>Overcurrent Detection CH3</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
SG3	11	undef	<b>Short to Ground Detection CH3</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected
OTE3	12	undef	<b>Overtemperature Error Detection CH3</b> 0 <sub>B</sub> No Fault Detected 1 <sub>B</sub> Fault Detected

### 5.3.2.14 Diagnosis Warning Register 0

Diagnosis Warning Register Channel Group 0

**DIAG\_WARN\_CHGR0**

Offset address: 0010<sub>H</sub>

Diagnosis Warning Register 0

value: 1010<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		OLS G_W ARN 1_CH K_N OK	OLS G_W ARN 1	OTW 1	I_RE G_W ARN 1	PWM _REG _WA RN1	Res				OLS G_W ARN 0_CH K_N OK	OLS G_W ARN 0	OTW 0	I_RE G_W ARN 0	PWM _REG _WA RNO
r		undef	undef	undef	undef	undef	r				undef	undef	undef	undef	undef

**Serial peripheral interface (SPI)**

Field	Bits	Type	Description
PWM_REG_WARN0	0	undef	<b>ICC PWM Regulation Warning Detection CH0</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
I_REG_WARN0	1	undef	<b>ICC Current Regulation Warning CH0</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OTW0	2	undef	<b>Overtemperature Warning Detection CH0</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN0	3	undef	<b>Open Load or Short to Ground Warning Detection CH0</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN0_CHK_NOK	4	undef	<b>Open Load or Short to Ground Warning Detection performed CH0</b> 0 <sub>B</sub> OLSG Warning Detection performed 1 <sub>B</sub> OLSG Warning Detection not possible
PWM_REG_WARN1	8	undef	<b>ICC PWM Regulation Warning Detection CH1</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
I_REG_WARN1	9	undef	<b>ICC Current Regulation Warning CH1</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OTW1	10	undef	<b>Overtemperature Warning Detection CH1</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN1	11	undef	<b>Open Load or Short to Ground Warning Detection CH1</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN1_CHK_NOK	12	undef	<b>Open Load or Short to Ground Warning Detection performed CH1</b> 0 <sub>B</sub> OLSG Warning Detection performed 1 <sub>B</sub> OLSG Warning Detection not possible

**5.3.2.15 Diagnosis Warning Register 1**

Diagnosis Warning Register Channel Group 1

**DIAG\_WARN\_CHGR1**

Diagnosis Warning Register 1

Offset address: 0011<sub>H</sub>

value: 1010<sub>H</sub>



# TLE92464EDHP

## High accuracy four channel low-side solenoid driver IC



### Serial peripheral interface (SPI)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		OLS G_W ARN 3_CH K_N OK	OLS G_W ARN 3	OTW 3	I_RE G_W ARN 3	PWM _REG _WA RN3	Res		OLS G_W ARN 2_CH K_N OK	OLS G_W ARN 2	OTW 2	I_RE G_W ARN 2	PWM _REG _WA RN2		
r		undef	undef	undef	undef	undef	r		undef	undef	undef	undef	undef		

Field	Bits	Type	Description
PWM_REG_WARN2	0	undef	<b>ICC PWM Regulation Warning Detection CH2</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
I_REG_WARN2	1	undef	<b>ICC Current Regulation Warning CH2</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OTW2	2	undef	<b>Overtemperature Warning Detection CH2</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN2	3	undef	<b>Open Load or Short to Ground Warning Detection CH2</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN2_CHK_NOK	4	undef	<b>Open Load or Short to Ground Warning Detection performed CH2</b> 0 <sub>B</sub> OLSG Warning Detection performed 1 <sub>B</sub> Warning Detected
PWM_REG_WARN3	8	undef	<b>ICC PWM Regulation Warning Detection CH3</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
I_REG_WARN3	9	undef	<b>ICC Current Regulation Warning CH3</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OTW3	10	undef	<b>Overtemperature Warning Detection CH3</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN3	11	undef	<b>Open Load or Short to Ground Warning Detection CH3</b> 0 <sub>B</sub> No Warning Detected 1 <sub>B</sub> Warning Detected
OLSG_WARN3_CHK_NOK	12	undef	<b>Open Load or Short to Ground Warning Detection performed CH3</b> 0 <sub>B</sub> OLSG Warning Detection performed 1 <sub>B</sub> OLSG Warning Detection not possible

**Serial peripheral interface (SPI)**

**5.3.2.16 Fault Mask Register 0**

FAULTN-pin Mask 0 Register

**FAULT\_MASK0** Offset address: 0016<sub>H</sub>  
 Fault Mask Register 0 value: C00F<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SUP_NOK_EXT_MASK</b>	<b>SUP_NO_K_IN_T_MASK</b>	<b>EN_PIN_MASK</b>	<b>Res</b>									<b>CH3_ERR_MASK</b>	<b>CH2_ERR_MASK</b>	<b>CH1_ERR_MASK</b>	<b>CH0_ERR_MASK</b>
rw	rw	rw	r									rw	rw	rw	rw

Field	Bits	Type	Description
CH0_ERR_MASK	0	rw	<b>OC0, SG0, OL0, OTE0, OLSG0 FAULTN-pin Indication</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH1_ERR_MASK	1	rw	<b>OC1, SG1, OL1, OTE1, OLSG1 FAULTN-pin Indication</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH2_ERR_MASK	2	rw	<b>OC2, SG2, OL2, OTE2, OLSG2 FAULTN-pin Indication</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH3_ERR_MASK	3	rw	<b>OC3, SG3, OL3, OTE3, OLSG3 FAULTN-pin Indication</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
EN_PIN_MASK	13	rw	<b>EN-pin Status at FAULTN-pin Indication</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
SUP_NOK_INT_MASK	14	rw	<b>Internal Supply UV/OV at FAULTN-pin Indication (SUP_NOK_INT)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
SUP_NOK_EXT_MASK	15	rw	<b>External Supply UV/OV at FAULTN-pin Indication (SUP_NOK_EXT)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

**5.3.2.17 Fault Mask Register 1**

FAULTN-pin Mask 1 Register

**FAULT\_MASK1** Offset address: 0017<sub>H</sub>  
 Fault Mask Register 1 value: 700F<sub>H</sub>

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>	<b>CLK_LOW_MASK</b>	<b>COTERR_MASK</b>	<b>COTWARN_MASK</b>	<b>Res</b>								<b>CH3_WARN_MASK</b>	<b>CH2_WARN_MASK</b>	<b>CH1_WARN_MASK</b>	<b>CH0_WARN_MASK</b>
r	rw	rw	rw	r								rw	rw	rw	rw

Field	Bits	Type	Description
CH0_WARN_MASK	0	rw	<b>CH0 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH1_WARN_MASK	1	rw	<b>CH1 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH2_WARN_MASK	2	rw	<b>CH2 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CH3_WARN_MASK	3	rw	<b>CH3 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
COTWARN_MASK	12	rw	<b>Central Overtemperature Warning at FAULTN-pin Indication (COTWRN)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
COTERR_MASK	13	rw	<b>Central Overtemperature Error at FAULTN-pin Indication (COTERR)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
CLK_LOW_MASK	14	rw	<b>Clock too Slow at FAULTN-pin Indication (DIG_CLK_TOO_SLOW, CLK_TOO_SLOW)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

**5.3.2.18 Fault Mask Register 2**

FAULTN-pin Mask 2 Register

**FAULT\_MASK2**

Fault Mask Register 2

Offset address: 0018<sub>H</sub>

value: C000<sub>H</sub>

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SPI_WD_MASK</b>	<b>DATA_ERR_MASK</b>	<b>Res</b>													
rw	rw	r													

Field	Bits	Type	Description
DATA_ERR_MASK	14	rw	<b>Data Error at FAULTN-pin Indication (DATA_ERR)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
SPI_WD_MASK	15	rw	<b>SPI Watchdog Fault at FAULTN-pin Indication (SPI_WD_ERR)</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

**5.3.2.19 Clock Control Register**

Clock Control Register: write access only possible in Config Mode

**CLK\_DIV** Offset address: 0019<sub>H</sub>  
 Clock Control Register value: 0438<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>EXT_CLK</b>	<b>PLL_REFDIV</b>					<b>PLL_FBDIV</b>									
undef	undef					undef									

Field	Bits	Type	Description
PLL_FBDIV	8:0	undef	<b>PLL feedback divider</b> $\langle \text{PLL\_FBDIV} \rangle = 56 \text{ MHz} * \langle \text{PLL\_REFDIV} \rangle / f_{\text{CLK}}$
PLL_REFDIV	14:9	undef	<b>PLL reference divider</b> $\langle \text{PLL\_REFDIV} \rangle = \text{round}(f_{\text{CLK}} / 1 \text{ MHz})$
EXT_CLK	15	undef	<b>Clock Source Selection</b> 0 <sub>B</sub> Internal Clock 1 <sub>B</sub> External clock (CLK-pin)

**5.3.2.20 BIST Register**

Built In Self Test (BIST) register: write access only possible in Config Mode

**SFF\_BIST** Offset address: 003F<sub>H</sub>  
 BIST Register value: 0000<sub>H</sub>

**Serial peripheral interface (SPI)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>Res</b>											<b>SMU _SLF _TST _CER _R</b>	<b>SMU _SLF _TST _UE _RR</b>	<b>SMU _SLF _TST _FAI _L</b>	<b>SMU _SLF _TST _DO _NE</b>	<b>SMU _SLF _TST _EN</b>	
											r	undef	undef	undef	undef	undef

Field	Bits	Type	Description
SMU_SLF_TST_EN	0	undef	<b>BIST Enable</b> 0 <sub>B</sub> BIST not triggered 1 <sub>B</sub> BIST triggered
SMU_SLF_TST_DONE	1	undef	<b>BIST Done</b> 0 <sub>B</sub> BIST not done 1 <sub>B</sub> BIST done
SMU_SLF_TST_FAIL	2	undef	<b>BIST Sequence</b> 0 <sub>B</sub> Passed 1 <sub>B</sub> Failed
SMU_SLF_TST_UERR	3	undef	<b>BIST Uncorrectable Errors</b> 0 <sub>B</sub> Not Tested 1 <sub>B</sub> Tested
SMU_SLF_TST_CERR	4	undef	<b>BIST Correctable Errors</b> 0 <sub>B</sub> Not Tested 1 <sub>B</sub> Tested

**5.3.2.21 Version Register**

IC version and ID

**ICVID** Offset address: 0200<sub>H</sub>  
 Version Register value: C1XX<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>MANUFACTURER</b>								<b>VERSION</b>							
undef								undef							

Field	Bits	Type	Description
VERSION	7:0	undef	<b>Chip Version</b> FC <sub>H</sub> B11 Design Step FD <sub>H</sub> B12 Design Step FE <sub>H</sub> B13 Design Step FF <sub>H</sub> B15 Design Step
MANUFACTURER	15:8	undef	<b>Manufacturer ID</b>

**Serial peripheral interface (SPI)**

**5.3.2.22 Pin Status Register**

Pin Status Feedback Register

**PIN\_STAT** Offset address: 0201<sub>H</sub>  
 Pin Status Register value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>									<b>FAUL TN_F B</b>	<b>FAUL TN</b>	<b>EN</b>	<b>DRV3</b>	<b>DRV2</b>	<b>DRV1</b>	<b>DRV0</b>
									undef	undef	undef	undef	undef	undef	undef

Field	Bits	Type	Description
DRV0	0	undef	<b>Logic Level of DRV0-pin</b> 0 <sub>B</sub> Low 1 <sub>B</sub> High
DRV1	1	undef	<b>Logic Level of DRV1-pin</b> 0 <sub>B</sub> Low 1 <sub>B</sub> High
DRV2	2	undef	<b>Logic Level of DRV2-pin</b> 0 <sub>B</sub> Low 1 <sub>B</sub> High
DRV3	3	undef	<b>Logic Level of DRV3-pin</b> 0 <sub>B</sub> Low 1 <sub>B</sub> High
EN	4	undef	<b>Logic Level of EN-pin</b> 0 <sub>B</sub> Low 1 <sub>B</sub> High
FAULTN	5	undef	<b>Internal Status of FAULTN-pin according to Fault Mask Configuration</b> 0 <sub>B</sub> Fault detected 1 <sub>B</sub> No Fault detected
FAULTN_FB	6	undef	<b>Logic Level of FAULTN-pin</b> 0 <sub>B</sub> Low 1 <sub>B</sub> High

**5.3.2.23 Feedback Status Register**

General status register

**FB\_STAT** Offset address: 0202<sub>H</sub>  
 Feedback Status Register Reset values see: [Table 21](#)

**Serial peripheral interface (SPI)**

															21	20	19	18	17	16		
															INIT_DON E	SPI_WD_ ERR	Res					
															undef	undef	r					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
ERR_ CHGR 1	ERR_ CHG R0	SUP_ NO_ K_IN T	SUP_ NO_ K_EX T	DATA_ _err	POR_ _eve nt	RES_ _even t	COT WAR N	COTE RR	CLK_ NOK	Res	OLS G_W ARN_ _CH K_N OK_ CHG R1	OLS G_W ARN_ _CH K_N OK_ CHG R0	Res	DIAG_ _WA RN_ CHG R1	DIAG_ _WA RN_ CHG R0							
undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	r	undef	undef	r	undef	undef							

Field	Bits	Type	Description
DIAG_WARN_C HGR0	0	undef	<b>Current status of DIAG_WARN_CHGR0 register (excluding &lt;OLSG_WARNx_CHK_NOK&gt;)</b> 0 <sub>B</sub> No Warning detected 1 <sub>B</sub> Warning detected
DIAG_WARN_C HGR1	1	undef	<b>Current status of DIAG_WARN_CHGR1 register (excluding &lt;OLSG_WARNx_CHK_NOK&gt;)</b> 0 <sub>B</sub> No Warning detected 1 <sub>B</sub> Warning detected
OLSG_WARN_ CHK_NOK_CH GR0	3	undef	<b>Current status of &lt;OLSG_WARNx_CHK_NOK&gt; bit in the DIAG_WARN_CHGR0 register</b> 0 <sub>B</sub> No Warning detected 1 <sub>B</sub> Warning detected
OLSG_WARN_ CHK_NOK_CH GR1	4	undef	<b>Current status of &lt;OLSG_WARNx_CHK_NOK&gt; bit in the DIAG_WARN_CHGR1 register</b> 0 <sub>B</sub> No Warning detected 1 <sub>B</sub> Warning detected
CLK_NOK	6	undef	<b>Current status of CLK_NOK in GLOBAL_DIAG0 register</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
COTERR	7	undef	<b>Current status of COTERR in GLOBAL_DIAG0 register</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
COTWARN	8	undef	<b>Current status of COTWARN in GLOBAL_DIAG0 register</b> 0 <sub>B</sub> No Warning detected 1 <sub>B</sub> Warning detected
RES_event	9	undef	<b>Current status of RES_event in GLOBAL_DIAG0 register</b> 0 <sub>B</sub> No Reset Event 1 <sub>B</sub> Reset occurred

(table continues...)

**Serial peripheral interface (SPI)**

(continued)

Field	Bits	Type	Description
POR_event	10	undef	<b>Current status of POR_event in GLOBAL DIAG0 register</b> 0 <sub>B</sub> No power on Reset 1 <sub>B</sub> Power on Reset occurred
DATA_err	11	undef	<b>Current status of &lt;OTP_ECC_ERR&gt;, &lt;OTP_VIRGIN&gt;, &lt;HV_ADC_ERR&gt;</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
SUP_NOK_EXT	12	undef	<b>Current status of &lt;VIO_UV/OV&gt;, &lt;VDD_UV/OV&gt;, &lt;VBAT_UV/OV&gt;</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
SUP_NOK_INT	13	undef	<b>Current status of &lt;VDD2V5_UV/OV&gt;, &lt;REF_UV/OV&gt;, &lt;VR_IREF_UV/OV&gt;, &lt;VPRE_OV&gt;</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
ERR_CHGR0	14	undef	<b>Current status of DIAG_ERR_CHGR1 register</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
ERR_CHGR1	15	undef	<b>Current status of DIAG_ERR_CHGR2 register</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
SPI_WD_ERR	20	undef	<b>Current status of &lt;SPI_WD_ERR&gt;</b> 0 <sub>B</sub> No Fault detected 1 <sub>B</sub> Fault detected
INIT_DONE	21	undef	<b>Chip Initialization</b> 0 <sub>B</sub> Not Done 1 <sub>B</sub> Done

**Table 21** Reset values of **FB\_STAT**

Reset type	Reset value	Note
	10 0000 0000 0110 0001 1000 <sub>B</sub>	

**5.3.2.24 Feedback Voltage Register 1**

Supply Voltage Feedback Register 1

**FB\_VOLTAGE1**

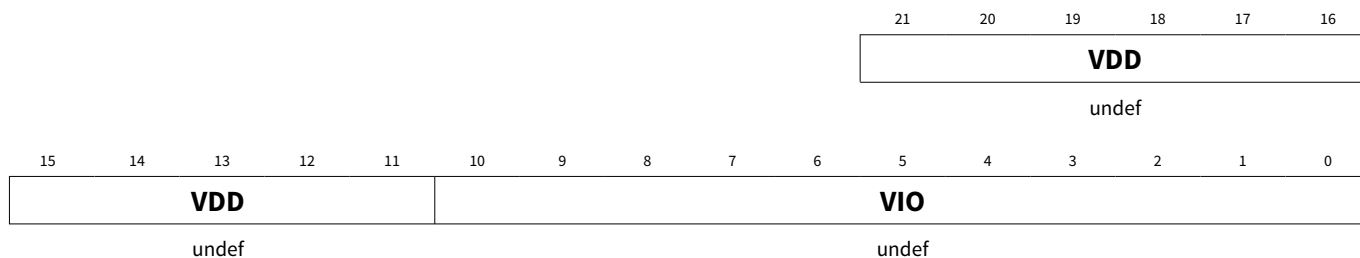
Feedback Voltage Register 1

Offset address: 0203<sub>H</sub>

value: XX XXXX<sub>H</sub>



**Serial peripheral interface (SPI)**



Field	Bits	Type	Description
VIO	10:0	undef	<b>VIO Voltage</b> $V_{IO} = 0.0034534 \text{ V} * \langle \text{VIO} \rangle$
VDD	21:11	undef	<b>VDD Voltage</b> $V_{DD} = 0.0034534 \text{ V} * \langle \text{VDD} \rangle$

**5.3.2.25 Feedback Voltage Register 2**

Supply Voltage Feedback Register 2

**FB\_VOLTAGE2**

Feedback Voltage Register 2

Offset address: 0204<sub>H</sub>  
 value: XX XXXX<sub>H</sub>



Field	Bits	Type	Description
TEMP_VALUE	10:0	undef	<b>Temperature Feedback</b> $T_{FB} = (\langle \text{TEMP\_VALUE} \rangle * 0.000593 - 0.819) / (-0.0016) \text{ [Celsius]}$
VBAT	21:11	undef	<b>VBAT Voltage</b> $V_{BAT} = 41.47 \text{ V} * \langle \text{VBAT} \rangle / (2^{11} - 1)$

### 5.3.3 Channel registers

#### 5.3.3.1 Register Overview - channelRegs (ascending Offset Address)

**Table 22 Register Overview - channelRegs (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
SETPOINT	Setpoint Register	0000 <sub>H</sub>	<a href="#">75</a>
CTRL	Control Register	0001 <sub>H</sub>	<a href="#">76</a>
PERIOD	ICC PWM Frequency Controller Register	0002 <sub>H</sub>	<a href="#">77</a>
INTEGRATOR_LIMIT	ICC Integrator Limitation Register	0003 <sub>H</sub>	<a href="#">78</a>
DITHER_CLK_DIV	Dither Clock Register	0004 <sub>H</sub>	<a href="#">79</a>
DITHER_STEP	Dither Step Register	0005 <sub>H</sub>	<a href="#">80</a>
DITHER_CTRL	Dither Control Register	0006 <sub>H</sub>	<a href="#">81</a>
CH_CONFIG	Channel Configuration Register	0007 <sub>H</sub>	<a href="#">82</a>
MODE	Channel Mode Register	000C <sub>H</sub>	<a href="#">84</a>
TON	On-Time Register	000D <sub>H</sub>	<a href="#">85</a>
CTRL_INT_THRESH	ICC Integrator Threshold Control Register	000E <sub>H</sub>	<a href="#">86</a>
FB_DC	Feedback Duty Cycle Register	0200 <sub>H</sub>	<a href="#">87</a>
FB_VBAT	Feedback Average VBAT	0201 <sub>H</sub>	<a href="#">88</a>
FB_I_AVG	Feedback Average Current	0202 <sub>H</sub>	<a href="#">89</a>
FB_IMIN_IMAX	Feedback Min/Max Current	0203 <sub>H</sub>	<a href="#">90</a>
FB_I_AVG_s16	Feedback signed Current	0204 <sub>H</sub>	<a href="#">91</a>
FB_INT_THRESH	Feedback ICC Integrator Threshold	0205 <sub>H</sub>	<a href="#">92</a>
FB_PERIOD_MIN_MAX	Feedback Min/Max PWM Period	0206 <sub>H</sub>	<a href="#">93</a>

#### 5.3.3.2 Register Address Space - channelRegs

**Table 23 Registers Address Space - channelRegs**

Module	Base Address	End Address	Note
CH0	00000040 <sub>H</sub>	0001003E <sub>H</sub>	
CH1	00000050 <sub>H</sub>	0001004E <sub>H</sub>	
CH2	00000060 <sub>H</sub>	0001005E <sub>H</sub>	
CH3	00000070 <sub>H</sub>	0001006E <sub>H</sub>	

### 5.3.3.3 Setpoint Register

Current Setpoint Register

**SETPOINT** Offset address: 0000<sub>H</sub>  
 Setpoint Register Value 0000<sub>H</sub>



Field	Bits	Type	Description
TARGET	14:0	rwh	<b>Current Setpoint Target</b> $I_{set} = 2A * <TARGET> / ( 2^{15} - 1)$ $I_{set,par} = 4A * <TARGET> / ( 2^{15} - 1)$ NOTE: Values higher than 0x6000 are saturated
AUTO_LIMIT_DIS	15	rwh	<b>Autolimit Feature</b> 0 <sub>B</sub> Enabled 1 <sub>B</sub> Disabled

### 5.3.3.4 Control Register

Channel Control Register

**CTRL** Offset address: 0001<sub>H</sub>  
 Control Register Value 4600<sub>H</sub>

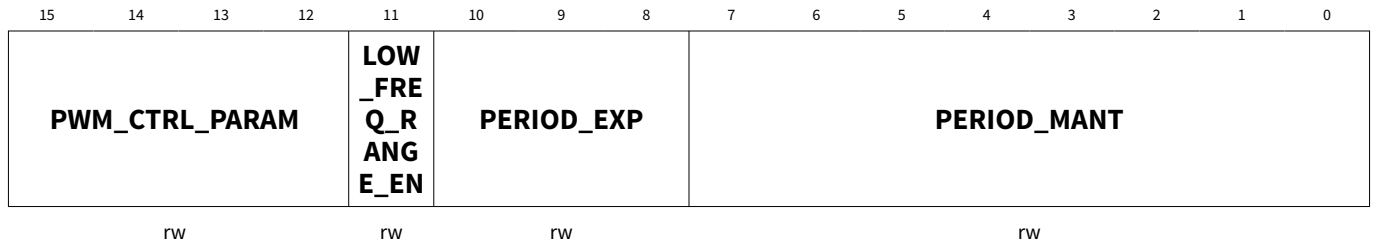
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>	<b>OLSG_WARN_EN</b>		<b>OLSG_WARN_WINDOW</b>					<b>PWM_PERIOD_CALC_MODE</b>	<b>MIN_INT_THRESH</b>							
r	rw		rw					rw	rw							

Field	Bits	Type	Description
MIN_INT_THRESH	7:0	rw	<b>Minimum limit for ICC integrator threshold</b> The value is signed: -128 to 127
PWM_PERIOD_CALC_MODE	8	rw	<b>ICC PWM controller does not consider falling Dither Slope</b> 0 <sub>B</sub> No disabling of threshold calculation 1 <sub>B</sub> Skip threshold calculation on falling dither
OLSG_WARN_WINDOW	13:9	rw	<b>OLSG Warning Detection Blanking Time</b> $t_{OLwindow} = (<OLSG\_WARN\_WINDOW> + 1) * 64 * 1 / f_{sys}$
OLSG_WARN_EN	14	rw	<b>OLSG Warning Detection</b> 0 <sub>B</sub> Disable warning 1 <sub>B</sub> Enable warning

### 5.3.3.5 ICC PWM Frequency Controller Register

ICC PWM Frequency Controller Register

**PERIOD** Offset address: 0002<sub>H</sub>  
 ICC PWM Frequency Controller Register Value 0000<sub>H</sub>



Field	Bits	Type	Description
PERIOD_MANT	7:0	rw	<b>Mantissa of PWM Target Frequency</b> $t_{PWM} = \langle \text{PERIOD\_MANT} \rangle * 2^{\langle \text{PERIOD\_EXP} \rangle} * 1/f_{sys}$ <PERIOD_MANT> = 0 disables the ICC PWM Frequency Controller
PERIOD_EXP	10:8	rw	<b>Exponent of PWM Target Frequency</b> $t_{PWM} = \langle \text{PERIOD\_MANT} \rangle * 2^{\langle \text{PERIOD\_EXP} \rangle} * 1/f_{sys}$
LOW_FREQ_RANGE_EN	11	rw	<b>Low PWM Frequency Range</b> $t_{PWM} = \langle \text{PERIOD\_MANT} \rangle * 8 * 2^{\langle \text{PERIOD\_EXP} \rangle} * 1/f_{sys}$ 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
PWM_CTRL_PARAM	15:12	rw	<b>Control parameter ki of PWM Frequency Controller</b>

### 5.3.3.6 ICC Integrator Limitation Register

ICC Integrator Limitation Register

**INTEGRATOR\_LIMIT**

Offset address: 0003<sub>H</sub>

ICC Integrator Limitation Register

Value 43FF<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>	<b>AUTO_LIM_VALUE_ABS</b>					<b>LIM_VALUE_ABS</b>									
r	rw					rw									

Field	Bits	Type	Description
LIM_VALUE_ABS	9:0	rw	<b>Absolut Integrator Limit of ICC</b>
AUTO_LIM_VALUE_ABS	14:10	rw	<b>Integrator Limit of ICC after a setpoint update (Autolimit)</b>

### 5.3.3.7 Dither Clock Register

Dither Period Configuration

**DITHER\_CLK\_DIV** Offset address: 0004<sub>H</sub>  
Dither Clock Register Value 0000<sub>H</sub>

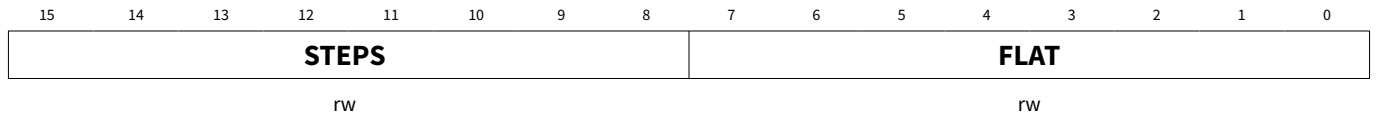
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>DITHER_SETPOINT_SYNC_EN</b>		<b>DITHER_PWM_SYNC_EN</b>		<b>EXP</b>						<b>MANT</b>					
rw		rw		rw						rw					

Field	Bits	Type	Description
MANT	9:0	rw	<b>Mantissa of Dither Reference Clock</b> $t_{ref\_clk} = (<MANT> * 2^{<EXP>}) * 1/f_{sys}$
EXP	13:10	rw	<b>Exponent of Dither Reference Clock</b> $t_{ref\_clk} = (<MANT> * 2^{<EXP>}) * 1/f_{sys}$
DITHER_PWM_SYNC_EN	14	rw	<b>Synchronization of Dither Period with PWM Period</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled
DITHER_SETPOINT_SYNC_EN	15	rw	<b>Synchronization of the Dither Period to a setpoint change</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

### 5.3.3.8 Dither Step Register

Dither Amplitude Configuration

**DITHER\_STEP** Offset address: 0005<sub>H</sub>  
 Dither Step Register Value 0000<sub>H</sub>



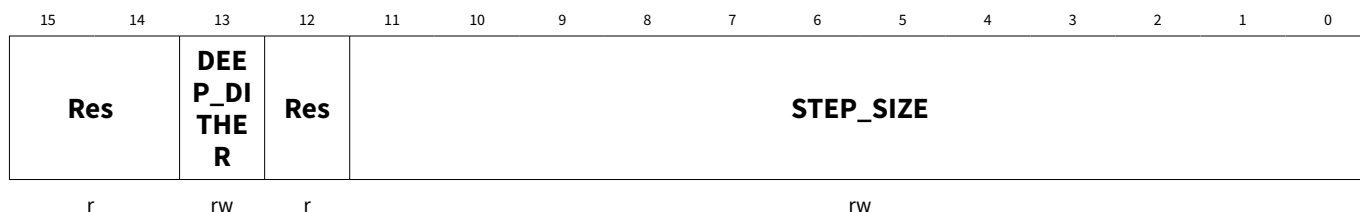
Field	Bits	Type	Description
FLAT	7:0	rw	<b>Number of flat Dither Reference Clocks tref_clk on top and bottom of the Dither waveform</b> $t_{flat} = \langle \text{FLAT} \rangle * t_{ref\_clk}$
STEPS	15:8	rw	<b>Number of Dither steps within a quarter Dither Period</b> $T_{Dither} = [4 * \langle \text{STEPS} \rangle + 2 * \langle \text{FLAT} \rangle] * t_{ref\_clk}$ $I_{Dither} = \langle \text{STEPS} \rangle * \langle \text{STEP\_SIZE} \rangle * 2 A / (2^{15} - 1)$ NOTE: If $\langle \text{STEP\_SIZE} \rangle = 0$ , the dither overlay $I_{Dither}$ is disabled. NOTE: If $\langle \text{STEPS} \rangle = 0$ , the dither overlay $I_{Dither}$ is disabled and the dither period $T_{Dither}$ is determined by $\langle \text{FLAT} \rangle$ NOTE: If $\langle \text{STEPS} \rangle = 0$ and $\langle \text{FLAT} \rangle = 0$ , the dither period $T_{Dither} = t_{ref\_clk}$



### 5.3.3.9 Dither Control Register

Dither Control Register

**DITHER\_CTRL** Offset address: 0006<sub>H</sub>  
 Dither Control Register Value 0000<sub>H</sub>



Field	Bits	Type	Description
STEP_SIZE	11:0	rw	<b>Size of Dither Steps resulting in a Dither Amplitude IDither</b> $I_{Dither} = \langle STEPS \rangle * \langle STEP\_SIZE \rangle * 2 A / (2^{15}-1)$
DEEP_DITHER	13	rw	<b>Deep Dither Feature</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

### 5.3.3.10 Channel Configuration Register

Channel Configuration Register

**CH\_CONFIG** Offset address: 0007<sub>H</sub>  
 Channel Configuration Register Value 0003<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>OFF_DIAG_C H</b>		<b>OC_ DIAG _EN</b>	<b>OL_TH_FIXED</b>					<b>OL_TH</b>		<b>I_DIAG</b>		<b>SLEWR</b>			
rwh		rwh	rw					rw		rw		rw			

Field	Bits	Type	Description
SLEWR	1:0	rw	<b>Channel Slew Rate</b> 00 <sub>B</sub> 1.0 V/us 01 <sub>B</sub> 2.5 V/us 10 <sub>B</sub> 5.0 V/us 11 <sub>B</sub> 10.0 V/us
I_DIAG	3:2	rw	<b>OFF-state Diagnosis Current Strength</b> 00 <sub>B</sub> 80 uA 01 <sub>B</sub> 190 uA 10 <sub>B</sub> 720 uA 11 <sub>B</sub> 1250 uA
OL_TH	6:4	rw	<b>Open Load Threshold relative to Setpoint</b> 000 <sub>B</sub> Disabled 001 <sub>B</sub> 1/8 of Current Setpoint 010 <sub>B</sub> 2/8 of Current Setpoint 011 <sub>B</sub> 3/8 of Current Setpoint 100 <sub>B</sub> 4/8 of Current Setpoint 101 <sub>B</sub> 5/8 of Current Setpoint 110 <sub>B</sub> 6/8 of Current Setpoint 111 <sub>B</sub> 7/8 of Current Setpoint
OL_TH_FIXED	12:7	rw	<b>Fixed Open Load Threshold</b> $I_{OLTH} = \langle OL\_TH\_FIXED \rangle * 128 * 2000\text{mA} / (2^{15} - 1)$ $I_{OLTH,parallel} = \langle OL\_TH\_FIXED \rangle * 128 * 4000\text{mA} / (2^{15} - 1)$
OC_DIAG_EN	13	rwh	<b>OC Diagnosis in OFF-state</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enable Output Stage for t <sub>OCon</sub> $t_{OCon} = [(\langle TON\_MANT \rangle + 1) * 2^{\langle EXP \rangle}] * 1/f_{SYS}$ NOTE: <TON_MANT> is located in the TON register. NOTE: <EXP> is located in the DITHER_CLK_DIV register.

(table continues...)

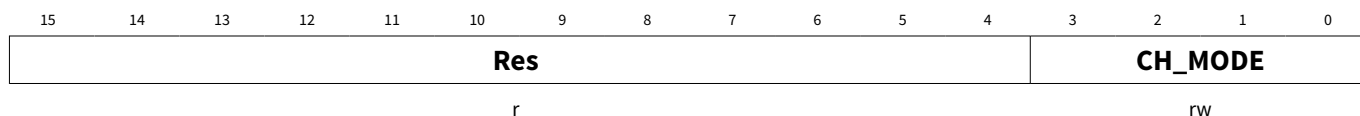
(continued)

Field	Bits	Type	Description
OFF_DIAG_CH	15:14	rwh	<b>OFF-state Diagnosis Current Sources Control</b> 00 <sub>B</sub> OFF-state Diagnosis Enabled 01 <sub>B</sub> Low Side Current Source Enabled 10 <sub>B</sub> High Side Current Source Enabled 11 <sub>B</sub> OFF-state Diagnosis Disabled

### 5.3.3.11 Channel Mode Register

Channel Mode Register: write access only possible in Config Mode

**MODE** Offset address: 000C<sub>H</sub>  
 Channel Mode Register Value 0000<sub>H</sub>

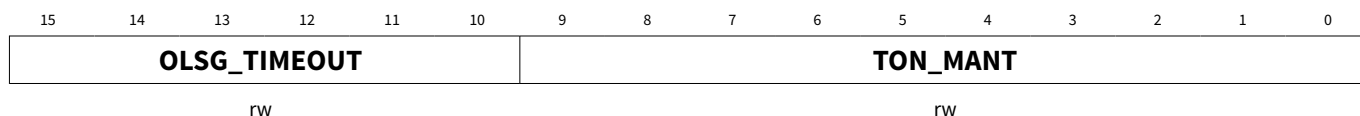


Field	Bits	Type	Description
CH_MODE	3:0	rw	<b>Channel Operation Mode</b> 0 <sub>H</sub> Off 1 <sub>H</sub> ICC Current Control 2 <sub>H</sub> Direct Drive Mode via SPI on-time setting (TON register) 3 <sub>H</sub> Direct Drive Mode via DRVx-pin C <sub>H</sub> Free running Measurement (2 <sup>16</sup> samples)

### 5.3.3.12 On-Time Register

Driver On-Time Configuration Register

**TON** Offset address: 000D<sub>H</sub>  
 On-Time Register Value 0000<sub>H</sub>

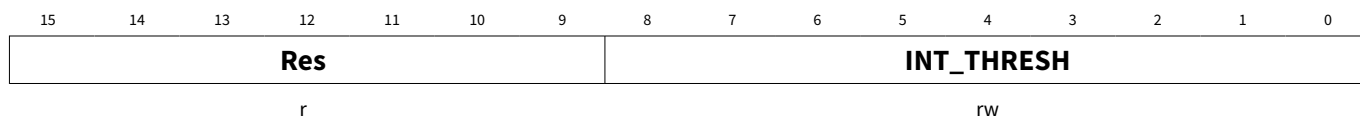


Field	Bits	Type	Description
TON_MANT	9:0	rw	<b>On-Time of Output stage (SPI Direct Drive Mode/OC-Detection)</b> $t_{OCOn} = [(<TON\_MANT>+1) * 2^{<EXP>}] * 1/f_{sys}$ NOTE: For OC detection in OFF-state the maximum $t_{on}$ period is 300ms and <TON_MANT> must be different to 0. $t_{on} = (<TON\_MANT> * 2^{<EXP>}) * 1/f_{sys}$ NOTE: The Period is derived from the Dither Period (DITHER_CLK_DIV) NOTE: <EXP> is located in the DITHER_CLK_DIV register
OLSG_TIMEOUT	15:10	rw	<b>Time out period for OLSG detection</b> $t_{OLSG\_TIMEOUT} = (<OLSG\_TIMEOUT> * 256 + 255) * 64 * 1/f_{sys}$

### 5.3.3.13 ICC Integrator Threshold Control Register

ICC Integrator Threshold Control Register

**CTRL\_INT\_THRESH** Offset address: 000E<sub>H</sub>  
 ICC Integrator Threshold Control Register Value 0003<sub>H</sub>



Field	Bits	Type	Description
INT_THRESH	8:0	rw	<b>ICC Integrator Threshold which determines the on-time of the PWM period</b> NOTE: <INT_THRESH> is used as initial threshold value for the ICC PWM Frequency Controller.

### 5.3.3.14 Feedback Duty Cycle Register

Duty Cycle Feedback Value

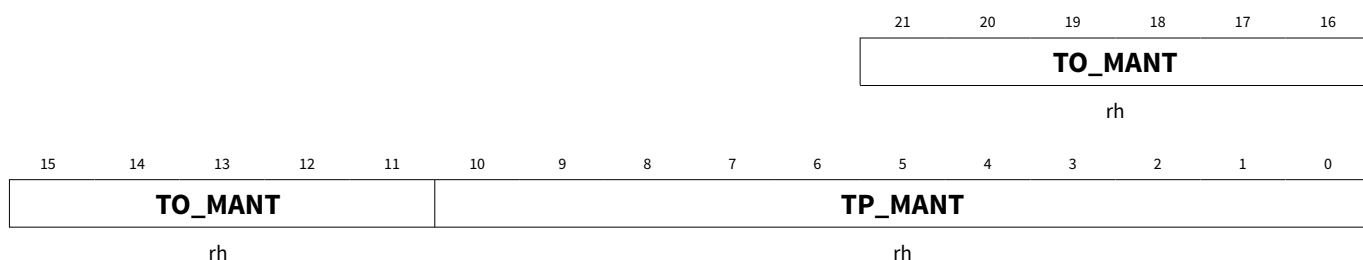
Read Only Register

**FB\_DC**

Feedback Duty Cycle Register

Offset address: 0200<sub>H</sub>

Value 00 0000<sub>H</sub>



Field	Bits	Type	Description
TP_MANT	10:0	rh	<b>Period Mantissa</b> $T_{meas} = \langle TP\_MANT \rangle * 2^{\langle EXP \rangle} * 1/f_{sys}$ NOTE: <EXP> is located in the FB_VBAT or FB_I_AVG register.
TO_MANT	21:11	rh	<b>On-time Mantissa</b> $t_{ON} = \langle TO\_MANT \rangle * 2^{\langle EXP \rangle} * 1/f_{sys}$ $DC = \langle TO\_MANT \rangle / \langle TP\_MANT \rangle$ NOTE: <EXP> is located in the FB_VBAT or FB_I_AVG register.

**Serial peripheral interface (SPI)**

**5.3.3.15 Feedback Average VBAT**

Average Battery Voltage (VBAT) Feedback Register  
 Read Only Register

**FB\_VBAT**

Feedback Average VBAT

Offset address: 0201<sub>H</sub>

Value 00 0000<sub>H</sub>



Field	Bits	Type	Description
VBAT_AVG_MANT	10:0	rh	<b>Average Battery Voltage Mantissa</b> $V_{BAT} = 41.47V * \langle VBAT\_AVG\_MANT \rangle / \langle TP\_MANT \rangle$ NOTE: <TP_MANT> is located in the FB_DC register
EXP	15:12	rh	<b>Measurement Exponent</b>



### 5.3.3.16 Feedback Average Current

Average Current Feedback Value

Read Only Register

#### FB\_I\_AVG

Feedback Average Current

Offset address: 0202<sub>H</sub>

Value 00 0000<sub>H</sub>



Field	Bits	Type	Description
I_AVG_MANT	11:0	rh	<b>Signed Mantissa of Average Current Feedback (two's complement)</b> $I_{avg} = 4A * \langle I\_AVG\_MANT \rangle / \langle TP\_MANT \rangle$ NOTE: <TP_MANT> is located in the FB_DC register
EXP	15:12	rh	<b>Measurement Exponent</b>

### 5.3.3.17 Feedback Min/Max Current

Minimum/Maximum Current Feedback Register

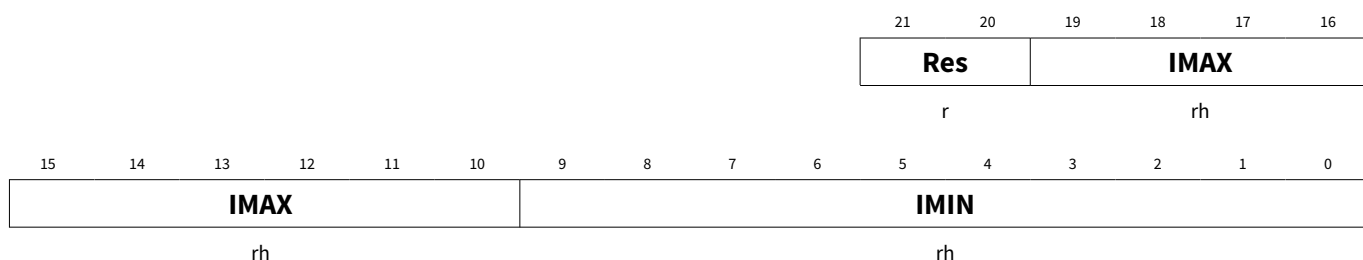
Read Only Register

#### FB\_IMIN\_IMAX

Feedback Min/Max Current

Offset address: 0203<sub>H</sub>

Value 00 0000<sub>H</sub>



Field	Bits	Type	Description
IMIN	9:0	rh	<b>Signed Minimum Current of last measurement period (two's complement)</b> $I_{min} = \langle \text{IMIN} \rangle * 4A / (2^9 - 1)$
IMAX	19:10	rh	<b>Signed Maximum Current of last measurement period (two's complement)</b> $I_{max} = \langle \text{IMAX} \rangle * 4A / (2^9 - 1)$

### 5.3.3.18 Feedback signed Current

Signed Average Current Measurement over free running period ( $2^{16} f_{sys}$  cycles)

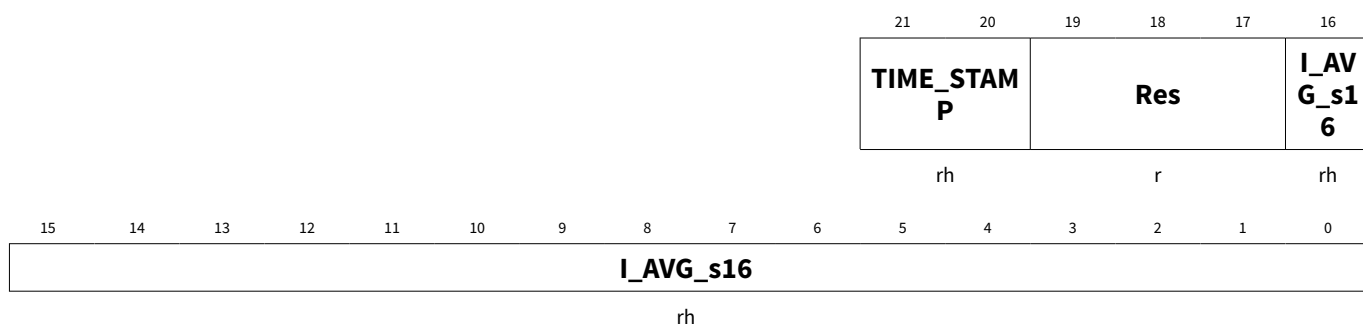
Read Only Register

#### FB\_I\_AVG\_s16

Feedback signed Current

Offset address: 0204<sub>H</sub>

Value 00 0000<sub>H</sub>



Field	Bits	Type	Description
I_AVG_s16	16:0	rh	<b>Average Current Measurement over free running period (<math>2^{16} f_{sys}</math> cycles) - two's complement</b> $I_{avg16} = 4A * \langle I\_AVG\_s16 \rangle / (2^{16} - 1)$
TIME_STAMP	21:20	rh	<b>Time Stamp for signed Average Current Measurement over free running period</b>

### 5.3.3.19 Feedback ICC Integrator Threshold

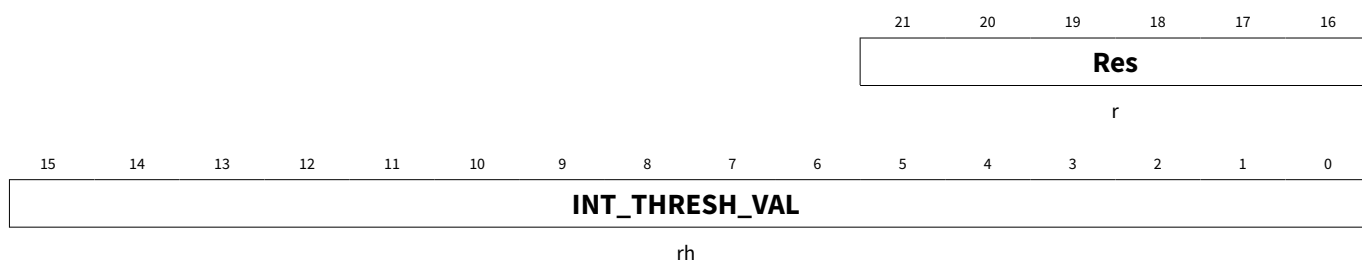
ICC PWM Frequency Controller Integrator Thershold Feedback  
 Read Only Register

**FB\_INT\_THRESH**

Feedback ICC Integrator Threshold

Offset address: 0205<sub>H</sub>

Value 00 0180<sub>H</sub>



Field	Bits	Type	Description
INT_THRESH_VAL	15:0	rh	ICC PWM Frequency Controller Calculated Integrator Threshold Value

### 5.3.3.20 Feedback Min/Max PWM Period

Minimum and Maximum PWM Frequency Feedback of last Measurement period

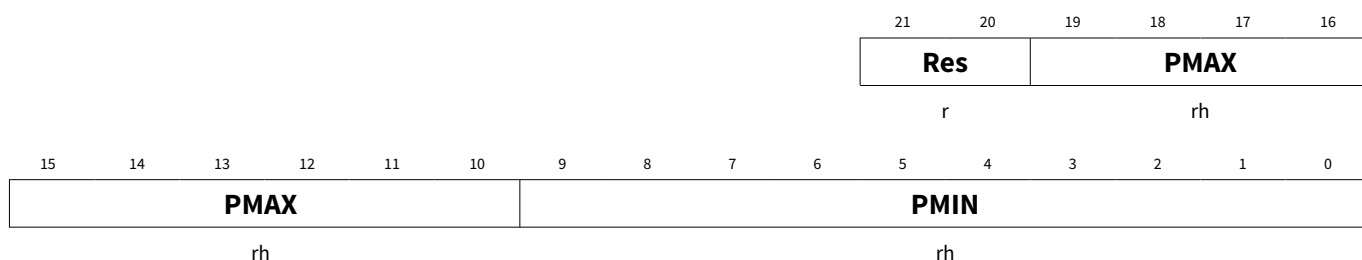
Read Only Register

**FB\_PERIOD\_MIN\_MAX**

Feedback Min/Max PWM Period

Offset address: 0206<sub>H</sub>

Value 00 0000<sub>H</sub>



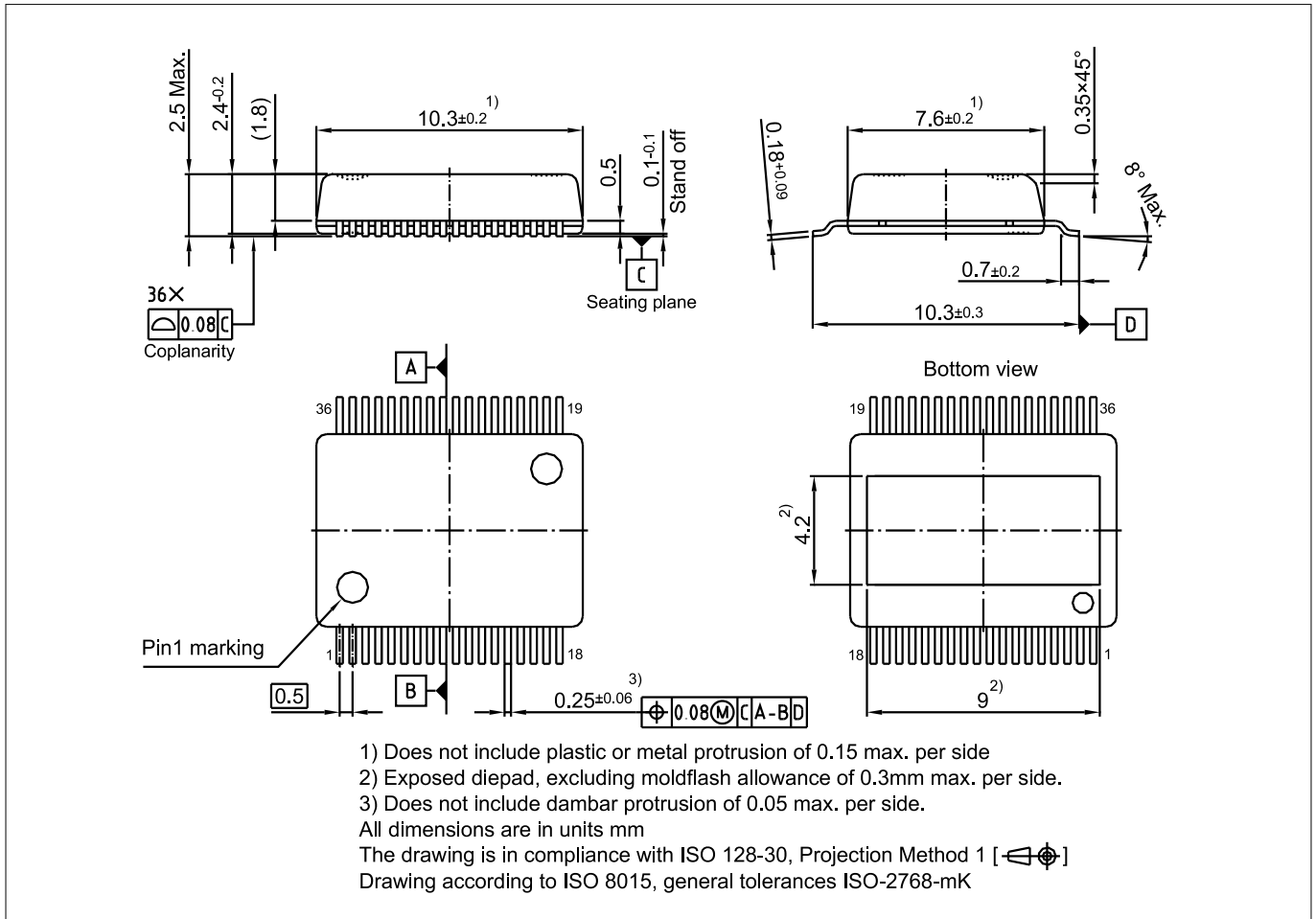
Field	Bits	Type	Description
PMIN	9:0	rh	<b>Minimum PWM period of last Measurement period</b> $f_{PWM\_min} = f_{sys} / (<PMIN> * 256)$
PMAx	19:10	rh	<b>Maximum PWM period of last Measurement period</b> $f_{PWM\_max} = f_{sys} / (<PMAx> * 256)$



**Package dimensions**

**7 Package dimensions**

**7.1 TDS\_Package dimensions**



**Figure 27 Package outlines**

**Green Product**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with the government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Revision history**

**Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
Datasheet v1.0	2021-12-15	Initial release



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