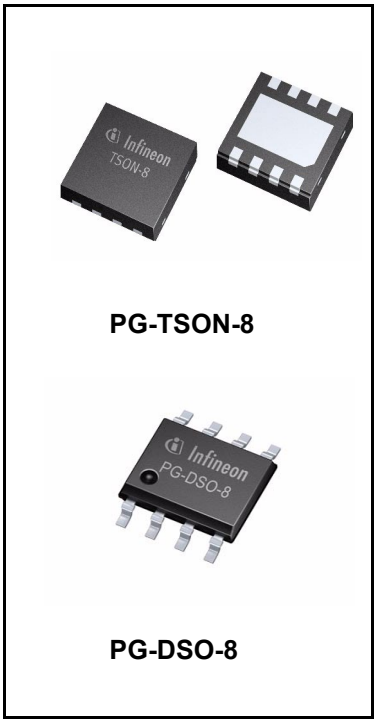
TLE9250V

High Speed CAN Transceiver



1 Overview

Features

- Fully compliant to ISO 11898-2 (2016) and SAE J2284-4/-5
- Reference device and part of Interoperability Test Specification for CAN Transceiver
- Guaranteed loop delay symmetry for CAN FD data frames up to 5 MBit/s
- Very low electromagnetic emission (EME) allows the use without additional common mode choke
- V_{IO} input for voltage adaption to the µC interface (3.3V & 5V)
- Wide common mode range for electromagnetic immunity (EMI)
- Excellent ESD robustness +/-8kV (HBM) and +/-11kV (IEC 61000-4-2)
- Extended supply range on the V_{CC} and V_{IO} supply
- CAN short circuit proof to ground, battery, V_{CC} and V_{IO}
- TxD time-out function
- Very low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients according ISO 7637 and SAE J2962-2 standards
- Power-save mode
- Green Product (RoHS compliant)
- Small, leadless TSON8 package designed for automated optical inspection (AOI)

Potential applications

- Engine Control Unit (ECUs)
- Electric Power Steering
- Transmission Control Units (TCUs)
- Chassis Control Modules

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

Type	Package	Marking
TLE9250VLE	PG-TSON-8	9250V
TLE9250VSJ	PG-DSO-8	9250V

The TLE9250V is the latest Infineon high-speed CAN transceiver generation, used inside HS CAN networks for automotive and also for industrial applications. It is designed to fulfill the requirements of ISO 11898-2 (2016) physical layer specification and respectively also the SAE standards J1939 and J2284.

The TLE9250V is available in a PG-DSO-8 package and in a small, leadless PG-TSON-8 package. Both packages are RoHS compliant and halogen free. The PG-TSON-8 package supports the solder joint requirements for automated optical inspection (AOI).

As an interface between the physical bus layer and the HS CAN protocol controller, the TLE9250V protects the microcontroller against interferences generated inside the network. A very high ESD robustness and the perfect RF immunity allows the use in automotive applications without adding additional protection devices, like suppressor diodes for example.

While the transceiver TLE9250V is not supplied the bus is switched off and illustrates an ideal passive behavior with the lowest possible load to all other subscribers of the HS CAN network.

Based on the high symmetry of the CANH and CANL output signals, the TLE9250V provides a very low level of electromagnetic emission (EME) within a wide frequency range. The TLE9250V fulfills even stringent EMC test limits without additional external circuit, like a common mode choke for example.

The perfect transmitter symmetry combined with the optimized delay symmetry of the receiver enables the TLE9250V to support CAN FD data frames. Depending on the size of the network and the along coming parasitic effects the device supports bit rates up to 5 MBit/s.

Fail-safe features like overtemperature protection, output current limitation or the TxD time-out feature protect the TLE9250V and the external circuitry from irreparable damage.

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2 Block diagram

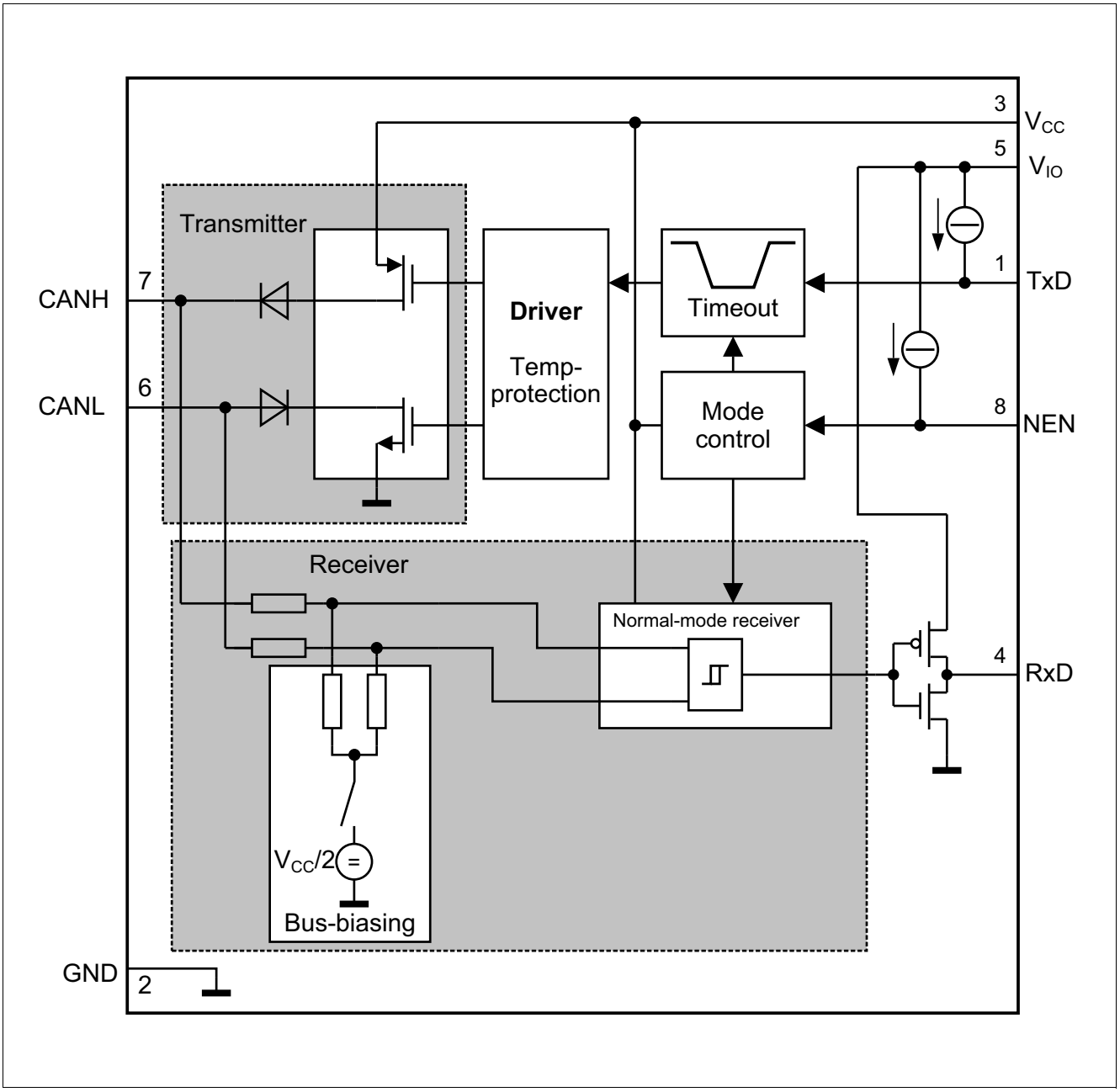

Figure 1 Functional block diagram

3 Pin configuration

3.1 Pin assignment

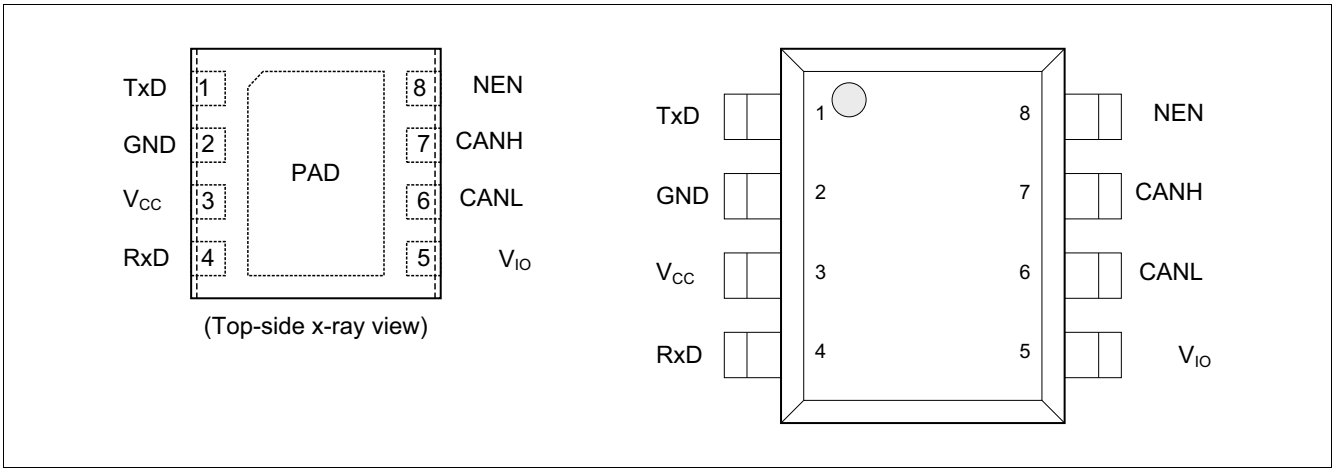

Figure 2 Pin configuration

3.2 Pin definitions

Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	**Transmit Data Input;** Internal pull-up to V_{IO}, “low” for dominant state.
2	GND	**Ground**
3	V_{CC}	**Transmitter Supply Voltage;** 100 nF decoupling capacitor to GND required, V_{CC} can be turned off in power-save mode.
4	RxD	**Receive Data Output;** “low” in dominant state.
5	V_{IO}	**Digital Supply Voltage;** Supply voltage input to adapt the logical input and output voltage levels of the transceiver to the microcontroller supply, 100 nF decoupling capacitor to GND required.
6	CANL	**CAN Bus Low Level I/O;** “low” in dominant state.
7	CANH	**CAN Bus High Level I/O;** “high” in dominant state.
8	NEN	**Not Enable Input;** Internal pull-up to V_{IO}, “low” for Normal-operating mode.
PAD	–	Connect to PCB heat sink area. Do not connect to other potential than GND.

4 General product characteristics

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_8.1.1
Digital supply voltage	V_{IO}	-0.3	–	6.0	V	–	P_8.1.2
CANH and CANL DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_8.1.3
Differential voltage between CANH and CANL	V_{CAN_Diff}	-40	–	40	V	–	P_8.1.4
Voltages at the digital I/O pins: NEN, RxD, TxD	V_{MAX_IO1}	-0.3	–	6.0	V	–	P_8.1.5
Voltages at the digital I/O pins: NEN, RxD, TxD	V_{MAX_IO2}	-0.3	–	V_{IO} + 0.3	V	–	P_8.1.6
Currents							
RxD output current	I_{RxD}	-5	–	5	mA	–	P_8.1.7
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_8.1.8
Storage temperature	T_S	-55	–	150	°C	–	P_8.1.9
ESD Resistivity							
ESD immunity at CANH, CANL versus GND	$V_{ESD\_HBM\_CAN}$	-8	–	8	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_8.1.11
ESD immunity at all other pins	$V_{ESD\_HBM\_ALL}$	-2	–	2	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_8.1.12
ESD immunity all pins	V_{ESD_CDM}	-750	–	750	V	CDM[3)]	P_8.1.13

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001
3) ESD susceptibility, Charge Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal-operating range. Protection functions are not designed for continuos repetitive operation.

4.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Transmitter supply voltage	V_{CC}	4.5	–	5.5	V	–	P_8.2.1
Digital supply voltage	V_{IO}	3.0	–	5.5	V	–	P_8.2.2
Thermal Parameters							
Junction temperature	T_j	-40	–	150	°C	1)	P_8.2.3

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistances							
Junction to Ambient PG-TSON-8	R_{thJA_TSON8}	–	65	–	K/W	2)	P_8.3.1
Junction to Ambient PG-DSO-8	R_{thJA_DSO8}	–	120	–	K/W	2)	P_8.3.2
Thermal Shutdown (junction temperature)							
Thermal shutdown temperature, rising	T_{JSD}	170	180	190	°C	temperature falling: Min. 150°C	P_8.3.3
Thermal shutdown hysteresis	ΔT	5	10	20	K	–	P_8.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board. The product (TLE9250V) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu)

5 High-speed CAN functional description

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the Controller Area Network (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed in recent years.

5.1 High-speed CAN physical layer

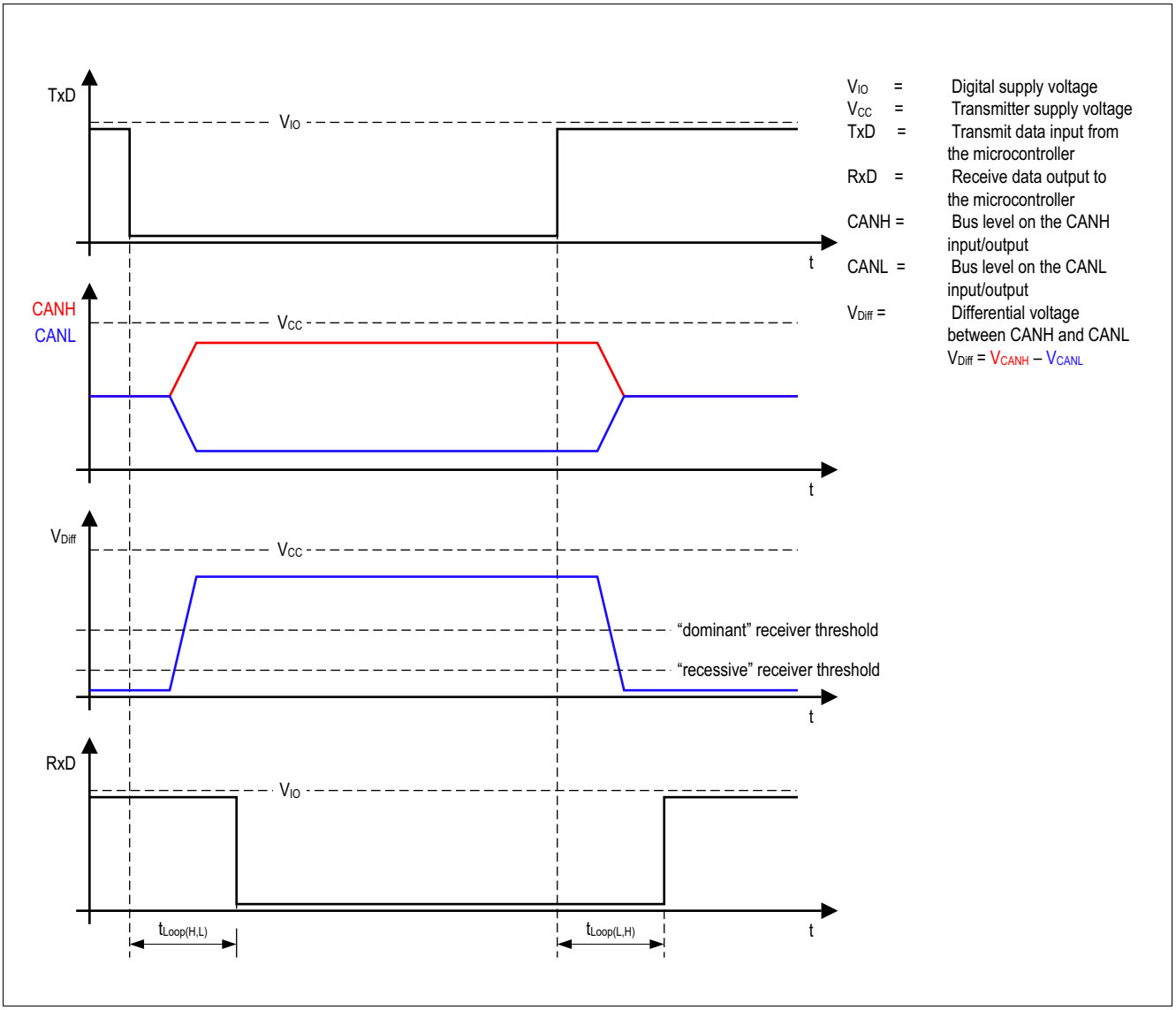

Figure 3 High-speed CAN bus signals and logic signals

High-speed CAN functional description

The TLE9250V is a high-speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential network which allows data transmission rates up to 5 MBit/s. The characteristic for a HS CAN network are the two signal states on the CAN bus: dominant and recessive (see **Figure 3**).

The CANH and CANL pins are the interface to the CAN bus and both pins operate as an input and output. The RxD and TxD pins are the interface to the microcontroller. The pin TxD is the serial data input from the CAN controller, the RxD pin is the serial data output to the CAN controller. As shown in **Figure 1**, the HS CAN transceiver TLE9250V includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time. The HS CAN transceiver TLE9250V converts the serial data stream which is available on the transmit data input TxD, into a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the TLE9250V monitors the data on the CAN bus and converts them to a serial, single-ended signal on the RxD output pin. A logical “low” signal on the TxD pin creates a dominant signal on the CAN bus, followed by a logical “low” signal on the RxD pin (see **Figure 3**). The feature, broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within CAN networks.

The voltage levels for HS CAN transceivers are defined in ISO 11898-2. Whether a data bit is dominant or recessive depends on the voltage difference between the CANH and CANL pins:
$V_{Diff} = V_{CANH} - V_{CANL}$.
To transmit a dominant signal to the CAN bus the amplitude of the differential signal V_{Diff} is higher than or equal to 1.5 V. To receive a recessive signal from the CAN bus the amplitude of the differential V_{Diff} is lower than or equal to 0.5 V.

“Partially-supplied” high-speed CAN networks are those where the CAN bus nodes of one common network have different power supply conditions. Some nodes are connected to the common power supply, while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus subscriber is supplied or not, each subscriber connected to the common bus media must not interfere in the communication. The TLE9250V is designed to support “partially-supplied” networks. In power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

For permanently supplied ECU's, the HS CAN transceiver TLE9250V provides a Power-save mode. In Power-save mode, the power consumption of the TLE9250V is optimized to a minimum

The voltage level on the digital input TxD and the digital output RxD is determined by the power supply level at the V_{IO} pin. Depending on the voltage level at the V_{IO} pin, the signal levels on the logic pins (STB, TxD and RxD) are compatible with microcontrollers having a 5 V or 3.3 V I/O supply. Usually the digital power supply V_{IO} of the transceiver is connected to the I/O power supply of the microcontroller (see **Figure 60**).

6 Modes of operation

The TLE9250V supports three different modes of operation (see **Figure 4** and **Table 5**):

- Normal-operating mode
- Power-save mode
- Forced-receive-only mode

Mode changes are either triggered by the mode selection input pin NEN or by an undervoltage event on the transmitter supply V_{CC}. An undervoltage event on the digital supply V_{IO} powers down the TLE9250V.

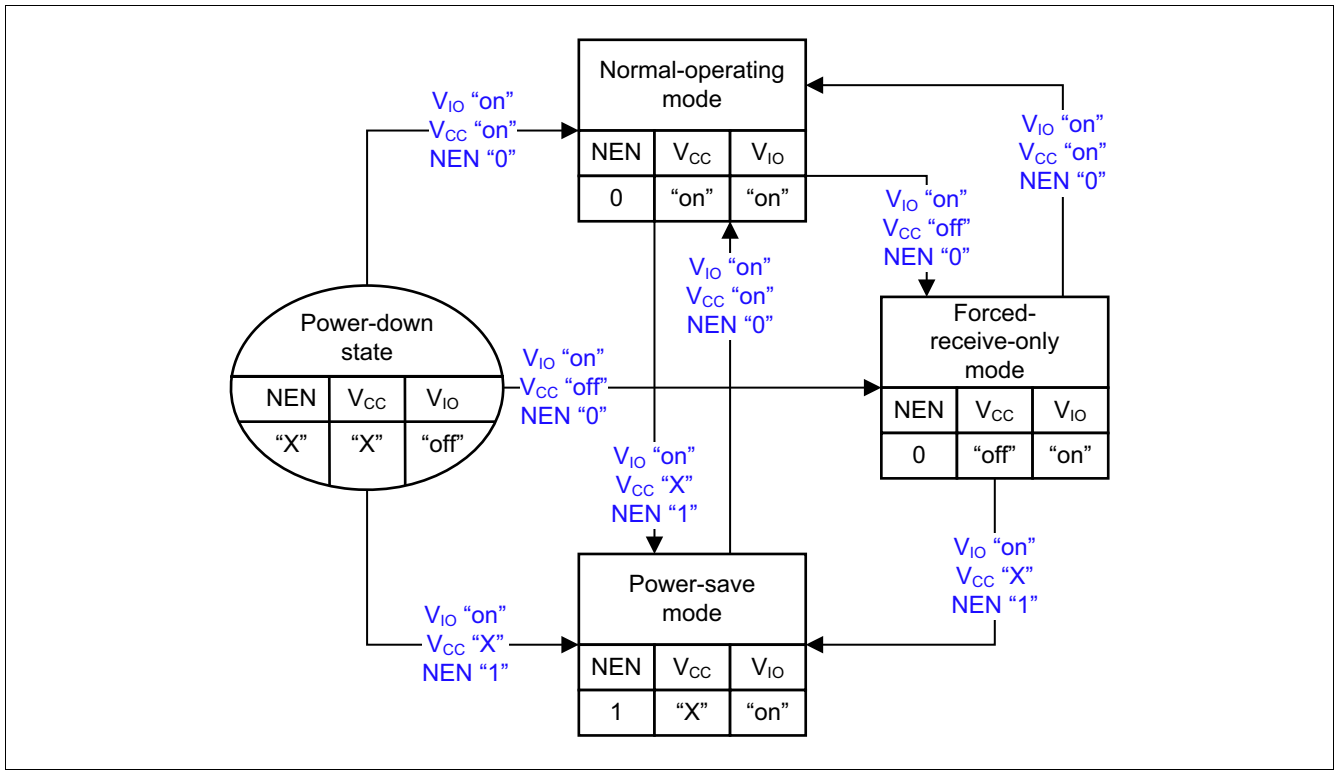

Figure 4 Mode state diagram

Table 5 Modes of operation

Mode	NEN	V_{IO}	V_{CC}	Bus Bias	Transmitter	Normal-mode Receiver
Normal-operating	“low”	“on”	“on”	$V_{CC}/2$	“on”	“on”
Power-save	“high”	“on”	“X”	floating	“off”	“off”
Forced-receive-only	“low”	“on”	“X”	GND	“off”	“on”
Power-down state	“X”	“off”	“X”	floating	“off”	“off”

6.1 Normal-operating mode

In Normal-operating mode the transceiver TLE9250V sends and receives data from the HS CAN bus. All functions are active (see also **Figure 4** and **Table 5**):

- The transmitter is active and drives the serial data stream on the TxD input pin to the bus pins CANH and CANL.
- The normal-mode receiver is active and converts the signals from the bus to a serial data stream on the RxD output.
- The RxD output pin indicates the data received by the normal-mode receiver.
- The bus biasing is connected to $V_{CC}/2$.
- The NEN input pin is active and changes the mode of operation.
- The TxD time-out function is enabled and disconnects the transmitter in case a time-out is detected.
- The overtemperature protection is enabled and disconnects the transmitter in case an overtemperature is detected.
- The undervoltage detection on V_{CC} is enabled and triggers a mode change to Forced-receive-only in case an undervoltage event is detected.
- The undervoltage detection on V_{IO} is enabled and powers down the device in case of detection.

Normal-operating mode is entered from Power-save mode and Forced-receive-only mode, when the NEN input pin is set to logical “low”.

Normal-operating mode can only be entered when all supplies are available:

- The transmitter supply V_{CC} is available ($V_{CC} > V_{CC(UV,R)}$).
- The digital supply V_{IO} is available ($V_{IO} > V_{IO(UV,R)}$).

6.2 Forced-receive-only mode

The Forced-receive-only mode is a fail-safe mode of the TLE9250V, which will be entered when the transmitter supply V_{CC} is not available . The following functions are available (see also **Figure 4** and **Table 5**):

- The transmitter is disabled and the data available on the TxD input is blocked.
- The normal-mode receiver is enabled.
- The RxD output pin indicates the data received by the normal-mode receiver.
- The bus biasing is connected to GND.
- The NEN input pin is active and changes the mode of operation to Power-save mode, if logical “high”.
- The TxD time-out function is disabled.
- The overtemperature protection is disabled.
- The undervoltage detection on V_{CC} is active.
- The undervoltage detection on V_{IO} is enabled and powers down the device in case of detection.
- Forced-receive-only mode is entered from power-down state if the NEN input pin is set to logical “low” and the digital supply V_{IO} is available ($V_{IO} > V_{IO(UV,R)}$).
- Forced-receive-only mode is entered from Normal-operating mode by an undervoltage event on the transmitter supply V_{CC}.

6.3 Power-save mode

In Power-save mode the transmitter and receiver are disabled. (see also and **Table 5**):

- The transmitter is disabled and the data available on the TxD input is blocked.
- The receiver is disabled and the data available on the bus is blocked.

- The RxD output pin is permanently set to logical “high”.
- The bus biasing is floating.
- The NEN input pin is active and changes the mode of operation to Normal-operating mode, if logical “low” and V_{CC} ($V_{CC} > V_{CC(UV,R)}$) is available.
- The overtemperature protection is disabled.
- The undervoltage detection on V_{CC} is disabled. In Power-save mode the device can operate without the transmitter supply V_{CC}.
- The undervoltage detection on V_{IO} is enabled and powers down the device in case of detection.

6.4 Power-down state

Independent of the transmitter supply V_{CC} and of the status at NEN input pin the TLE9250V is powered down if the supply voltage $V_{IO} < V_{IO(UV,F)}$ (see **Figure 4**).

In the power-down state the differential input resistors of the receiver are switched off. The CANH and CANL bus interface of the TLE9250V is floating and acts as a high-impedance input with a very small leakage current. The high-ohmic input does not influence the recessive level of the CAN network and allows an optimized EME performance of the entire HS CAN network. In power-down state the transceiver is an invisible node to the bus.

7 Changing the mode of operation

7.1 Power-up and power-down

The HS CAN transceiver TLE9250V powers up by applying the digital supply V_{IO} to the device ($V_{IO} > V_{IO(U,R)}$). After powering up, the device enters one out of three operating modes (see **Figure 5** and **Figure 6**). Depending on the condition of the transmitter supply voltage V_{CC} and the mode selection pin NEN the device can enter every mode of operation after the power-up:

- V_{CC} is available and the NEN input is set to “low” - Normal-operating mode
- The NEN input is set to “high” - Power-save mode
- V_{CC} is disabled and the NEN input is set to “low” - Forced-receive-only mode

The device TLE9250V powers down when the V_{IO} supply falls below the undervoltage detection threshold ($V_{IO} < V_{IO(U,F)}$), regardless if the transmitter supply V_{CC} is available or not. The power-down detection is active in every mode of operation.

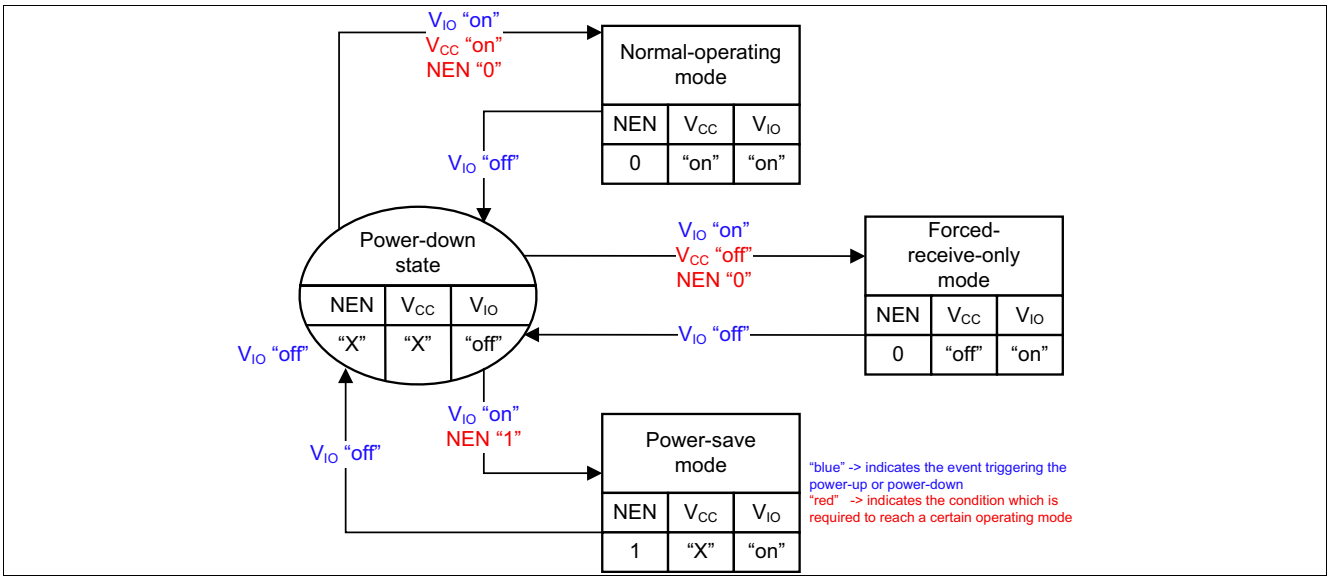

Figure 5 Power-up and power-down

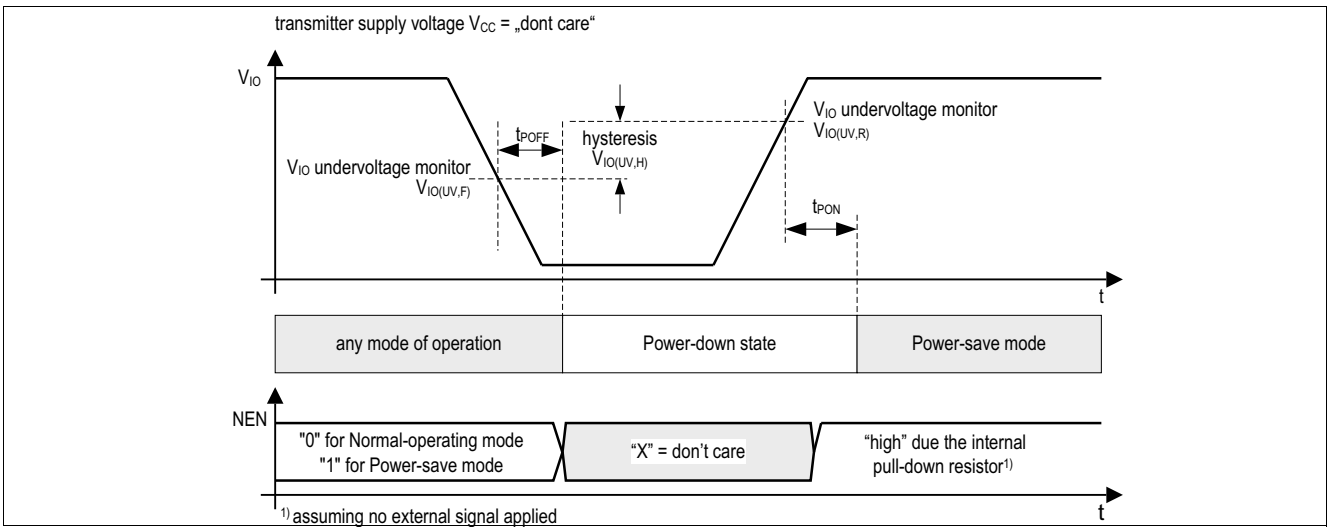

Figure 6 Power-up and power-down timings

7.2 Mode change by the NEN pin

When the TLE9250V is supplied with the digital voltage V_{IO} the internal logic works and mode change by the mode selection pin NEN is possible.

By default the NEN input pin is logical “high” due to the internal pull-up current source to V_{IO}. Changing the NEN input pin to logical “low” in Power-save mode triggers a mode change to Normal-operating mode (see **Figure 7**). To enter Normal-operating mode the transmitter supply V_{CC} needs to be available.

Power-save mode can be entered from Normal-operating mode and from Forced-receive-only mode by setting the NEN pin to logical “high”. Entering Forced-receive-only mode from Power-save mode is not possible by the NEN pin. The device remains in Power-save mode independently of the V_{CC} supply voltage.

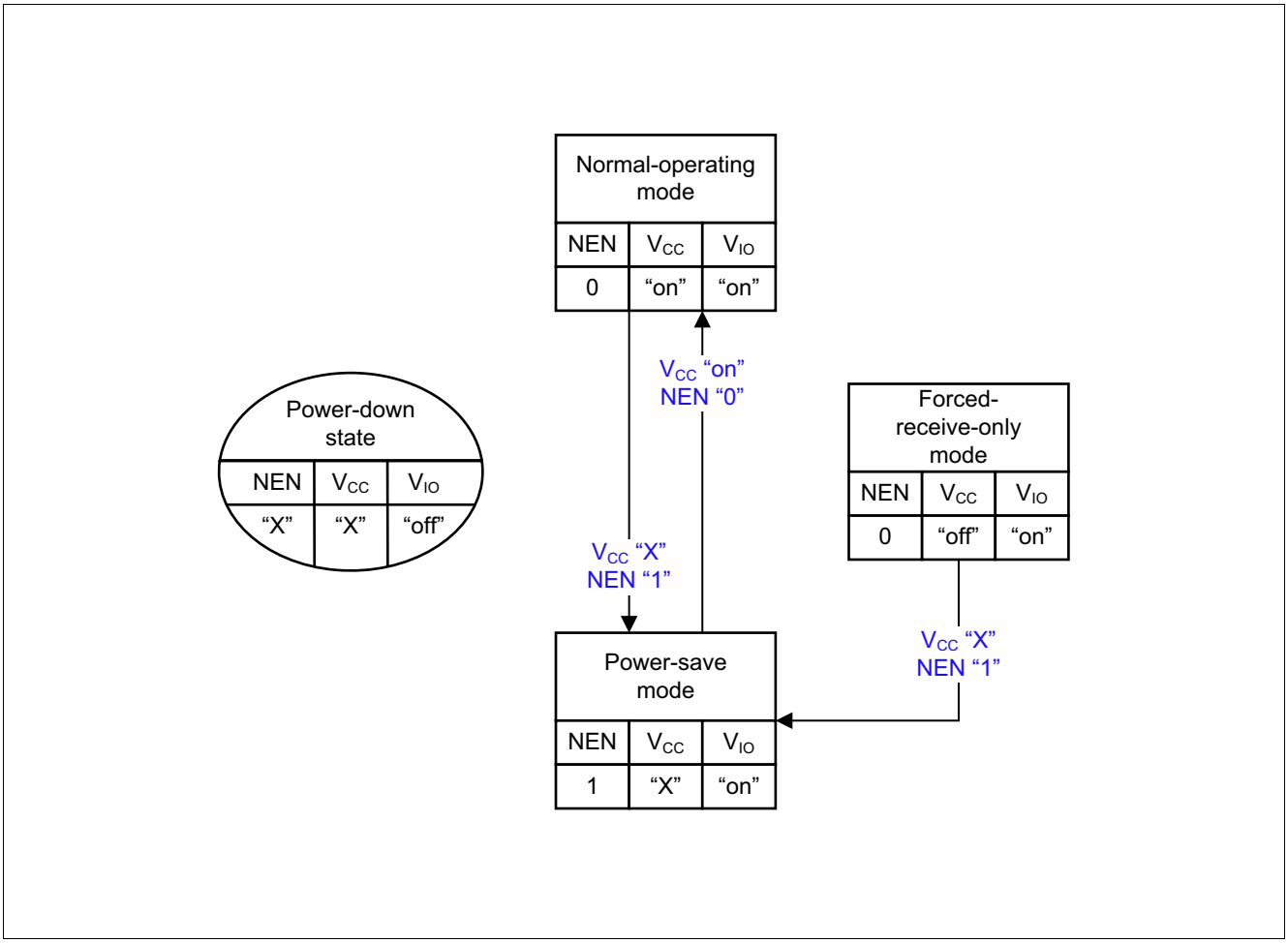

Figure 7 Mode selection by the NEN pin

7.3 Mode changes by V_{CC} undervoltage

When the transmitter supply V_{CC} ($V_{CC} < V_{CC(U/F)}$) is in undervoltage condition, the TLE9250V might not be able to provide the correct bus levels on the CANH and CANL output pins. To avoid any interference with the network the TLE9250V blocks the transmitter and changes the mode of operation when an undervoltage event is detected (see **Figure 8** and **Figure 9**).

In Normal-operating mode a undervoltage event on transmitter supply V_{CC} ($V_{CC} < V_{CC(U/F)}$) triggers a mode change to Forced-receive-only mode.

In Forced-receive-only mode the undervoltage detection V_{CC} ($V_{CC} < V_{CC(U/F)}$)is enabled. In Power-save mode the undervoltage detection is disabled. In these modes the TLE9250V can operate without the transmitter supply V_{CC}.

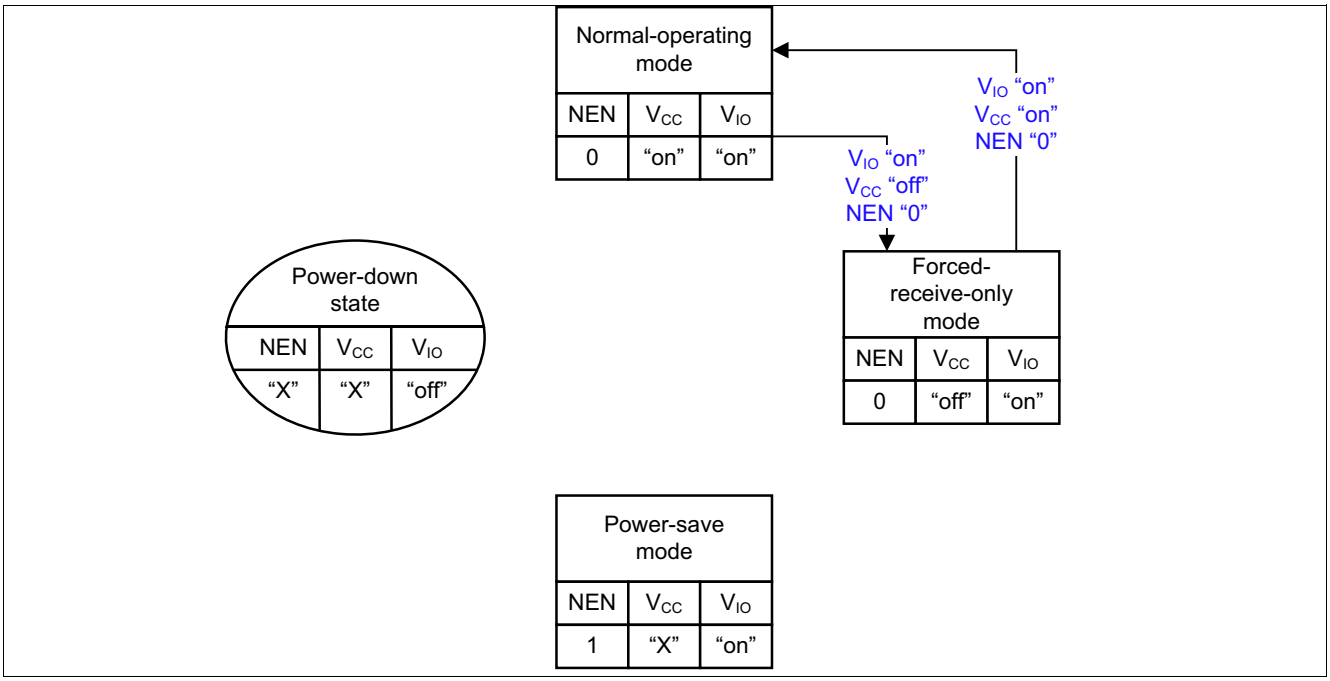

Figure 8 Mode changes by undervoltage events on V_{CC}

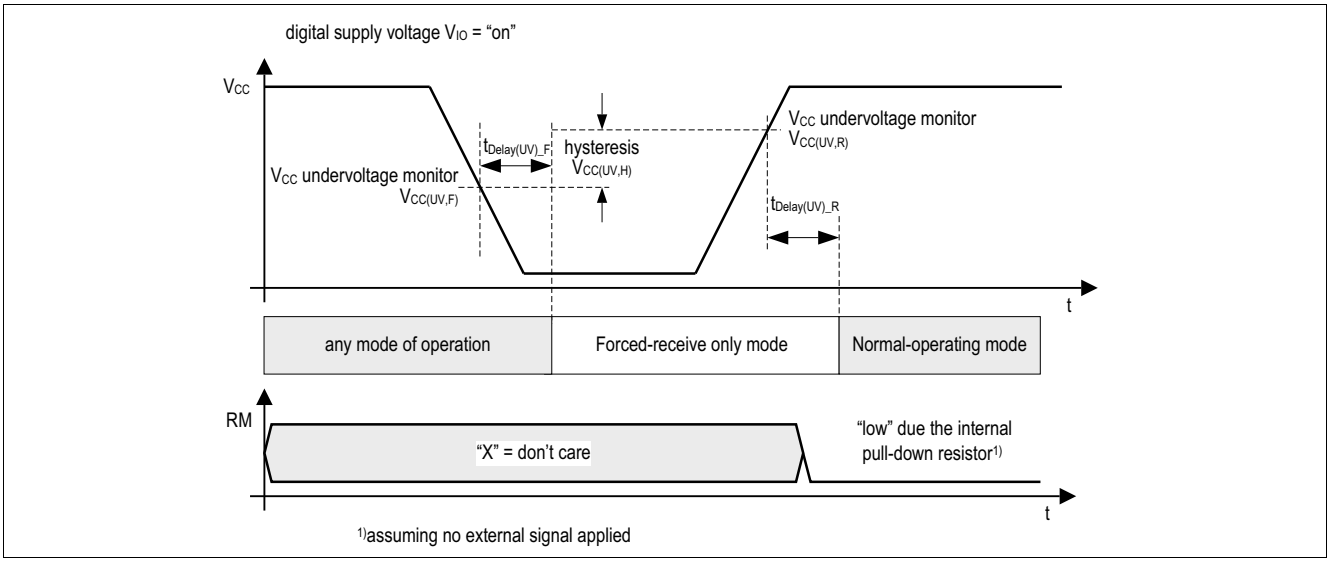

Figure 9 Undervoltage on the transmitter supply V_{CC}

8 Fail safe functions

8.1 Short circuit protection

The CANH and CANL bus pins are proven to cope with a short circuit fault against GND and against the supply voltages. A current limiting circuit protects the transceiver against damages. If the device is heating up due to a continuous short on the CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

8.2 Unconnected logic pins

All logic input pins have an internal pull-up current source to V_{IO}. In case the V_{IO} and V_{CC} supply is activated and the logical pins are open, the TLE9250V enters into the Power-save mode by default.

8.3 TxD time-out function

The TxD time-out feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously “low”. A continuous “low” signal on the TxD pin might have its root cause in a locked-up microcontroller or in a short circuit on the printed circuit board, for example.

In Normal-operating mode, a logical “low” signal on the TxD pin for the time $t > t_{TxD}$ enables the TxD time-out feature and the TLE9250V disables the transmitter (see **Figure 10**). The receiver is still active and the data on the bus continues to be monitored by the RxD output pin.

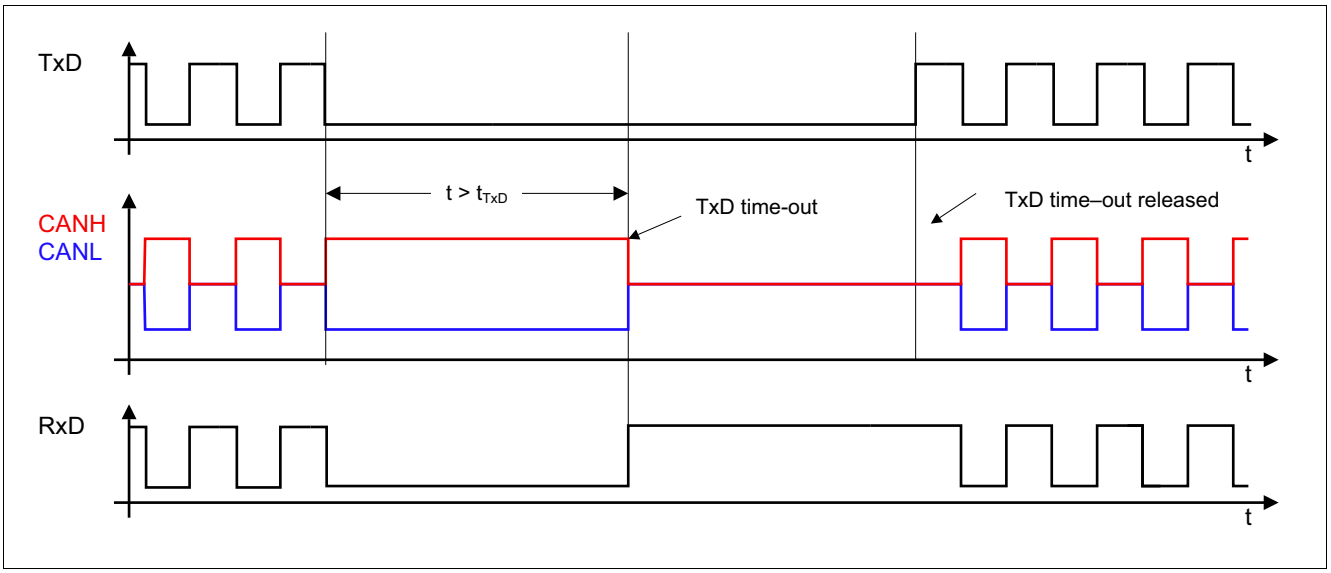

Figure 10 TxD time-out function

Figure 10 illustrates how the transmitter is deactivated and activated again. A permanent “low” signal on the TxD input pin activates the TxD time-out function and deactivates the transmitter. To release the transmitter after a TxD time-out event, the TLE9250V requires a signal change on the TxD input pin from logical “low” to logical “high”.

8.4 Overtemperature protection

The TLE9250V has an integrated overtemperature detection to protect the TLE9250V against thermal overstress of the transmitter. The overtemperature protection is only active in Normal-operating mode. In

case of an overtemperature condition, the temperature sensor will disable the transmitter while the transceiver remains in Normal-operating mode. After the device has cooled down the transmitter is activated again (see **Figure 11**). A hysteresis is implemented within the temperature sensor.

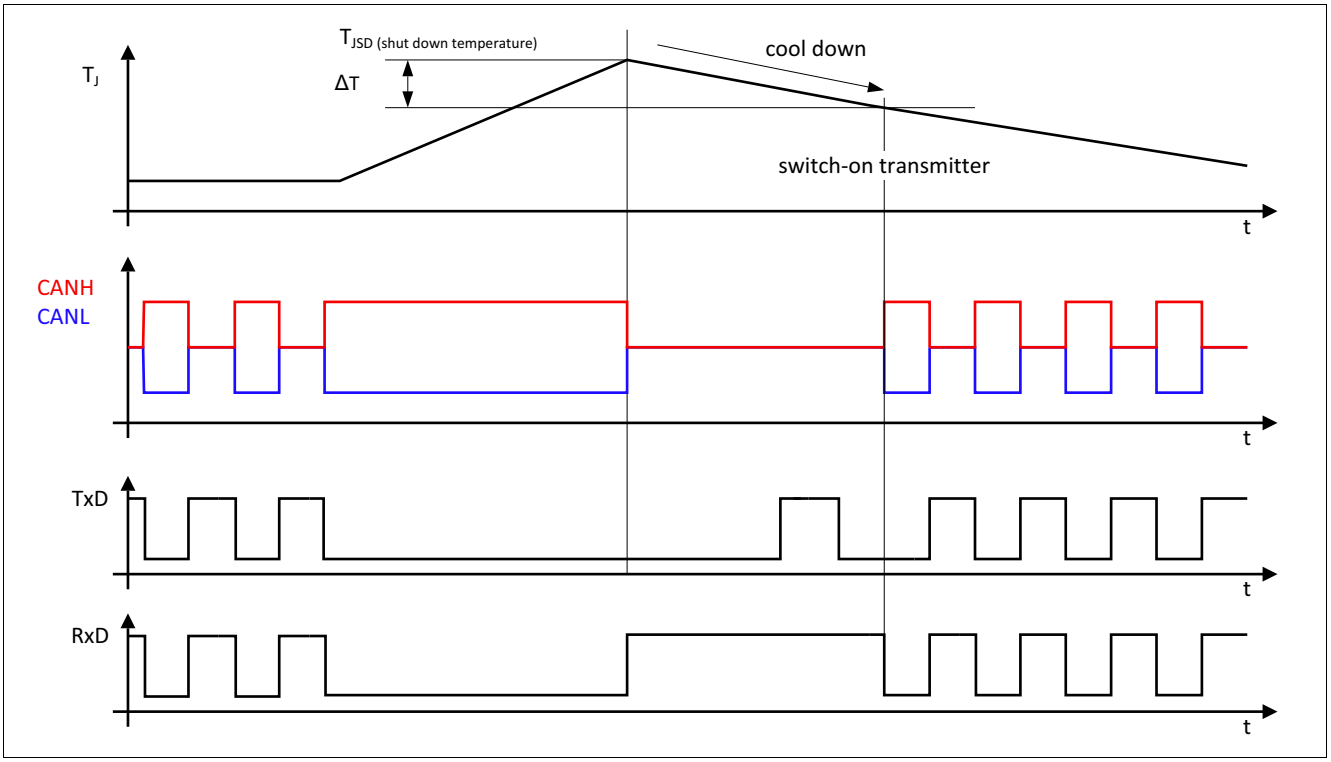

Figure 11 Overtemperature proctection

8.5 Delay time for mode change

The HS CAN transceiver TLE9250V changes the mode of operation within the time window t_{Mode}. During the mode change from Power-save mode to non-low power mode the RxD output pin is permanently set to logical “high” and does not reflect the status on the CANH and CANL input pins.
After the mode change is completed, the transceiver TLE9250V releases the RxD output pin.

9 Electrical characteristics

9.1 Functional device characteristics

Table 6 Electrical characteristics

4.5 V $< V_{CC} <$ 5.5 V; 3.0 V $< V_{IO} <$ 5.5 V; R_L = 60 Ω; -40 °C $< T_j <$ 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption at V_{CC} Normal-operating, recessive state	I_{CC_R}	–	2	4	mA	$V_{TxD} = V_{IO}$; V_{NEN} = 0 V; V_{Diff} = 0 V;	P_9.1.1
Current consumption at V_{CC} Normal-operating mode, dominant state	I_{CC_D}	–	38	48	mA	$V_{TxD} = V_{NEN}$ = 0 V;	P_9.1.2
Current consumption at V_{IO} Normal-operating mode	I_{IO}	–	–	1.5	mA	V_{NEN} = 0 V; V_{Diff} = 0 V; $V_{TxD} = V_{IO}$;	P_9.1.3
Current consumption at V_{CC} Power-save mode	$I_{CC(PSM)}$	–	–	5	µA	$V_{TxD} = V_{NEN} = V_{IO}$;	P_9.1.4
Current consumption at V_{IO} Power-save mode	$I_{IO(PSM)}$	–	5	14	µA	$V_{TxD} = V_{NEN} = V_{IO}$; 0 V $< V_{CC} <$ 5.5 V;	P_9.1.5
Current consumption at V_{CC} Forced-receive-only mode	$I_{CC(FROM)}$	–	–	1	mA	$V_{TxD} = V_{NEN}$ = 0 V; 0 V $< V_{CC} < V_{CC(UV,F)}$; V_{Diff} = 0 V;	P_9.1.10
Current consumption at V_{IO} Forced-receive-only mode	$I_{IO(FROM)}$	–	0.8	1.5	mA	$V_{TxD} = V_{NEN}$ = 0 V; 0 V $< V_{CC} < V_{CC(UV,F)}$; V_{Diff} = 0 V;	P_9.1.11
Supply resets							
V_{CC} undervoltage monitor rising edge	$V_{CC(UV,R)}$	3.8	4.35	4.5	V	–	P_9.1.12
V_{CC} undervoltage monitor falling edge	$V_{CC(UV,F)}$	3.8	4.25	4.5	V	–	P_9.1.13
V_{CC} undervoltage monitor hysteresis	$V_{CC(UV,H)}$	–	100	–	mV	1)	P_9.1.14
V_{IO} undervoltage monitor rising edge	$V_{IO(UV,R)}$	2.0	2.55	3.0	V	–	P_9.1.15
V_{IO} undervoltage monitor falling edge	$V_{IO(UV,F)}$	2.0	2.4	3.0	V	–	P_9.1.16
V_{IO} undervoltage monitor hysteresis	$V_{IO(UV,H)}$	–	150	–	mV	1)	P_9.1.17

Table 6 Electrical characteristics (cont'd)

4.5 V $< V_{CC} <$ 5.5 V; 3.0 V $< V_{IO} <$ 5.5 V; R_L = 60 Ω; -40 °C $< T_j <$ 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
V_{CC} undervoltage delay time	$t_{Delay(UV)\_F}$ $t_{Delay(UV)\_R}$	–	–	30 100	µs	[1] (see **Figure 9**);	P_9.1.18
V_{IO} delay time power-up	t_{PON}	–	–	280	µs	[1] (see **Figure 6**);	P_9.1.19
V_{IO} delay time power-down	t_{POFF}	–	–	100	µs	[1] (see **Figure 6**);	P_9.1.20
Receiver output RxD							
"High" level output current	$I_{RxD,H}$	–	-4	-1	mA	$V_{RxD} = V_{IO}$ - 0.4 V; $V_{Diff} <$ 0.5 V;	P_9.1.21
"Low" level output current	$I_{RxD,L}$	1	4	–	mA	V_{RxD} = 0.4 V; $V_{Diff} >$ 0.9 V;	P_9.1.22
Transmission input TxD							
"High" level input voltage threshold	$V_{TxD,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	recessive state;	P_9.1.26
"Low" level input voltage threshold	$V_{TxD,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	dominant state;	P_9.1.27
Input hysteresis	$V_{HYS(TxD)}$	–	200	–	mV	[1]	P_9.1.28
"High" level input current	$I_{TxD,H}$	-2	–	2	µA	$V_{TxD} = V_{IO}$;	P_9.1.29
"Low" level input current	$I_{TxD,L}$	-200	–	-20	µA	V_{TxD} = 0 V;	P_9.1.30
Input capacitance	C_{TxD}	–	–	10	pF	[1]	P_9.1.31
TxD permanent dominant time-out, optional	t_{TxD}	1	–	4	ms	Normal-operating mode;	P_9.1.32
non-enable input NEN							
"High" level input voltage threshold	$V_{NEN,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	Power-save mode;	P_9.1.36
"Low" level input voltage threshold	$V_{NEN,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	Normal-operating mode;	P_9.1.37
"High" level input current	$I_{NEN,H}$	-2	–	2	µA	$V_{NEN} = V_{IO}$;	P_9.1.38
"Low" level input current	$I_{NEN,L}$	-200	–	-20	µA	V_{NEN} = 0 V;	P_9.1.39
Input hysteresis	$V_{HYS(NEN)}$	–	200	–	mV	[1]	P_9.1.42
Input capacitance	$C_{(NEN)}$	–	–	10	pF	[1]	P_9.1.43
Bus receiver							
Differential range dominant Normal-operating mode	$V_{Diff\_D\_Range}$	0.9	–	8.0	V	-12 V ≤ V_{CMR} ≤ 12 V;	P_9.1.46
Differential range recessive Normal-operating mode	$V_{Diff\_R\_Range}$	-3.0	–	0.5	V	-12 V ≤ V_{CMR} ≤ 12 V;	P_9.1.48
Differential receiver hysteresis Normal-operating mode	$V_{Diff,hys}$		30		mV	[1]	P_9.1.49
Common mode range	*CMR*	-12	–	12	V	–	P_9.1.52

Table 6 Electrical characteristics (cont'd)

4.5 V $< V_{CC} <$ 5.5 V; 3.0 V $< V_{IO} <$ 5.5 V; R_L = 60 Ω; -40 °C $< T_j <$ 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Single ended internal resistance	R_{CAN_H}, R_{CAN_L}	6	–	50	kΩ	recessive state; -2 V ≤ V_{CANH} ≤ 7 V; -2 V ≤ V_{CANL} ≤ 7 V;	P_9.1.53
Differential internal resistance	R_{Diff}	12	–	100	kΩ	recessive state; -2 V ≤ V_{CANH} ≤ 7 V; -2 V ≤ V_{CANL} ≤ 7 V;	P_9.1.54
Input resistance deviation between CANH and CANL	ΔR_i	-3	–	3	%	[1] recessive state; V_{CANH} = V_{CANL} = 5 V;	P_9.1.55
Input capacitance CANH, CANL versus GND	C_{In}	–	20	40	pF	[2] recessive state	P_9.1.56
Differential input capacitance	C_{InDiff}	–	10	20	pF	[2] recessive state	P_9.1.57
Bus transmitter							
CANL, CANH recessive output voltage Normal-operating mode	$V_{CANL,H}$	2.0	2.5	3.0	V	V_{TxD} = V_{IO}; no load;	P_9.1.58
CANH, CANL recessive output voltage difference Normal-operating mode	$V_{Diff\_R\_NM}$ = V_{CANH} - V_{CANL}	-50	–	50	mV	V_{TxD} = V_{IO}; no load;	P_9.1.59
CANL dominant output voltage Normal-operating mode	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω; 4.75 V < V_{CC} < 5.25 V;	P_9.1.60
CANH dominant output voltage Normal-operating mode	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω; 4.75 V < V_{CC} < 5.25 V;	P_9.1.61
Differential voltage dominant Normal-operating mode V_{Diff} = V_{CANH} - V_{CANL}	$V_{Diff\_D\_NM}$	1.5	2.0	2.5	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω; 4.75 V < V_{CC} < 5.25 V;	P_9.1.62
Differential voltage dominant extended bus load Normal-operating mode	$V_{Diff\_EXT\_BL}$	1.4	2.0	3.3	V	V_{TxD} = 0 V; 45 Ω < R_L < 70 Ω; 4.75 V < V_{CC} < 5.25 V;	P_9.1.63
Differential voltage dominant high extended bus load Normal-operating mode	$V_{Diff\_HEXT\_BL}$	1.5	–	5.0	V	V_{TxD} = 0 V; R_L = 2240 Ω; 4.75 V < V_{CC} < 5.25 V; static behavior;[1]	P_9.1.64
Driver symmetry (V_{SYM} = V_{CANH} + V_{CANL})	V_{SYM}	0.9 × V_{CC}	1.0 × V_{CC}	1.1 × V_{CC}	V	[1] [3] C_1 = 4.7 nF;	P_9.1.67
CANL short circuit current	I_{CANLsc}	40	75	115	mA	$V_{CANLshort}$ = 18 V; $t < t_{TxD}$; V_{TxD} = 0 V;	P_9.1.68

Table 6 Electrical characteristics (cont'd)

4.5 V $< V_{CC} <$ 5.5 V; 3.0 V $< V_{IO} <$ 5.5 V; R_L = 60 Ω; -40 °C $< T_j <$ 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH short circuit current	I_{CANHsc}	-115	-75	-40	mA	$V_{CANHshort}$ = -3 V; $t < t_{TxD}$; V_{TxD} = 0 V;	P_9.1.70
Leakage current, CANH	$I_{CANH,lk}$	-5	–	5	µA	$V_{CC} = V_{IO}$ = 0 V; 0 V < $V_{CANH} \leq$ 5 V; $V_{CANH} = V_{CANL}$;	P_9.1.71
Leakage current, CANL	$I_{CANL,lk}$	-5	–	5	µA	$V_{CC} = V_{IO}$ = 0 V; 0 V < $V_{CANL} \leq$ 5 V; $V_{CANH} = V_{CANL}$;	P_9.1.72
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	–	–	70	V/µs	[1] 30 % to 70 % of measured differential bus voltage; C_2 = 100 pF; R_L = 60 Ω; 4.75 V < V_{CC} < 5.25 V;	P_9.1.190
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	–	–	70	V/µs	[1] 70 % to 30 % of measured differential bus voltage; C_2 = 100 pF; R_L = 60 Ω; 4.75 V < V_{CC} < 5.25 V;	P_9.1.191
Dynamic CAN-transceiver characteristics							
Propagation delay TxD-to-RxD	t_{Loop}	80	–	215	ns	C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 15 pF; (see **Figure 13**)	P_9.1.73
Propagation delay increased load TxD-to-RxD	t_{Loop_150}	80	–	330	ns	[1] C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 15 pF; R_L = 150 Ω;	P_9.1.74
Delay Times							
Delay time for mode change	t_{Mode}	–	–	20	µs	[1]	P_9.1.79
CAN FD characteristics							
Received recessive bit width at 2 MBit/s	$t_{Bit(RxD)\_2M}$	400	500	550	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 500 ns; (see **Figure 14**);	P_9.1.84
Received recessive bit width at 5 MBit/s	$t_{Bit(RxD)\_5M}$	120	200	220	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 200 ns; (see **Figure 14**);	P_9.1.85

Table 6 Electrical characteristics (cont'd)

4.5 V $< V_{CC} <$ 5.5 V; 3.0 V $< V_{IO} <$ 5.5 V; R_L = 60 Ω; -40 °C $< T_j <$ 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmitted recessive bit width at 2 MBit/s	$t_{Bit(Bus)\_2M}$	435	500	530	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 500 ns; (see **Figure 14**);	P_9.1.86
Transmitted recessive bit width at 5 MBit/s	$t_{Bit(Bus)\_5M}$	155	200	210	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 200 ns; (see **Figure 14**);	P_9.1.87
Receiver timing symmetry at 2 MBit/s $\Delta t_{Rec\_2M} = t_{Bit(RxD)\_2M} - t_{Bit(Bus)\_2M}$	Δt_{Rec_2M}	-65	–	40	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 500 ns; (see **Figure 14**);	P_9.1.88
Receiver timing symmetry at 5 MBit/s $\Delta t_{Rec\_5M} = t_{Bit(RxD)\_5M} - t_{Bit(Bus)\_5M}$	Δt_{Rec_5M}	-45	–	15	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 200 ns; (see **Figure 14**);	P_9.1.89

1) Not subject to production test, specified by design
2) Not subject to production test, specified by design, S2P-Method; f = 10 MHz
3) VSYM shall be observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TxD is stimulated by a square wave signal with a frequency of 1 MHz.

9.2 Diagrams

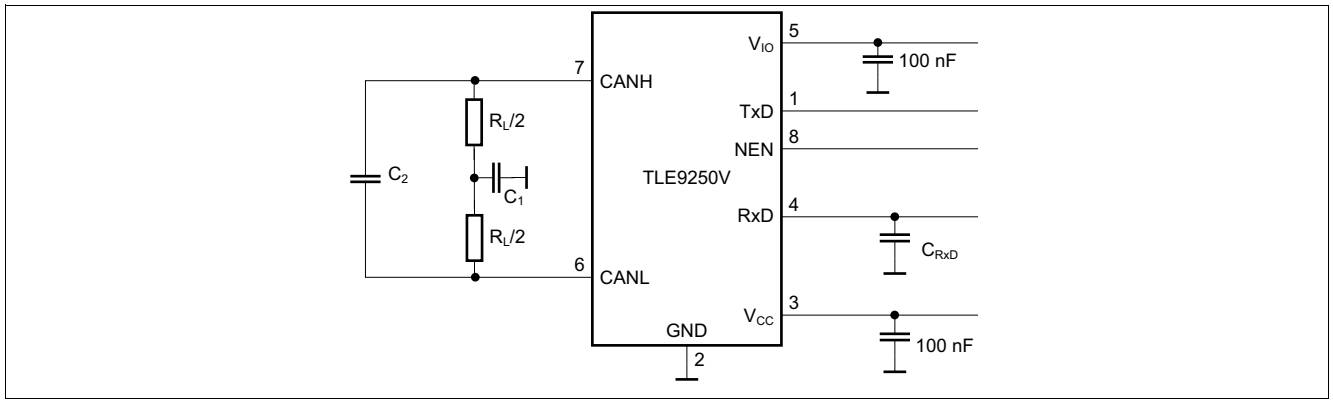

Figure 12 Test circuit for dynamic characteristics

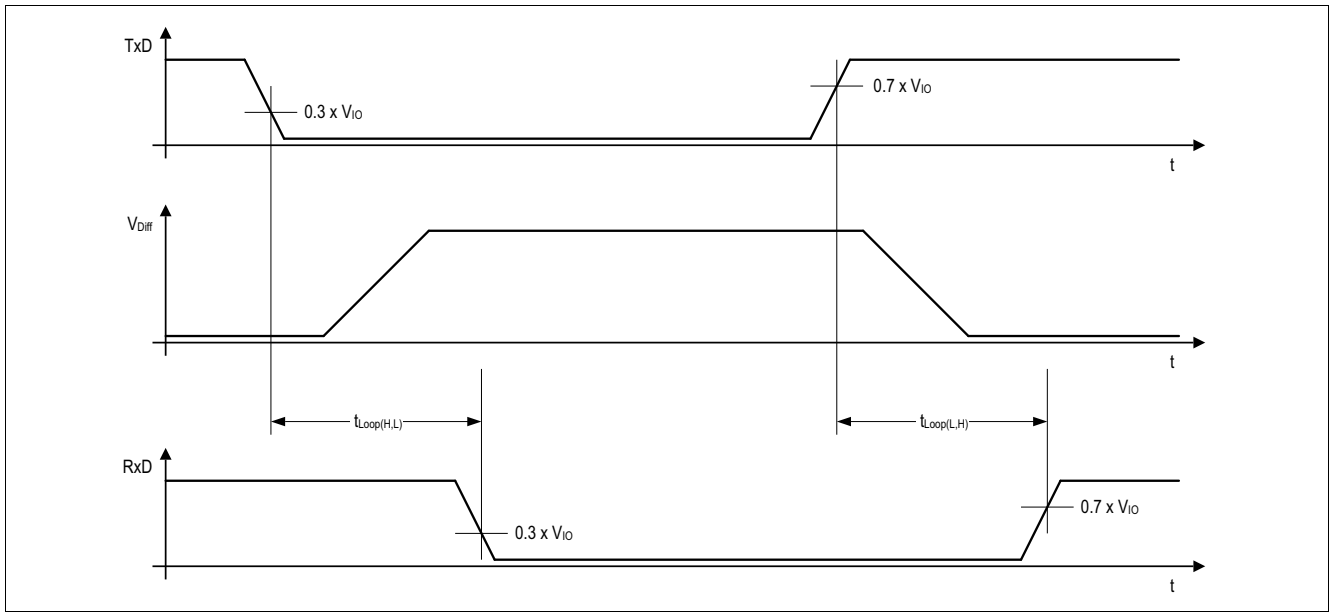

Figure 13 Timing diagrams for dynamic characteristics

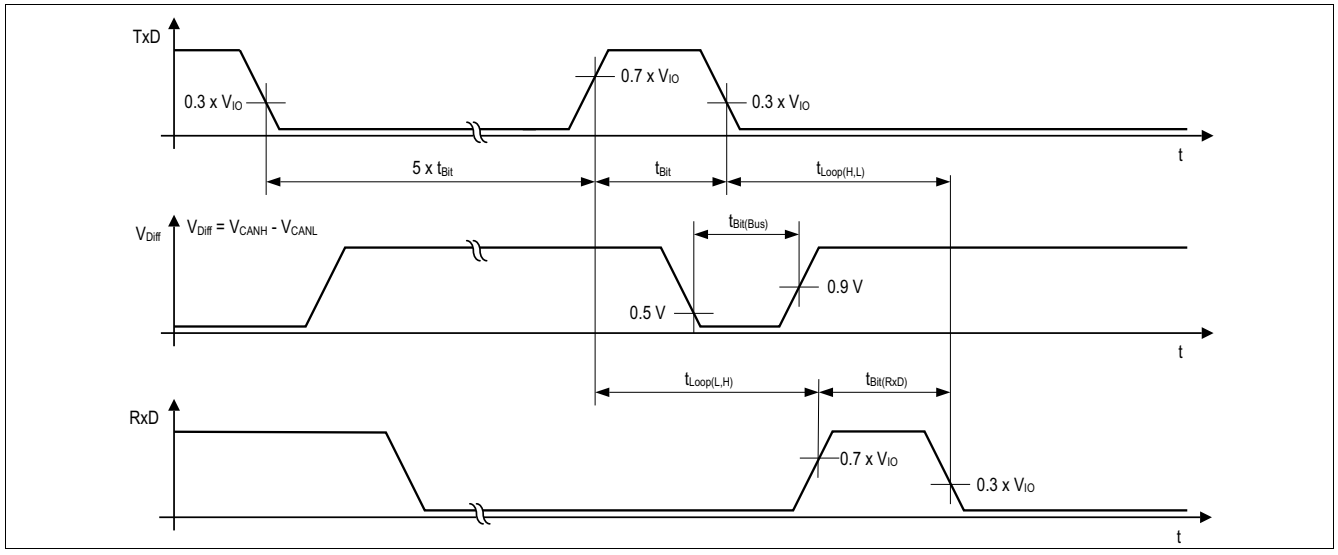

Figure 14 Recessive bit time for five dominant bits followed by one recessive bit

10 Application information

10.1 ESD robustness according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 7 ESD robustness according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus GND	≥ +11	kV	[1)]Positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	≤ -11	kV	[1)]Negative pulse

1) Not subject to production test. ESD susceptibility “ESD GUN” according to GIFT / ICT paper: “EMC Evaluation of CAN Transceivers, version IEC TS62228”, section 4.3. (DIN EN61000-4-2)
Tested by external test facility (IBEE Zwickau, EMC test report Nr. 01-07-2017 and Nr. 06-08-17)

10.2 Application example

10.3 Voltage adaption to the microcontroller supply

To adapt the digital input and output levels of the TLE9250V to the I/O levels of the microcontroller, connect the power supply pin V_{IO} to the microcontroller voltage supply (see **Figure 60**).

Note: In case no dedicated digital supply voltage V_{IO} is required in the application, connect the digital supply voltage V_{IO} to the transmitter supply V_{CC}.

10.4 Further application information

- For further information you may visit: **http://www.infineon.com/automotive-transceiver**

11 Package outline

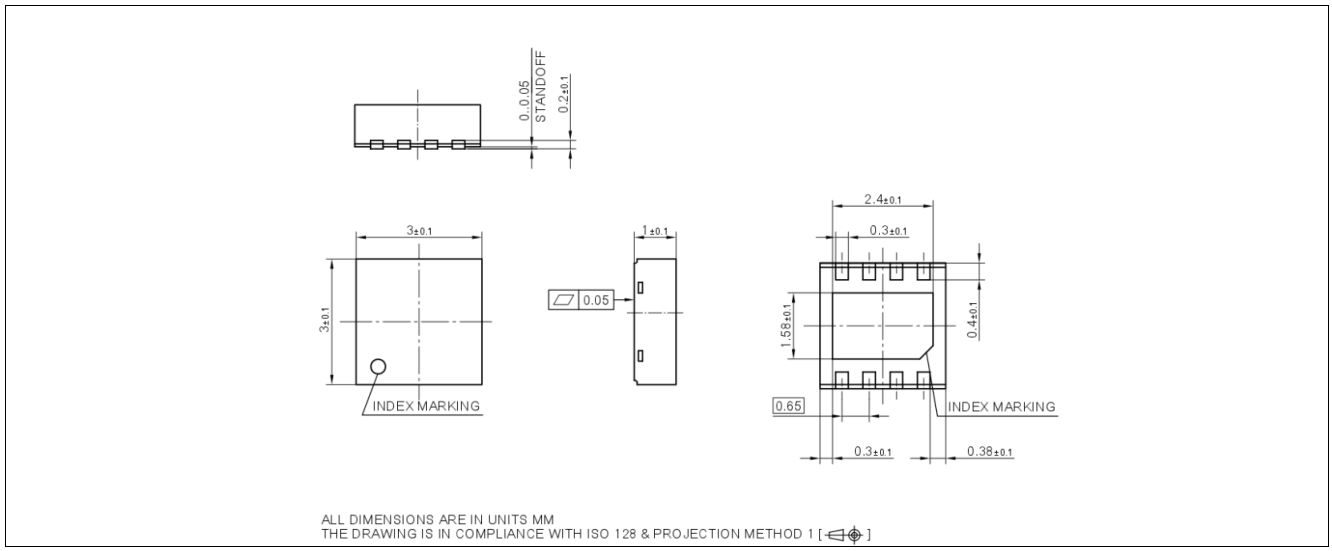

Figure 15 PG-TSON-8 (Plastic Thin Small Outline Nonleaded)

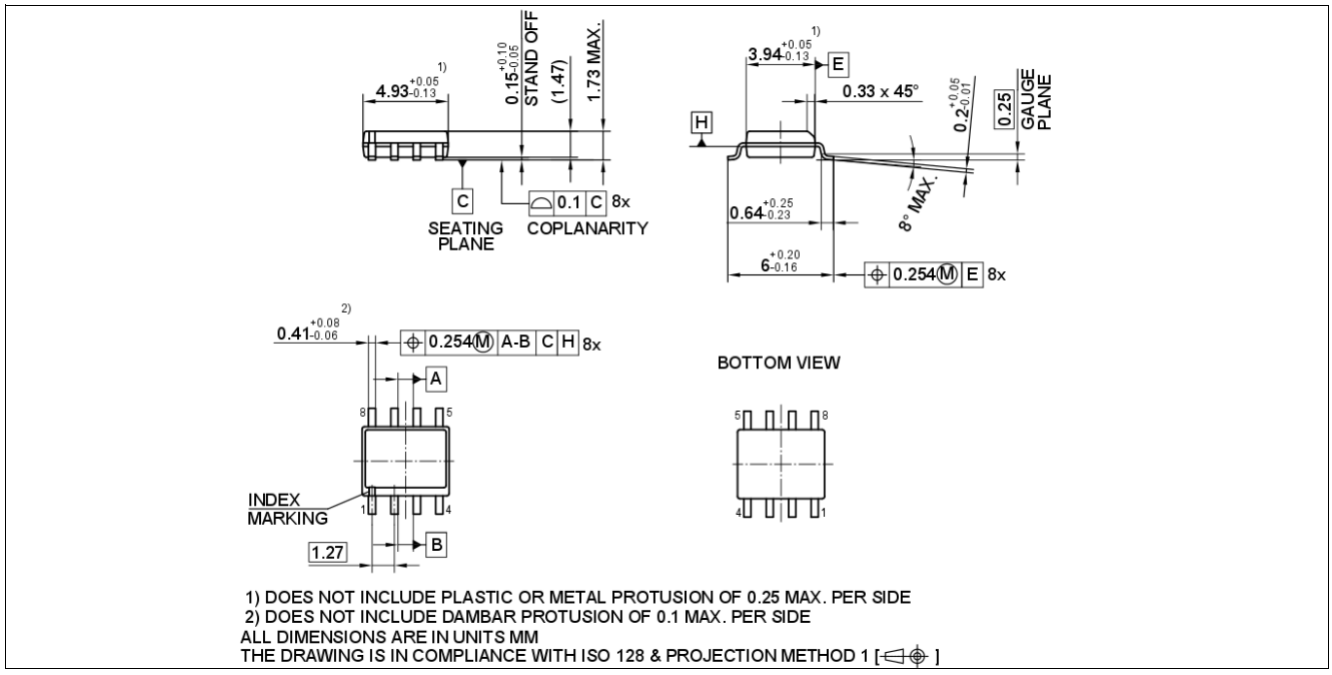

Figure 16 PG-DSO-8 (Plastic Dual Small Outline)

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

12 Revision history

Revision	Date	Changes
1.11	2019-09-19	Datasheet updated: • Editorial changes • Updated bus transmitter table – added P_9.1.190 and P_ 9.1.191 (no product change) – tightened P_9.1.59 and P_9.1.62 – tightened P_9.1.56 and P_9.1.57 by additional footnote • Updated dynamic CAN-transceiver characteristics table – tightened P_9.1.73
1.1	2018-05-23	Datasheet updated: • I_{CC_D} max. lowered from 60mA to 48mA (see **P_9.1.2**) • $I_{IO\_(PSM)}$ max. lowered from 15µA to 14µA (see **P_9.1.5**) • Extended temperature condition T_J < 150°C and reduced typical value from 7µA to 5µA (see **P_9.1.5**) • $t_{Delay(UV)}$ divided in $t_{Delay(UV)\_F}$ (max. 30µs) and $t_{Delay(UV)\_R}$ (max. 100µs)(see **P_9.1.18** and **Figure 9**) • Corrected description for NEN pin in **Table 5** • Removed description of bus wake-up capability in **Chapter 5** • Updated **Figure 13**. Removed unspecified parameters $t_{d(L),T}$, $t_{d(L),R}$, $t_{d(H),T}$, $t_{d(H),R}$. • Editorial Changes
1.0	2017-09-14	Datasheet created

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