

# TLE9255W

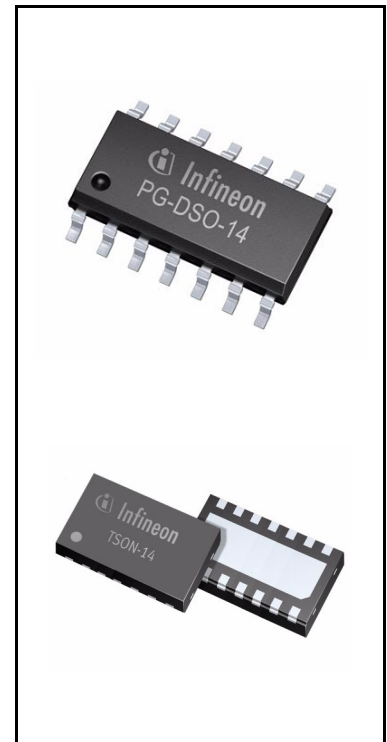
## HS CAN Transceiver with Partial Networking



### 1 Overview

#### Features

- Fully compliant to ISO 11898-2 (2016)
- HS CAN standard data rates up to 1MBit/s
- CAN FD data rates up to 5 MBit/s
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME)
- Excellent ESD robustness,  $\pm 10$  kV according to IEC 61000-4-2
- Independent supply concept on  $V_{CC}$  and  $V_{BAT}$  pins
- Fail safe features
  - TxD-timeout
  - overtemperature shutdown
  - overtemperature warning
- Extended supply range on  $V_{CC}$  and  $V_{IO}$  supply
- CAN short circuit proof to ground, battery and  $V_{CC}$
- Overtemperature protection
- Advanced bus biasing according to ISO 11898-2 (2016)
- Wake filter time  $0.5\mu\text{s} < t_{\text{Filter}} < 1.8\mu\text{s}$  meeting worldwide OEM requirements
- Wake-up pattern (WUP) detection in all low-power modes
- Wake-up frame (WUF) detection according to ISO 11898-2 (2016)
- Wake-up frame detection with CAN FD tolerant feature
- Local wake-up input
- SPI clock frequency up to 4 MHz
- Green Product (RoHS compliant)



#### Potential applications

- HS CAN networks in automotive applications
- HS CAN networks in industrial applications

#### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Overview

### Description

As an interface between the physical bus layer and the CAN protocol controller, the TLE9255W drives the signals to the bus and protects the microcontroller from interference generated within the network. Based on the high symmetry of the CANH and CANL signals, the TLE9255W provides a very low level of electromagnetic emission within a wide frequency range, allowing the operation of the TLE9255W without a common mode choke in automotive and industrial applications.

The TLE9255W is enclosed in an RoHS compliant PG-DSO-14 or PG-TSON-14 package and fulfills the requirements of the ISO11898-2 (2016).

The TLE9255W is part of the Infineon standard HS CAN transceiver family and provides beside CAN partial networking functions also a CAN FD capability up to 5 MBit/s in HS CAN networks. Configured as a partial networking HS CAN transceiver the TLE9255W can drive and receive CAN FD messages. It can also be used to block the payload of CAN FD messages. This CAN FD tolerant feature allows the usage of microcontrollers in CAN FD networks, which are not CAN FD capable.

The SPI of TLE9255W controls the setup of the wake-up messages and the status message generated by the internal state machine. Most of the functions, including wake-up functions, INH output control, mode control, undervoltage control are configurable by the SPI. This allows a very flexible usage of the TLE9255W in different applications.

The two non-low power modes (Normal-operating Mode and Receive-only Mode) and the two low power modes (Sleep Mode and Stand-by Mode) provide minimum current consumption based on the required functionality.

In Sleep Mode the TLE9255W can detect a wake-up pattern (WUP) on the HS CAN and then change the mode of operation accordingly; even at a quiescent current below 26  $\mu$ A over the full temperature range.

In Selective-wake Sub-mode the TLE9255W monitors the CAN messages on the HS CAN bus. If the TLE9255W detects a matching wake-up frame, then it triggers a mode change. The TLE9255W monitors wake-up identifiers up to 29 bit as well as up to 64 bit wide data. The internal protocol handler counts all bus errors. The SPI indicates failures, error counter overflow and synchronization failures to the microcontroller.

The unique power-supply management allows the application to use the TLE9255W without the battery supply  $V_{BAT}$  connected. In this case the TLE9255W is supplied over the  $V_{CC}$  pin. The  $V_{IO}$  voltage reference supports 3.3 V and 5 V supplied microcontrollers.

Based on Infineon Smart Power Technology (SPT), the TLE9255W provides excellent immunity together with a very high electromagnetic immunity (EMI). The TLE9255W and the Infineon SPT are AEC qualified and tailored to withstand the harsh conditions of the automotive environment.

Type	Package	Marking
TLE9255WSK	PG-DSO-14	9255W
TLE9255WLC	PG-TSON-14	9255W

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Block Diagram

2 Block Diagram

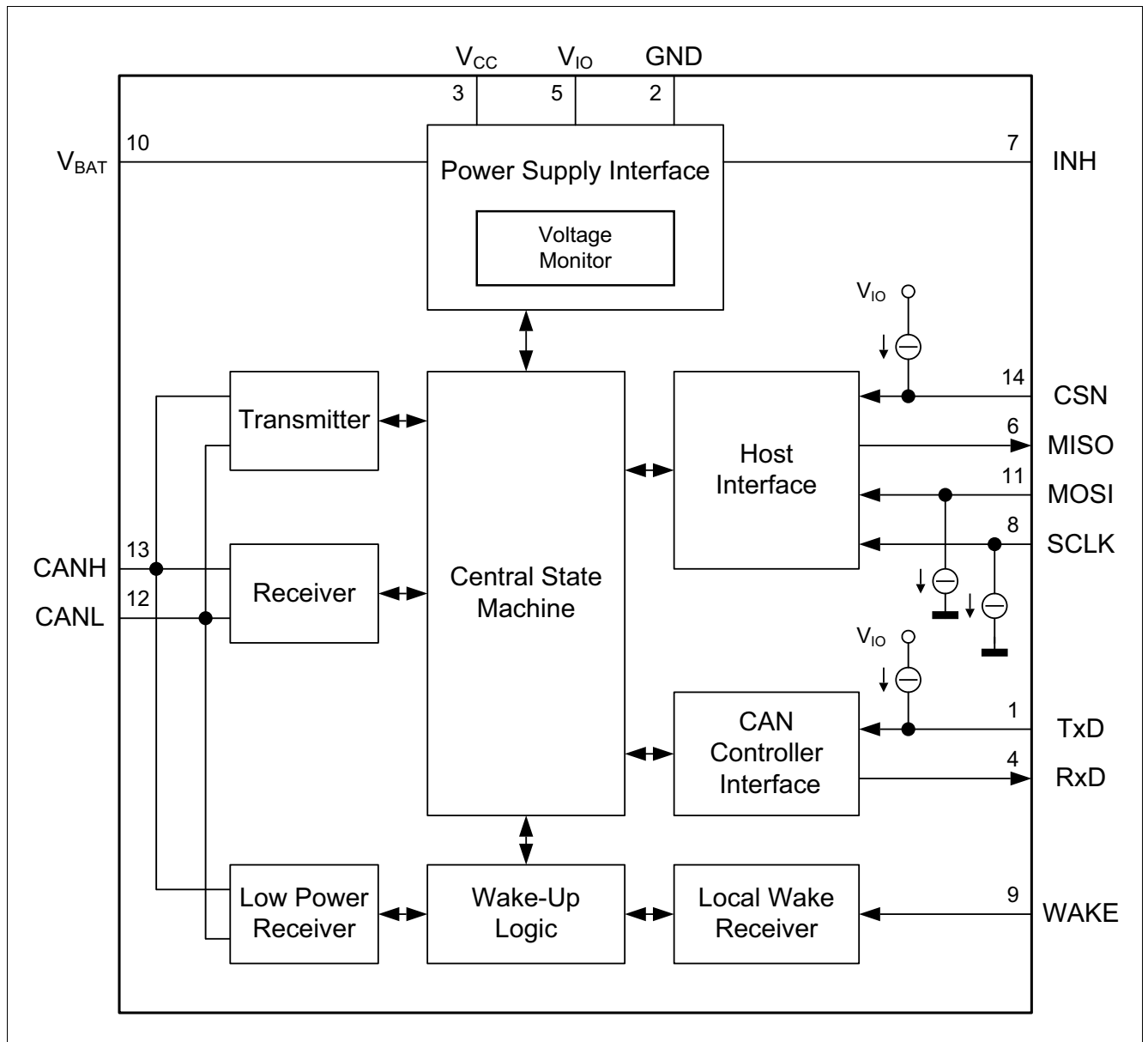


Figure 1 Block Diagram

Pin Configuration

### 3 Pin Configuration

#### 3.1 Pin Assignment

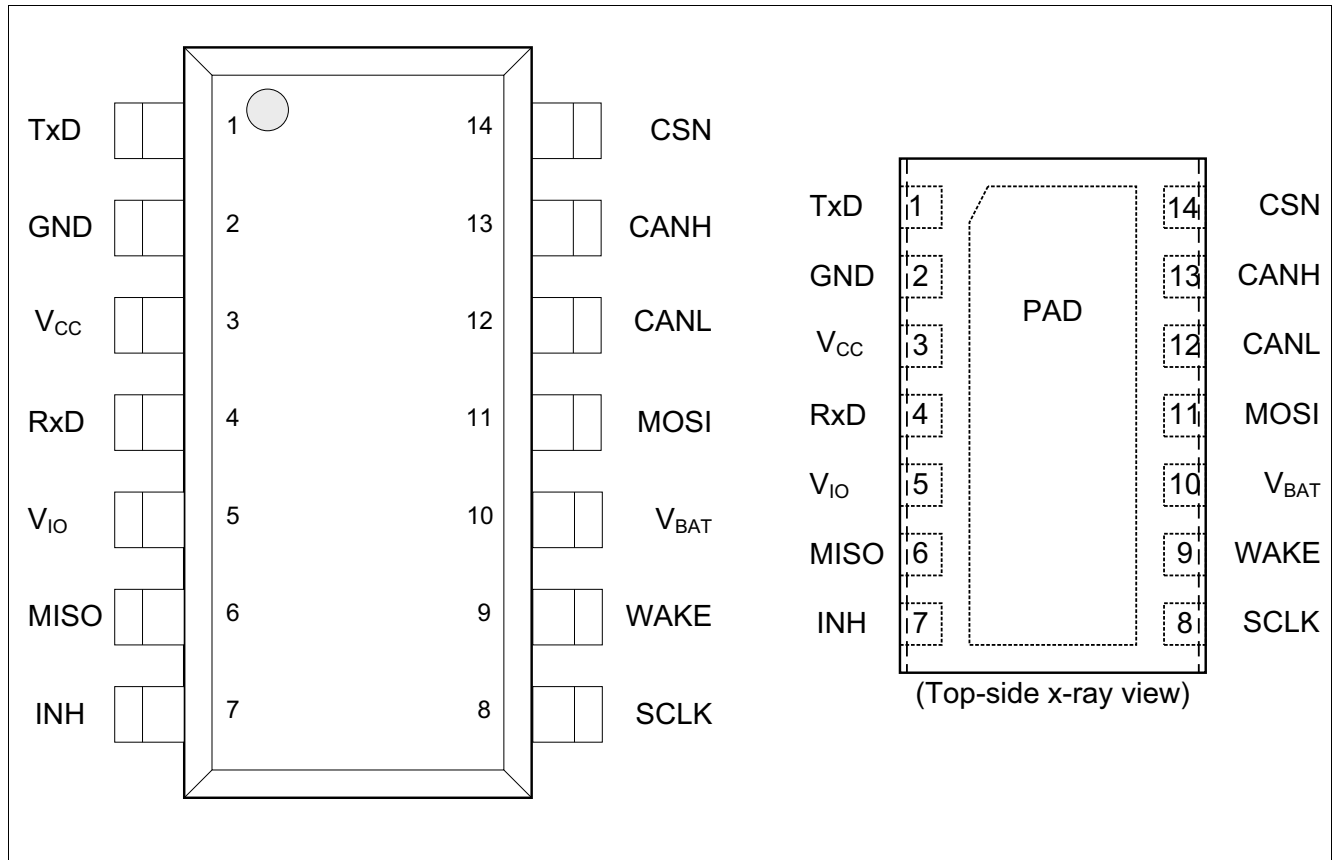


Figure 2 Pin configuration for PG-DSO-14 and PG-TSON-14

#### 3.2 Pin Definitions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	TxD	<b>Transmit Data Input;</b> integrated pull-up current source to $V_{IO}$ , "low" to drive a dominant signal on CANH and CANL
2	GND	<b>Ground.</b>
3	$V_{CC}$	<b>Transmitter Supply Voltage;</b> 100 nF decoupling capacitor to GND is recommended

## Pin Configuration

**Table 1 Pin definitions and functions (cont'd)**

Pin	Symbol	Function
4	RxD	<b>Receive Data Output;</b> “low” while a dominant signal is on the HS CAN bus, output voltage adapted to the voltage on the $V_{IO}$ level shift input
5	$V_{IO}$	<b>Level Shift Input;</b> reference voltage for the digital input and output pins, 100 nF decoupling capacitor to GND is recommended
6	MISO	<b>SPI Serial Data Output;</b> tri-state while CSN is “high”
7	INH	<b>Inhibit Output;</b> open drain output to control external circuitry
8	SCLK	<b>SPI Clock Input;</b> integrated pull-down current source to GND
9	WAKE	<b>Wake-up Input;</b> local wake-up input, terminated against GND and $V_{BAT}$ , wake-up input sensitive to signal changes in both directions
10	$V_{BAT}$	<b>Battery Supply Voltage;</b> 100 nF decoupling capacitor to GND is recommended
11	MOSI	<b>SPI Serial Data Input;</b> integrated pull-down current source to GND
12	CANL	<b>Low-level HS CAN Bus Line</b>
13	CANH	<b>High-level HS CAN Bus Line</b>
14	CSN	<b>SPI Chip Select Not Input;</b> integrated pull-up current source to $V_{IO}$
PAD	-	Connect to PCB heat sink area. Do not connect to other potential than GND.



High Speed CAN Functional Description

### 4 High Speed CAN Functional Description

High speed CAN (HS CAN) is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. ISO 11898-2 (2016) describes the use of the Controller Area Network (CAN) within road vehicles. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The CAN transceiver is part of the physical layer. The physical layer specification of a CAN bus system includes all electrical specifications of a CAN network.

The TLE9255W supports:

- standard bus wake-up functionality
- CAN Partial Networking with selective wake-up functionality according to ISO 11898-2 (2016)
- CAN Flexible data rate (CAN FD) transmission up to 5 MBit/s

#### 4.1 High Speed CAN Physical Layer

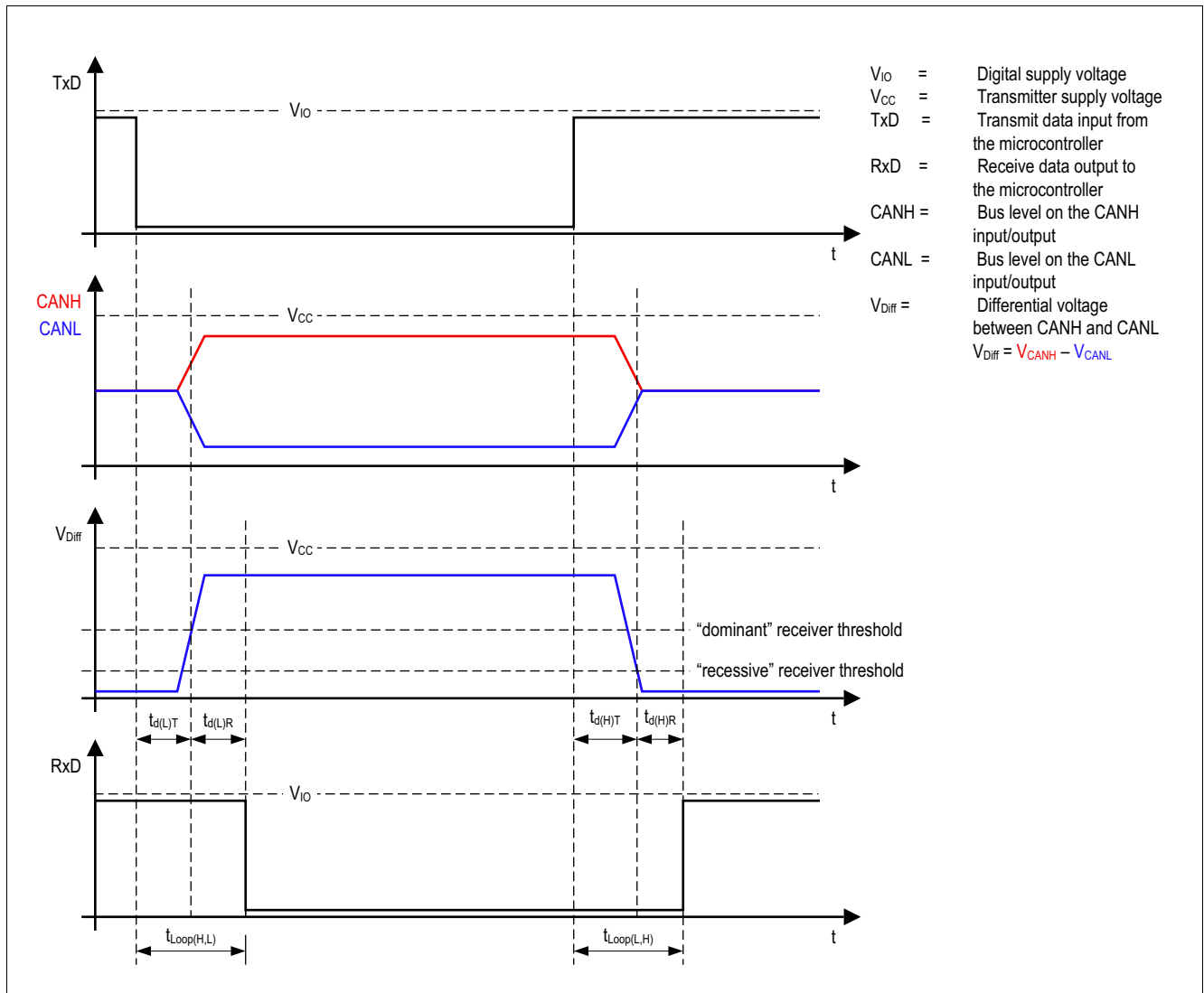


Figure 3 High speed CAN bus signals and logic signals

## High Speed CAN Functional Description

The TLE9255W is a HS CAN transceiver operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential network which allows data transmission rates up to 5 MBit/s. HS CAN networks have two signal states on the CAN bus (see [Figure 3](#)):

- dominant
- recessive

The CANH and CANL pins are the interface to the CAN bus and operate both as an input and as an output. The RxD and TxD pins are the interface to the microcontroller. The TxD pin is the serial data input from the CAN controller. The RxD pin is the serial data output to the CAN controller. The HS CAN transceiver TLE9255W includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitoring the data from the bus medium at the same time (see [Figure 1](#)). The TLE9255W converts the serial data stream, which is available on the transmit data input TxD, to a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the TLE9255W monitors the data on the CAN bus and converts it to a serial, single-ended signal on the RxD output pin. A “low” signal on the TxD pin creates a dominant signal on the CAN bus, followed by a “low” signal on the RxD pin (see [Figure 3](#)). The feature of broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within CAN networks.

ISO 11898-2 (2016) defines the voltage levels for HS CAN transceivers. Whether a data bit is dominant or recessive depends on the voltage difference between the CANH and CANL pins:

$$V_{\text{Diff}} = V_{\text{CANH}} - V_{\text{CANL}}$$

To transmit a dominant signal to the CAN bus the amplitude of the differential signal  $V_{\text{Diff}}$  is  $\geq 1.5$  V. To receive a recessive signal from the CAN bus the amplitude of the differential  $V_{\text{Diff}}$  is  $\leq 0.5$  V.

Partially supplied High-Speed CAN networks have CAN bus nodes with different power supply conditions. Some nodes are connected to the common power supply, while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus subscriber is supplied or not, each subscriber connected to the common bus media must not interfere with the communication. The TLE9255W is designed to support Partially supplied networks. In power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

For permanently supplied ECUs, the TLE9255W provides low power modes. In these low power modes, the current consumption of the TLE9255W is optimized to a minimum, while the TLE9255W can still recognize wake-up patterns or wake-up frames on the CAN bus and signal the wake-up event to the external microcontroller.

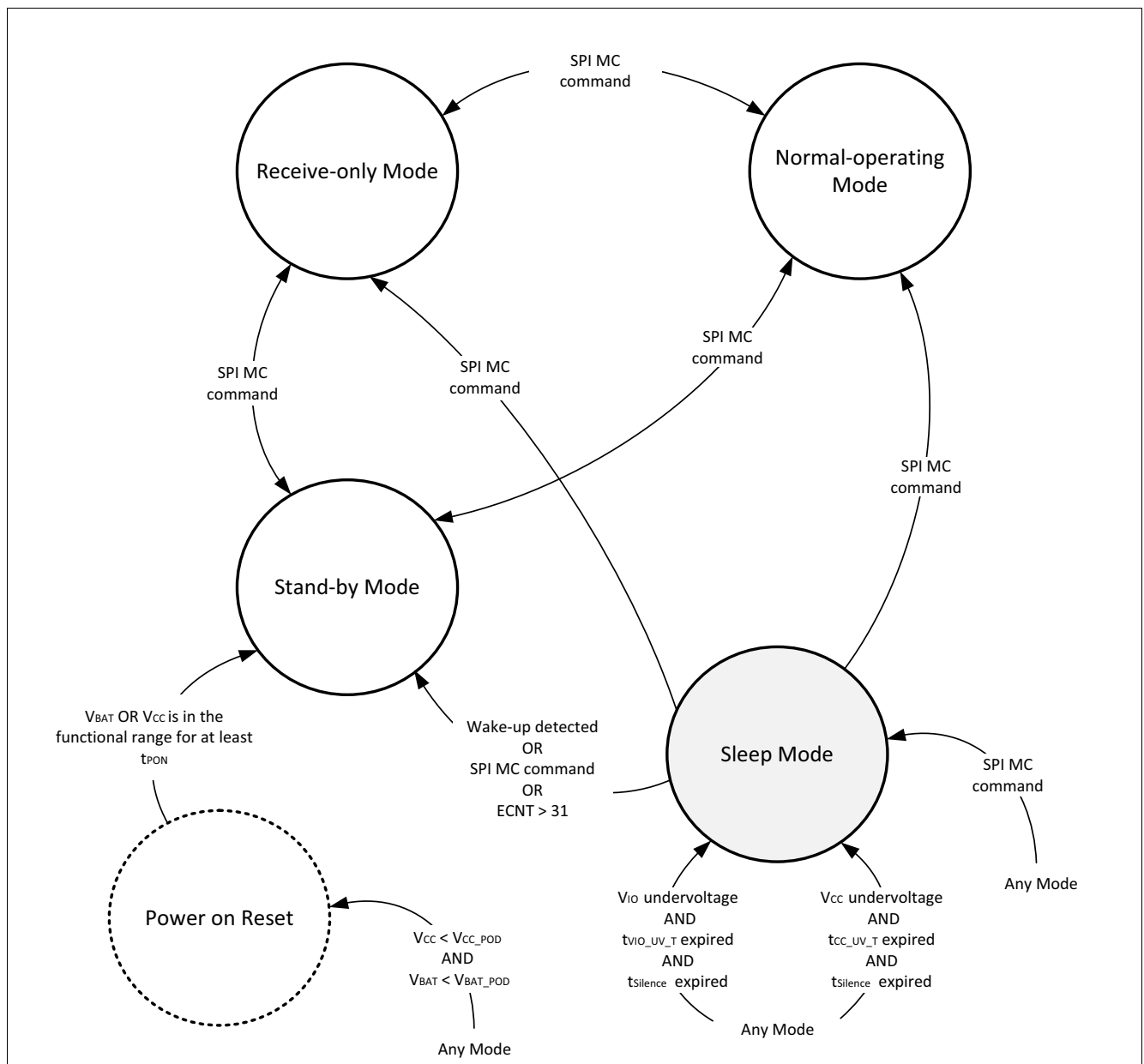
The voltage level on the digital input TxD and the digital output RxD is determined by the reference supply level at the  $V_{\text{IO}}$  pin. Depending on the voltage level at the  $V_{\text{IO}}$  pin, the signal levels on the logic pins (CSN, SCLK, MOSI, MISO, TxD and RxD) are compatible to microcontrollers having a 5 V or 3.3 V I/O supply. It is highly recommended that the digital power supply of  $V_{\text{IO}}$  of the transceiver is connected to the I/O power supply of the microcontroller; this is the way it is intended to be used (see [Figure 53](#)).

Modes of Operation

### 5 Modes of Operation

The TLE9255W supports four different Modes of operation (see **Figure 4**):

- Normal-operating Mode (**Chapter 5.1**)
- Receive-only Mode (**Chapter 5.2**)
- Stand-by Mode (**Chapter 5.3**)
- Sleep Mode (**Chapter 5.4**)



**Figure 4** Mode of operation

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**Modes of Operation**
**Table 2 Types of Modes and Sub-Modes**

<b>Type of mode</b>	<b>Mode</b>	<b>Sub-Mode</b>
Normal power mode	Normal-operating mode	–
	Receive-only Mode	–
Low power mode	Stand-by Mode	–
	Sleep Mode	Sleep WUP Sub-Mode
		Selective Wake Sub-Mode
Selective Sleep Sub-Mode		

## Modes of Operation

### 5.1 Normal-operating Mode

In Normal-operating mode all functions of the TLE9255W are available. The TLE9255W can receive data from the HS CAN bus as well as transmit data to the HS CAN bus.

- The transmitter is active and drives the serial data stream on the TxD input pin to the bus pins CANH, CANL.
- The normal mode receiver is active and converts the signals from the bus to a serial data stream on the RxD output pin.
- The bus biasing is on.
- The TxD timeout function is enabled ([Chapter 6.4](#)).
- The overtemperature protection is enabled ([Chapter 6.5](#)).
- The undervoltage detection on  $V_{BAT}$  is enabled ([Chapter 6.2.1](#)).
- The undervoltage detection on  $V_{CC}$  is enabled ([Chapter 6.2.2](#)).
- The undervoltage detection on  $V_{IO}$  is enabled ([Chapter 6.2.4](#)).
- The INH output pin is “high”.
- A valid wake-up pattern is not signalled in the SPI bit **WUP** ([Chapter 5.7.1](#)).
- Only if the selective wake function is enabled (**SWK\_EN** = 1), then the HS CAN bus will be continuously monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is disabled ([Chapter 5.7.3](#)).

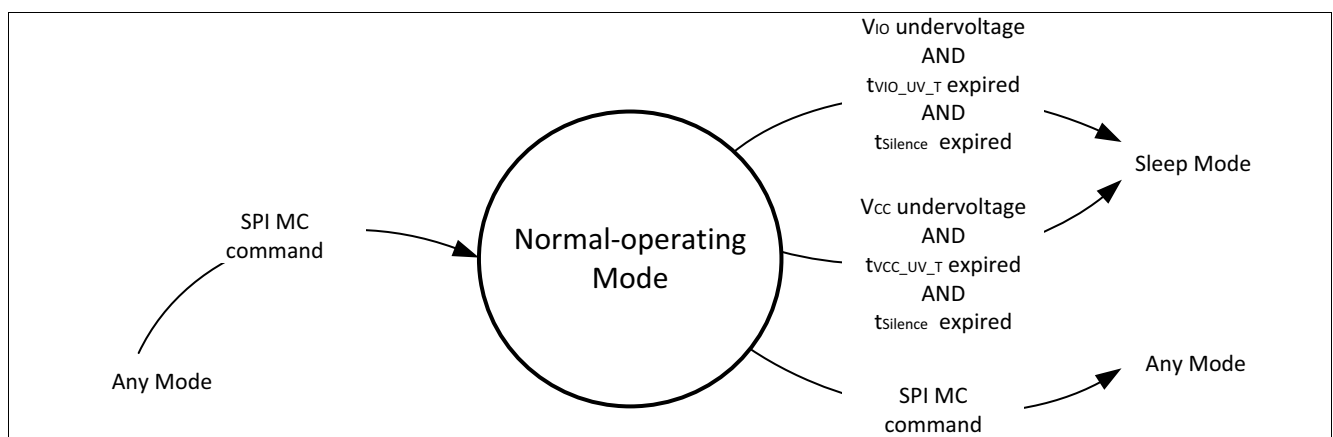
Conditions for entering the Normal-operating Mode:

- Normal-operating Mode can be entered via an SPI MC command from any mode of operation.

Conditions for leaving the Normal-operating Mode:

- If  $V_{IO} < V_{IO\_UV}$  AND  $t_{VIO\_UV\_T}$  has expired AND  $t_{silence}$  has expired, then this triggers a mode change to Sleep Mode
- If  $V_{CC} < V_{CC\_UV}$  AND  $t_{VCC\_UV\_T}$  has expired AND  $t_{silence}$  has expired, then this triggers a mode change to Sleep Mode.
- An SPI MC command triggers a mode change.

**Figure 5** shows possible mode changes.



**Figure 5** Mode changes in Normal-operating Mode

## Modes of Operation

### 5.2 Receive-only Mode

In Receive-only Mode the transmitter is disabled and the receiver is enabled. The TLE9255W can receive data from the HS CAN bus, but cannot transmit data to the HS CAN bus.

- The transmitter is disabled and the data available on the TxD input is blocked.
- The RxD output pin indicates the data received by the normal-mode receiver.
- The bus biasing is on.
- The TxD timeout function is disabled ([Chapter 6.4](#)).
- The overtemperature protection is disabled ([Chapter 6.5](#)).
- The undervoltage detection on  $V_{BAT}$  is enabled ([Chapter 6.2.1](#)).
- The undervoltage detection on  $V_{CC}$  is enabled ([Chapter 6.2.2](#)).
- The undervoltage detection on  $V_{IO}$  is enabled ([Chapter 6.2.4](#)).
- The INH output pin is “high”.
- A valid wake-up pattern is not signalled in the SPI bit **WUP** ([Chapter 5.7.1](#)).
- Only if the selective wake function is enabled (**SWK\_EN** = 1), then the HS CAN bus is continuously monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is disabled ([Chapter 5.7.3](#)).

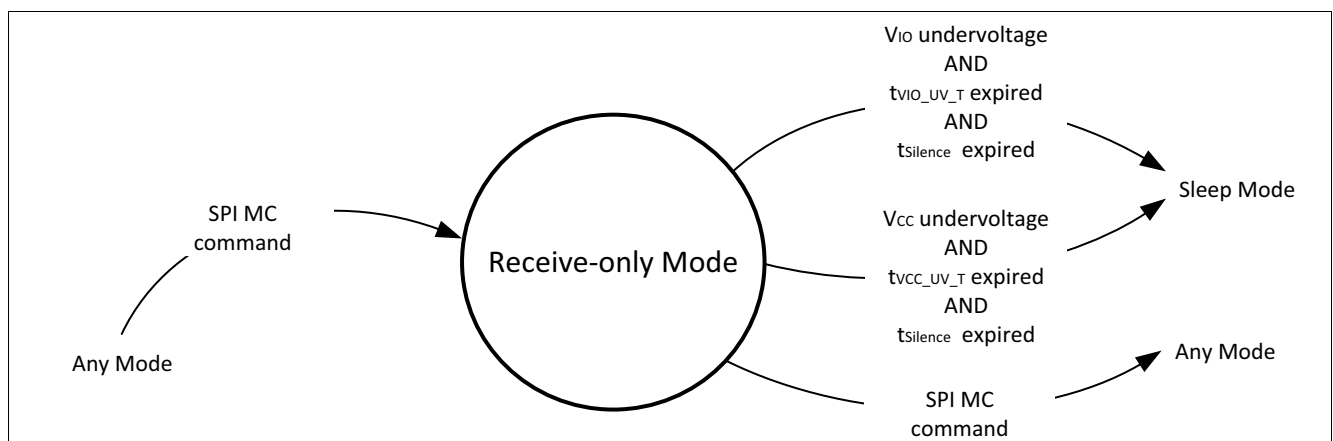
Conditions for entering the Receive-only Mode:

- Receive-only Mode can be entered via an SPI MC command from any mode of operation.

Conditions for leaving the Received-only Mode:

- If  $V_{IO} < V_{IO\_UV}$  AND  $t_{VIO\_UV\_T}$  has expired AND  $t_{silence}$  has expired, then this triggers a mode change to Sleep Mode.
- If  $V_{CC} < V_{CC\_UV}$  AND  $t_{VCC\_UV\_T}$  has expired AND  $t_{silence}$  has expired, then this triggers a mode change to Sleep Mode.
- An SPI MC command triggers a mode change.

**Figure 6** shows possible mode changes.



**Figure 6** Mode changes in Receive-only Mode

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## Modes of Operation

### 5.3 Stand-by Mode

Stand-by Mode is a low power mode of the TLE9255W with both the transmitter and the receiver disabled. In Stand-by Mode the transceiver can neither send data to the HS CAN bus nor can it receive data from the HS CAN bus:

- The transmitter is disabled and the data available on the TxD input is blocked.
- The RxD output pin indicates a wake-up event ([Chapter 5.8](#)). If no wake-up event is pending, then the default value of the RxD output pin is “high”.
- After Power on Reset the bus biasing is off. [Chapter 5.6](#) describes the conditions for the bus biasing.
- The TxD timeout function is disabled ([Chapter 6.4](#)).
- The overtemperature protection is disabled ([Chapter 6.5](#)).
- The undervoltage detection on  $V_{BAT}$  is enabled([Chapter 6.2.1](#))
- The undervoltage detection on  $V_{CC}$  is enabled ([Chapter 6.2.2](#)).
- The undervoltage detection on  $V_{IO}$  is enabled ([Chapter 6.2.4](#)).
- The INH output pin is “high”.
- If the selective wake function is disabled ( $SWK\_EN = 0$ ), then the HS CAN bus is continuously monitored for a valid wake-up pattern ([Chapter 5.7.1](#)). If the selective wake function is enabled, then a valid wake-up pattern is not signalled in the SPI bit **WUP**.
- Only if the selective wake function is enabled ( $SWK\_EN = 1$ ), then the HS CAN bus is continuously monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is enabled ([Chapter 5.7.3](#)).
- If  $V_{IO} > V_{IO\_UV}$ , then a mode change is possible.

## Modes of Operation

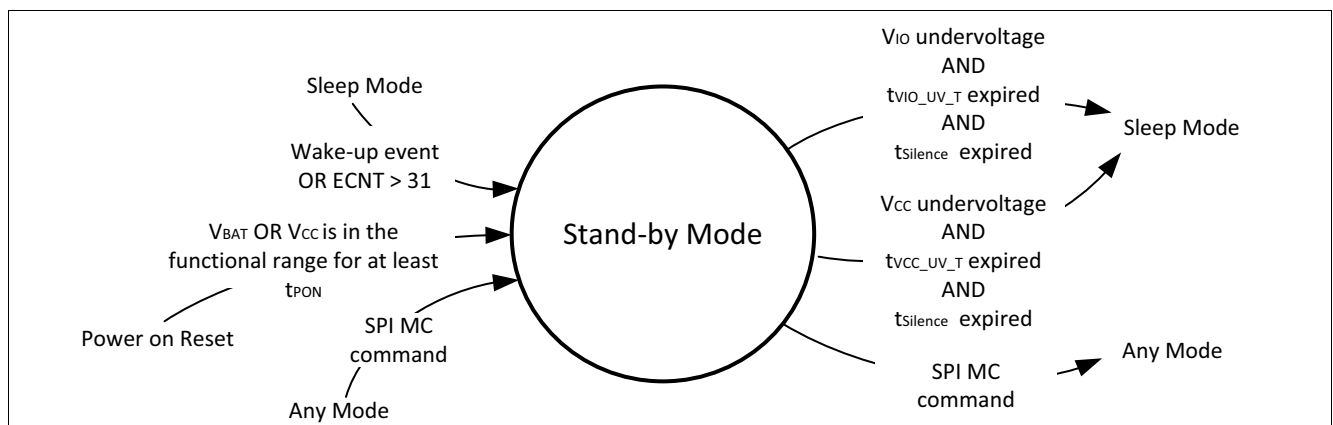
Conditions for entering the Stand-by Mode:

- After Power on Reset: If  $V_{CC}$  OR  $V_{BAT}$  is within the functional range for at least  $t_{PON}$ , then the TLE9255W enters Stand-by Mode.
- If a wake-up (WUP, WUF, LWU) is detected in Sleep Mode, then the TLE9255W enters Stand-by Mode.
- If the selective wake unit is active (Selective wake Sub-Mode) AND if the value of the error counter is 32 (see [Chapter 7.3](#)), then the TLE9255W enters Stand-by Mode.
- Stand-by Mode can be entered via an SPI MC command from any mode of operation.

Conditions for leaving the Stand-by Mode:

- If  $V_{IO} < V_{IO\_UV}$  AND  $t_{VIO\_UV\_T}$  has expired AND  $t_{silence}$  has expired, then this triggers a mode change to Sleep Mode.
- If  $V_{CC} < V_{CC\_UV}$  AND  $t_{VCC\_UV\_T}$  has expired AND  $t_{silence}$  has expired, then this triggers a mode change to Sleep Mode.
- An SPI MC command triggers a mode change.

**Figure 7** shows possible mode changes.



**Figure 7** Mode changes in Stand-by Mode



Modes of Operation

5.4 Sleep Mode

Sleep mode is a low power mode with minimized quiescent current. If the TLE9255W detects a wake-up event in Sleep Mode, then it changes to Stand-by Mode. Sleep Mode has three Sub-Modes.

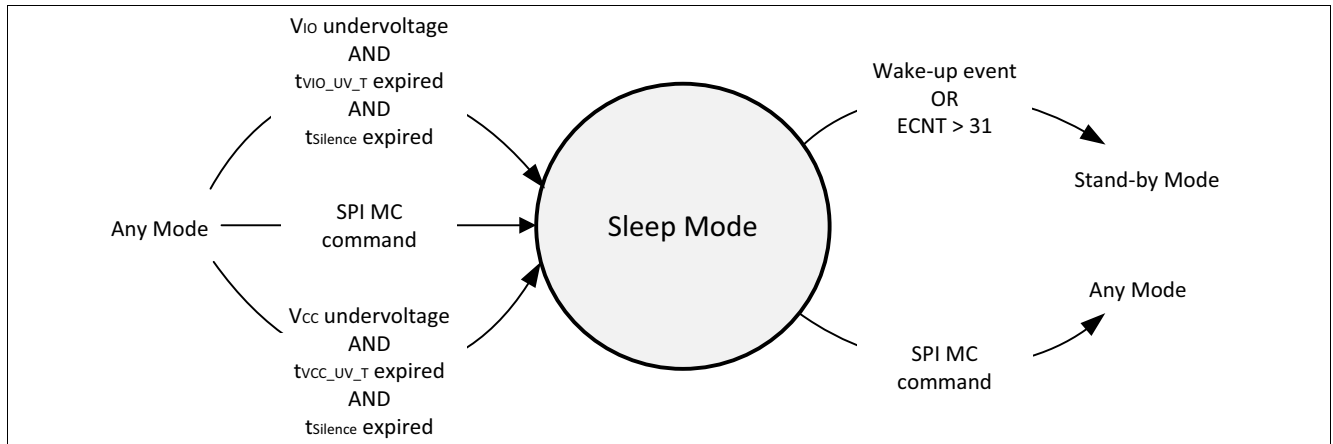


Figure 8 Mode change in Sleep Mode

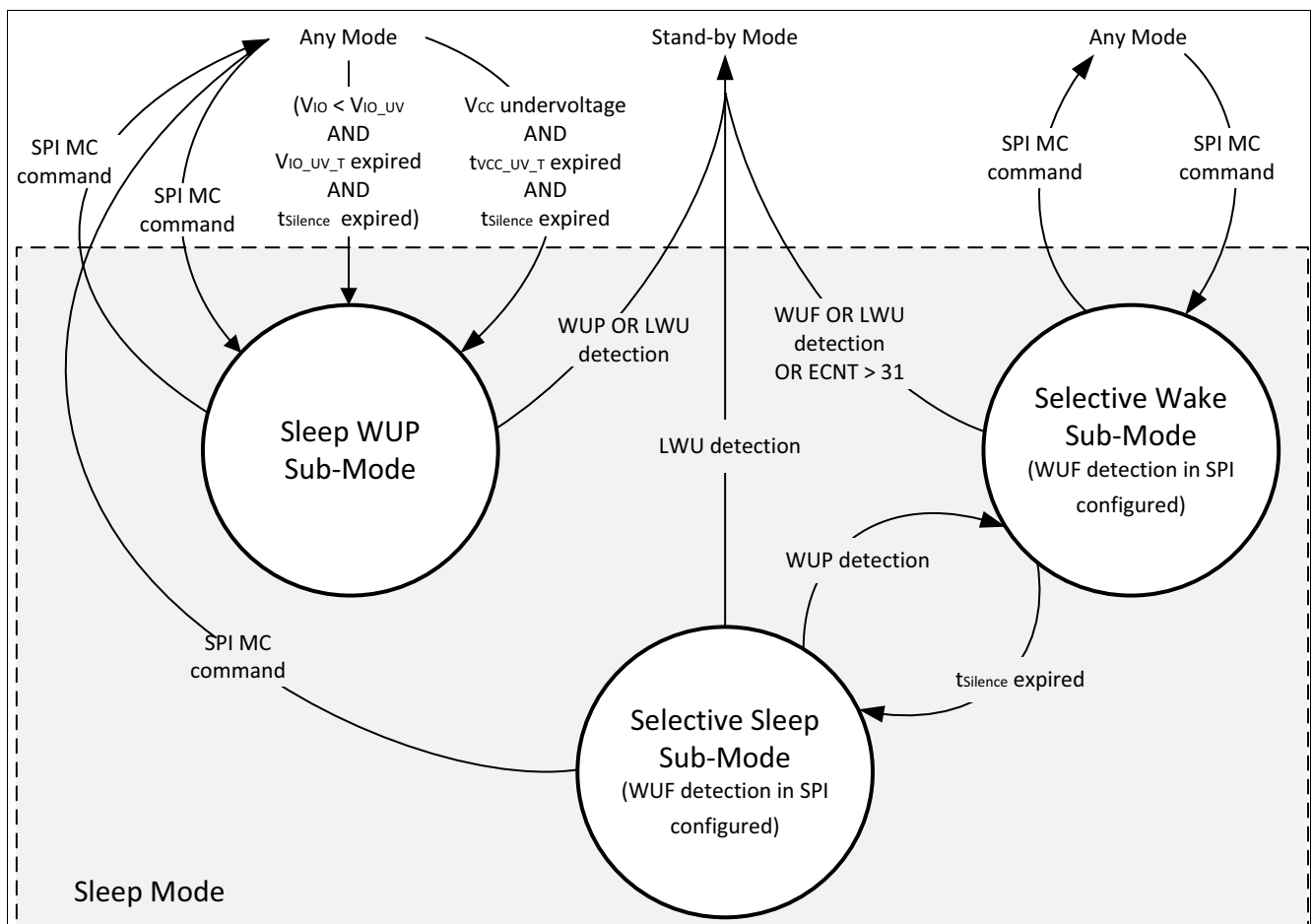


Figure 9 Sub-Modes in Sleep Mode

Modes of Operation

Figure 10 shows the internal behavior of the TLE9255W in case the microcontroller sends a change to Sleep Mode SPI command.

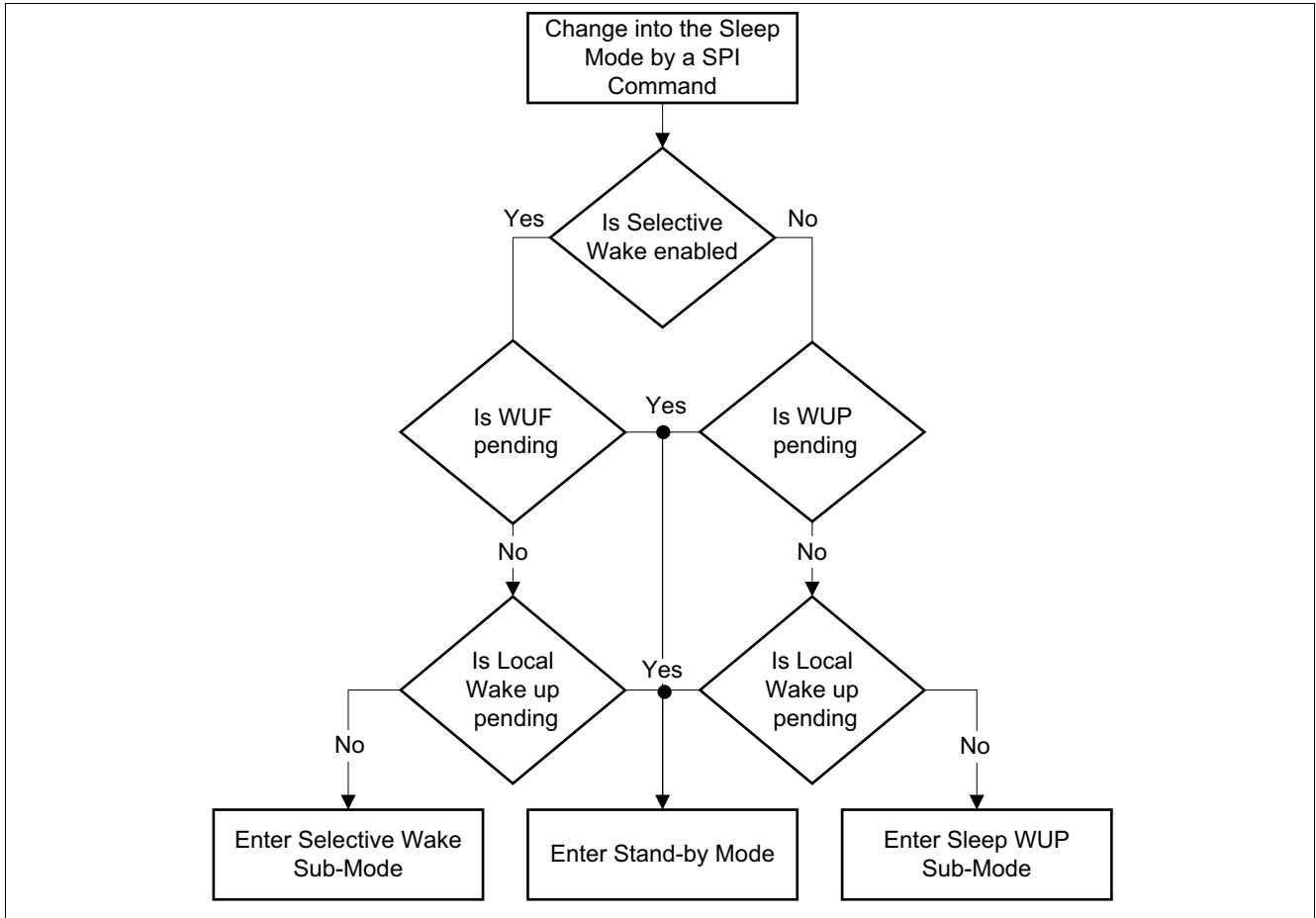


Figure 10 Internal behavior of the TLE9255W after receiving a change to Sleep Mode SPI command

## Modes of Operation

### 5.4.1 Sleep WUP Sub-Mode

Sleep WUP Sub-Mode is a low power mode of the TLE9255W. Sleep WUP Sub-Mode reduces current consumption. The following conditions are valid for the Sleep WUP Sub-Mode:

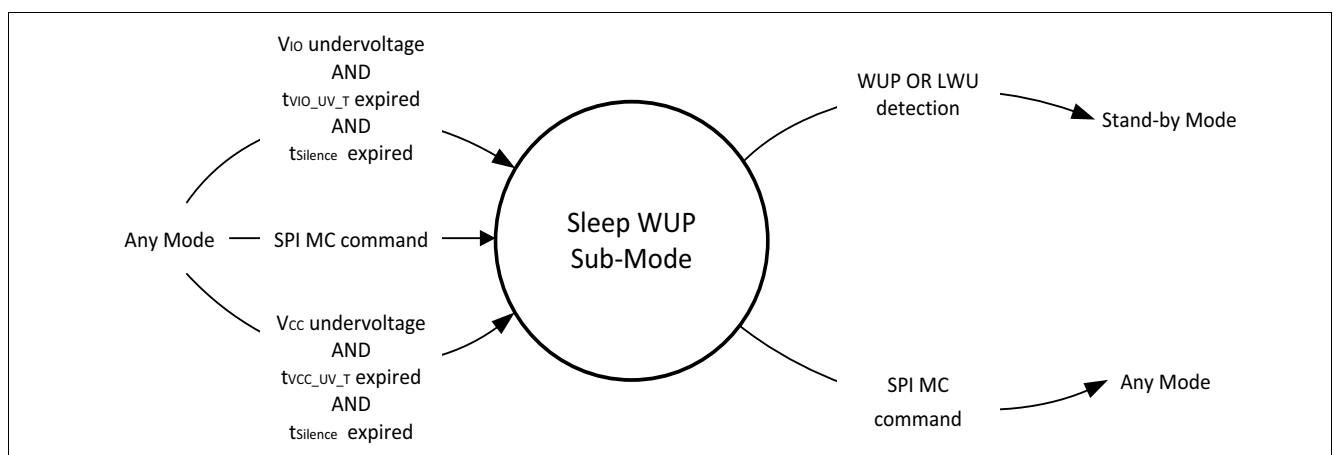
- The transmitter is disabled and the data available on the TxD input is blocked.
- The value of the RxD output pin depends on the power supply circuit of  $V_{IO}$ .
  - Permanent power supply of  $V_{IO}$  (INH pin is not used)  
The RxD output pin is “high”
  - The INH pin controls the power supply of  $V_{IO}$   
The RxD output pin is “low”
- If the  $t_{\text{silence}}$  timer has expired, then the bus biasing is off.
- The TxD timeout function is disabled ([Chapter 6.4](#)).
- The overtemperature protection is disabled ([Chapter 6.5](#)).
- The undervoltage detection on  $V_{BAT}$  ([Chapter 6.2.1](#)) is not signalled in the SPI bit **VBAT\_UV**.
- The undervoltage detection on  $V_{CC}$  is disabled ([Chapter 6.2.2](#)).
- The undervoltage detection on  $V_{IO}$  ([Chapter 6.2.4](#)) is not signalled in the SPI bits **VIO\_LTUV** and **VIO\_STUV**.
- The INH output pin is “low”. The SPI bit **VBAT\_CON** in the register **SWK\_CTRL\_1** controls the behavior of the INH pin.
- The HS CAN bus is continuously monitored for a valid wake-up pattern ([Chapter 5.7.1](#)).
- The HS CAN bus is not monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is enabled.

Conditions for entering the Sleep WUP Sub-Mode:

- If  $V_{IO} < V_{IO\_UV}$  ( $V_{IO}$  undervoltage) AND  $t_{VIO\_UV\_T}$  has expired AND  $t_{\text{silence}}$  has expired, then the TLE9255W enters Sleep WUP Sub-Mode.
- If  $V_{CC} < V_{CC\_UV}$  ( $V_{CC}$  undervoltage) AND  $t_{VCC\_UV\_T}$  has expired AND  $t_{\text{silence}}$  has expired, then the TLE9255W enters Sleep WUP Sub-Mode. The SPI bit **STTS\_EN** controls this state transition.
- The Sleep WUP Sub-Mode can be entered via an SPI MC command from any mode of operation.

Conditions for leaving the Sleep WUP Sub-Mode:

- If a wake-up (WUP, LWU) is detected in Sleep WUP Sub-Mode, then the TLE9255W enters Stand-by Mode.
- An SPI MC command triggers a mode change to any mode of operation.



**Figure 11 Mode change in Sleep WUP Sub-Mode**

---

## Modes of Operation

### 5.4.2 Selective Wake Sub-Mode

Selective Wake Sub-Mode is a low power mode of the TLE9255W. Only if the selective wake function is enabled (**SWK\_EN**= 1), then the TLE9255W can enter Selective Wake Sub-Mode. [Chapter 7](#) describes the partial networking functionality and the configuration. The following conditions are valid for the Selective Wake Sub-Mode:

- The transmitter is disabled and the data available on the TxD input is blocked.
- The default value of the RxD output pin depends on the power supply circuit of  $V_{IO}$ .
  - Permanent power supply of  $V_{IO}$  (INH pin is not used)  
The RxD output pin is “high”
  - The INH pin controls the power supply of  $V_{IO}$   
The RxD output pin is “low”
- The bus biasing is on.
- The TxD timeout function is disabled ([Chapter 6.4](#)).
- The overtemperature protection is disabled ([Chapter 6.5](#)).
- The undervoltage detection on  $V_{BAT}$  is enabled ([Chapter 6.2.1](#)).
- The undervoltage detection on  $V_{CC}$  is disabled ([Chapter 6.2.2](#)).
- The undervoltage detection on  $V_{IO}$  is enabled ([Chapter 6.2.4](#)).
- The INH output pin is “low”. The SPI bit **VBAT\_CON** in the register **SWK\_CTRL\_1** controls the behavior of the INH pin.
- A valid wake-up pattern is not signalled in the SPI bit **WUP** ([Chapter 5.7.1](#)).
- The HS CAN bus is continuously monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is enabled.

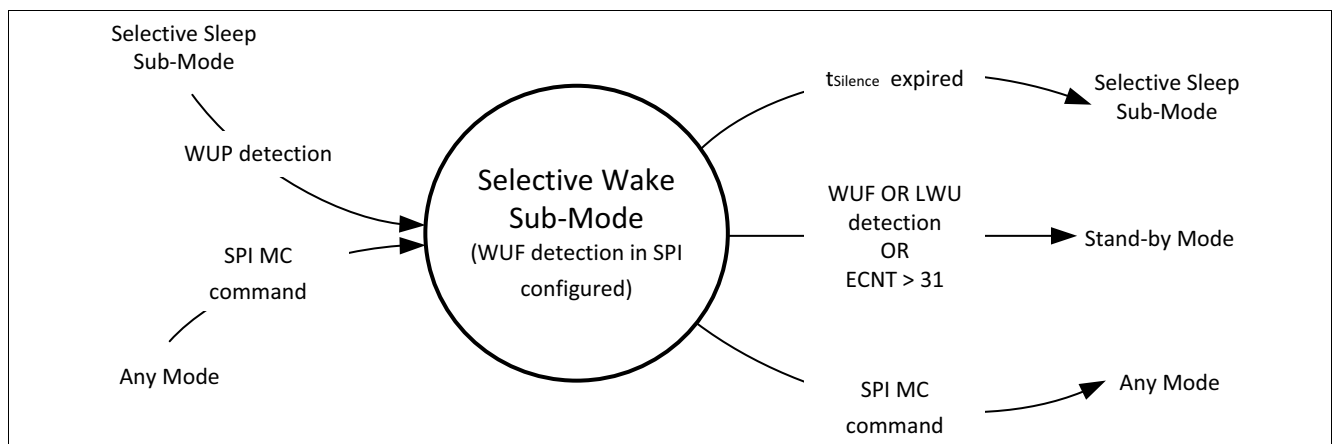
## Modes of Operation

Conditions for entering the Selective Wake Sub-Mode:

- The Selective Wake Sub-Mode can be entered via an SPI MC command from any mode of operation.
- If the TLE9255W detects a WUP in Selective Sleep Sub-Mode, then it enters Selective Wake Sub-Mode.

Conditions for leaving the Selective Wake Sub-Mode:

- If a wake-up (WUF, LWU) is detected in Selective Wake Sub-Mode, then Stand-by Mode is entered.
- If the error counter > 31 ([Chapter 7.3](#)) in Selective Wake Sub-Mode, then Stand-by Mode is entered.
- If  $t_{\text{Silence}}$  has expired, then Selective Sleep Sub-Mode is entered.
- An SPI MC command will trigger a mode change to any mode of operation.



**Figure 12 Mode change in Selective Wake Sub-Mode**

## Modes of Operation

### 5.4.3 Selective Sleep Sub-Mode

Selective Sleep Sub-mode is a low power mode with optimized quiescent current. The following conditions are valid for the Selective Wake Sub-Mode:

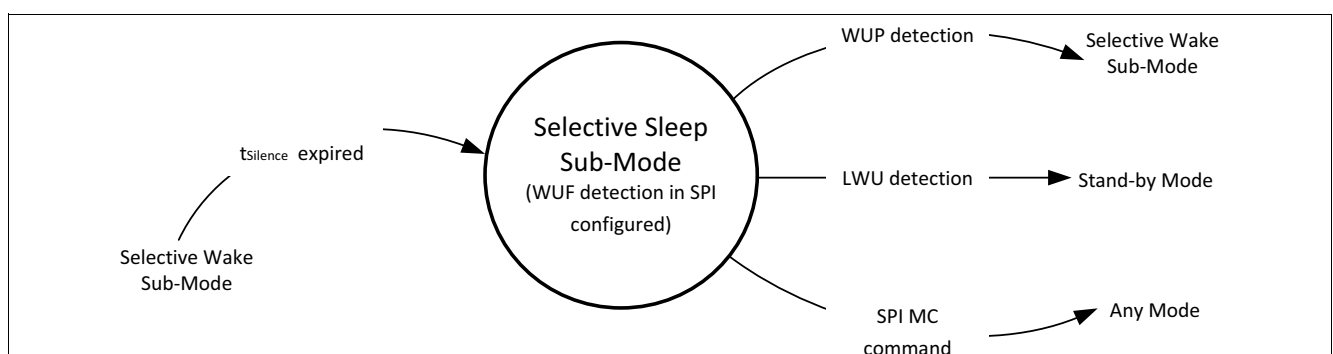
- The transmitter is disabled and the data available on the TxD input is blocked.
- The default value of the RxD output pin depends on the power supply circuit of  $V_{IO}$ .
  - Permanent power supply of  $V_{IO}$  (INH pin is not used)  
The RxD output pin is “high”
  - The INH pin controls the power supply of  $V_{IO}$   
The RxD output pin is “low”
- The bus biasing is off.
- The TxD timeout function is disabled ([Chapter 6.4](#)).
- The overtemperature protection is disabled ([Chapter 6.5](#)).
- The undervoltage detection on  $V_{BAT}$  ([Chapter 6.2.1](#)) is not signalled in the SPI bit **VBAT\_UV**.
- The undervoltage detection on  $V_{CC}$  is disabled ([Chapter 6.2.2](#)).
- The undervoltage detection on  $V_{IO}$  ([Chapter 6.2.4](#)) is not signalled in the SPI bits **VIO\_LTUV** and **VIO\_STUV**.
- The INH output pin is “low”. The SPI bit **VBAT\_CON** in the register **SWK\_CTRL\_1** controls the behavior of the INH pin.
- The HS CAN bus is continuously monitored for a valid wake-up pattern ([Chapter 5.7.1](#)), but a valid wake-up pattern is not signalled in the SPI bit **WUP** ([Chapter 5.7.1](#)).
- The HS CAN bus is not monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is enabled.

Conditions for entering the Selective Sleep Sub-Mode:

- If there is no communication on the HS CAN bus for longer than  $t_{\text{Silence}}$  in the Selective Wake Sub-Mode, then the TLE9255W enters the Selective Sleep Sub-Mode.

Conditions for leaving the Selective Sleep Sub-Mode:

- If a WUP is detected, then Selective Wake Sub-Mode is entered.
- If an LWU has been detected, then Stand-by Mode will be entered.
- An SPI MC command triggers a mode change to any mode of operation.



**Figure 13 Mode change in Selective Sleep Sub-Mode**

## Modes of Operation

### 5.5 Power On Reset

Power on Reset is a transition state of the TLE9255W after power is applied and the transceiver is not yet fully functional.

- The transmitter and receiver are disabled.
- The bus biasing is off.
- The TxD timeout function is disabled.
- The overtemperature protection is disabled.
- The undervoltage detection on  $V_{BAT}$  is enabled ([Chapter 6.2.1](#)), but it is not signalled in the SPI bit **VBAT\_UV**.
- The undervoltage detection on  $V_{CC}$  is disabled.
- The undervoltage detection on  $V_{IO}$  is enabled ([Chapter 6.2.4](#)), but it is not signalled in the SPI bits **VIO\_LTUV** and **VIO\_STUV**.
- The SPI communication is blocked (MOSI, SCLK, CSN),
- RxD and MISO pins are high impedance.
- TxD pin is blocked
- If  $V_{BAT} > V_{BAT\_POD}$  OR  $V_{CC} > V_{CC\_POD}$ , then the INH output pin is switched on
- All SPI registers are reset to default values.
- The HS CAN bus is not continuously monitored for a valid wake-up pattern ([Chapter 5.7.1](#))
- The HS CAN bus is not monitored for a valid WUF ([Chapter 5.7.2](#)).
- Local wake-up function is disabled.

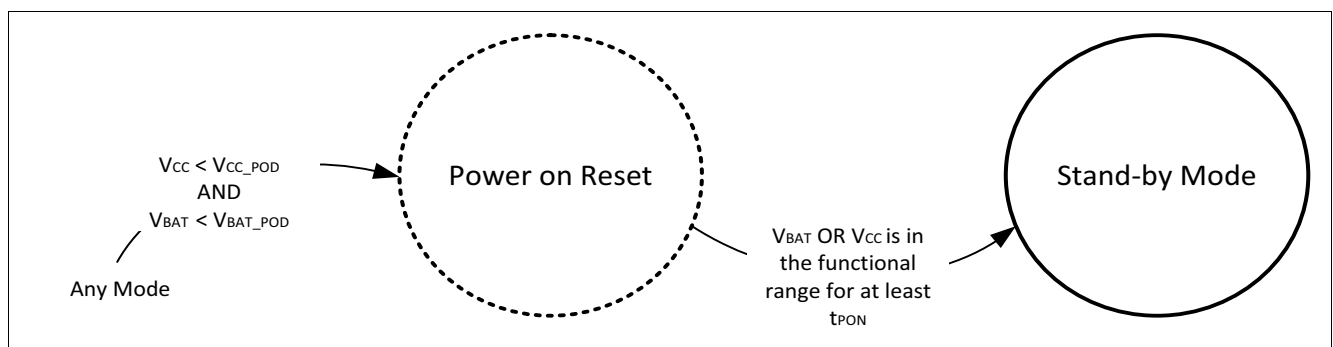
Conditions for entering the Power on Reset:

- $V_{BAT} < V_{BAT\_POD}$  AND  $V_{CC} < V_{CC\_POD}$  threshold.

Conditions for leaving the Power on Reset:

- If  $V_{BAT}$  is within the functional range for at least  $t_{PON}$  OR if  $V_{CC}$  is within the functional range for at least  $t_{PON}$ , then the TLE9255W enters Stand-by Mode

**Figure 14** shows power up behavior and power down behavior:



**Figure 14** Power down and power up behavior

#### SPI bit **POR**

The **POR** flag indicates that all registers are reset and the state machine is in the default mode (Stand-by Mode) If all of the following conditions are fulfilled, then the **POR** flag is set:

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**Modes of Operation**

- $V_{BAT}$  is within the functional range for at least  $t_{PON}$  OR  $V_{CC}$  is within the functional range for at least  $t_{PON}$ , then the TLE9255W enters Stand-by Mode
- $V_{IO}$  is within the functional range (SPI communication is possible)

Any of the following events resets the **POR** flag:

- an SPI clear command
- a transition to the Normal-operating Mode



Modes of Operation

5.6 Automatic Bus Voltage Biasing

The automatic bus voltage biasing improves EMC performance of the entire network and increases the reliability of communication performance in networks using CAN partial networking.

The automatic bus voltage biasing is enabled in all low power modes. The biasing unit operates independently from all other transceiver functions and only depending on the network activity ( $t_{Silence}$ ). If  $t_{Silence}$  has expired, then there is no activity on the CAN bus. The  $t_{Silence}$  timer is restarted under the following conditions:

- If  $t_{Silence}$  has expired in Sleep WUP Sub-Mode AND a WUP is detected
- If  $t_{Silence}$  has not expired in Sleep WUP Sub-Mode AND a rising or falling edge is detected AND the pulse width (dominant or recessive) is greater than  $t_{Filter}$
- If a WUP is detected in Selective Sleep Sub-Mode
- If  $t_{Silence}$  has expired in Stand-by Mode AND a WUP is detected
- If the  $t_{Silence}$  has not expired in Stand-by Mode AND a rising edge or a falling edge is detected AND the pulse width (dominant or recessive) is greater than  $t_{Filter}$
- If a rising or falling edge is detected in any other mode AND the pulse width (dominant or recessive) is greater than  $t_{Filter}$

If there is no activity on the bus for longer than  $t_{SILENCE}$ , then the internal resistors bias the bus pins towards GND. On detection of a valid wake-up pattern (WUP), the internal biasing is enabled and terminates the biasing resistors towards 2.5 V within  $t > t_{RW\_Bias}$ .

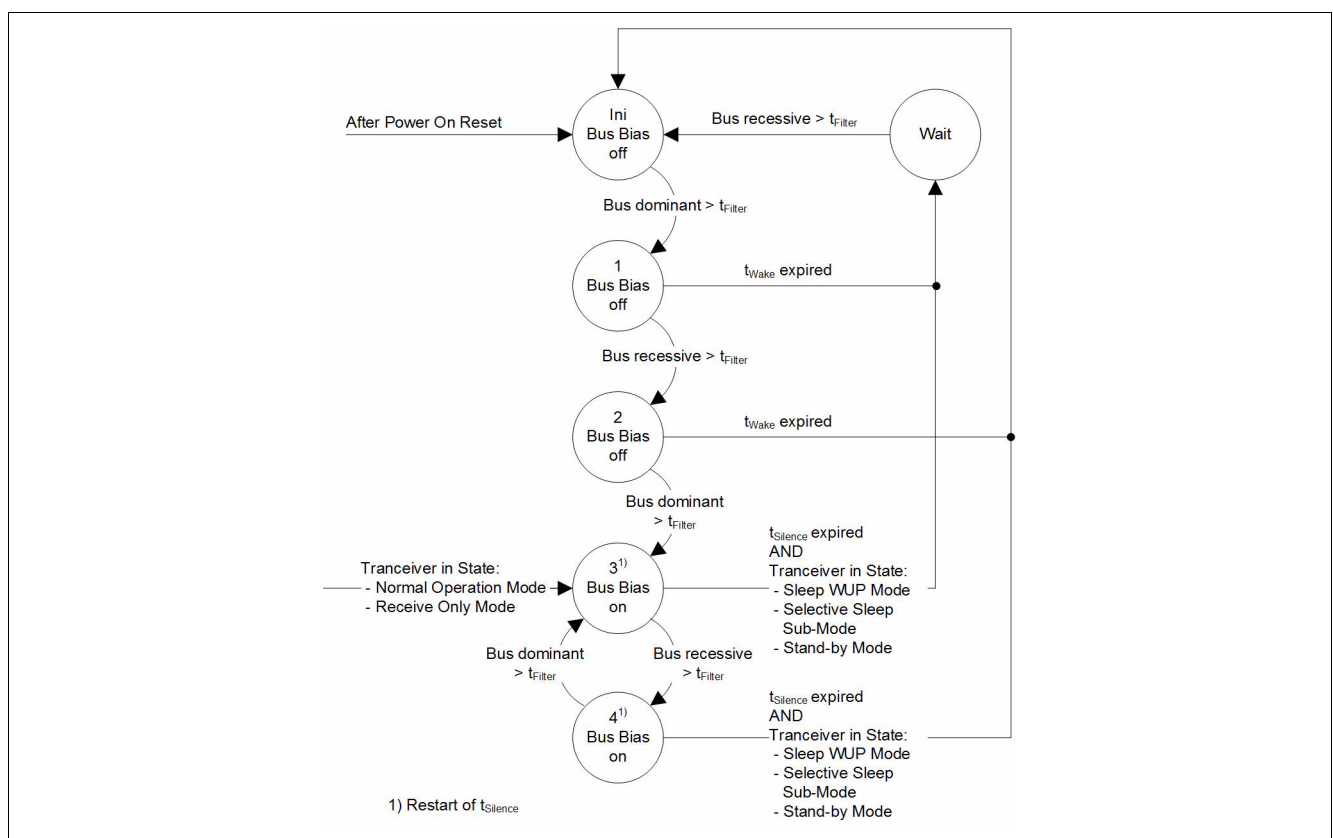


Figure 15 Bus Biasing and  $t_{Silence}$

Modes of Operation

5.7 Wake-up event

Valid wake-up events are:

- a Wake-up pattern (WUP) in Sleep WUP Sub-Mode
  - a Wake-up frame (WUF) in Selective Wake Sub-Mode
  - a Local Wake-up (LWU) in Sleep WUP Sub-Mode, Selective Sleep Sub-Mode or Selective Wake Sub-Mode
- If a valid wake-up event is detected, then this triggers a mode change to Stand-by Mode.

5.7.1 Wake-up pattern (WUP)

Within the maximum wake-up time  $t_{WAKE}$ , the wake-up pattern consists of the following sequence (see Figure 16):

- a dominant signal with pulse width  $t > t_{Filter}$
- a recessive signal with pulse width  $t > t_{Filter}$
- a dominant signal with pulse width  $t > t_{Filter}$

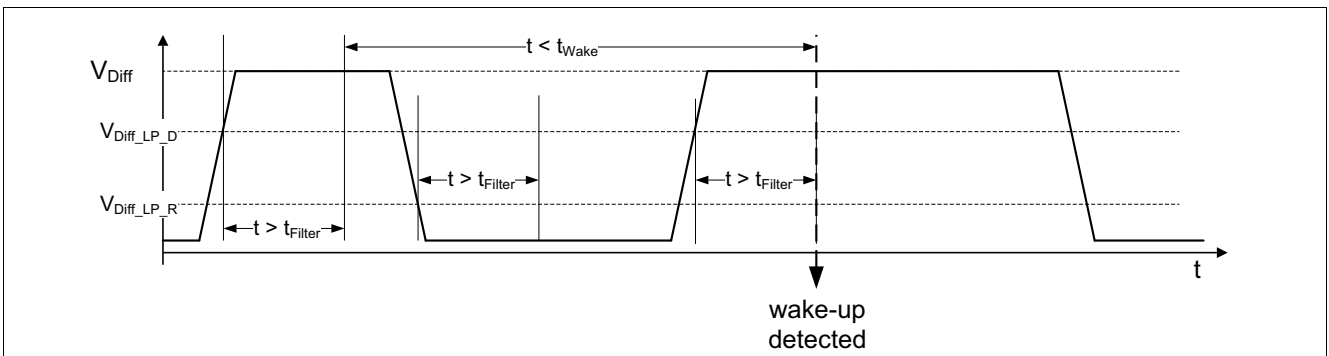


Figure 16 Wake-up pattern

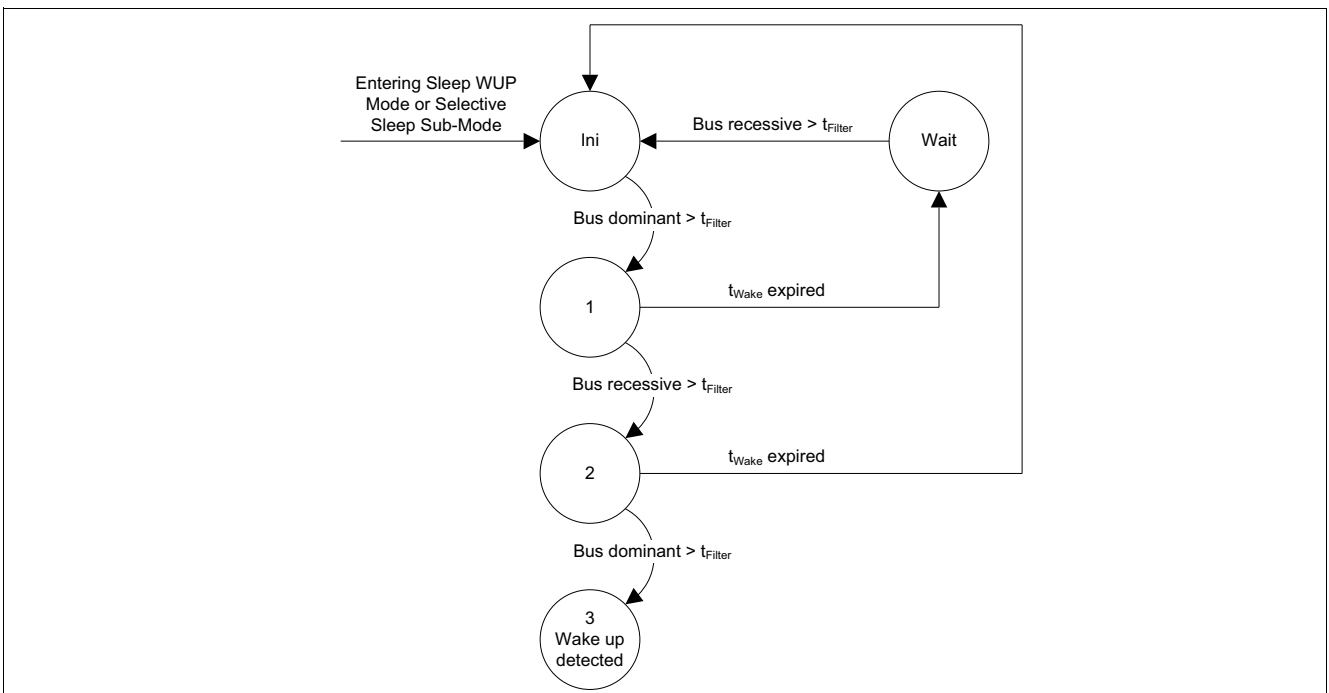


Figure 17 WUP detection

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## Modes of Operation

The **WUP** bit in the register **WAKE\_STAT** indicates detection of a wake-up pattern on the HS CAN bus. If the transceiver is not in the Selective Sleep Sub-Mode AND if the transceiver detects a valid wake-up pattern, then the WUP bit is set. An SPI clear command resets the bit. A wake-up is not executed under the following conditions:

- A mode change to Normal-operating Mode is performed during the wake-up pattern.
- The maximum wake-up time  $t_{\text{WAKE}}$  expires before a valid WUP is detected.
- The transceiver is powered down ( $V_{\text{CC}} < V_{\text{CC\_POD}}$  AND  $V_{\text{BAT}} < V_{\text{BAT\_POD}}$ ).

### 5.7.2 Wake-up frame (WUF)

If the selective wake unit is enabled (**SWK\_EN** =1), then the selective wake unit continuously monitors the HS CAN Bus for a valid wake-up frame. If a valid WUF is detected, then the **WUF** bit in the register **WAKE\_STAT** is set to "1". An SPI clear command resets the **WUF** bit. **Chapter 7** describes the selective wake feature.

## Modes of Operation

### 5.7.3 Local Wake-up (LWU)

The WAKE input pin can detect a rising edge as well as a falling edge as a wake-up event (configurable in **LWU\_NEG**, **LWU\_POS**). The **LWU** bit in the register **WAKE\_STAT** indicates that a local wake-up is detected on the local wake-up pin. The transceiver sets the **LWU** bit. An SPI command resets the **LWU** bit. The **LWU\_DIR** bit in the register **WAKE\_STAT** indicates on which edge a local wake-up has been detected. The transceiver sets the **LWU\_DIR** flag and it is only valid, if a local wake-up has been detected. **Chapter 10.6.3** describes the local wake-up timing.

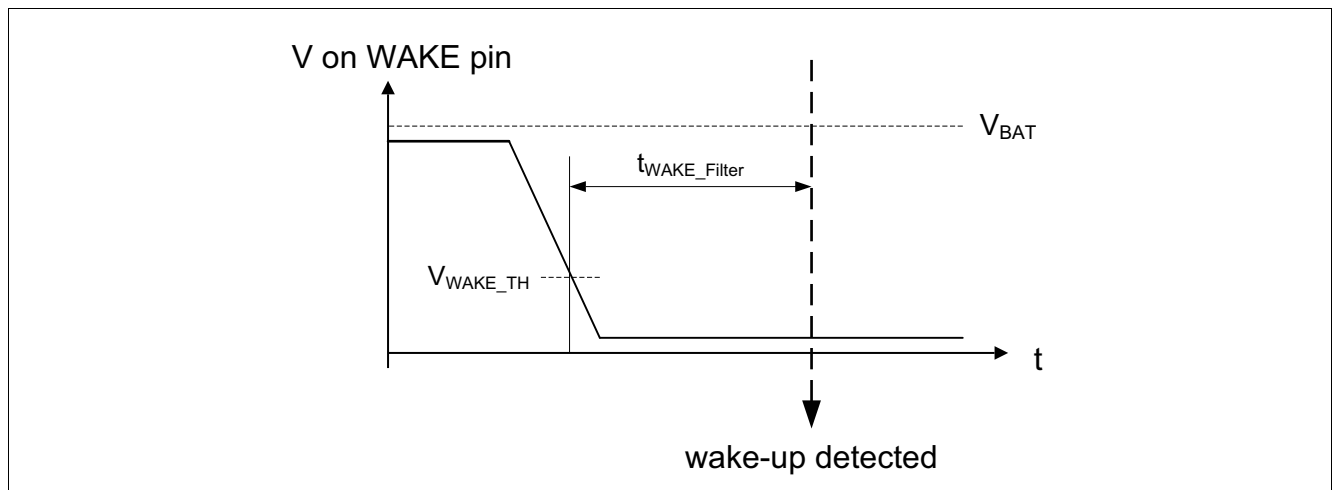


Figure 18 Local wake-up negative edge

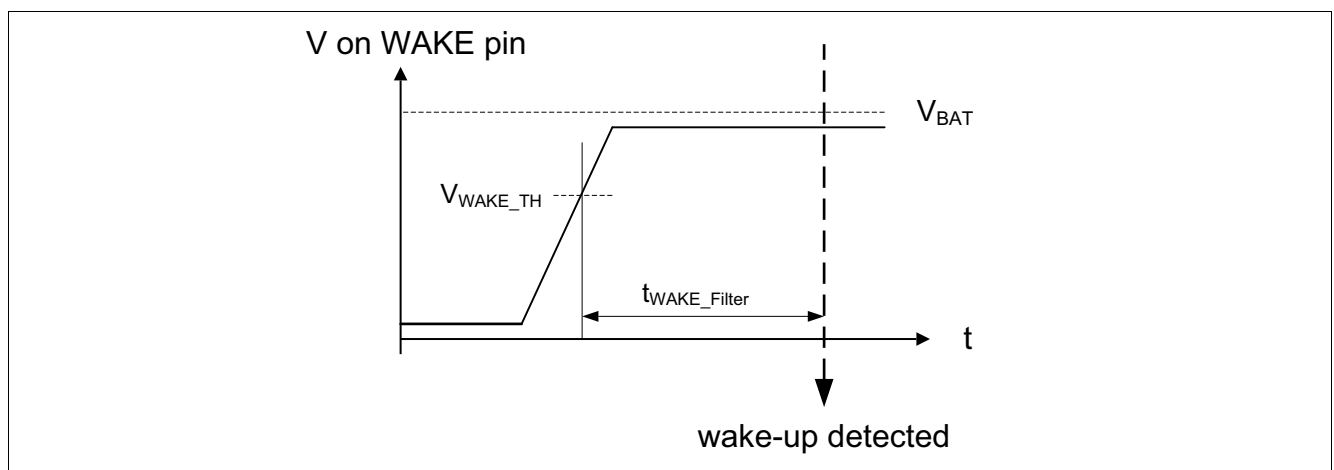


Figure 19 Local wake-up positive edge

Modes of Operation

5.8 RxD pin wake-up behavior

The RxD output pin indicates a wake-up event to the microcontroller. On detection of a valid wake-up event the RxD output pin reacts with one of the following behaviors, depending on the **WAKE\_TOG** bit in the SPI register **HW\_CTRL**:

- RxD output pin is set to “low”
- RxD output pin starts to toggle

If Stand-by Mode is re-entered by a mode change (microcontroller) the previous indication of a valid wake-up event is not signalled on the RxD pin. Only if a new wake-up event has been detected, the RxD pin indicates the wake-up event. The clearing of a **WUP**, **WUF** or **LWU** has no influence on the behavior of the RxD pin.

5.8.1 RxD permanent “low”

If a valid wake-up event is detected AND if SPI bit **WAKE\_TOG** = 0, then the RxD output pin is set to “low”. If a mode change occurs, then the RxD output pin behavior is defined by the new state.

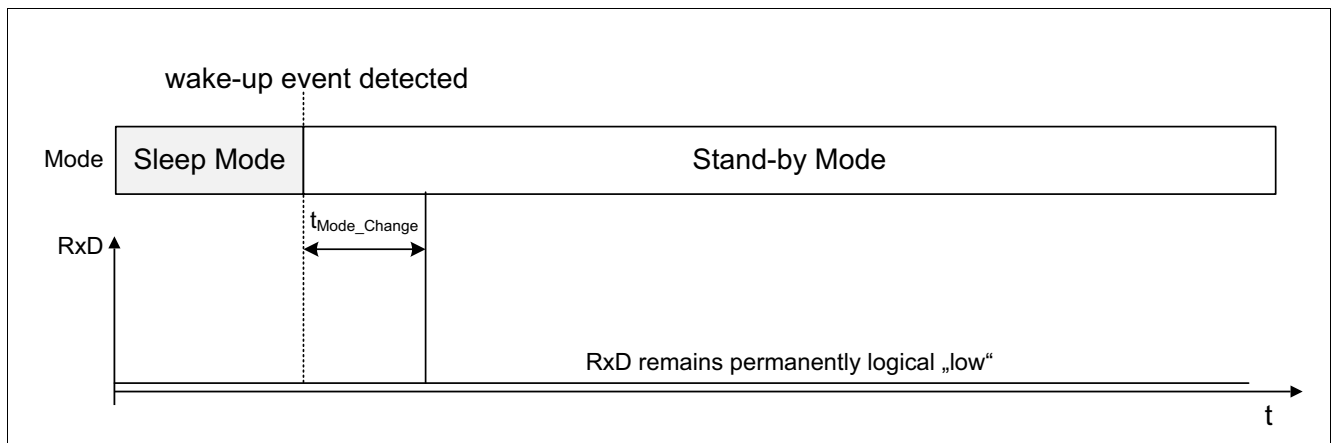


Figure 20 RxD “low” after wake-up event

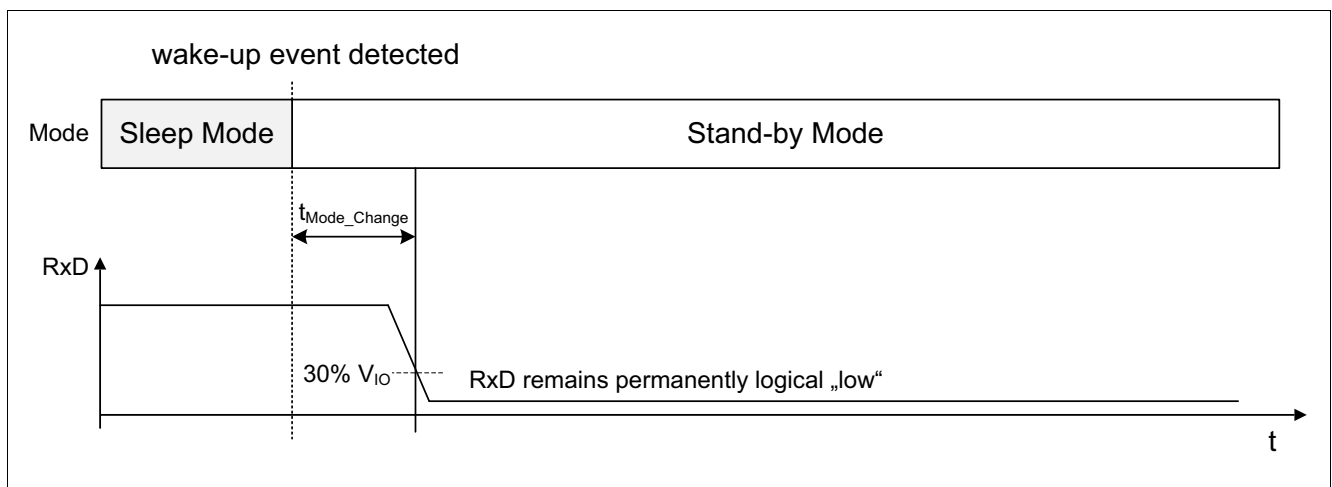


Figure 21 RxD “low” after wake-up event (permanently supplied  $V_{IO}$ )

Modes of Operation

5.8.2 RxD Toggle

If **WAKE\_TOG** is set to 1 AND if a valid wake-up event is detected AND if  $V_{IO}$  is within the functional range, then the RxD output pin starts to toggle from “low” to “high” and “high” to “low” with time period of  $t_{Toggle}$ . **Figure 22** and **Figure 23** show this behavior. If a mode change occurs, then the RxD output pin behavior is defined by the new state.

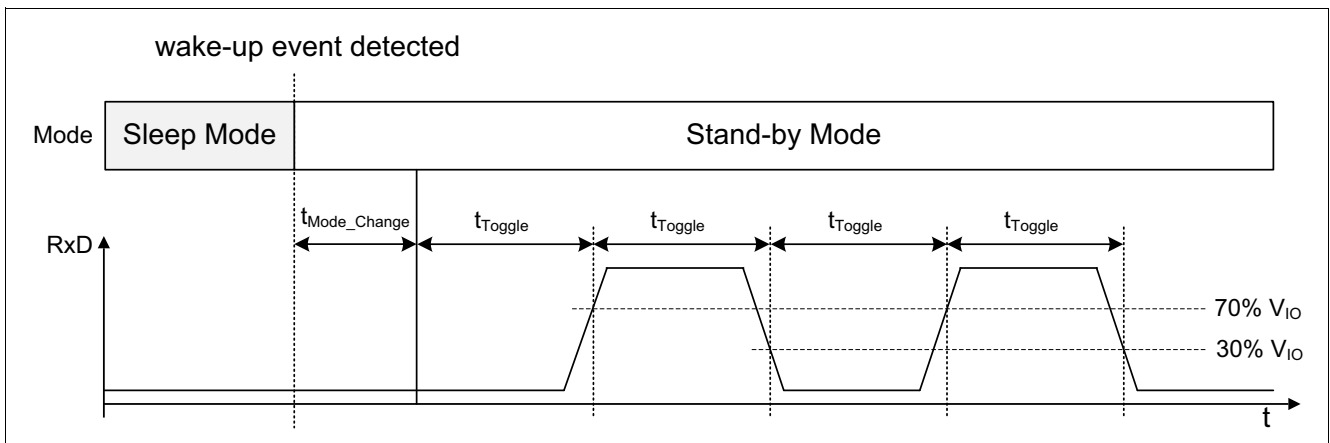


Figure 22 RxD toggling behavior after wake-up event

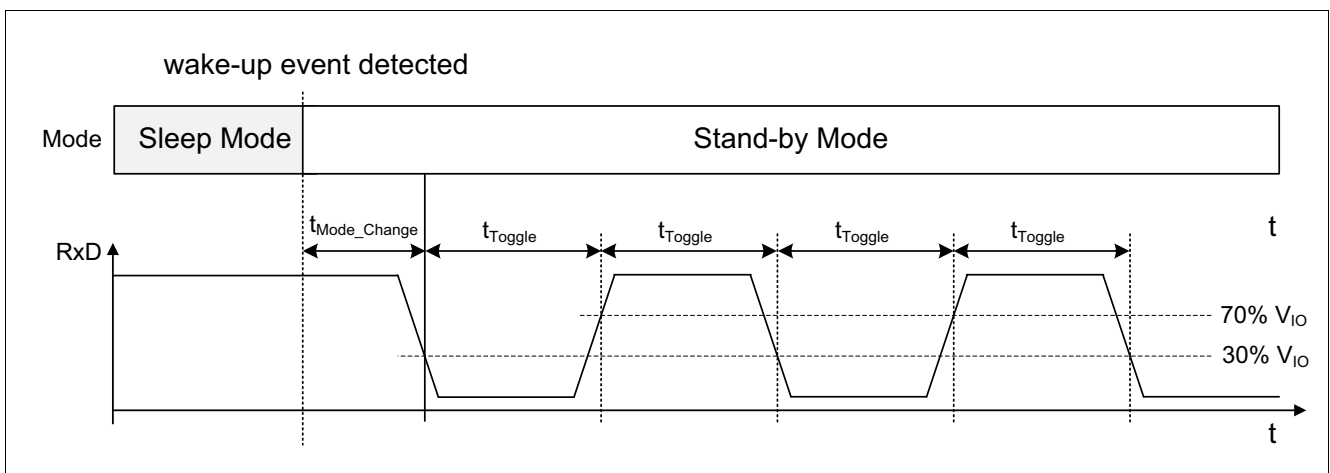


Figure 23 RxD toggling behavior after wake-up event (permanently supplied  $V_{IO}$ )

## 6 Fail Safe Functions

### 6.1 Short Circuit Protection

The CANH and CANL bus pins are proven to cope with a short circuit fault to GND and to the supply voltages. A current limiting circuit protects the transceiver from damage.

### 6.2 Undervoltage detection

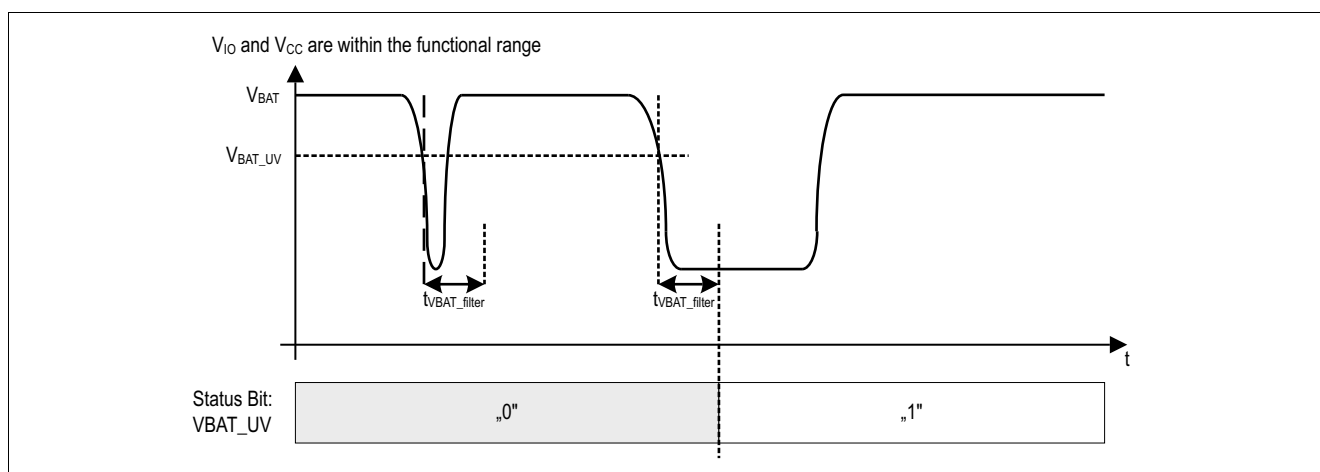
The TLE9255W has independent undervoltage detection on  $V_{BAT}$ ,  $V_{CC}$  and  $V_{IO}$ . Undervoltage events at these pins may have impact on the functionality of the device and also may change the mode of operation.

#### 6.2.1 Undervoltage detection on $V_{BAT}$

If the power supply  $V_{BAT} < V_{BAT\_UV}$  for more than the glitch filter time  $t_{VBAT\_filter}$ , then an undervoltage is detected. On detection of undervoltage the TLE9255W performs the following actions:

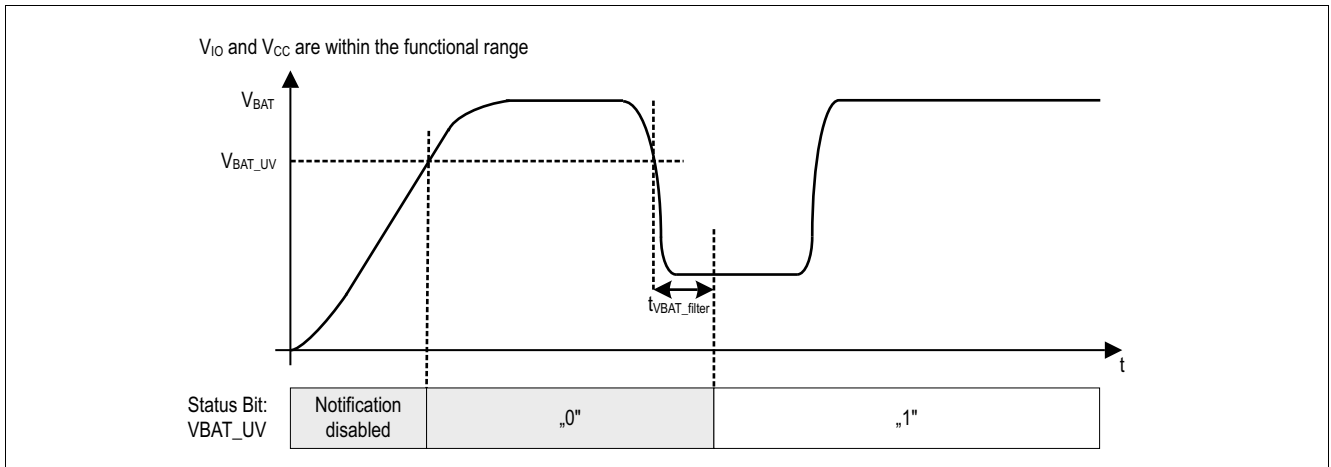
- disable Local wake-up
- Set the bit **VBAT\_UV** in the SPI register **TRANS\_UV\_STAT** to "1". After the completion of a Power on Reset or after a transition from Sleep Mode to Stand-by Mode the  $V_{BAT}$  supply stabilization period must be completed before an undervoltage notification can be recorded in the **VBAT\_UV** bit. The undervoltage notification is only possible once the  $V_{BAT}$  supply has exceeded the threshold  $V_{BAT\_UV}$ , that is  $V_{BAT} > V_{BAT\_UV}$ . **Figure 25** shows this scenario.

Only an SPI command can reset the undervoltage bit **VBAT\_UV** (see **Chapter 8.2**). The glitch filter is implemented in order to prevent an undervoltage detection due to short voltage transients on  $V_{BAT}$ . **Figure 24** shows the effect of glitch filter time in different undervoltage scenarios.



**Figure 24** Undervoltage detection  $V_{BAT}$

Fail Safe Functions



**Figure 25 Undervoltage detection  $V_{BAT}$  during  $V_{BAT}$  supply stabilization period**

After power up the application can set the  **$VBAT\_CON$**  to "0" in the SPI Register  **$SUPPLY\_CTRL$**  in order to disable undervoltage detection.



Fail Safe Functions

6.2.2 Short-term Undervoltage detection on  $V_{CC}$

If the power supply  $V_{CC} < V_{CC\_UV}$  for more than the glitch filter time  $t_{V_{CC\_filter}}$ , then a short-term undervoltage on  $V_{CC}$  is detected. The glitch filter prevents an undervoltage detection due to short voltage transients on  $V_{CC}$ . On detection of short-term undervoltage the TLE9255W performs the following actions:

- Set short-term undervoltage bit **VCC\_STUV** to “1” in the SPI register **TRANS\_UV\_STAT**. Only after the completion of a Power on Reset, the  $V_{CC}$  supply stabilization period must be completed before an undervoltage notification can be recorded in the **VCC\_STUV** bit. After Power on Reset the undervoltage notification is only possible once the  $V_{CC}$  supply has exceeded the threshold  $V_{CC\_UV}$ , that is  $V_{CC} > V_{CC\_UV}$ . **Figure 27** shows this scenario.
- disable the transmitter

An SPI command can reset the undervoltage bit **VCC\_STUV**. If  $V_{CC} > V_{CC\_UV}$  for more than the glitch filter time  $t_{V_{CC\_filter}}$  AND if the transmitter recovery time  $t_{V_{CC\_recovery}}$  has expired, then the transmitter is re-enabled.

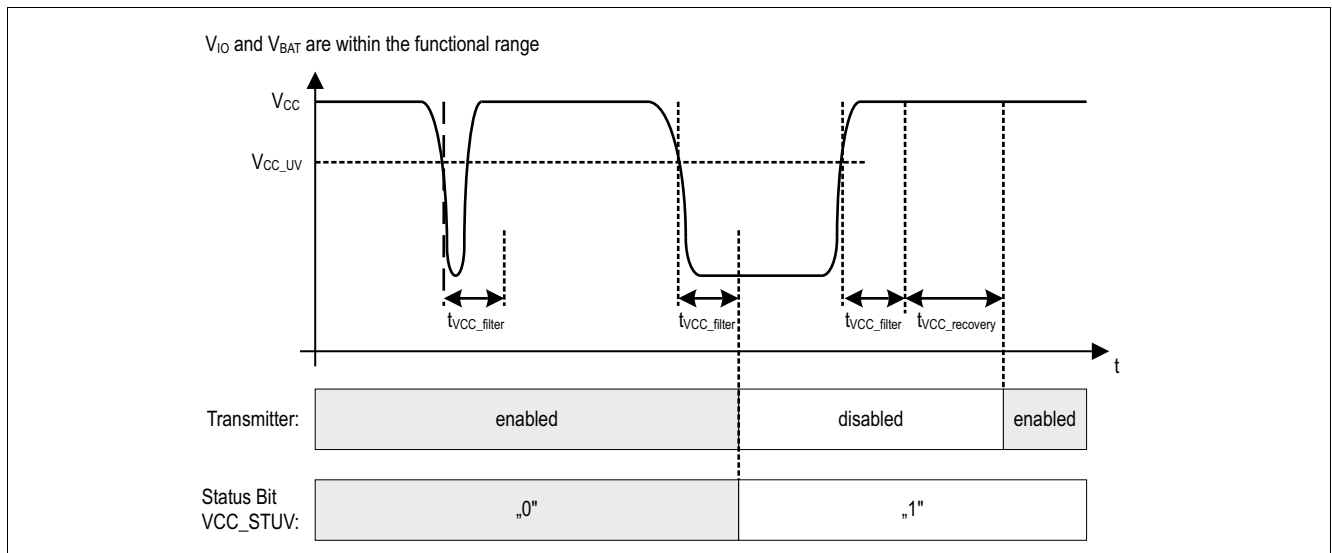


Figure 26  $V_{CC}$  undervoltage detection

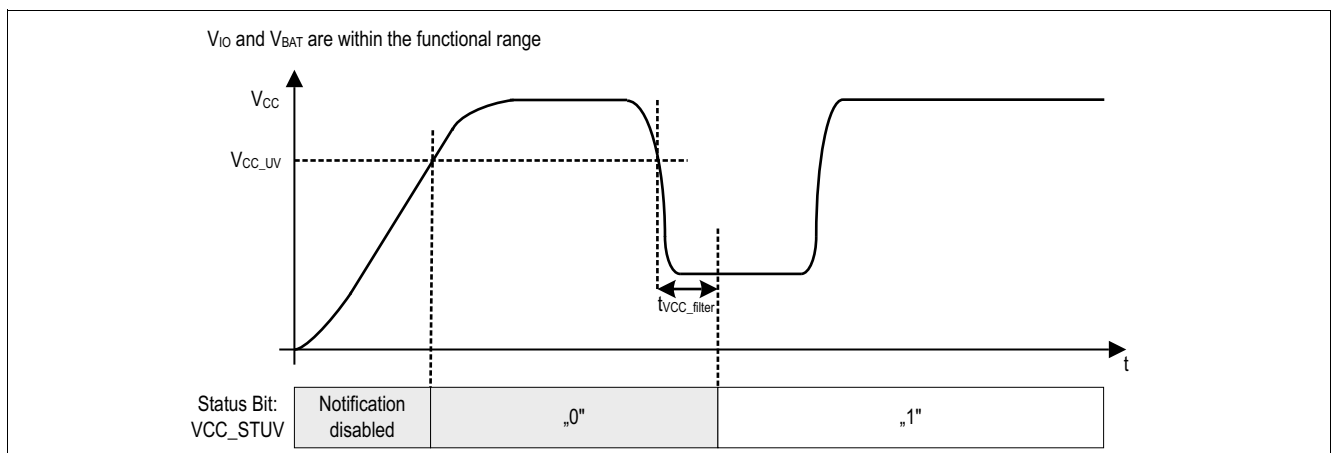


Figure 27 Undervoltage detection  $V_{CC}$  during  $V_{CC}$  supply stabilization period after Power on Reset

Fail Safe Functions

6.2.3 Long-term undervoltage detection on  $V_{CC}$

If  $V_{CC} < V_{CC\_UV}$  for more than the glitch filter time  $t_{V_{CC\_filter}}$ , then the undervoltage detection timer is started. If  $t_{V_{CC\_UV\_T}}$  has expired, then a long-term undervoltage is detected and the bit **VCC\_LTUV** is set to "1". Besides, if the SPI bit **STTS\_EN** = 1 (default value) AND if  $t_{Silence}$  has expired, then a state transition to Sleep WUP Sub-Mode is triggered. If  $V_{CC} > V_{CC\_UV}$  for more than the glitch filter time  $t_{V_{CC\_filter}}$ , then the timer  $t_{V_{CC\_UV\_T}}$  is stopped and reset. Only an SPI command can reset the undervoltage bit **VCC\_LTUV**. The  $t_{V_{CC\_UV\_T}}$  can be configured in the SPI register **SUPPLY\_CTRL**.

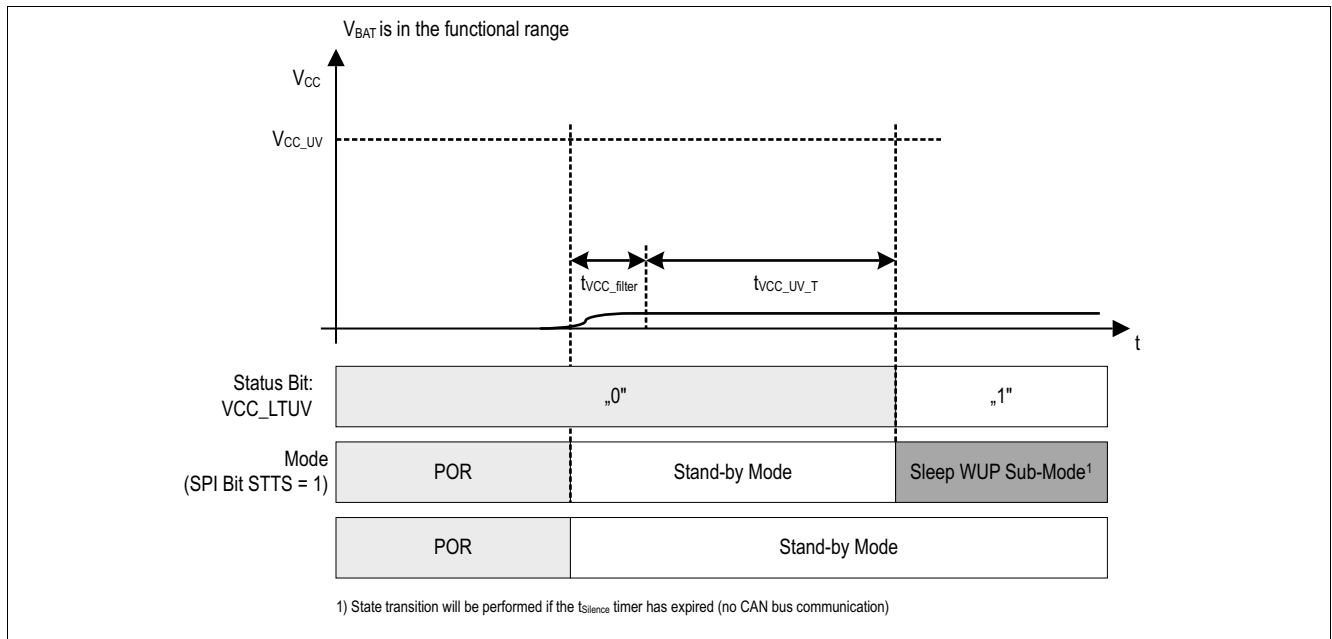


Figure 28  $V_{CC}$  long-term undervoltage detection after power up

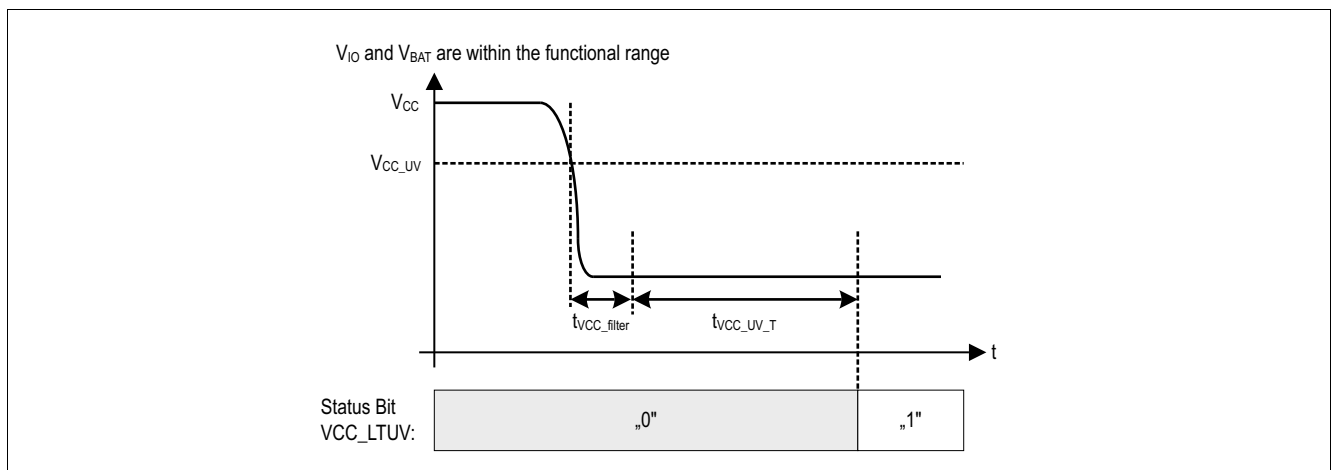


Figure 29  $V_{CC}$  long-term undervoltage detection during operation

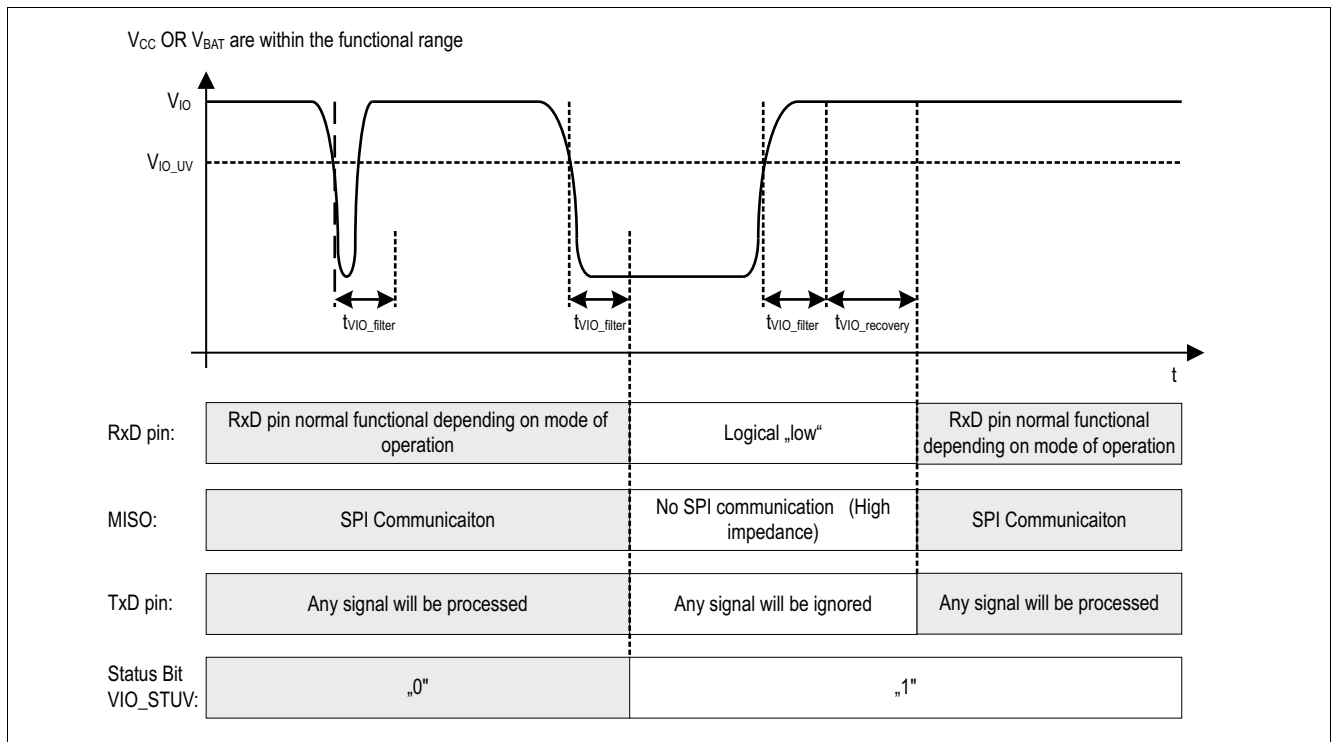
6.2.4 Short-term Undervoltage detection on  $V_{IO}$

If the power supply  $V_{IO} < V_{IO\_UV}$  for more than the glitch filter time  $t_{V_{IO\_filter}}$ , then short-term undervoltage on  $V_{IO}$  is detected. The glitch filter prevents an undervoltage detection due to short voltage transients on  $V_{IO}$ . On detection of short-term undervoltage the TLE9255W performs the following actions:

**Fail Safe Functions**

- Set the short-term undervoltage bit **VIO\_STUV** to “1” in the SPI register **TRANS\_UV\_STAT**. After the completion of a Power on Reset, the  $V_{IO}$  supply stabilization period must be completed before an undervoltage notification can be recorded in the **VIO\_STUV** bit. After Power on Reset the undervoltage notification is only be possible once the  $V_{IO}$  supply has exceeded the threshold  $V_{IO\_UV}$ , that is  $V_{IO} > V_{IO\_UV}$ . **Figure 31** shows this scenario.
- set the RxD pin to “low”
- disable SPI communication by switching the MISO pin to high impedance
- TLE9255W ignores all signals on the input TxD pin

Only an SPI command can reset the undervoltage bit **VIO\_STUV**. If  $V_{IO}$  has recovered ( $V_{IO} > V_{IO\_UV}$ ) for more than the glitch filter time  $t_{VIO\_filter}$  AND if the  $t_{VIO\_recovery}$  time has expired, then the RxD pin returns to normal functionality depending on the mode of operation and the SPI communication is restored.



**Figure 30 V<sub>IO</sub> short-term undervoltage detection**

Fail Safe Functions

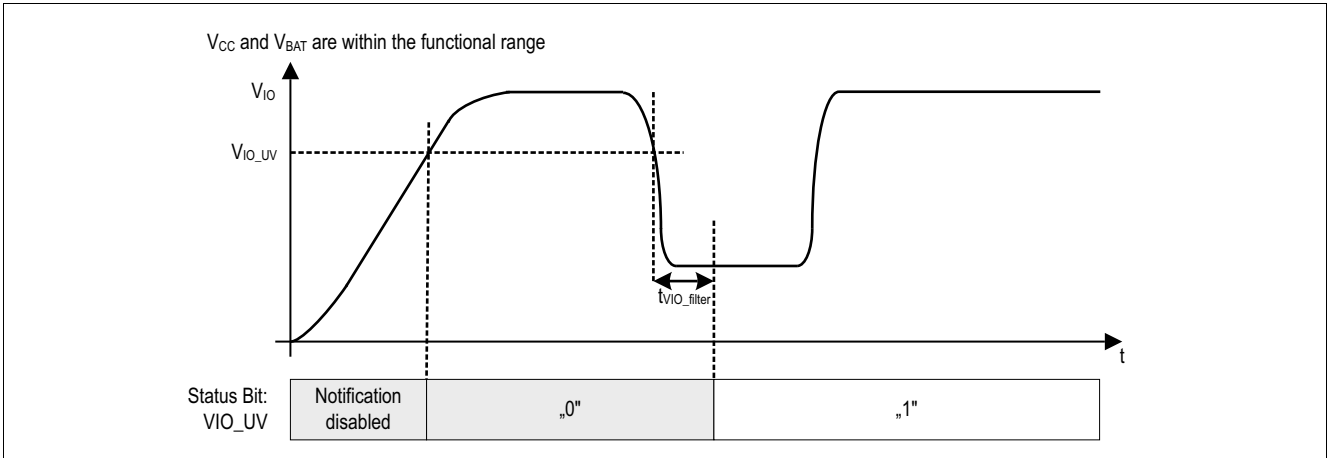


Figure 31 Undervoltage detection V<sub>IO</sub> during V<sub>IO</sub> supply stabilization period after Power on Reset

6.2.5 Long-term Undervoltage detection on V<sub>IO</sub>

If V<sub>IO</sub> < V<sub>IO\_UV</sub> for more than the glitch filter time t<sub>VIO\_filter</sub>, then the undervoltage detection timer is started. If t<sub>VIO\_UV\_T</sub> expires, then a long-term undervoltage is detected. On detection of long-term undervoltage the TLE9255W performs the following actions:

- set the bit **VIO\_LTUV** to “1”
- perform a mode change to Sleep WUP Sub-Mode only after t<sub>Silence</sub> has expired (no bus communication)

If V<sub>IO</sub> > V<sub>IO\_UV</sub> for more than the glitch filter time t<sub>VIO\_filter</sub>, then the timer t<sub>VIO\_UV\_T</sub> is stopped and reset. Only an SPI command can reset the undervoltage bit **VIO\_LTUV**. The t<sub>VIO\_UV\_T</sub> is configurable in the SPI Register **SUPPLY\_CTRL**.

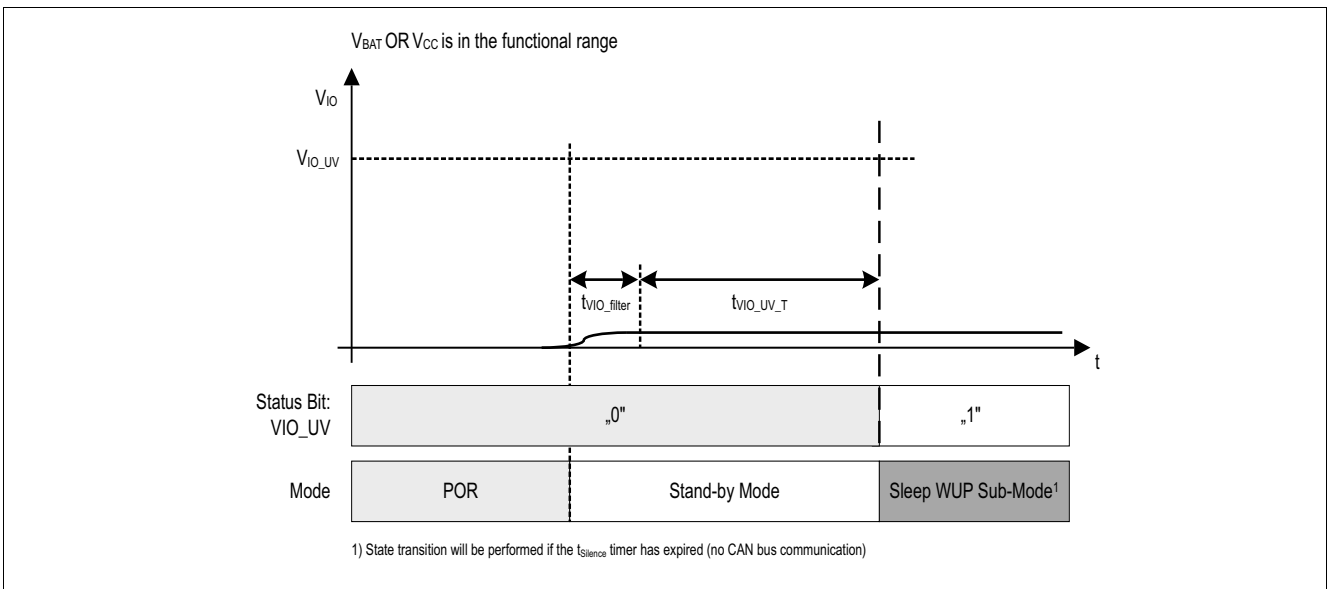


Figure 32 V<sub>IO</sub> long-term undervoltage detection after power up

Fail Safe Functions

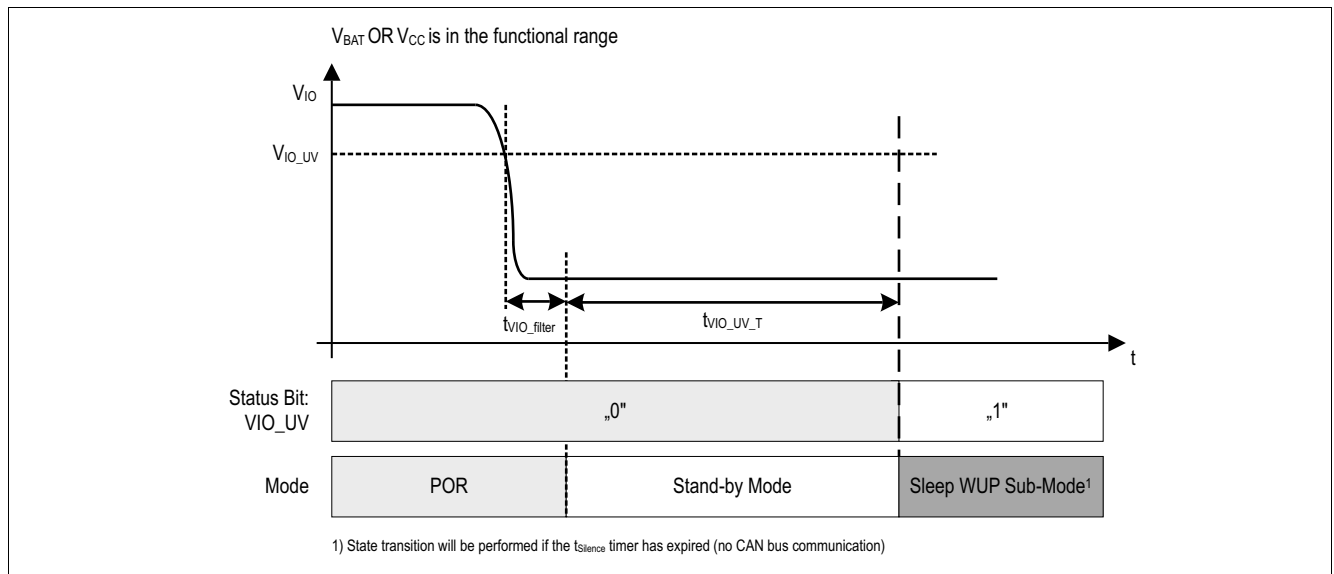


Figure 33 V<sub>IO</sub> long-term undervoltage detection during operation

### 6.3 Unconnected Logic Pins

If the input pins are not connected and floating, the integrated pull-up and pull-down resistors at the digital input pins force the TLE9255W into fail safe behavior (see Table 3).

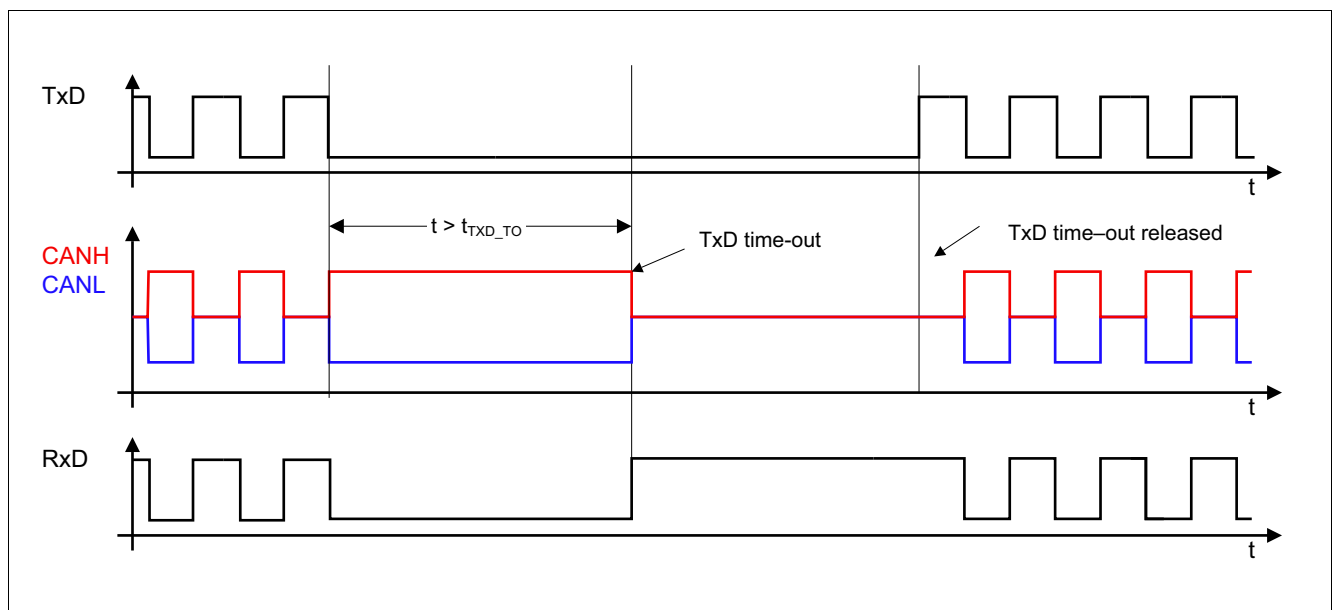
Table 3 Logical Inputs when unconnected

Input Signal	Default State	Comment
TxD	“high”	pull-up current source to V <sub>IO</sub>
MOSI	“low”	pull-down current source to GND
SCLK	“low”	pull-down current source to GND
CSN	“high”	pull-up current source to V <sub>IO</sub>

## Fail Safe Functions

### 6.4 TxD Time-out Function

If the logical signal on the TxD pin is permanently “low”, then the TxD time-out feature protects the CAN bus from blocked communication due to this errant logic signal on TxD. A permanent “low” signal on the TxD pin can occur due to a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In Normal-operating Mode, a “low” signal on the TxD pin for the time  $t > t_{\text{TxD\_TO}}$  enables the TxD time-out feature and the TLE9255W disables the transmitter (see [Figure 34](#)) and sets the **TXD\_TO** bit in the register **TRANS\_STAT**. The timer  $t_{\text{TxD\_TO}}$  is configurable in SPI register **TXD\_TO\_CTRL**. The receiver is still active and the RxD output pin continues monitoring data on the bus.



**Figure 34** TxD time-out function

**Figure 34** shows how the transmitter is deactivated and re-activated. To release the transmitter after a TxD time-out event, the TLE9255W requires a signal change on the TxD input pin from “low” to “high”.

## Fail Safe Functions

### 6.5 Overtemperature Protection

Integrated overtemperature detection protects the TLE9255W from thermal overstress of the transmitter. The overtemperature protection is active in Normal-operating Mode only. The temperature sensor provides the temperature threshold  $T_{JSD}$ . If the junction temperature exceeds the upper threshold  $T_{JSD}$ , then the TLE9255W disables the transmitter and sets the bit **TSD**, indicating that a critical temperature situation is reached. After the device cools down the transmitter is re-enabled. Only an SPI command can reset the **TSD** bit. A hysteresis is implemented within the temperature sensor.



**Figure 35** Overtemperature protection

### 6.6 Delay Time for Mode Change

The TLE9255W performs mode changes within the time window  $t_{\text{Mode\_Change}}$ . During mode changes ( $t_{\text{Mode\_Change}}$ ) the RxD output pin is permanently set to “high” and does not reflect the status on the CANH and CANL input pins. After the mode change is completed, the TLE9255W releases the RxD output pin.

## 7 CAN Partial Networking

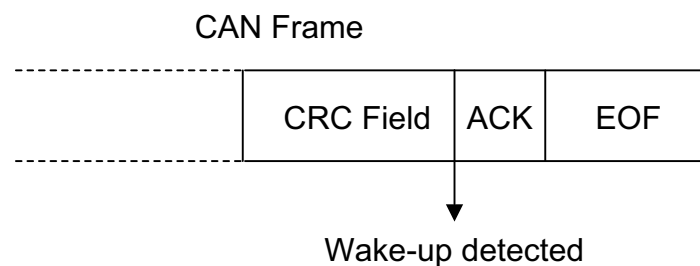
Partial networking allows to exclude nodes from the CAN communication in a CAN network. If the TLE9255W is in the Selective Wake Sub-Mode, then a CAN frame can wake-up the TLE9255W. This feature is called selective wake and the CAN frame is called wake-up frame (WUF). The selective wake unit implements the selective wake feature.

### 7.1 Wake-up frame evaluation

For a WUF detection the TLE9255W evaluates, whether a received CAN frame is a valid wake-up frame. This wake-up frame evaluation consists of the following parts:

- CAN ID evaluation
- Frame data length code (DLC) and data field evaluation

If both parts are evaluated successfully AND if the CRC of the CAN Frame is valid, then a valid wake-up frame is detected (see [Figure 36](#)). The following chapter describes the process in more detail.



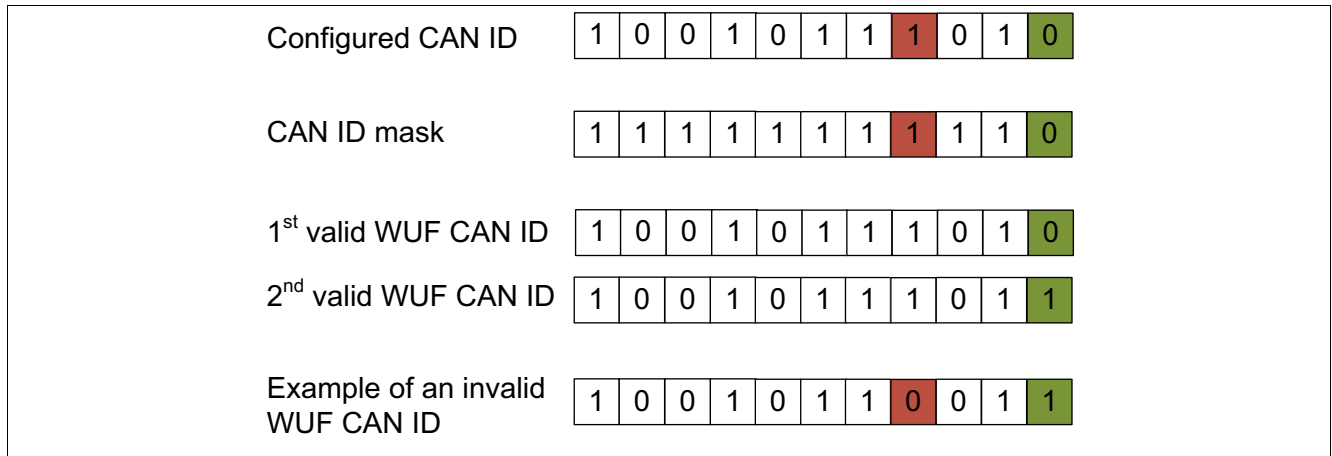
**Figure 36 WUF detection**

#### 7.1.1 Wake-up frame identifier evaluation

If all relevant CAN ID bits of a CAN frame match the configured CAN ID bits in the TLE9255W, then a valid WUF CAN ID is received. The CAN ID mask excludes CAN ID bits from the evaluation. The CAN ID bits of a received CAN frame are compared bit by bit with the CAN ID configured in register [SWK\\_ID0\\_CTRL](#) to [SWK\\_ID3\\_CTRL](#). If the received CAN ID is equal to the configured CAN ID, then the wake-up frame identifier evaluation is successful. The CAN ID mask (registers [SWK\\_MASK\\_ID0\\_CTRL](#) to [SWK\\_MASK\\_ID3\\_CTRL](#)) defines which bits the comparison considers. [Figure 37](#) shows an example of the CAN ID evaluation (11 bit CAN ID). The green background color defines the CAN ID bits which are not considered in the comparison.



**CAN Partial Networking**



**Figure 37 CAN ID and CAN ID mask**

The registers **SWK\_ID0\_CTRL**, **SWK\_ID1\_CTRL**, **SWK\_ID2\_CTRL** and **SWK\_ID3\_CTRL** configure the CAN ID. The **IDE** bit defines the CAN ID format (11 bit or 29 bit identifier).

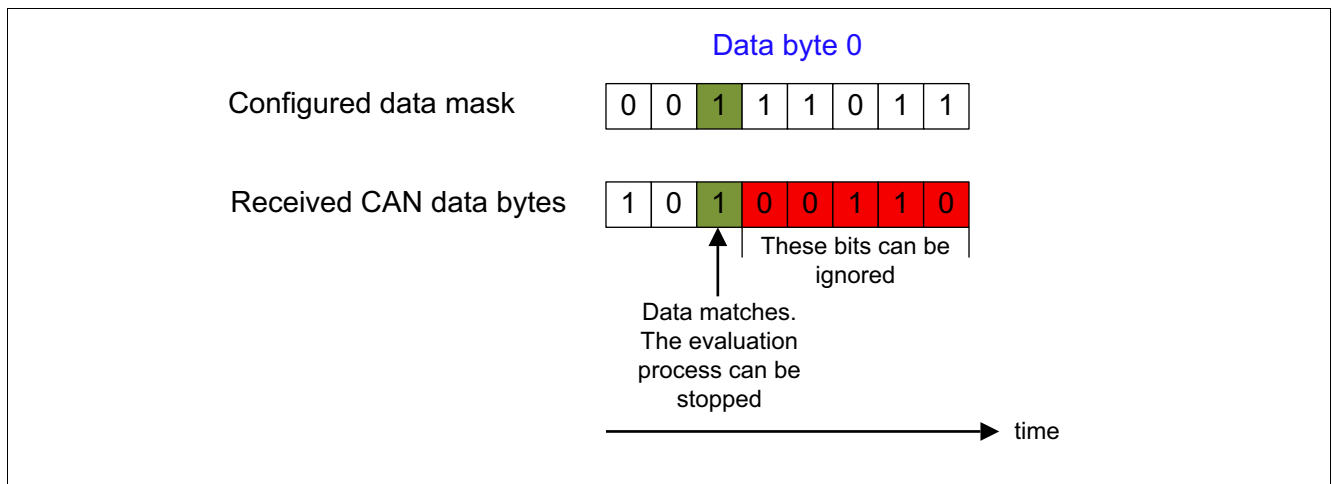
The registers **SWK\_MASK\_ID0\_CTRL**, **SWK\_MASK\_ID1\_CTRL**, **SWK\_MASK\_ID2\_CTRL** and **SWK\_MASK\_ID3\_CTRL** configure the CAN-ID mask.

**7.1.2 DLC and data field evaluation**

If all of the following conditions are fulfilled, then the DLC and data field evaluation is successful:

- the DLC of the received CAN frame is equal to the DLC configured in the **DLC** field of the register **SWK\_DLC\_CTRL**
- At least one bit within the data field of the received CAN frame is “1” and matches to a bit (“1”) of the configured data field. If one bit matches, then the evaluation is stopped. The registers **SWK\_DATA0\_CTRL**, **SWK\_DATA1\_CTRL**, **SWK\_DATA2\_CTRL**, **SWK\_DATA3\_CTRL**, **SWK\_DATA4\_CTRL**, **SWK\_DATA5\_CTRL**, **SWK\_DATA6\_CTRL** and **SWK\_DATA7\_CTRL** configure the data field.

**Figure 38** shows an example for the data field evaluation. The DLC in this example is 1.



**Figure 38 Data field evaluation**

CAN Partial Networking

7.2 Activation of Selective Wake

Figure 39 shows the recommended way to activate the selective wake function in the TLE9255W.

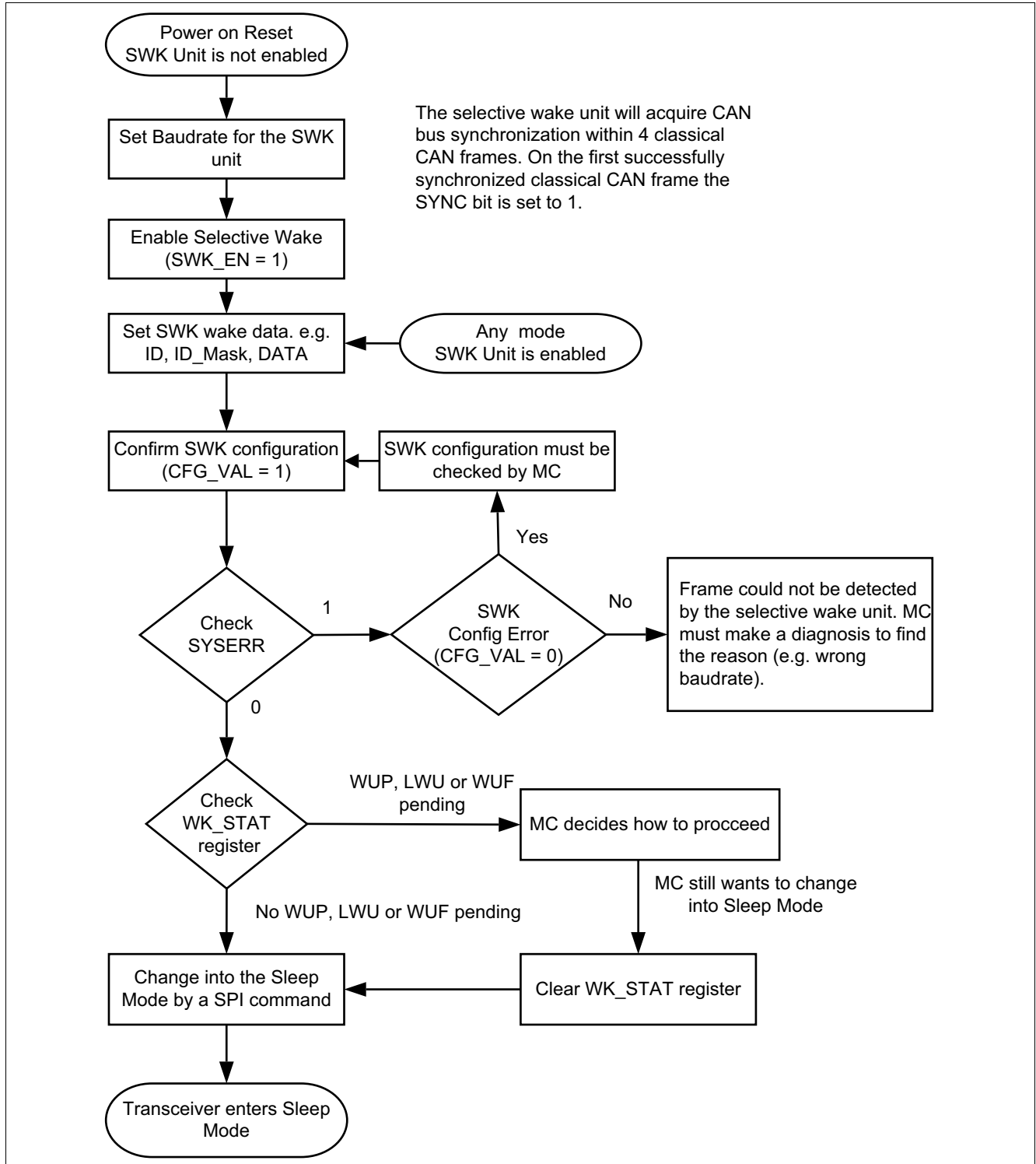


Figure 39 Activation of selective wake function

## CAN Partial Networking

### 7.3 Frame Error Counter

The frame error counter indicates, whether received classical CAN frames are valid. CAN FD frames are not evaluated and therefore CAN FD frame errors do not affect the frame error counter. If the selective wake unit detects a classical CAN frame error, then the frame error counter is increased by 1. If the selective wake unit detects a valid classical CAN frame, then the error counter is decreased by 1. The following types of errors cause invalid classical CAN Frames:

- Bit stuffing error
- CRC error
- CRC delimiter error

If the SPI bit **SWK\_EN** = 1, then the frame error counter is active in any mode of operation. The error counter value can be read via SPI (register **SWK\_ECNT\_STAT**). Each time that the Selective Wake Unit is enabled (**SWK\_EN** = 1) OR if the  $t_{\text{silence}}$  timer has expired, then the error counter is reset to zero.

If the TLE9255W repeatedly receives invalid classical CAN frames in the Selective Wake Sub-Mode, then the frame error counter ensures that a wake-up is performed. If the TLE9255W is in the Selective Wake Sub-Mode and the error counter reaches the value 32, then a wake-up is performed.

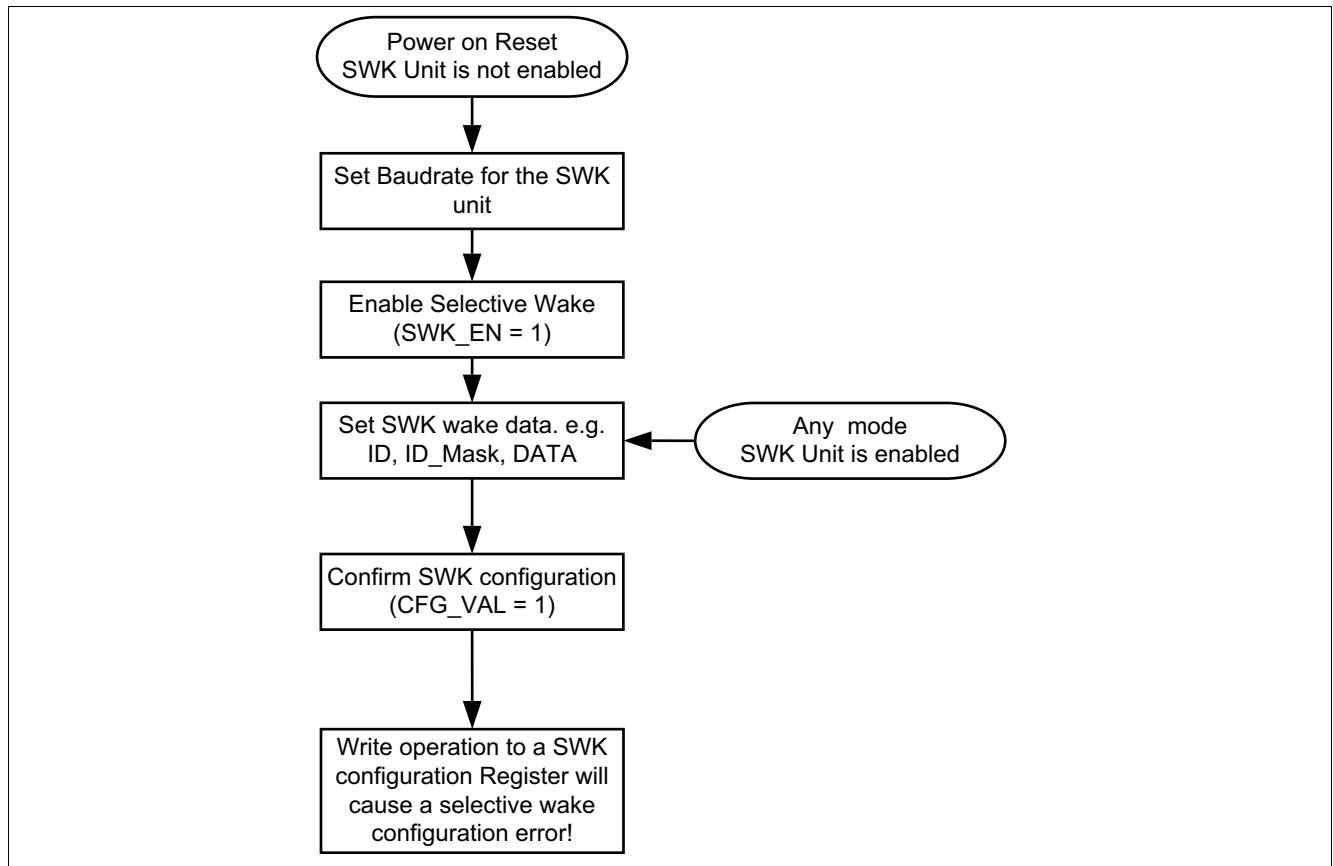
### 7.4 Selective Wake Configuration Error

After the microcontroller has confirmed the configuration (**CFG\_VAL** = 1), writing the following registers generates a selective wake configuration error:

- Baudrate control register (**SWK\_CTRL\_2**)
- Identifier control registers (**SWK\_ID3\_CTRL**, **SWK\_ID2\_CTRL**, **SWK\_ID1\_CTRL** and **SWK\_ID0\_CTRL**)
- Mask identifier control registers (**SWK\_MASK\_ID3\_CTRL**, **SWK\_MASK\_ID2\_CTRL**, **SWK\_MASK\_ID1\_CTRL** and **SWK\_MASK\_ID0\_CTRL**)
- Data Length control register (**SWK\_DLC\_CTRL**)
- Data control registers (**SWK\_DATA7\_CTRL**, **SWK\_DATA6\_CTRL**, **SWK\_DATA5\_CTRL**, **SWK\_DATA4\_CTRL**, **SWK\_DATA3\_CTRL**, **SWK\_DATA2\_CTRL**, **SWK\_DATA1\_CTRL** and **SWK\_DATA0\_CTRL**)

## CAN Partial Networking

The following figure shows a selective wake configuration error.



**Figure 40 Selective wake configuration Error**

## 7.5 CAN Flexible Data Rate (CAN FD) Tolerant Feature

The CAN FD tolerant feature means that selective wake unit ignores CAN FD frames. Therefore it is not possible to configure a CAN FD frame for wake-up frame (WUF) detection.

At the completion of a detected CAN FD frame, that is, the End of Frame (EOF) is detected, the selective wake unit is ready for detecting the next available classical CAN frame. If at least 6 recessive bits and at most 10 recessive bits are received, then EOF detection is successful. The FDF Bit of the Control Field of a CAN FD frame identifies the type of CAN frame:

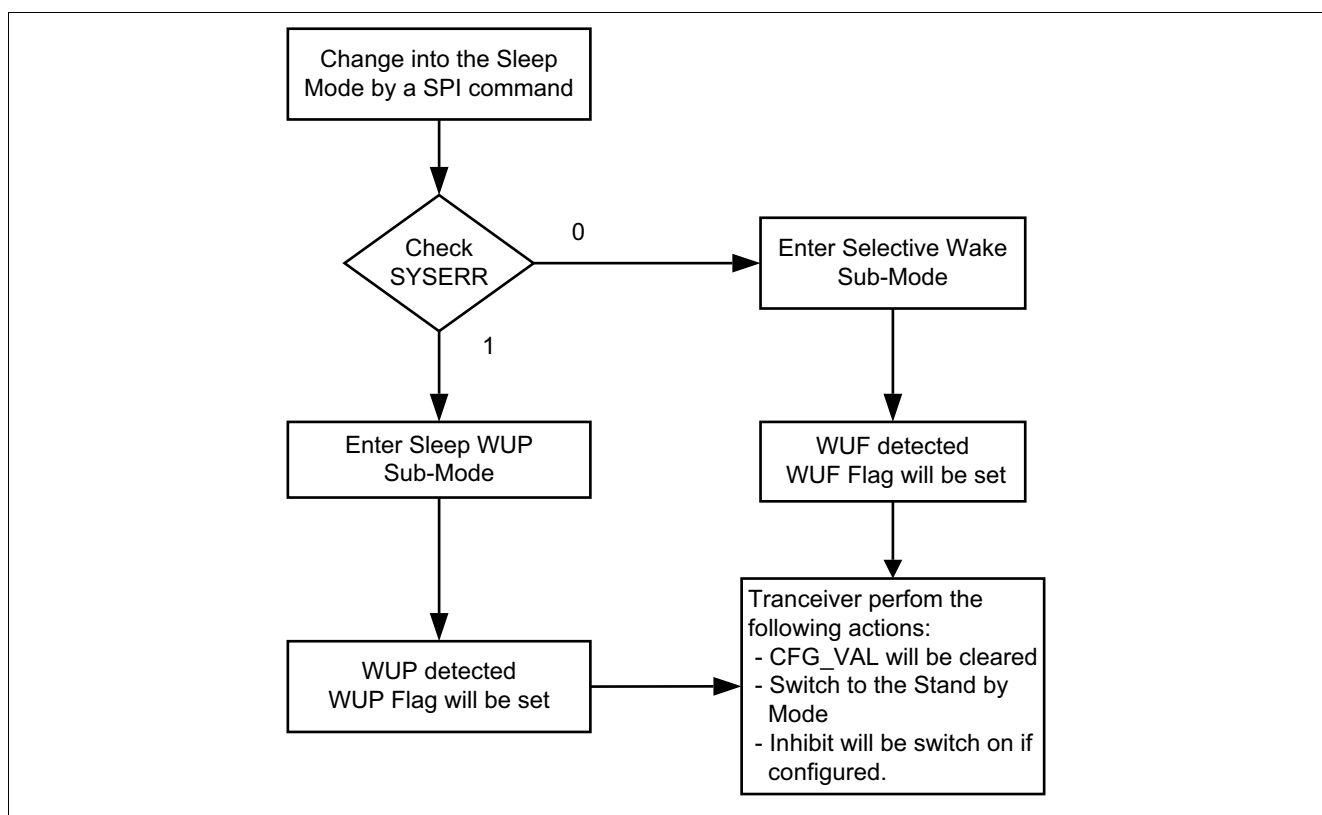
- FDF bit = 1:  
CAN FD frame recognized, decoding stops
- FDF bit = 0:  
classical CAN frame recognized, processing of the frame continues

In this way it is possible to send mixed CAN frame formats without affecting the selective wake functionality by error counter increment and a misleading wake-up. The CAN FD data phase baud rate must be configured in the SPI field **BR\_RATIO** of the register **SWK\_CTRL\_2** to enable detection of CAN FD frames.

## 7.6 Selective wake SPI flags

### 7.6.1 SysErr Flag

The **SysErr** flag in the register **SWK\_STAT** indicates an error condition in the selective wake unit of the TLE9255W. Only if the SPI bit **SWK\_EN** = 1, then the **SysErr** flag is set. The **SysErr** flag does not prevent entering the Sleep Mode by an SPI command. However, the **SysErr** flag determines, whether the TLE9255W enters the Selective Wake Sub-Mode (**SysErr** = 0) or Sleep WUP Mode (**SysErr** = 1). **Figure 41** shows this scenario.



**Figure 41** Impact of SysErr flag if a mode change SPI command to Sleep Mode has been sent

The **SysErr** flag is set under any of the following conditions:

- Selective wake configuration error is detected (see **Chapter 7.4**).
- The frame error counter value is greater than 31.

Only if no configuration error (**CFG\_VAL** = 1) exists AND if the error counter is less than 32, then the TLE9255W resets the **SysErr** flag.

### 7.6.2 SYNC Flag

The **SYNC** flag in the register **SWK\_STAT** indicates that a classical CAN frame is detected correctly by the selective wake unit. The **SYNC** flag works, if all of the following conditions are fulfilled:

- Selective Wake is enabled (**SWK\_EN** Bit = 1)
- After Power on Reset the configuration is confirmed (**CFG\_VAL** Bit = 1) at least once.

## CAN Partial Networking

If the selective wake unit detects an invalid classical CAN frame, then the **SYNC** flag is reset. The **SYNC** flag has no influence on the transition to the Sleep Mode by an SPI command. After power up **SYNC** = 0. The **SYNC** flag is not valid in the Selective Sleep Sub-Mode.

### 7.6.3 CANTO Flag

The **CANTO** flag in the register **SWK\_STAT** indicates that the TLE9255W has entered Selective Sleep Mode (no bus communication) at least once. Only if the SPI bit **SWK\_EN** = 1, then the **CANTO** flag can be set. If the TLE9255W is in the Selective Sleep Mode AND if the  $t_{\text{Silence}}$  timer expires, then the **CANTO** flag is set. Only an SPI command can reset the **CANTO** flag.

### 7.6.4 CANSIL Flag

The **CANSIL** flag in the register **SWK\_STAT** indicates that there is no communication on the CAN bus ( $t_{\text{Silence}}$  timer has expired). **Figure 15** defines the restart conditions for the  $t_{\text{Silence}}$  timer.

### 7.6.5 SWK\_ACTIVE Flag

The **SWK\_ACTIVE** flag in the register **SWK\_STAT** indicates that the TLE9255W is in Selective Wake Sub-Mode. If the TLE9255W enters the Selective Wake Sub-Mode, then the **SWK\_ACTIVE** flag is set. If the TLE9255W exits Sleep Mode, then it resets the **SWK\_ACTIVE** flag.

### 7.6.6 CFG\_VAL Flag

The microcontroller sets the **CFG\_VAL** flag in the register **SWK\_CTRL\_1** to confirm the selective wake configuration. This confirmation must be performed each time before a mode change to Sleep Mode by an SPI command (Selective Wake Sub-Mode) is sent. The TLE9255W resets the **CFG\_VAL** bit under any of the following conditions:

- If a mode change from Selective Wake Sub-Mode to Stand-by Mode is performed.
- If a mode change from Selective Sleep Sub-Mode to Stand-by Mode is performed.
- If a selective wake configuration error is detected (**Chapter 7.4**).

## Serial Peripheral Interface

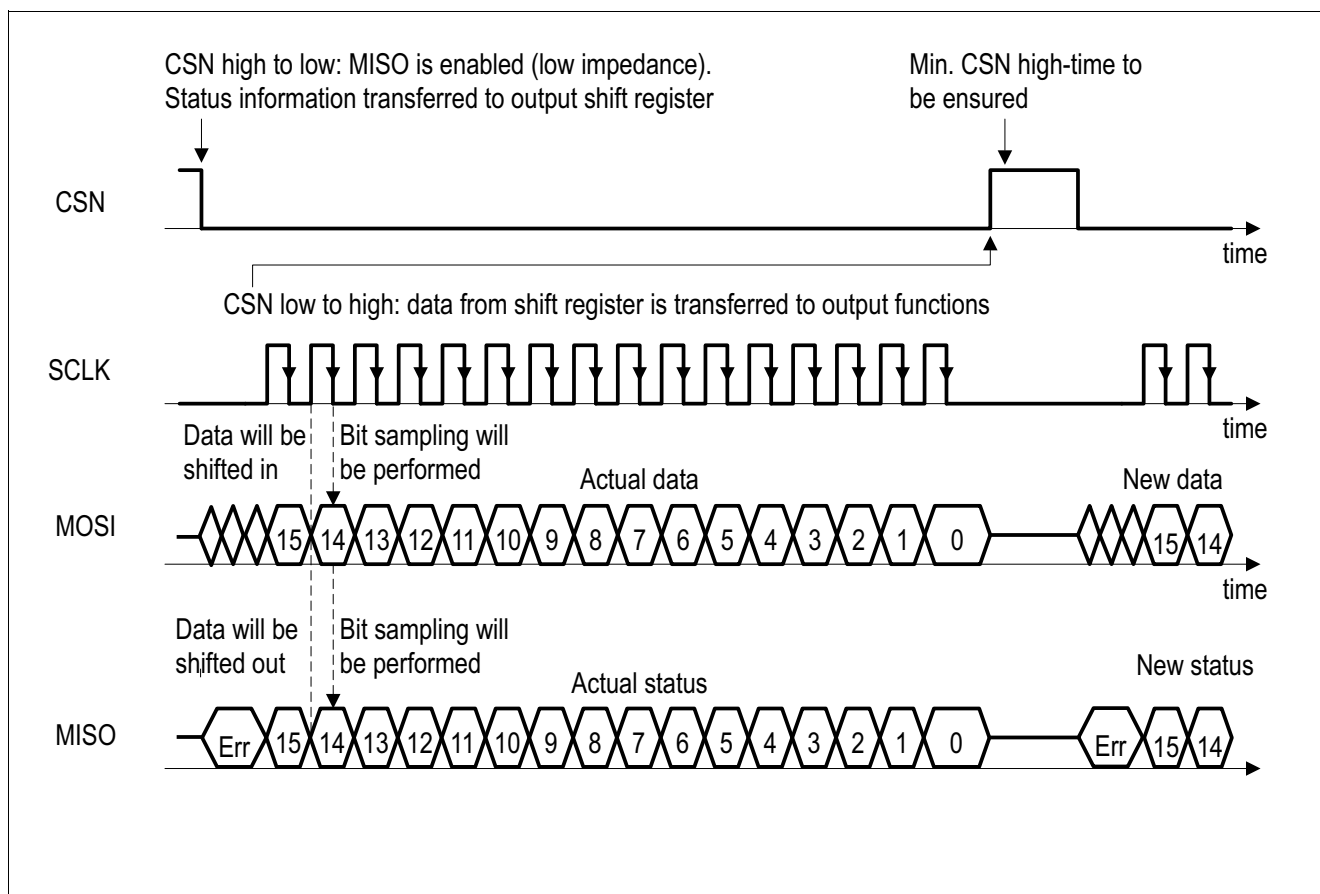
### 8 Serial Peripheral Interface

The communication between the microcontroller and the transceiver is implemented via Serial Peripheral Interface (SPI). This communication is configured as a full duplex multi slave data transfer. A valid SPI command consists of 16 bits.

Only if  $V_{IO} > V_{IO\_UV}$  AND if  $V_{BAT}$  OR  $V_{CC}$  is within the functional range, then SPI communication between the microcontroller and the transceiver can be established. The SPI uses four interface signals for synchronization and data transfer:

- CSN: SPI chip select (active low)
- SCLK: SPI clock
- MOSI: SPI data input
- MISO: SPI data output

**Figure 42** shows the SPI data transfer.



**Figure 42 SPI Data Transfer**

The SPI command transmission cycle begins when the transceiver is selected by the CSN pin (active low). When the signal of the CSN input pin returns from “low” to “high”, the TLE9255W decodes the data that was shifted in on the MOSI. The data of MOSI and MISO is shifted in and out (MSB comes first) on every rising edge of SCLK. The bit sampling is performed on every falling edge of SCLK. If the CSN input pin is “high”, then the MISO pin has a high impedance. The SPI of the transceiver does not support TLE9255W daisy chaining. The MISO pin signals invalid SPI commands ([Chapter 8.5](#)) or SPI failures ([Chapter 8.4](#)). If an invalid SPI

## Serial Peripheral Interface

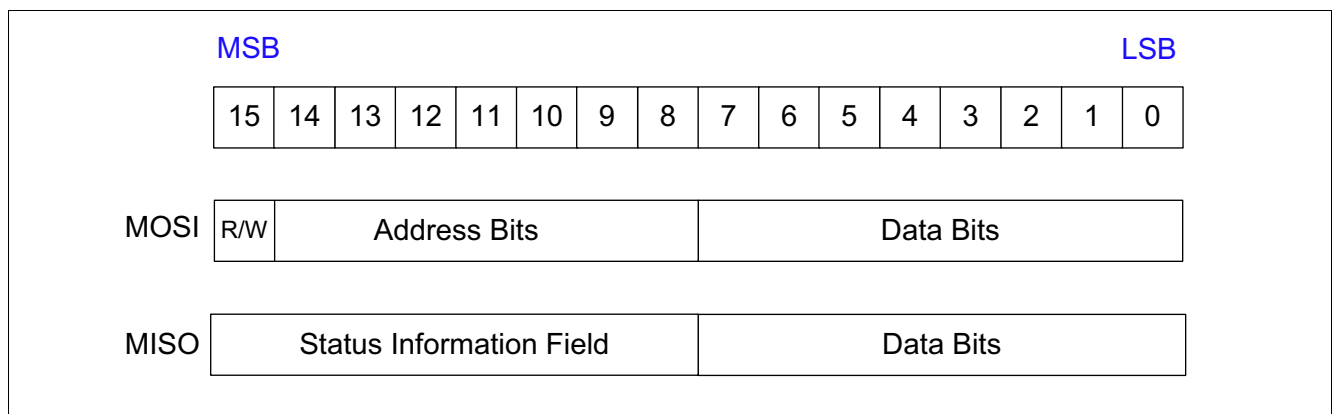
command OR an SPI failure occurs, then the MISO pin is “high” after the CSN pin is “low” and before a clock starts. [Chapter 8.4](#) defines the conditions for an SPI Error.

### 8.1 SPI command format

An SPI command consists of:

- MOSI request format
- MISO response format

[Figure 43](#) shows the SPI command format.



**Figure 43** Command Format of the MOSI and MISO register

#### MOSI Format Frame

The MOSI format frame consists of address bits (Bits 14-8) and data bits (Bits 7-0). The R/W bit (Bit15) defines a write operation (R/W = 1) or a read (R/W = 0) operation to the addressed register. For read operations the data bits are not relevant.

#### MISO Format Frame

The MISO format frame consists of the status information field (Bits 15-8) and the data bits (Bits 7-0). The data bits contain the data of the addressed register. The status information field contains compressed information about the Status Register ([Chapter 8.3](#)).



Serial Peripheral Interface

8.2 Control and Status Register

There are two types of registers:

- Control registers:  
Control the behavior of the TLE9255W, for example mode change and selective wake configuration.
- Status registers:  
Status registers represent the status of the TLE9255W, for example wake events and failures. The TLE9255W controls the bits of the status register. However, the microcontroller must reset some of these bits. Writing “1” clears the register (w1c). In case of reading the register the address bits for the register must be set, the R/W bit must be set to 0 and the data bits are not relevant. Writing a “1” to the specific bits in the status register resets the status bits in the status register. **Figure 44** shows this scenario.

	R/W	Address Bits								Data Bits						
Status Register	-	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1
SPI Command	1	0	0	1	1	0	0	1	0	1	1	0	0	0	0	0
Status Register after SPI Command	-	0	0	1	1	0	0	1	1	0	0	1	0	1	1	1

Figure 44 Read and clear command

## Serial Peripheral Interface

### 8.3 Status Information Field

The Status Information Field informs the microcontroller that status register bits have changed. The Status Information Field is returned during each SPI write or read command in the MISO format frame. Each bit of the Status Information Field represents an OR operation of some bits of a specific status register. If an SPI access occurs while the status register is being updated due to an event, the content of the Status Information Field may not reflect the latest state of the status registers. **Table 4** defines the content of the Status Information Field.

**Table 4** Status Information Field

Name	Bit Position	Reflected Bits
Reserved	0	-
TRANS_UV_STAT (Transceiver undervoltage status)	1	<b>VBAT_UV</b> OR <b>VCC_LTUV</b> OR <b>VCC_STUV</b> OR <b>VIO_LTUV</b> OR <b>VIO_STUV</b>
TEMP_STAT (Temperature status)	2	<b>TSD</b> OR <b>Reserved</b>
WAKE_STAT (Wake-up status)	3	<b>LWU</b> OR <b>WUP</b> OR <b>WUF</b>
TXD_TO (TxD timeout)	4	<b>TXD_TO</b>
CANSIL (CAN Silence)	5	<b>CANSIL</b>
POR (Power on Reset)	6	<b>POR</b>
ERR_STAT (Error status)	7	<b>CMD_ERR</b> or <b>COM_ERR</b>

The ERR\_STAT is flagged on the MISO pin.

### 8.4 SPI Failure

The SPI bit **COM\_ERR** signals an SPI failure. Any of the following conditions define the SPI failure:

- Register address does not exist
- Number of received SPI clocks is neither 0 nor 16

On SPI failure SPI commands are ignored.

### 8.5 Invalid SPI Command

Any attempt to write undefined bit combinations to one of the following SPI registers is an invalid SPI command.

- **Mode** of the register **MODE\_CTRL**
- **TXD\_TO** of the register **TXD\_TO\_CTRL**
- **BR\_RATIO** of the register **SWK\_CTRL\_2**
- **BR** of the register **SWK\_CTRL\_2**
- **VIO\_UV\_T** of the register **SUPPLY\_CTRL**
- **VCC\_UV\_T** of the register **SUPPLY\_CTRL**

An invalid SPI command is ignored and the **CMD\_ERR** bit is set and signalled on the MISO pin. Only the microcontroller can reset the **CMD\_ERR** bit.

Serial Peripheral Interface

8.6 CSN Timeout

The CSN timeout ( $t_{CSN\_TO}$ ) prevents the SPI communication from disturbance. After the CSN pin of the TLE9255W is set to “low” (start of the SPI communication and  $t_{CSN\_TO}$ ) the communication must be finished and the CSN pin must be set to “high” within  $t_{CSN\_TO}$ . If the  $t_{CSN\_TO}$  timeout occurs, then the TLE9255W sets the MISO pin to high impedance. If the CSN pin is set to “high”, then the  $t_{CSN\_TO}$  is reset. **Figure 45** shows this scenario.

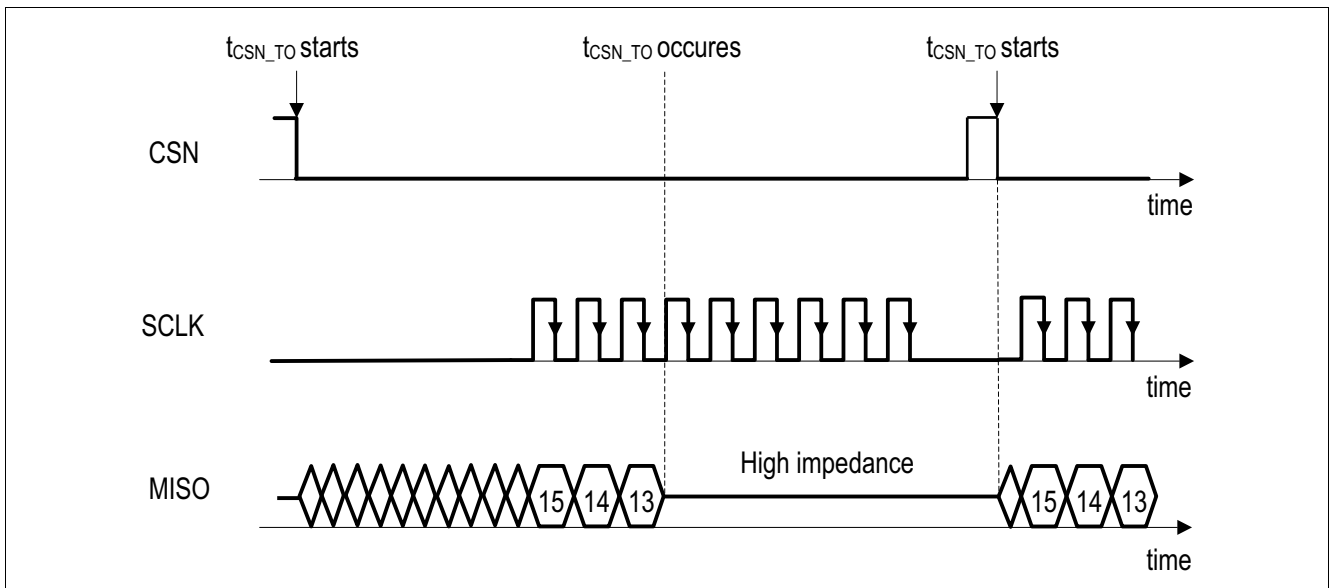


Figure 45 CSN Timeout

8.7 SPI Register

The following figure gives an overview of the SPI register.

Serial Peripheral Interface

Register Short Name	7	6	5	4	3	2	1	0	15	14...8
	Data Bit 15...8								Access Mode	Address A14...A8
<b>CONTROL REGISTERS</b>										
MODE_CTRL	reserved	reserved	reserved	reserved	reserved	reserved	reserved	Mode	read/write	0000001
HW_CTRL	STTS_EN	LWU_NEG	LWU_POS	reserved	reserved	reserved	WAKE_TOG	VBAT_CON	read/write	0000010
TXD_TO_CTRL	reserved	reserved	reserved	reserved	reserved	TXD_TO_2	TXD_TO_1	TXD_TO_0	read/write	0000011
SUPPLY_CTRL	VIO_UV_T_3	VIO_UV_T_2	VIO_UV_T_1	VIO_UV_T_0	VCC_UV_T_3	VCC_UV_T_2	VCC_UV_T_1	VCC_UV_T_0	read/write	0000100
<b>SELECTIVE WAKE REGISTERS</b>										
SWK_CTRL_1	reserved	reserved	reserved	reserved	reserved	reserved	reserved	CFG_VAL	read/write	0000101
SWK_CTRL_2	SWK_EN	reserved	BR_RATIO_1	BR_RATIO_0	reserved	BR_2	BR_1	BR_0	read/write	0000110
SWK_ID3_CTRL	reserved	reserved	IDE	IDE28/ID10	IDE27/ID9	IDE26/ID8	IDE25/ID7	IDE24/ID6	read/write	0000111
SWK_ID2_CTRL	IDE23/ID5	IDE22/ID4	IDE21/ID3	IDE20/ID2	IDE19/ID1	IDE18/ID0	IDE17	IDE16	read/write	0001000
SWK_ID1_CTRL	IDE15	IDE14	IDE13	IDE12	IDE11	IDE10	IDE9	IDE8	read/write	0001001
SWK_ID0_CTRL	IDE7	IDE6	IDE5	IDE4	IDE3	IDE2	IDE1	IDE0	read/write	0001010
SWK_MASK_ID3_CTRL	reserved	reserved	reserved	MASK_ID28	MASK_ID27	MASK_ID26	MASK_ID25	MASK_ID24	read/write	0001011
SWK_MASK_ID2_CTRL	MASK_ID23	MASK_ID22	MASK_ID21	MASK_ID20	MASK_ID19	MASK_ID18	MASK_ID17	MASK_ID16	read/write	0001100
SWK_MASK_ID1_CTRL	MASK_ID15	MASK_ID14	MASK_ID13	MASK_ID12	MASK_ID11	MASK_ID10	MASK_ID9	MASK_ID8	read/write	0001101
SWK_MASK_ID0_CTRL	MASK_ID7	MASK_ID6	MASK_ID5	MASK_ID4	MASK_ID3	MASK_ID2	MASK_ID1	MASK_ID0	read/write	0001110
SWK_DLC_CTRL	reserved	reserved	reserved	reserved	DLC_3	DLC_2	DLC_1	DLC_0	read/write	0001111
SWK_DATA7_CTRL	DATA7_7	DATA7_6	DATA7_5	DATA7_4	DATA7_3	DATA7_2	DATA7_1	DATA7_0	read/write	0010000
SWK_DATA6_CTRL	DATA6_7	DATA6_6	DATA6_5	DATA6_4	DATA6_3	DATA6_2	DATA6_1	DATA6_0	read/write	0010001
SWK_DATA5_CTRL	DATA5_7	DATA5_6	DATA5_5	DATA5_4	DATA5_3	DATA5_2	DATA5_1	DATA5_0	read/write	0010010
SWK_DATA4_CTRL	DATA4_7	DATA4_6	DATA4_5	DATA4_4	DATA4_3	DATA4_2	DATA4_1	DATA4_0	read/write	0010011
SWK_DATA3_CTRL	DATA3_7	DATA3_6	DATA3_5	DATA3_4	DATA3_3	DATA3_2	DATA3_1	DATA3_0	read/write	0010100
SWK_DATA2_CTRL	DATA2_7	DATA2_6	DATA2_5	DATA2_4	DATA2_3	DATA2_2	DATA2_1	DATA2_0	read/write	0010101
SWK_DATA1_CTRL	DATA1_7	DATA1_6	DATA1_5	DATA1_4	DATA1_3	DATA1_2	DATA1_1	DATA1_0	read/write	0010110
SWK_DATA0_CTRL	DATA0_7	DATA0_6	DATA0_5	DATA0_4	DATA0_3	DATA0_2	DATA0_1	DATA0_0	read/write	0010111
<b>STATUS REGISTERS</b>										
TRANS_STAT	POR	reserved	reserved	reserved	reserved	TXD_TO	TSD	reserved	read/clear	0011000
TRANS_UV_STAT	VBAT_UV	reserved	VCC_LTUV	VCC_STUV	reserved	reserved	VIO_LTUV	VIO_STUV	read/clear	0011001
ERR_STAT	reserved	reserved	reserved	reserved	reserved	reserved	COM_ERR	CMD_ERR	read/clear	0011010
WAKE_STAT	reserved	reserved	reserved	reserved	LWU_DIR	LWU	WUP	WUF	read/clear	0011011
<b>SELECTIVE WAKE STATUS REGISTERS</b>										
SWK_STAT	reserved	reserved	reserved	SYSERR	SYNC	CANTO	CANSIL	SWK_ACTIVE	read	0011100
SWK_ECNT_STAT	reserved	reserved	ECNT_5	ECNT_4	ECNT_3	ECNT_2	ECNT_1	ECNT_0	read	0011101

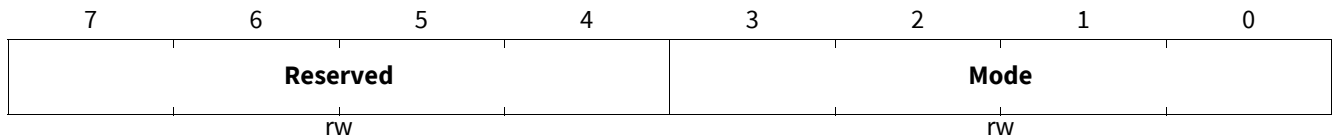
Figure 46 Register overview

## Serial Peripheral Interface

## 8.7.1 Mode Control Register

## MODE\_CTRL

## Mode Control

(01<sub>H</sub>)Reset Value:0002<sub>H</sub>

Field	Bits	Type	Description
Reserved	7:4	rw	Reserved
Mode	3:0	rw	<b>Mode<sup>1)2)</sup></b> 0001 <sub>B</sub> , Sleep Mode 0010 <sub>B</sub> , Standby Mode 0100 <sub>B</sub> , Receive Only Mode 1000 <sub>B</sub> , Normal Operation Mode

1) Internal state transitions have higher priority than mode change SPI commands

2) The Mode bits are a reflection of the state of the transceiver which includes internal state transitions

## HW\_CTRL

## Hardware Control

(02<sub>H</sub>)Reset Value:00E1<sub>H</sub>

Field	Bits	Type	Description
STTS_EN	7	rw	<b>State transition to Sleep WUP Sub-Mode if a <math>V_{CC} &lt; V_{CC\_UV}</math> AND <math>t &gt; t_{VCC\_UV\_T}</math> AND <math>t_{Silence}</math> has expired</b> 0 <sub>B</sub> , State transition will not be performed 1 <sub>B</sub> , State transition will be performed
LWU_NEG	6	rw	<b>Local wake-up direction</b> 0 <sub>B</sub> , Local wake-up will not be performed on the negative edge 1 <sub>B</sub> , Local wake-up will be performed on the negative edge
LWU_POS	5	rw	<b>Local wake-up direction</b> 0 <sub>B</sub> , Local wake-up will not be performed on the positive edge 1 <sub>B</sub> , Local wake-up will be performed on the positive edge
Reserved	4:2	rw	Reserved
WAKE_TOG	1	rw	<b>Toggle RxD Pin if a wake-up event is detected</b> 0 <sub>B</sub> , The RxD Pin will be constant “low” 1 <sub>B</sub> , The RxD Pin will toggle between “low” and “high”

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**Serial Peripheral Interface**

Field	Bits	Type	Description
VBAT_CON	0	rw	<p><b>Transceiver is connected with the battery</b></p> <p>0<sub>B</sub> , INH pin will not be switched off by entering the sleep mode,  <math>V_{BAT\_UV}</math> is disabled            LWU is disabled</p> <p>1<sub>B</sub> , INH pin will be switched off by entering the sleep mode  <math>V_{BAT\_UV}</math> is enabled            LWU is enabled</p>

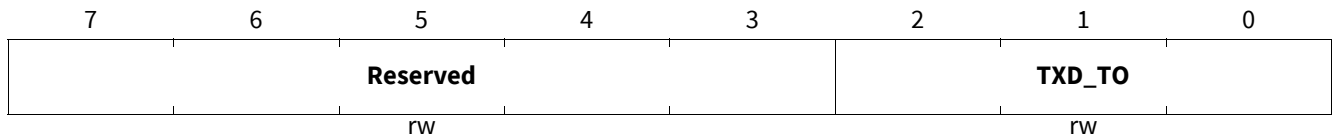
Serial Peripheral Interface

**TXD\_TO\_CTRL**

**TXD Timeout Control**

(03<sub>H</sub>)

Reset Value:0001<sub>H</sub>



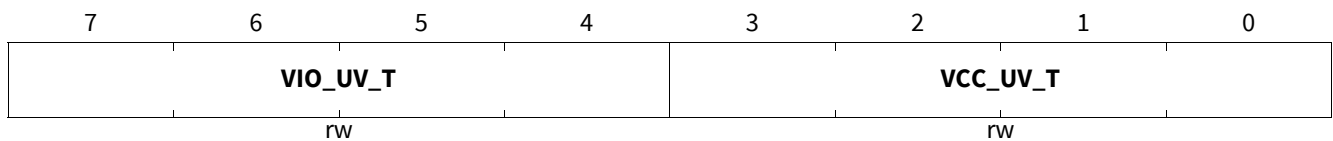
Field	Bits	Type	Description
Reserved	7:3	rw	Reserved
TXD_TO	2:0	rw	<b>TXD Timeout (min - max)</b> 001 <sub>B</sub> , 1 - 4 ms 010 <sub>B</sub> , 2 - 8 ms 011 <sub>B</sub> , 5 - 10 ms 100 <sub>B</sub> , disabled

**SUPPLY\_CTRL**

**Supply Control**

(04<sub>H</sub>)

Reset Value:00CC<sub>H</sub>



Field	Bits	Type	Description
VIO_UV_T	7:4	rw	<b>VIO Undervoltage Detection Timer<sup>1)</sup></b> 0001 <sub>B</sub> , 100 ms 0010 <sub>B</sub> , 200 ms 0011 <sub>B</sub> , 300 ms 0100 <sub>B</sub> , 400 ms 0101 <sub>B</sub> , 500 ms 0110 <sub>B</sub> , 600 ms 0111 <sub>B</sub> , 700 ms 1000 <sub>B</sub> , 800 ms 1001 <sub>B</sub> , 900 ms 1010 <sub>B</sub> , 1000 ms 1011 <sub>B</sub> , 1100 ms 1100 <sub>B</sub> , 1200 ms 1101 <sub>B</sub> , 1300 ms 1110 <sub>B</sub> , 1400 ms 1111 <sub>B</sub> , 1500 ms

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**Serial Peripheral Interface**

Field	Bits	Type	Description
VCC_UV_T	3:0	rw	<b>VCC Undervoltage Detection Timer<sup>1)</sup></b> 0001 <sub>B</sub> , 100 ms 0010 <sub>B</sub> , 200 ms 0011 <sub>B</sub> , 300 ms 0100 <sub>B</sub> , 400 ms 0101 <sub>B</sub> , 500 ms 0110 <sub>B</sub> , 600 ms 0111 <sub>B</sub> , 700 ms 1000 <sub>B</sub> , 800 ms 1001 <sub>B</sub> , 900 ms 1010 <sub>B</sub> , 1000 ms 1011 <sub>B</sub> , 1100 ms 1100 <sub>B</sub> , 1200 ms 1101 <sub>B</sub> , 1300 ms 1110 <sub>B</sub> , 1400 ms 1111 <sub>B</sub> , 1500 ms

1) The derivation of the value can be +/- 40%



Serial Peripheral Interface

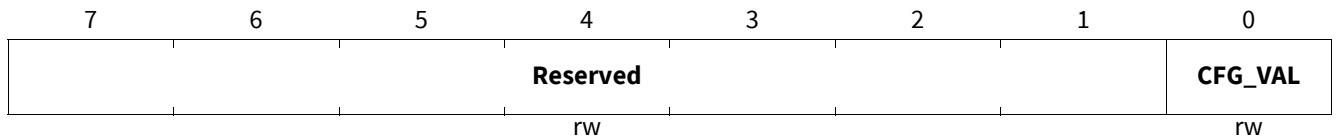
8.7.2 Selective Wake Control Register

SWK\_CTRL\_1

Selective Wake Control

(05<sub>H</sub>)

Reset Value: 0000<sub>H</sub>



Field	Bits	Type	Description
Reserved	7:1	rw	Reserved
CFG_VAL	0	rw	<b>Selective Wake Configuration valid</b> 0 <sub>B</sub> , Invalid 1 <sub>B</sub> , Valid

## Serial Peripheral Interface

## SWK\_CTRL\_2

## Baudrate Control

(06<sub>H</sub>)Reset Value: 0004<sub>H</sub>

7	6	5	4	3	2	1	0
<b>SWK_EN</b>	<b>Reserved</b>	<b>BR_RATIO</b>		<b>Reserved</b>	<b>BR</b>		
rw	rw	rw	rw	rw	rw	rw	rw

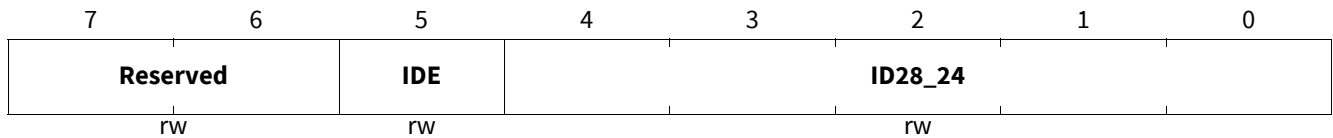
Field	Bits	Type	Description
<b>SWK_EN</b>	7	rw	<b>Selective Wake Unit</b> 0 <sub>B</sub> , Disabled 1 <sub>B</sub> , Enabled
<b>Reserved</b>	6	rw	<b>Reserved</b>
<b>BR_RATIO</b>	5:4	rw	<b>Baudrate ratio from arbitration phase to CAN FD data phase</b> 00 <sub>B</sub> , Ratio <= 4 01 <sub>B</sub> , Ratio <= 10
<b>Reserved</b>	3	rw	<b>Reserved</b>
<b>BR</b>	2:0	rw	<b>Selective Wake Unit Baudrate</b> 010 <sub>B</sub> , 125 kbit/s <sup>1)</sup> 011 <sub>B</sub> , 250 kbit/s 100 <sub>B</sub> , 500 kbit/s 101 <sub>B</sub> , 1 Mbit/s

1) Glitch filter time is 300 ns in case of ratio 4

## Serial Peripheral Interface

## SWK\_ID3\_CTRL

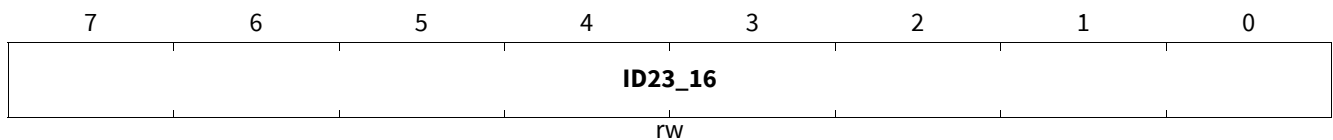
## Identifier 3 Control

(07<sub>H</sub>)Reset Value:001F<sub>H</sub>

Field	Bits	Type	Description
Reserved	7:6	rw	Reserved
IDE	5	rw	<b>Identifier Type</b> 0 <sub>B</sub> , Normal Identifier 1 <sub>B</sub> , Extended Identifier
ID28_24	4:0	rw	<b>Wake-up frame Identifier</b>  <i>Note: If a normal Identifier is configured (IDE = 0) the bits ID28 - ID24 define the normal identifier bits ID10 - ID6</i>

## SWK\_ID2\_CTRL

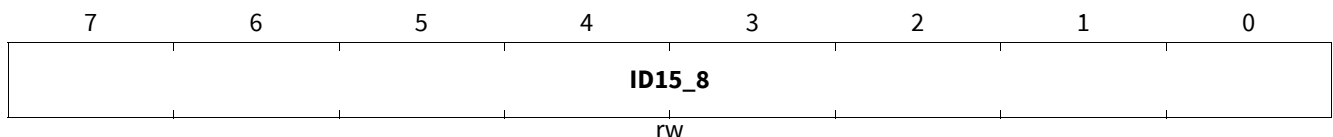
## Identifier 2 Control

(08<sub>H</sub>)Reset Value:00FF<sub>H</sub>

Field	Bits	Type	Description
ID23_16	7:0	rw	<b>Wake-up frame Identifier</b>  <i>Note: If a normal Identifier is configured (IDE = 0) the bits ID23 - ID18 define the normal identifier bits ID5 - ID0</i>

## SWK\_ID1\_CTRL

## Identifier 1 Control

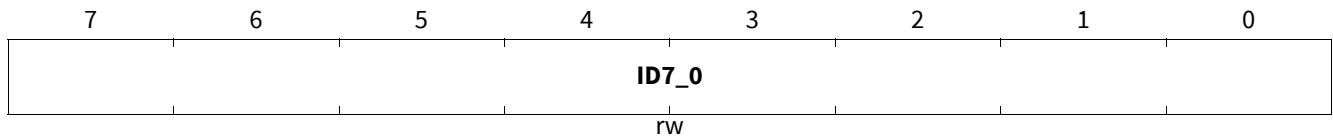
(09<sub>H</sub>)Reset Value:00FF<sub>H</sub>

Field	Bits	Type	Description
ID15_8	7:0	rw	<b>Wake-up frame Identifier</b>

## Serial Peripheral Interface

**SWK\_ID0\_CTRL**

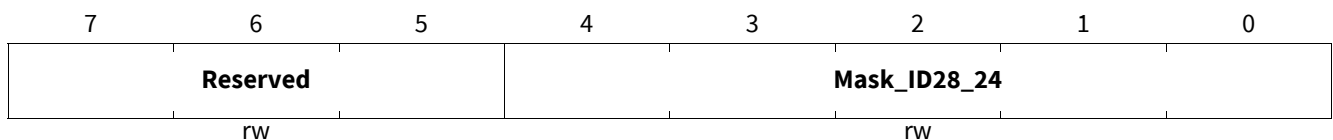
Identifier 0 Control

(0A<sub>H</sub>)Reset Value:00FF<sub>H</sub>

Field	Bits	Type	Description
ID7_0	7:0	rw	Wake-up frame Identifier

**SWK\_MASK\_ID3\_CTRL**

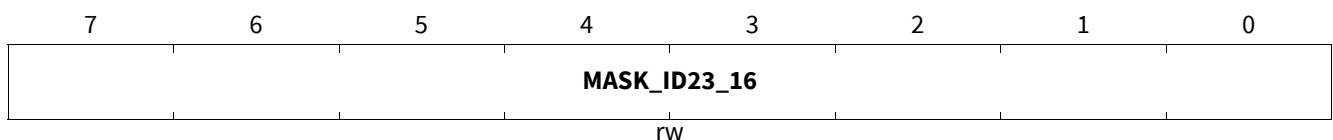
Mask Identifier 3 Control

(0B<sub>H</sub>)Reset Value:0000<sub>H</sub>

Field	Bits	Type	Description
Reserved	7:5	rw	Reserved
Mask_ID28_24	4:0	rw	Mask Identifier

**SWK\_MASK\_ID2\_CTRL**

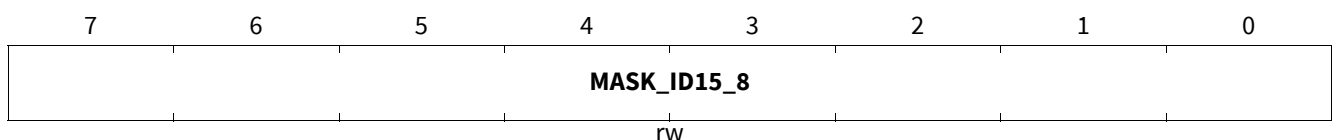
Mask Identifier 2 Control

(0C<sub>H</sub>)Reset Value:0000<sub>H</sub>

Field	Bits	Type	Description
MASK_ID23_16	7:0	rw	Mask Identifier

**SWK\_MASK\_ID1\_CTRL**

Mask Identifier 1 Control

(0D<sub>H</sub>)Reset Value:0000<sub>H</sub>

Field	Bits	Type	Description
MASK_ID15_8	7:0	rw	Mask Identifier

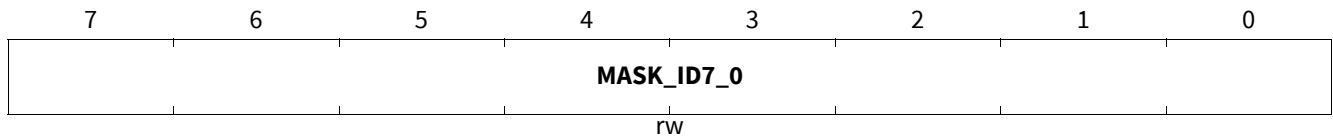
Serial Peripheral Interface

**SWK\_MASK\_ID0\_CTRL**

Mask Identifier 0 Control

(0E<sub>H</sub>)

Reset Value: 0000<sub>H</sub>



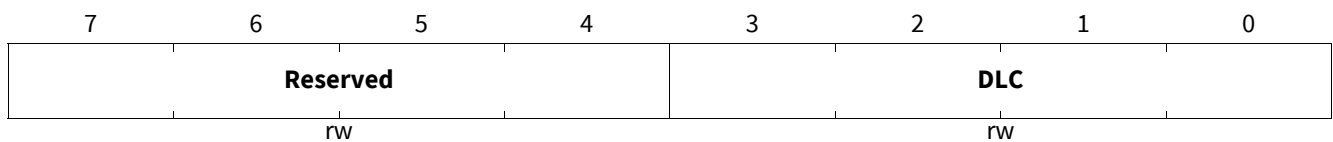
Field	Bits	Type	Description
MASK_ID7_0	7:0	rw	Mask Identifier

**SWK\_DLC\_CTRL**

Data Length Code Control

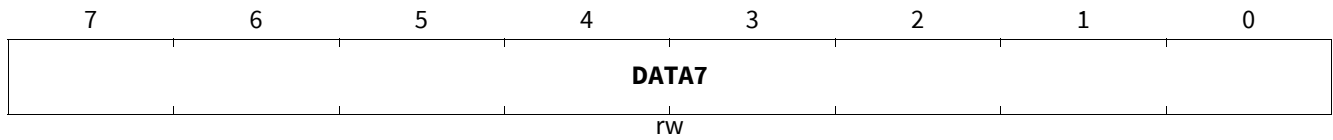
(0F<sub>H</sub>)

Reset Value: 0000<sub>H</sub>

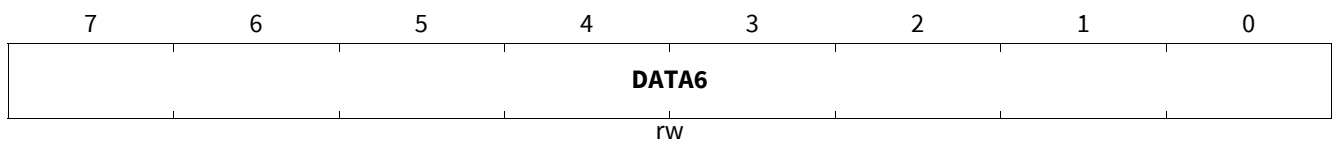


Field	Bits	Type	Description
Reserved	7:4	rw	Reserved
DLC	3:0	rw	<b>Data Length Code</b> 0000 <sub>B</sub> , 0 Data Bytes 0001 <sub>B</sub> , 1 Data Bytes 0010 <sub>B</sub> , 2 Data Bytes 0011 <sub>B</sub> , 3 Data Bytes 0100 <sub>B</sub> , 4 Data Bytes 0101 <sub>B</sub> , 5 Data Bytes 0110 <sub>B</sub> , 6 Data Bytes 0111 <sub>B</sub> , 7 Data Bytes 1000 <sub>B</sub> , 8 Data Bytes 1001 <sub>B</sub> , 8 Data Bytes 1010 <sub>B</sub> , 8 Data Bytes 1011 <sub>B</sub> , 8 Data Bytes 1100 <sub>B</sub> , 8 Data Bytes 1101 <sub>B</sub> , 8 Data Bytes 1110 <sub>B</sub> , 8 Data Bytes 1111 <sub>B</sub> , 8 Data Bytes

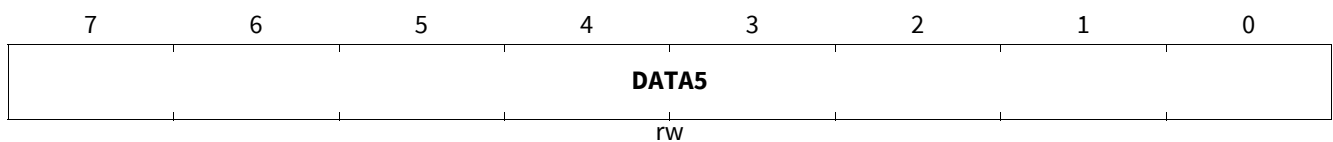
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**Serial Peripheral Interface**
**SWK\_DATA7\_CTRL****Data 7 Control****(10<sub>H</sub>)****Reset Value:0000<sub>H</sub>**

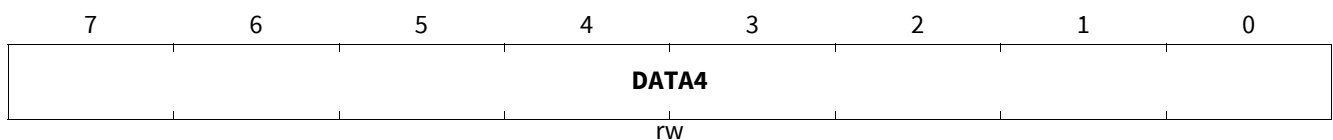
Field	Bits	Type	Description
<b>DATA7</b>	7:0	rw	<b>Data Byte 7</b>

**SWK\_DATA6\_CTRL****Data 6 Control****(11<sub>H</sub>)****Reset Value:0000<sub>H</sub>**

Field	Bits	Type	Description
<b>DATA6</b>	7:0	rw	<b>Data Byte 6</b>

**SWK\_DATA5\_CTRL****Data 5 Control****(12<sub>H</sub>)****Reset Value:0000<sub>H</sub>**

Field	Bits	Type	Description
<b>DATA5</b>	7:0	rw	<b>Data Byte 5</b>

**SWK\_DATA4\_CTRL****Data 4 Control****(13<sub>H</sub>)****Reset Value:0000<sub>H</sub>**

Field	Bits	Type	Description
<b>DATA4</b>	7:0	rw	<b>Data Byte 4</b>

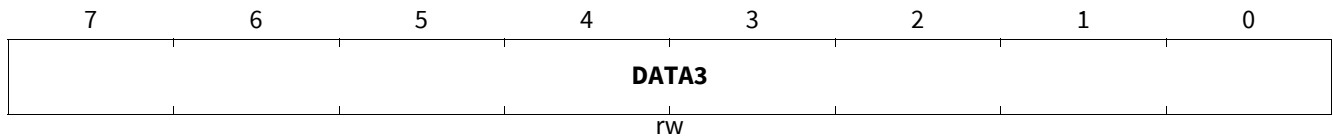
Serial Peripheral Interface

**SWK\_DATA3\_CTRL**

Data 3 Control

(14<sub>H</sub>)

Reset Value:0000<sub>H</sub>



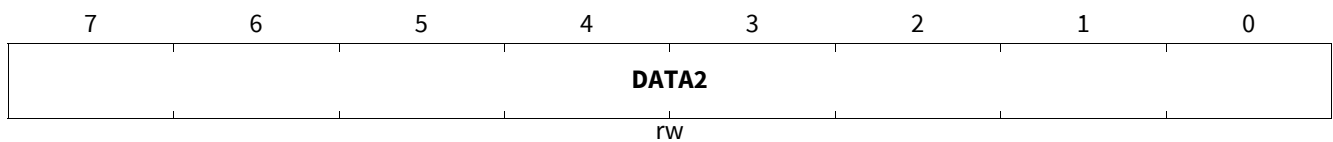
Field	Bits	Type	Description
DATA3	7:0	rw	Data Byte 3

**SWK\_DATA2\_CTRL**

Data 2 Control

(15<sub>H</sub>)

Reset Value:0000<sub>H</sub>



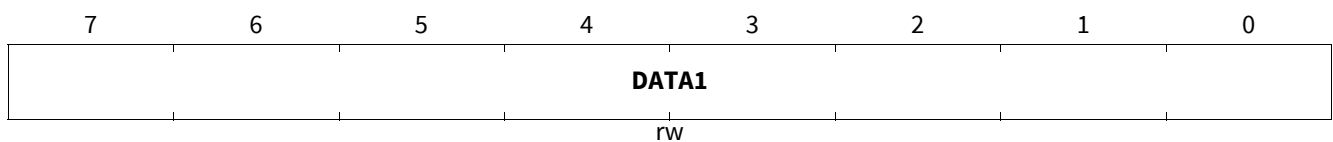
Field	Bits	Type	Description
DATA2	7:0	rw	Data Byte 2

**SWK\_DATA1\_CTRL**

Data 1 Control

(16<sub>H</sub>)

Reset Value:0000<sub>H</sub>



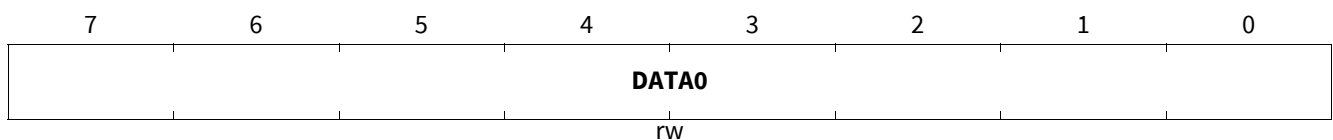
Field	Bits	Type	Description
DATA1	7:0	rw	Data Byte 1

**SWK\_DATA0\_CTRL**

Data 0 Control

(17<sub>H</sub>)

Reset Value:0000<sub>H</sub>



Field	Bits	Type	Description
DATA0	7:0	rw	Data Byte 0

## Serial Peripheral Interface

## 8.7.3 Status Register

## TRANS\_STAT

## Transceiver Status

(18<sub>H</sub>)Reset Value: 0000<sub>H</sub>

7	6	5	4	3	2	1	0
<b>POR</b>	<b>Reserved</b>			<b>TXD_TO</b>		<b>TSD</b>	<b>Reserved</b>
w1c	w1c			w1c		w1c	w1c

Field	Bits	Type	Description
<b>POR</b>	7	w1c	<b>Power On Reset</b> 0 <sub>B</sub> , No POR occurred 1 <sub>B</sub> , POR occurred
<b>Reserved</b>	6:3	w1c	<b>Reserved</b>
<b>TXD_TO</b>	2	w1c	<b>TxD Timeout</b> 0 <sub>B</sub> , No TxD timeout detected 1 <sub>B</sub> , TxD timeout detected
<b>TSD</b>	1	w1c	<b>CAN Thermal Shut Down</b> 0 <sub>B</sub> , No Thermal Shut Down detected 1 <sub>B</sub> , Thermal Shut Down detected
<b>Reserved</b>	0	w1c	<b>Reserved</b>

## TRANS\_UV\_STAT

## Transceiver Undervoltage Status

(19<sub>H</sub>)Reset Value: 0000<sub>H</sub>

7	6	5	4	3	2	1	0
<b>VBAT_UV</b>	<b>Reserved</b>	<b>VCC_LTUV</b>	<b>VCC_STUV</b>	<b>Reserved</b>		<b>VIO_LTUV</b>	<b>VIO_STUV</b>
w1c	w1c	w1c	w1c	w1c		w1c	w1c

Field	Bits	Type	Description
<b>VBAT_UV</b>	7	w1c	<b>Battery Undervoltage detected</b> 0 <sub>B</sub> , No battery undervoltage detected 1 <sub>B</sub> , Battery undervoltage detected
<b>Reserved</b>	6	w1c	<b>Reserved</b>
<b>VCC_LTUV</b>	5	w1c	<b>V<sub>CC</sub> long-term undervoltage detection</b> 0 <sub>B</sub> , No V <sub>CC</sub> long-term undervoltage detected 1 <sub>B</sub> , V <sub>CC</sub> long-term undervoltage detected
<b>VCC_STUV</b>	4	w1c	<b>V<sub>CC</sub> short-term undervoltage detection</b> 0 <sub>B</sub> , No V <sub>CC</sub> short-term undervoltage detected 1 <sub>B</sub> , V <sub>CC</sub> short-term undervoltage detected
<b>Reserved</b>	3:2	w1c	<b>Reserved</b>



## Serial Peripheral Interface

Field	Bits	Type	Description
VIO_LTUV	1	w1c	<b>V<sub>IO</sub> long-term undervoltage detection</b> 0 <sub>B</sub> , No V <sub>IO</sub> long-term undervoltage detected 1 <sub>B</sub> , V <sub>IO</sub> long-term undervoltage detected
VIO_STUV	0	w1c	<b>V<sub>IO</sub> short-term undervoltage detection</b> 0 <sub>B</sub> , No V <sub>IO</sub> short-term undervoltage detected 1 <sub>B</sub> , V <sub>IO</sub> short-term undervoltage detected

## ERR\_STAT

## Error Status

(1A<sub>H</sub>)Reset Value:0000<sub>H</sub>

7	6	5	4	3	2	1	0
Reserved						COM_ERR	CMD_ERR
w1c						w1c	w1c

Field	Bits	Type	Description
Reserved	7:2	w1c	Reserved
COM_ERR	1	w1c	<b>SPI failure detected (Chapter 8.4)</b> 0 <sub>B</sub> , No SPI failure detected 1 <sub>B</sub> , SPI failure detected
CMD_ERR	0	w1c	<b>Invalid SPI Command (Chapter 8.5)</b> 0 <sub>B</sub> , No invalid SPI command received 1 <sub>B</sub> , Invalid SPI command received

## WAKE\_STAT

## Wake Status

(1B<sub>H</sub>)Reset Value:0000<sub>H</sub>

7	6	5	4	3	2	1	0
Reserved				LWU_DIR	LWU	WUP	WUF
w1c				r	w1c	w1c	w1c

Field	Bits	Type	Description
Reserved	7:4	w1c	Reserved
LWU_DIR	3	r	<b>Local Wake-Up Direction</b> 0 <sub>B</sub> , Local Wake-Up has been performed by the falling edge 1 <sub>B</sub> , Local Wake-Up has been performed by the rising edge
LWU	2	w1c	<b>Local Wake-Up</b> 0 <sub>B</sub> , No Local Wake-Up performed 1 <sub>B</sub> , Local Wake-Up performed
WUP	1	w1c	<b>Wake-Up Pattern</b> 0 <sub>B</sub> , No Wake-Up Pattern detected 1 <sub>B</sub> , Wake-Up Pattern detected

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**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>WUF</b>	0	w1c	<b>Wake-Up Frame</b> 0 <sub>B</sub> , No Wake-Up Frame detected 1 <sub>B</sub> , Wake-Up Frame detected

## Serial Peripheral Interface

**SWK\_STAT****Selective Wake Status****(1C<sub>H</sub>)****Reset Value:0002<sub>H</sub>**

7	6	5	4	3	2	1	0
<b>Reserved</b>			<b>SysErr</b>	<b>SYNC</b>	<b>CANTO</b>	<b>CANSIL</b>	<b>SWK_ACTIVE</b>
w1c			r	r	w1c	r	r

Field	Bits	Type	Description
<b>Reserved</b>	7:5	w1c	<b>Reserved</b>
<b>SysErr</b>	4	r	<b>System Error</b> 0 <sub>B</sub> , No System Error detected 1 <sub>B</sub> , System Error detected
<b>SYNC</b>	3	r	<b>Synchronisation of the Selective Wake Unit</b> 0 <sub>B</sub> , SWK Unit is not synchronous to the CAN bit stream 1 <sub>B</sub> , SWK Unit is synchronous to the CAN bit stream
<b>CANTO</b>	2	w1c	<b>CAN Timeout</b> 0 <sub>B</sub> , Transceiver has not entered the Selective Sleep Sub-Mode 1 <sub>B</sub> , Transceiver has entered the Selective Sleep Sub-Mode at least once in Sleep Mode
<b>CANSIL</b>	1	r	<b>CAN Silence</b> 0 <sub>B</sub> , Transceiver is not in the Selective Sleep Mode 1 <sub>B</sub> , Transceiver is in the Selective Sleep Mode (No CAN bus communication)
<b>SWK_ACTIVE</b>	0	r	<b>Selective Wake</b> 0 <sub>B</sub> , Transceiver is not in the Selective Wake Mode 1 <sub>B</sub> , Transceiver is in the Selective Wake Mode

**SWK\_ECNT\_STAT****Error Counter Status****(1D<sub>H</sub>)****Reset Value:0000<sub>H</sub>**

7	6	5	4	3	2	1	0
<b>Reserved</b>			<b>ECNT</b>				
r			r				

Field	Bits	Type	Description
<b>Reserved</b>	7:6	r	<b>Reserved</b>
<b>ECNT</b>	5:0	r	<b>Error Counter Value</b>

## General Product Characteristics

# 9 General Product Characteristics

## 9.1 Absolute Maximum Ratings

**Table 5 Absolute Maximum Ratings<sup>1)</sup>**

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Battery supply voltage	$V_{BAT}$	-0.3	–	40	V	–	P_9.1.1
Transmitter supply voltage	$V_{CC}$	-0.3	–	6.0	V	–	P_9.1.2
Digital voltage reference	$V_{IO}$	-0.3	–	6.0	V	–	P_9.1.3
CANH DC voltage versus GND	$V_{CANH}$	-40	–	40	V	–	P_9.1.4
CANL DC voltage versus GND	$V_{CANL}$	-40	–	40	V	–	P_9.1.5
Differential voltage between CANH and CANL	$V_{CAN\_DIFF}$	-40	–	40	V	–	P_9.1.6
Voltage at pin WAKE	$V_{WAKE}$	-27	–	40	V	–	P_9.1.7
Voltage at pin INH	$V_{INH}$	-0.3	–	$V_{BAT} + 0.3$	V	–	P_9.1.8
Voltage at pin digital input pins: CSN, SCLK, MOSI, TxD	$V_{Max\_In}$	-0.3	–	$V_{IO} + 0.3$	V	–	P_9.1.9
Voltage at pin digital output pins: MISO, RxD	$V_{Max\_Out}$	-0.3	–	$V_{IO} + 0.3$	V	–	P_9.1.10
<b>Currents</b>							
Maximum output current on INH	$I_{INH\_Max}$	-1.0	–	–	mA	–	P_9.1.11
Maximum output current on digital output pins: MISO, RxD	$I_{Out\_Max}$	-20	–	20	mA	–	P_9.1.12
<b>Temperatures</b>							
Junction Temperature	$T_j$	-40	–	150	°C	–	P_9.1.13
Storage Temperature	$T_{stg}$	-55	–	150	°C	–	P_9.1.14

## General Product Characteristics

**Table 5 Absolute Maximum Ratings<sup>1)</sup>** (cont'd)

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>ESD Resistivity</b>							
ESD immunity at CANH, CANL, WAKE and $V_{BAT}$ versus to GND	$V_{ESD\_HBM\_CAN}$	-10	–	10	kV	HBM <sup>2)</sup>	P_9.1.15
ESD immunity at all other pins	$V_{ESD\_HBM}$	-4	–	4	kV	HBM <sup>2)</sup>	P_9.1.16
ESD immunity at corner pins	$V_{ESD\_CDM\_CP}$	-750	–	750	V	CDM <sup>3)</sup>	P_9.1.17
ESD immunity at any pin	$V_{ESD\_CDM\_OP}$	-500	–	500	V	CDM <sup>3)</sup>	P_9.1.18

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS001 (1.5k  $\Omega$ , 100 pF.)

3) ESD susceptibility, Charged Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM 5.3.1.

### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

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**General Product Characteristics**
**9.2 Functional Range**
**Table 6 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Supply Voltages</b>							
Transceiver battery supply voltage	$V_{BAT}$	5.5	–	40	V	–	P_9.2.1
Transmitter supply voltage	$V_{CC}$	4.75	–	5.25	V	–	P_9.2.2
Digital voltage reference	$V_{IO}$	3.0	–	5.5	V	–	P_9.2.3
<b>Thermal Parameters</b>							
Junction Temperature	$T_j$	-40	–	150	°C	–	P_9.2.4

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

## General Product Characteristics

### 9.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information please visit [www.jedec.org](http://www.jedec.org).

**Table 7 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Thermal Resistance</b>							
Junction to ambient	$R_{thJA\_DSO14}$	–	130	–	K/W	<sup>2)</sup>	P_9.3.1
<b>Thermal Shutdown Junction Temperature</b>							
Thermal shut-down temperature	$T_{JSD}$	170	180	190	°C	–	P_9.3.3
Thermal shutdown hysteresis	$\Delta T$	5	10	20	K	–	P_9.3.4

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu).

## Electrical Characteristics

# 10 Electrical Characteristics

## 10.1 General Timing Parameter

**Table 8** General Timing Parameter

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power up delay time	$t_{PON}$	–	–	1	ms	–	P_10.1.1
Delay time for mode change	$t_{Mode\_Change}$	–	–	20	$\mu$ s	–	P_10.1.2
CAN Bus Silence timeout	$t_{Silence}$	0.6	–	1.2	s	–	P_10.1.3

## 10.2 Power Supply Interface

### 10.2.1 Current Consumption

**Table 9** Current Consumption

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Normal-operating Mode</b>							
$V_{BAT}$ supply current	$I_{BAT\_NM}$	–	0.8	1.3	mA	INH = not connected;	P_10.2.1
$V_{CC}$ supply current dominant bus signal	$I_{CC\_NM\_D}$	–	35	45	mA	–	P_10.2.2
$V_{CC}$ supply current recessive bus signal	$I_{CC\_NM\_R}$	–	0.9	4.0	mA	–	P_10.2.3
$V_{IO}$ supply current	$I_{IO\_NM}$	–	0.2	0.5	mA	–	P_10.2.4
<b>Receive-only Mode</b>							
$V_{BAT}$ and $V_{CC}$ supply current $I_{BAT\_CC\_ROM} = I_{BAT} + I_{CC}$	$I_{BAT\_CC\_ROM}$	–	0.9	1.3	mA	INH = not connected;	P_10.2.5
$V_{CC}$ supply current	$I_{CC\_ROM}$	–	0.8	1.3	mA	$V_{BAT}$ = not connected;	P_10.2.6
$V_{IO}$ supply current	$I_{IO\_ROM}$	–	2	20	$\mu$ A	–	P_10.2.7



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**Table 9 Current Consumption** (cont'd)

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Stand-by Mode</b>							
$V_{BAT}$ and $V_{CC}$ supply current $I_{BAT\_CC\_STB} = I_{BAT} + I_{CC}$	$I_{BAT\_CC\_STB}$	–	260	320	$\mu\text{A}$	$T_J = 85^\circ$ , INH = not connected, WAKE pin = GND, SPI Bit <b>SWK_EN</b> = "0", No CAN Bus communication;	P_10.2.8
$V_{BAT}$ and $V_{CC}$ supply current $I_{BAT\_CC\_STB} = I_{BAT} + I_{CC}$	$I_{BAT\_CC\_STB}$	–	300	365	$\mu\text{A}$	INH = not connected, WAKE pin = GND, SPI Bit <b>SWK_EN</b> = "0", No CAN Bus communication;	P_10.2.21
$V_{CC}$ supply current	$I_{CC\_STB}$	–	260	320	$\mu\text{A}$	$T_J = 85^\circ$ , $V_{BAT}$ = not connected, WAKE pin = GND, SPI Bit <b>SWK_EN</b> = "0", No CAN Bus communication;	P_10.2.9
$V_{CC}$ supply current	$I_{CC\_STB}$	–	300	365	$\mu\text{A}$	$V_{BAT}$ = not connected, WAKE pin = GND, SPI Bit <b>SWK_EN</b> = "0", No CAN Bus communication;	P_10.2.38
$V_{IO}$ supply current	$I_{IO\_STB}$	–	2.0	5.0	$\mu\text{A}$	–	P_10.2.10
<b>Sleep WUP Sub-Mode</b>							
<b>Selective-sleep Sub-Mode</b>							
$V_{BAT}$ supply current	$I_{BAT\_SLP}$	–	18.0	30.0	$\mu\text{A}$	$V_{CC} = V_{IO} = 0\text{ V}$ , bus biasing = GND, INH = not connected, $5.5\text{ V} < V_{BAT} < 18\text{ V}$ , $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ;	P_10.2.11

## Electrical Characteristics

**Table 9 Current Consumption** (cont'd)

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
$V_{BAT}$ supply current	$I_{BAT\_SLP}$	–	12.0	20.0	$\mu\text{A}$	$V_{CC} = V_{IO} = 0\text{ V}$ , bus biasing = GND, INH = not connected, $5.5\text{ V} < V_{BAT} < 18\text{ V}$ , $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$ ;	P_10.2.35
$V_{CC}$ supply current	$I_{CC\_SLP}$	–	0.3	5.0	$\mu\text{A}$	CSN, TxD = $V_{IO}$ , MOSI, SCLK = GND, $V_{BAT} = 12\text{ V}$ ;	P_10.2.12
$V_{IO}$ supply current	$I_{IO\_SLP}$	–	2.0	5.0	$\mu\text{A}$	CSN, TxD = $V_{IO}$ , MOSI, SCLK = GND;	P_10.2.13

## Electrical Characteristics

**Table 9 Current Consumption (cont'd)**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40 \text{ }^\circ\text{C} < T_J < 150 \text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Selective-wake mode</b>							
$V_{BAT}$ supply current	$I_{BAT\_SEL\_WK}$	–	590	705	$\mu\text{A}$	$V_{CC} = V_{IO} = 0 \text{ V}$ , INH = not connected, 500 kbit/s with 100% bus load, Classical CAN Frame: Id = 0x4C7 DLC = 3 Data = 0xC7, 0x8E, 0x68;	P_10.2.14
$V_{BAT}$ supply current	$I_{BAT\_SEL\_WK}$	–	550	650	$\mu\text{A}$	$V_{CC} = V_{IO} = 0 \text{ V}$ , $T_J = 85 \text{ }^\circ\text{C}$ , INH = not connected, 500 kbit/s with 100% bus load, Classical CAN Frame: Id = 0x4C7 DLC = 3 Data = 0xC7, 0x8E, 0x68;	P_10.2.39
$V_{CC}$ supply current	$I_{CC\_SEL\_WK}$	–	0.4	5.0	$\mu\text{A}$	CSN, TxD = $V_{IO}$ , MOSI, SCLK = GND, $V_{BAT} = 12 \text{ V}$ ;	P_10.2.16
$V_{IO}$ supply current	$I_{IO\_SEL\_WK}$	–	2.0	5.0	$\mu\text{A}$	CSN, TxD = $V_{IO}$ , MOSI, SCLK = GND;	P_10.2.17

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### 10.2.2 Undervoltage Detection

**Table 10 Undervoltage Detection**

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Undervoltage Detection <math>V_{BAT}</math></b>							
Undervoltage detection threshold	$V_{BAT\_UV}$	4.2	5.0	5.5	V	1)	P_10.2.18
Power down threshold	$V_{BAT\_POD}$	3	4.0	4.4	V	1), falling edge, $V_{CC} = 0\text{ V}$ ;	P_10.2.20
Undervoltage glitch filter	$t_{VBAT\_filter}$	1	–	400	$\mu\text{s}$	(see <a href="#">Figure 24</a> )	P_10.2.22
<b>Undervoltage Detection <math>V_{CC}</math></b>							
Undervoltage detection threshold	$V_{CC\_UV}$	4.5	4.65	4.75	V	–	P_10.2.23
Power down threshold	$V_{CC\_POD}$	2.5	3	4.0	V	falling edge, $V_{BAT} = 0\text{ V}$ ;	P_10.2.25
Undervoltage glitch filter	$t_{VCC\_filter}$	1	–	10	$\mu\text{s}$	(see <a href="#">Figure 26</a> )	P_10.2.27
Transmitter recovery time	$t_{VCC\_recovery}$			20	$\mu\text{s}$	(see <a href="#">Figure 26</a> )	P_10.2.36
Response time $V_{CC}$ for long-term undervoltage detection	$t_{VCC\_UV\_T}$	$0.6 \times V_{CC\_UV\_T}$	–	$1.4 \times V_{CC\_UV\_T}$		Adjustable by SPI bit <b>VCC_UV_T</b> (see <a href="#">Figure 28</a> and <a href="#">Figure 29</a> )	P_10.2.28
<b>Undervoltage Detection <math>V_{IO}</math></b>							
Undervoltage detection threshold	$V_{IO\_UV}$	2.4	2.6	3.0	V	–	P_10.2.29
Undervoltage glitch filter	$t_{VIO\_filter}$	1	–	10	$\mu\text{s}$	(see <a href="#">Figure 30</a> )	P_10.2.31
Transmitter recovery time	$t_{VIO\_recovery}$			20	$\mu\text{s}$	(see <a href="#">Figure 30</a> )	P_10.2.37
Response time $V_{IO}$ for long-term undervoltage detection	$t_{VIO\_UV\_T}$	$0.6 \times V_{IO\_UV\_T}$	–	$1.4 \times V_{IO\_UV\_T}$		Adjustable by SPI field <b>VIO_UV_T</b> (see <a href="#">Figure 32</a> and <a href="#">Figure 33</a> )	P_10.2.32

1) The design of the TLE9255W guarantees that the  $V_{Bat}$  powerdown threshold is below the  $V_{Bat}$  undervoltage threshold

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### 10.2.3 INH Output

**Table 11 INH Output**

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Analog Output INH</b>							
Output voltage INH enabled	$V_{INH}$	$V_{BAT} - 0.8$	-	-	V	$I_{INH} = -0.2\text{ mA}$ , Normal-operating Mode Receive-only Mode Stand-by Mode;	P_10.2.33
Absolute leakage current	$I_{INH\_Leak}$	-5.0	-	-	$\mu\text{A}$	$V_{INH} = 0\text{ V}$ , Sleep Mode;	P_10.2.34

### 10.3 CAN Controller Interface

**Table 12 CAN Controller Interface**

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $t_{Bit(min)} = 500\text{ ns}$ ;  $t_{Bit(Flash)} = 200\text{ ns}$ ;  
 $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Receiver Output RxD</b>							
“high” level output current	$I_{RxD\_H}$	-	-1.8	-1.0	mA	$V_{RxD} = V_{IO} - 0.4\text{ V}$ , $V_{Diff} < 0.5\text{ V}$ ;	P_10.3.1
“low” level output current	$I_{RxD\_L}$	1.0	1.8	-	mA	$V_{RxD} = 0.4\text{ V}$ , $V_{Diff} > 0.9\text{ V}$ ;	P_10.3.2
RxD toggling time after wake-up event	$t_{Toggle}$	6	-	14	ms	see <a href="#">Chapter 5.8.2</a>	P_10.3.6
<b>Transmitter Input TxD</b>							
“high” level input voltage threshold	$V_{TxD\_H}$	-	$0.5 \times V_{IO}$	$0.7 \times V_{IO}$	V	recessive state;	P_10.3.7
“low” level input voltage threshold	$V_{TxD\_L}$	$0.3 \times V_{IO}$	$0.4 \times V_{IO}$	-	V	dominant state;	P_10.3.8
“high” level input current	$I_{TxD\_H}$	-2.0	-	2.0	$\mu\text{A}$	$V_{TxD} = V_{IO}$ ;	P_10.3.10
“low” level input current	$I_{TxD\_L}$	-220	-	-20.0	$\mu\text{A}$	$V_{TxD} = 0\text{ V}$ ;	P_10.3.11

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**Table 12 CAN Controller Interface** (cont'd)

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $t_{\text{Bit}(\text{min})} = 500\text{ ns}$ ;  $t_{\text{Bit}(\text{Flash})} = 200\text{ ns}$ ;  
 $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TxD permanent dominant timeout	$t_{\text{TxD\_TO}}$	1	–	4	ms	Default value is 001 <sub>B</sub> in TXD_TO_CTRL Adjustable by SPI register <b>TXD_TO_CTRL</b>	P_10.3.12
Input capacitance	$C_{\text{TxD}}$	–	–	10	pF	<sup>1)</sup>	P_10.3.13

1) Not subject to production test, specified by design.

## Electrical Characteristics

### 10.4 Transmitter and Receiver

#### 10.4.1 Transmitter

**Table 13 Transmitter**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Bus Transmitter</b>							
CANH, CANL recessive output voltage	$V_{CANL/H}$	2.0	2.5	3.0	V	Normal-operating Mode, Receive-only Mode, Selective Wake Sub-Mode;	P_10.4.1
CANH, CANL recessive output voltage difference	$V_{Diff\_R\_NM} = V_{CANH} - V_{CANL}$	-500	-	50	mV	$V_{TXD} = V_{IO}$ , no load;	P_10.4.2
CANH dominant output voltage Normal-operating Mode	$V_{CANH}$	2.75	-	4.5	V	$V_{TXD} = 0\text{ V}$ , $50 \Omega < R_L < 65 \Omega$ ;	P_10.4.3
CANL dominant output voltage Normal-operating Mode	$V_{CANL}$	0.5	-	2.25	V	$V_{TXD} = 0\text{ V}$ , $50 \Omega < R_L < 65 \Omega$ ;	P_10.4.4
CANH dominant output voltage difference: $V_{Diff\_D} = V_{CANH} - V_{CANL}$ Normal-operating Mode	$V_{Diff\_D}$	1.5	2.0	3.0	V	$V_{TXD} = 0\text{ V}$ , $50 \Omega < R_L < 65 \Omega$ ;	P_10.4.5
CANH dominant output voltage difference extended bus load $V_{Diff\_D} = V_{CANH} - V_{CANL}$ Normal-operating Mode	$V_{Diff\_D\_EXT\_BL}$	1.4	-	3.3	V	$V_{TXD} = 0\text{ V}$ , $R_L = 45 \Omega < R_L < 70 \Omega$	P_10.4.6
CANH, CANL dominant output voltage difference high extended bus load Normal-operating mode $V_{Diff} = V_{CANH} - V_{CANL}$	$V_{Diff\_D\_HEXT\_BL}$	1.5	-	5.0	V	$V_{TXD} = 0\text{ V}$ , $R_L = 2240 \Omega^1$ ;	P_10.4.7

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**Table 13 Transmitter** (cont'd)

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40 \text{ }^\circ\text{C} < T_J < 150 \text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH, CANL recessive output voltage Sleep WUP Sub-Mode, Selective sleep Sub-Mode	$V_{CANL\_H}$	-0.1	–	0.1	V	no load;	P_10.4.10
CANH, CANL recessive output voltage difference Sleep WUP Sub-Mode, Selective sleep Sub-Mode	$V_{Diff\_SLP}$	-0.2	–	0.2	V	no load;	P_10.4.11
Driver symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	$V_{SYM}$	0.9 x $V_{CC}$	1.0 x $V_{CC}$	1.1 x $V_{CC}$	V	Split termination, $R_L = 60 \text{ Ohm}$ , $C = 4.7 \text{ nF}$ , 1)2)	P_10.4.12
CANH short circuit current	$I_{CANHSC}$	115	-	-115	mA	$-3 \leq V_{CAN} \leq 18 \text{ V}$ , $t < \mathbf{TXD\_TO}$ , $V_{TXD} = 0 \text{ V}$ ;	P_10.4.13
CANL short circuit current	$I_{CANLSC}$	-115	-	115	mA	$-3 \leq V_{CAN} \leq 18 \text{ V}$ , $t < \mathbf{TXD\_TO}$ , $V_{TXD} = 0 \text{ V}$ ;	P_10.4.14
Leakage current CANH	$I_{CANH\_Ik}$	-5	–	5	$\mu\text{A}$	$V_{CC} = V_{IO} = V_{BAT} = 0 \text{ V}^3)$ , $0 \text{ V} < V_{CANH} < 5 \text{ V}$ ; $V_{CANH} = V_{CANL}$ ;	P_10.4.16
Leakage current CANL	$I_{CANL\_Ik}$	-5	–	5	$\mu\text{A}$	$V_{CC} = V_{IO} = V_{BAT} = 0 \text{ V}^3)$ , $0 \text{ V} < V_{CANL} < 5 \text{ V}$ ; $V_{CANH} = V_{CANL}$ ;	P_10.4.17

1) Not subject to production test, specified by design

2)  $V_{SYM}$  shall be observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TxD is stimulated by a square wave signal with a frequency of 62,5 kHz (125 kbit/s), 125 kHz (250 kbit/s), 250 kHz (500 kbit/s), 500 kHz (1 Mbit/s), 1 MHz (2 Mbit/s), 2,5 MHz (5 Mbit/s)

3) Additional requirement  $V_{IO} = V_{CC}$  connected via 47 k $\Omega$  to GND



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### 10.4.2 Receiver

**Table 14 Receiver**

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Bus Receiver</b>							
Common Mode Range	$V_{CMR}$	-12	-	12	V	-	P_10.4.18
Differential range dominant Normal-operating Mode Receive-only Mode Selective Wake SUB-Mode	$V_{Diff\_D\_Range}$	0.9	-	8.0	V	$V_{CMR}$ Bus Biasing on, 1);	P_10.4.21
Differential range recessive Normal-operating Mode, Receive-only Mode Selective Wake SUB-Mode	$V_{Diff\_R\_Range}$	-3.0	-	0.5	V	$V_{CMR}$ Bus Biasing on, 1);	P_10.4.23
Single ended internal resistance	$R_{CAN\_H}$ , $R_{CAN\_L}$	6	37	50	k $\Omega$	$-2\text{ V} \leq V_{CAN\_H} \leq 7\text{ V}$ , $-2\text{ V} \leq V_{CAN\_L} \leq 7\text{ V}$ , recessive state;	P_10.4.25
Input resistance deviation between CANH and CANL	$\Delta R_i$	-3.0	-	3.0	%	$V_{CAN\_L} = V_{CAN\_H} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$ , recessive state;	P_10.4.26
Differential internal resistance	$R_{Diff}$	12	75	100	k $\Omega$	$-2\text{ V} \leq V_{CAN\_H} \leq 7\text{ V}$ , $-2\text{ V} \leq V_{CAN\_L} \leq 7\text{ V}$ , recessive state;	P_10.4.27
Input capacitance CANH, CANL versus GND	$C_{In}$	-	-	40	pF	1)	P_10.4.28
Differential input capacitance	$C_{InDiff}$	-	-	20	pF	1)	P_10.4.29

1) Not subject to production test, specified by design.

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### 10.4.3 Dynamic Transceiver Parameter

**Table 15 Propagation Delay**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40 \text{ }^\circ\text{C} < T_J < 150 \text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Propagation Delay Characteristic</b>							
Propagation delay, TxD to RxD	$t_{Loop}$	80	160	255	ns	$C_L = 100 \text{ pF}$ , $C_{RXD} = 15 \text{ pF}$ ; (see <a href="#">Figure 48</a> )	P_10.4.30
Propagation delay, increased load, TxD to RxD	$t_{Loop\_150}$	80	–	330	ns	$C_L = 100 \text{ pF}$ , $C_{RXD} = 15 \text{ pF}$ , $R_L = 150 \Omega$ ; (see <a href="#">Figure 48</a> )	P_10.4.31
Propagation delay, TxD to bus (“low” to dominant)	$t_{d(L),T}$	30	85	140	ns	$C_L = 100 \text{ pF}$ , $C_{RXD} = 15 \text{ pF}$ ; (see <a href="#">Figure 48</a> )	P_10.4.32
Propagation delay, TxD to bus (“high” to recessive)	$t_{d(H),T}$	30	90	140	ns	$C_L = 100 \text{ pF}$ , $C_{RXD} = 15 \text{ pF}$ ; (see <a href="#">Figure 48</a> )	P_10.4.33
Propagation delay, bus to RxD (dominant to “low”)	$t_{d(L),R}$	30	75	140	ns	$C_{RXD} = 15 \text{ pF}$ ; (see <a href="#">Figure 48</a> )	P_10.4.34
Propagation delay, bus to RxD (recessive to “high”)	$t_{d(H),R}$	30	105	140	ns	$C_{RXD} = 15 \text{ pF}$ ; (see <a href="#">Figure 48</a> )	P_10.4.35

## Electrical Characteristics

**Table 16 CAN FD**

4.75 V < V<sub>CC</sub> < 5.25 V; 3.0 V < V<sub>IO</sub> < 5.5 V; 5.5V < V<sub>BAT</sub> < 40V; R<sub>L</sub> = 60 Ω; -40 °C < T<sub>J</sub> < 150 °C;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>CAN FD Characteristics</b>							
Received recessive bit width at 2 MBit/s	$t_{\text{Bit(RxD)}\_2\text{M}}$	400	500	550	ns	C <sub>L</sub> = 100 pF, C <sub>RxD</sub> = 15 pF, t <sub>Bit</sub> = 500 ns; (see <a href="#">Figure 49</a> );	P_10.4.36
Received recessive bit width at 5 MBit/s	$t_{\text{Bit(RxD)}\_5\text{M}}$	120	200	220	ns	C <sub>L</sub> = 100 pF, C <sub>RxD</sub> = 15 pF, t <sub>Bit</sub> = 200 ns; (see <a href="#">Figure 49</a> );	P_10.4.37
Transmitted recessive bit width at 2 MBit/s	$t_{\text{Bit(Bus)}\_2\text{M}}$	435	500	530	ns	C <sub>L</sub> = 100 pF, C <sub>RxD</sub> = 15 pF, t <sub>Bit</sub> = 500 ns; (see <a href="#">Figure 49</a> );	P_10.4.38
Transmitted recessive bit width at 5 MBit/s	$t_{\text{Bit(Bus)}\_5\text{M}}$	155	200	210	ns	C <sub>L</sub> = 100 pF, C <sub>RxD</sub> = 15 pF, t <sub>Bit</sub> = 200 ns; (see <a href="#">Figure 49</a> );	P_10.4.39
Receiver timing symmetry at 2 MBit/s $\Delta t_{\text{Rec}_2\text{M}} = t_{\text{Bit(RxD)}\_2\text{M}} - t_{\text{Bit(Bus)}\_2\text{M}}$	$\Delta t_{\text{Rec}_2\text{M}}$	-65	-	40	ns	C <sub>L</sub> = 100 pF, C <sub>RxD</sub> = 15 pF, t <sub>Bit</sub> = 500 ns, (see <a href="#">Figure 49</a> );	P_10.4.40
Receiver timing symmetry at 5 MBit/s $\Delta t_{\text{Rec}_5\text{M}} = t_{\text{Bit(RxD)}\_5\text{M}} - t_{\text{Bit(Bus)}\_5\text{M}}$	$\Delta t_{\text{Rec}_5\text{M}}$	-45	-	15	ns	C <sub>L</sub> = 100 pF, C <sub>RxD</sub> = 15 pF, t <sub>Bit</sub> = 200 ns, (see <a href="#">Figure 49</a> );	P_10.4.41

Electrical Characteristics

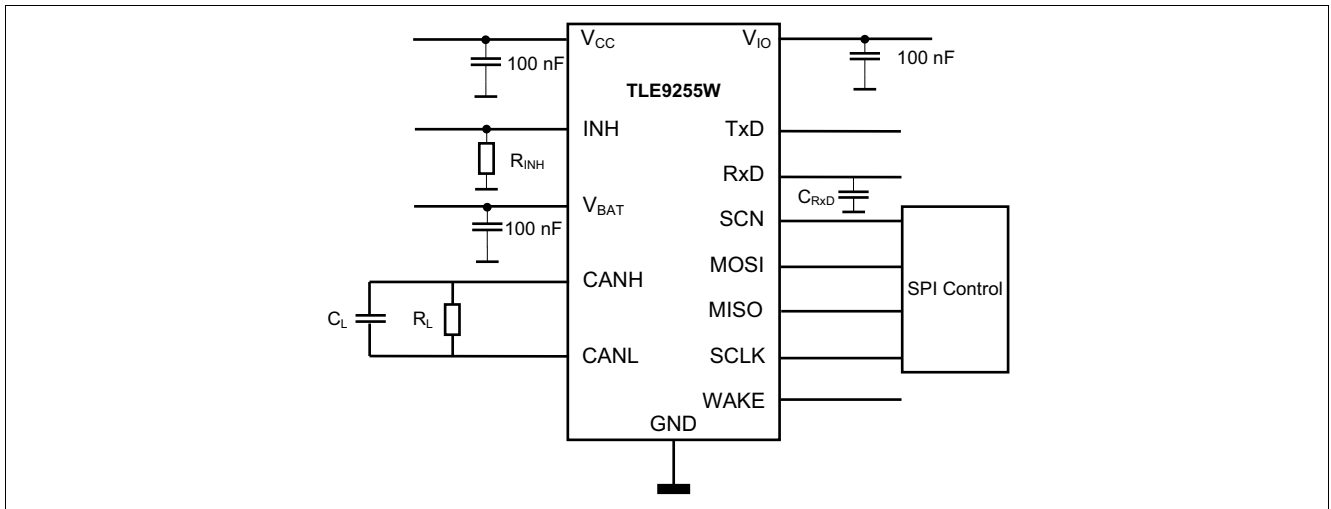


Figure 47 Test Circuit for dynamic characteristics

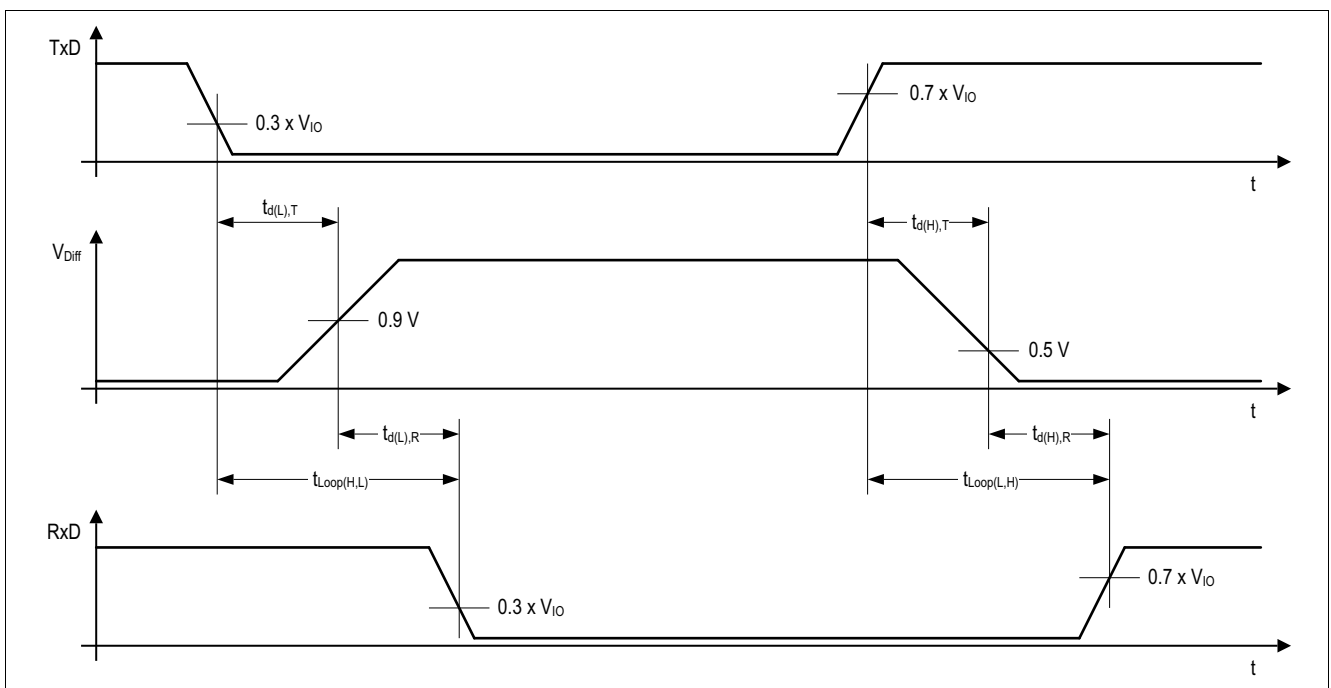


Figure 48 Timing diagrams for dynamic characteristics

Electrical Characteristics

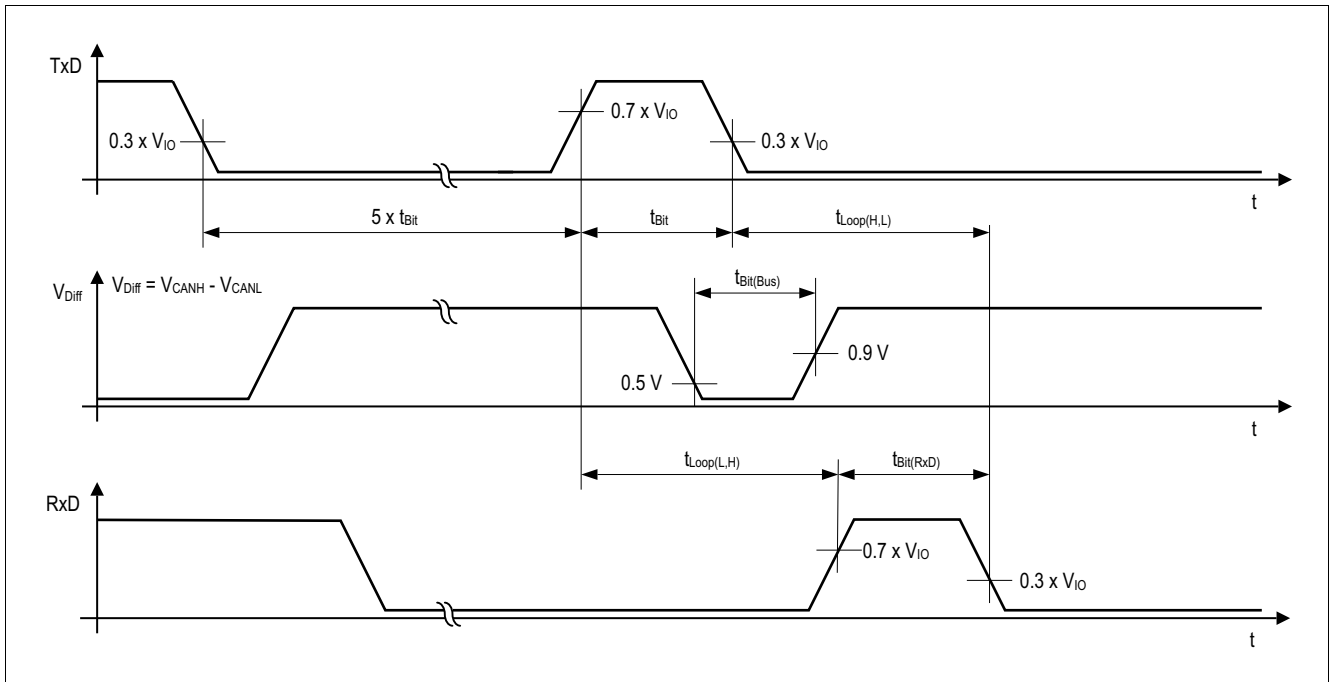


Figure 49 Recessive bit time for five dominant bits followed by one recessive bit

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**Electrical Characteristics**
**10.5 Selective Wake Parameter**
**10.5.1 General Timings**
**Table 17 Electrical Characteristics: CAN FD**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Network propagation delay	$t_{Net\_Prop\_125}$	-400	-	5450	ns	Baudrate = 125 kBit/sec;	P_10.5.1
Network propagation delay	$t_{Net\_Prop\_250}$	-200	-	2675	ns	Baudrate = 250 kBit/sec;	P_10.5.2
Network propagation delay	$t_{Net\_Prop\_500}$	-100	-	1350	ns	Baudrate = 500 kBit/sec;	P_10.5.3
Network propagation delay	$t_{Net\_Prop\_1000}$	-50	-	550	ns	Baudrate = 1 MBit/sec;	P_10.5.4

## Electrical Characteristics

### 10.5.2 CAN FD Tolerance

**Table 18 Electrical Characteristics: CAN FD**

$4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ;  $3.0\text{ V} < V_{IO} < 5.5\text{ V}$ ;  $5.5\text{ V} < V_{BAT} < 40\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
dominant signal which must be ignored and interpreted as a glitch	$t_{FD\_Glitch\_4}$	0	–	$0.05 \times t_{arbitratio\_n}$		Ratio $\leq 4$ , up to 2MBit/s;	P_10.5.5
dominant signal which must be detected as a data bit after the FDF bit and before EOF bit	$t_{FD\_DOM\_4}$	$t_{arbitratio\_n} \times 0.175$	–	–		Ratio $\leq 4$ , up to 2MBit/s;	P_10.5.7

Electrical Characteristics

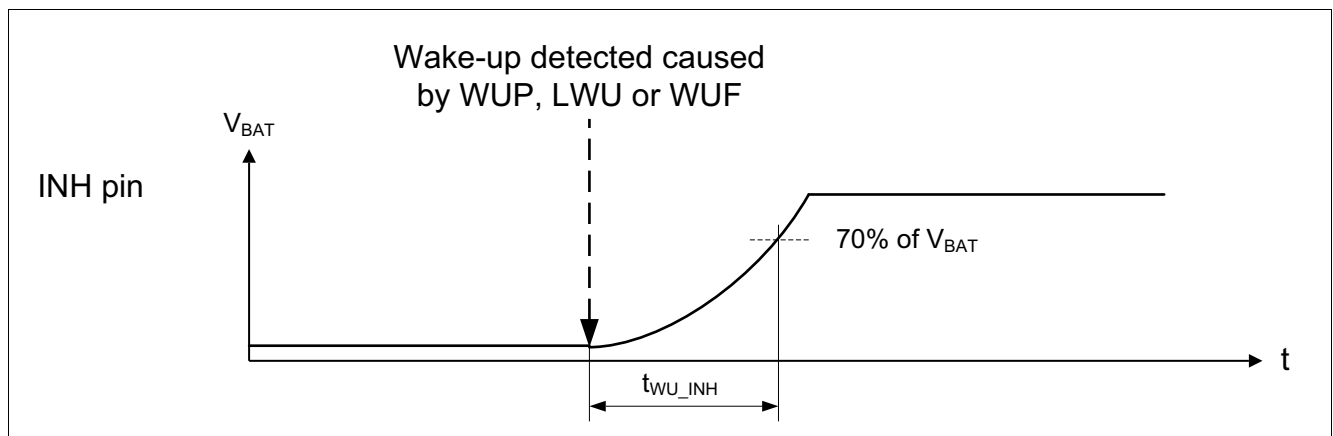
10.6 Wake-Up

10.6.1 General Timings

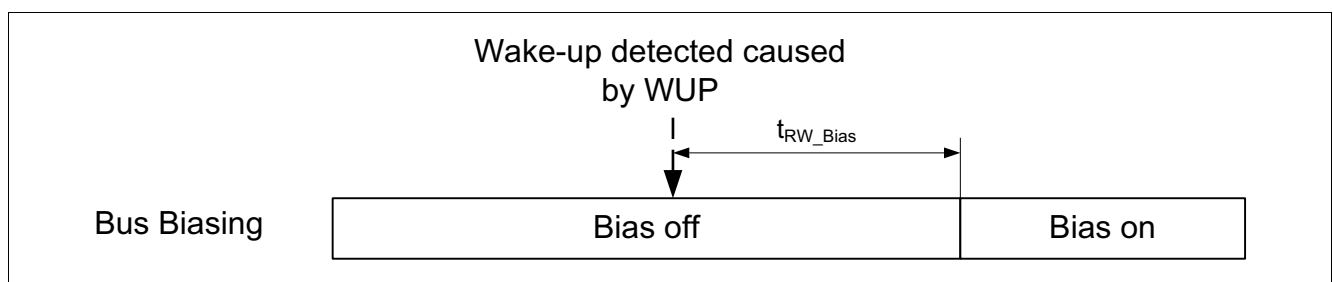
**Table 19 General Timings**

4.75 V < V<sub>CC</sub> < 5.25 V; 3.0 V < V<sub>IO</sub> < 5.5 V; 5.5V < V<sub>BAT</sub> < 40V; R<sub>L</sub> = 60 Ω; -40 °C < T<sub>J</sub> < 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
INH wake-up delay time	t <sub>WU_INH</sub>	–	–	30.0	μs	V <sub>BAT</sub> = 14.0V, R <sub>INH</sub> = 100kΩ; see <a href="#">Figure 50</a>	P_10.6.1
Bias reaction time	t <sub>RW_Bias</sub>	–	–	100	μs	V <sub>CANL/H</sub> = 0.5 V; see <a href="#">Figure 51</a>	P_10.6.2



**Figure 50 INH wake-up delay time**



**Figure 51 Bias reaction time**



## Electrical Characteristics

### 10.6.2 WUP detection Characteristics

**Table 20 WUP detection**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40 \text{ }^\circ\text{C} < T_J < 150 \text{ }^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Differential range dominant low power modes	$V_{\text{Diff\_D\_SLP\_Range}}$	1.05	–	8.0	V	$V_{\text{CMR}}$ , Bus Biasing off 1);	P_10.6.3
Differential range recessive low power modes	$V_{\text{Diff\_R\_SLP\_Range}}$	-3.0	–	0.45	V	$V_{\text{CMR}}$ , Bus Biasing off 1);	P_10.6.5
CAN activity filter time	$t_{\text{Filter}}$	0.5	–	1.8	$\mu\text{s}$	–	P_10.6.8
Bus wake-up timeout	$t_{\text{WAKE}}$	0.8	–	10.0	ms	–	P_10.6.9

1) Not subject to production test, specified by design.

## Electrical Characteristics

### 10.6.3 Local Wake-Up

**Table 21 Local Wake-Up**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Local wake-up detection threshold	$V_{WAKE\_TH}$	0.35 x $V_{BAT}$	0.5 x $V_{BAT}$	0.65 x $V_{BAT}$	V	5.5 < $V_{BAT}$ < 32V	P_10.6.10
Local wake-up detection threshold	$V_{WAKE\_TH}$	0.25 x $V_{BAT}$	0.5 x $V_{BAT}$	0.75 x $V_{BAT}$	V	32 < $V_{BAT}$ < 40V	P_10.6.15
“high” level input current	$I_{WAKE\_H}$	-20	-	-	$\mu\text{A}$		P_10.6.12
“low” level input current	$I_{WAKE\_L}$	-	-	20	$\mu\text{A}$		P_10.6.13
Wake pulse filter time	$t_{WAKE\_Filter}$	10	-	50	$\mu\text{s}$	Figure 18 and Figure 19	P_10.6.14

### 10.7 SPI

**Table 22 SPI**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>SPI Clock Frequency</b>							
SPI clock frequency	$f_{SPI}$	0.01	-	4.0	MHz	-	P_10.7.1
<b>Logic Input MOSI, SCLK</b>							
“high” level input voltage threshold	$V_H$	-	0.5 x $V_{IO}$	0.7 x $V_{IO}$	V	-	P_10.7.2
“low” level input voltage threshold	$V_L$	0.3 x $V_{IO}$	0.4 x $V_{IO}$	-	V	-	P_10.7.3
“high” level input current	$I_H$	20	-	220	$\mu\text{A}$	$V_{MOSI} = V_{IO}$ , $V_{SCLK} = V_{IO}$ , pull-down;	P_10.7.5
“low” level input current	$I_L$	-2.0	-	2.0	$\mu\text{A}$	$V_{MOSI} = 0\text{V}$ , $V_{SCLK} = 0\text{V}$ ;	P_10.7.6
Input capacitance	$C_{IN}$	-	-	10	pF	1)	P_10.7.7

## Electrical Characteristics

**Table 22 SPI (cont'd)**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V; 5.5V <  $V_{BAT}$  < 40V;  $R_L = 60 \Omega$ ; -40 °C <  $T_J$  < 150 °C;  
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Logic Input CSN</b>							
“high” level input voltage threshold	$V_H$	-	0.5 x $V_{IO}$	0.7 x $V_{IO}$	V	-	P_10.7.21
“low” level input voltage threshold	$V_L$	0.3 x $V_{IO}$	0.4 x $V_{IO}$	-	V	-	P_10.7.31
“high” level input current	$I_H$	-2.0	-	2.0	$\mu$ A	$V_{CSN} = V_{IO}$ , pull-down;	P_10.7.33
“low” level input current	$I_L$	-200	-	-20	$\mu$ A	$V_{CSN} = 0$ V;	P_10.7.34
Input capacitance	$C_{IN}$	-	-	10	pF	1)	P_10.7.35
<b>Logic Output: MISO</b>							
“high” level output current	$I_{MISO\_H}$	-	-	-1.0	mA	$V_{MISO} = V_{IO} - 0.4$ V;	P_10.7.8
“low” level output current	$I_{MISO\_L}$	1	-	-	mA	$V_{MISO} = 0.4$ V;	P_10.7.9
Rise time	$t_{MISO\_R}$	-	-	80.0	ns	30% - 70% of $V_{IO}$ , $C_{MISO} = 100$ pF;	P_10.7.10
Fall time	$t_{MISO\_F}$	-	-	80.0	ns	70% - 30% of $V_{IO}$ , $C_{MISO} = 100$ pF;	P_10.7.11
Difference of rise and fall time	$ t_{MISO\_R} - t_{MISO\_F} $	-	-	10.0	ns	$C_{MISO} = 100$ pF;	P_10.7.12
“tri-state” leakage current	$I_{MISO\_Tri}$	-10.0	-	10.0	$\mu$ A	$0 < V_{MISO} < V_{IO}$ ;	P_10.7.13
“tri-state” Input capacitance	$C_{IN\_MISO}$	-	-	10	pF	1)	P_10.7.14
<b>SPI data timing<sup>1)</sup></b>							
Clock “high” period	$t_{SCLK\_H}$	125	-	-	ns	-	P_10.7.15
Clock “low” period	$t_{SCLK\_L}$	125	-	-	ns	-	P_10.7.16
Clock “low” before CSN “low”	$t_{bef}$	125	-	-	ns	-	P_10.7.17
CSN setup time	$t_{lead\_NM}$	1	-	-	$\mu$ s	Normal-operating Mode, Stand-by Mode, Receive-only Mode;	P_10.7.18
CSN setup time	$t_{lead\_SP}$	6.0	-	-	$\mu$ s	Selective Wake Sub-Mode, Selective Sleep Sub-Mode, Sleep WUP Mode;	P_10.7.19
SCLK setup time	$t_{lag}$	250	-	-	ns	-	P_10.7.20
MOSI setup time	$t_{MOSI\_SU}$	25	-	-	ns	-	P_10.7.22

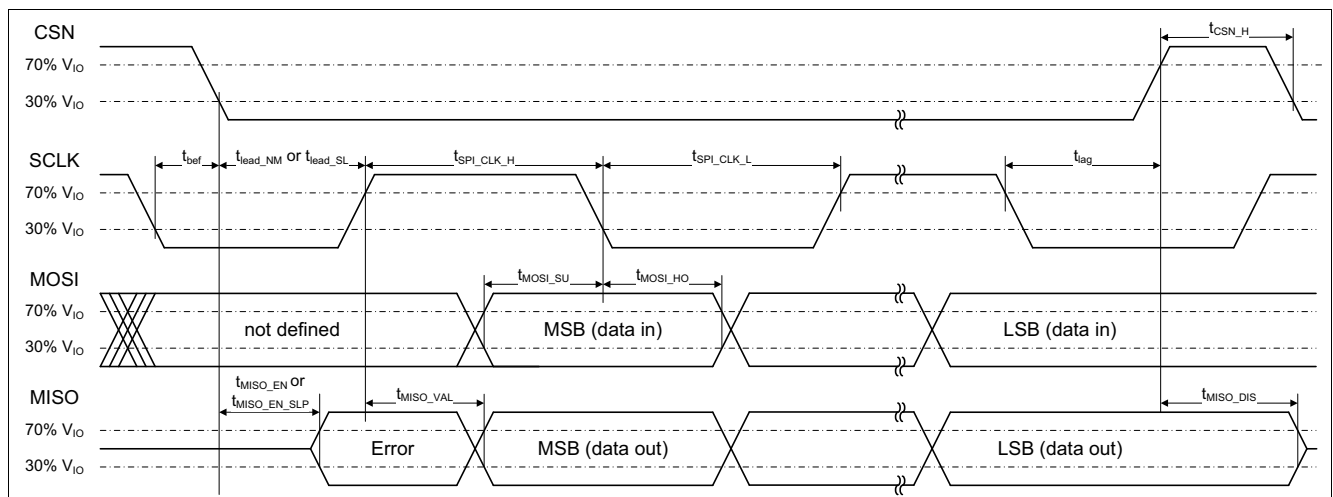
**Electrical Characteristics**

**Table 22 SPI (cont'd)**

4.75 V < V<sub>CC</sub> < 5.25 V; 3.0 V < V<sub>IO</sub> < 5.5 V; 5.5V < V<sub>BAT</sub> < 40V; R<sub>L</sub> = 60 Ω; -40 °C < T<sub>J</sub> < 150 °C;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
MOSI hold time	t <sub>MOSI_HO</sub>	50	-	-	ns	-	P_10.7.23
CSN "high" time	t <sub>CSN_H</sub>	3.0	-	-	μs	-	P_10.7.24
Maximum signal rise time on SPI inputs: MOSI, SCLK and CSN	t <sub>R_max</sub>	-	-	50	ns	-	P_10.7.25
Maximum signal fall time on SPI inputs: MOSI, SCLK and CSN	t <sub>F_max</sub>	-	-	50	ns	-	P_10.7.26
MISO enable time	t <sub>MISO_EN</sub>	-	-	120	ns	-	P_10.7.27
MISO enable time in Sleep Mode	t <sub>MISO_EN_SLP</sub>	-	-	5.5	μs	-	P_10.7.36
MISO disable time	t <sub>MISO_DIS</sub>	-	-	50	ns	-	P_10.7.28
MISO valid time	t <sub>MISO_VAL</sub>	-	-	100	ns	-	P_10.7.29
CSN Timeout	t <sub>CSN_TO</sub>	2.1	-	4	ms	-	P_10.7.30

1) Not subject to production test, specified by design.



**Figure 52 SPI timings**

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**Application Information**

## 11 Application Information

### 11.1 ESD Robustness according to IEC 61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

**Table 23 ESD robustness according to IEC61000-4-2**

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin $V_{BAT}$ , CANH, CANL and WAKE <sup>1)</sup> versus GND	$\geq +10$	kV	<sup>2)</sup> Positive pulse
Electrostatic discharge voltage at pin $V_{BAT}$ , CANH, CANL and WAKE <sup>1)</sup> versus GND	$\leq -10$	kV	<sup>2)</sup> Negative pulse

1) 10 nF capacitor and 3.3 kΩ resistor required (see [Figure 53](#)).

2) ESD susceptibility “ESD GUN” according to GIFT / ICT paper: “EMC Evaluation of CAN Transceivers, IEC TS 62228”, section 4.3. (DIN EN 61000-4-2)  
Tested by external test facility (IBEE Zwickau, EMC test report).

Application Information

11.2 Application Example

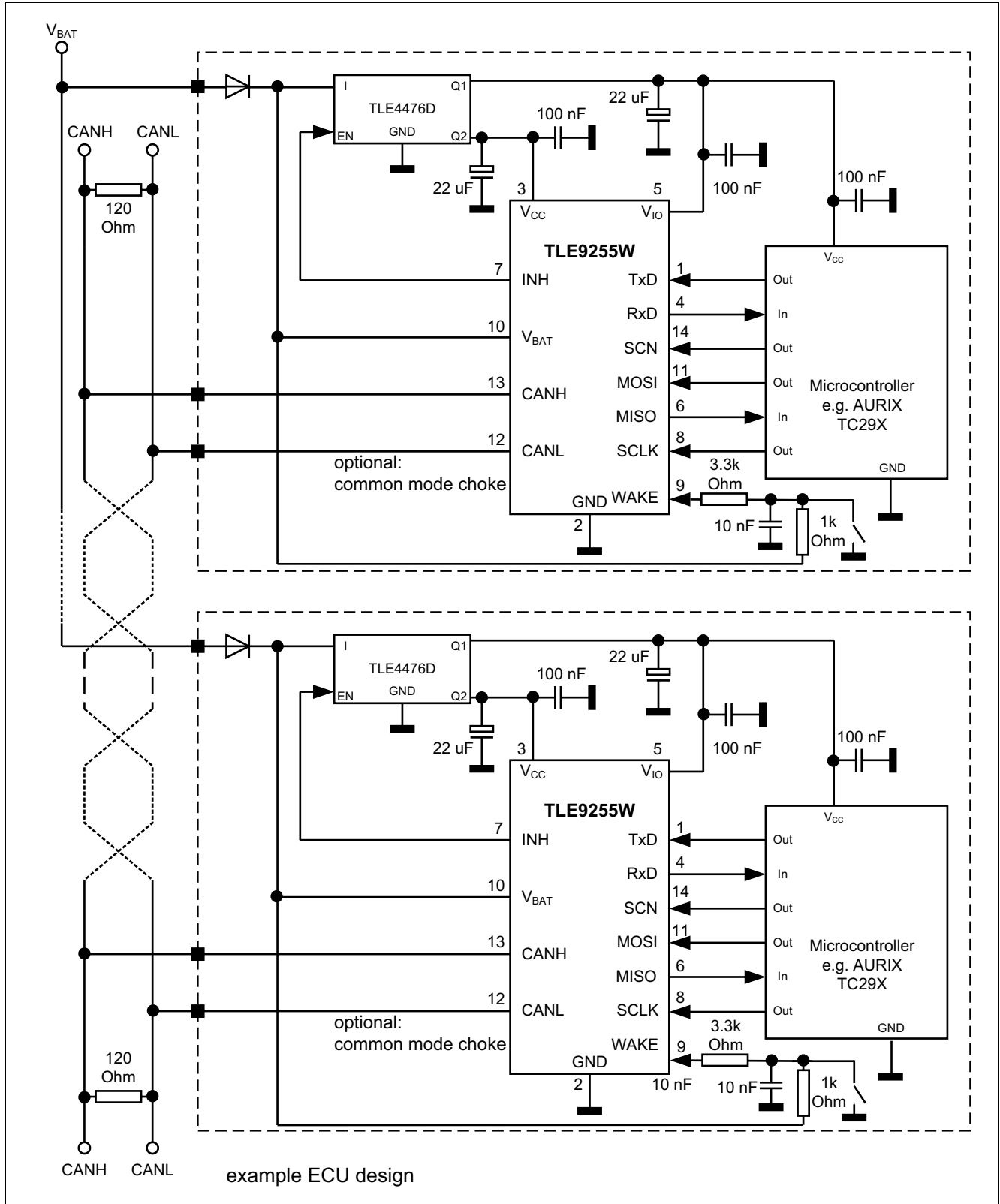


Figure 53 Application circuit

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## Application Information

### 11.3 Voltage Adaption to the Microcontroller Supply

To adapt the digital input and output levels of the TLE9255W to the I/O levels of the microcontroller, connect the power supply pin  $V_{IO}$  to the microcontroller voltage supply (see [Figure 53](#)).

*Note:* In case the digital supply voltage  $V_{IO}$  is not required in the application, connect the digital supply voltage  $V_{IO}$  to the transmitter supply  $V_{CC}$ .

### 11.4 Further Application Information

- Please contact us for information regarding the pin FMEA.
- For further information you may visit: [www.infineon.com/automotive-transceiver](http://www.infineon.com/automotive-transceiver)

Package Outlines

## 12 Package Outlines

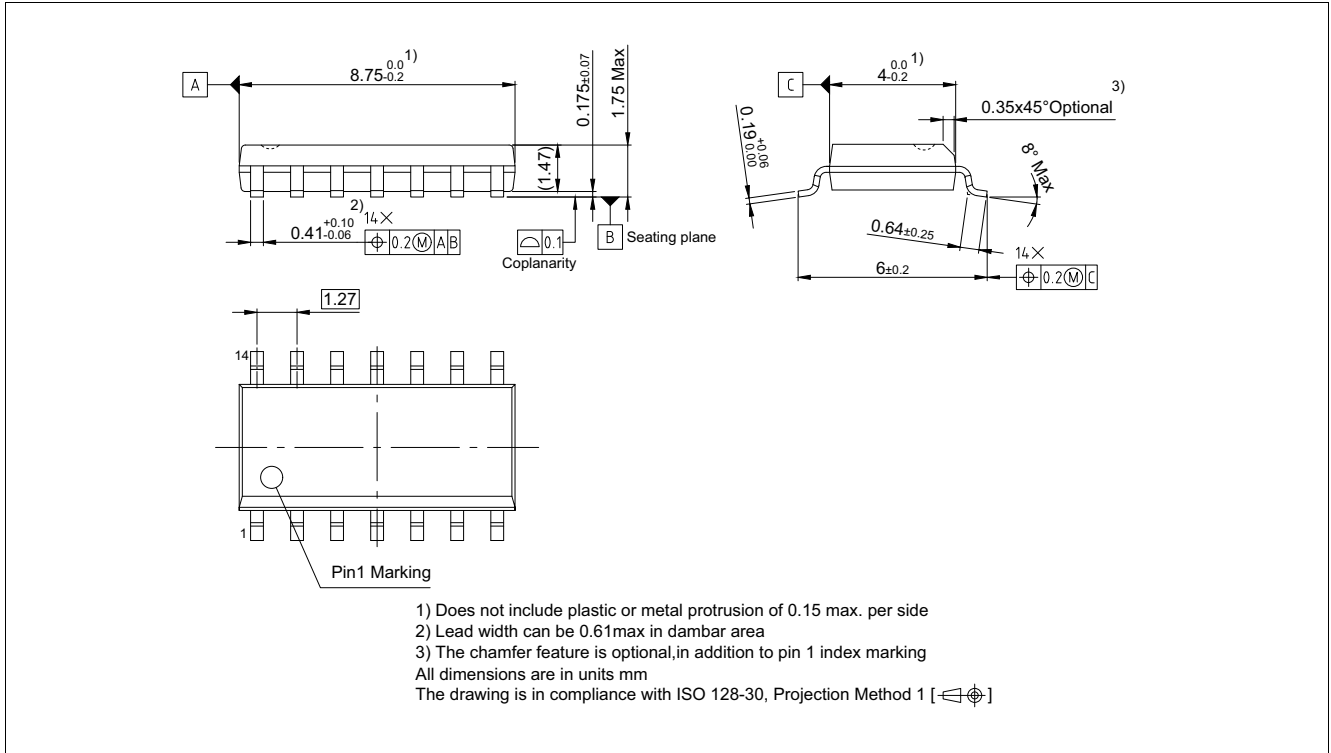


Figure 54 PG-DSO-14



Package Outlines

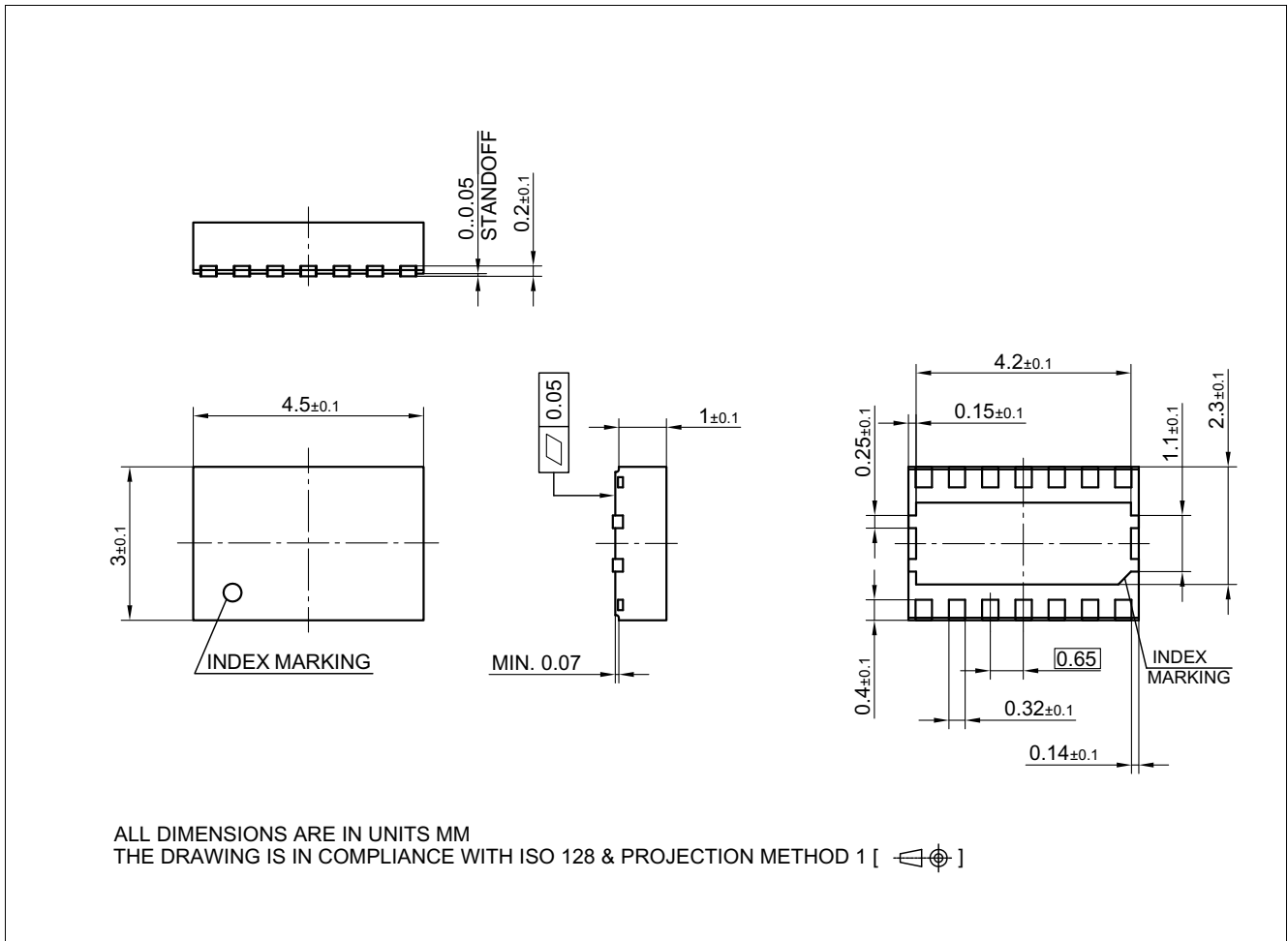


Figure 55 PG-TSON-14

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:  
<http://www.infineon.com/packages>.

Dimensions in mm

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## Terminology

DLC	Data Length Code
LWU	Local Wake Up
SPI	Serial Peripheral Interface
WUF	Wake-up Frame
WUP	Wake-up Pattern

---

**Revision History**

### 13 Revision History

Revision	Date	Changes
1.00	2016-09-15	Data Sheet Rev. 1.0 created
1.01	2017-02-27	<ul style="list-style-type: none"> <li>• <b>SWK_ACTIVE</b> bit description changed in register <b>SWK_STAT</b></li> <li>• Internal state transitions have higher priority than mode change SPI commands</li> <li>• <math>t_{FD\_Glitch\_10}</math> and <math>t_{FD\_DOM\_10}</math> removed (<b>Chapter 10.5.2</b>)</li> </ul>
1.02	2018-02-02	<ul style="list-style-type: none"> <li>• ESD immunity at CANH, CANL, WAKE and <math>V_{BAT}</math> versus to GND set from +-8 kV to +-10 kV</li> <li>• ESD immunity at all other pins set from +-2kV to +-4 kV</li> <li>• ESD robustness according to IEC 61000-4-2 changed form +-8 kV to +-10 kV</li> <li>• Tightening of limits for <math>V_{BAT}</math> and <math>V_{CC}</math> supply current at Receive-only Mode (P_10.2.5)</li> <li>• Tightening of limits for <math>V_{IO}</math> supply current at Normal-operating Mode (P_10.2.4)</li> <li>• Tightening of limits for <math>V_{CC}</math> supply current dominant bus signal at Normal-operating Mode (P_10.2.2)</li> <li>• Tightening of limits for <math>V_{BAT}</math> supply current at Normal-operating Mode (P_10.2.1)</li> <li>• Tightening of limits for <math>V_{IO}</math> supply current at Receive-only Mode (P_10.2.7)</li> <li>• Pin configuration for TSON Package added (<b>Figure 2</b>)</li> <li>• Test condition for the Parameter Absolute current on CAN_L (P_10.04.14) compliant to ISO 11898-2 (2016).</li> <li>• Test condition for the Parameter Absolute current on CAN_H (P_10.04.13) compliant to ISO 11898-2 (2016)</li> <li>• Test condition for the Parameter Driver Symmetry (P_10.04.12) compliant to ISO 11898-2 (2016).</li> <li>• Test condition for the Parameter Input resistance deviation between CANH and CANL(P_10.04.26) compliant to ISO 11898-2 (2016).</li> </ul>
1.03	2018-10-25	<ul style="list-style-type: none"> <li>• Package outline for TSON changed</li> </ul>
1.04	2021-08-04	Editorial change: package outline drawing PG-DSO14 updated

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[MCP2515-I/ST](#) [MCP2515T-I/SO](#) [MCP2551-E/P](#) [MCP2551-E/SN](#) [MCP2551-I/P](#) [MCP2551-I/SN](#) [MCP2561-E/P](#) [MCP2561T-ESN](#)  
[MCP2562FD-E/SN](#) [MCP2562T-ESN](#) [MCP2515-E/ML](#) [PCA82C250T/YM,118](#) [PCA82C251T/YM,118](#) [SJA1000T/N1,118](#)