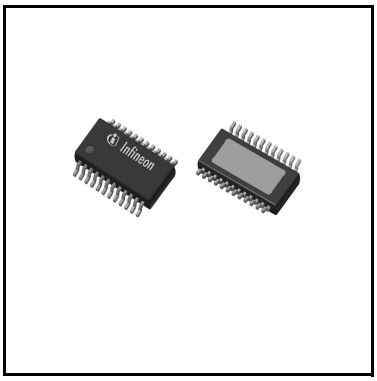
# TLE94108ES



## Features

- Eight half bridge power outputs
- Very low power consumption in sleep mode
- 3.3V / 5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Independently diagnosable outputs (overcurrent, open load)
- Open load diagnostics in ON-state for all high-side and low-side
- Outputs with selectable open load thresholds (HS1, HS2)
- 16-bit Standard SPI interface with daisy chain and in-frame response capability for control and diagnosis
- Fast diagnosis with the global error flag
- PWM capable outputs for frequencies 80Hz, 100Hz and 200Hz with 8-bit duty cycle resolution
- Overtemperature pre-warning and protection
- Over- and Undervoltage lockout
- Cross-current protection

## Applications

- HVAC Flap DC motors
- Monostable and bistable Relays
- Side mirror x-y adjustment and mirror fold
- LEDs

## Description

The TLE94108ES is a protected eight-fold half-bridge driver designed especially for automotive motion control applications such as Heating, Ventilation and Air Conditioning (HVAC) flap DC motor control. It is part of a larger family offering half-bridge drivers from three outputs to twelve outputs with direct interface or SPI interface.

The half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. It offers diagnosis features such as short circuit, open load, power supply failure and overtemperature detection. In combination with its low quiescent current, this device is attractive among others for automotive applications. The small fine pitch exposed pad package, PG-TSDSO-24, provides good thermal performance and reduces PCB-board space and costs.

| Type | Package | Marking |
|---|---|---|
| TLE94108ES | PG-TSDSO-24 | TLE94108ES |

**Table 1 Product Summary**

| | | |
|---|---|---|
| Normal Operating Voltage | $V_S$ | 5.5 ... 18 V |
| Extended Operating Voltage | $V_S$ | 18 ... 20 V |
| Logic Supply Voltage | $V_{DD}$ | 3.0 ... 5.5 V |
| Maximum Supply Voltage for Load Dump Protection | $V_{S(LD)}$ | 40 V |
| Minimum Overcurrent Threshold | $I_{SD}$ | 0.9 A |
| Maximum On-State Path Resistance at $T_j$ = 150°C | $R_{DSON(total)\_HSx+LSy}$ | 1.8 + 1.8 Ω |
| Typical Quiescent Current at $T_j$ = 85°C | $I_{SQ}$ | 0.1 µA |
| Maximum SPI Access Frequency | $f_{SCLK}$ | 5 MHz |

# Table of Contents

# 1 Pin Configuration

## 1.1 Pin Assignment

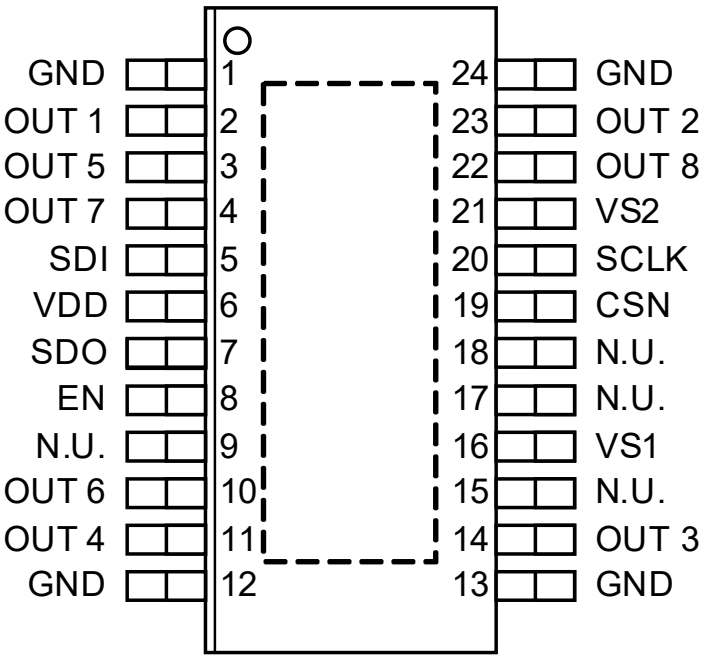



**Figure 1 Pin Configuration TLE94108ES**

## 1.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | GND | Ground. All ground pins should be externally connected together. |
| 2 | OUT 1 | Power half-bridge 1 |
| 3 | OUT 5 | Power half-bridge 5 |
| 4 | OUT 7 | Power half-bridge 7 |
| 5 | SDI | Serial data input with internal pull down |
| 6 | VDD | Logic supply voltage |
| 7 | SDO | Serial data output |
| 8 | EN | Enable with internal pull-down; Places device in standby mode by pulling the EN line Low |
| 9 | N.U. | Not used. This pin should be left open. |
| 10 | OUT 6 | Power half-bridge 6 |
| 11 | OUT 4 | Power half-bridge 4 |
| 12 | GND | Ground. All ground pins should be externally connected together. |

## Pin Configuration

| Pin | Symbol | Function |
|---|---|---|
| 13 | GND | Ground. All ground pins should be externally connected together. |
| 14 | OUT 3 | Power half-bridge 3 |
| 15 | N.U. | Not used. This pin should be left open. |
| 16 | VS1 | Main supply voltage for power half bridges. VS1 should be externally connected to VS2. |
| 17 | N.U. | Not used. This pin should be left open. |
| 18 | N.U. | Not used. This pin should be left open. |
| 19 | CSN | Chip select Not input with internal pull up |
| 20 | SCLK | Serial clock input with internal pull down |
| 21 | VS2 | Main supply voltage for power half bridges. VS1 should be externally connected to VS2. |
| 22 | OUT 8 | Power half-bridge 8 |
| 23 | OUT 2 | Power half-bridge 2 |
| 24 | GND | Ground. All ground pins should be externally connected together. |
| EDP | - | Exposed Die Pad; For cooling and EMC purposes only - not usable as electrical ground. Electrical ground must be provided by pins 1,12,13,24.[1)] |

1) The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB. The exposed pad (EP) must be either left open or connected to GND. It is recommended to connect EP to GND for best EMC and thermal performance.

*Note: Not used (N.U.) pins and unused outputs are recommended to be left unconnected (open) on the application board. If N.U. pins or unused output pins are routed to an external connector which leaves the PCB, then these outputs should have provision for a zero ohm jumper (depopulated if unused) or ESD protection. In other words, they should be treated like used pins.*

# 2 Block Diagram

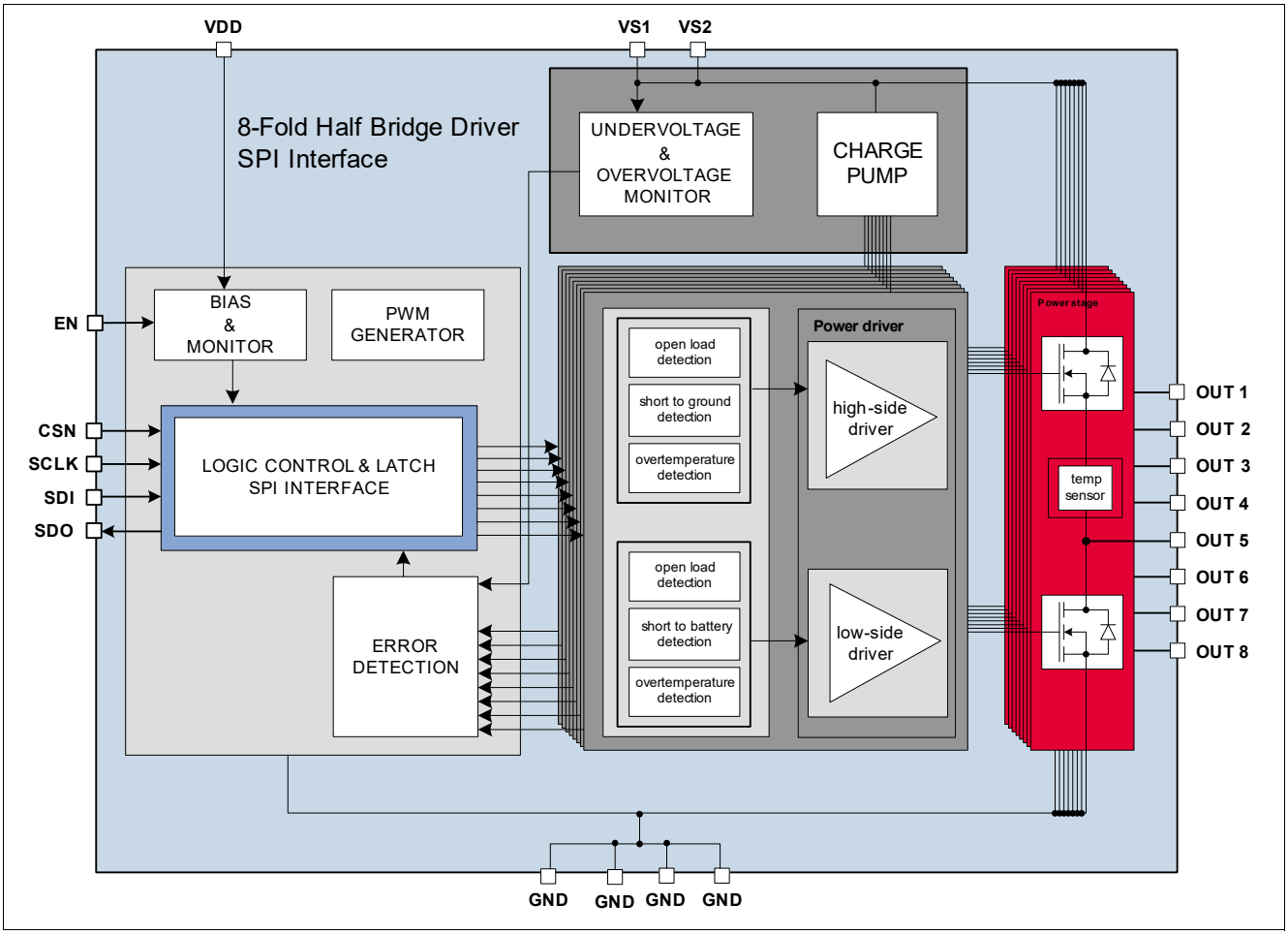



**Figure 2 Block Diagram TLE94108ES(SPI Interface)**

## 2.1 Voltage and current definition

**Figure 3** shows terms used in this datasheet, with associated convention for positive values.

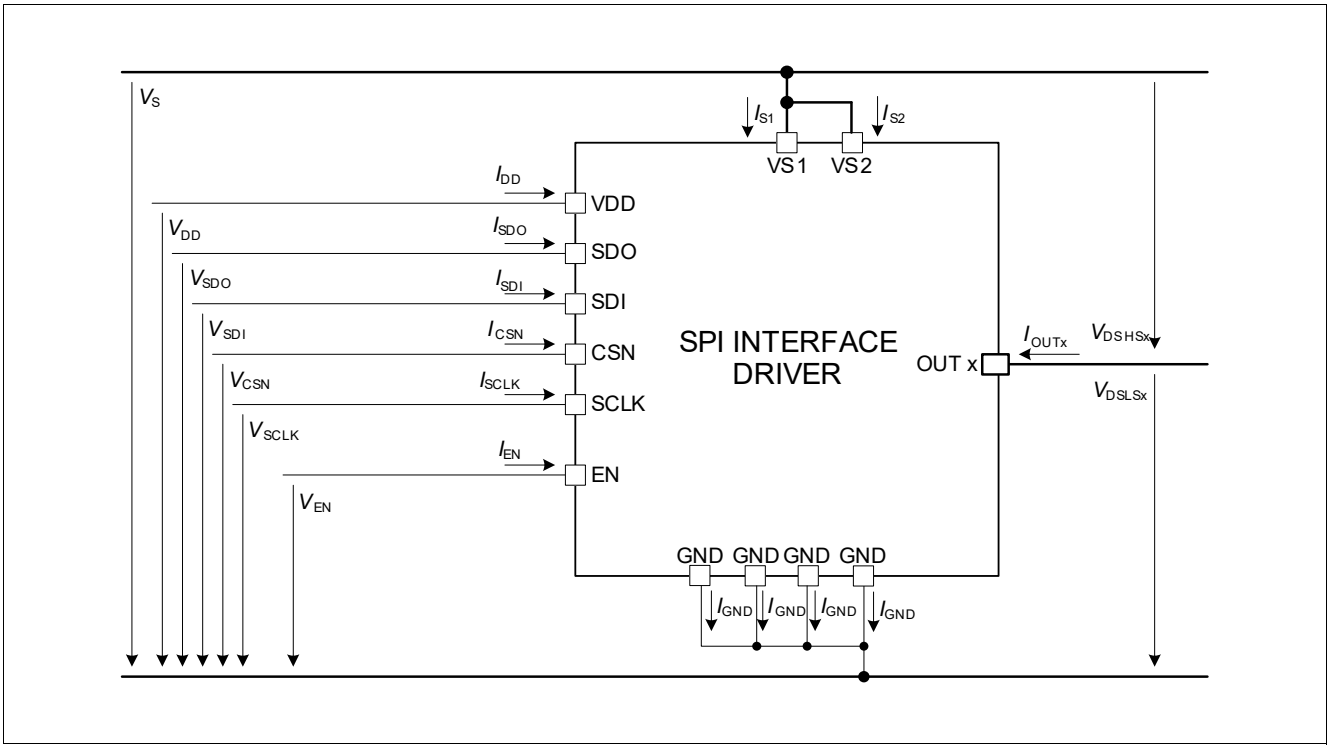



**Figure 3 Voltage and Current Definition**

# 3 General Product Characteristics

## 3.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings[1] $T_j$ = -40°C to +150°C**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Supply voltage | $V_S$ | -0.3 | – | 40 | V | $V_S = V_{S1} = V_{S2}$ | P_4.1.1 |
| Supply Voltage Slew Rate | $\lvert dV_S/dt \rvert$ | – | – | 10 | V/µs | $V_S$ increasing and decreasing [1] | P_4.2.2 |
| Power half-bridge output voltage | $V_{OUT}$ | -0.3 | – | 40 | V | 0 V < $V_{OUT}$ < $V_S$ [2] | P_4.1.2 |
| Logic supply voltage | $V_{DD}$ | -0.3 | – | 5.5 | V | 0 V < $V_S$ < 40 V | P_4.1.3 |
| Logic input voltages (SDI, SCLK, CSN, EN) | $V_{SDI}$, $V_{SCLK}$, $V_{CSN}$, $V_{EN}$ | -0.3 | – | VDD | V | 0 V < $V_S$ < 40 V<br>0 V < $V_{DD}$ < 5.5V | P_4.1.4 |
| Logic output voltage (SDO) | $V_{SDO}$ | -0.3 | – | VDD | V | 0 V < $V_S$ < 40 V<br>0 V < $V_{DD}$ < 5.5V | P_4.1.5 |
| **Currents** | | | | | | | |
| Continuous Supply Current for $V_{S1}$ | $I_{S1}$ | 0 | – | 2.0 | A | – | P_4.1.6 |
| Continuous Supply Current for $V_{S2}$ | $I_{S2}$ | 0 | – | 2.0 | A | – | P_4.1.7 |
| Current per GND pin | $I_{GND}$ | 0 | – | 2.0 | A | – | P_4.1.14 |
| Output Currents | $I_{OUT}$ | -2.0 | – | 2.0 | A | – | P_4.1.15 |
| **Temperatures** | | | | | | | |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.1.8 |
| Storage temperature | $T_{stg}$ | -50 | – | 150 | °C | – | P_4.1.9 |
| **ESD Susceptibility** | | | | | | | |
| ESD susceptibility OUTn and VSx pins versus GND. All other pins grounded. | $V_{ESD}$ | -8 | – | 8 | kV | JEDEC HBM[1)3)] | P_4.1.10 |
| ESD susceptibility all pins | $V_{ESD}$ | -2 | – | 2 | kV | JEDEC HBM[1)3)] | P_4.1.11 |
| ESD susceptibility all pins | $V_{ESD}$ | -500 | – | 500 | V | CDM[1)4)] | P_4.1.12 |
| ESD susceptibility corner pins | $V_{ESD}$ | -750 | – | 750 | V | CDM[1)4)] | P_4.1.13 |

1) Not subject to production test, specified by design
2) Also applicable to not used (N.U.) pins
3) ESD susceptibility, “JEDEC HBM” according to ANSI/ ESDA/ JEDEC JS001 (1.5 kΩ, 100pF)
4) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 3.2 Functional Range

**Table 3 Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Supply voltage range for normal operation | $V_{S(nor)}$ | 5.5 | – | 18 | V | – | P_4.2.1 |
| Extended supply voltage range | $V_{S(ext)}$ | 18 | – | 20 | V | 1)2) | P_4.2.7 |
| Logic supply voltage range for normal operation | $V_{DD}$ | 3.0 | – | 5.5 | V | – | P_4.2.3 |
| Logic input voltages (SDI, SCLK, CSN, EN) | $V_{SDI}$, $V_{SCLK}$, $V_{CSN}$, $V_{EN}$ | -0.3 | – | 5.5 | V | – | P_4.2.4 |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | | P_4.2.5 |

1) Not subject to production test, specified by design.

2) In the extended supply range, the device is still functional. However, deviations of the specified electrical characteristics are possible.

*Note: Within the normal functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 3.3 Thermal Resistance

**Table 4 Thermal Resistance TLE94108ESTLE94106EL**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Case, $T_A$ = 85°C | $R_{thjC\_hot}$ | – | 2.5 | – | K/W | 1) | |
| Junction to ambient, $T_A$ = 85°C (1s0p, minimal footprint) | $R_{thjA\_hot\_min}$ | – | 81.0 | – | K/W | 1) 2) | |
| Junction to ambient, $T_A$ = 85°C (1s0p, 300mm2 Cu) | $R_{thjA\_hot\_300}$ | – | 47.7 | – | K/W | 1) 3) | |
| Junction to ambient, $T_A$ = 85°C (1s0p, 600mm2 Cu) | $R_{thjA\_hot\_600}$ | – | 40.5 | – | K/W | 1) 1) | |
| Junction to ambient, $T_A$ = 85°C (2s2p) | $R_{thjA\_hot\_2s2p}$ | – | 28.4 | – | K/W | 1) 5) | |

1) Specified $R_{thJA}$ value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 600mm2 copper area and 35µm thickness. Ta = 85°C, each channel dissipates 0.135W.

## 3.4 Electrical Characteristics

**Table 5 Electrical Characteristics, $V_S$ =5.5 V to 18 V, $V_{DD}$ = 3.0V to 5.5V, $T_j$ = -40°C to +150°C, EN= HIGH, $I_{OUTn}$= 0 A; Typical values refer to $V_{DD}$ = 5.0 V, $V_S$ = 13.5 V and $T_J$ = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Current Consumption, EN = GND** | | | | | | | |
| Supply Quiescent current | $I_{SQ}$ | – | 0.5 | 2 | µA | -40°C ≤ $T_j$ ≤ 85°C | P_4.4.1 |
| Logic supply quiescent current | $I_{DD\_Q}$ | – | 0.1 | 1 | µA | -40°C ≤ $T_j$ ≤ 85°C | P_4.4.2 |
| Total quiescent current | $I_{SQ}$ + $I_{DD\_Q}$ | – | 0.6 | 3 | µA | -40°C ≤ $T_j$ ≤ 85°C | P_4.4.3 |
| **Current Consumption, EN=HIGH** | | | | | | | |
| Supply current | $I_S$ | – | 0.5 | 1 | mA | Power drivers and power stages are off | P_4.4.4 |
| Supply current | $I_{S\_HSON}$ | – | 4.5 | 9 | mA | All high-sides ON[1)] | P_4.4.101 |
| Logic supply current | $I_{DD}$ | – | 1.5 | 3 | mA | SPI not active | P_4.4.5 |
| Logic supply current | $I_{DD\_RUN}$ | – | 5 | – | mA | SPI 5MHz [3)] | P_4.4.6 |
| Total supply current | $I_S$ + $I_{DD\_RUN}$ | – | 5.5 | – | mA | SPI 5MHz [3)] | P_4.4.7 |
| **Over- and Undervoltage Lockout** | | | | | | | |
| Undervoltage Switch ON voltage threshold | $V_{UV\ ON}$ | 4.25 | – | 5.25 | V | $V_S$ increasing | P_4.4.8 |
| Undervoltage Switch OFF voltage threshold | $V_{UV\ OFF}$ | 4 | – | 5.0 | V | $V_S$ decreasing | P_4.4.9 |
| Undervoltage Switch ON/OFF hysteresis | $V_{UV\ HY}$ | – | 0.25 | – | V | $V_{UV\ ON}$ - $V_{UV\ OFF}$ [3)] | P_4.4.10 |
| Overvoltage Switch OFF voltage threshold | $V_{OV\ OFF}$ | 21 | – | 25 | V | $V_S$ increasing | P_4.4.11 |
| Overvoltage Switch ON voltage threshold | $V_{OV\ ON}$ | 20 | – | 24 | V | $V_S$ decreasing | P_4.4.12 |
| Overvoltage Switch ON/OFF hysteresis | $V_{OV\ HY}$ | – | 1 | – | V | $V_{OV\ OFF}$ - $V_{OV\ ON}$ [3)] | P_4.4.13 |
| $V_{DD}$ Power-On-Reset | $V_{DD\ POR}$ | 2.40 | 2.70 | 2.90 | V | $V_{DD}$ increasing | P_4.4.14 |
| $V_{DD}$ Power-Off-Reset | $V_{DD\ POffR}$ | 2.35 | 2.65 | 2.85 | V | $V_{DD}$ decreasing | P_4.4.15 |
| $V_{DD}$ Power ON/OFF hysteresis | $V_{DD\ POR\ HY}$ | – | 0.05 | – | V | $V_{DD\ POR}$ - $V_{DD\ POffR}$ [3)] | P_4.4.98 |
| **Static Drain-source ON-Resistance (High-Side or Low-Side)** | | | | | | | |
| High-Side or Low-Side $R_{DSON}$ (all outputs) | $R_{DSON\_HB\_25C}$ | – | 850 | 1200 | mΩ | $I_{OUT}$ = ±0.5 A; $T_j$ = 25 °C | P_4.4.16 |
| High-Side or Low-Side $R_{DSON}$ (all outputs) | $R_{DSON\_HB\_150C}$ | – | 1400 | 1800 | mΩ | $I_{OUT}$ = ±0.5 A; $T_j$ = 150 °C | P_4.4.17 |

**Table 5 Electrical Characteristics, $V_S$ =5.5 V to 18 V, $V_{DD}$ = 3.0V to 5.5V, $T_j$ = -40°C to +150°C, EN= HIGH, $I_{OUTn}$= 0 A; Typical values refer to $V_{DD}$ = 5.0 V, $V_S$ = 13.5 V and $T_J$ = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| High-Side $R_{DSON}$ (HS1 and HS2 in LED mode) | $R_{DSON\_HI\_HB\_25C}$ | – | 950 | 1300 | mΩ | [2] $I_{OUT}$ = -0.1 A; $T_j$ = 25 °C | P_4.4.18 |
| High-Side $R_{DSON}$ (HS1 and HS2 in LED mode) | $R_{DSON\_HI\_HB\_150C}$ | – | 1500 | 2000 | mΩ | [2] $I_{OUT}$ = -0.1 A; $T_j$ = 150 °C | P_4.4.19 |
| **Output Protection and Diagnosis of high-side (HS) channels of half-bridge output** | | | | | | | |
| HS Overcurrent Shutdown Threshold | $I_{SD\_HS}$ | -1.4 | -1.1 | -0.9 | A | See **Figure 7** | P_4.4.89 |
| Difference between shutdown and limit current | $I_{LIM\_HS}$ - $I_{SD\_HS}$ | -1.2 | -0.6 | 0 | A | [3] $\|I_{LIM\_HS}\| \geq \|I_{SD\_HS}\|$ See **Figure 7** | P_4.4.21 |
| Overcurrent Shutdown filter time | $t_{dSD\_HS}$ | 15 | 19 | 23 | µs | [3] | P_4.4.22 |
| Open Load Detection Current | $I_{OLD1\_HS}$ | -15 | -8 | -3 | mA | - | P_4.4.23 |
| Open Load Detection filter time | $t_{OLD1\_HS}$ | 2000 | 3000 | 4000 | µs | [3] | P_4.4.24 |
| Open Load Detection Current for LED mode (HS1 & HS2) | $I_{OLD2\_HS1,2}$ | -3.2 | -2 | -0.5 | mA | Bit OL_SEL_HS1 = 1, OL_SEL_HS2 = 1 | P_4.4.25 |
| Open Load Detection filter time for LED mode (HS1 & HS2) | $t_{OLD2\_HS1,2}$ | 100 | 200 | 300 | µs | Bit OL_SEL_HS1 = 1, OL_SEL_HS2 = 1; [3] | P_4.4.26 |
| **Output Protection and Diagnosis of low-side (LS) channels of half-bridge output** | | | | | | | |
| LS Overcurrent Shutdown Threshold | $I_{SD\_LS}$ | 0.9 | 1.1 | 1.4 | A | **Figure 8** | P_4.4.104 |
| Difference between shutdown and limit current | $I_{LIM\_LS}$ - $I_{SD\_LS}$ | 0 | 0.6 | 1.2 | A | [3] $I_{LIM\_LS} \geq I_{SD\_LS}$ **Figure 8** | P_4.4.28 |
| Overcurrent Shutdown filter time | $t_{dSD\_LS}$ | 15 | 19 | 23 | µs | [3] | P_4.4.29 |
| Open Load Detection Current | $I_{OLD\_LS}$ | 3 | 8 | 15 | mA | - | P_4.4.30 |
| Open Load Detection filter time | $t_{OLD\_LS}$ | 2000 | 3000 | 4000 | µs | [3] | P_4.4.31 |
| **Outputs OUT(1...n) leakage current** | | | | | | | |
| HS leakage current in off state | $I_{QLHn\_NOR}$ | -2 | -0.5 | – | µA | $V_{OUTn}$ = 0V ; EN=High | P_4.4.32 |
| HS leakage current in off state | $I_{QLHn\_SLE}$ | -2 | -0.5 | – | µA | $V_{OUTn}$ = 0V; EN=GND | P_4.4.33 |
| LS Leakage current in off state | $I_{QLLn\_NOR}$ | – | 0.5 | 2 | µA | $V_{OUTn}$ = $V_S$ ; EN=High | P_4.4.34 |
| LS Leakage current in off state | $I_{QLLn\_SLE}$ | – | 0.5 | 2 | µA | $V_{OUTn}$ = $V_S$ ; EN=GND | P_4.4.35 |
| **Output Switching Times. See Figure 9 and Figure 10.** | | | | | | | |
| Slew rate of high-side and low-side outputs | $d_{VOUT}/dt$ | 0.1 | 0.45 | 0.75 | V/µs | Resistive load = 100Ω; $V_S$=13.5V [4] | P_4.4.36 |

**Table 5 Electrical Characteristics, $V_S$ =5.5 V to 18 V, $V_{DD}$ = 3.0V to 5.5V, $T_j$ = -40°C to +150°C, EN= HIGH, $I_{OUTn}$= 0 A; Typical values refer to $V_{DD}$ = 5.0 V, $V_S$ = 13.5 V and $T_J$ = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output delay time high side driver on | $t_{dONH}$ | 5 | 20 | 35 | µs | Resistive load = 100Ω to GND | P_4.4.37 |
| Output delay time high side driver off | $t_{dOFFH}$ | 15 | 45 | 75 | µs | Resistive load = 100Ω to GND | P_4.4.38 |
| Output delay time low side driver on | $t_{dONL}$ | 5 | 20 | 35 | µs | Resistive load = 100Ω to VS | P_4.4.39 |
| Output delay time low side driver off | $t_{dOFFL}$ | 15 | 45 | 75 | µs | Resistive load = 100Ω to VS | P_4.4.40 |
| Cross current protection time, high to low | $t_{DHL}$ | 100 | 130 | 160 | µs | Resistive load = 100Ω[3] | P_4.4.41 |
| Cross current protection time, low to high | $t_{DLH}$ | 100 | 130 | 160 | µs | Resistive load = 100Ω[3] | P_4.4.42 |
| **Input Interface: Logic Input EN** | | | | | | | |
| High-input voltage | $V_{ENH}$ | 0.7 * $V_{DD}$ | – | – | V | – | P_4.4.43 |
| Low-input voltage | $V_{ENL}$ | – | – | 0.3 * $V_{DD}$ | V | – | P_4.4.44 |
| Hysteresis of input voltage | $V_{ENHY}$ | – | 500 | – | mV | [3] | P_4.4.45 |
| Pull down resistor | $R_{PD\_EN}$ | 20 | 40 | 70 | kΩ | $V_{EN}$ = 0.2 x $V_{DD}$ | P_4.4.46 |
| **SPI frequency** | | | | | | | |
| Maximum SPI frequency | $f_{SPI,max}$ | – | – | 5.0 | MHz | [3] [5] | P_4.4.47 |
| **SPI INTERFACE: Delay Time from EN rising edge to first Data in** | | | | | | | |
| Setup time | $t_{set}$ | – | – | 150 | µs | [3] See **Figure 14** | P_4.4.48 |
| **SPI INTERFACE: Input Interface, Logic Inputs SDI, SCLK, CSN** | | | | | | | |
| H-input voltage threshold | $V_{IH}$ | 0.7 * $V_{DD}$ | – | – | V | – | P_4.4.50 |
| L-input voltage threshold | $V_{IL}$ | – | – | 0.3 * $V_{DD}$ | V | – | P_4.4.51 |
| Hysteresis of input voltage | $V_{IHY}$ | – | 500 | – | mV | [3] | P_4.4.52 |
| Pull up resistor at pin CSN | $R_{PU\_CSN}$ | 30 | 50 | 80 | kΩ | $V_{CSN}$ = 0.7 x $V_{DD}$ | P_4.4.53 |
| Pull down resistor at pin SDI, SCLK | $R_{PD\_SDI}$, $R_{PD\_SCLK}$ | 20 | 40 | 70 | kΩ | $V_{SDI}$, $V_{SCLK}$ = 0.2 x $V_{DD}$ | P_4.4.54 |
| Input capacitance at pin CSN, SDI or SCLK | $C_I$ | – | 10 | 15 | pF | 0V < $V_{DD}$ < 5.25V [3] | P_4.4.55 |
| **Input Interface, Logic Output SDO** | | | | | | | |
| H-output voltage level | $V_{SDOH}$ | $V_{DD}$ - 0.4 | $V_{DD}$ - 0.2 | – | V | $I_{SDOH}$ = -1.6 mA | P_4.4.56 |

**Table 5 Electrical Characteristics, $V_S$ =5.5 V to 18 V, $V_{DD}$ = 3.0V to 5.5V, $T_j$ = -40°C to +150°C, EN= HIGH, $I_{OUTn}$= 0 A; Typical values refer to $V_{DD}$ = 5.0 V, $V_S$ = 13.5 V and $T_J$ = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| L-output voltage level | $V_{SDOL}$ | – | 0.2 | 0.4 | V | $I_{SDOL}$ = 1.6 mA | P_4.4.57 |
| Tri-state Leakage Current | $I_{SDOLK}$ | -1 | – | 1 | µA | $V_{CSN} = V_{DD}$; 0V < $V_{SDO}$ < $V_{DD}$ | P_4.4.58 |
| Tri-state input capacitance | $C_{SDO}$ | – | 10 | 15 | pF | 3) | P_4.4.59 |
| **Data Input Timing. See Figure 15 and Figure 17.** | | | | | | | |
| SCLK Period | $t_{pCLK}$ | 200 | – | – | ns | 3) | P_4.4.60 |
| SCLK High Time | $t_{SCLKH}$ | 0.45 * $t_{pCLK}$ | – | 0.55 * $t_{pCLK}$ | ns | 3) | P_4.4.61 |
| SCLK Low Time | $t_{SCLKL}$ | 0.45 * $t_{pCLK}$ | – | 0.55 * $t_{pCLK}$ | ns | 3) | P_4.4.62 |
| SCLK Low before CSN Low | $t_{BEF}$ | 125 | – | – | ns | 3) | P_4.4.63 |
| CSN Setup Time | $t_{lead}$ | 250 | – | – | ns | 3) | P_4.4.64 |
| SCLK Setup Time | $t_{lag}$ | 250 | – | – | ns | 3) | P_4.4.65 |
| SCLK Low after CSN High | $t_{BEH}$ | 125 | – | – | ns | 3) | P_4.4.66 |
| SDI Setup Time | $t_{SDI\_setup}$ | 30 | – | – | ns | 3) | P_4.4.67 |
| SDI Hold Time | $t_{SDI\_hold}$ | 30 | – | – | ns | 3) | P_4.4.68 |
| Input Signal Rise Time at pin SDI, SCLK, CSN | $t_{rIN}$ | – | – | 50 | ns | 3) | P_4.4.69 |
| Input Signal Fall Time at pin SDI, SCLK, CSN | $t_{fIN}$ | – | – | 50 | ns | 3) | P_4.4.70 |
| Delay time from EN falling edge to standby mode | $t_{DMODE}$ | – | – | 8 | µs | 3) | P_4.4.71 |
| Minimum CSN High Time | $t_{CSNH}$ | 5 | – | – | µs | 3) | P_4.4.72 |
| **Data Output Timing. See Figure 15.** | | | | | | | |
| SDO Rise Time | $t_{rSDO}$ | – | 30 | 80 | ns | $C_{load}$ = 40pF 3) | P_4.4.73 |
| SDO Fall Time | $t_{fSDO}$ | – | 30 | 80 | ns | $C_{load}$ = 40pF 3) | P_4.4.74 |
| SDO Enable Time after CSN falling edge | $t_{ENSDO}$ | – | – | 75 | ns | Low Impedance 3) | P_4.4.75 |
| SDO Disable Time after CSN rising edge | $t_{DISSDO}$ | – | – | 75 | ns | High Impedance 3) | P_4.4.76 |
| Duty cycle of incoming clock at SCLK | $duty_{SCLK}$ | 45 | – | 55 | % | 3) | P_4.4.77 |
| SDO Valid Time for $V_{DD}$ = 3.3V | $t_{VASDO3}$ | – | 70 | 95 | ns | $V_{SDO}$ < 0.2 x $V_{DD}$ $V_{SDO}$ > 0.8 x $V_{DD}$ $C_{load}$ = 40pF 3) | P_4.4.78 |

**Table 5 Electrical Characteristics, $V_S$ =5.5 V to 18 V, $V_{DD}$ = 3.0V to 5.5V, $T_j$ = -40°C to +150°C, EN= HIGH, $I_{OUTn}$= 0 A; Typical values refer to $V_{DD}$ = 5.0 V, $V_S$ = 13.5 V and $T_J$ = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SDO Valid Time for $V_{DD}$ = 5V | $t_{VASDO5}$ | – | 50 | 65 | ns | $V_{SDO}$ < 0.2 x $V_{DD}$<br>$V_{SDO}$ > 0.8 $V_{DD}$<br>$C_{load}$ = 40pF 3) | P_4.4.79 |
| **Thermal warning & Shutdown** | | | | | | | |
| Thermal warning junction temperature | $T_{jW}$ | 120 | 140 | 170 | °C | See **Figure 11** 3) | P_4.4.80 |
| Thermal shutdown junction temperature | $T_{jSD}$ | 150 | 175 | 200 | °C | See **Figure 11** 3) | P_4.4.81 |
| Thermal comparator hysteresis | $T_{jHYS}$ | – | 5 | – | °C | 3) | P_4.4.82 |
| Ratio of SD to W temperature | $T_{jSD}$ / $T_{jW}$ | 1.05 | 1.20 | – | – | 3) | P_4.4.83 |

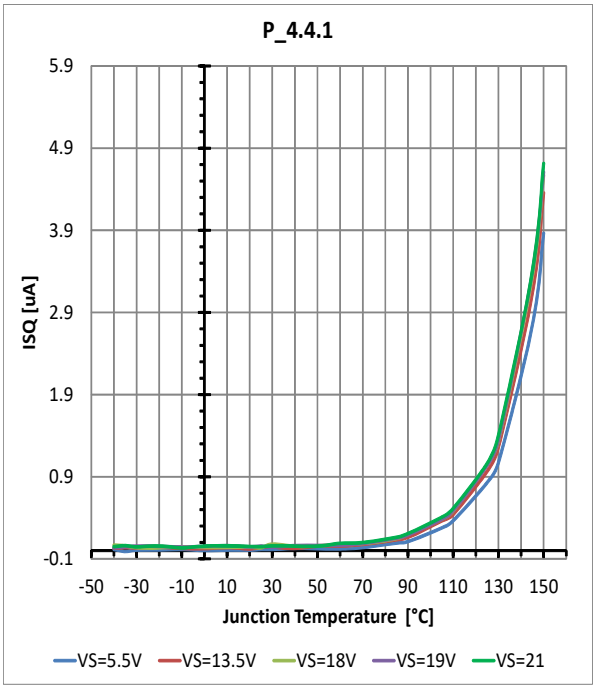
1) $I_{S\_HSON}$ does not include the load current
2) HS1, respectively HS2, is set to LED mode by setting OL_SEL_HS1 bit to 1, respectively OL_SEL_HS2 bit to 1
3) Not subject to production test, specified by design
4) Measured for 20% - 80% of $V_S$.
5) Not applicable in daisy chain configuration

# 4 Characterization results

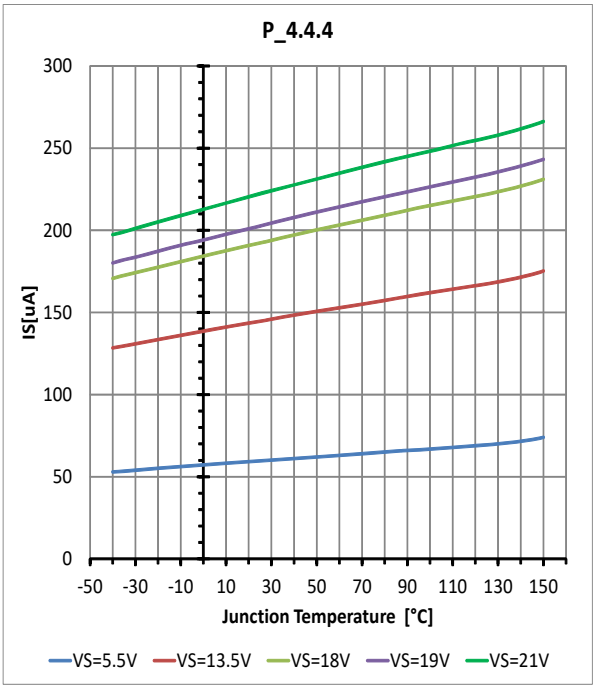
Performed on 7 devices from 2 lots, over operating temperature and nominal/extended supply range.

## Typical performance characteristics

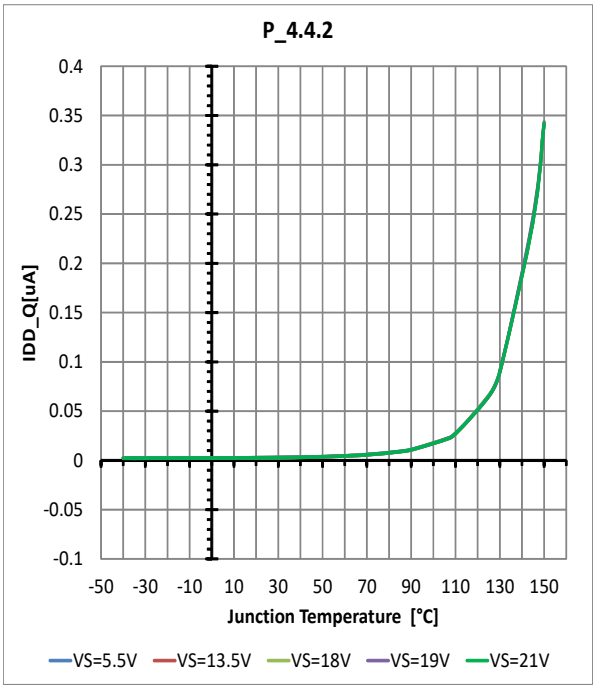
### Supply quiescent current



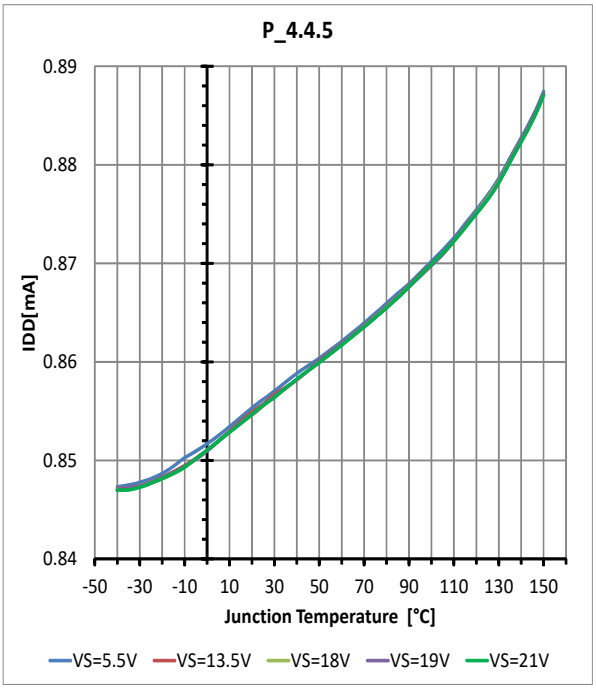

### Supply current




### Logic supply quiescent current

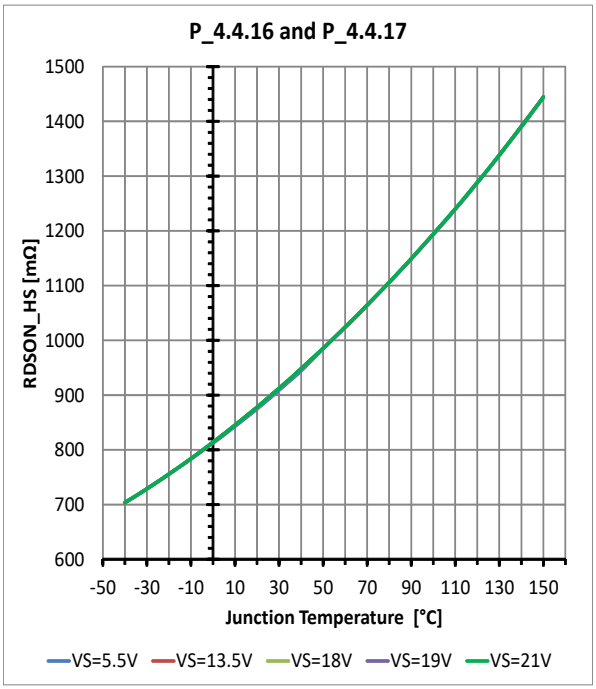



### Logic supply current

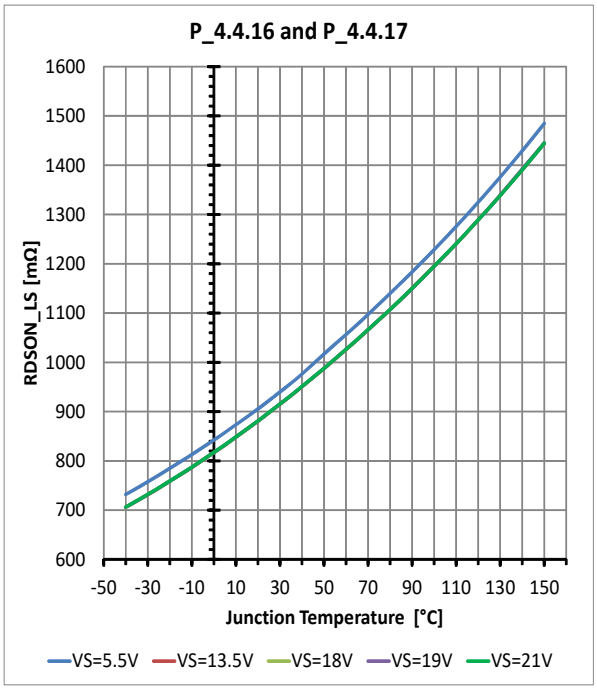


## Characterization results

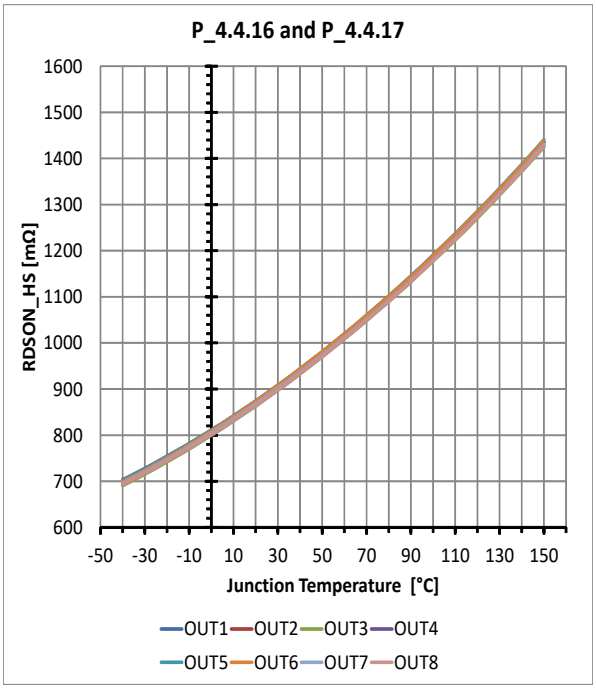
### HS static Drain-source ON-resistance



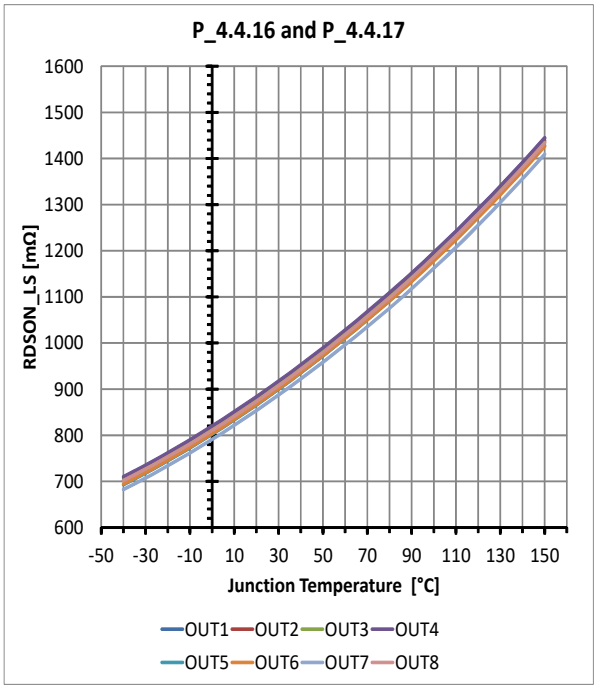

### LS static Drain-source ON-resistance




### HS static drain-source ON-resistance VS = 13.5V and VDD = 5V

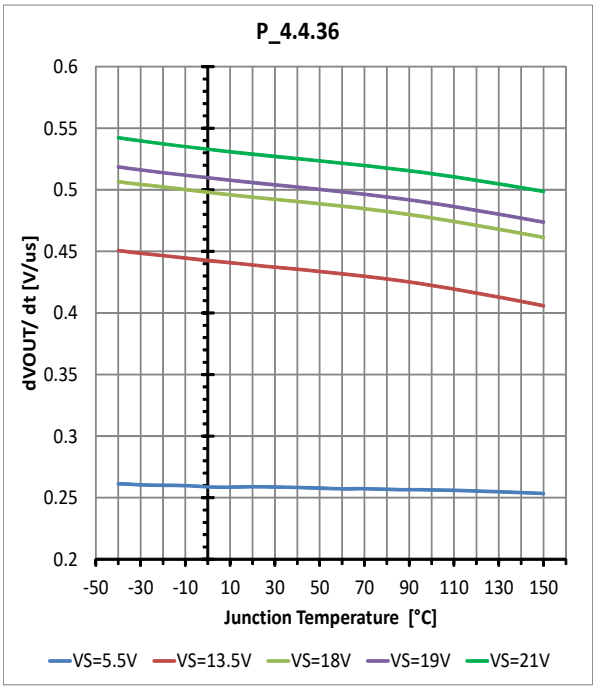



### LS static drain-source ON-resistance VS = 13.5V and VDD = 5V

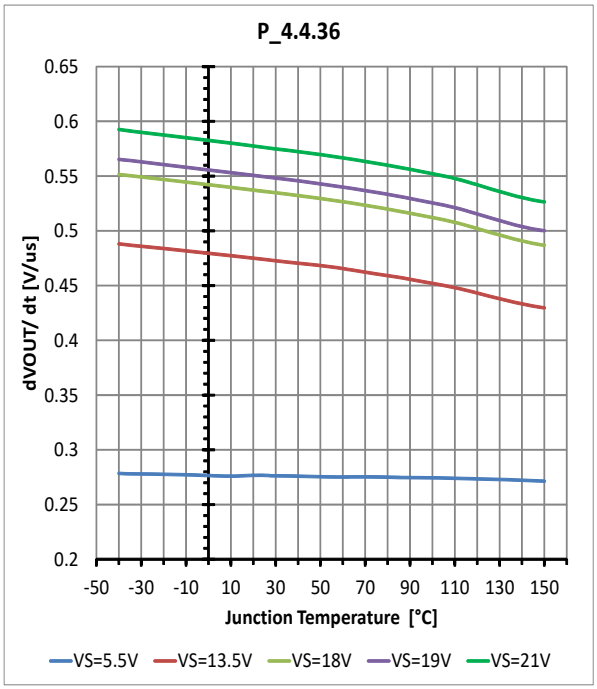


## Characterization results

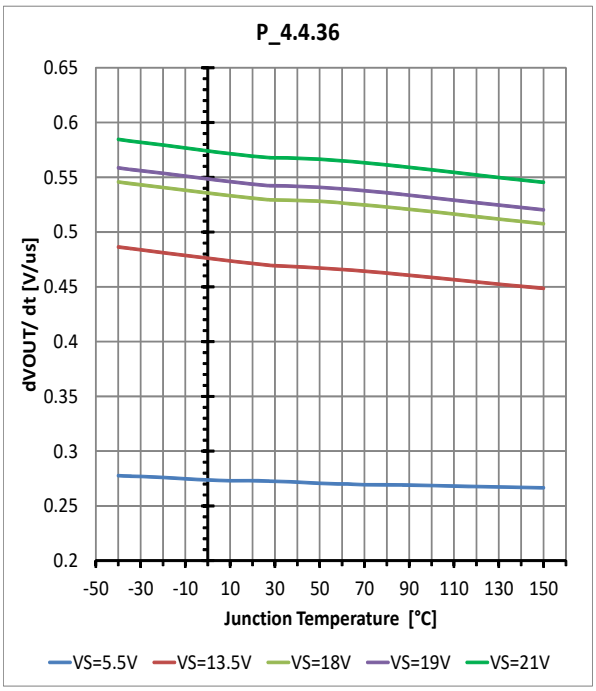
### Slew rate ON of high-side outputs



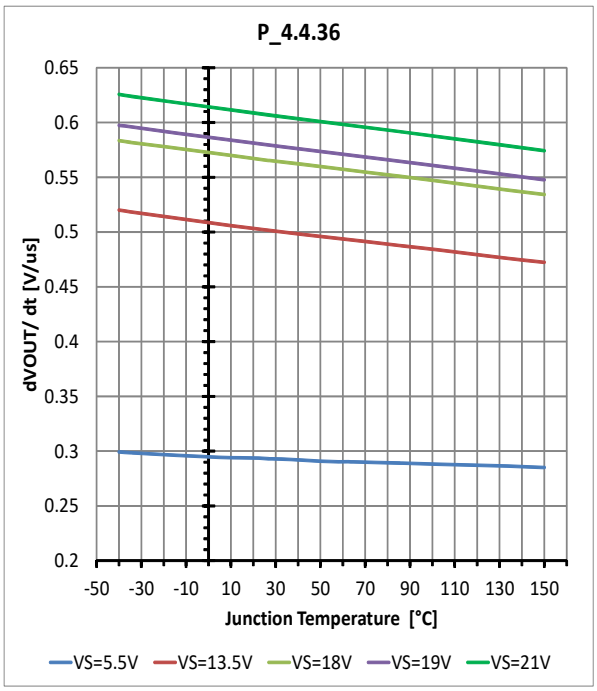

### Slew rate ON of low-side outputs




### Slew rate OFF of high-side outputs

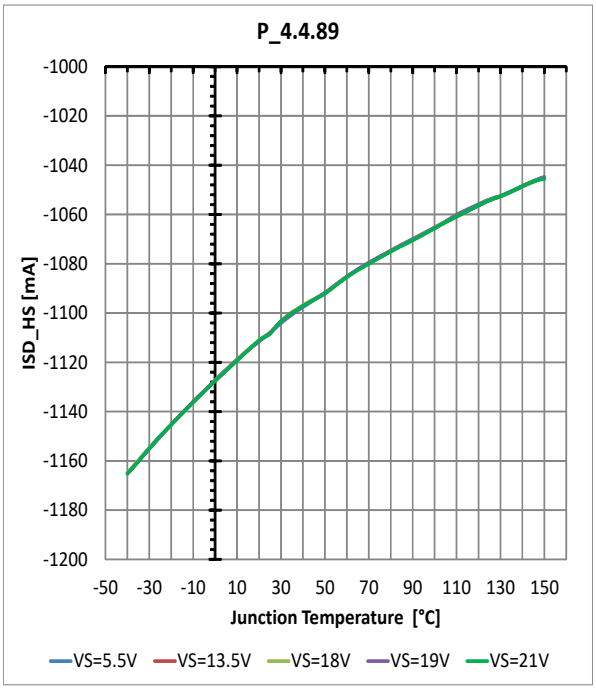



### Slew rate OFF of low-side outputs

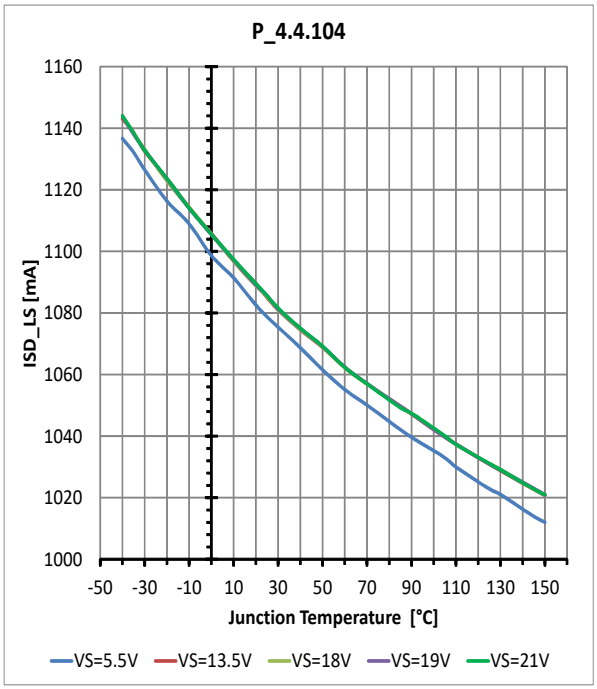


## Characterization results

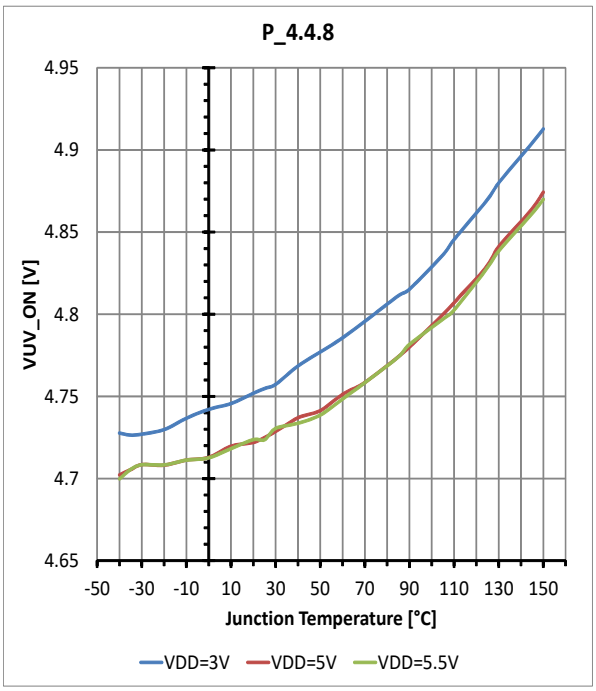
### HS overcurrent shutdown threshold



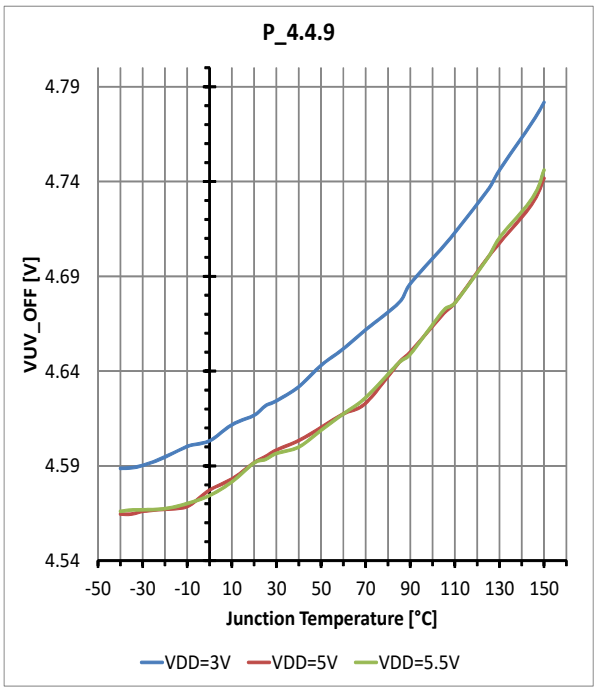

### LS overcurrent shutdown threshold




### Undervoltage switch ON voltage threshold

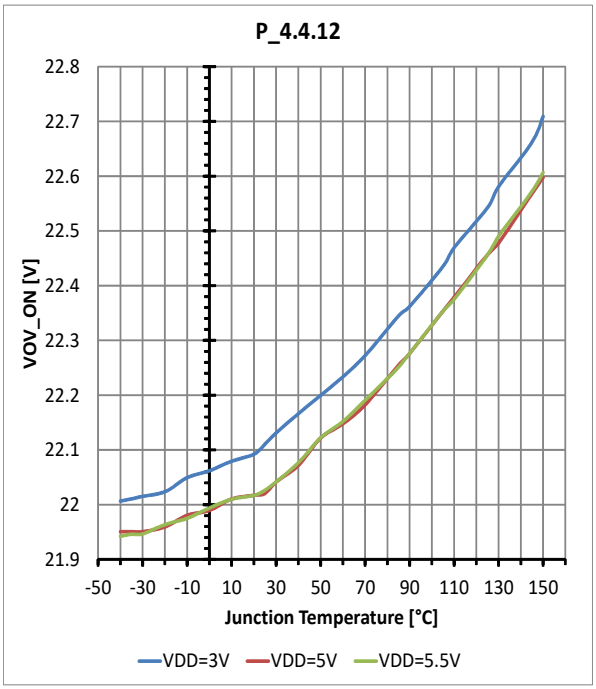



### Undervoltage switch OFF voltage threshold

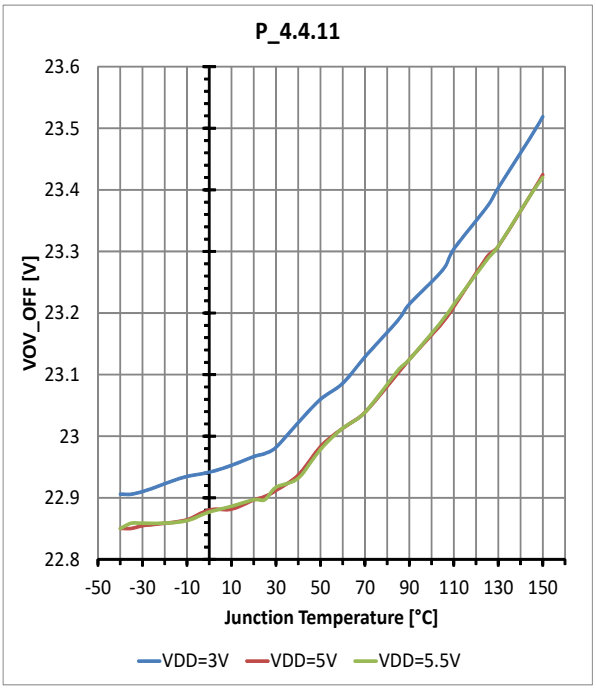


## Characterization results

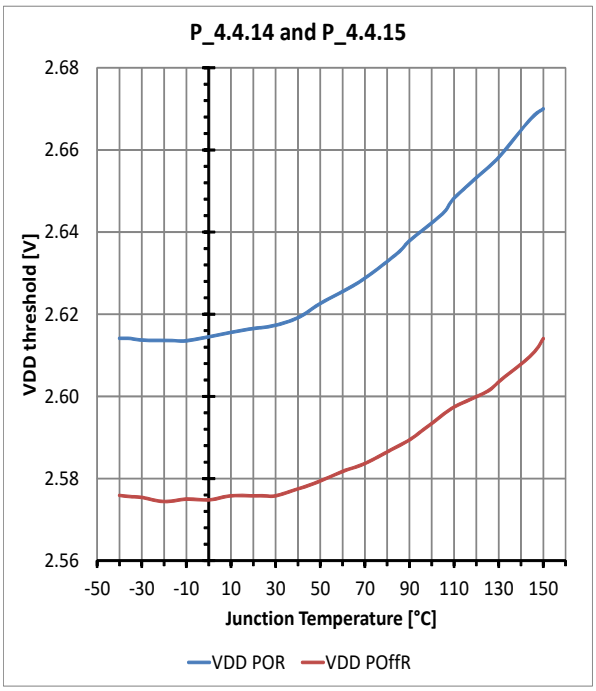
### Overvoltage switch ON voltage threshold




### Overvoltage switch OFF voltage threshold




### VDD Power-on-reset and VDD Power-off-reset



# 5 General Description

## 5.1 Power Supply

The TLE94108ES has two power supply inputs, $V_S$ and $V_{DD}$. The half bridge outputs are supplied by $V_S$, which is connected to the 12V automotive supply rail. $V_{DD}$ is used to supply the I/O buffers and internal voltage regulator of the device.

$V_S$ and $V_{DD}$ supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on $V_S$. The system can therefore continue to operate once $V_S$ has recovered, without having to resend commands to the device.

A rising edge on $V_{DD}$ crossing $V_{DD\ POR}$ triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched off (high impedance).

An electrolytic and 100nF ceramic capacitors are recommended to be placed as close as possible to the $V_S$ supply pin of the device for improved EMC performance in the high and low frequency band. The electrolytic capacitor must be dimensioned to prevent the VS voltage from exceeding the absolute maximum rating. In addition, decoupling capacitors are recommended on the $V_{DD}$ supply pin.

## 5.2 Operation modes

### 5.2.1 Normal mode

The TLE94108ES enters normal mode by setting the EN input High. In normal mode, the charge pump is active and all output transistors can be configured via SPI.

### 5.2.2 Sleep mode

The TLE94108ES enters sleep mode by setting the EN input Low. The EN input has an internal pull-down resistor.

In sleep mode, all output transistors are turned off and the SPI register banks are reset. The current consumption is reduced to $I_{SQ} + I_{DD\_Q}$.

## 5.3 Reset Behaviour

The following reset triggers have been implemented in the TLE94108ES:

**$V_{DD}$ Undervoltage Reset:**

The SPI Interface shall not function if $V_{DD}$ is below the undervoltage threshold, $V_{DD\ POffR}$. The digital block will be deactivated, the logic contents cleared and the output stages are switched off . The digital block is initialized once $V_{DD}$ voltage levels is above the undervoltage threshold, $V_{DD\ POR}$. Then the NPOR bit is reset (NPOR = 0 in **SYS_DIAG1** and Global Status Register).

**Reset on EN pin:**

If the EN pin is pulled Low, the logic content is reset and the device enters sleep mode.

The reset event is reported by the NPOR bit (NPOR = 0) once the TLE94108ES is in normal mode (EN = High; VDD > $V_{DD\ POR}$).

## 5.4 Reverse Polarity Protection

The TLE94108ES requires an external reverse polarity protection. During reverse polarity, the free-wheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow ($I_{RB}$) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended (see **Figure 4**).

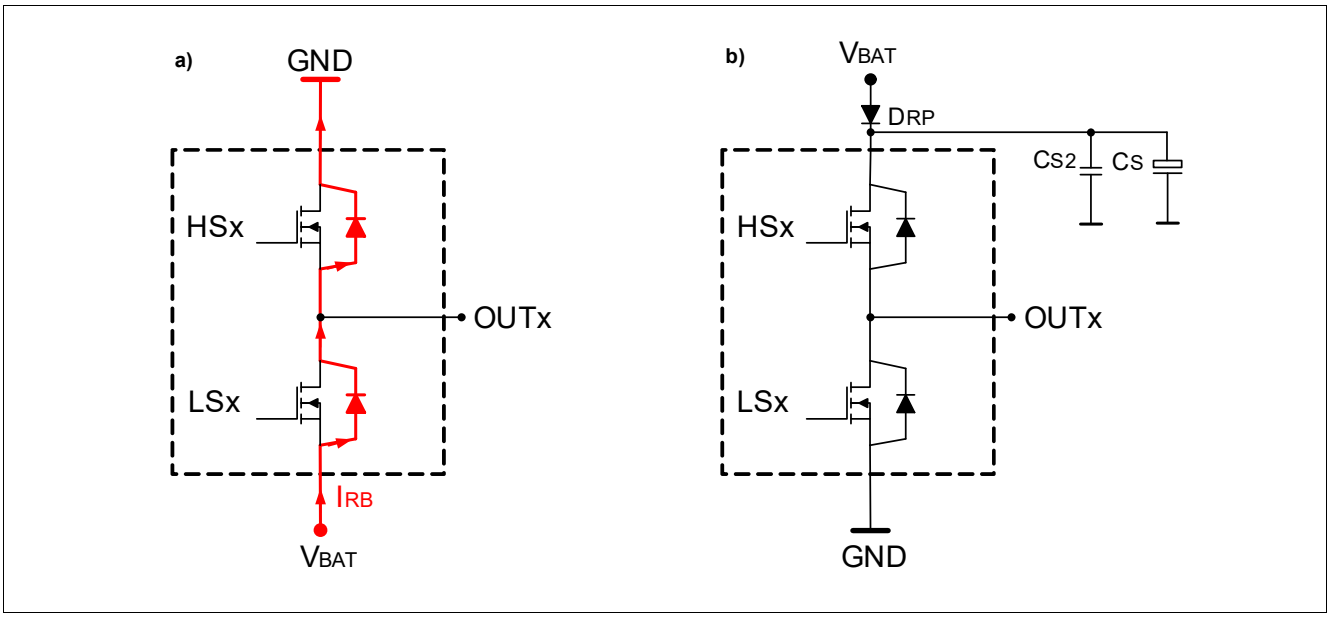



**Figure 4 Reverse Polarity Protection**

# 6 Half-Bridge Outputs

## 6.1 Functional Description

The half-bridge outputs of the TLE94108ES are intended to drive motor loads. These outputs can either be driven continuously or PWM enabled via SPI.

If the outputs are driven continuously via SPI, for example HS1 and LS2 used to drive a motor, then the following suggested SPI commands shall be sent:

- Activate HS1: Bit HB1_HS_EN in HB_ACT_1_CTRL register
- Activate LS2: Bit HB2_LS_EN in HB_ACT_1_CTRL register

### 6.1.1 Half-bridge operation with PWM enabled

All half-bridge outputs of the TLE94108ES are capable of PWM operation. They can either be used to drive an inductive load (e.g. DC brush motor) or optionally a resistive load (e.g. LED). Each half-bridge output has been allocated a maximum of three PWM channels with individual duty cycle settings with 8-bit resolution. Each channel is further mapped to a maximum of three PWM frequency options, i.e. 80Hz,100Hz and 200Hz. This feature enables a highly flexible PWM operation while driving loads with varying control profiles.

PWM frequency and duty cycle can be changed on demand during PWM operation of the desired half-bridge output. Glitches on the PWM output waveform, which may arise as a result of on-demand changes in PWM operation, will be prevented by the internal logic circuitry.

When operating with motor loads, active or passive free-wheeling configuration is available via SPI to select the speed at which the inductive current can decay over the full-bridge circuit. The default setting is passive free-wheeling.

*Note: Active free-wheeling is effectively applied if the selected duty cycle corresponds to turn-on times of the HS and the LS, which are longer than the sum of the cross conduction times tDHL + tDLH.*

**Table 6 PWM capability and frequency selection per half-bridge output**

| Control Register: HBx_MODEn (n=0,1) | PWM Frequency 80Hz (Control Register: PWM_CH_FREQ_CTRL) | PWM Frequency 100Hz (Control Register: PWM_CH_FREQ_CTRL) | PWM Frequency 200Hz (Control Register: PWM_CH_FREQ_CTRL) |
|---|---|---|---|
| PWM Channel 1 | PWM_CH1_FREQ_n (n=0,1) Bit '$01_B$' | PWM_CH1_FREQ_n (n=0,1) Bit '$10_B$' | PWM_CH1_FREQ_n (n=0,1) Bit '$11_B$' |
| PWM Channel 2 | PWM_CH2_FREQ_n (n=0,1) Bit '$01_B$' | PWM_CH2_FREQ_n (n=0,1) Bit '$10_B$' | PWM_CH2_FREQ_n (n=0,1) Bit '$11_B$' |
| PWM Channel 3 | PWM_CH3_FREQ_n (n=0,1) Bit '$01_B$' | PWM_CH3_FREQ_n (n=0,1) Bit '$10_B$' | PWM_CH3_FREQ_n (n=0,1) Bit '$11_B$' |

### 6.1.1.1 Inductive Load

An illustration is shown in **Figure 5** with OUT1 and OUT2 driving a DC brush motor. With this configuration, HS1 is permanently driven while LS2 is driven in PWM operation. HS2 serves to actively free-wheel (FW) the motor current load, reducing the power dissipation of the device.

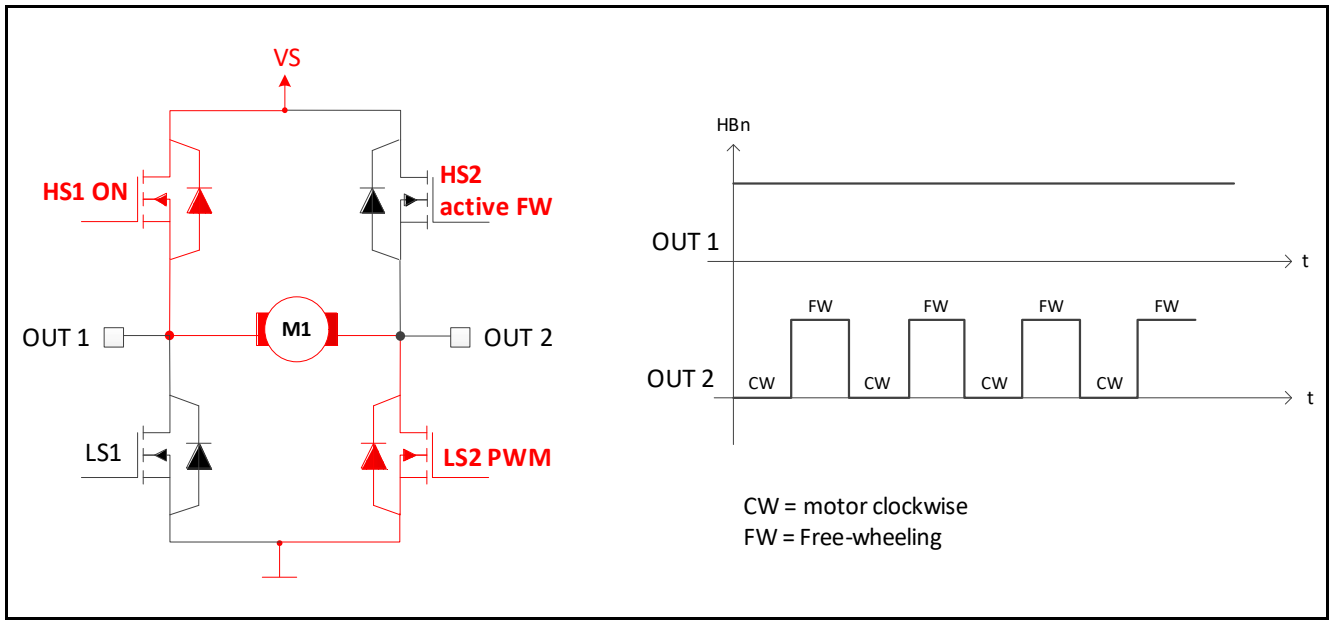



**Figure 5 PWM operation on OUT 2**

Assuming HBx Mode = 00 and both HSx and LSx are considered off (tri-state). The suggested SPI control commands for proper PWM operation are:

**Option 1: The considered output is not put in parallel with another one**

- Configure the frequency to 00 (PWM is stopped and off) for selected PWM channel
- Configure active or passive free-wheeling of the inductive decay current in FW_CTRL register
- Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_CTRL register
- Configure the duty cycle of the selected half-bridge output in PWM_DC_CTRL register
- Select the PWM frequency in PWM_CH_FREQ_CTRL register to begin the PWM period
- Activate the channel to be driven in PWM operation: HSn or LSn in the HB_ACT_CTRL register

**Option 2: Outputs controlled by different control registers are put paralleled. This sequence ensures that corresponding HS or LS are activated simultaneously**

- Configure the frequency 00 (PWM is stopped and off) for selected PWM channel
- Configure active or passive free-wheeling of the inductive decay current in FW_CTRL register
- Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_CTRL register
- Configure the duty cycle of the selected half-bridge output in PWM_DC_CTRL register
- Activate the channel to be driven in PWM operation: HSn or LSn in the HB_ACT_CTRL register
- Select the PWM frequency in PWM_CH_FREQ_CTRL register to begin the PWM period

Careful attention should be paid to the free-wheeling configuration of the half-bridge required to be driven in PWM operation. For example, in the event a high-side channel is activated and assigned a PWM channel, and active free-wheeling is selected, but a frequency mode of ‘00’ (PWM is stopped and off) is configured in the

PWM_CH_FREQ_CTRL register, then the respective high-side channel will be configured low and the adjacent low-side channel within the half-bridge will be enabled. This is a result of enabling active free-wheeling.

### 6.1.1.2 LED mode (optional)

Outputs, OUT1 and OUT2, are designed to optionally drive low current loads such as LEDs. The high-side channels, HS1 and HS2 are equipped with a lower open load threshold detection current and shorter filter time, specifically for low current loads such as LEDs. See OL_SEL_HS1 and OL_SEL_HS2 bits in FW_OL_CTRL register. Setting HS1 or HS2 in LED mode increases the $R_{DSON}$ and decreases the open load detection threshold. An illustration is shown in **Figure 6** with OUT1 driving an LED. With this configuration, HS1 is driven in PWM operation while LS1 is deactivated.

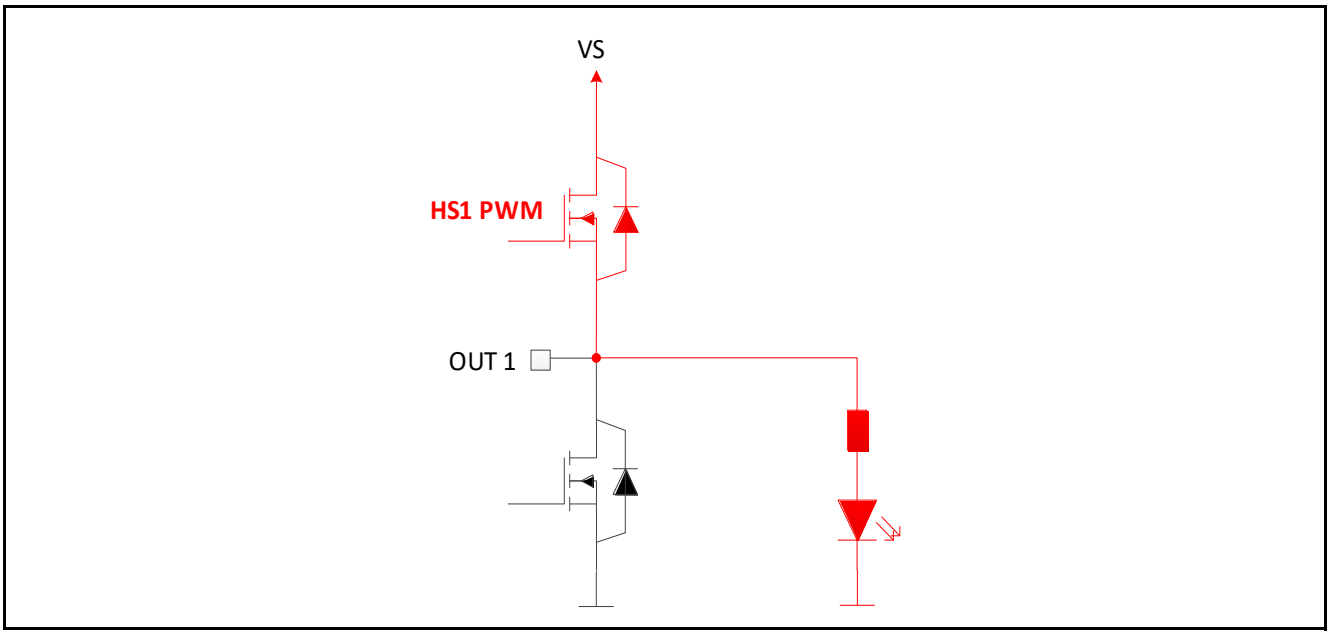



**Figure 6 PWM operation on OUT 1**

Assuming HBx Mode = 00 and both HSx and LSx are considered off (tri-state). The suggested SPI control commands are:

- Configure frequency 00 (PWM is stopped and off) for selected channel to ensure PWM is off.
- Assign an appropriate PWM channel for selected HS1 or HS2 output in HB_MODE_CTRL register
- Configure duty cycle of selected HS1 or HS2 output in PWM_DC_CTRL register
- Activate channel to be driven in PWM operation: HS1 or HS2 in the HB_ACT_CTRL register
- Select low current open load detection threshold for HS1 or HS2 in FW_OL_CTRL register
- Select PWM frequency in PWM_CH_FREQ_CTRL register to begin the PWM period.

## 6.2 Protection & Diagnosis

The TLE94108ES is equipped with an SPI interface to control and diagnose the state of the half-bridge drivers.

This device has embedded protective functions which are designed to prevent IC destruction under fault conditions described in the following sections. Fault conditions are treated as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

The following table provides a summary of fault conditions, protection mechanisms and recovery states embedded in the TLE94108ES device.

**Table 7 Summary of diagnosis and monitoring of outputs**

| Fault condition | Error Flag (EF) behaviour | Error bit: Status Register | Output Protection mechanism | Output error state | Output and error flag (EF) recovery |
|---|---|---|---|---|---|
| Overcurrent | Latch | 1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register<br>2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OC and HBn_LS_OC bits in SYS_DIAG_2, SYS_DIAG_3 status registers. | Error output shutdown and latched | High-Z | Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage. |
| Open load | Latch | 1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register<br>2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OL and HBn_LS_OL bits in SYS_DIAG_5, SYS_DIAG_6 status registers. | None | No state change | An open load detection does not change the state of the output.<br>EF to be cleared. |
| Temperature pre-warning | Latch | Global error bit 1, TPW in SYS_DIAG_1: Global Status 1 register | None | No state change | Not applicable |
| Temperature shutdown | Latch | Global error bit 2, TSD in SYS_DIAG_1: Global Status 1 register | All outputs shutdown and latched. | High-Z | Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage. |

**Table 7 Summary of diagnosis and monitoring of outputs** (cont'd)

| Fault condition | Error Flag (EF) behaviour | Error bit: Status Register | Output Protection mechanism | Output error state | Output and error flag (EF) recovery |
|---|---|---|---|---|---|
| Power supply failure due to undervoltage | Latch | Global error bit 5, VS_UV in SYS_DIAG_1: Global Status 1 register | All outputs shutdown and automatically recovers. | High-Z | Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared. |
| Power supply failure due to overvoltage | Latch | Global error bit 4, VS_OV in SYS_DIAG_1: Global Status 1 register | All outputs shutdown and automatically recover. | High-Z | Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared. |

### 6.2.1 Short Circuit of Output to Supply or Ground

The high-side switches are protected against short to ground whereas the low-side switches are protected against short to supply.

The high-side and low-side power switches will enter into an over-current condition if the current within the switch exceeds the overcurrent shutdown detection threshold, $I_{SD}$. Upon detection of the $I_{SD}$ threshold, an overcurrent shutdown filter, $t_{dSD}$ is begun. As the current rises beyond the threshold $I_{SD}$, it will be limited by the current limit threshold, $I_{LIM}$. Upon expiry of the overcurrent shutdown filter time, the affected power switch is latched off and the corresponding error bit, HBn_HS_OC or HBn_LS_OC is set and latched. See **Figure 7** and **Figure 8** for more detail. A global load error bit, LE, contained in the global status register, SYS_DIAG_1, is also set for ease of error scanning by the application software. The power switch remains deactivated as long as the error bit is set.

To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists) the microcontroller shall clear the error bit in the respective status register to reactivate the desired power switch.

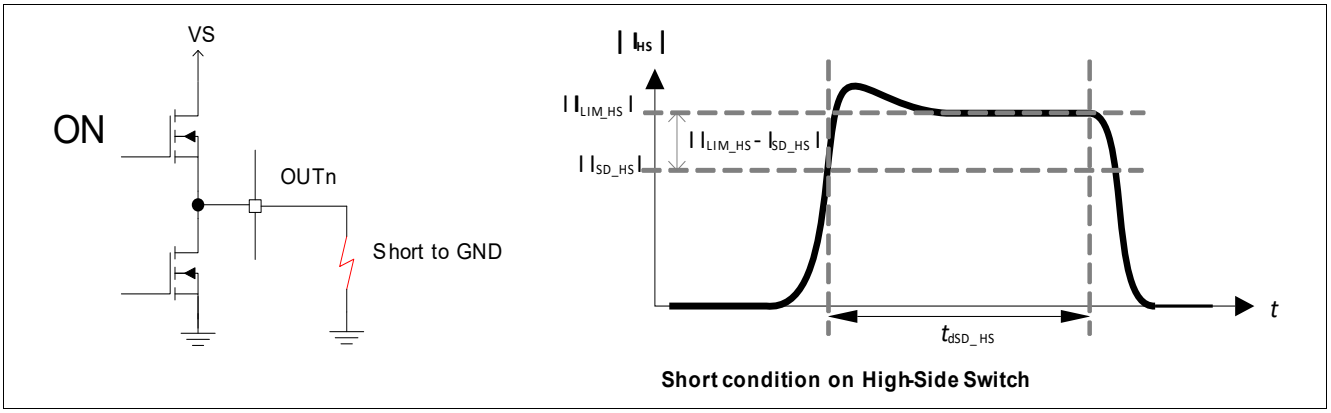



**Figure 7 High-Side Switch - Short Circuit and Overcurrent Protection**

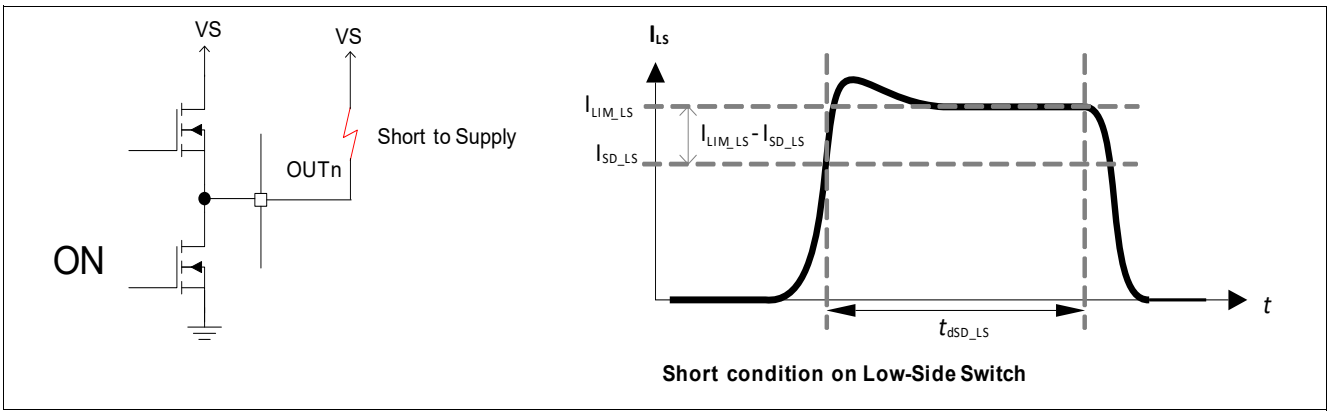



**Figure 8 Low-Side Switch - Short Circuit and Overcurrent Protection**

## Half-Bridge Outputs

**Table 8 Control and Status register bit state in the event of an overcurrent condition for an activated power switch**

| REGISTER TYPE | REGISTER NAME | Bit | BEFORE OVERCURRENT | DURING OVERCURRENT | AFTER OVERCURRENT |
|---|---|---|---|---|---|
| | | | Bit State | Bit State | Bit State |
| Control | HB_ACT_CTRL_n | HBn_HS_EN<br>HBn_LS_EN | 1 | 1 | 1 (corresponding half-bridge deactivated) |
| Status | SYS_DIAG_1: Global Status 1 | LE | 0 | 0 | 1 |
| Status | SYS_DIAG_x where x=2,3 | HBn_HS_OC<br>HBn_LS_OC | 0 | 0 | 1 |

### 6.2.2 Cross-Current

In bridge configurations the high-side and low-side power transistors are ensured never to be simultaneously “ON” to avoid cross currents. This is achieved by integrating delays in the driver stage of the power outputs to create a dead-time between switching off of one power transistor and switching on of the adjacent power transistor within the half-bridge. The dead times, $t_{DHL}$ and $t_{DLH}$, as shown in **Figure 9** case 3 and **Figure 10** case 3, have been specified to ensure that the switching slopes do not overlap with each other. This prevents a cross conduction event.

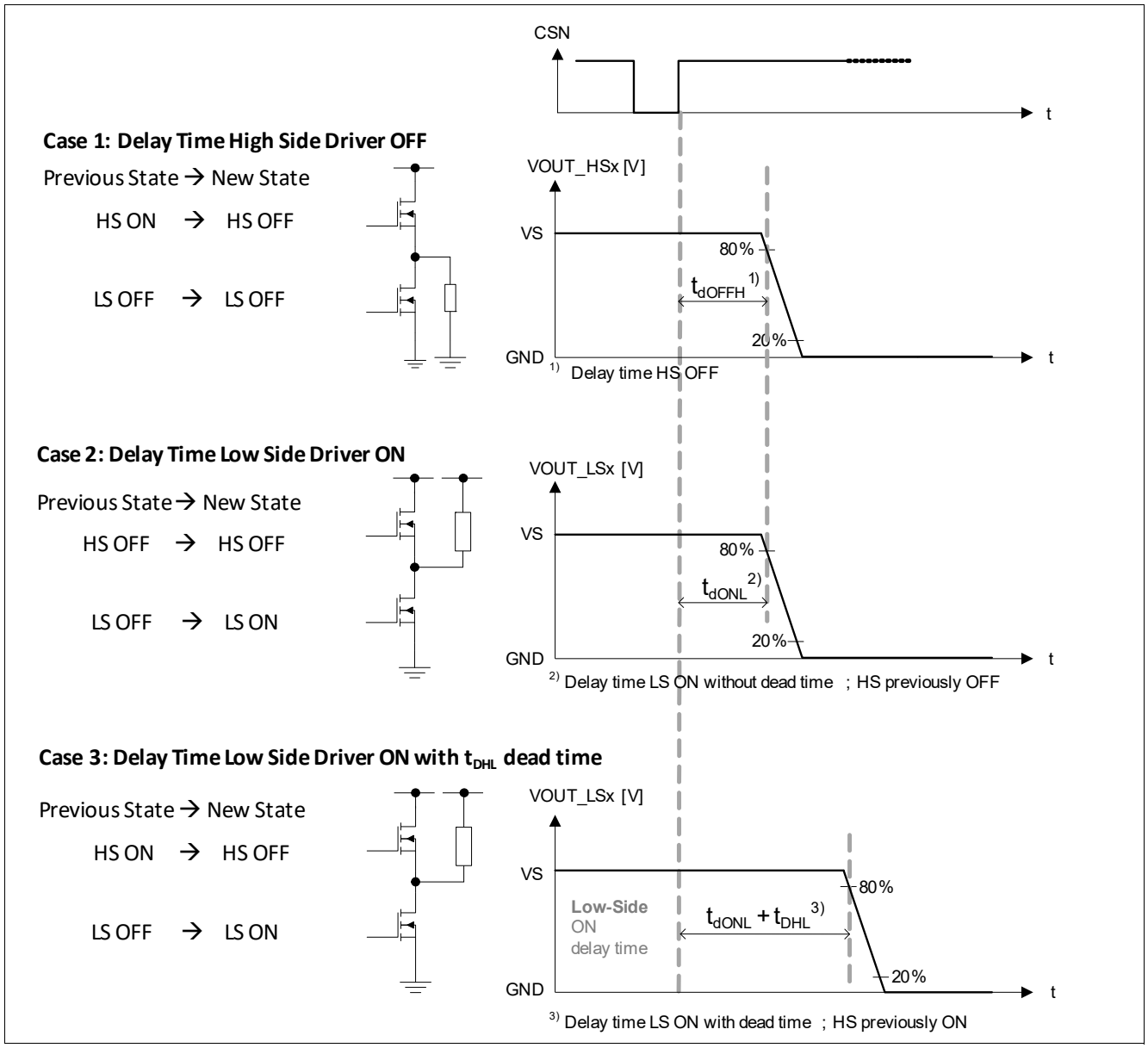



**Figure 9 Half bridge outputs switching times - high-side to low-side transition**

## Half-Bridge Outputs

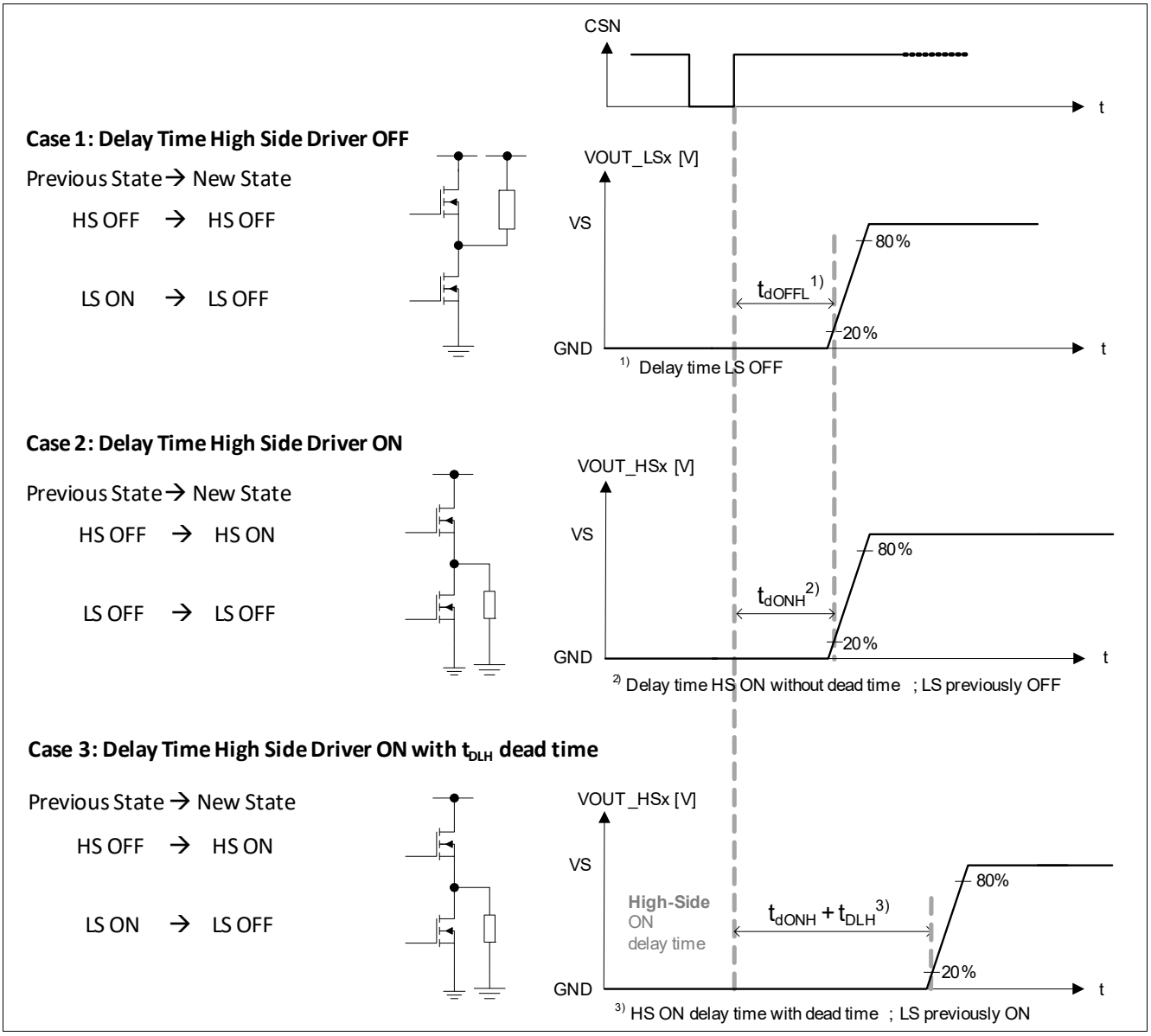



**Figure 10 Half bridge outputs switching times- low-side to high-side transition**

### 6.2.3 Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, TPW is set. This bit is latched and can only be cleared via SPI. The outputs stages however remain activated.

If one or more temperature sensors reach the shut-down temperature threshold, **all outputs are latched off**. The TSD bit in SYS_DIAG_1: Global Status 1 is set. All outputs remain deactivated until the TSD bit is cleared. See **Figure 11**.

To resume normal functionality of the power switch (in the event the overtemperature condition disappears, or to verify if the failure still exists) the microcontroller shall clear the TSD error bit in the status register to reactivate the respective power switch.

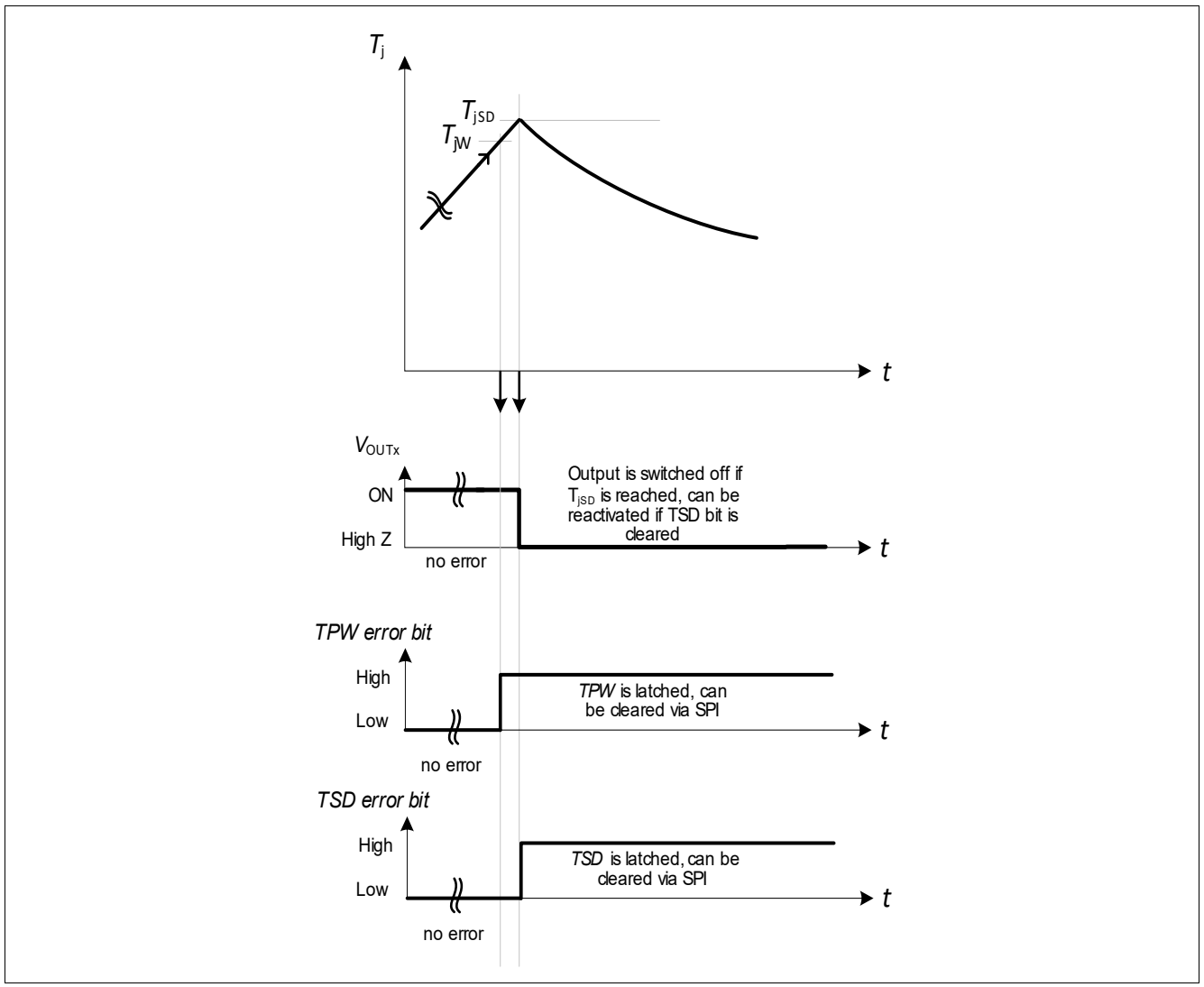



**Figure 11 Overtemperature Behavior**

**Table 9 Control and Status register bit state in the event of an overtemperature condition for an activated power switch**

| REGISTER TYPE | REGISTER NAME | Bit | $T_j < T_{jW}$ | $T_j > T_{jW}$ | $T_j > T_{jSD}$ | $T_j < T_{jSD} - T_{jHYS}$ |
|---|---|---|---|---|---|---|
| | | | Bit State | Bit State | Bit State | Bit State |
| Control | HB_ACT_CTRL_n | HBn_HS_EN<br>HBn_LS_EN | 1 | 1 | 1<br>(all outputs are latched off) | '1' (outputs are latched off unless error is cleared) |
| Status | SYS_DIAG_1: Global status 1 | TPW | 0 | 1<br>(latched) | 1<br>(latched) | '0' if error is cleared and $T_j < T_{jW}$, else '1' |
| Status | SYS_DIAG_1: Global status 1 | TSD | 0 | 0 | 1<br>(latched) | '0' if error is cleared, else '1' |

### 6.2.4 Overvoltage and undervoltage shutdown

The power supply rails $V_S$ and $V_{DD}$ are monitored for supply fluctuations. The $V_S$ supply is monitored for under- and over-voltage conditions where as the $V_{DD}$ supply is monitored for under-voltage conditions.

#### 6.2.4.1 $V_S$ Undervoltage

In the event the supply voltage $V_S$ drops below the switch off voltage $V_{UV\ OFF}$, all output stages are switched off, however, the logic information remains intact and uncorrupted. The $V_S$ under-voltage error bit, VS_UV, located in SYS_DIAG_1: Global Status 1 status register, will be set and latched. If $V_S$ rises again and reaches the switch on voltage $V_{UV\ ON}$ threshold, the power stages will automatically be activated. The VS_UV error bit should be cleared to verify if the supply disruption is still present. See **Figure 12**.

#### 6.2.4.2 $V_S$ Overvoltage

In the event the supply voltage $V_S$ rises above the switch off voltage $V_{OV\ OFF}$, all output stages are switched off. The $V_S$ over-voltage error bit, VS_OV, located in SYS_DIAG_1: Global Status 1 status register, will be set and latched. If $V_S$ falls again and reaches the switch on voltage $V_{OV\ ON}$ threshold, the power stages will automatically be activated. The VS_OV error bit should be cleared to verify if the overvoltage condition is still present. See **Figure 12**.

#### 6.2.4.3 $V_{DD}$ Undervoltage

In the event the VDD logic supply decreases below the undervoltage threshold, $V_{DD\ POffR}$, the SPI interface shall no longer be functional and the TLE94108ES will enter reset.

The digital block will be initialized and the output stages are switched off to High impedance. The undervoltage reset is released once $V_{DD}$ voltage levels are above the undervoltage threshold, $V_{DD\ POR}$.

The reset event is reported in SYS_DIAG1 by the NPOR bit (NPOR = 0) once the TLE94108ES is in normal mode (EN = High ; VDD > $V_{DD\ POR}$).

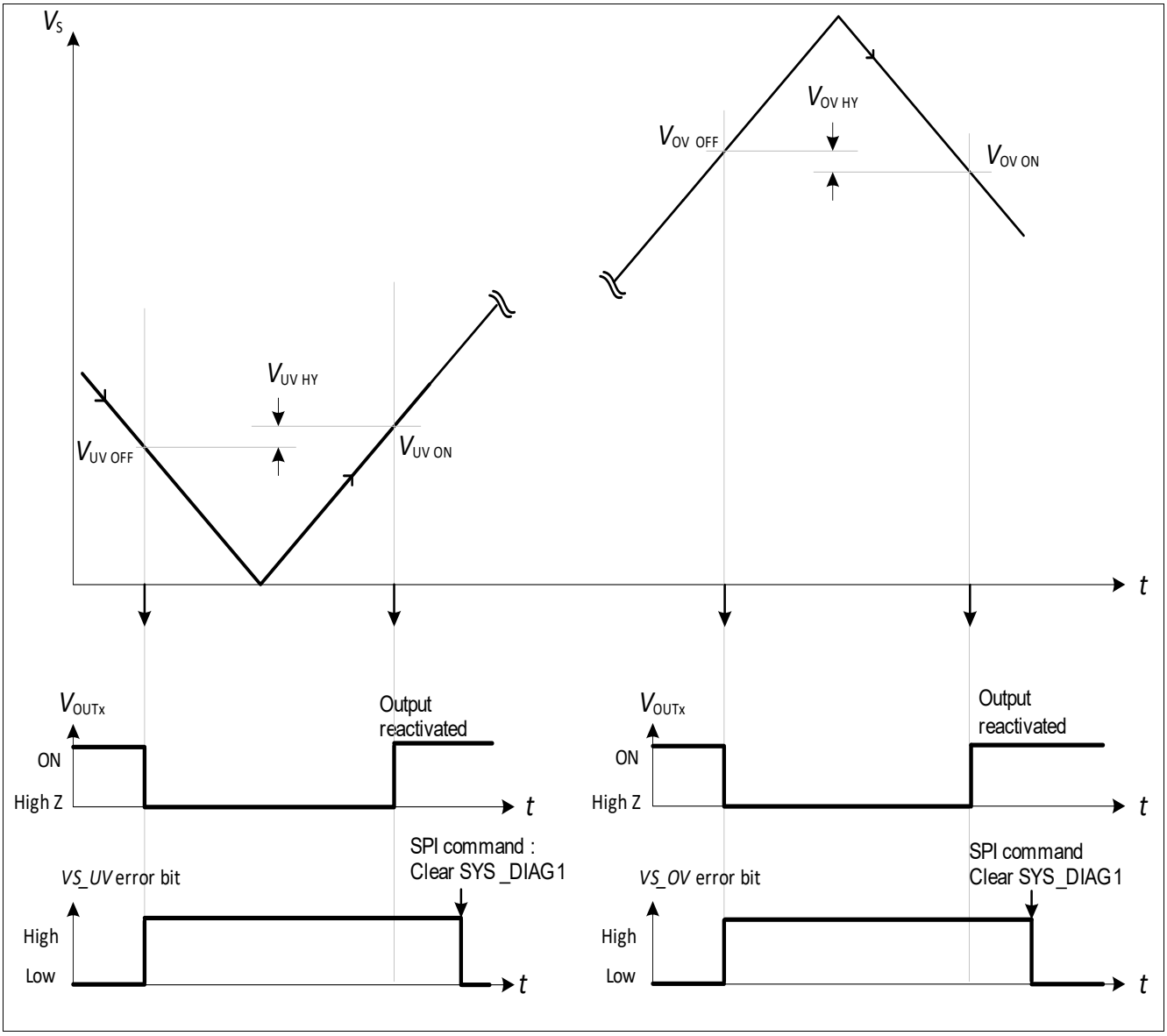



**Figure 12 Output behavior during under- and overvoltage $V_S$ condition**

### 6.2.5 Open Load

Both high-side and low-side switches of the half-bridge power outputs are capable of detecting an open load in their activated state. If a load current lower than the open load detection threshold, $I_{OLD}$ for at least $t_{dOLD}$ is detected at the activated switch, the corresponding error bit, HBn_HS_OL or HBn_LS_OL is set and latched. A global load error bit, LE, in the global status register, SYS_DIAG_1: Global Status 1, is also set for ease of error scanning by the application software. The half-bridge output however, remains activated.

The microcontroller must clear the error bit in the respective status register to determine if the open load is still present or disappeared.

High-side outputs, HS1 and HS2, are specifically designed to detect open load thresholds for LED loads. Both HS1 and HS2 have a unique and lower open load current threshold and filter time which are configurable via SPI in control register, FW_OL_CTRL.

During PWM operation, the open load detection is blanked and will not be visible in the status register for power stages used in active free-wheeling

# 7 Serial Peripheral Interface (SPI)

The TLE94108ES has a 16-bit SPI interface for output control and diagnostics. This section describes the SPI protocol, the control and status registers.

## 7.1 SPI Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input SCLK provided by the microcontroller. SCLK must be Low during CSN falling edge (Clock Polarity = 0). The SPI incorporates an in-frame response: the content of the addressed register is shifted out at SDO within the same SPI frame (see **Figure 19** and **Figure 21**).The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), Low active. After the CSN input returns from Low to High, the word that has been read is interpreted according to the content. The SDO output switches to tri-state status (High impedance) at this point, thereby releasing the SDO bus for other use.The state of SDI is shifted into the input register with every falling edge on SCLK. The state of SDO is shifted out of the output register at every rising edge on SCLK (Clock Phase = 1). The SPI protocol of the TLE94108ES is compatible with independent slave configuration and with daisy chain. Daisy chaining is applicable to SPI devices with the same protocol.

Writing, clearing and reading is done byte wise. The SPI configuration and status bits are not cleared automatically by the device and therefore must be cleared by the microcontroller, e.g. if the TSD bit was set due to over temperature (refer to the respective register description for detailed information).

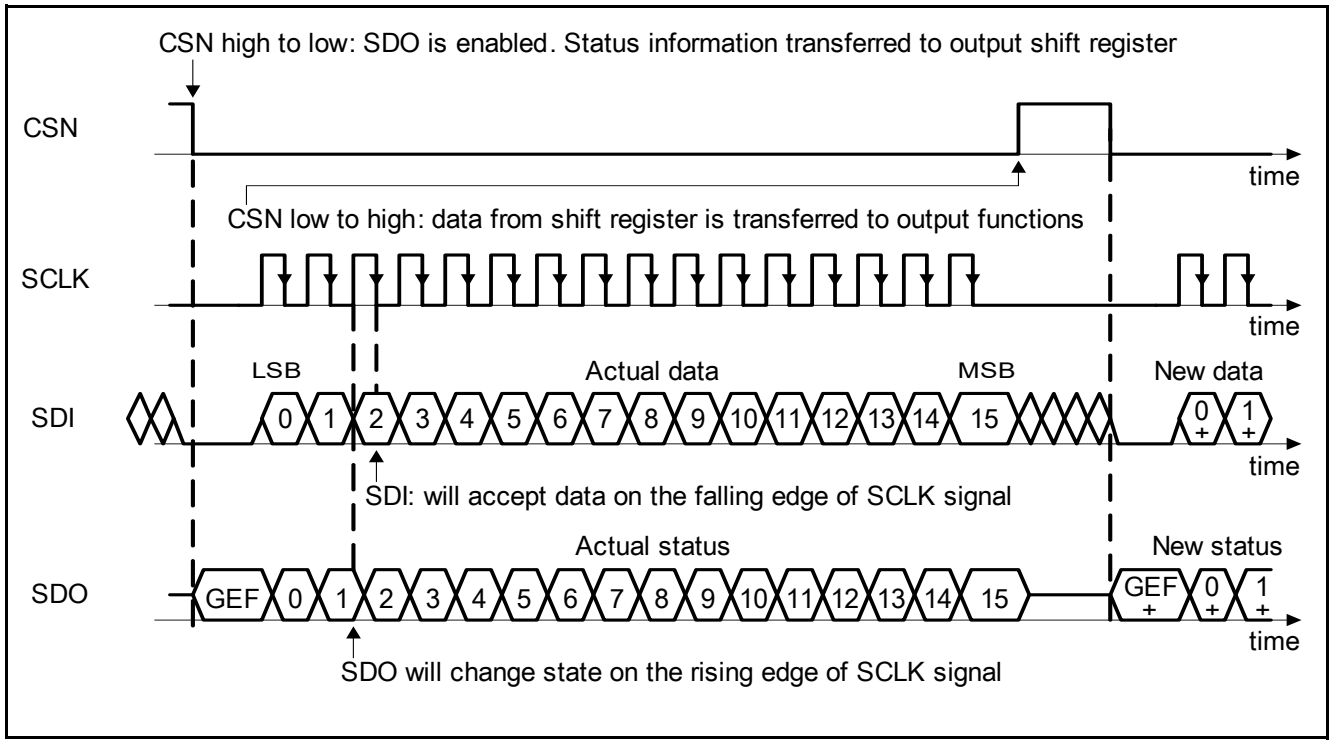



**Figure 13 SPI Data Transfer Timing (note the reversed order of LSB and MSB as shown in this figure compared to the register description)**

SPI messages are only recognized if a minimum set time, tSET, is observed upon rising edge of the EN pin (**Figure 14**).

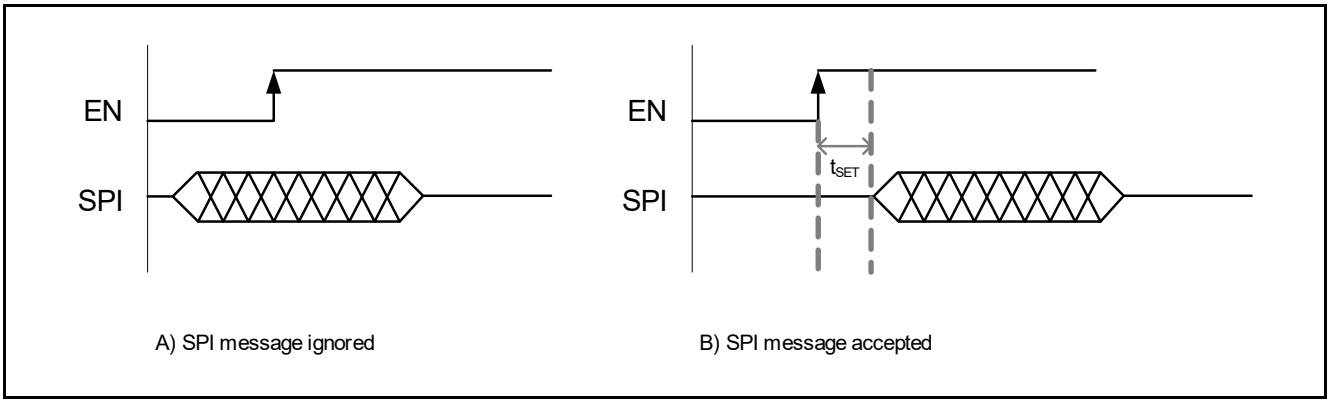



**Figure 14 Setup time from EN rising edge to first SPI communication**

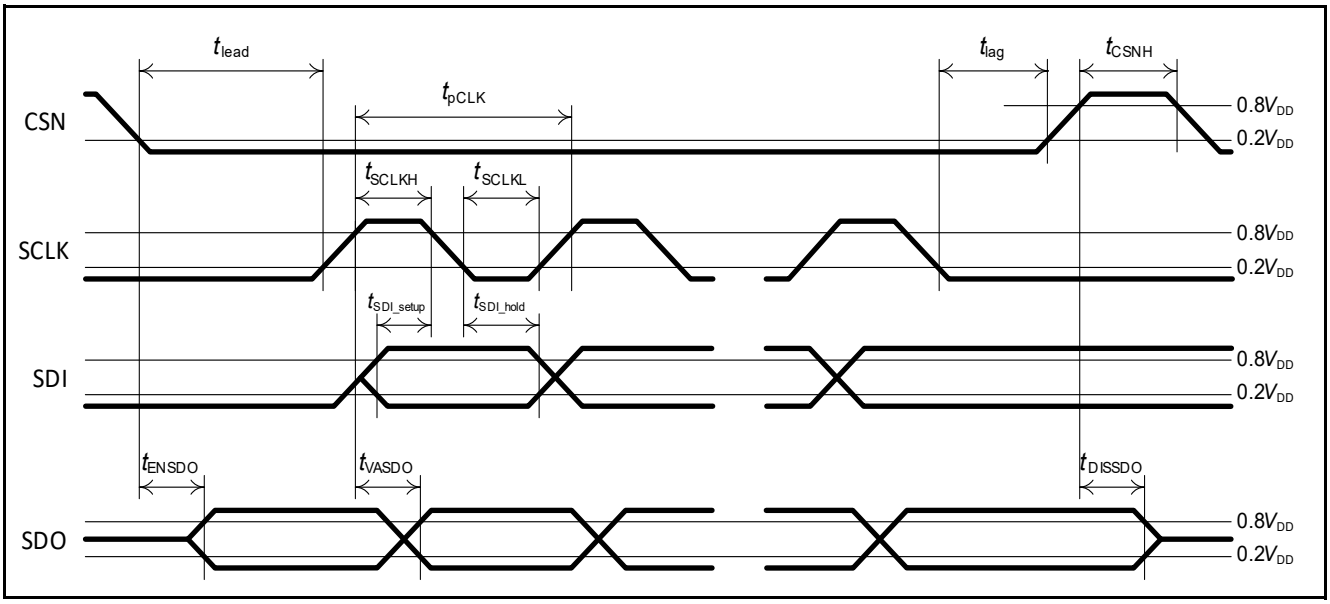



**Figure 15 SPI Data Timing**

### 7.1.1 Global Error Flag

A logic OR combination between Global Error Flag (GEF) and the signal present on SDI is reported on SDO between a CSN falling edge and the first SCLK rising edge (**Figure 13**). GEF is set if a fault condition is detected or if the device comes from a Power On Reset (POR).

*Note: The SDI pin of all devices in daisy chain or non daisy chain mode must be Low at the beginning of the SPI frame (between the CSN falling edge and the first SCLK rising edge).*

It is possible to check if the TLE94108ES has detected a fault by reading the GEF without SPI clock pulse (**Figure 16**).

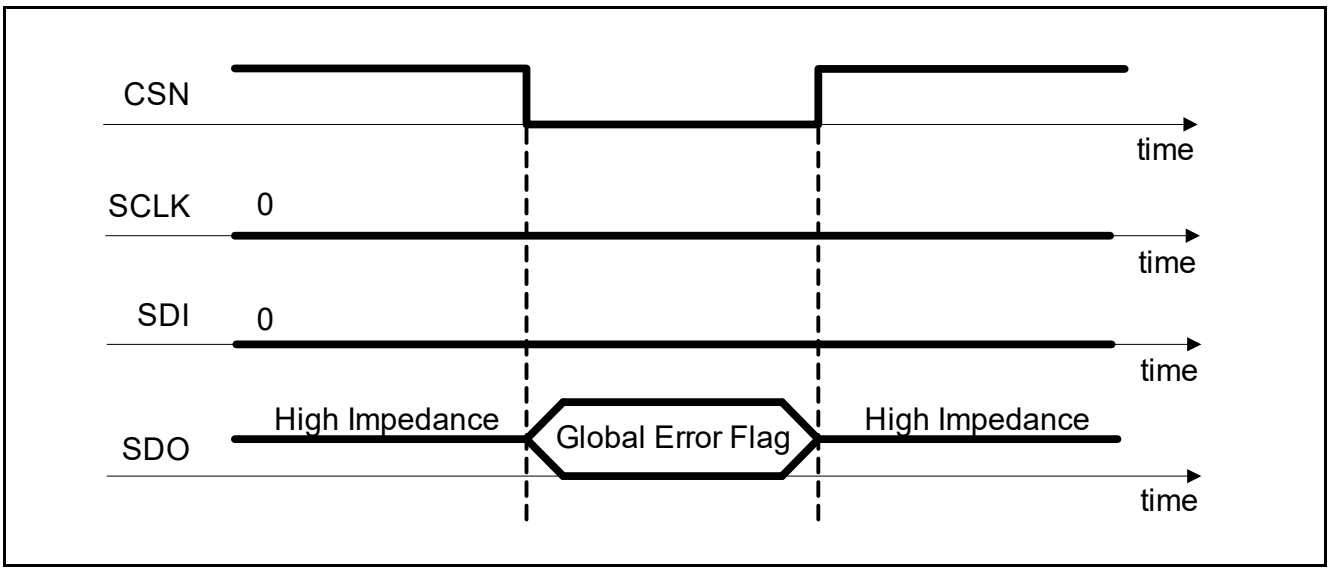



**Figure 16 SDO behaviour with 0-clock cycle**

### 7.1.2 Global Status Register

The SDO shifts out during the first eight SCLK cycles the Global Status Register. This register provides an overview of the device status. All failures conditions are reported in this byte:

- SPI protocol error (SPI_ERR)
- Load Error (LE bit): logical OR between Open Load (OL) and Overcurrent (OC) failures
- VS Undervoltage (VS_UV bit)
- VS Overvoltage (VS_OV bit)
- Negated Power ON Reset (NPOR bit)
- Temperature Shutdown (TSD bit)
- Temperature Pre-Warning (TPW bit)

See **Chapter 7.7.1** for details.

*Note: The Global Error Flag is a logic OR combination of every bit of the Global Status Register with the exception of NPOR: GEF = (SPI_ERR) OR (LE) OR (VS_UV) OR (VS_OV) OR (NOT(NPOR)) OR (TSD) OR (TPW).*

The following table shows how failures are reported in the Global Status Register and by the Global Error Flag.

**Table 10 Failure reported in the Global Status Register and Global Error Flag**

| Type of Error | Failure reported in the Global Status Register | Global Error Flag |
|---|---|---|
| SPI protocol error | SPI_ERR = 1 | 1 |
| Open load or Overcurrent | LE = 1 | 1 |
| VS Undervoltage | VS_UV = 1 | 1 |
| VS Overvoltage | VS_OV = 1 | 1 |
| Power ON Reset | **NPOR = 0** | 1 |
| Thermal Shutdown | TSD = 1 | 1 |

**Table 10 Failure reported in the Global Status Register and Global Error Flag**

| Type of Error | Failure reported in the Global Status Register | Global Error Flag |
|---|---|---|
| Thermal Warning | TPW = 1 | 1 |
| No Error and no Power ON Reset | SPI_ERR = 0<br>LE = 0<br>VS_UV = 0<br>VS_OV = 0<br>**NPOR = 1**<br>TSD = 0<br>TPW = 0 | 0 |

*Note: The default value (after Power ON Reset) of NPOR is 0, therefore the default value of GEF is 1.*

### 7.1.3 SPI protocol error detection

The SPI incorporates an error flag in the Global Status Register (SPI_ERR, Bit7) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPI_ERR bit is set in the next SPI communication.

The SPI_ERR bit is set in the following error conditions:

- the number of SCLK clock pulses received when CSN is Low is not 0, or is not a multiple of 8 and at least 16
- the microcontroller sends an SPI command to an unused address. In particular, SDI stuck to High is reported in the SPI_ERR bit
- the LSB of an address byte is not set to 1. In particular, SDI stuck to Low is reported in the SPI_ERR bit
- the Last Address Bit Token (LABT, bit 1 of the address byte, see **Chapter 7.2**) in independent slave configuration is not set to 1
- the LABT bit of the last address byte in daisy chain configuration is not set to 1 (see **Chapter 7.3**)
- a clock polarity error is detected (see **Figure 17** Case 2 and Case 3): the incoming clock signal was High during CSN rising or falling edges.

For a correct SPI communication:

- SCLK must be Low for a minimum $t_{BEF}$ before CSN falling edge and $t_{lead}$ after CSN falling edge
- SCLK must be Low for a minimum $t_{lag}$ before CSN rising edge and $t_{BEH}$ after CSN rising edge

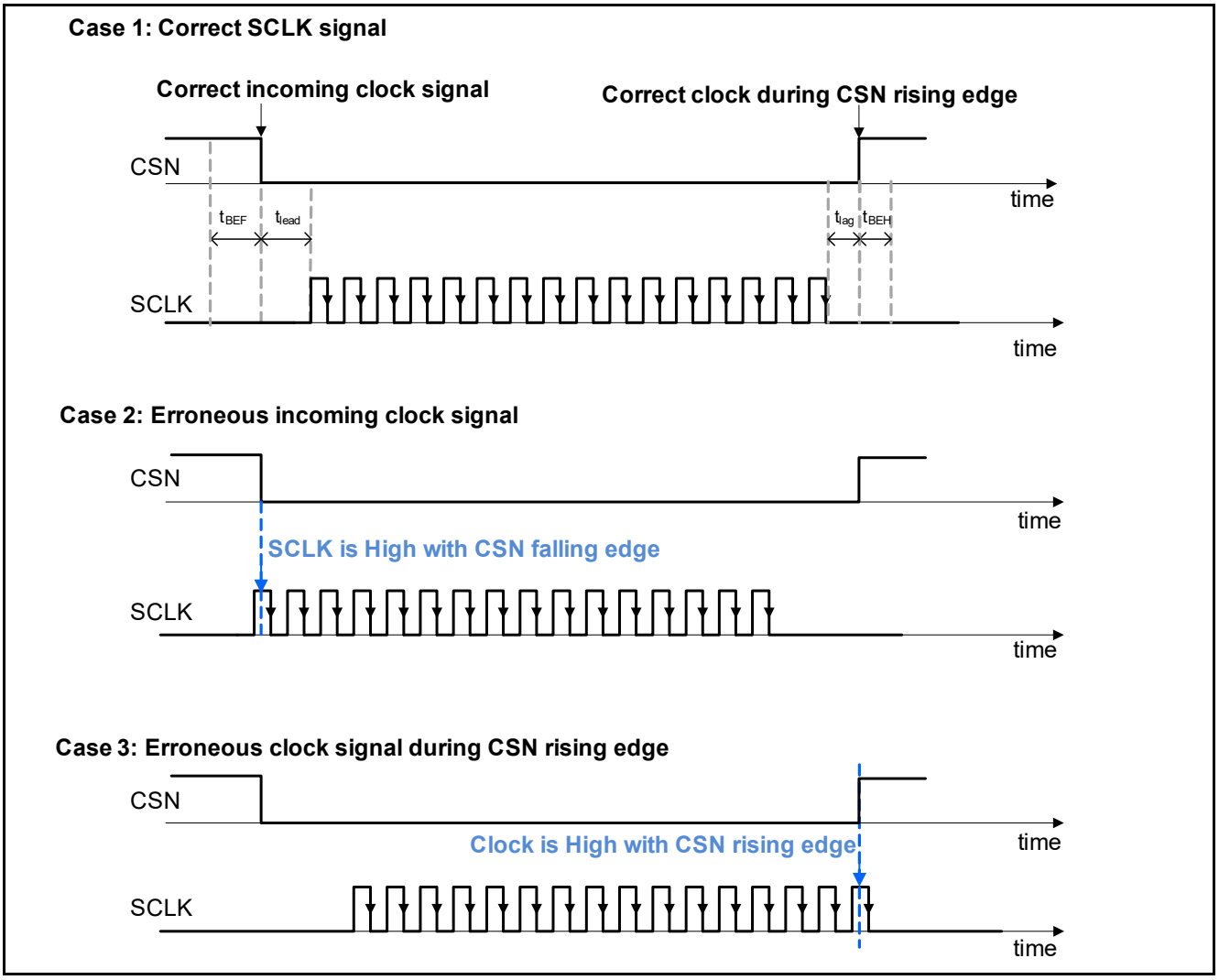



**Figure 17 Clock Polarity Error**

## 7.2 SPI with independent slave configuration

In an independent slave configuration, the microcontroller controls the CSN of each slave individually (**Figure 18**).

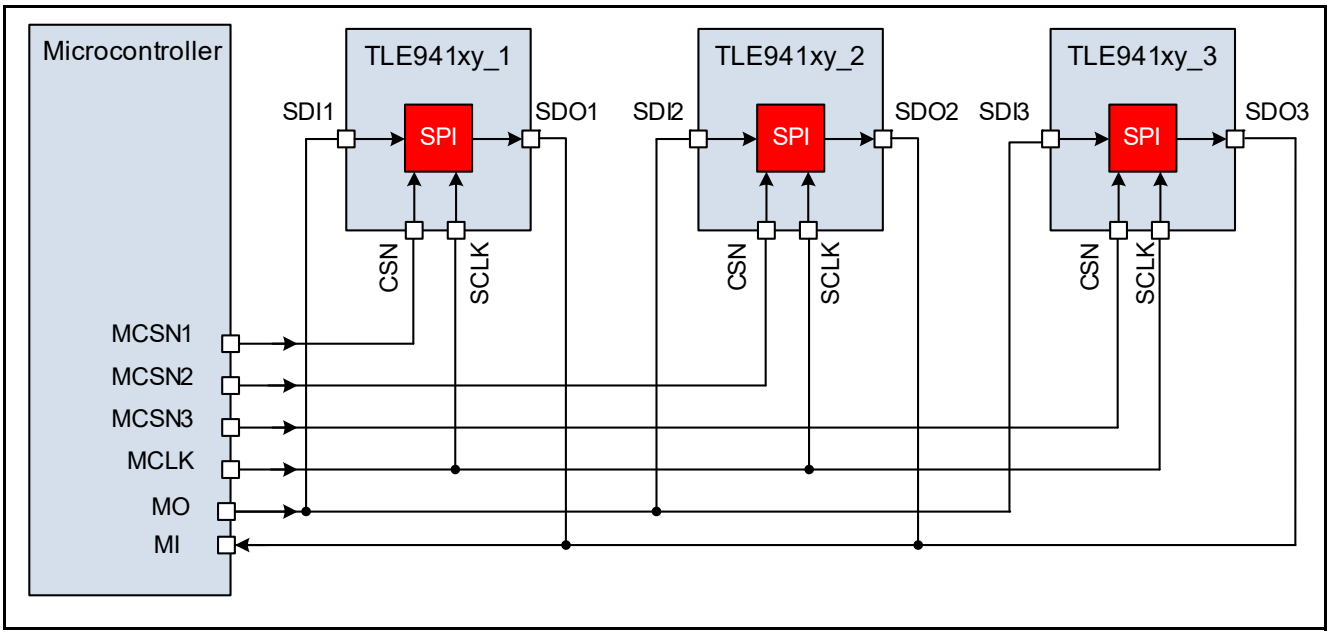



**Figure 18 SPI with independent slave configuration**

Each SPI communication starts with one address byte followed by one data byte (**Figure 19**).The LSB of the data byte must be set to '1'.The address bytes specifies:

- the type of operation: READ ONLY (OP bit =0) or READ/ WRITE (OP bit = 1) of the configuration bits, and READ ONLY (OP bit =0)or READ & CLEAR (OP bit = 1) of the status bits.
- The target register address (A[6:2])

The Last Address Byte Token bit (LABT, Bit1 of the address byte) must be set to 1, as no daisy chain configuration is used.

While the microcontroller sends the address byte on SDI, SDO shifts out GEF and the Global Status Register.

A further data byte (Bit15...8) is allocated to either configure the half-bridges or retrieve status information of the TLE94108ES.

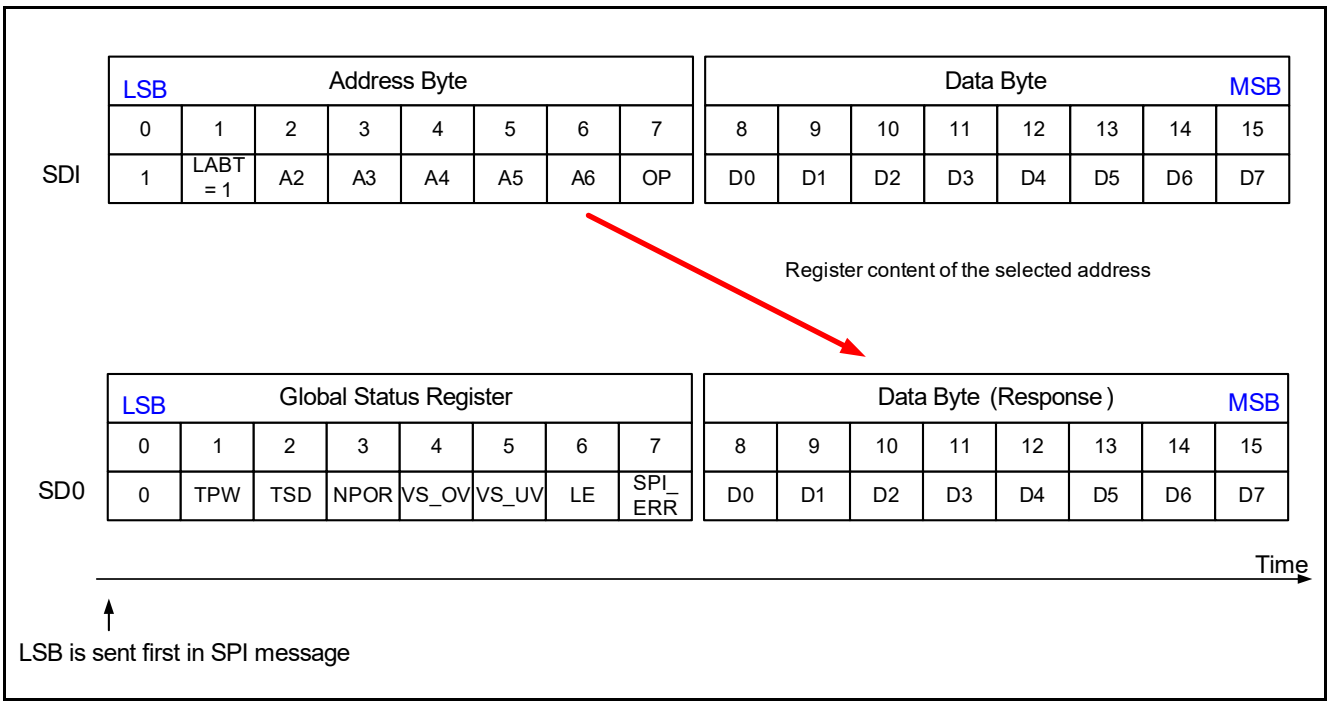



**Figure 19 SPI Operation Mode with independent slave configuration**

The in-frame response characteristic enables the microcontroller to read the contents of the addressed register within the SPI command. See **Figure 19**.

## 7.3 Daisy chain operation

The TLE94108ES supports daisy chain operation with devices with the same SPI protocol.This section describes the daisy chain hardware configuration with three devices from the TLE941xy family (See **Figure 20**).

The master output (noted MO) is connected to a slave SDI and the first slave SDO is connected to the next slave SDI to form a chain. The SDO of the final slave in the chain will be connected to the master input (MI) to close the loop of the SPI communication frame. In daisy chain configuration, a single chip select, CSN, and clock signal, SCLK, connected in parallel to each slave device, are used by the microcontroller to control or access the SPI devices.

In this configuration, the Master Output must send the address bytes and data bytes in the following order:

- All address bytes must be sent first:
  - Address Byte 1 (for TLE941xy_1) is sent first, followed by Address Byte 2 (for TLE941xy_2) etc,...
  - The LABT bit of the last address byte must be 1, while the LABT bit of all the other address bytes must be 0
- The data bytes are sent all together once all address bytes have been transmitted: Data Byte 1 (for TLE941xy_1) is sent first, followed by Data Byte 2 (for TLE941xy_2) etc,...

*Note: The signal on the SDI pin of the first IC in daisy chain (and in non-daisy chain mode), must be Low at the beginning of the SPI frame (between CSN falling edge and the first SCLK rising edge). This is because each Global Error Flag in daisy chain operation is implemented in OR logic.*

The Master Input (MI), which is connected to the SDO of the last device in the daisy chain receives:

- A logic OR combination of all Global Error Flags (GEF), at the beginning of the SPI frame, between CSN falling edge and the first SCLK rising edge
- The logic OR combination of the GEFs is followed by the Global Status Registers in reverse order. In other words MI receives first the Global Status Register of the last device of the daisy chain
- Once all Global Status Registers are received, MI receives the response bytes corresponding to the respective address and data bytes in reverse order. For example, if the daisy chain consists of three devices with SDO or TLE941xy_3 connected to MI, the master receives first the Response Byte 3 of TLE941xy_3 (corresponding to Address Byte 3 and Data Byte 3) followed by the Response Byte 2 of TLE941xy_2 and finally the Response Byte 1 of TLE941xy_1.

An example of an SPI frame with three devices from the TLE941xy family is shown in **Figure 21**.

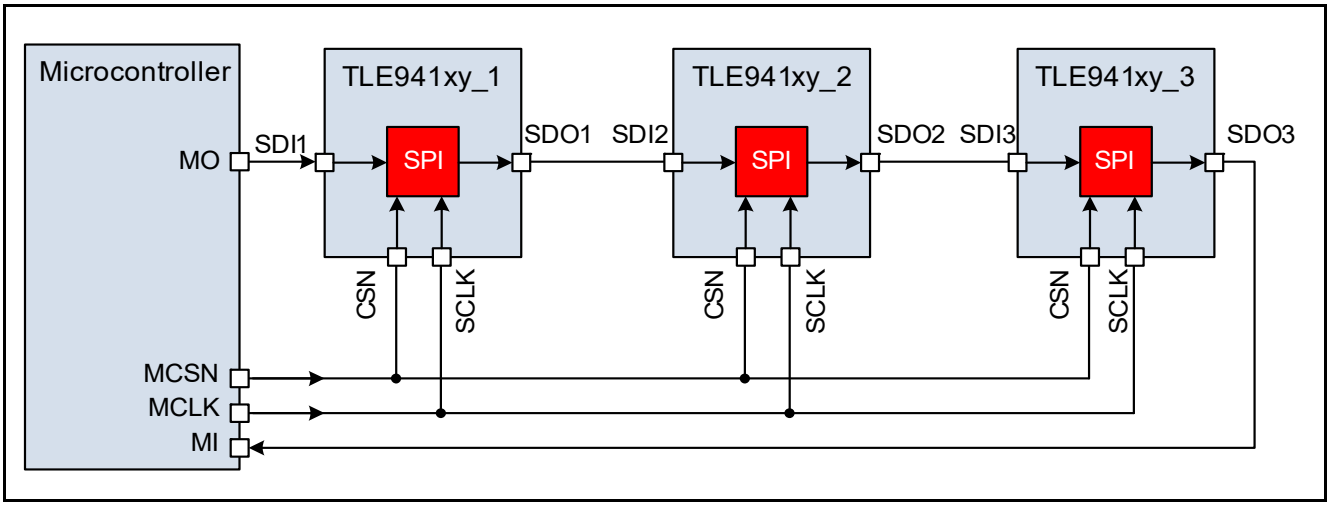



**Figure 20 Example of daisy chain hardware configuration with devices from the TLE941xy family**

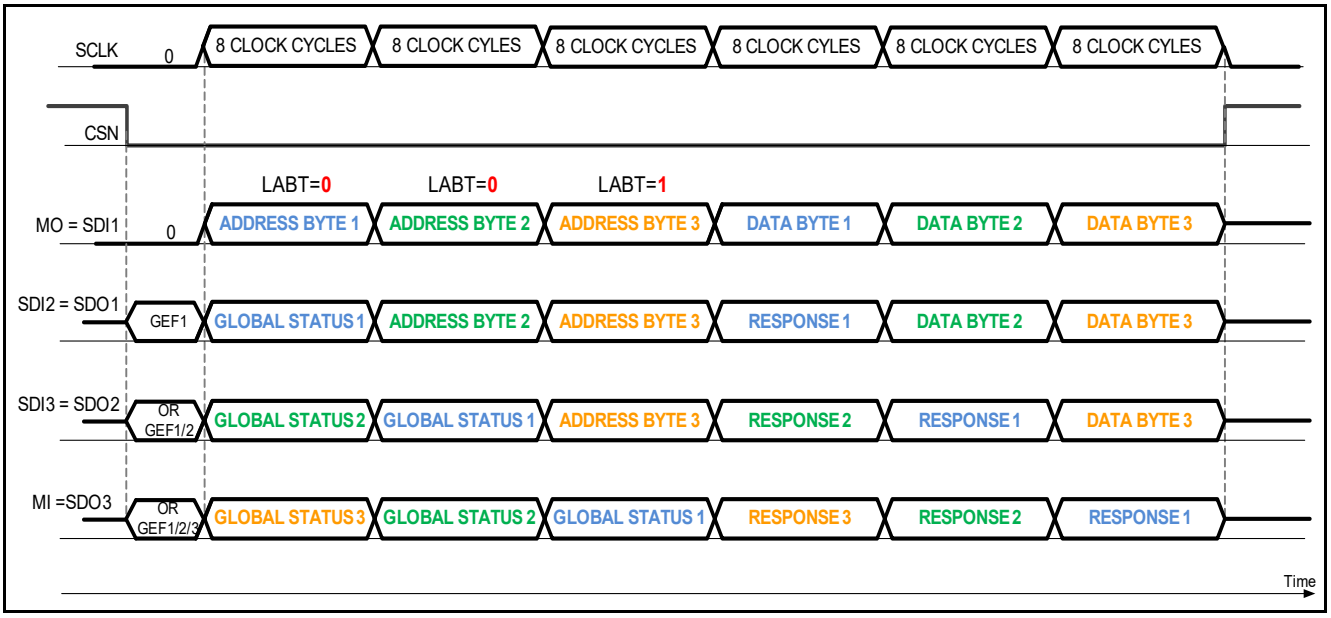



**Figure 21 SPI frame with three devices of the TLE941xy family**

Like in the individual slave configuration, it is possible to check if one or several TLE941xy have detected a fault condition by reading the logic OR combination of all the Global Error Flags when CSN goes Low without any clock cycle (**Figure 22**).

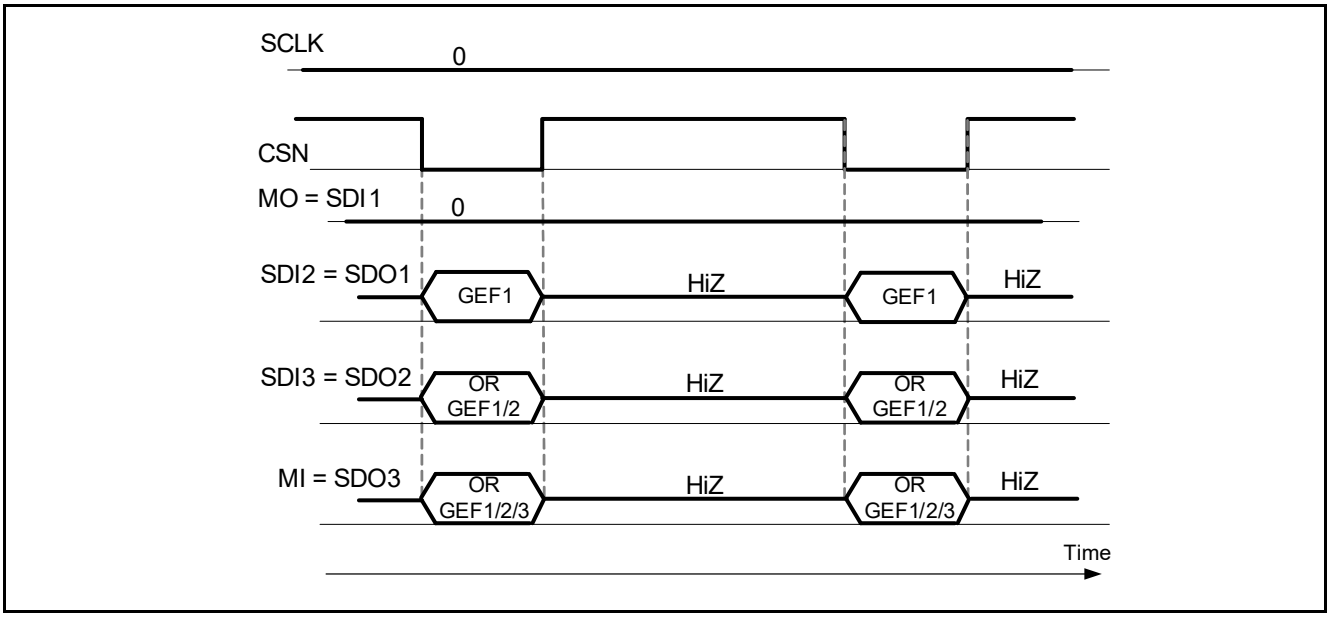



**Figure 22 Global Error Flag with zero SCLK clock cycle in daisy chain consisting only of TLE941xy devices**

*Note: Some SPI protocol errors such as the LSB of an address byte is wrongly equal to 0, may be reported in the SPI_ERR bit of another device in the daisy chain (refer to **Chapter 7.1.3** and **Chapter 7.7** for more details on SPI_ERR). In this case some devices might accept wrong data during the corrupted SPI frame. Therefore if one of the devices in the daisy chain reports an SPI error, it is recommended to verify the content of the registers of all devices.*

## 7.4 Status register change during SPI communication

If a new failure occurs after the transfer of the data byte(s), i.e. between the end of the last address byte and the CSN rising edge, this failure will be reported in the next SPI frame (see example in **Figure 23**).

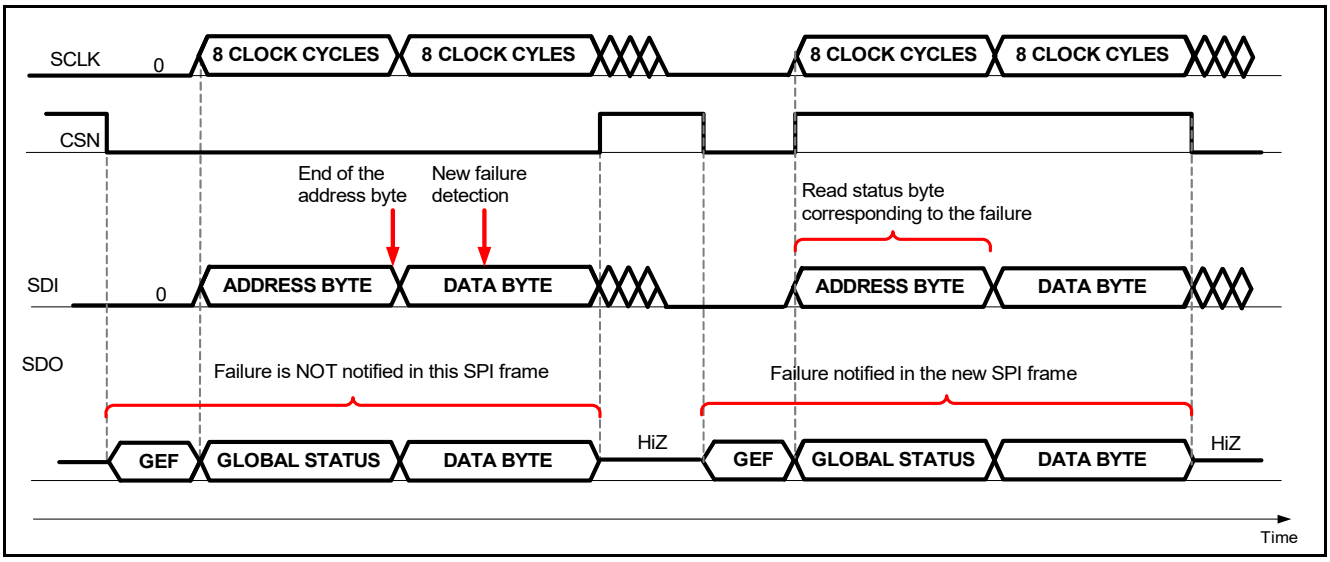



**Figure 23 Status register change during transfer of data byte - Example in independent slave configuration**

No information is lost, even if a status register is changed during a SPI frame, in particular during a Read and Clear command. For example:

- the microcontroller sends a Read and Clear command to a status register
- the TLE94108ES detects during the transfer the data byte(s) a new fault condition, which is normally reported in the target status register

The incoming Clear command will be ignored, so that the microcontroller can read the new failure in the subsequent SPI frames.

Data inconsistency between the Global Status Register (see **Chapter 7.7**) and the data byte (status register) within the same SPI frame is possible if:

- an open load or overcurrent error is detected during the transfer of the data byte
- the target status register corresponds to the new detected failure

In this case the new failure:

- is not reported in the Global Status Register of the current SPI frame but in the next one
- is reported in the data byte of the current SPI frame

Refer to **Figure 23**.

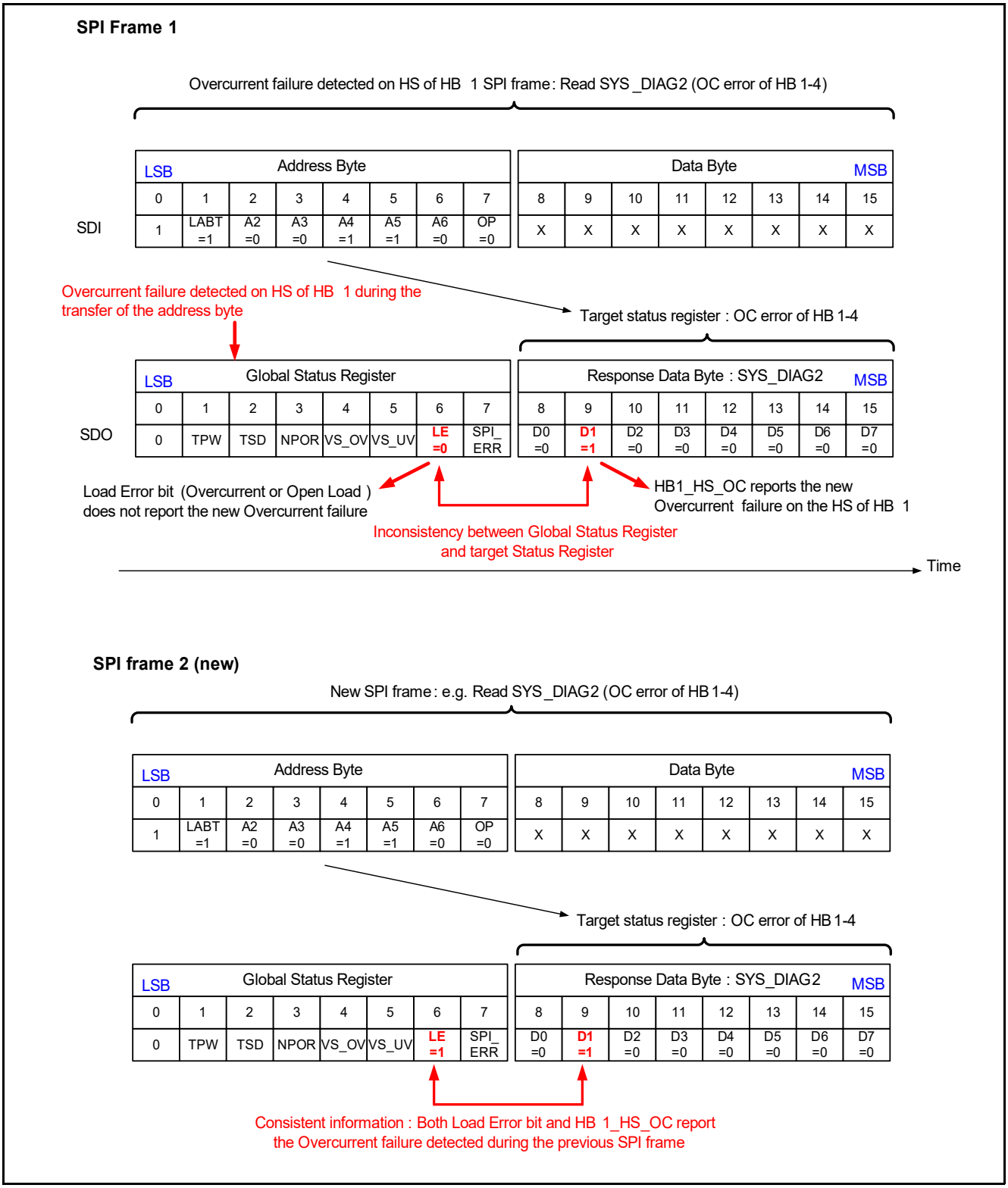



**Figure 24 Example of inconsistency between Global Error Flag and Status Register when a status bit is changed during the transfer of an address byte**

## 7.5 SPI Bit Mapping

The SPI Registers have been mapped as shown in **Figure 25** and **Figure 26** respectively.

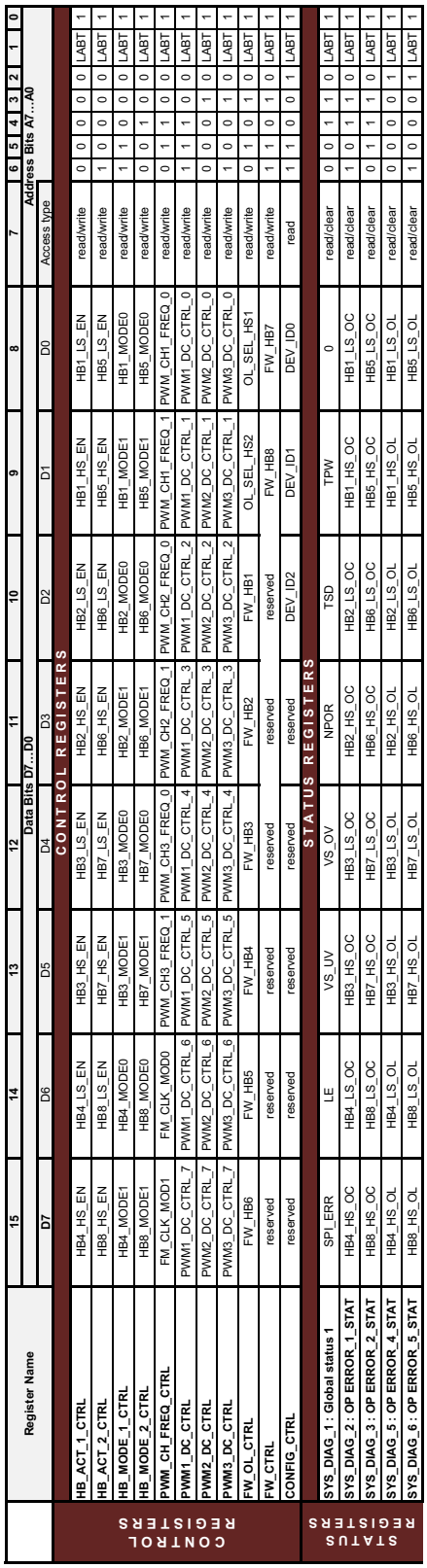
The control registers are READ/ WRITE registers. To set the control register to READ, bit 7 of the address byte (OP bit) must be programmed to ‘0’, otherwise ‘1’ for WRITE.

The status registers are READ/CLEAR registers. To CLEAR any Status Register, bit 7 of the address byte must be set to ‘1’, otherwise ‘0’ for READ.

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 8 Data Bits [D7…D0] for Configuration & Status Information | | | | | | | | Access type | 8 Address Bits [A7…0] | | | | | | |
| CONTROL REGISTERS | HB_ACT_1_CTRL | | | | | | | | read/write | 0 | 0 | 0 | 0 | 0 | LABT | 1 |
| | HB_ACT_2_CTRL | | | | | | | | read/write | 1 | 0 | 0 | 0 | 0 | LABT | 1 |
| | HB_MODE_1_CTRL | | | | | | | | read/write | 1 | 1 | 0 | 0 | 0 | LABT | 1 |
| | HB_MODE_2_CTRL | | | | | | | | read/write | 0 | 0 | 1 | 0 | 0 | LABT | 1 |
| | PWM_CH_FREQ_CTRL | | | | | | | | read/write | 0 | 1 | 1 | 0 | 0 | LABT | 1 |
| | PWM1_DC_CTRL | | | | | | | | read/write | 1 | 1 | 1 | 0 | 0 | LABT | 1 |
| | PWM2_DC_CTRL | | | | | | | | read/write | 0 | 0 | 0 | 1 | 0 | LABT | 1 |
| | PWM3_DC_CTRL | | | | | | | | read/write | 1 | 0 | 0 | 1 | 0 | LABT | 1 |
| | FW_OL_CTRL | | | | | | | | read/write | 0 | 1 | 0 | 1 | 0 | LABT | 1 |
| | FW_CTRL | | | | | | | | read/write | 1 | 1 | 0 | 1 | 0 | LABT | 1 |
| | CONFIG_CTRL | | | | | | | | read | 1 | 1 | 0 | 0 | 1 | LABT | 1 |
| STATUS REGISTERS | SYS_DIAG_1 : Global status 1 | | | | | | | | read/clear | 0 | 0 | 1 | 1 | 0 | LABT | 1 |
| | SYS_DIAG_2 : OP ERROR_1_STAT | | | | | | | | read/clear | 1 | 0 | 1 | 1 | 0 | LABT | 1 |
| | SYS_DIAG_3 : OP ERROR_2_STAT | | | | | | | | read/clear | 0 | 1 | 1 | 1 | 0 | LABT | 1 |
| | SYS_DIAG_5 : OP ERROR_4_STAT | | | | | | | | read/clear | 0 | 0 | 0 | 0 | 1 | LABT | 1 |
| | SYS_DIAG_6 : OP ERROR_5_STAT | | | | | | | | read/clear | 1 | 0 | 0 | 0 | 1 | LABT | 1 |

**Figure 25 TLE94108ES SPI Register mapping**

*Note: LABT: Last Address Bit Token, refer to **Chapter 7.2** and **Chapter 7.3**.*



| | Register Name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Access type | Address Bits A7...A0 | | | | | | |
| CONTROL REGISTERS | HB_ACT_1_CTRL | HB4_HS_EN | HB4_LS_EN | HB3_HS_EN | HB3_LS_EN | HB2_HS_EN | HB2_LS_EN | HB1_HS_EN | HB1_LS_EN | read/write | 0 | 0 | 0 | 0 | 0 | LABT | 1 |
| | HB_ACT_2_CTRL | HB8_HS_EN | HB8_LS_EN | HB7_HS_EN | HB7_LS_EN | HB6_HS_EN | HB6_LS_EN | HB5_HS_EN | HB5_LS_EN | read/write | 1 | 0 | 0 | 0 | 0 | LABT | 1 |
| | HB_MODE_1_CTRL | HB4_MODE1 | HB4_MODE0 | HB3_MODE1 | HB3_MODE0 | HB2_MODE1 | HB2_MODE0 | HB1_MODE1 | HB1_MODE0 | read/write | 1 | 1 | 0 | 0 | 0 | LABT | 1 |
| | HB_MODE_2_CTRL | HB8_MODE1 | HB8_MODE0 | HB7_MODE1 | HB7_MODE0 | HB6_MODE1 | HB6_MODE0 | HB5_MODE1 | HB5_MODE0 | read/write | 0 | 0 | 1 | 0 | 0 | LABT | 1 |
| | PWM_CH_FREQ_CTRL | FM_CLK_MOD1 | FM_CLK_MOD0 | PWM_CH3_FREQ_1 | PWM_CH3_FREQ_0 | PWM_CH2_FREQ_1 | PWM_CH2_FREQ_0 | PWM_CH1_FREQ_1 | PWM_CH1_FREQ_0 | read/write | 0 | 1 | 1 | 0 | 0 | LABT | 1 |
| | PWM1_DC_CTRL | PWM1_DC_CTRL_7 | PWM1_DC_CTRL_6 | PWM1_DC_CTRL_5 | PWM1_DC_CTRL_4 | PWM1_DC_CTRL_3 | PWM1_DC_CTRL_2 | PWM1_DC_CTRL_1 | PWM1_DC_CTRL_0 | read/write | 1 | 1 | 1 | 0 | 0 | LABT | 1 |
| | PWM2_DC_CTRL | PWM2_DC_CTRL_7 | PWM2_DC_CTRL_6 | PWM2_DC_CTRL_5 | PWM2_DC_CTRL_4 | PWM2_DC_CTRL_3 | PWM2_DC_CTRL_2 | PWM2_DC_CTRL_1 | PWM2_DC_CTRL_0 | read/write | 0 | 0 | 0 | 1 | 0 | LABT | 1 |
| | PWM3_DC_CTRL | PWM3_DC_CTRL_7 | PWM3_DC_CTRL_6 | PWM3_DC_CTRL_5 | PWM3_DC_CTRL_4 | PWM3_DC_CTRL_3 | PWM3_DC_CTRL_2 | PWM3_DC_CTRL_1 | PWM3_DC_CTRL_0 | read/write | 1 | 0 | 0 | 1 | 0 | LABT | 1 |
| | FW_OL_CTRL | FW_HB6 | FW_HB5 | FW_HB4 | FW_HB3 | FW_HB2 | FW_HB1 | OL_SEL_HS2 | OL_SEL_HS1 | read/write | 0 | 1 | 0 | 1 | 0 | LABT | 1 |
| | FW_CTRL | reserved | reserved | reserved | reserved | reserved | reserved | FW_HB8 | FW_HB7 | read/write | 1 | 1 | 0 | 1 | 0 | LABT | 1 |
| | CONFIG_CTRL | reserved | reserved | reserved | reserved | reserved | DEV_ID2 | DEV_ID1 | DEV_ID0 | read | 1 | 1 | 0 | 0 | 1 | LABT | 1 |
| STATUS REGISTERS | SYS_DIAG_1 : Global status 1 | SPI_ERR | LE | VS_UV | VS_OV | NPOR | TSD | TPW | 0 | read/clear | 0 | 0 | 1 | 1 | 0 | LABT | 1 |
| | SYS_DIAG_2 : OP ERROR_1_STAT | HB4_HS_OC | HB4_LS_OC | HB3_HS_OC | HB3_LS_OC | HB2_HS_OC | HB2_LS_OC | HB1_HS_OC | HB1_LS_OC | read/clear | 1 | 0 | 1 | 1 | 0 | LABT | 1 |
| | SYS_DIAG_3 : OP ERROR_2_STAT | HB8_HS_OC | HB8_LS_OC | HB7_HS_OC | HB7_LS_OC | HB6_HS_OC | HB6_LS_OC | HB5_HS_OC | HB5_LS_OC | read/clear | 0 | 1 | 1 | 1 | 0 | LABT | 1 |
| | SYS_DIAG_5 : OP ERROR_4_STAT | HB4_HS_OL | HB4_LS_OL | HB3_HS_OL | HB3_LS_OL | HB2_HS_OL | HB2_LS_OL | HB1_HS_OL | HB1_LS_OL | read/clear | 0 | 0 | 0 | 0 | 1 | LABT | 1 |
| | SYS_DIAG_6 : OP ERROR_5_STAT | HB8_HS_OL | HB8_LS_OL | HB7_HS_OL | HB7_LS_OL | HB6_HS_OL | HB6_LS_OL | HB5_HS_OL | HB5_LS_OL | read/clear | 1 | 0 | 0 | 0 | 1 | LABT | 1 |

**Figure 26 TLE94108ES Bit Mapping**

*Note: LABT: Last Address Bit Token, refer to **Chapter 7.2** and **Chapter 7.3**.*

## 7.6 SPI Control Registers

The Control Registers have a READ/WRITE access (see **Chapter 7.5**):

- The ‘POR’ value is defined by the register content after a POR or device Reset
  - The default value of all control registers is 0000 $0000_B$ with the exception of CONFIG_CTRL
  - The default value of the CONFIG_CTRL register is 0000 $0010_B$
- One 16-bit SPI command consists of two bytes (see **Figure 25** and **Figure 26**), i.e.
  - an address byte
  - followed by a data byte
- The control bits are not cleared or changed automatically by the device. This must be done by the microcontroller via SPI programming.
- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= READ ONLY).
- Writing to a register is done byte wise by setting the SPI bit 7 to “1”.

### 7.6.1 Control register definition

**HB_ACT_1_CTRL**
**Half-bridge output control 1 (Address Byte [OP] 000 00[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB4_HS_EN** | **HB4_LS_EN** | **HB3_HS_EN** | **HB3_LS_EN** | **HB2_HS_EN** | **HB2_LS_EN** | **HB1_HS_EN** | **HB1_LS_EN** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB4_HS_EN** | D7 | rw | **Half-bridge output 4 high side switch enable**<br>$0_B$ HS4 OFF/ High-Z (default value)<br>$1_B$ HS4 ON |
| **HB4_LS_EN** | D6 | rw | **Half-bridge output 4 low side switch enable**<br>$0_B$ LS4 OFF/ High-Z (default value)<br>$1_B$ LS4 ON |
| **HB3_HS_EN** | D5 | rw | **Half-bridge output 3 high side switch enable**<br>$0_B$ HS3 OFF/ High-Z (default value)<br>$1_B$ HS3 ON |
| **HB3_LS_EN** | D4 | rw | **Half-bridge output 3 low side switch enable**<br>$0_B$ LS3 OFF/ High-Z (default value)<br>$1_B$ LS3 ON |
| **HB2_HS_EN** | D3 | rw | **Half-bridge output 2 high side switch enable**<br>$0_B$ HS2 OFF/ High-Z (default value)<br>$1_B$ HS2 ON |
| **HB2_LS_EN** | D2 | rw | **Half-bridge output 2 low side switch enable**<br>$0_B$ LS2 OFF/ High-Z (default value)<br>$1_B$ LS2 ON |
| **HB1_HS_EN** | D1 | rw | **Half-bridge output 1 high side switch enable**<br>$0_B$ HS1 OFF/ High-Z (default value)<br>$1_B$ HS1 ON |
| **HB1_LS_EN** | D0 | rw | **Half-bridge output 1 low side switch enable**<br>$0_B$ LS1 OFF/ High-Z (default value)<br>$1_B$ LS1 ON |

*Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.*

### HB_ACT_2_CTRL
### Half-bridge output control 2 (Address Byte [OP]100 00[LABT]$1_B$)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB8_HS_EN** | **HB8_LS_EN** | **HB7_HS_EN** | **HB7_LS_EN** | **HB6_HS_EN** | **HB6_LS_EN** | **HB5_HS_EN** | **HB5_LS_EN** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB8_HS_EN** | D7 | rw | **Half-bridge output 8 high side switch enable**<br>$0_B$ HS8 OFF/ High-Z (default value)<br>$1_B$ HS8 ON |
| **HB8_LS_EN** | D6 | rw | **Half-bridge output 8 low side switch enable**<br>$0_B$ LS8 OFF/ High-Z (default value)<br>$1_B$ LS8 ON |
| **HB7_HS_EN** | D5 | rw | **Half-bridge output 7 high side switch enable**<br>$0_B$ HS7 OFF/ High-Z (default value)<br>$1_B$ HS7 ON |
| **HB7_LS_EN** | D4 | rw | **Half-bridge output 7 low side switch enable**<br>$0_B$ LS7 OFF/ High-Z (default value)<br>$1_B$ LS7 ON |
| **HB6_HS_EN** | D3 | rw | **Half-bridge output 6 high side switch enable**<br>$0_B$ HS6 OFF/ High-Z (default value)<br>$1_B$ HS6 ON |
| **HB6_LS_EN** | D2 | rw | **Half-bridge output 6 low side switch enable**<br>$0_B$ LS6 OFF/ High-Z (default value)<br>$1_B$ LS6 ON |
| **HB5_HS_EN** | D1 | rw | **Half-bridge output 5 high side switch enable**<br>$0_B$ HS5 OFF/ High-Z (default value)<br>$1_B$ HS5 ON |
| **HB5_LS_EN** | D0 | rw | **Half-bridge output 5 low side switch enable**<br>$0_B$ LS5 OFF/ High-Z (default value)<br>$1_B$ LS5 ON |

*Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.*

### HB_MODE_1_CTRL
### Half-bridge output mode control 1 (Address Byte [OP]110 00[LABT]$1_B$)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB4_MODE1** | **HB4_MODE0** | **HB3_MODE1** | **HB3_MODE0** | **HB2_MODE1** | **HB2_MODE0** | **HB1_MODE1** | **HB1_MODE0** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB4_MODEn (n = 0,1)** | D7:D6 | rw | **Half-bridge output 4 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |
| **HB3_MODEn (n = 0,1)** | D5:D4 | rw | **Half-bridge output 3 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |
| **HB2_MODEn (n = 0,1)** | D3:D2 | rw | **Half-bridge output 2 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |
| **HB1_MODEn (n = 0,1)** | D1:D0 | rw | **Half-bridge output 1 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

### HB_MODE_2_CTRL
### Half-bridge output mode control 2 (Address Byte [OP]001 00[LABT]$1_B$)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB8_MODE1** | **HB8_MODE0** | **HB7_MODE1** | **HB7_MODE0** | **HB6_MODE1** | **HB6_MODE0** | **HB5_MODE1** | **HB5_MODE0** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB8_MODEn (n = 0,1)** | D7:D6 | rw | **Half-bridge output 8 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |
| **HB7_MODEn (n = 0,1)** | D5:D4 | rw | **Half-bridge output 7 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |
| **HB6_MODEn (n = 0,1)** | D3:D2 | rw | **Half-bridge output 6 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |
| **HB5_MODEn (n = 0,1)** | D1:D0 | rw | **Half-bridge output 5 mode select**<br>$00_B$ No PWM (default value)<br>$01_B$ PWM control with PWM Channel 1<br>$10_B$ PWM control with PWM Channel 2<br>$11_B$ PWM control with PWM Channel 3 |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

### PWM_CH_FREQ_CTRL
### PWM channel frequency select (Address Byte [OP]011 00[LABT]$1_B$)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **FM_CLK_MOD1** | **FM_CLK_MOD0** | **PWM_CH3_FREQ_1** | **PWM_CH3_FREQ_0** | **PWM_CH2_FREQ_1** | **PWM_CH2_FREQ_0** | **PWM_CH1_FREQ_1** | **PWM_CH1_FREQ_0** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **FM_MOD_EN** | D7:D6 | rw | **FM Modulation Enable**[1)]<br>$00_B$ No modulation (default)<br>$01_B$ Modulation frequency 15.625kHz<br>$10_B$ Modulation frequency 31.25kHz<br>$11_B$ Modulation frequency 62.5kHz |
| **PWM_CH3_FREQ_n (n=0,1)** | D5:D4 | rw | **PWM Channel 3 frequency select**<br>$00_B$ PWM is stopped and off (default value)<br>$01_B$ PWM frequency 1 : 80Hz<br>$10_B$ PWM frequency 2 : 100Hz<br>$11_B$ PWM frequency 3 : 200Hz |
| **PWM_CH2_FREQ_n (n=0,1)** | D3:D2 | rw | **PWM Channel 2 frequency select**<br>$00_B$ PWM is stopped and off (default value)<br>$01_B$ PWM frequency 1 : 80Hz<br>$10_B$ PWM frequency 2 : 100Hz<br>$11_B$ PWM frequency 3 : 200Hz |
| **PWM_CH1_FREQ_n (n=0,1)** | D1:D0 | rw | **PWM Channel 1 frequency select**<br>$00_B$ PWM is stopped and off (default value)<br>$01_B$ PWM frequency 1 : 80Hz<br>$10_B$ PWM frequency 2 : 100Hz<br>$11_B$ PWM frequency 3 : 200Hz |

1) Not subject to production test, guaranteed by design. Frequency may deviate by ±10%

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

**PWM1_DC_CTRL**
**PWM channel 1 duty cycle configuration (Address Byte [OP]111 00[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **PWM1_DC_CTRL_7** | **PWM1_DC_CTRL_6** | **PWM1_DC_CTRL_5** | **PWM1_DC_CTRL_4** | **PWM1_DC_CTRL_3** | **PWM1_DC_CTRL_2** | **PWM1_DC_CTRL_1** | **PWM1_DC_CTRL_0** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **PWM1_DC_CTRLn** | D7:D0 | rw | **PWM Channel 1 Duty Cycle configuration (bit7=MSB; bit0)**<br>0000 $0000_B$ 100% OFF (default value)<br>xxxx $xxxx_B$ parts of 255 ON<br>1111 $1111_B$ 100% ON |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

**PWM2_DC_CTRL**
**PWM channel 2 duty cycle configuration (Address [OP]000 10[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **PWM2_DC_CTRL_7** | **PWM2_DC_CTRL_6** | **PWM2_DC_CTRL_5** | **PWM2_DC_CTRL_4** | **PWM2_DC_CTRL_3** | **PWM2_DC_CTRL_2** | **PWM2_DC_CTRL_1** | **PWM2_DC_CTRL_0** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **PWM2_DC_CTRLn** | D7:D0 | rw | **PWM Channel 2 Duty Cycle configuration (bit7=MSB; bit0)**<br>0000 $0000_B$ 100% OFF (default value)<br>xxxx $xxxx_B$ parts of 255 ON<br>1111 $1111_B$ 100% ON |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

### PWM3_DC_CTRL

**PWM channel 3 duty cycle configuration (Address Byte [OP]100 10[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **PWM3_DC_CTRL_7** | **PWM3_DC_CTRL_6** | **PWM3_DC_CTRL_5** | **PWM3_DC_CTRL_4** | **PWM3_DC_CTRL_3** | **PWM3_DC_CTRL_2** | **PWM3_DC_CTRL_1** | **PWM3_DC_CTRL_0** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **PWM3_DC_CTRLn** | D7:D0 | rw | **PWM Channel 3 Duty Cycle configuration (bit7=MSB; bit0)**<br>0000 $0000_B$ 100% OFF (default value)<br>xxxx $xxxx_B$ parts of 255 ON<br>1111 $1111_B$ 100% ON |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

### FW_OL_CTRL

**Free-wheeling configuration and Open load detection setting of HS1 and HS2 (Address Byte [OP]010 10[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **FW_HB6** | **FW_HB5** | **FW_HB4** | **FW_HB3** | **FW_HB2** | **FW_HB1** | **OL_SEL_HS2** | **OL_SEL_HS1** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **FW_HB6** | D7 | rw | **HB6 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **FW_HB5** | D6 | rw | **HB5 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **FW_HB4** | D5 | rw | **HB4 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **FW_HB3** | D4 | rw | **HB3 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **FW_HB2** | D3 | rw | **HB2 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **FW_HB1** | D2 | rw | **HB1 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **OL_SEL_HS2** | D1 | rw | **HS2 open load detection current and filter time select**<br>$0_B$ High-current mode (default value)<br>$1_B$ LED Mode (Low current mode) |
| **OL_SEL_HS1** | D0 | rw | **HS1 open load detection current and filter time select**<br>$0_B$ High current mode (default value)<br>$1_B$ LED Mode (Low current mode) |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

**FW_CTRL**
**Free-wheeling configuration (Address Byte [OP]110 10[LABT]1)$_B$**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **reserved** | **reserved** | **reserved** | **reserved** | **reserved** | **reserved** | **FW_HB8** | **FW_HB7** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **reserved** | D7:D6 | rw | **To be programmed as ‘0’.** |
| **reserved** | D5 | rw | **Reserved. Always reads as ‘0’.** |
| **reserved** | D4 | rw | **Reserved. Always reads as ‘0’.** |
| **reserved** | D3 | rw | **Reserved. Always reads as ‘0’.** |
| **reserved** | D2 | rw | **Reserved. Always reads as ‘0’.** |
| **FW_HB8** | D1 | rw | **HB8 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |
| **FW_HB7** | D0 | rw | **HB7 free-wheeling configuration**<br>$0_B$ Passive free-wheeling (default value)<br>$1_B$ Active free-wheeling |

*Note: Refer to **Chapter 6.1.1** for more information on PWM operation*

### CONFIG_CTRL
### Device Configuration control (Address Byte [OP]110 01[LABT]$1_B$)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **reserved** | **reserved** | **reserved** | **reserved** | **reserved** | **DEV_ID2** | **DEV_ID1** | **DEV_ID0** |
| r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| **reserved** | D7:D3 | r | **Always reads as '0'** |
| **DEV_IDn** | D2:D0 | r | **Device/ derivative identifier**<br><br>*Note: These bits can be used to verify the silicon content of the device*<br><br>$000_B$ TLE94112EL/ES chip<br>$001_B$ TLE94110EL/ES chip<br>$010_B$ TLE94108EL/ES chip<br>$011_B$ TLE94106EL/ES chip<br>$100_B$ TLE94104EP chip<br>$101_B$ TLE94103EP chip<br>$110_B$ reserved<br>$111_B$ reserved |

## 7.7 SPI Status Registers

The Control Registers have a READ/CLEAR access (see also **Chapter 7.5**):

- The 'POR Value' of the Status registers (content after a POR or device Reset) and is $0000\ 0000_B$.
- One 16-bit SPI command consists of two bytes (see **Figure 25** and **Figure 26**), i.e.
  - an address byte
  - followed by a data byte
- Reading a register is done byte wise by setting the SPI bit 7 of the address byte to "0" (= Read Only).
- Clearing a register is done byte wise by setting the SPI bit 7 of the address byte to "1".
- SPI status registers are not cleared automatically by the device. This must be done by the microcontroller via SPI command.

### 7.7.1 Status register definition

**SYS_DIAG1**
**Global status 1 (Address Byte [OP]001 10[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **SPI_ERR** | **LE** | **VS_UV** | **VS_OV** | **NPOR** | **TSD** | **TPW** | **reserved** |
| rc | r | rc | rc | rc | rc | rc | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| **SPI_ERR** | D7 | rc | **SPI error detection**<br>$0_B$ No SPI protocol error is detected (default value).<br>$1_B$ An SPI protocol error is detected. |
| **LE** | D6 | r | **Load error detection (logic OR combination of Open Load and Overcurrent)**<br>$0_B$ No Open Load and no Overcurrent detected (default value)<br>$1_B$ Open Load or Overcurrent detected in at least one of the power outputs. Error latched. Faulty output is latched off in case of Overcurrent |
| **VS_UV** | D5 | rc | **VS Undervoltage error detection**<br>$0_B$ No undervoltage on $V_S$ detected (default value)<br>$1_B$ Undervoltage on $V_S$ detected. Error latched and all outputs disabled. |
| **VS_OV** | D4 | rc | **VS Overvoltage error detection**<br>$0_B$ No overvoltage on $V_S$ detected (default value)<br>$1_B$ Overvoltage on $V_S$ detected. Error latched and all outputs disabled. |
| **NPOR** | D3 | rc | **Not Power On Reset (NPOR) detection**<br>$0_B$ POR on EN or VDD supply rail (default value)<br>$1_B$ No POR |
| **TSD** | D2 | rc | **Temperature shutdown error detection**<br>$0_B$ Junction temperature below temperature shutdown threshold (default value)<br>$1_B$ Junction temperature has reached temperature shutdown threshold. Error latched and all outputs disabled. |
| **TPW** | D1 | rc | **Temperature pre-warning error detection**<br>$0_B$ Junction temperature below temperature pre-warning threshold (default value)<br>$1_B$ Junction temperature has reached temperature pre-warning threshold. |
| **reserved** | D0 | r | **Bit reserved. Always reads ‘0’.** |

*Note: The LE bit in the Global Status register is read only. It reflects an OR combination of the respective open load and overcurrent errors of the half-bridge channels. If all OC/ OL bits of the respective high-side and low-side channels are cleared to ‘0’, the LE bit will be automatically updated to ‘0’.*

### SYS_DIAG_2 : OP_ERROR_1_STAT

**Overcurrent error status of half-bridge outputs 1 - 4 (Address Byte [OP]101 10[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB4_HS_OC** | **HB4_LS_OC** | **HB3_HS_OC** | **HB3_LS_OC** | **HB2_HS_OC** | **HB2_LS_OC** | **HB1_HS_OC** | **HB1_LS_OC** |
| rc | rc | rc | rc | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB4_HS_OC** | D7 | rc | **High-side (HS) switch of half-bridge 4 overcurrent detection**<br>$0_B$ No error on HS4 switch (default value)<br>$1_B$ Overcurrent detected on HS4 switch. Error latched and HS4 disabled. |
| **HB4_LS_OC** | D6 | rc | **Low-side (LS) switch of half-bridge 4 overcurrent detection**<br>$0_B$ No error on LS4 switch (default value)<br>$1_B$ Overcurrent detected on LS4 switch. Error latched and LS4 disabled. |
| **HB3_HS_OC** | D5 | rc | **High-side (HS) switch of half-bridge 3 overcurrent detection**<br>$0_B$ No error on HS3 switch (default value)<br>$1_B$ Overcurrent detected on HS3 switch. Error latched and HS3 disabled. |
| **HB3_LS_OC** | D4 | rc | **Low-side (LS) switch of half-bridge 3 overcurrent detection**<br>$0_B$ No error on LS3 switch (default value)<br>$1_B$ Overcurrent detected on LS3 switch. Error latched and LS3 disabled. |
| **HB2_HS_OC** | D3 | rc | **High-side (HS) switch of half-bridge 2 overcurrent detection**<br>$0_B$ No error on HS2 switch (default value)<br>$1_B$ Overcurrent detected on HS2 switch. Error latched and HS2 disabled. |
| **HB2_LS_OC** | D2 | rc | **Low-side (LS) switch of half-bridge 2 overcurrent detection**<br>$0_B$ No error on LS2 switch (default value)<br>$1_B$ Overcurrent detected on LS2 switch. Error latched and LS2 disabled. |
| **HB1_HS_OC** | D1 | rc | **High-side (HS) switch of half-bridge 1 overcurrent detection**<br>$0_B$ No error on HS1 switch (default value)<br>$1_B$ Overcurrent detected on HS1 switch. Error latched and HS1 disabled. |
| **HB1_LS_OC** | D0 | rc | **Low-side (LS) switch of half-bridge 1 overcurrent detection**<br>$0_B$ No error on LS1 switch (default value)<br>$1_B$ Overcurrent detected on LS1 switch. Error latched and LS1 disabled. |

### SYS_DIAG_3 : OP_ERROR_2_STAT

**Overcurrent error status of half-bridge outputs 5 - 8 (Address Byte [OP]011 10[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB8_HS_OC** | **HB8_LS_OC** | **HB7_HS_OC** | **HB7_LS_OC** | **HB6_HS_OC** | **HB6_LS_OC** | **HB5_HS_OC** | **HB5_LS_OC** |
| rc | rc | rc | rc | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB8_HS_OC** | D7 | rc | **High-side (HS) switch of half-bridge 8 overcurrent detection**<br>$0_B$ No error on HS8 switch (default value)<br>$1_B$ Overcurrent detected on HS8 switch. Error latched and HS8 disabled. |
| **HB8_LS_OC** | D6 | rc | **Low-side (LS) switch of half-bridge 8 overcurrent detection**<br>$0_B$ No error on LS8 switch (default value)<br>$1_B$ Overcurrent detected on LS8 switch. Error latched and LS8 disabled. |
| **HB7_HS_OC** | D5 | rc | **High-side (HS) switch of half-bridge 7 overcurrent detection**<br>$0_B$ No error on HS7 switch (default value)<br>$1_B$ Overcurrent detected on HS7 switch. Error latched and HS7 disabled. |
| **HB7_LS_OC** | D4 | rc | **Low-side (LS) switch of half-bridge 7 overcurrent detection**<br>$0_B$ No error on LS7 switch (default value)<br>$1_B$ Overcurrent detected on LS7 switch. Error latched and LS7 disabled. |
| **HB6_HS_OC** | D3 | rc | **High-side (HS) switch of half-bridge 6 overcurrent detection**<br>$0_B$ No error on HS6 switch (default value)<br>$1_B$ Overcurrent detected on HS6 switch. Error latched and HS6 disabled. |
| **HB6_LS_OC** | D2 | rc | **Low-side (LS) switch of half-bridge 6 overcurrent detection**<br>$0_B$ No error on LS6 switch (default value)<br>$1_B$ Overcurrent detected on LS6 switch. Error latched and LS6 disabled. |
| **HB5_HS_OC** | D1 | rc | **High-side (HS) switch of half-bridge 5 overcurrent detection**<br>$0_B$ No error on HS5 switch (default value)<br>$1_B$ Overcurrent detected on HS5 switch. Error latched and HS5 disabled. |
| **HB5_LS_OC** | D0 | rc | **Low-side (LS) switch of half-bridge 5 overcurrent detection**<br>$0_B$ No error on LS5 switch (default value)<br>$1_B$ Overcurrent detected on LS5 switch. Error latched and LS5 disabled. |

### SYS_DIAG_5 : OP_ERROR_4_STAT

**Open load error status of half-bridge outputs 1 - 4 (Address Byte [OP]000 01[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB4_HS_OL** | **HB4_LS_OL** | **HB3_HS_OL** | **HB3_LS_OL** | **HB2_HS_OL** | **HB2_LS_OL** | **HB1_HS_OL** | **HB1_LS_OL** |
| rc | rc | rc | rc | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB4_HS_OL** | D7 | rc | **High-side (HS) switch of half-bridge 4 open load detection**<br>$0_B$ No error on HS4 switch (default value)<br>$1_B$ Open load detected on HS4 switch. Error latched. |
| **HB4_LS_OL** | D6 | rc | **Low-side (LS) switch of half-bridge 4 open load detection**<br>$0_B$ No error on LS4 switch (default value)<br>$1_B$ Open load detected on LS4 switch. Error latched. |
| **HB3_HS_OL** | D5 | rc | **High-side (HS) switch of half-bridge 3 open load detection**<br>$0_B$ No error on HS3 switch (default value)<br>$1_B$ Open load detected on HS3 switch. Error latched. |
| **HB3_LS_OL** | D4 | rc | **Low-side (LS) switch of half-bridge 3 open load detection**<br>$0_B$ No error on LS3 switch (default value)<br>$1_B$ Open load detected on LS3 switch. Error latched. |
| **HB2_HS_OL** | D3 | rc | **High-side (HS) switch of half-bridge 2 open load detection**<br>$0_B$ No error on HS2 switch (default value)<br>$1_B$ Open load detected on HS2 switch. Error latched. |
| **HB2_LS_OL** | D2 | rc | **Low-side (LS) switch of half-bridge 2 open load detection**<br>$0_B$ No error on LS2 switch (default value)<br>$1_B$ Open load detected on LS2 switch. Error latched. |
| **HB1_HS_OL** | D1 | rc | **High-side (HS) switch of half-bridge 1 open load detection**<br>$0_B$ No error on HS1 switch (default value)<br>$1_B$ Open load detected on HS1 switch. Error latched. |
| **HB1_LS_OL** | D0 | rc | **Low-side (LS) switch of half-bridge 1 open load detection**<br>$0_B$ No error on LS1 switch (default value)<br>$1_B$ Open load detected on LS1 switch. Error latched. |

### SYS_DIAG_6 : OP_ERROR_5_STAT

**Open load error status of half-bridge outputs 5 - 8 (Address Byte [OP]100 01[LABT]$1_B$)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **HB8_HS_OL** | **HB8_LS_OL** | **HB7_HS_OL** | **HB7_LS_OL** | **HB6_HS_OL** | **HB6_LS_OL** | **HB5_HS_OL** | **HB5_LS_OL** |
| rc | rc | rc | rc | rc | rc | rc | rc |

| Field | Bits | Type | Description |
|---|---|---|---|
| **HB8_HS_OL** | D7 | rc | **High-side (HS) switch of half-bridge 8 open load detection**<br>$0_B$ No error on HS8 switch (default value)<br>$1_B$ Open load detected on HS8 switch. Error latched. |
| **HB8_LS_OL** | D6 | rc | **Low-side (LS) switch of half-bridge 8 open load detection**<br>$0_B$ No error on LS8 switch (default value)<br>$1_B$ Open load detected on LS8 switch. Error latched. |
| **HB7_HS_OL** | D5 | rc | **High-side (HS) switch of half-bridge 7 open load detection**<br>$0_B$ No error on HS7 switch (default value)<br>$1_B$ Open load detected on HS7 switch. Error latched. |
| **HB7_LS_OL** | D4 | rc | **Low-side (LS) switch of half-bridge 7 open load detection**<br>$0_B$ No error on LS7 switch (default value)<br>$1_B$ Open load detected on LS7 switch. Error latched. |
| **HB6_HS_OL** | D3 | rc | **High-side (HS) switch of half-bridge 6 open load detection**<br>$0_B$ No error on HS6 switch (default value)<br>$1_B$ Open load detected on HS6 switch. Error latched. |
| **HB6_LS_OL** | D2 | rc | **Low-side (LS) switch of half-bridge 6 open load detection**<br>$0_B$ No error on LS6 switch (default value)<br>$1_B$ Open load detected on LS6 switch. Error latched. |
| **HB5_HS_OL** | D1 | rc | **High-side (HS) switch of half-bridge 5 open load detection**<br>$0_B$ No error on HS5 switch (default value)<br>$1_B$ Open load detected on HS5 switch. Error latched. |
| **HB5_LS_OL** | D0 | rc | **Low-side (LS) switch of half-bridge 5 open load detection**<br>$0_B$ No error on LS5 switch (default value)<br>$1_B$ Open load detected on LS5 switch. Error latched. |

# 8 Application Information

*Note: The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application.*

## 8.1 Application Diagram

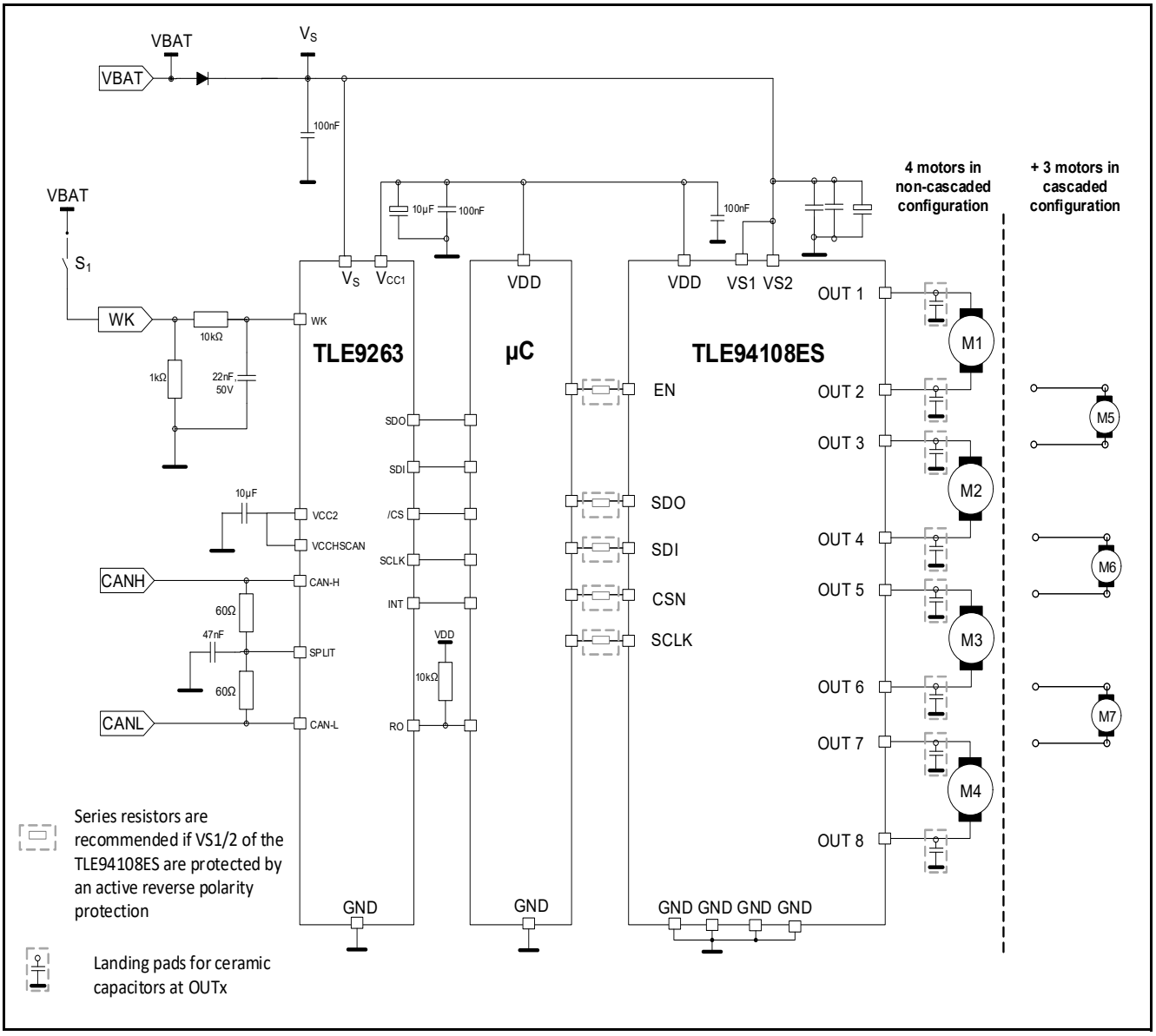



**Figure 27 Application example for DC-motor loads**

## Application Information

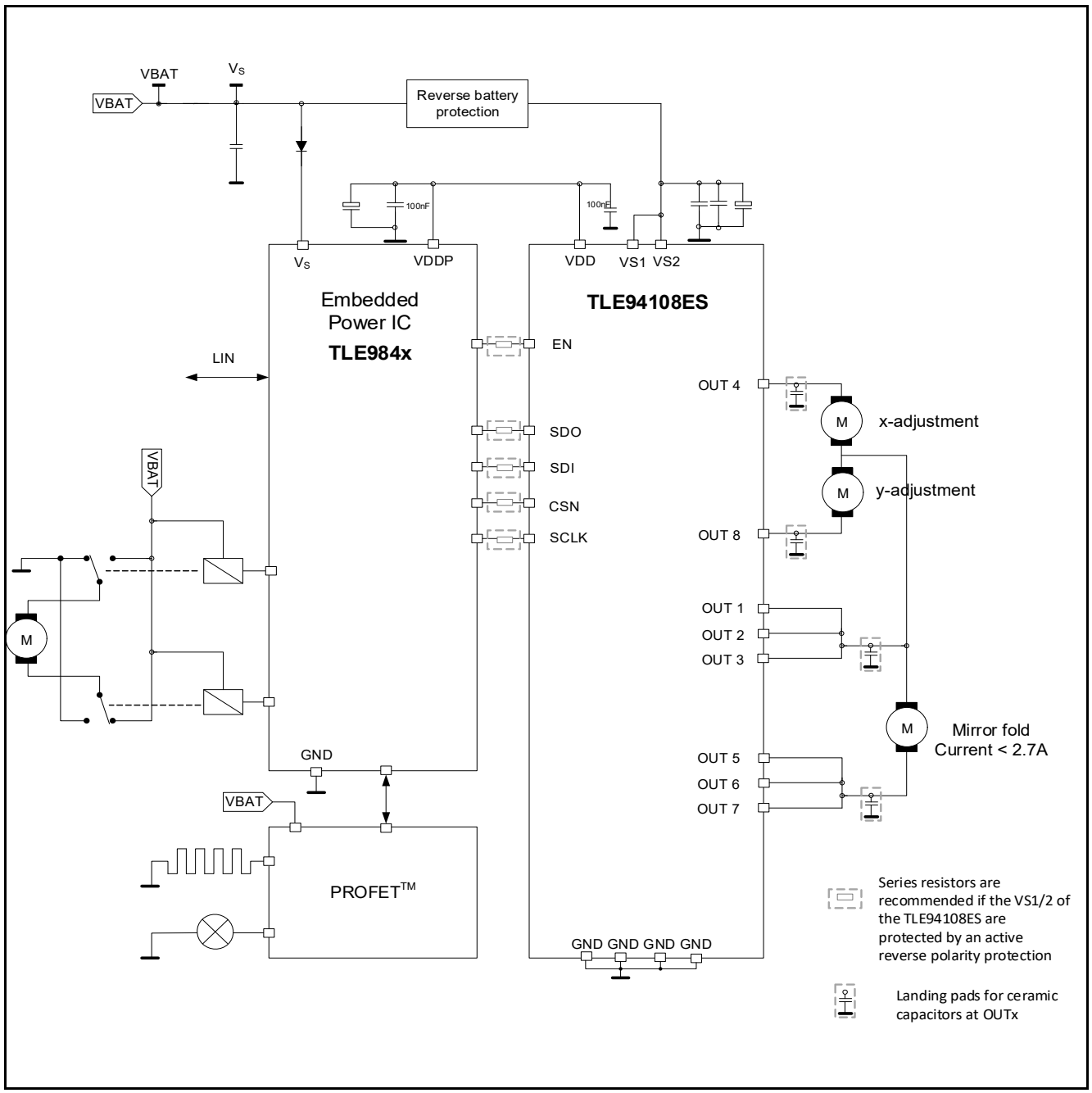



**Figure 28 Application example for side mirror control**

### Notes on the application example

1. *Series resistors between the microcontroller and the signal pins of the TLE94108ES are recommended if an active reverse polarity protection (MOSFET) is used to protect VS1 and VS2 pins. These resistors limit the current between the microcontroller and the device during negative transients on VBAT (e.g. ISO/TR 7637 pulse 1)*
2. *Landing pads for ceramic capacitors at the outputs of the TLE94108ES as close as possible to the connectors are recommended (the ceramic capacitors are not populated if unused). These ceramic capacitors can be mounted if a higher performance in term of ESD capability is required.*
3. *The electrolytic capacitor at the VSx pins should be dimensioned in order to prevent the VS voltage from exceeding the absolute maximum rating. PWM operation with a too low capacitance can lead to a VS voltage overshoot, which results in a VS overvoltage detection.*

4. *Not used (NU) pins and unused outputs are recommended to be left unconnected (open) in the application. If NU pins or unused output pins are routed to an external connector which leaves the PCB, then these outputs should have provision for a zero ohm jumper (depopulated if unused) or ESD protection. In other words, NU and unused pins should be treated like used pins.*
5. *Place bypass ceramic capacitors as close as possible to the VSx pins, with shortest connections the GND pins and GND layer, for best EMC performance*

## 8.2 Thermal application information

Ta = 85°C, Ch1 to Ch8 are dissipating a total of 1.08W (0.135W each).

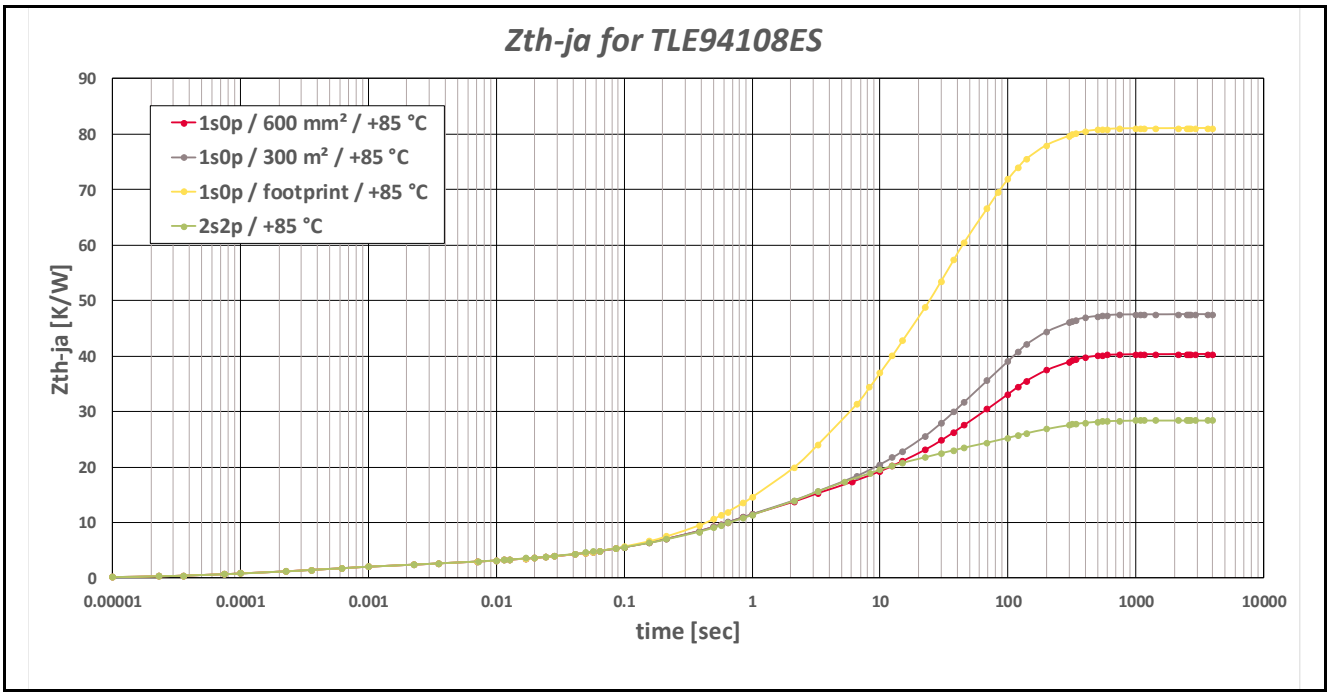



**Figure 29 ZthJA Curve for different PCB setups**

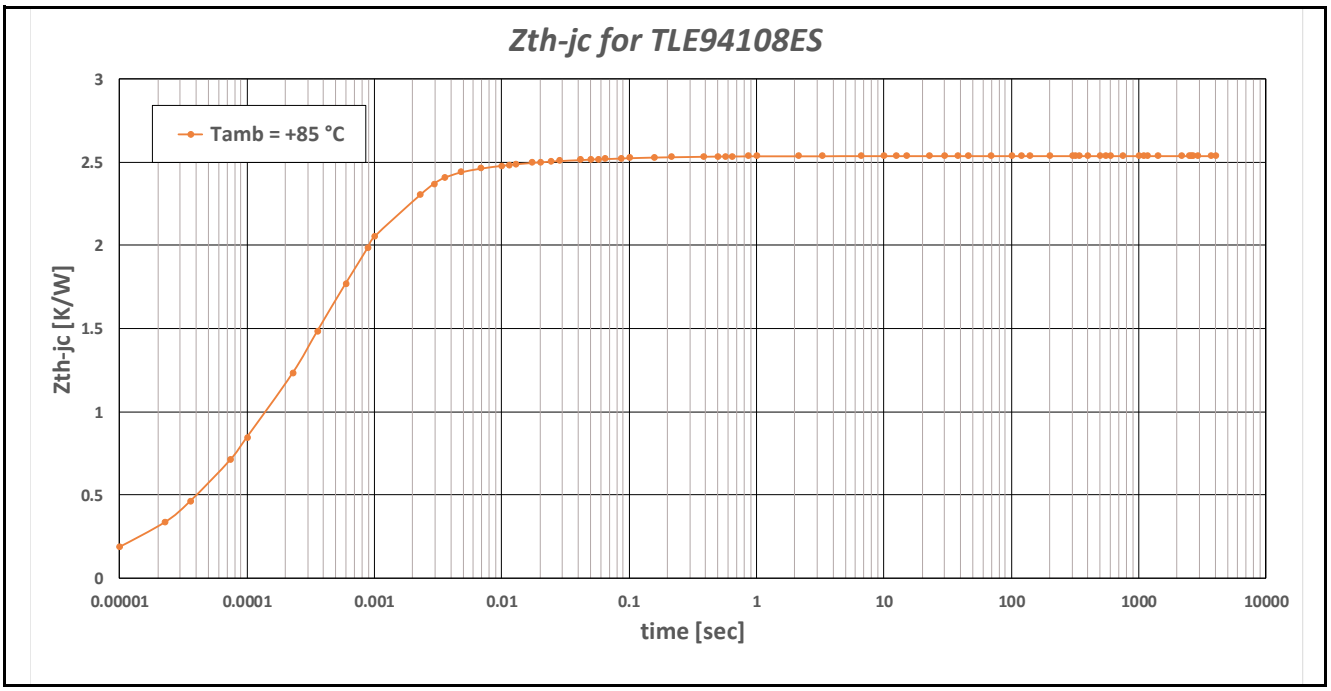



**Figure 30 ZthJC Curve**

## 8.3 EMC Enhancement

In the event the emissions of the device exceed the allowable limits, a modulation of the oscillator frequency is incorporated to reduce eventual harmonics of the 8MHz base clock. The frequencies can be selected based on the resolution bandwidth of the peak detector during EMC testing.

The selection is achieved by setting the FM_CLK_MODn bits in the PWM_CH_FREQ_CTRL register as follows:

$00_B$: OFF

$01_B$: FM CLK=15.625 kHZ

$10_B$: FM CLK=31.25 kHz

$11_B$: FM CLK=62.5 kHz

# 9 Package Outlines

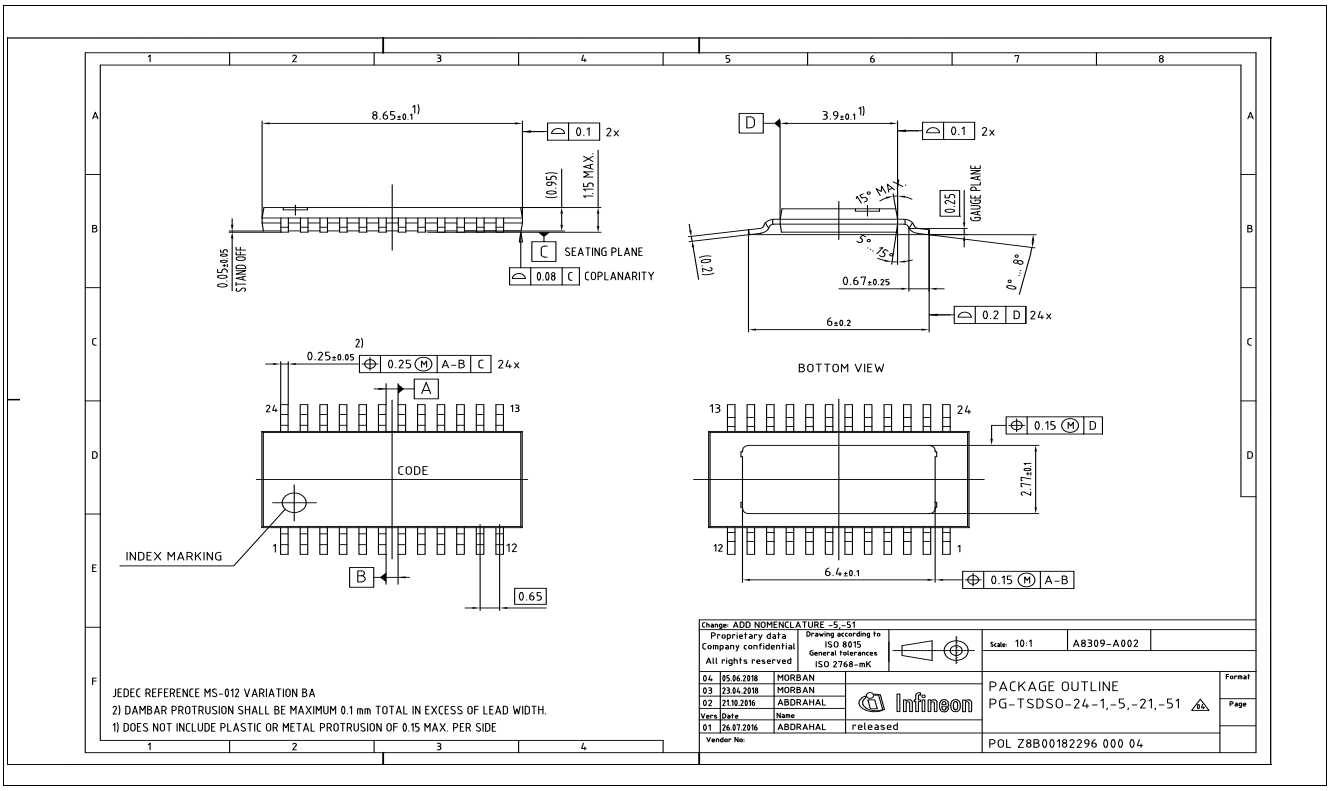



**Figure 31 PG-TSDSO-24** (Plastic/Plastic Green - Dual Small Outline Package)

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e lead-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
**http://www.infineon.com/packages**.

Dimensions in mm

# 10 Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2020-09-29 | Initial release |

**Edition 2020-09-29**
**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**



**Do you have a question about any aspect of this document?**
**Email: erratum@infineon.com**

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Motor/Motion/Ignition Controllers & Drivers ***category:***

***Click to view products by*** Infineon ***manufacturer:***

Other Similar products are found below :

FSB50550TB2 MSVCPM2-63-12 MSVGW45-14-2 MSVGW54-14-3 NTE7043 LA6565VR-TLM-E LB1837M-TLM-E STK534U342C-E AM4967GSTR-G1 TB6562AFG(O,8,EL) BA5839FP-E2 VND5T050AK-E LA6584JA-AH LB11961-W-AH LC898212XD-SH NCV70501DW002R2G TND315S-TL-2H FSB50250AB FNA41060 MSVBTC50E MSVCPM3-54-12 MSVCPM3-63-12 MSVCPM4-63-12 FSB50550AB L99MC6TR LC898301XA-MH LV8413GP-TE-L-E MSVGW45-14-3 MSVGW54-14-4 TB6552FNG,C,8,EL LB11651-E IRSM515-025DA4 LV8127T-TLM-H MC33812EKR2 MC33PT2000AF LB11851FA-BH LB1938FAGEVB TB6569FTG,8,EL STIPN2M50-H BH67172NUX-GE2 RSHR4006BV20 DMPU-CPAN DMPU-CPC DMPUC-R2 AIS-D-42MA FNB81560T3 NCV7535DBR2G NCP81274MNTXG PT8A2767FWEX IM240S6Y1BAKMA1