TLF80511

Low Dropout Linear Fixed Voltage Regulator

TLF80511TC

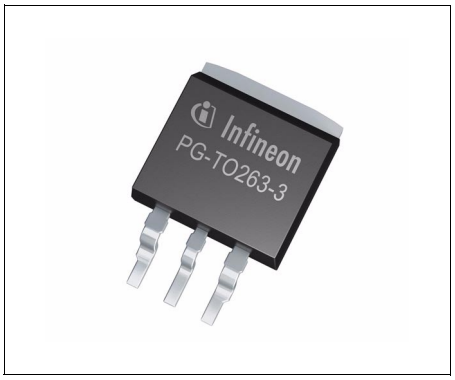
Data Sheet

Rev. 1.01, 2016-06-21

Automotive Power

Low Dropout Linear Fixed Voltage Regulator **TLF80511**
TLF80511V50

1 Overview



PG-TO263-3

Features

- Output Voltage 5 V
- Output Voltage Precision ± 2 %
- Output Current up to 400 mA
- Ultra Low Current Consumption 38 µA
- Very Low Dropout Voltage: 100 mV at 100 mA Output Current
- Extended Operating Range Starting at 3.3 V
- Small Output Capacitor 1 µF
- Output Current Limitation
- Overtemperature Shutdown
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLF80511 is a linear low dropout voltage regulator for load currents up to 400 mA. An input voltage of up to 40 V is regulated to $V_{Q,nom}$ = 5 V with ±2 % precision.

The TLF80511 with a typical quiescent current of 38 µA, is the ideal solution for systems requiring very low operating currents, such as those permanently connected to a battery.

It features a very low dropout voltage of 100 mV, when the output current is less than 100 mA. In addition, the dropout region begins at input voltages of 3.3 V (extended operating range). This makes the TLF80511 suitable to supply automotive systems.

In addition, the TLF80511's new fast regulation concept requires only a single, 1 µF output capacitor to maintain stable regulation.

The device is designed for the harsh environment of automotive applications. Therefore standard features like output current limitation and overtemperature shutdown are implemented and protect the device against failures like output short circuit to GND, over-current and over-temperatures. The TLF80511 can be also used in all other applications requiring a stabilized 5 V supply voltage.

Type	Package	Marking
TLF80511TC	PG-TO263-3	TLF80511

2 Block Diagram

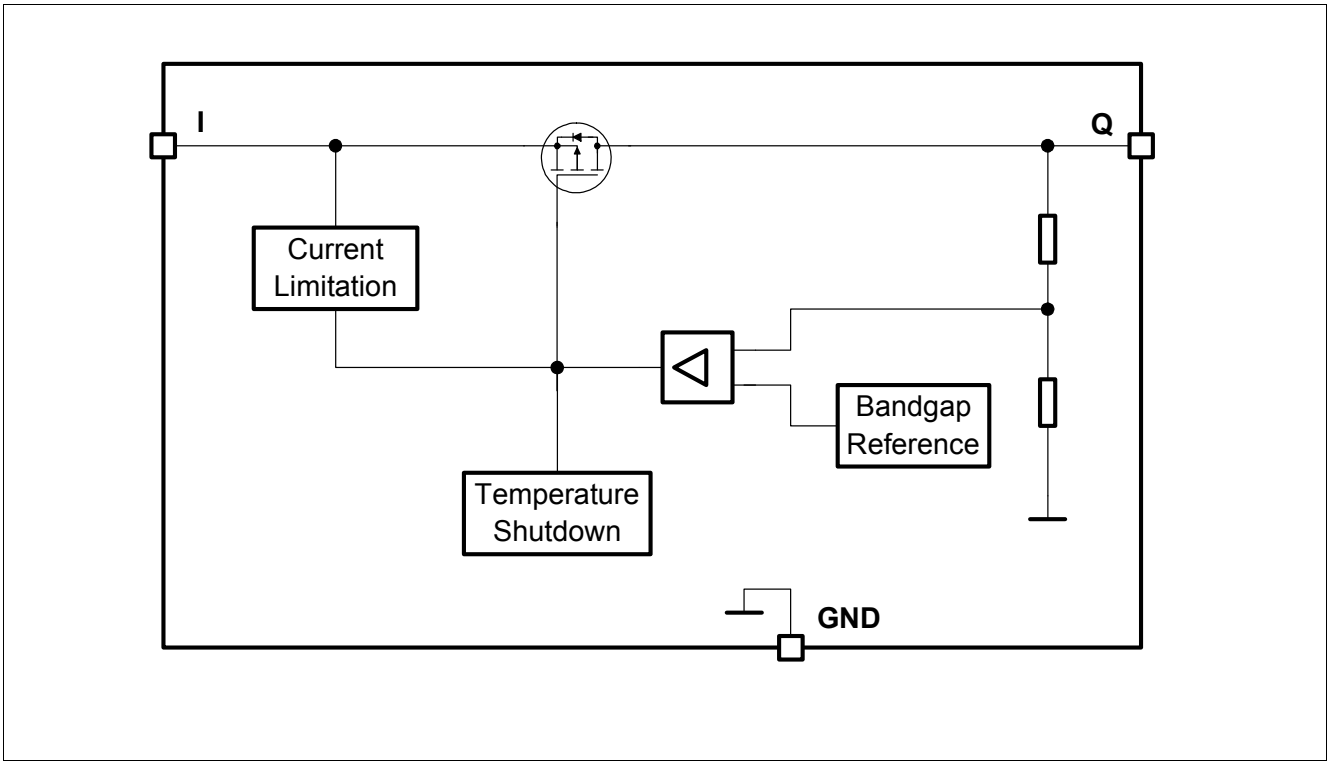


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment PG-TO263-3

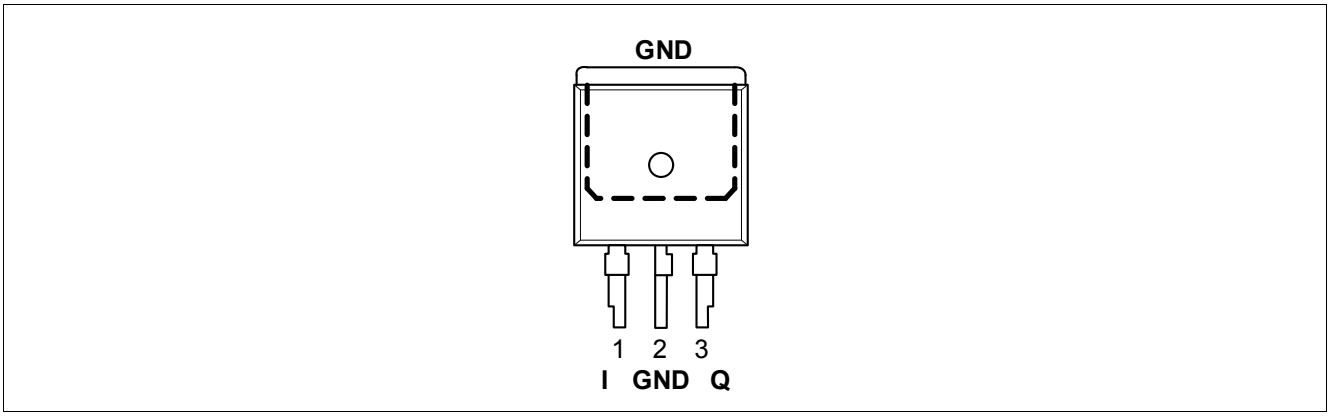


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions PG-TO263-3

Pin	Symbol	Function
1	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	GND	**Ground**
3	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **“Functional Range” on Page 6**
Tab	GND	**Heat Slug** connect to heatsink area; connect with GND on PCB

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

-40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input I						
4.1.1	Voltage	V_I	-0.3	45	V	–
Output Q						
4.1.2	Voltage	V_Q	-0.3	7	V	–
Temperature						
4.1.3	Junction Temperature	T_j	-40	150	°C	–
4.1.4	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Absorption						
4.1.5	ESD Absorption	$V_{ESD,HBM}$	-4	4	kV	Human Body Model (HBM)[2)]
4.1.6		$V_{ESD,CDM}$	-1.5	1.5	kV	Charge Device Model (CDM)[3)]

1) Not subject to production test, specified by design.
2) ESD HBM Test according AEC-Q100-002 - JESD22-A114 (1.5kOhm, 100pF)
3) ESD CDM Test according ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage Range for Normal Operation	V_I	$V_{Q,nom}$ + V_{dr}	40	V	–
4.2.2	Extended Input Voltage Range	$V_{I,ext}$	3.3	40	V	–[1]
4.2.3	Output Capacitor's Requirements for Stability	C_Q	1	–	µF	–[2]
		$ESR(C_Q)$	–	5	Ω	–[3]
4.2.4	Junction Temperature	T_j	-40	150	°C	–

1) Between min. value and $V_{Q,nom}$ + V_{dr}: V_Q = V_I - V_{dr}. Below min. value: V_Q = 0 V

2) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

3) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Package Versions PG-TO263-3							
4.3.1	Junction to Case[1]	R_{thJC}	–	4	–	K/W	–
4.3.2	Junction to Ambient[1]	R_{thJA}	–	22	–	K/W	[2]
4.3.3			–	65	–	K/W	footprint only[3]
4.3.4			–	39	–	K/W	300 mm² heatsink area on PCB[3]
4.3.5			–	33	–	K/W	600 mm² heatsink area on PCB[3]

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Voltage Regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **Table 4.2 "Functional Range" on Page 6** must be maintained. For details see the typical performance graph **"Stability Region: Equivalent Serial Resistor ESR versus Output Current IQ" on Page 12**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_I is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the regulator terminals.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the 150° C maximum and significantly reducing the IC's life.

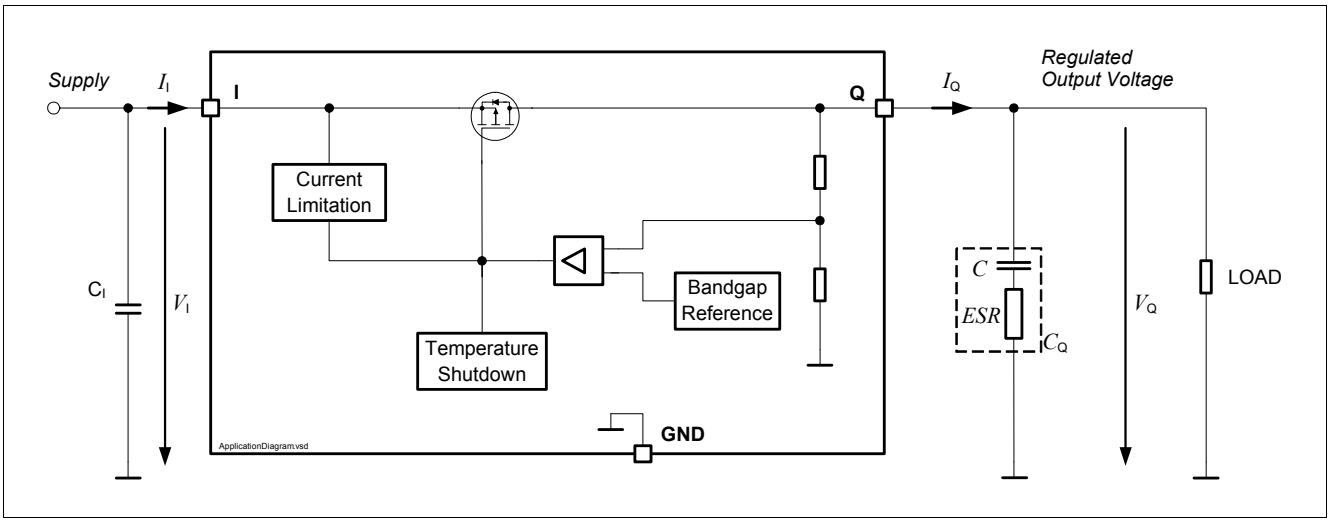


Figure 3 Block Diagram Voltage Regulation

Electrical Characteristics Voltage Regulator 5 V version

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Output Voltage Precision	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 400 mA 6 V < V_I < 28 V
5.1.2	Output Voltage Precision	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 200 mA 5.5 V < V_I < 40 V
5.1.3	Output Current Limitation	$I_{Q,max}$	401	600	900	mA	0 V < V_Q < 4.8 V
5.1.4	Load Regulation steady-state	$\lvert\Delta V_{Q,load}\rvert$	–	20	50	mV	I_Q = 0.05 mA to 400 mA V_I = 6 V
5.1.5	Line Regulation steady-state	$\lvert\Delta V_{Q,line}\rvert$	–	10	30	mV	V_I = 8 V to 32 V I_Q = 5 mA
5.1.6	Dropout Voltage[1] V_{dr} = V_I - V_Q	V_{dr}	–	250	500	mV	I_Q = 250 mA
			–	100	200	mV	I_Q = 100 mA
5.1.7	Power Supply Ripple Rejection[2]	$PSRR$	–	55	–	dB	f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp
5.1.8	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	175	200	°C	T_j increasing[2]
5.1.9	Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	15	–	K	T_j decreasing[2]

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V

2) Not subject to production test, specified by design

5.2 Current Consumption

Electrical Characteristics Current Consumption

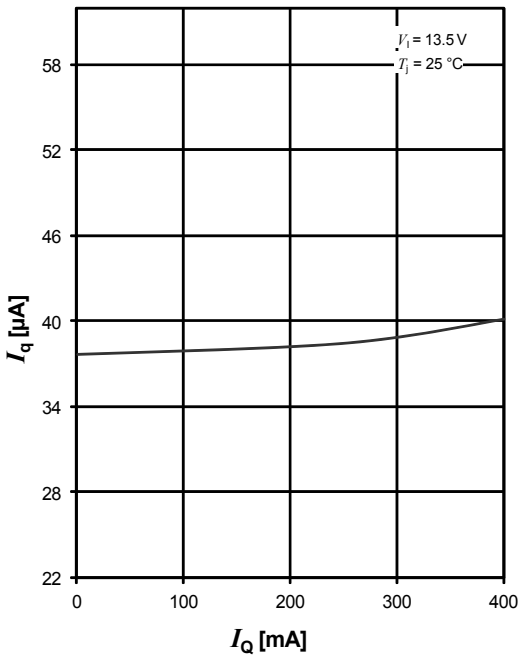
V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Current Consumption $I_q = I_I - I_Q$	I_q	–	38	46	µA	I_Q = 0.05 mA T_j < 25 °C
5.2.2			–	–	75	µA	I_Q = 0.05 mA T_j < 125 °C
5.2.3			–	67	80	µA	I_Q = 400 mA T_j < 125 °C[1)]

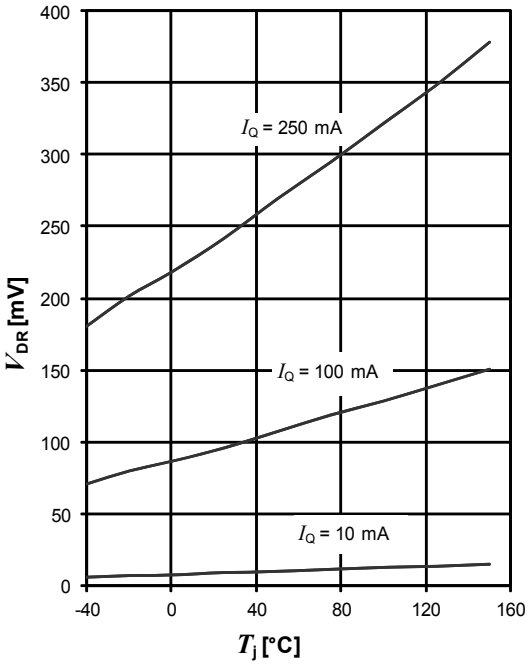
1) Not subject to production test, specified by design.

5.3 Typical Performance Characteristics Voltage Regulator

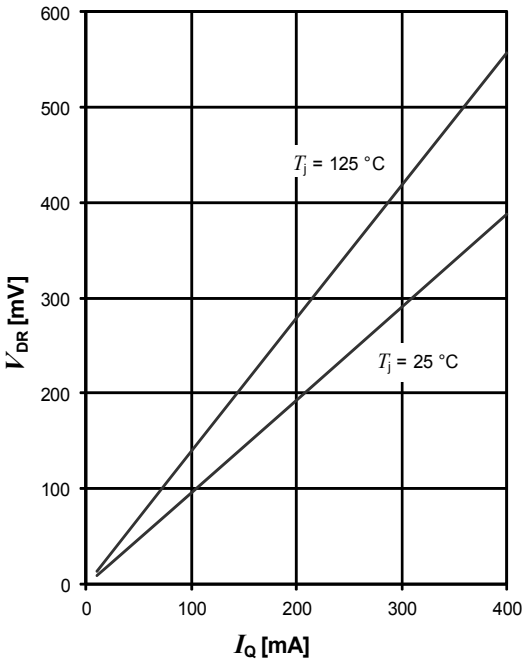
Current Consumption I_q versus Output Current I_Q



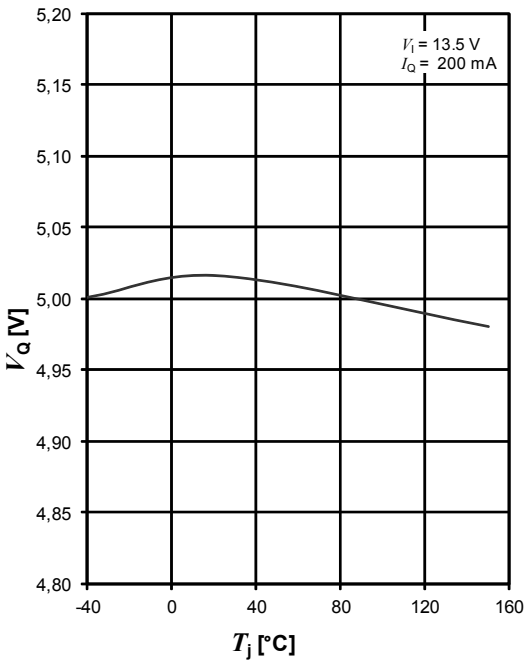
Dropout Voltage V_{dr} versus Junction Temperature T_j



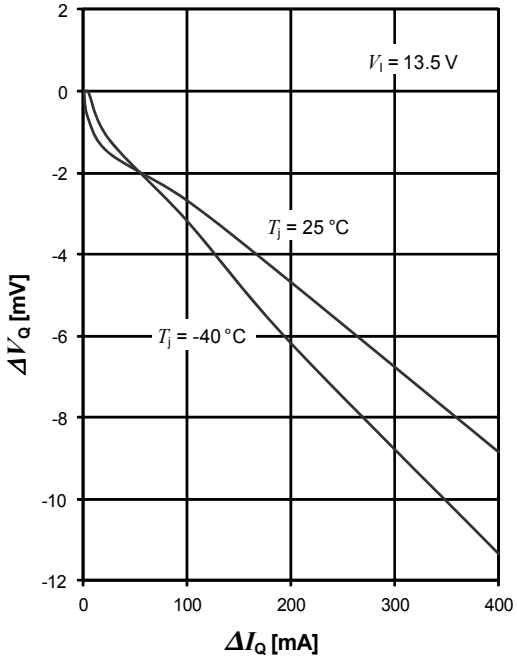
Dropout Voltage V_{dr} versus Output Current I_Q



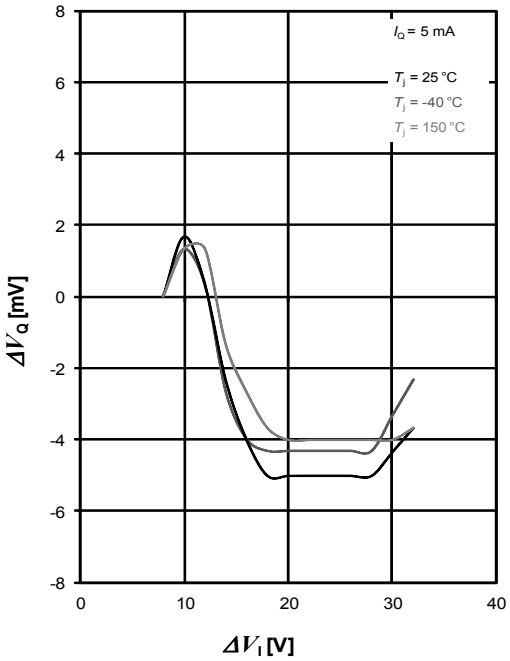
Output Voltage V_Q versus Junction Temperature T_j



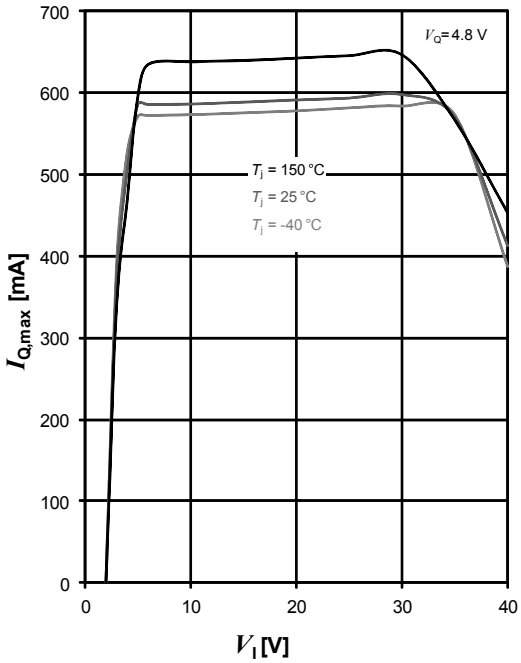
Output Voltage ΔV_Q versus Output Current ΔI_Q



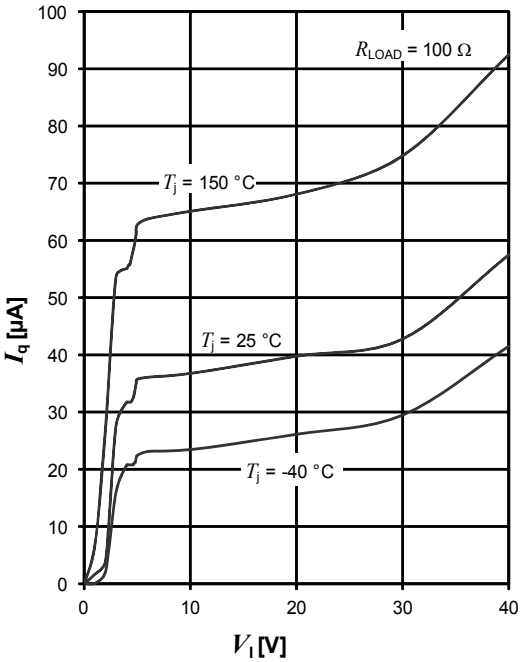
Output Voltage ΔV_Q versus Input Voltage ΔV_I



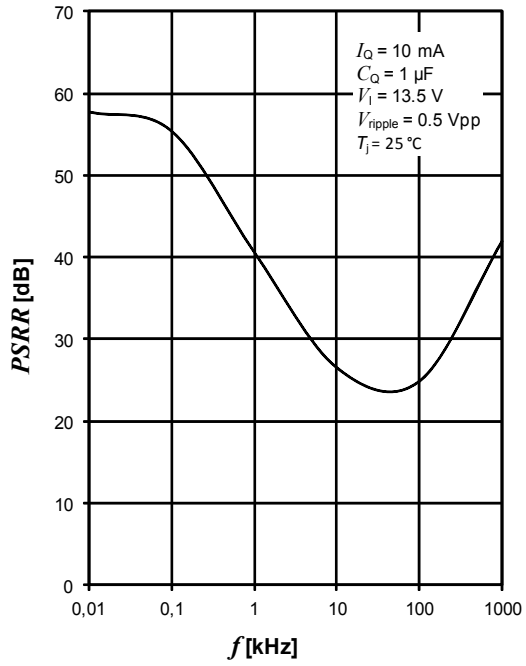
Maximum Output Current I_Q versus Input Voltage V_I



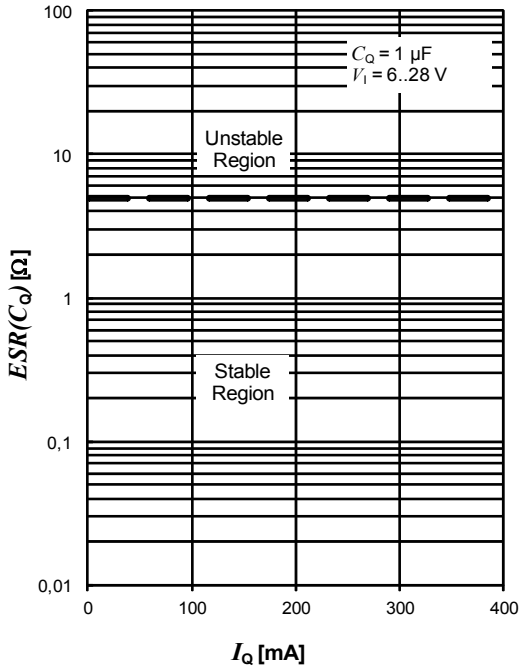
Current Consumption I_q versus Input Voltage V_I



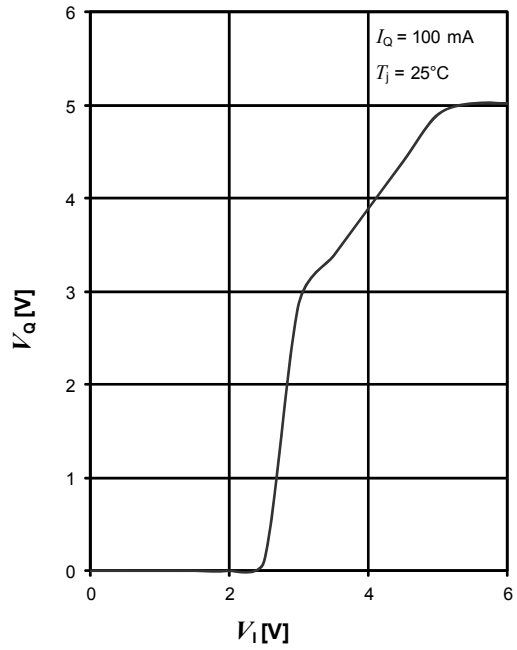
Power Supply Ripple Rejection versus Frequency



Stability Region: Equivalent Serial Resistor *ESR* versus Output Current I_Q



Output Voltage V_Q versus Input Voltage V_I



6 Package Outlines

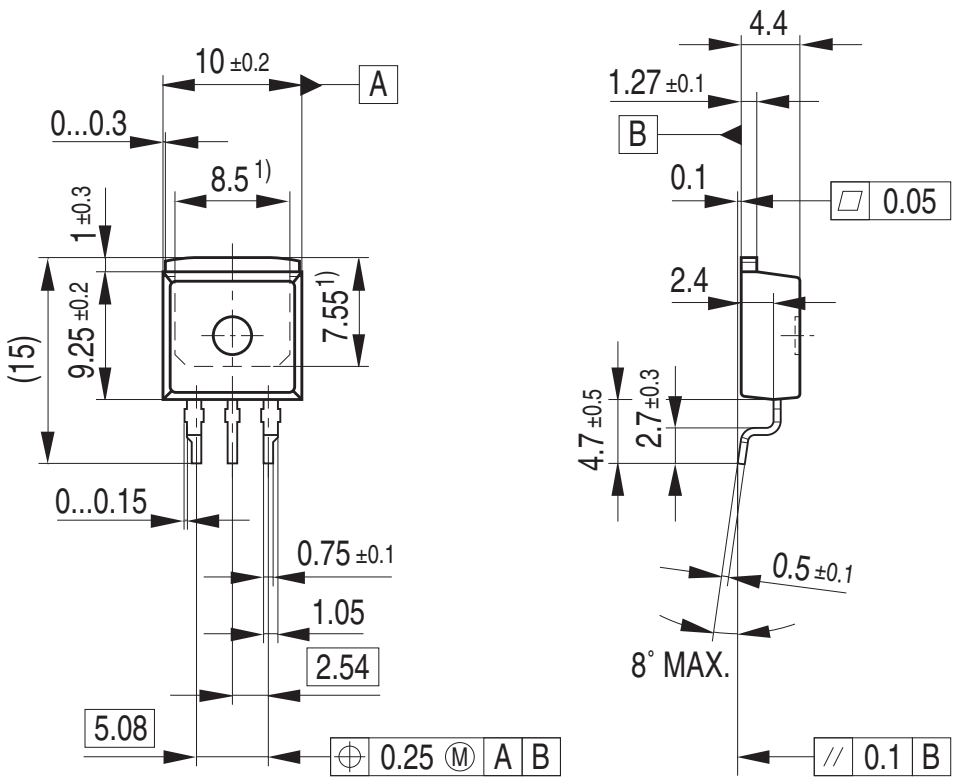


Figure 4 PG-TO263-3

7 Revision History

Revision	Date	Changes
1.01	2016-06-21	Editorial change: corrected page number Updated disclaimer
1.0	2012-06-15	Data Sheet - Initial Version

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Edition 2016-06-21
Published by
Infineon Technologies AG
81726 Munich, Germany

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