OPTIREG™ linear voltage regulator TLS8xxx2ELVxx demoboard

Z8F61720705

Family overview Support

Preface

Scope and purpose

This document provides information about the usage of the demoboards for the low dropout linear voltage regulators

- TLS820B2ELVSE
- TLS820D2ELVSE
- TLS835B2ELV
- TLS835B2ELVSE
- TLS835D2ELVSE

in a PG-SSOP-14 package from Infineon Technologies AG.

Intended audience

This document is intended for engineers who develop applications.

Table of contents

1 Introduction

1.1 Feature sets and packages

Table 1 shows an overview of the feature sets and packages in the TLS8xxx2ELVxx voltage regulator family.

Table 1   **Feature sets and packages**

Type	Package	Output current	Enable	Reset	Output voltage
TLS820B2ELVSE	PG-SSOP-14	200 mA	✓	–	3.3 V or 5 V
TLS820D2ELVSE	PG-SSOP-14	200 mA	✓	✓	3.3 V or 5 V
TLS835B2ELV	PG-SSOP-14	350 mA	✓	–	adjustable
TLS835B2ELVSE	PG-SSOP-14	350 mA	✓	–	3.3 V or 5 V
TLS835D2ELVSE	PG-SSOP-14	350 mA	✓	✓	3.3 V or 5 V

1.2 TLS8xxx2ELVxx features

- Wide input voltage range from 3.0 V to 40 V
- Output voltage selectable (3.3 V and 5 V) or adjustable (between 1.5 V and 6 V)
- 200 mA or 350 mA current capability
- Output voltage accuracy ≤ ±2%
- Ultra low current consumption, typically 20 µA
- Very low dropout voltage, typical 100 mV at 100 mA
- Stable with ceramic output capacitor of 1 µF
- Adjustable reset threshold down to 2 V[1]
- Wide temperature range
- Green product (RoHS compliant)
- internal protection features make the devices robust against immediate damage:
  - output current limitation
  - overtemperature shutdown

These features make the voltage regulators perfectly suitable as automotive supplies that are connected to the battery permanently and that need to operate in cranking condition.

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1   For TLS820D2ELVSE, TLS835D2ELVSE.

1.3   Block diagram

*Figure 1* shows the block diagram of TLS835D2ELVSE, which offers the full feature set.
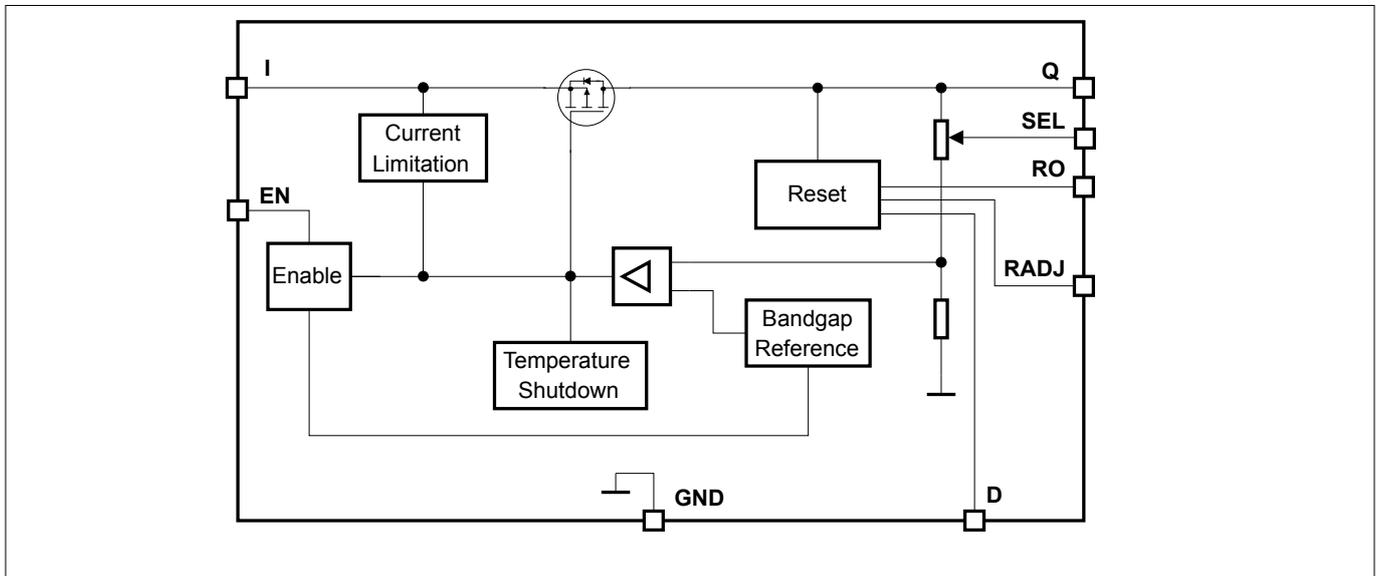
Figure 1   **Block diagram of TLS835D2ELVSE**

2 Demoboard

The OPTIREG™ linear voltage regulator TLS8xxx2ELVxx demoboard is available for all devices of the TLS8xxx2ELVxx voltage regulator family in a PG-SSOP-14 package, see **Table 1**.

2.1 Operating conditions

To avoid electrical damage of the demoboard, the operating range defined in **Table 2** must be followed.

Table 2   **Operating conditions**[2]

Parameter	Pin	Values		Unit	Note
		Min.	Max.		
Board supply voltage	VIN	0	40	V	power supply
Regulator output voltage	VOUT	0	6	V	[3]
Enable input signal	EN	0	40	V	enable or disable voltage regulator
Reset output signal	RO	0	5	V	[4] indicates, whether reset occurred
Ground	GND	0	0	V	system GND

2.2 Demoboard configuration

The TLS8xxx2ELVxx demoboard can be easily configured via jumpers on the board. The board provides the following configuration options:

- Input capacitor C1 (X7)
- Enable function (X8)
- Placeholder for additional output capacitor (C4)
- Placeholder for external pull-up resistor for reset output RO (R2)
- Selectable output voltage (X9)
- Adjustable output voltage: placeholder for voltage divider (R3, R4) and jumper (X10)
- Adjustable reset threshold: placeholder for voltage divider (R5, R6) and jumper (X11)
- Reset timing selection (X12)

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2   Demoboard operates at an ambient temperature of 25°C.
3   Nominal output voltage depends on voltage version.
4   For TLS820D2ELVSE, TLS835D2ELVSE.

2.2.1 Jumper settings for all variants

Header X7 (Input capacitor C1)

A capacitor C1 of 47 µF can be connected to VIN by placing a jumper on X7.

Header X8 (Enable function)

EN input pin can be configured by X8.

Table 3 **Header X8 options for Enable function**

X8	Function
EN ↔ VIN	The regulator is enabled while the EN pin is connected to VIN
EN ↔ GND	The regulator is disabled while the EN pin is connected to GND
open	The EN input pin is supplied from the EN banana jack connector[5]

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5   Without supplying a signal to EN, the regulator is disabled due to the internal pull-down resistor.

2.2.2 Jumper settings TLS820B2ELVSE, TLS835B2ELVSE

Headers X9 (selectable output voltage)

The output voltage can be configured via X9.

Table 4 **Header X9 options for selectable output voltage**

X9	Function
SEL ↔ VOUT	[6] Sets VOUT to 5 V
SEL ↔ GND	Sets VOUT to 3.3 V

Headers X10, X11 and X12

These headers are not relevant. They can be set to open or as shown in **Figure 2**.

Default setting of the jumpers TLS820B2ELVSE, TLS835B2ELVSE

Figure 2 shows the default setting of the jumpers of TLS835B2ELVSE and TLS820B2EVLSE demoboards.
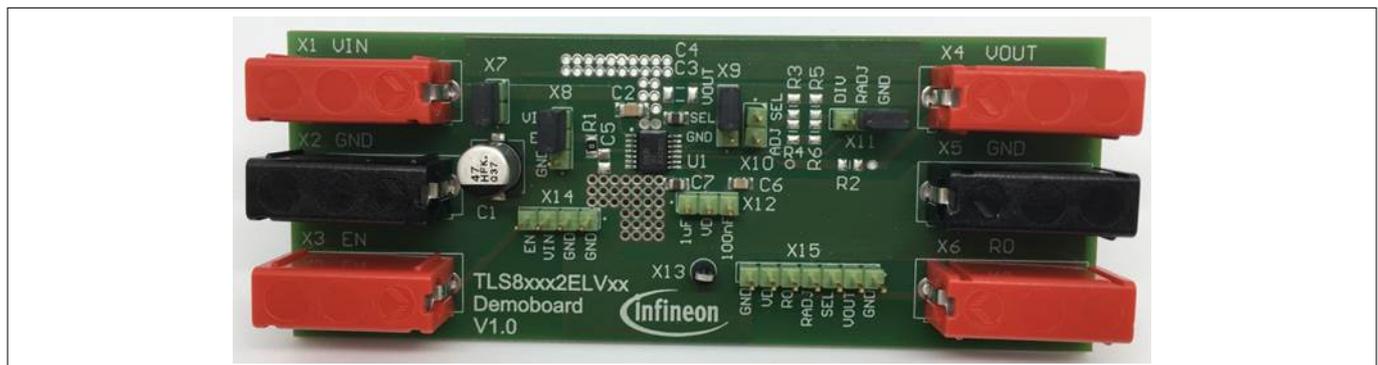
Figure 2 **TLS820B2ELVSE and TLS835B2ELVSE default jumper setting**

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6   Default setting.

2.2.3 Jumper settings TLS820D2ELVSE, TLS835D2ELVSE

Headers X9 (selectable output voltage)

The output voltage can be configured via X9.

Table 5 **Header X9 options for selectable output voltage**

X9	Function
SEL ↔ VOUT	[7] sets VOUT to 5 V
SEL ↔ GND	sets VOUT to 3.3 V

Headers X12 (Reset timing selection)

Reset delay timing can be configured via X12.

Table 6 **Header X12 options for reset delay timing**

X12	Function
VD ↔ 100nF	[7] Sets the reset delay time to typically 10 μs
VD ↔ 1uF	Sets the reset delay time to typically 28 μs

Headers X11 (Adjustable reset threshold)

Reset threshold can be configured via X11 and voltage divider R5, R6.

Table 7 **Header X11 options for adjustable reset threshold**

X11	Function
RADJ ↔ GND	[7] Sets the default reset threshold
RADJ ↔ DIV	Sets a reset threshold between 2 V and 4.2 V (for 5 V output voltage), or between 2 V and 2.75 V (for 3.3 V output voltage), depending on the voltage divider R5, R6

The undervoltage reset switching threshold can be adjusted according to the application's requirements by connecting an external voltage divider (R5, R6). For selecting the default threshold connect RADJ to GND.

With a voltage divider connected, the reset switching threshold $V_{\text{RT,low,new}}$ is calculated according to the following formula:

$$V_{\text{RT, low, new}} = V_{\text{RADJ, th}} \left(\frac{R5}{R6} + 1 \right)$$

Equation 1

Header X10

Leave header X10 open as it is not relevant.

Default setting of the jumpers TLS820D2ELVSE, TLS835D2ELVSE

Figure 3 shows the default setting of the jumpers of the TLS820D2ELVSE, TLS835D2ELVSE demoboard.

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7   Default setting.
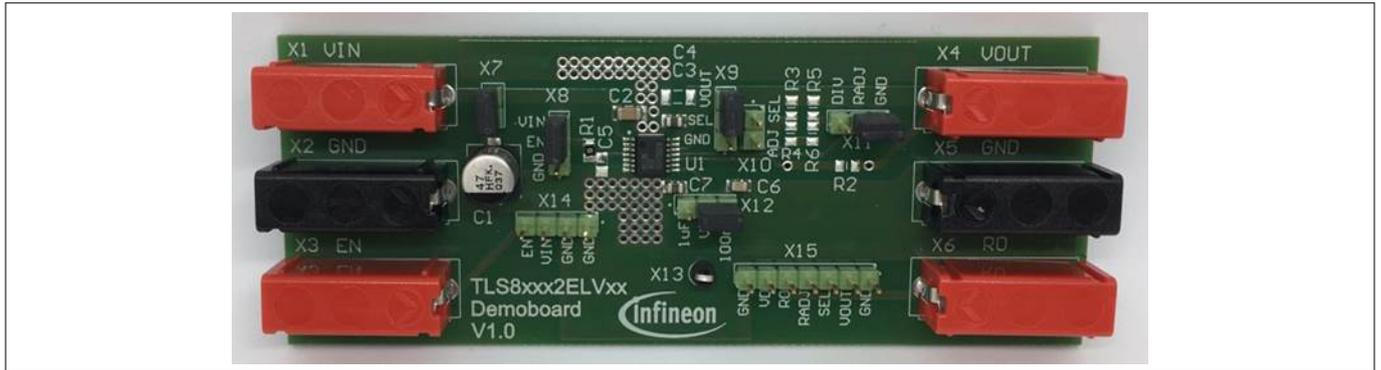
Figure 3   **TLS820D2ELVSE, TLS835D2ELVSE default jumper setting**

2.2.4 Jumper settings TLS835B2ELV

Headers X9 and X10 (Adjustable output voltage)

The output voltage can be configured via X9, X10 and voltage divider R3, R4.

Table 8 **Headers X9 and X10 options for adjustable output voltage**

X9 / X10	Function
X9: SEL ↔ VOUT X10: open	[8] Sets VOUT to 1.5 V
X9: open X10: SEL ↔ ADJ	Sets VOUT between 1.5 V and 6 V, depending on the voltage divider R3, R4

If the ADJ pin is to be supplied from the output voltage of the voltage divider, then the resistors of the voltage divider must be implemented. The value of the resistors can be easily calculated when neglecting the current flowing into the ADJ pin as follows:

$$\frac{R_1}{R_2} = \frac{V_Q}{V_{\text{ADJ}}} - 1$$

Equation 2

Headers X11 and X12

These headers are not relevant. They can be set to open or as shown in **Figure 4**.

Default setting of the jumpers TLS835B2ELV

Figure 4 shows the default setting of the jumpers of TLS835B2ELV demoboard.
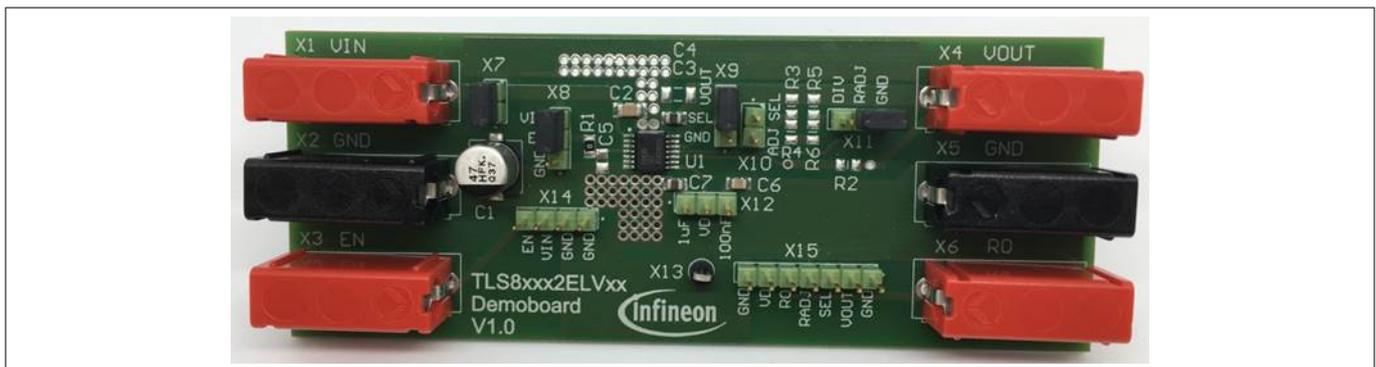
Figure 4 **TLS835B2ELV default jumper setting**

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8   Default setting.

2.2.5   Signal access

The connectors X13, X14 and X15 offer easy signal access, for example for probes of an oscilloscope.

Table 9   Signals on connector

Connector	Accessible signal
X13	• GND (ground)
X14	• EN (Enable input signal) • VIN (input voltage) • GND (ground) • GND (ground)
X15	• GND (ground) • VD (Reset delay setting) • RO (Reset output signal) • RADJ (Reset threshold setting) • SEL (output voltage selection) • VOUT (output voltage) • GND (ground)

3 Schematic and layout

3.1 Schematic
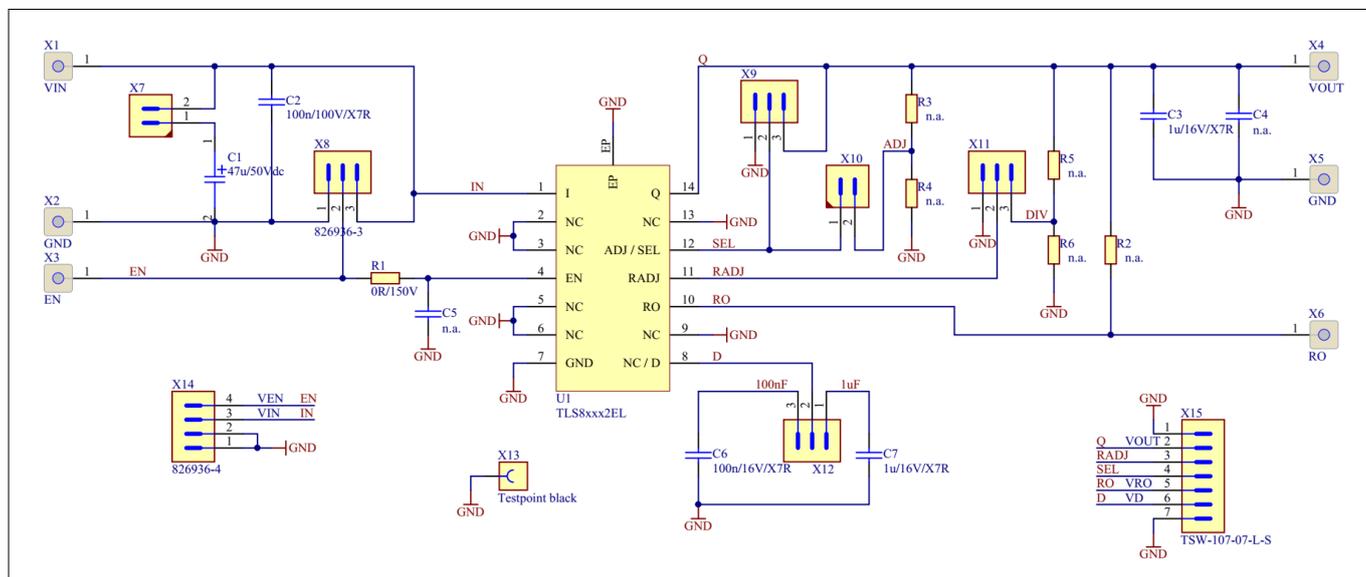
Figure 5   **Schematic**

3.2 Layout
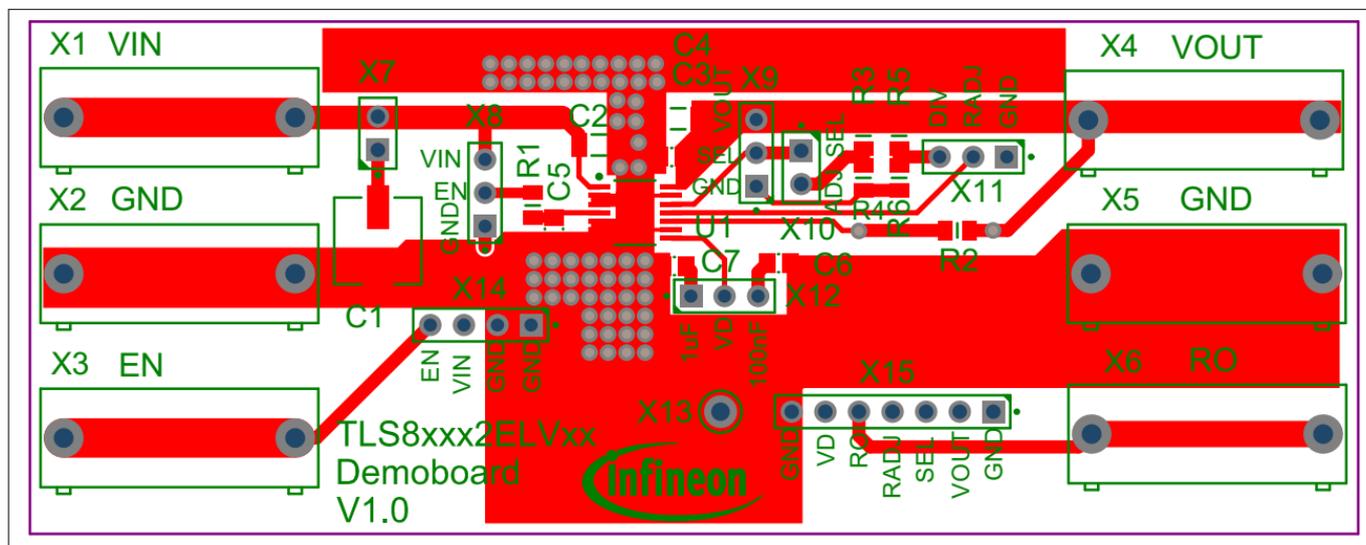
Figure 6   **Top layer**
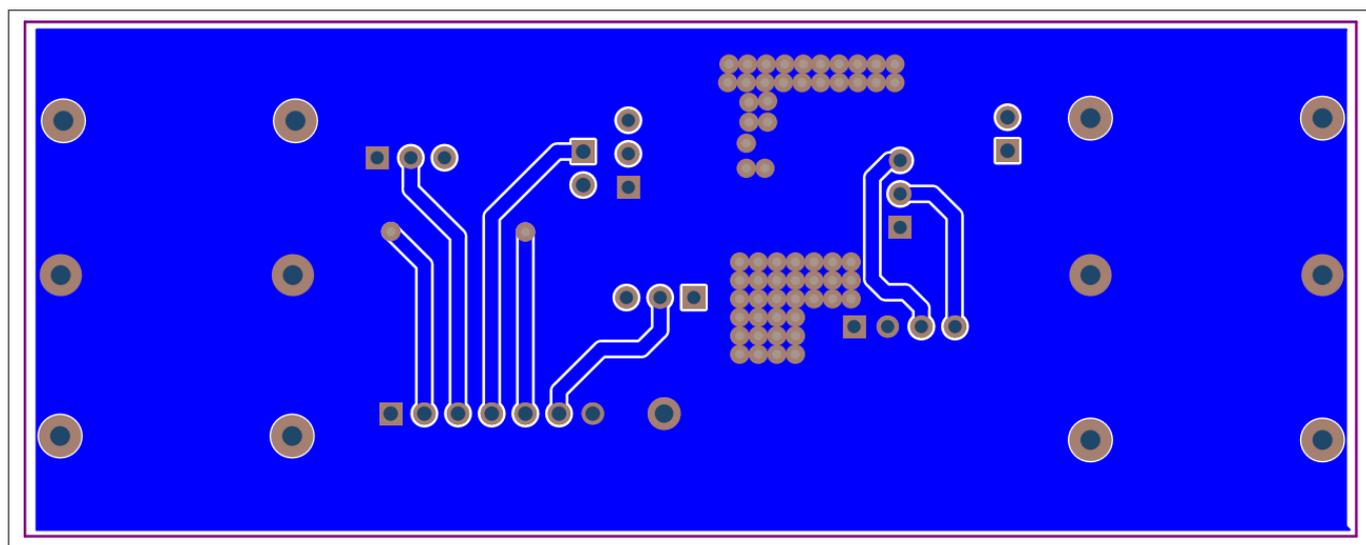
Figure 7   **Bottom layer**

4 Bill of materials

Table 10   **Bill of materials**

Part	Value	Package
U1	one of the following: • TLS820B2ELVSE • TLS820D2ELVSE • TLS835B2ELV • TLS835B2ELVSE • TLS835D2ELVSE	PG-SSOP-14
VIN	banana jack	BABU4MM
GND	banana jack	BABU4MM
EN	banana jack	BABU4MM
VOUT	banana jack	BABU4MM
GND	banana jack	BABU4MM
RO	banana jack	BABU4MM
R1	0 Ω	R0805
R2, R3, R4	n.a.	R0805
C1	47 µF / 50 V	SMD
C2	100 nF / 100 V	C1206
C3, C7	1 µF / 16 V	C0805
C4	n.a.	C1206
C5	n.a.	C0805
C6	100 nF / 100 V	C0805
X7, X10	2 pin header	–
X8, X9, X11, X12	3 pin header	–
X13	Test point	–
X14	4 pin header	–
X15	7 pin header	–

5 Restrictions

This demoboard offers limited features only for evaluation and testing of Infineon products. The demoboard is not an end product or finished appliance, nor is it intended or authorized by Infineon to be integrated into end products. The demoboard may not be used in any production system.

For further information please contact **www.infineon.com**.

6 Revision history

Revision	Date	Changes
1.1	2021-06-24	TLS820D2ELVSE added
1.0	2018-05-15	Document created

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