

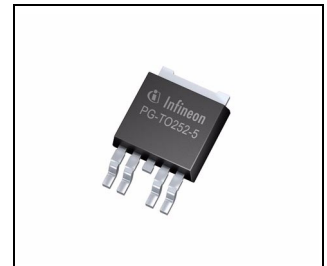
# OPTIREG™ Linear TLS850C2TEV33

## Low Dropout Linear Voltage Regulator



### Features

- Wide input voltage range from 3.0 V to 40 V
- Fixed output voltage 3.3 V
- Output voltage accuracy  $\leq \pm 2\%$
- Output current capability up to 500 mA
- Ultra low current consumption, typical 20  $\mu\text{A}$
- Very low dropout voltage, typical 120 mV at output currents below 100 mA
- Stable with ceramic output capacitor of 1  $\mu\text{F}$
- Reset output
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)



### Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The OPTIREG™ Linear TLS850C2TEV33 is a linear voltage regulator with high performance, very low dropout voltage and very low quiescent current.

With an input voltage range of 3 V to 40 V and very low quiescent current of only 20  $\mu\text{A}$ , this regulator is perfectly suitable for automotive or other supply systems permanently connected to the battery.

The new loop concept combines fast regulation and very high stability while requiring only one small ceramic capacitor of 1  $\mu\text{F}$  at the output. At output currents below 100 mA the device has a very low dropout voltage of only 120 mV. The operating range starts at an input voltage of only 3 V (extended operating range). This makes the TLS850C2TEV33 suitable for automotive systems that need to operate during cranking condition.

The reset feature supervises the output voltage, including undervoltage reset and delayed reset at power-on.

Internal protection features such as output current limitation and overtemperature shutdown, protect the device from immediate damage caused by failure such as output shorted to GND, overcurrent or overtemperature conditions.

**External components**

An input capacitor  $C_1$  is recommended to compensate for line influences. The output capacitor  $C_O$  is necessary for the stability of the regulating circuit. The TLS850C2TEV33 is designed to be stable with low ESR ceramic capacitors.

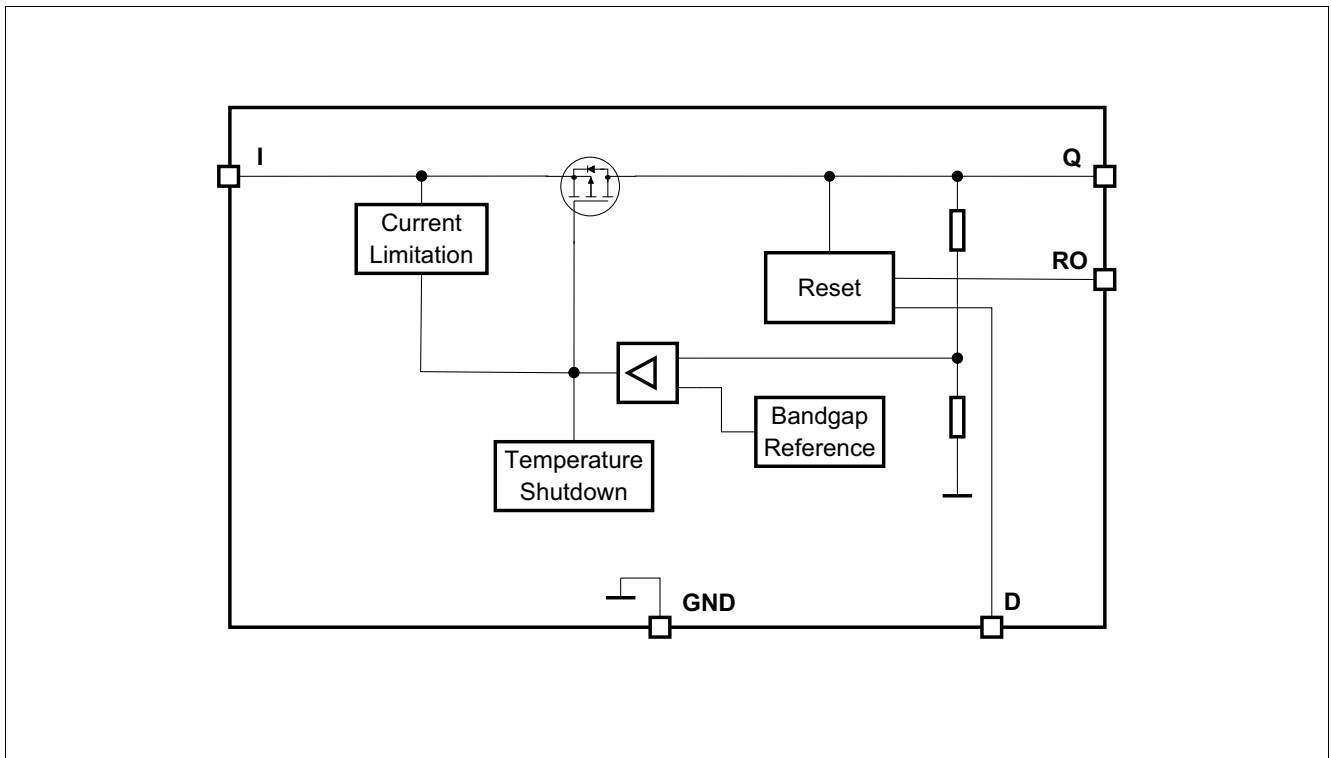
Type	Package	Marking
TLS850C2TEV33	PG-TO252-5	850C2V33

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**Block diagram**

**1 Block diagram**

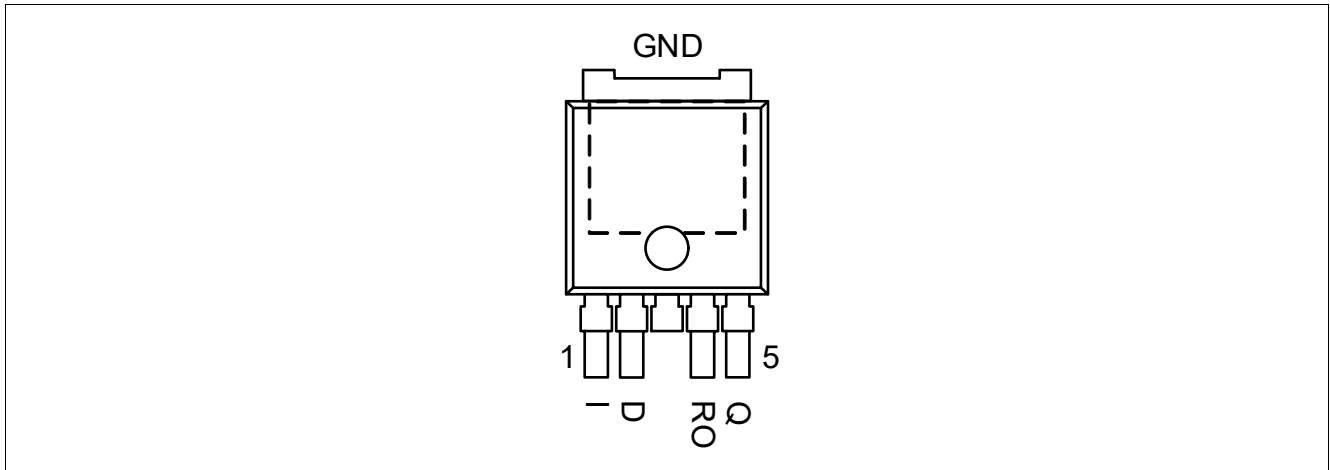


**Figure 1** Block diagram TLS850C2TEV33

**Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment TLS850C2TEV33**



**Figure 2 Pin configuration TLS850C2TEV33**

**2.2 Pin definitions and functions TLS850C2TEV33**

Pin	Symbol	Function
1	I	<b>Input</b> It is recommended to place a small ceramic capacitor to GND, close to the pins, in order to compensate line influences.
2	D	<b>Reset delay timing</b> Connect a ceramic capacitor to GND for adjusting the reset delay time. Leave open if the reset function is not needed.
3	GND	<b>Ground</b>
4	RO	<b>Reset output</b> (integrated pull-up resistor to Q) Open collector output. Leave open if the reset function is not needed.
5	Q	<b>Output</b> Connect output capacitor $C_Q$ to GND close to the pin, respecting the values specified for its capacitance and ESR in <b>“Functional range” on Page 7.</b>
Heat Slug	-	<b>Heat slug</b> Connect to heatsink area. Connect to GND.

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 1 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input I</b>							
Voltage	$V_I$	-0.3	-	45	V	-	P_3.1.1
<b>Output Q, reset output RO</b>							
Voltage	$V_Q, V_{RO}$	-0.3	-	7	V	-	P_3.1.2
<b>Reset delay D</b>							
Voltage	$V_D$	-0.3	-	7	V	-	P_3.1.4
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	-	150	°C	-	P_3.1.5
Storage temperature	$T_{stg}$	-55	-	150	°C	-	P_3.1.6
<b>ESD Absorption</b>							
ESD susceptibility	$V_{ESD,HBM}$	-2	-	2	kV	Human Body Model (HBM) <sup>2)</sup>	P_3.1.7
ESD susceptibility	$V_{ESD,CDM}$	-750	-	750	V	Charged Device Model (CDM) <sup>3)</sup> at all pins	P_3.1.8

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kV, 100 pF)

3) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

#### Notes

1. Exceeding the absolute max ratings may cause permanent damage to the device and affects the device's reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as operation outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

**General product characteristics**

**3.2 Functional range**

**Table 2 Functional range**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	$V_I$	$V_{Q,nom} + V_{dr}$	–	40	V	<sup>1)</sup> –	P_3.2.1
Extended input voltage range	$V_{I,ext}$	3.0	–	40	V	<sup>2)</sup> –	P_3.2.2
Capacitance of output capacitor for stability	$C_Q$	1	–	–	$\mu\text{F}$	<sup>3)4)</sup> –	P_3.2.4
Equivalent Series Resistance of output capacitor	$ESR(C_Q)$	–	–	50	$\Omega$	<sup>3)</sup> –	P_3.2.6
Junction temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	P_3.2.7

- 1) Output current is limited internally and depends on the input voltage, see electrical characteristics for more details.
- 2) If  $V_{I,ext,min} \leq V_I \leq V_{Q,nom} + V_{dr}$ , then  $V_Q = V_I - V_{dr}$ . If  $V_I < V_{I,ext,min}$ , then  $V_Q$  can drop to 0 V.
- 3) Not subject to production test, specified by design.
- 4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

**General product characteristics**

**3.3 Thermal resistance**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3 Thermal resistance TLS850C2TEV33 in PG-TO252-5 package**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	$R_{thJC}$	–	3.1	–	K/W	<sup>1)</sup> –	P_3.3.11
Junction to ambient	$R_{thJA}$	–	26	–	K/W	<sup>1)2)</sup> 2s2p board	P_3.3.12
Junction to ambient	$R_{thJA}$	–	101	–	K/W	<sup>1)3)</sup> 1s0p board, footprint only	P_3.3.13
Junction to ambient	$R_{thJA}$	–	48	–	K/W	<sup>1)3)</sup> 1s0p board, 300 mm <sup>2</sup> heatsink area on PCB	P_3.3.14
Junction to ambient	$R_{thJA}$	–	39	–	K/W	<sup>1)3)</sup> 1s0p board, 600 mm <sup>2</sup> heatsink area on PCB	P_3.3.15

- 1) Not subject to production test, specified by design.
- 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
- 3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 1 copper layer (1 × 70 μm Cu).



## **4 Block description and electrical characteristics**

### **4.1 Voltage regulation**

The output voltage  $V_O$  is divided by a resistor network. The TLS850C2TEV33 compares this fractional voltage to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the following factors:

- output capacitor  $C_O$
- load current
- chip temperature
- internal circuit design

#### **Output capacitor**

To ensure stable operation, the capacitance of the output capacitor and its equivalent series resistor (ESR) requirements as specified in **“Functional range” on Page 7** must be maintained. The output capacitor must be sized according to the requirements of the application to be able to buffer load steps.

#### **Input capacitors, reverse polarity protection diode**

An input capacitor  $C_I$  is recommended to compensate for line influences.

In order to block influences such as pulses and high frequency distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

#### **Smooth ramp-up**

In order to prevent overshoots during startup, a smooth ramp-up function is implemented. This ensures a reduced output voltage overshoot during startup, mostly independent from load and output capacitance.

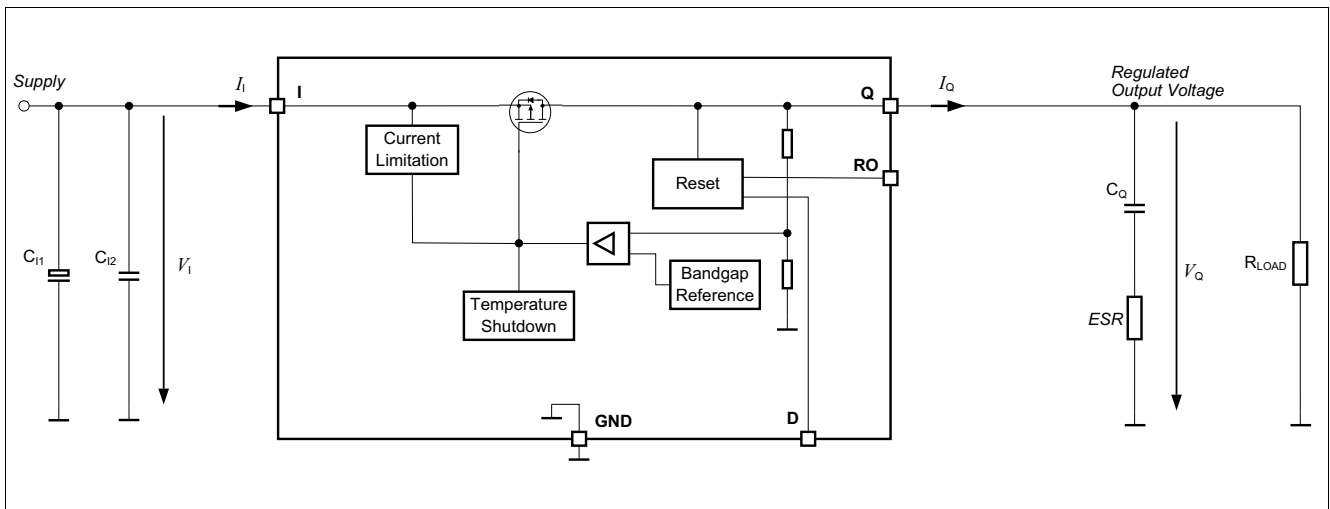
#### **Output current limitation**

If the load current exceeds the specified limit, due to a short-circuit for example, then the device limits the output current and the output voltage decreases.

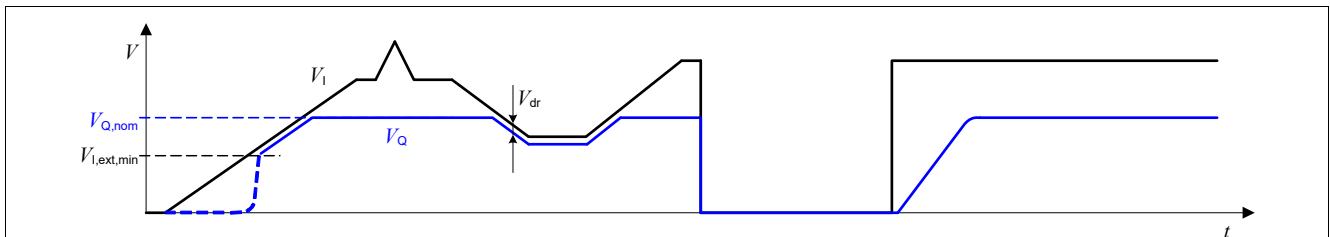
#### **Overtemperature shutdown**

The overtemperature shutdown circuit prevents the device from immediate destruction in case of a fault condition, for example due to a permanent short-circuit at the output, by switching off the power stage. After the device has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the device.

**Block description and electrical characteristics**



**Figure 3 Voltage regulation**



**Figure 4 Output voltage versus input voltage**

**Block description and electrical characteristics**

**Table 4 Electrical characteristics voltage regulator**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified)  
 Typical values are given at  $T_j = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage accuracy	$V_Q$	3.23	3.3	3.37	V	$0.05\text{ mA} \leq I_Q \leq 500\text{ mA}$ $4.6\text{ V} \leq V_I \leq 28\text{ V}$	P_4.1.13
Output voltage accuracy	$V_Q$	3.23	3.3	3.37	V	$0.05\text{ mA} \leq I_Q \leq 250\text{ mA}$ $3.97\text{ V} \leq V_I \leq 40\text{ V}$	P_4.1.14
Dropout voltage $V_{dr} = V_I - V_Q$	$V_{dr}$	–	300	600	mV	<sup>1)</sup> $I_Q = 250\text{ mA}$	P_4.1.20
Dropout voltage $V_{dr} = V_I - V_Q$	$V_{dr}$	–	120	240	mV	<sup>1)</sup> $I_Q = 100\text{ mA}$	P_4.1.22
Power Supply Ripple Rejection	$PSRR$	–	63	–	dB	<sup>2)</sup> $f_{\text{ripple}} = 100\text{ Hz}$ $V_{\text{ripple}} = 0.5 V_{pp}$ $I_Q = 10\text{ mA}$	P_4.1.23

**Other electrical characteristics**

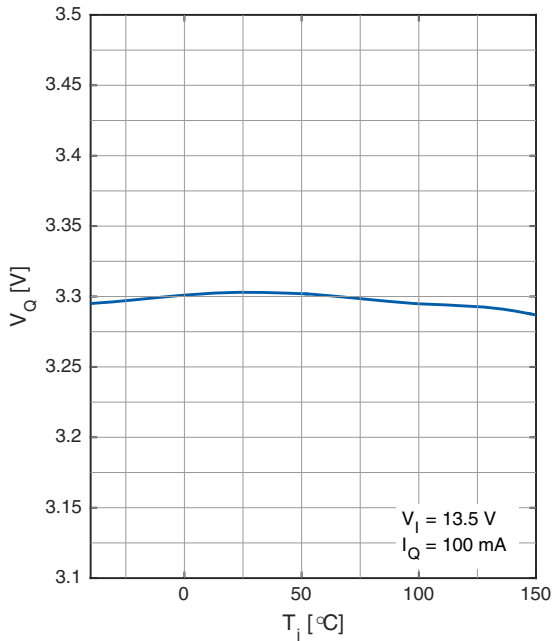
Output current limitation	$I_{Q,max}$	501	750	1100	mA	$0\text{ V} < V_Q < V_{Q,nom} - 0.1\text{ V}$	P_4.1.27
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-5	–	mV	$I_Q = 0.05\text{ mA}$ to $500\text{ mA}$ $V_I = 6.5\text{ V}$	P_4.1.31
Line regulation steady-state	$\Delta V_{Q,line}$	–	1	10	mV	$V_I = 8\text{ V}$ to $32\text{ V}$ $I_Q = 5\text{ mA}$	P_4.1.32
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	$^\circ\text{C}$	<sup>2)</sup> $T_j$ increasing	P_4.1.33
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	<sup>2)</sup> $T_j$ decreasing	P_4.1.34

1) Measured when the output voltage  $V_Q$  has dropped by 100 mV while input voltage was gradually decreased.

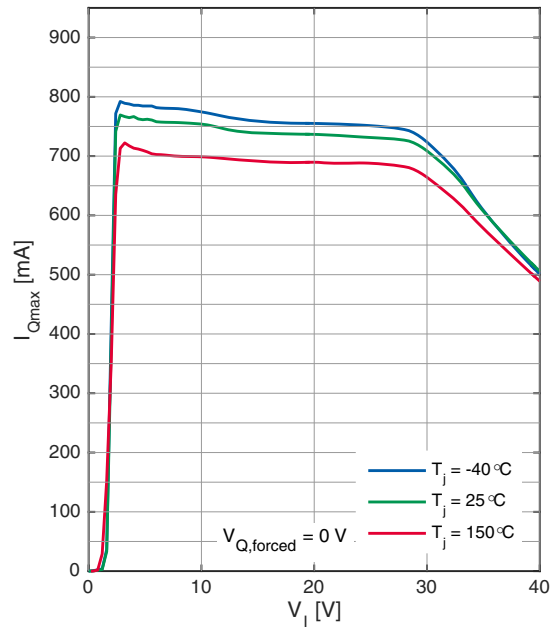
2) Not subject to production test, specified by design.

**4.2 Typical performance characteristics voltage regulator**

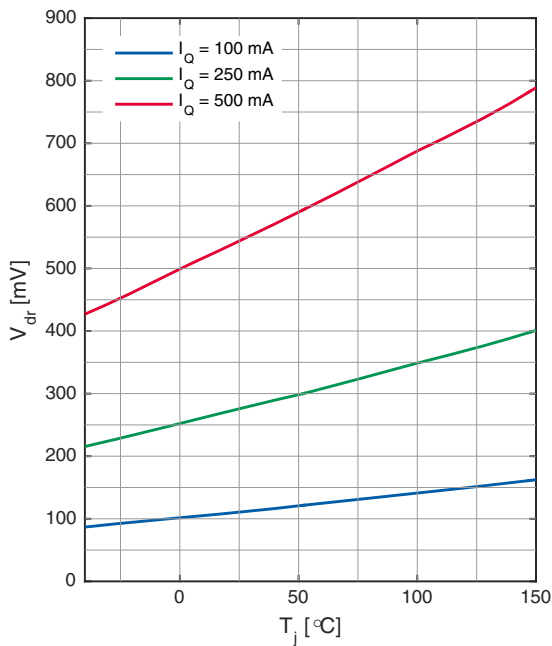
**Output voltage  $V_Q$  versus junction temperature  $T_j$**



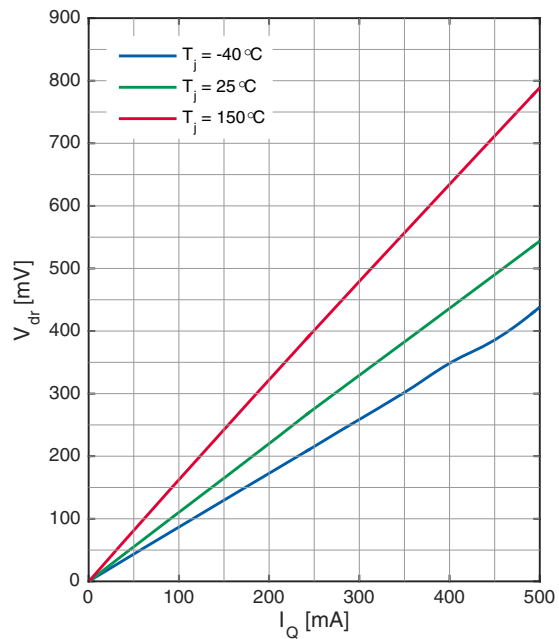
**Maximum output current  $I_{Qmax}$  versus input voltage  $V_i$**



**Dropout voltage  $V_{dr}$  versus junction temperature  $T_j$**

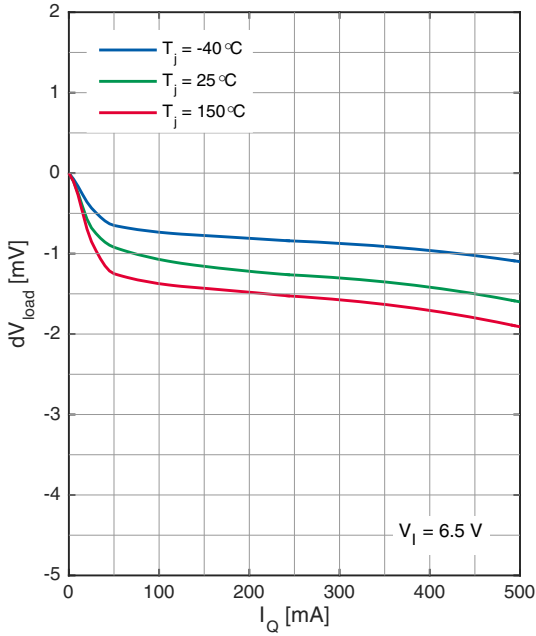


**Dropout voltage  $V_{dr}$  versus Output Current  $I_Q$**

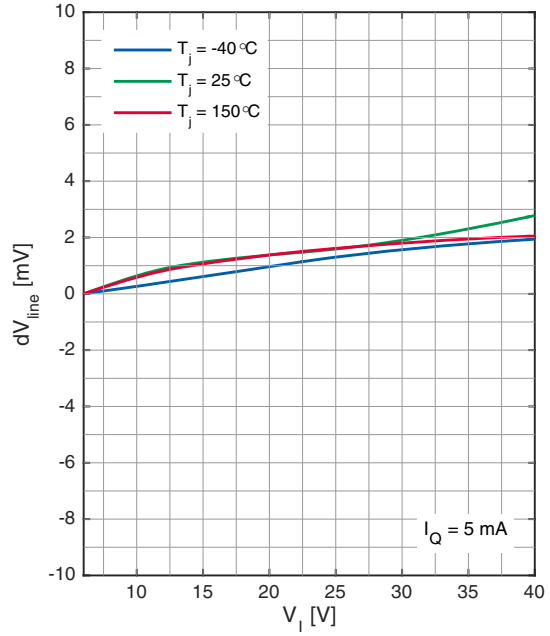


**Block description and electrical characteristics**

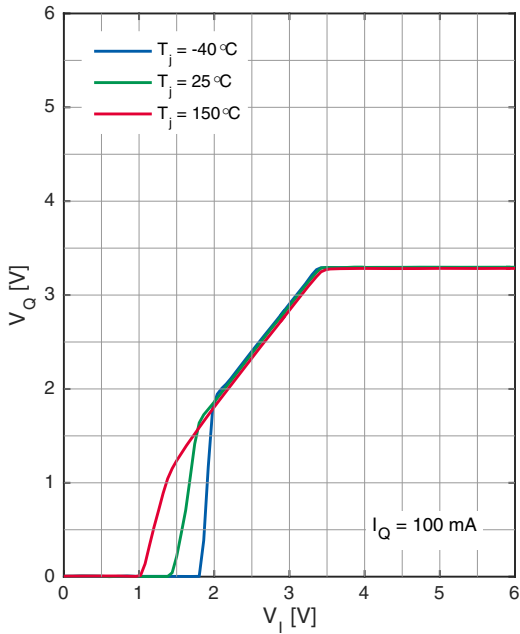
**Load regulation  $\Delta V_{Q,load}$  versus output current change  $I_Q$**



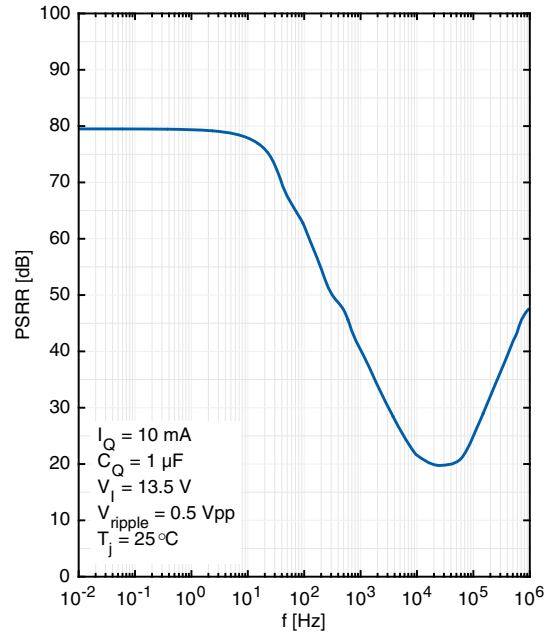
**Line regulation  $\Delta V_{Q,line}$  versus input voltage  $V_I$**



**Output Voltage  $V_Q$  versus Input Voltage  $V_I$**

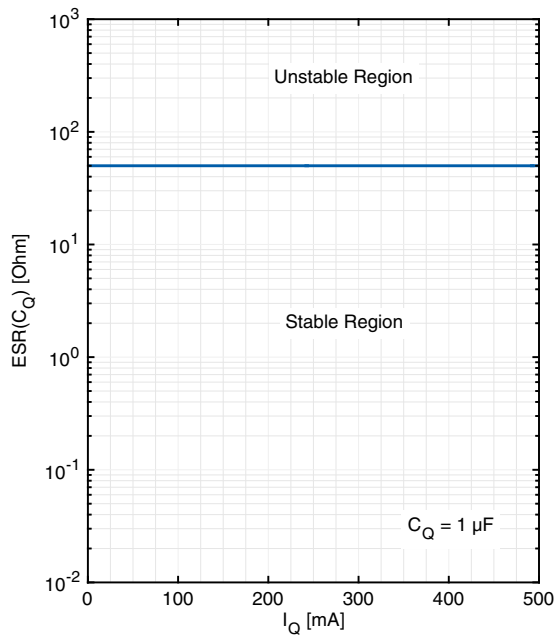


**Power Supply Ripple Rejection  $PSRR$  versus ripple frequency  $f$**



**Block description and electrical characteristics**

**Equivalent Series Resistance of output capacitor**  
 **$ESR(C_Q)$  versus output current  $I_Q$**



**Block description and electrical characteristics**

**4.3 Current consumption**

**Table 5 Electrical characteristics current consumption**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$  (unless otherwise specified)

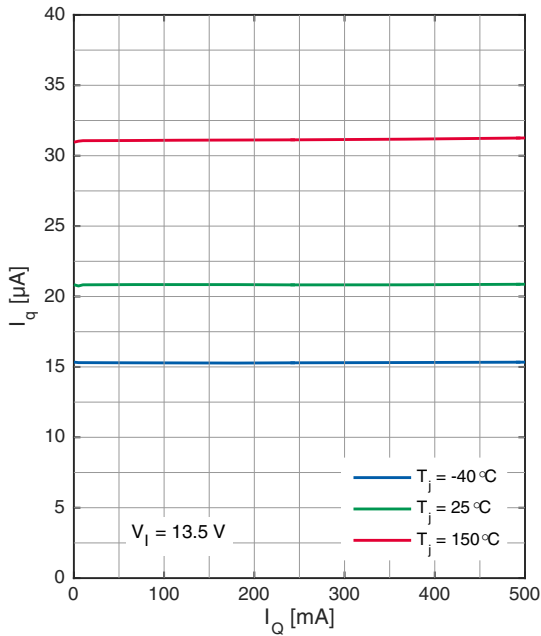
Typical values are given at  $T_j = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I - I_Q$	$I_q$	–	20	30	$\mu\text{A}$	$I_Q = 0.05\text{ mA}$ $T_j = 25^\circ\text{C}$	P_4.5.11
Current consumption $I_q = I_I - I_Q$	$I_q$	–	23	36	$\mu\text{A}$	$I_Q = 0.05\text{ mA}$ $T_j < 125^\circ\text{C}$	P_4.5.12
Current consumption $I_q = I_I - I_Q$	$I_q$	–	25	42	$\mu\text{A}$	<sup>1)</sup> $I_Q = 500\text{ mA}$ $T_j < 125^\circ\text{C}$	P_4.5.13

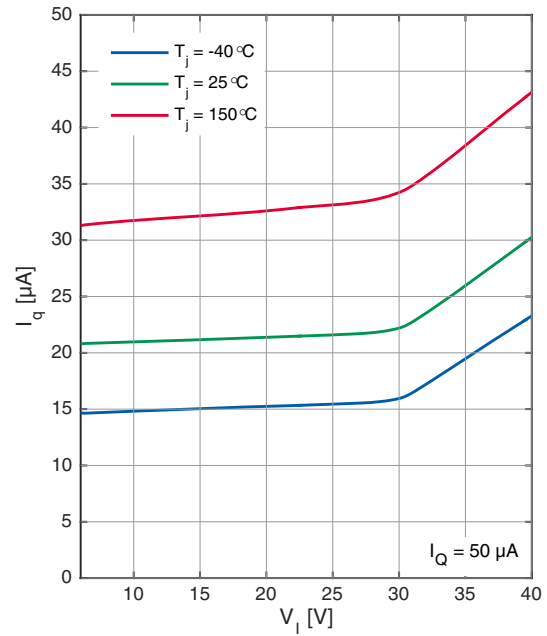
1) Not subject to production test, specified by design.

#### 4.4 Typical performance characteristics current consumption

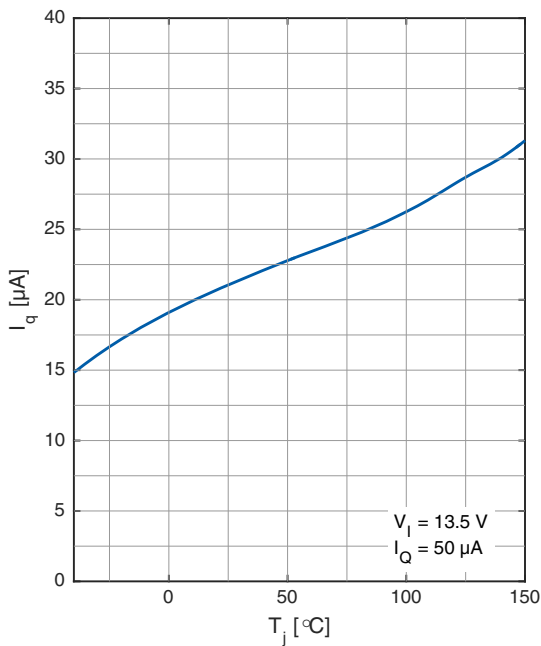
**Current consumption  $I_q$  versus output current  $I_Q$**



**Current consumption  $I_q$  versus input voltage  $V_i$**



**Current consumption  $I_q$  versus junction temperature  $T_j$**





## Block description and electrical characteristics

### 4.5 Reset function

The reset function monitors the output voltage  $V_Q$  and indicates a potential imminent loss of power. This then allows enough time for the system to shut down or do the transition into a safe state. To meet the requirements of the application, some reset parameters can be adjusted by measures described below.

#### Output undervoltage reset

The reset output RO is an open collector stage. It is internally pulled up to  $V_Q$  via a resistor **Reset output internal pull-up resistor** (Table 6). In case of an undervoltage event at  $V_Q$ , RO is pulled to “low”. This signal can then be used to reset a microcontroller during low supply voltage.

#### Optional reset output pull-up resistor $R_{RO,ext}$

Although the reset output RO is an open collector output with an integrated pull-up resistor, an additional external pull-up resistor can be added to the output Q, if needed. Table 6 specifies a minimum value for the external resistor  $R_{RO,ext}$  for this option.

#### Power-on reset delay time

The power-on reset delay time  $t_{rd}$  allows a microcontroller and oscillator to start up. This delay time is the time interval from exceeding the reset switching threshold  $V_{RT,high}$  until the reset is released by switching the reset output RO from “low” to “high”. The power-on reset delay time  $t_{rd}$  is defined by an external delay capacitor  $C_D$  connected to pin D. The delay capacitor charge current  $I_{D,ch}$  charges  $C_D$  by starting from  $V_D = 0$  V.

If the application requires a power-on reset delay time  $t_{rd}$  that differs from the default value specified in Table 6, then the required value of the delay capacitor can be derived from the specified value and the desired power-on delay time as follows:

$$C_D = \frac{t_{rd}}{t_{rd,100\text{ nF}}} \cdot C_{D,100\text{ nF}} \quad (4.1)$$

where

- $C_D$ : required capacitance of the delay capacitor
- $t_{rd}$ : desired power-on reset delay time
- $t_{rd,100\text{ nF}}$ : **Power-on reset delay time** (Table 6) for  $C_D = 100$  nF as specified in the data sheet

For a precise calculation, the tolerance of the delay capacitor must also be considered.

#### Reset reaction time

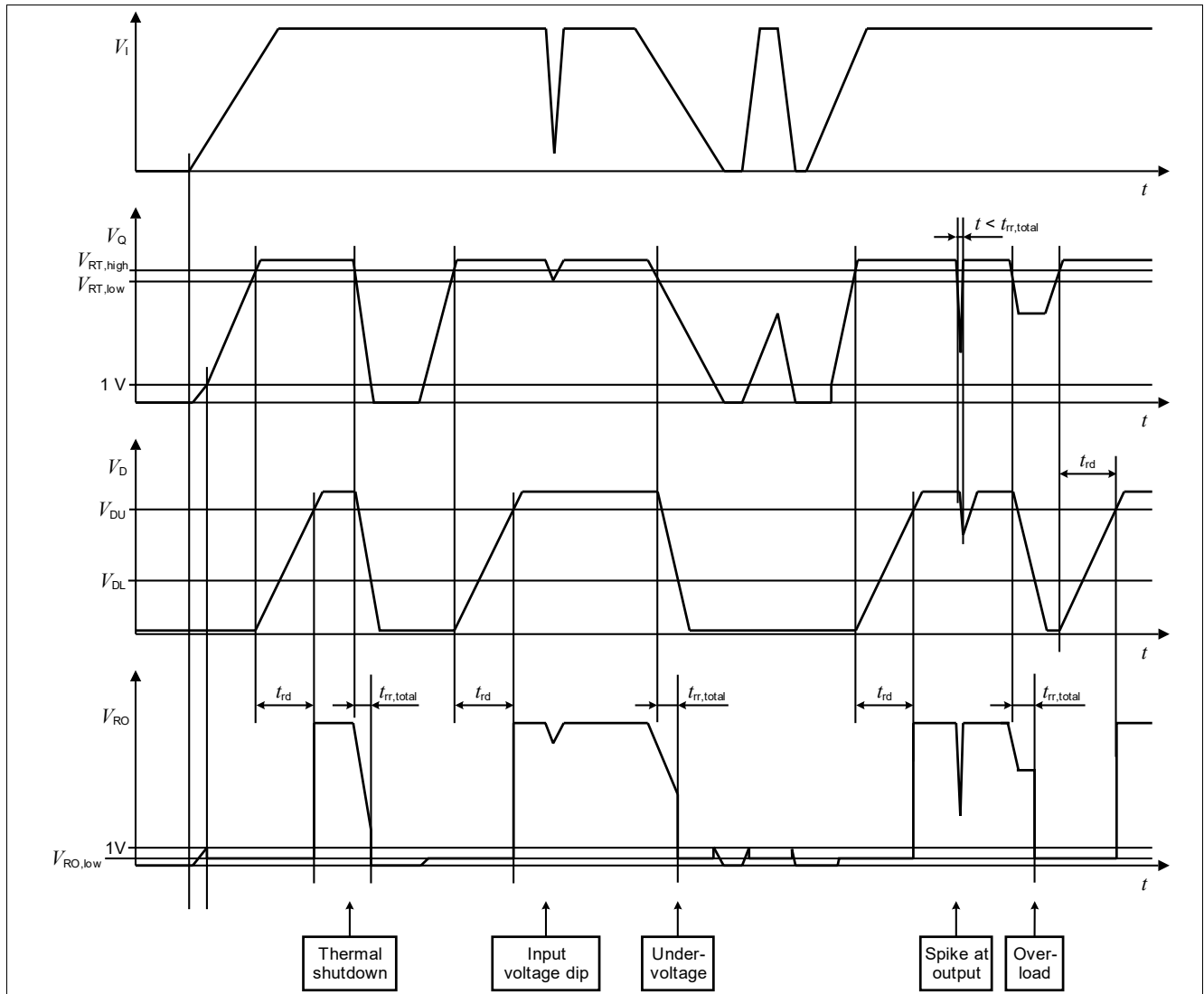
The reset reaction time ensures that short undervoltage spikes do not trigger an unwanted reset “low” signal. The reset reaction time  $t_{rr,total}$  comprises the internal reaction time  $t_{rr,int}$  and the discharge time  $t_{rr,d}$  defined by the external delay capacitor  $C_D$ . Therefore, the total reset reaction time becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \quad (4.2)$$

where

- $t_{rr,total}$ : **Reset reaction time**
- $t_{rr,int}$ : **Internal reset reaction time**
- $t_{rr,d}$ : **Delay capacitor discharge time**

**Block description and electrical characteristics**



**Figure 5 Timing diagram reset**

**Table 6 Electrical characteristics reset**

$T_j = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ,  $V_i = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified).  
 Typical values are given at  $T_j = 25^{\circ}\text{C}$ ,  $V_i = 13.5\text{ V}$ .

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Output undervoltage reset (3.3 V output voltage)</b>							
Output undervoltage reset upper switching threshold	$V_{RT,high}$	3.00	3.10	3.20	V	$V_Q$ increasing,	P_4.14.6
Output undervoltage reset lower switching threshold	$V_{RT,low}$	2.93	3.03	3.13	V	$V_Q$ decreasing,	P_4.14.7
<b>Reset output RO</b>							
Reset output “low” voltage	$V_{RO,low}$	-	0.2	0.4	V	$1\text{ V} \leq V_Q \leq V_{RT}$ ; $R_{RO} > 4.7\text{ k}\Omega$	P_4.14.11

**Block description and electrical characteristics**

**Table 6 Electrical characteristics reset (cont'd)**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified).  
 Typical values are given at  $T_j = 25^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ .

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset output internal pull-up resistor	$R_{RO,int}$	13	20	36	k $\Omega$	internally connected to Q	P_4.14.12
Reset output external pull-up resistor to $V_Q$	$R_{RO,ext}$	4.7	–	–	k $\Omega$	$1\text{ V} \leq V_Q \leq V_{RT}$ ; $V_{RO} \leq 0.4\text{ V}$	P_4.14.13

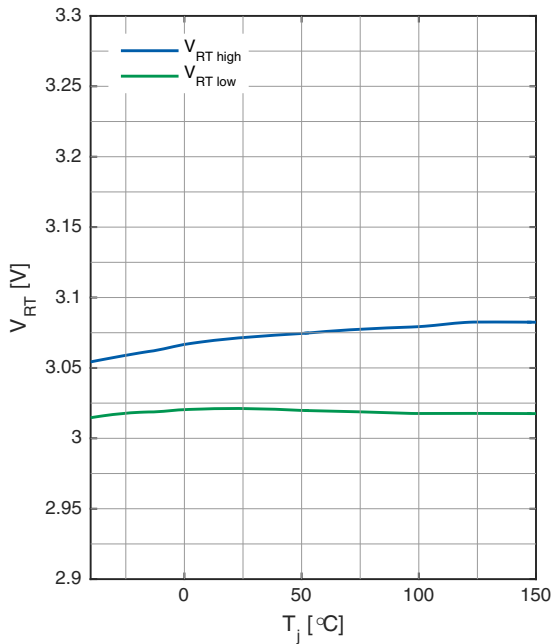
**Reset delay timing**

Power-on reset delay time	$t_{rd}$	17	25	37	ms	$C_D = 100\text{ nF}$ Calculated value	P_4.14.15
Upper delay switching threshold	$V_{DU}$	–	0.9	–	V	–	P_4.14.16
Lower delay switching threshold	$V_{DL}$	–	0.6	–	V	–	P_4.14.17
Delay capacitor charge current	$I_{D,ch}$	–	3.6	–	$\mu\text{A}$	$V_D = 1\text{ V}$	P_4.14.18
Delay capacitor discharge current	$I_{D,dch}$	–	210	–	mA	$V_D = 1\text{ V}$	P_4.14.19
Delay capacitor discharge time	$t_{rr,d}$	–	2	4	$\mu\text{s}$	$C_D = 100\text{ nF}$ Calculated value	P_4.14.20
Internal reset reaction time	$t_{rr,int}$	–	15	44	$\mu\text{s}$	<sup>1)</sup> $C_D = 0\text{ nF}$	P_4.14.21
Reset reaction time	$t_{rr,total}$	–	17	48	$\mu\text{s}$	$C_D = 100\text{ nF}$ Calculated value	P_4.14.22

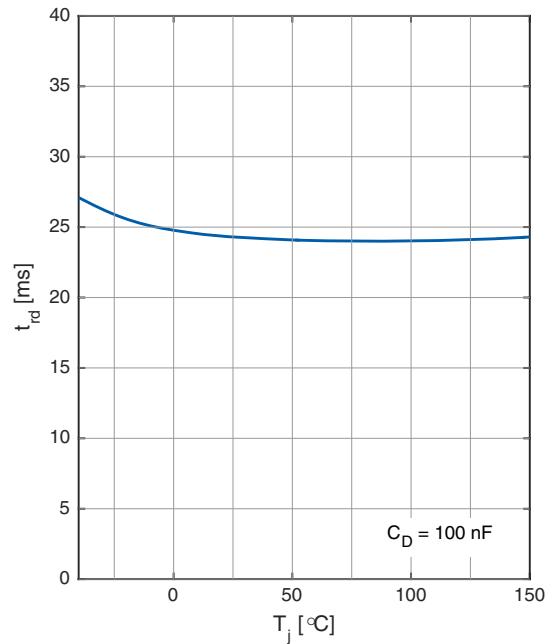
1) Parameter not subject to production test; specified by design.

### 4.6 Typical performance characteristics reset

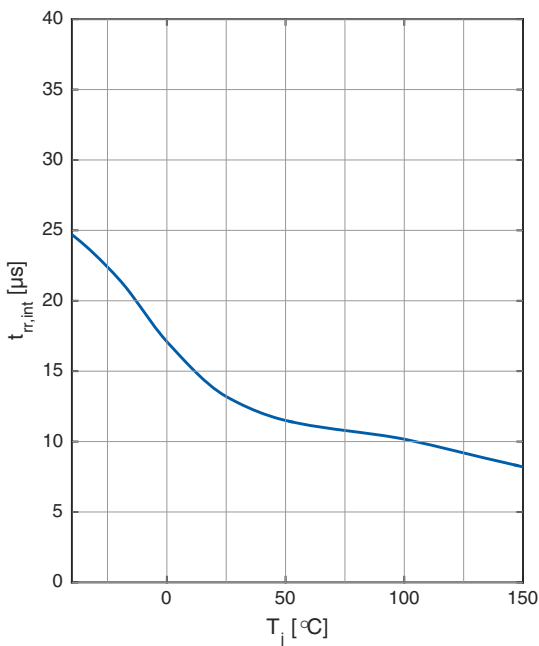
**Undervoltage reset threshold  $V_{RT}$  versus junction temperature  $T_j$**



**Power-on reset delay time  $t_{rd}$  versus junction temperature  $T_j$**



**Internal Reset reaction time  $t_{rr,int}$  versus junction temperature  $T_j$**

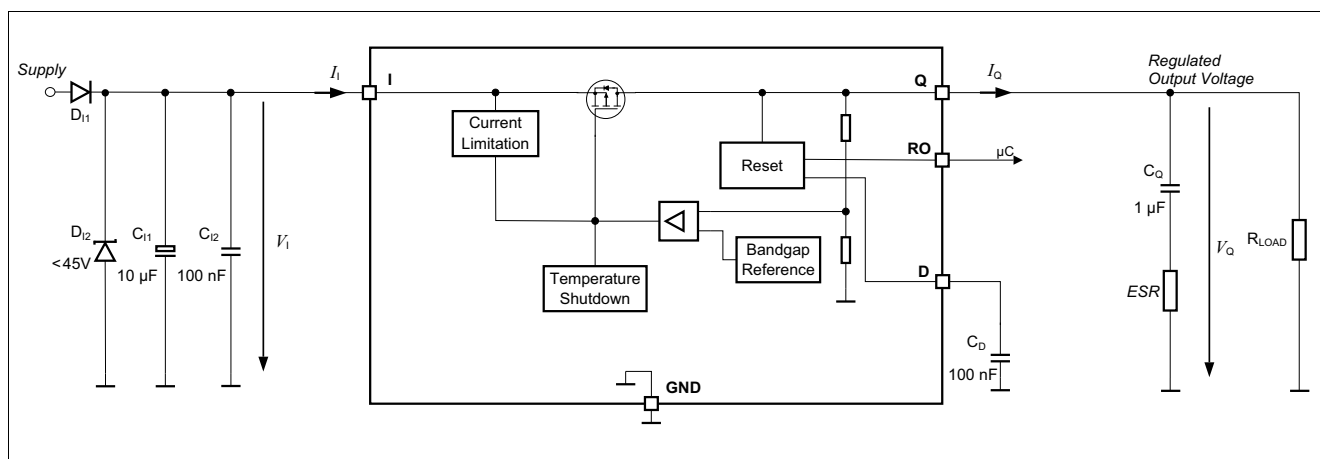


**Application information**

## 5 Application information

### 5.1 Application diagram

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 6 Application diagram**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

### 5.2 Selection of external components

#### 5.2.1 Input pin

**Figure 6** shows an example of the input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 μF to 470 μF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended to deal with possible external disturbances.

#### 5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators. Furthermore it serves as an energy buffer during load jumps, to compensate and maintain a constant output voltage potential. It must be dimensioned according to the specific requirements of the application. The requirements for the output capacitor are given in **“Functional range” on Page 7**.

## Application information

The TLS850C2TEV33 is designed to be stable with low ESR capacitors as well. According to automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin and on the same side of the PCB as the regulator itself.

In case of transients of input voltage or of load current, the capacitance should be dimensioned accordingly. The configuration must be verified in the real application to ensure that the output stability requirements are fulfilled.

### 5.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated as follow:

$$P_D = (V_I - V_Q)I_Q + V_I I_q \quad (5.1)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  is given by:

$$R_{thJA} = \frac{T_{j,max} - T_a}{P_D} \quad (5.2)$$

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined by referencing to the specification for **“Thermal resistance” on Page 8**.

### 5.4 Reverse polarity protection

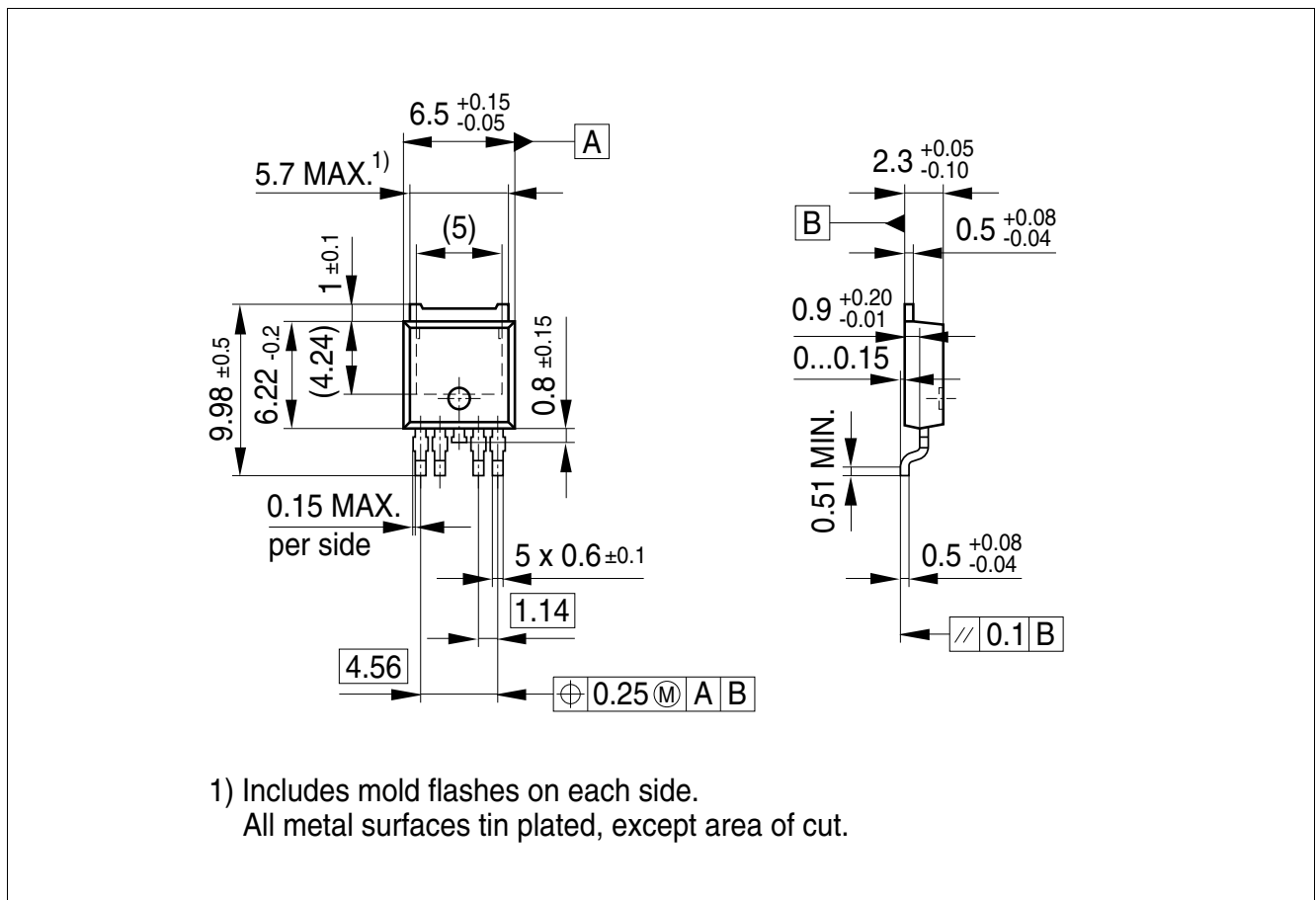
The TLS850C2TEV33 is not protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is necessary. The absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 6** must be maintained.

### 5.5 Further application information

For further information you may contact <http://www.infineon.com/>

**Package information**

**6 Package information**



**Figure 7 PG-T0252-5<sup>1)</sup>**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Further information on packages**

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2020-01-31	Initial version



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[AZ1117ID-ADJTRG1](#) [TCR3DG12,LF](#) [MIC5514-3.3YMT-T5](#) [MIC5512-1.2YMT-T5](#) [MIC5317-2.8YM5-T5](#) [SCD7912BTG](#)  
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