

# XMC1300 AB-Step

Microcontroller Series  
for Industrial Applications

XMC1000 Family

ARM<sup>®</sup> Cortex<sup>®</sup>-M0  
32-bit processor core

Data Sheet

V2.0 2017-10

Microcontrollers

**Edition 2017-10**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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## **XMC1300 Data Sheet**

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### **Revision History: V2.0 2017-10**

Previous Version: V1.9 2017-03

Page	Subjects
<b>Page 10,</b> <b>Page 13</b>	Add marking option for XMC1302-T28X0032, XMC1302-T28X0064, XMC1302-T28X0128, XMC1302-T28X0200.

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## **About this Document**

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

### **XMC1000 Family User Documentation**

The set of user documentation includes:

- **Reference Manual**
  - describes the functionality of the superset of devices.
- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

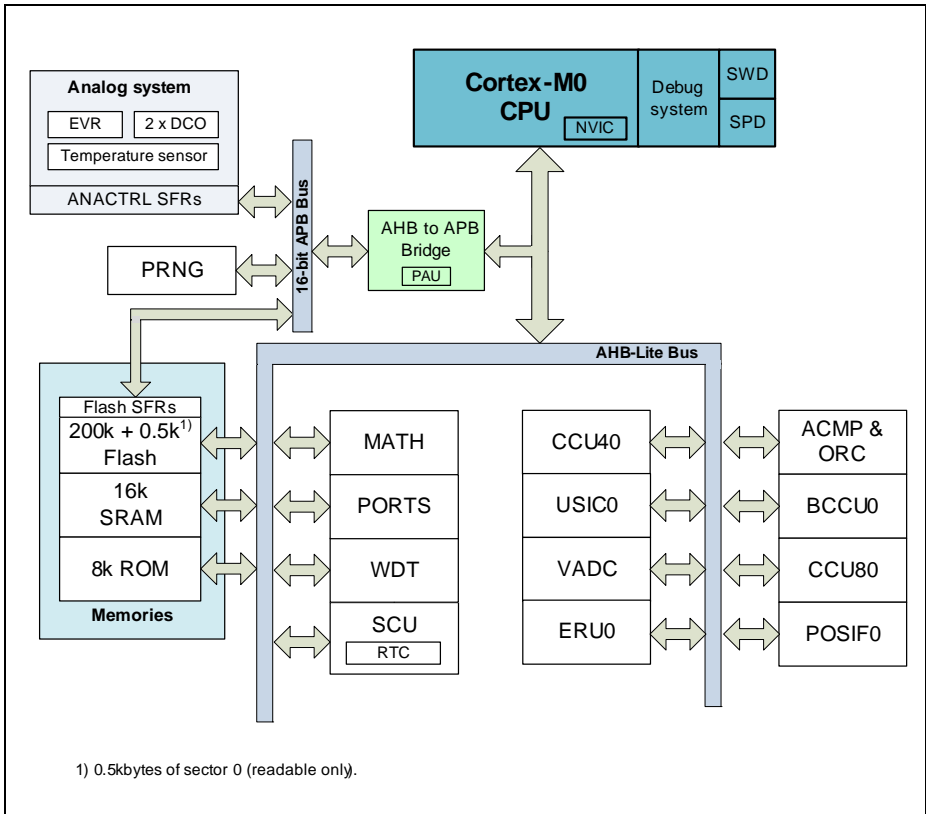
***Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.***

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

# 1 Summary of Features

The XMC1300 devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1300 series addresses the real-time control needs of motor control, digital power conversion. It also features peripherals for LED Lighting applications.



**Figure 1 System Block Diagram**

## CPU Subsystem

- CPU Core
  - High-performance 32-bit ARM Cortex-M0 CPU
  - Most 16-bit Thumb and subset of 32-bit Thumb2 instruction set
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support



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**Summary of Features**

- Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for processing of external and internal service requests
- MATH Co-processor (MATH)
  - CORDIC unit for trigonometric calculation
  - division unit

**On-Chip Memories**

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

**Communication Peripherals**

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces

**Analog Frontend Peripherals**

- A/D Converters
  - up to 12 analog input pins
  - 2 sample and hold stages with 8 analog input channels each
  - fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

**Industrial Control Peripherals**

- Capture/Compare Units 4 (CCU4) as general purpose timers
- Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Position Interfaces (POSIF) for hall and quadrature encoders and motor positioning
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

**System Control**

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG) for fast random data generation

**Input/Output Lines**

- Tri-stated in input mode
- Push/pull or open drain output mode

- Configurable pad hysteresis

### **On-Chip Debug Support**

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

## **1.1 Ordering Information**

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

## **1.2 Device Types**

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

**Table 1 Synopsis of XMC1300 Device Types**

<b>Derivative</b>	<b>Package</b>	<b>Flash Kbytes</b>	<b>SRAM Kbytes</b>
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16
XMC1301-T016F0032	PG-TSSOP-16-8	32	16
XMC1301-T016X0008	PG-TSSOP-16-8	8	16
XMC1301-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0008	PG-TSSOP-16-8	8	16

**Summary of Features**
**Table 1 Synopsis of XMC1300 Device Types (cont'd)**

<b>Derivative</b>	<b>Package</b>	<b>Flash Kbytes</b>	<b>SRAM Kbytes</b>
XMC1302-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0032	PG-TSSOP-16-8	32	16
XMC1302-T028X0016	PG-TSSOP-28-8	16	16
XMC1302-T028X0032	PG-TSSOP-28-8	32	16
XMC1302-T028X0064	PG-TSSOP-28-8	64	16
XMC1302-T028X0128	PG-TSSOP-28-8	128	16
XMC1302-T028X0200	PG-TSSOP-28-8	200	16
XMC1301-T038F0008	PG-TSSOP-38-9	8	16
XMC1301-T038F0016	PG-TSSOP-38-9	16	16
XMC1301-T038F0032	PG-TSSOP-38-9	32	16
XMC1301-T038X0032	PG-TSSOP-38-9	32	16
XMC1301-T038F0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0016	PG-TSSOP-38-9	16	16
XMC1302-T038X0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0128	PG-TSSOP-38-9	128	16
XMC1302-T038X0200	PG-TSSOP-38-9	200	16
XMC1301-Q024F0008	PG-VQFN-24-19	8	16
XMC1301-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0032	PG-VQFN-24-19	32	16
XMC1302-Q024F0064	PG-VQFN-24-19	64	16
XMC1302-Q024X0016	PG-VQFN-24-19	16	16
XMC1302-Q024X0032	PG-VQFN-24-19	32	16
XMC1302-Q024X0064	PG-VQFN-24-19	64	16
XMC1301-Q040F0008	PG-VQFN-40-13	8	16
XMC1301-Q040F0016	PG-VQFN-40-13	16	16
XMC1301-Q040F0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0016	PG-VQFN-40-13	16	16
XMC1302-Q040X0032	PG-VQFN-40-13	32	16

**Summary of Features**

**Table 1 Synopsis of XMC1300 Device Types (cont'd)**

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1302-Q040X0064	PG-VQFN-40-13	64	16
XMC1302-Q040X0128	PG-VQFN-40-13	128	16
XMC1302-Q040X0200	PG-VQFN-40-13	200	16

### 1.3 Device Type Features

The following table lists the available features per device type.

**Table 2 Features of XMC1300 Device Types<sup>1)</sup>**

Derivative	ADC channel	ACMP	BCCU	MATH
XMC1301-T016	11	2	-	-
XMC1302-T016	11	2	1	1
XMC1302-T028	14	3	1	1
XMC1301-T038	16	3	-	-
XMC1302-T038	16	3	1	1
XMC1301-Q024	13	3	-	-
XMC1302-Q024	13	3	1	1
XMC1301-Q040	16	3	-	-
XMC1302-Q040	16	3	1	1

1) Features that are not included in this table are available in all the derivatives

**Table 3 ADC Channels<sup>1)</sup>**

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	CH0..CH4
PG-TSSOP-28	CH0..CH7	CH0 .. CH4, CH7
PG-TSSOP-38	CH0..CH7	CH0..CH7
PG-VQFN-24	CH0..CH7	CH0..CH4
PG-VQFN-40	CH0..CH7	CH0..CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

## 1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00<sub>H</sub> (MSB) - 1000 0F1B<sub>H</sub> (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

**Table 4 XMC1300 Chip Identification Number**

<b>Derivative</b>	<b>Value</b>	<b>Marking</b>
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 <sub>H</sub>	AB
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1301-T016F0032	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 <sub>H</sub>	AB
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00003000 201ED083 <sub>H</sub>	AB
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-T028X0016	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-T028X0032	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-T028X0064	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 <sub>H</sub>	AB
XMC1302-T028X0128	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 201ED083 <sub>H</sub>	AB
XMC1302-T028X0200	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 201ED083 <sub>H</sub>	AB
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 <sub>H</sub>	AB

**Summary of Features**

**Table 4 XMC1300 Chip Identification Number (cont'd)**

<b>Derivative</b>	<b>Value</b>	<b>Marking</b>
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1301-T038X0032	00013013 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1301-T038F0064	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00011000 201ED083 <sub>H</sub>	AB
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 <sub>H</sub>	AB
XMC1302-T038X0128	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 201ED083 <sub>H</sub>	AB
XMC1302-T038X0200	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 201ED083 <sub>H</sub>	AB
XMC1301-Q024F0008	00013062 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 <sub>H</sub>	AB
XMC1301-Q024F0016	00013062 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-Q024F0016	00013062 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-Q024F0032	00013062 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-Q024F0064	00013062 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 <sub>H</sub>	AB
XMC1302-Q024X0016	00013063 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-Q024X0032	00013063 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-Q024X0064	00013063 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 <sub>H</sub>	AB

**Summary of Features**

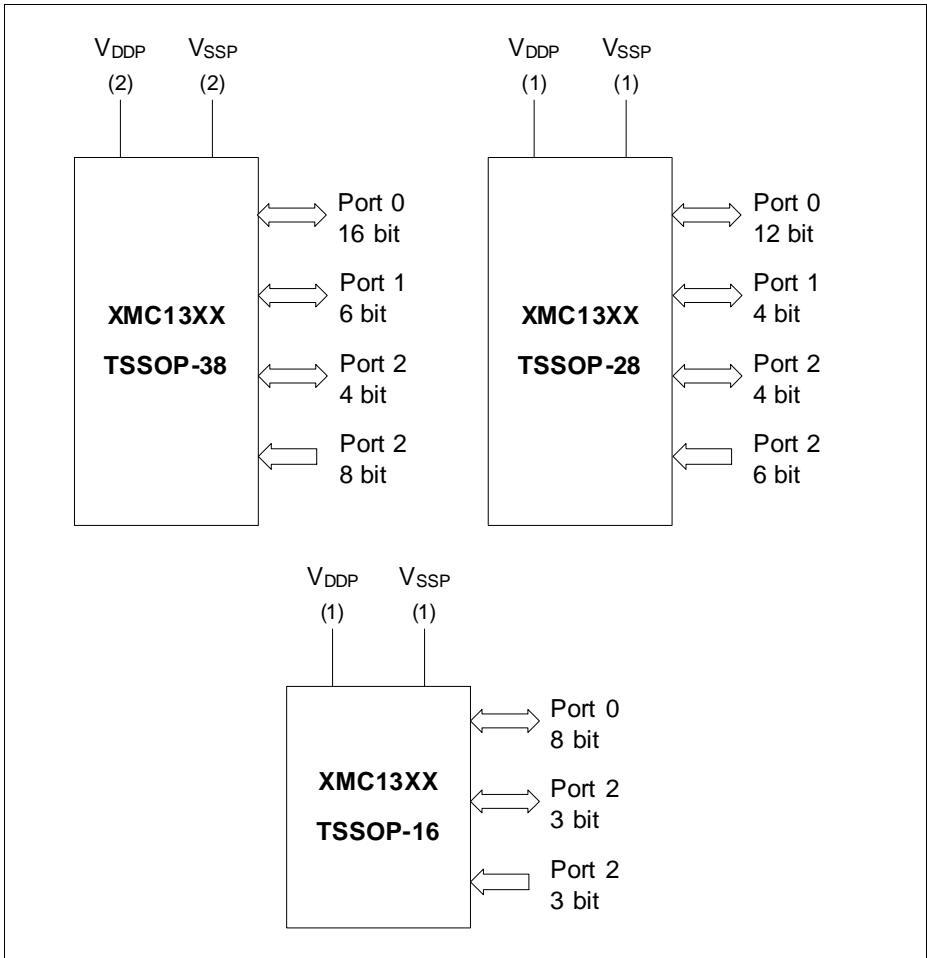
**Table 4 XMC1300 Chip Identification Number (cont'd)**

<b>Derivative</b>	<b>Value</b>	<b>Marking</b>
XMC1301-Q040F0008	00013042 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 <sub>H</sub>	AB
XMC1301-Q040F0016	00013042 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1301-Q040F0032	00013042 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-Q040X0016	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 <sub>H</sub>	AB
XMC1302-Q040X0032	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 <sub>H</sub>	AB
XMC1302-Q040X0064	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 <sub>H</sub>	AB
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 201ED083 <sub>H</sub>	AB
XMC1302-Q040X0200	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 201ED083 <sub>H</sub>	AB

## 2 General Device Information

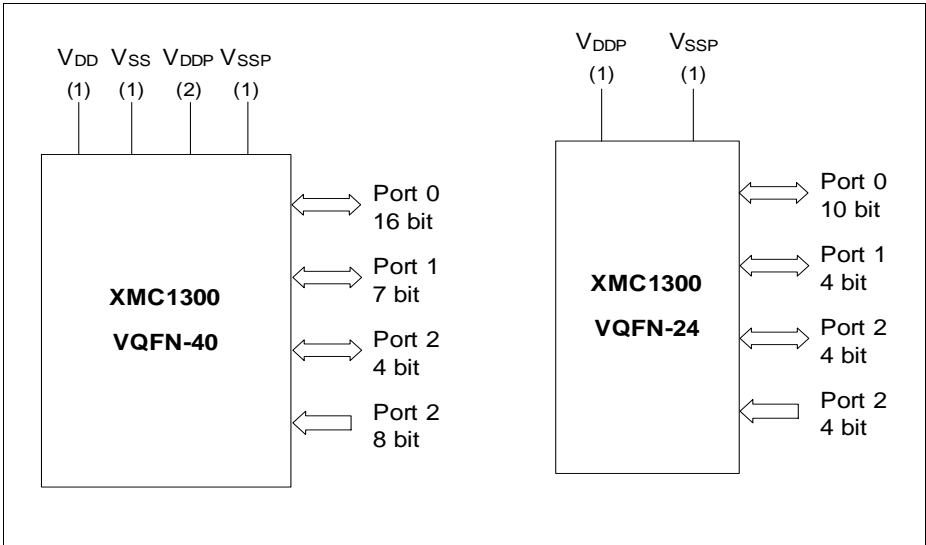
This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

### 2.1 Logic Symbols



**Figure 2 XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16**





**Figure 3 XMC1300 Logic Symbol for VQFN-24 and VQFN-40**

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

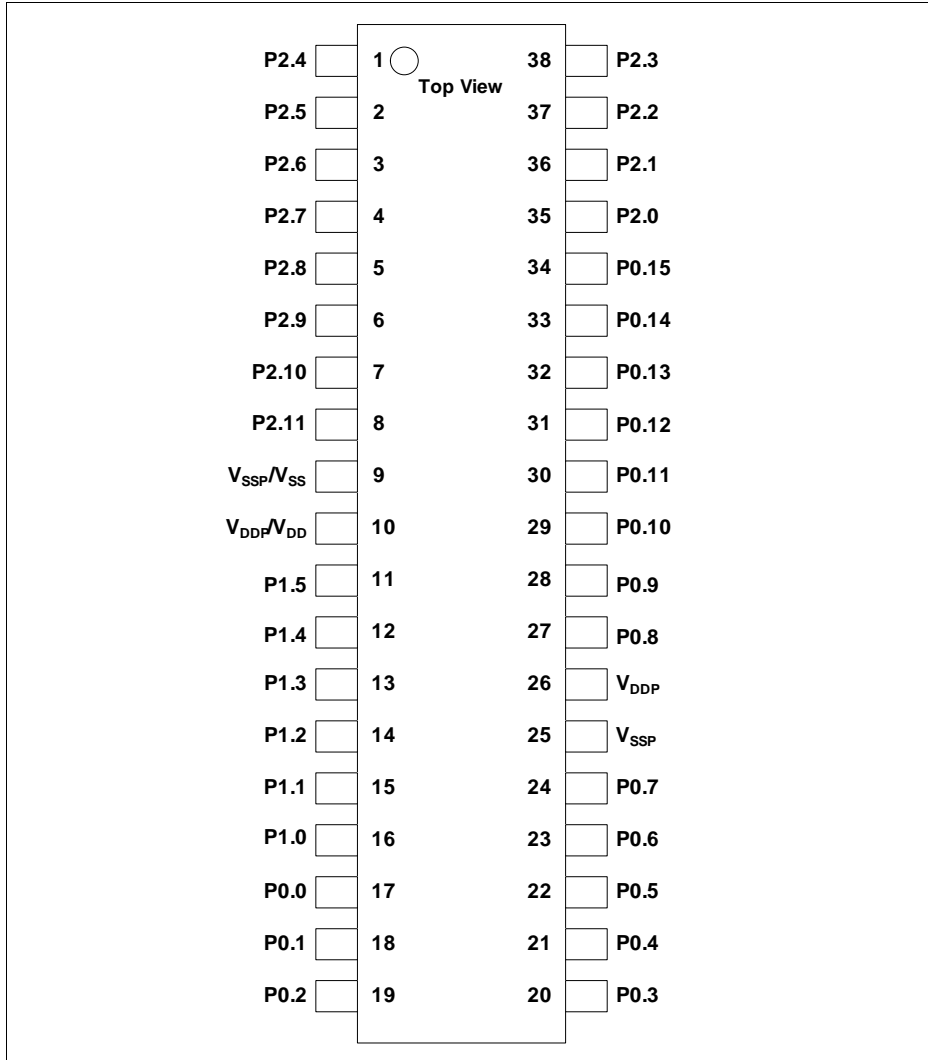


Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

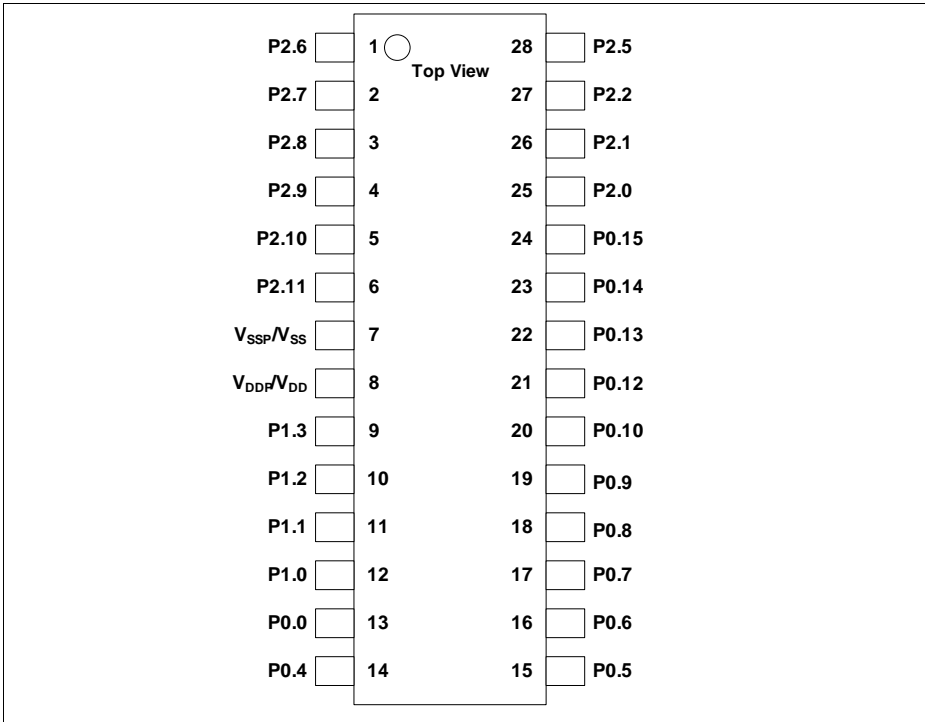


Figure 5 XMC1300 PG-TSSOP-28 Pin Configuration (top view)

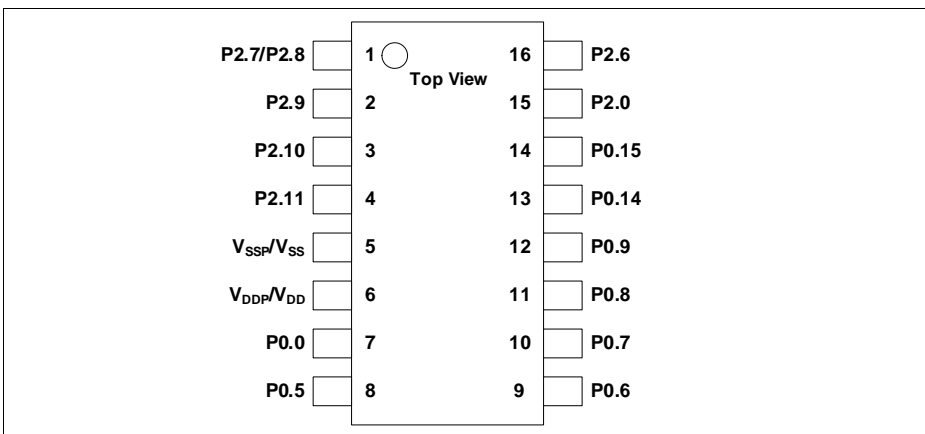
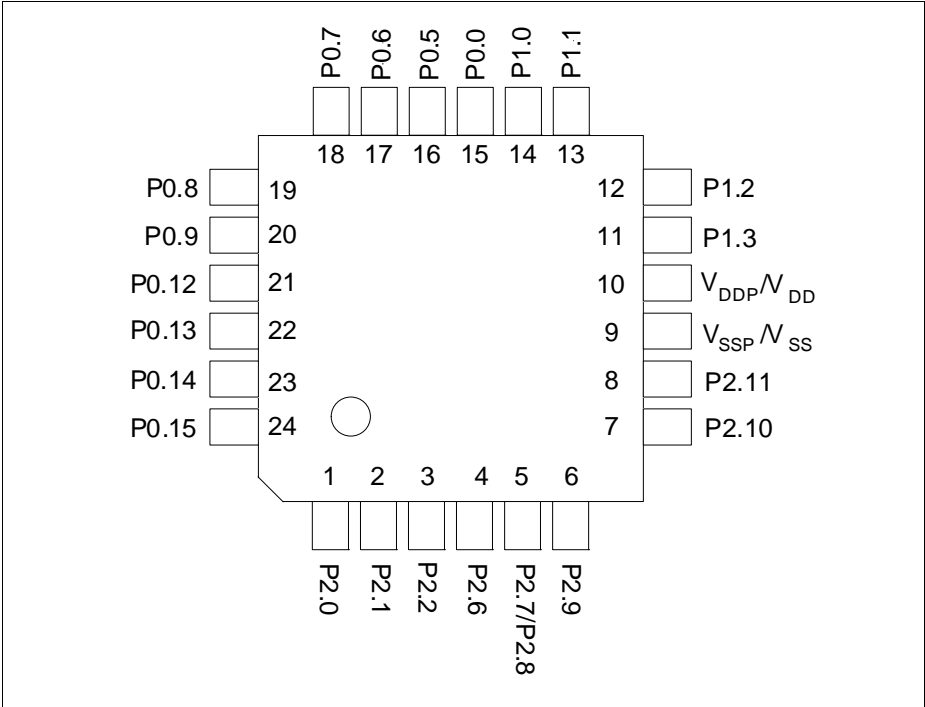
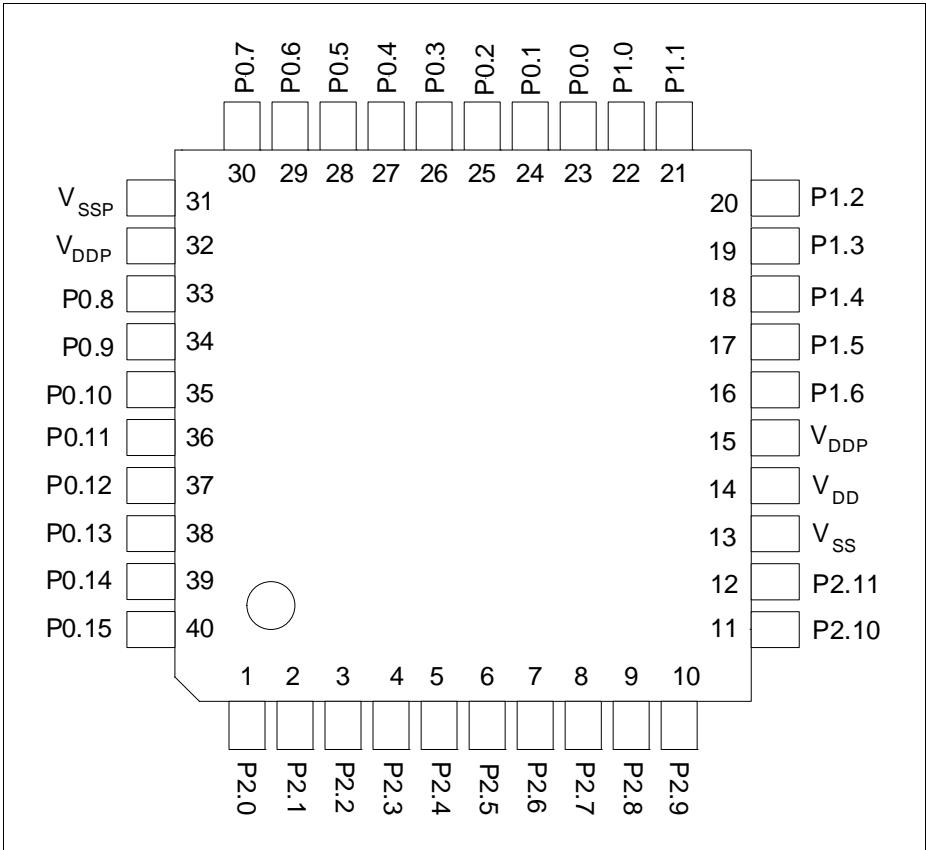


Figure 6 XMC1300 PG-TSSOP-16 Pin Configuration (top view)



**Figure 7 XMC1300 PG-VQFN-24 Pin Configuration (top view)**



**Figure 8 XMC1300 PG-VQFN-40 Pin Configuration (top view)**

### 2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

**Table 5 Package Pin Mapping Description**

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD\_INOUT(standard bi-directional pads)
- STD\_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD\_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

**Table 6 Package Pin Mapping**

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_IN OUT	
P0.1	24	18	-	-	-	STD_IN OUT	
P0.2	25	19	-	-	-	STD_IN OUT	
P0.3	26	20	-	-	-	STD_IN OUT	
P0.4	27	21	14	-	-	STD_IN OUT	
P0.5	28	22	15	16	8	STD_IN OUT	
P0.6	29	23	16	17	9	STD_IN OUT	

**General Device Information**

**Table 6 Package Pin Mapping (cont'd)**

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.7	30	24	17	18	10	STD_IN OUT	
P0.8	33	27	18	19	11	STD_IN OUT	
P0.9	34	28	19	20	12	STD_IN OUT	
P0.10	35	29	20	-	-	STD_IN OUT	
P0.11	36	30	-	-	-	STD_IN OUT	
P0.12	37	31	21	21	-	STD_IN OUT	
P0.13	38	32	22	22	-	STD_IN OUT	
P0.14	39	33	23	23	13	STD_IN OUT	
P0.15	40	34	24	24	14	STD_IN OUT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_IN OUT	
P2.0	1	35	25	1	15	STD_IN OUT/AN	

**General Device Information**
**Table 6 Package Pin Mapping (cont'd)**

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P2.1	2	36	26	2	-	STD_IN OUT/AN	
P2.2	3	37	27	3	-	STD_IN/ AN	
P2.3	4	38	-	-	-	STD_IN/ AN	
P2.4	5	1	-	-	-	STD_IN/ AN	
P2.5	6	2	28	-	-	STD_IN/ AN	
P2.6	7	3	1	4	16	STD_IN/ AN	
P2.7	8	4	2	5	1	STD_IN/ AN	
P2.8	9	5	3	5	1	STD_IN/ AN	
P2.9	10	6	4	6	2	STD_IN/ AN	
P2.10	11	7	5	7	3	STD_IN OUT/AN	
P2.11	12	8	6	8	4	STD_IN OUT/AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	8	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	10	8	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.



**General Device Information**

**Table 6 Package Pin Mapping (cont'd)**

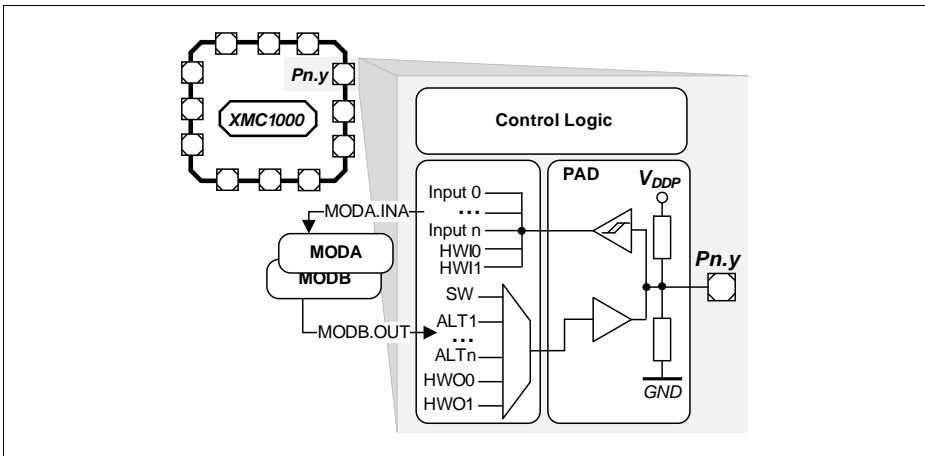
Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	<b>Exposed Die Pad</b> The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

### 2.2.2 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

**Table 7 Port I/O Function Description**

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB



**Figure 9 Simplified Port Structure**

$Pn.y$  is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via  $Pn\_IN.y$ ,  $Pn\_OUT$  defines the output value.

Up to seven alternate output functions ( $ALT1/2/3/4/5/6/7$ ) can be mapped to a single port pin, selected by  $Pn\_IOCR.PC$ . The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the [Port I/O Functions](#) table for the complete Port I/O function mapping.

### 2.2.3 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

**Table 8 Hardware Controlled I/O Function Description**

Function	Outputs	Inputs	Pull Control	
	HWO0	HWI0	HW0_PD	HW0_PU
P0.0	MODB.OUT	MODB.INA		
Pn.y			MODC.OUT	MODC.OUT

By Pn\_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0\_PD/HW1\_PD and HW0\_PU/HW1\_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the [Hardware Controlled I/O Functions](#) table for the complete hardware I/O and pull control function mapping.

**Table 2-1 Port I/O Functions**

Function	Outputs						Inputs						
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOJT0		ERU0. GOUT0	CCU40. OUT0	CCU80. OUT00	USIC0_C H0.SELO 0	USIC0_C H1.SELO 0	BCCU0. TRAPINB	CCU40. IN0C	CCU40. IN1C	USIC0_C H0.DX2A	USIC0_C H1.DX2A	
P0.1	ERU0. PDOJT1	ERU0. GOUT1	ERU0. GOUT2	CCU40. OUT1	CCU80. OUT01	BCCU0. OUT8	SCU. VDR0P		CCU40. IN1C				
P0.2	ERU0. PDOJT2	ERU0. GOUT2	ERU0. GOUT2	CCU40. OUT2	CCU80. OUT02	VADCO. EMUX02	CCU80. OUT10	CCU40. IN2C	CCU40. IN2C				
P0.3	ERU0. PDOJT3	ERU0. GOUT3	ERU0. GOUT3	CCU40. OUT3	CCU80. OUT03	VADCO. EMUX01	CCU80. OUT11	CCU40. IN3C	CCU40. IN3C				
P0.4	BCCU0. OUT0			CCU40. OUT1	CCU80. OUT13	VADCO. EMUX00	WWDT. SERVICE _OUT	CCU80. IN0B	CCU80. IN0B				
P0.5	BCCU0. OUT1			CCU40. OUT0	CCU80. OUT12	ACMP2. OUT	CCU80. OUT01	CCU80. IN1B	CCU80. IN1B				
P0.6	BCCU0. OUT2			CCU40. OUT0	CCU80. OUT11	USIC0_C H1.MCLK H1.DOUT OUT	USIC0_C H1.DOUT 0	CCU40. IN0B	CCU40. IN0B	USIC0_C H1.DX0C			
P0.7	BCCU0. OUT3			CCU40. OUT1	CCU80. OUT10	USIC0_C H0.SCLK OUT	USIC0_C H1.DOUT 0	CCU40. IN1B	CCU40. IN1B	USIC0_C H0.DX1C	USIC0_C H1.DX1C		
P0.8	BCCU0. OUT4			CCU40. OUT2	CCU80. OUT20	USIC0_C H0.SCLK OUT	USIC0_C H1.SCLK OUT	CCU40. IN2B	CCU40. IN2B	USIC0_C H0.DX1B	USIC0_C H1.DX1B		
P0.9	BCCU0. OUT5			CCU40. OUT3	CCU80. OUT21	USIC0_C H0.SELO 0	USIC0_C H1.SELO 0	CCU40. IN3B	CCU40. IN3B	USIC0_C H0.DX2B	USIC0_C H1.DX2B		
P0.10	BCCU0. OUT6			ACMP0. OUT	CCU80. OUT22	USIC0_C H0.SELO H1.SELO 1	USIC0_C H1.SELO 1	CCU80. IN2B	CCU80. IN2B	USIC0_C H0.DX2C	USIC0_C H1.DX2C		
P0.11	BCCU0. OUT7			USIC0_C H0.MCLK OUT	CCU80. OUT23	USIC0_C H0.SELO H1.SELO 2	USIC0_C H1.SELO 2			USIC0_C H0.DX2D	USIC0_C H1.DX2D		
P0.12	BCCU0. OUT6				CCU80. OUT33	USIC0_C H0.SELO 3	CCU80. OUT20	BCCU0. TRAPINA	CCU40. IN0A	CCU40. IN1A	CCU40. IN3A	CCU80. IN0A	USIC0_C H0.DX2E
P0.13	WWDT. SERVICE _OUT				CCU80. OUT32	USIC0_C H0.SELO 4	CCU80. OUT21	CCU80. IN3B	CCU80. IN3B	POSIF0. IN0B			

**Table 2-1 Port I/O Functions (cont'd)**

Function	Outputs						Inputs							
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	
P0.14	BCCU0. OUT7				CCU80. OUT31	USIC0.C H0.DOUT 0	USIC0.C H0.SCLK OUT			POSIF0. IN1B	USIC0.C H0.DX0A	USIC0.C H0.DX1A		
P0.15	BCCU0. OUT8				CCU80. OUT30	USIC0.C H0.DOUT 0	USIC0.C H1.MCLK OUT			POSIF0. IN2B	USIC0.C H0.DX0B			
P1.0	BCCU0. OUT0	CCU40. OUT0			CCU80. OUT00	ACMP1. OUT 0	USIC0.C H0.DOUT 0			POSIF0. IN2A	USIC0.C H0.DX0C			
P1.1	VADC0. EMUX00	CCU40. OUT1			CCU80. OUT01	USIC0.C H0.DOUT 0	USIC0.C H1.SELO 0			POSIF0. IN1A	USIC0.C H0.DX0D	USIC0.C H0.DX1D	USIC0.C H1.DX2E	
P1.2	VADC0. EMUX01	CCU40. OUT2			CCU80. OUT10	ACMP2. OUT 0	USIC0.C H1.DOUT 0			POSIF0. IN2A	USIC0.C H1.DX0B			
P1.3	VADC0. EMUX02	CCU40. OUT3			CCU80. OUT11	USIC0.C H1.SCLK OUT	USIC0.C H1.DOUT 0				USIC0.C H1.DX0A	USIC0.C H1.DX1A		
P1.4	VADC0. EMUX10	USIC0.C H1.SCLK OUT			CCU80. OUT20	USIC0.C H0.SELO 0	USIC0.C H1.SELO 1				USIC0.C H0.DX5E	USIC0.C H1.DX6E		
P1.5	VADC0. EMUX11	USIC0.C H0.DOUT 0		BCCU0. OUT1	CCU80. OUT21	USIC0.C H0.SELO 1	USIC0.C H1.SELO 2				USIC0.C H1.DX5F			
P1.6	VADC0. EMUX12	USIC0.C H1.DOUT 0		USIC0.C H0.SCLK OUT	BCCU0. OUT2	USIC0.C H0.SELO 2	USIC0.C H1.SELO 3		USIC0.C H0.DX5F					
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3		CCU80. OUT20	USIC0.C H0.DOUT 0	USIC0.C H0.SCLK OUT		VADC0. G0CH6	ERU0.0B 0	USIC0.C H0.DX0E	USIC0.C H1.DX2F		
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2		CCU80. OUT21	USIC0.C H0.DOUT 0	USIC0.C H1.SCLK OUT		VADC0. G0CH6	ERU0.1B 0	USIC0.C H0.DX0F	USIC0.C H1.DX4A		
P2.2									VADC0. G0CH7	ERU0.0B 1	USIC0.C H0.DX3A	USIC0.C H1.DX5A	ORC0.AI N	
P2.3									VADC0. G1CH6	ERU0.1B 1	USIC0.C H0.DX5B	USIC0.C H1.DX4C	ORC1.AI N	
P2.4									VADC0. G1CH6	ERU0.0A 1	USIC0.C H0.DX3B	USIC0.C H1.DX4B	ORC2.AI N	

**Table 2-1 Port I/O Functions (cont'd)**

Function	Outputs							Inputs								
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	
P2.5								VADCO: G1CH7	ERU0.1A 1	USICO_C H0.DX8D	USICO_C H1.DX4E	USICO_C H1.DX4E	USICO_C H1.DX4E	USICO_C H1.DX4E	USICO_C H1.DX4E	ORC3.AI N
P2.6								VADCO: G0CH0	ERU0.2A 1	USICO_C H0.DX3E	USICO_C H0.DX4E	USICO_C H0.DX4E	USICO_C H0.DX4E	USICO_C H0.DX4E	USICO_C H0.DX4E	ORC4.AI N
P2.7								VADCO: G1CH1	ERU0.3A 1	USICO_C H0.DX5C	USICO_C H1.DX3D	USICO_C H1.DX4D	USICO_C H1.DX4D	USICO_C H1.DX4D	USICO_C H1.DX4D	ORC5.AI N
P2.8								VADCO: G0CH1	ERU0.3B 1	USICO_C H0.DX3D	USICO_C H0.DX4D	USICO_C H0.DX4D	USICO_C H0.DX4D	USICO_C H0.DX4D	USICO_C H0.DX4D	ORC6.AI N
P2.9								VADCO: G0CH2	ERU0.3B 0	USICO_C H0.DX9A	USICO_C H1.DX3B	USICO_C H1.DX4B	USICO_C H1.DX4B	USICO_C H1.DX4B	USICO_C H1.DX4B	ORC7.AI N
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1		CCU80. OUT30	ACMP0. OUT	USICO_C H1.DOUT 0	VADCO: G0CH3	ERU0.2B 0	USICO_C H0.DX3C	USICO_C H0.DX4C	USICO_C H0.DX4C	USICO_C H0.DX4C	USICO_C H0.DX4C	USICO_C H0.DX4C	
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0		CCU80. OUT31	USICO_C H1.SCLK OUT	USICO_C H1.DOUT 0	VADCO: G0CH4	ERU0.2B 1	USICO_C H1.DX0E	USICO_C H1.DX1E	USICO_C H1.DX1E	USICO_C H1.DX1E	USICO_C H1.DX1E	USICO_C H1.DX1E	

**Table 2-2 Hardware Controlled I/O Functions**

Function	Outputs		Inputs		Pull Control			
	HW00	HW01	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0								
P0.1								
P0.2								
P0.3								
P0.4								
P0.5								
P0.6								
P0.7								
P0.8								
P0.9								
P0.10								
P0.11								
P0.12								
P0.13								
P0.14								
P0.15								
P1.0		USICO_CH0.DOUT0		USICO_CH0.HWIN0	BCCU0.OUT2	BCCU0.OUT2		
P1.1		USICO_CH0.DOUT1		USICO_CH0.HWIN1	BCCU0.OUT3	BCCU0.OUT3		
P1.2		USICO_CH0.DOUT2		USICO_CH0.HWIN2	BCCU0.OUT4	BCCU0.OUT4		
P1.3		USICO_CH0.DOUT3		USICO_CH0.HWIN3	BCCU0.OUT5	BCCU0.OUT5		
P1.4					BCCU0.OUT6	BCCU0.OUT6		
P1.5					BCCU0.OUT7	BCCU0.OUT7		
P1.6					BCCU0.OUT8	BCCU0.OUT8		
P2.0					BCCU0.OUT1	BCCU0.OUT1		
P2.1					BCCU0.OUT6	BCCU0.OUT6		
P2.2					BCCU0.OUT0	BCCU0.OUT0	CCU40.OUT3	CCU40.OUT3
P2.3					ACMP2.OUT	ACMP2.OUT		
P2.4					BCCU0.OUT8	BCCU0.OUT8		

**Table 2-2 Hardware Controlled I/O Functions (cont'd)**

Function	Outputs		Inputs		Pull Control				
	HWO0	HWO1	HWI0	HWI1	HWO_PD	HWO_PU	HW1_PD	HW1_PU	HW1_PU
P2.5					ACMP1.OUT	ACMP1.OUT			HW1_PU
P2.6					BCCU0.OUT2	BCCU0.OUT2		CCU40.OUT3	CCU40.OUT3
P2.7					BCCU0.OUT8	BCCU0.OUT8		CCU40.OUT3	CCU40.OUT3
P2.8					BCCU0.OUT1	BCCU0.OUT1		CCU40.OUT2	CCU40.OUT2
P2.9					BCCU0.OUT7	BCCU0.OUT7		CCU40.OUT2	CCU40.OUT2
P2.10					BCCU0.OUT4	BCCU0.OUT4			
P2.11					BCCU0.OUT5	BCCU0.OUT5			



## **3 Electrical Parameters**

This section provides the electrical parameters which are implementation-specific for the XMC1300.

### **3.1 General Parameters**

#### **3.1.1 Parameter Interpretation**

The parameters listed in this section represent partly the characteristics of the XMC1300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**  
Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1300 and must be regarded for a system design.
- **SR**  
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1300 is designed in.

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 9 Absolute Maximum Rating Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min	Typ.	Max.		
Junction temperature	$T_J$	SR	-40	–	115	°C	–
Storage temperature	$T_{ST}$	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to $V_{SSP}$	$V_{DDP}$	SR	-0.3	–	6	V	–
Voltage on digital pins with respect to $V_{SSP}$ <sup>1)</sup>	$V_{IN}$	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Voltage on P2 pins with respect to $V_{SSP}$ <sup>2)</sup>	$V_{INP2}$	SR	-0.3	–	$V_{DDP} + 0.3$	V	–
Voltage on analog input pins with respect to $V_{SSP}$	$V_{AIN}$ $V_{AREF}$	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Input current on any pin during overload condition	$I_{IN}$	SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	$\Sigma I_{IN}$	SR	-50	–	+50	mA	–

1) Excluding port pins P2.[1,2,6,7,8,9,11].

2) Applicable to port pins P2.[1,2,6,7,8,9,11].

### 3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 10** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ( $V_{DDP}$ )
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

*Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

**Table 10** Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	$I_{OV}$	SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	$I_{OVS}$	SR	–	–	25	mA	

**Figure 10** shows the path of the input currents during overload via the ESD protection structures. The diodes against  $V_{DDP}$  and ground are a simplified representation of these ESD protection structures.

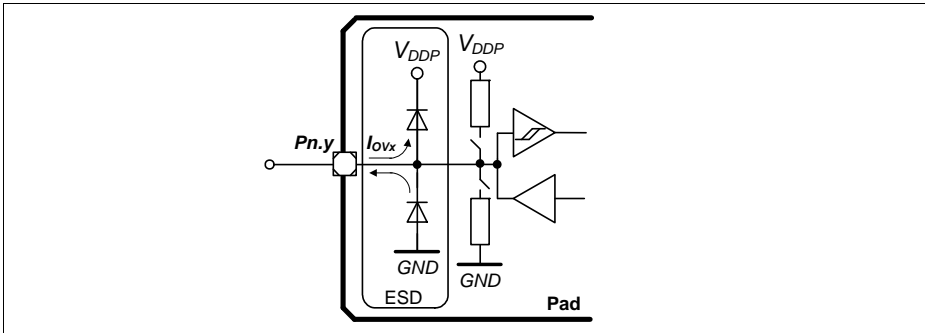


Figure 10 Input Overload Current via ESD structures

Table 11 and Table 12 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute Maximum Ratings must not be exceeded during overload.

Table 11 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5 \text{ V}$ $V_{AIN} = V_{DDP} + 0.5 \text{ V}$ $V_{AREF} = V_{DDP} + 0.5 \text{ V}$
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3 \text{ V}$

Table 12 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5 \text{ V}$ $V_{AIN} = V_{SS} - 0.5 \text{ V}$ $V_{AREF} = V_{SS} - 0.5 \text{ V}$
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3 \text{ V}$

### 3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

**Table 13 Operating Conditions Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	$T_A$	SR	-40	–	85	°C	Temp. Range F
			-40	–	105	°C	Temp. Range X
Digital supply voltage <sup>1)</sup>	$V_{DDP}$	SR	1.8	–	5.5	V	
MCLK Frequency	$f_{MCLK}$	CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	$f_{PCLK}$	CC	–	–	66.4	MHz	Peripherals clock
Short circuit current of digital outputs	$I_{SC}$	SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	$\Sigma I_{SC\_D}$	SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, [Chapter 3.3.2](#).

### 3.2 DC Parameters

#### 3.2.1 Input/Output Characteristics

**Table 14** provides the characteristics of the input/output pins of the XMC1300.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

**Table 14 Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Output low voltage on port pins (with standard pads)	$V_{OLP}$ CC	–	1.0	V	$I_{OL} = 11 \text{ mA}$ (5 V) $I_{OL} = 7 \text{ mA}$ (3.3 V)
		–	0.4	V	$I_{OL} = 5 \text{ mA}$ (5 V) $I_{OL} = 3.5 \text{ mA}$ (3.3 V)
Output low voltage on high current pads	$V_{OLP1}$ CC	–	1.0	V	$I_{OL} = 50 \text{ mA}$ (5 V) $I_{OL} = 25 \text{ mA}$ (3.3 V)
		–	0.32	V	$I_{OL} = 10 \text{ mA}$ (5 V)
		–	0.4	V	$I_{OL} = 5 \text{ mA}$ (3.3 V)
Output high voltage on port pins (with standard pads)	$V_{OHP}$ CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA}$ (5 V) $I_{OH} = -7 \text{ mA}$ (3.3 V)
		$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA}$ (5 V) $I_{OH} = -2.5 \text{ mA}$ (3.3 V)
Output high voltage on high current pads	$V_{OHP1}$ CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA}$ (5 V)
		$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA}$ (3.3 V)
		$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA}$ (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	$V_{ILPS}$ SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

**Electrical Parameters**
**Table 14 Input/Output Characteristics (Operating Conditions apply) (cont'd)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Standard Hysteresis)	$V_{IHPS}$	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	$V_{ILPL}$	SR	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) <sup>18)</sup>
Input high voltage on port pins (Large Hysteresis)	$V_{IHPL}$	SR	$0.85 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V) <sup>18)</sup>
Rise time on High Current Pad <sup>1)</sup>	$t_{HCPR}$	CC	–	9	ns	50 pF @ 5 V <sup>2)</sup>
			–	12	ns	50 pF @ 3.3 V <sup>3)</sup>
			–	25	ns	50 pF @ 1.8 V <sup>4)</sup>
Fall time on High Current Pad <sup>1)</sup>	$t_{HCPF}$	CC	–	9	ns	50 pF @ 5 V <sup>2)</sup>
			–	12	ns	50 pF @ 3.3 V <sup>3)</sup>
			–	25	ns	50 pF @ 1.8 V <sup>4)</sup>
Rise time on Standard Pad <sup>1)</sup>	$t_R$	CC	–	12	ns	50 pF @ 5 V <sup>5)</sup>
			–	15	ns	50 pF @ 3.3 V <sup>6)</sup>
			–	31	ns	50 pF @ 1.8 V <sup>7)</sup>
Fall time on Standard Pad <sup>1)</sup>	$t_F$	CC	–	12	ns	50 pF @ 5 V <sup>5)</sup>
			–	15	ns	50 pF @ 3.3 V <sup>6)</sup>
			–	31	ns	50 pF @ 1.8 V <sup>7)</sup>

**Electrical Parameters**
**Table 14 Input/Output Characteristics (Operating Conditions apply) (cont'd)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis <sup>8)</sup>	<i>HYS</i>	CC	$0.08 \times V_{DDP}$	–	V	CMOS Mode (5 V), Standard Hysteresis
			$0.03 \times V_{DDP}$	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			$0.02 \times V_{DDP}$	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
			$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis
			$0.2 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	$C_{IO}$	CC	–	10	pF	
Pull-up resistor on port pins	$R_{PUP}$	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	$R_{PDP}$	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current <sup>9)</sup>	$I_{OZP}$	CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$ , $T_A \leq 105\text{ °C}$
Voltage on any pin during $V_{DDP}$ power off	$V_{PO}$	SR	–	0.3	V	<sup>10)</sup>
Maximum current per pin (excluding P1, $V_{DDP}$ and $V_{SS}$ )	$I_{MP}$	SR	-10	11	mA	–
Maximum current per high current pins	$I_{MP1A}$	SR	-10	50	mA	–
Maximum current into $V_{DDP}$ (TSSOP16, VQFN24)	$I_{MVDD1}$	SR	–	130	mA	<sup>18)</sup>
Maximum current into $V_{DDP}$ (TSSOP38, VQFN40)	$I_{MVDD2}$	SR	–	260	mA	<sup>18)</sup>



**Electrical Parameters**

**Table 14 Input/Output Characteristics (Operating Conditions apply) (cont'd)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current out of $V_{SS}$ (TSSOP16, VQFN24)	$I_{MVSS1}$	SR	–	130	mA	<sup>18)</sup>
Maximum current out of $V_{SS}$ (TSSOP38, VQFN40)	$I_{MVSS2}$	SR	–	260	mA	<sup>18)</sup>

- 1) Rise/Fall time parameters are taken with 10% - 90% of supply.
- 2) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
- 3) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
- 4) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
- 5) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
- 6) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
- 7) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.
- 8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 9) An additional error current ( $I_{INL}$ ) will flow if an overload current flows through an adjacent pin.
- 10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when  $V_{DDP}$  is powered off.

### 3.2.2 Analog to Digital Converters (ADC)

**Table 15** shows the Analog to Digital Converter (ADC) characteristics.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 15 ADC Characteristics (Operating Conditions apply)<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	$V_{DD\_int}$ SR	2.0	–	3.0	V	SHSCFG.AREF = 11 <sub>B</sub> CALCTR.CALGNSTC = 0C <sub>H</sub>
		3.0	–	5.5	V	SHSCFG.AREF = 10 <sub>B</sub>
Supply voltage range (external reference)	$V_{DD\_ext}$ SR	3.0	–	5.5	V	SHSCFG.AREF = 00 <sub>B</sub>
Analog input voltage range	$V_{AIN}$ SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Auxiliary analog reference ground	$V_{REFGND}$ SR	$V_{SSP} - 0.05$	–	1.0	V	G0CH0
		$V_{SSP} - 0.05$	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	$V_{REFINT}$ CC	5			V	
Switched capacitance of an analog input	$C_{AINS}$ CC	–	1.2	2	pF	GNCTRxz.GAINy = 00 <sub>B</sub> (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01 <sub>B</sub> (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10 <sub>B</sub> (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11 <sub>B</sub> (gain g3)
Total capacitance of an analog input	$C_{AINT}$ CC	–	–	10	pF	
Total capacitance of the reference input	$C_{AREFT}$ CC	–	–	10	pF	

**Electrical Parameters**
**Table 15 ADC Characteristics (Operating Conditions apply)<sup>1)</sup> (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	$G_{IN}$ CC	1			–	GNCTRxz.GAINy = 00 <sub>B</sub> (unity gain)
		3			–	GNCTRxz.GAINy = 01 <sub>B</sub> (gain g1)
		6			–	GNCTRxz.GAINy = 10 <sub>B</sub> (gain g2)
		12			–	GNCTRxz.GAINy = 11 <sub>B</sub> (gain g3)
Sample Time	$t_{sample}$ CC	3	–	–	1 / $f_{ADC}$	$V_{DD} = 5.0$ V
		3	–	–	1 / $f_{ADC}$	$V_{DD} = 3.3$ V
		30	–	–	1 / $f_{ADC}$	$V_{DD} = 2.0$ V
Sigma delta loop hold time	$t_{SD\_hold}$ CC	20	–	–	μs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	$t_{CF}$ CC	9			1 / $f_{ADC}$	<sup>2)</sup>
Conversion time in 12-bit mode	$t_{C12}$ CC	20			1 / $f_{ADC}$	<sup>2)</sup>
Maximum sample rate in 12-bit mode <sup>3)</sup>	$f_{C12}$ CC	–	–	$f_{ADC} / 42.5$	–	1 sample pending
		–	–	$f_{ADC} / 62.5$	–	2 samples pending
Conversion time in 10-bit mode	$t_{C10}$ CC	18			1 / $f_{ADC}$	<sup>2)</sup>
Maximum sample rate in 10-bit mode <sup>3)</sup>	$f_{C10}$ CC	–	–	$f_{ADC} / 40.5$	–	1 sample pending
		–	–	$f_{ADC} / 58.5$	–	2 samples pending
Conversion time in 8-bit mode	$t_{C8}$ CC	16			1 / $f_{ADC}$	<sup>2)</sup>

**Electrical Parameters**
**Table 15 ADC Characteristics (Operating Conditions apply)<sup>1)</sup> (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode <sup>3)</sup>	$f_{C8}$ CC	–	–	$f_{ADC} / 38.5$	–	1 sample pending
		–	–	$f_{ADC} / 54.5$	–	2 samples pending
RMS noise <sup>4)</sup>	$EN_{RMS}$ CC	–	1.5	–	LSB 12	DC input, $V_{DD} = 5.0$ V, $V_{AIN} = 2.5$ V, 25°C
DNL error	$EA_{DNL}$ CC	–	±2.0	–	LSB 12	
INL error	$EA_{INL}$ CC	–	±4.0	–	LSB 12	
Gain error with external reference	$EA_{GAIN}$ CC	–	±0.5	–	%	SHSCFG.AREF = 00 <sub>B</sub> (calibrated)
Gain error with internal reference <sup>5)</sup>	$EA_{GAIN}$ CC	–	±3.6	–	%	SHSCFG.AREF = 1X <sub>B</sub> (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = 1X <sub>B</sub> (calibrated), 0°C - 85°C
Offset error	$EA_{OFF}$ CC	–	±8.0	–	mV	Calibrated, $V_{DD} = 5.0$ V

1) The parameters are defined for ADC clock frequency  $f_{SH} = 32$  MHz, SHSCFG.DIVS = 0000<sub>B</sub>. Usage of any other frequencies may affect the ADC performance.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

4) This parameter can also be defined as an SNR value:  $SNR[dB] = 20 \times \log(A_{MAXeff} / N_{RMS})$ .

With  $A_{MAXeff} = 2^N / 2$ ,  $SNR[dB] = 20 \times \log(2048 / N_{RMS})$  [N = 12].

$N_{RMS} = 1.5$  LSB<sub>12</sub>, therefore, equals  $SNR = 20 \times \log(2048 / 1.5) = 62.7$  dB.

5) Includes error from the reference voltage.

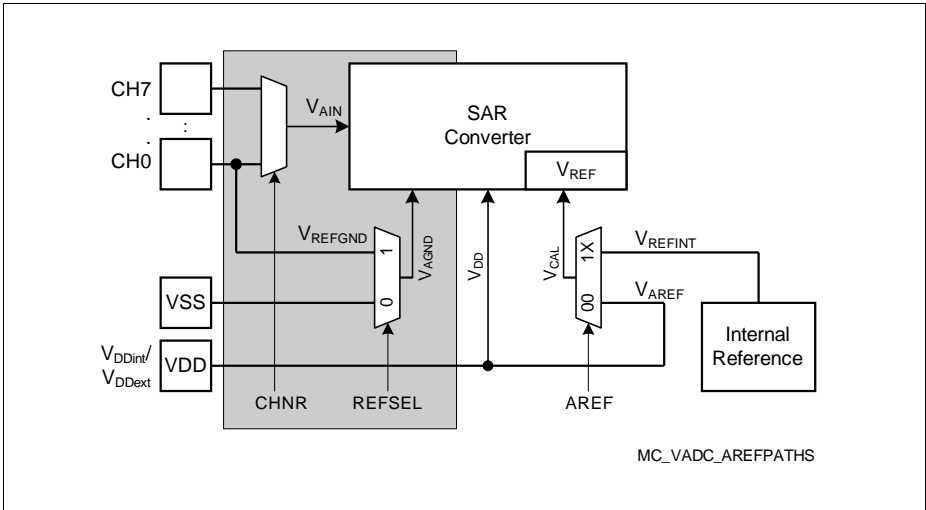


Figure 11 ADC Voltage Supply

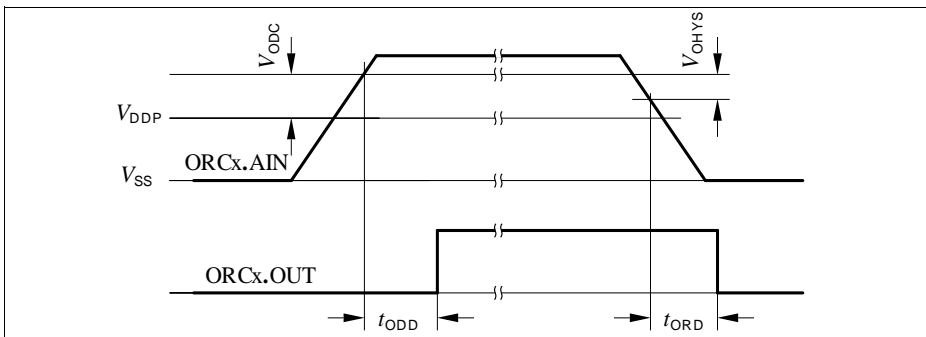
### 3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages ( $V_{AIN}$ ) above the  $V_{DDP}$  on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 16 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply;  $V_{DDP} = 3.0\text{ V} - 5.5\text{ V}$ ;  $C_L = 0.25\text{ pF}$ )**

Parameter	Symbol	Values	Unit			Note / Test Condition
			Min.	Typ.	Max.	
DC Switching Level	$V_{ODC}$ CC	54	–	183	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	$V_{OHYS}$ CC	15	–	54	mV	
Always detected Overvoltage Pulse	$t_{OPDD}$ CC	103	–	-	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
		88	–	-	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Never detected Overvoltage Pulse	$t_{OPDN}$ CC	–	–	21	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
		–	–	11	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Detection Delay of a persistent Overvoltage	$t_{ODD}$ CC	39	–	132	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
		31	–	121	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Release Delay	$t_{ORD}$ CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$ ; $V_{DDP} = 5\text{ V}$
		57	–	340	ns	$V_{AIN} \leq V_{DDP}$ ; $V_{DDP} = 3.3\text{ V}$
Enable Delay	$t_{OED}$ CC	–	–	300	ns	ORCCTRL.ENORCx = 1



**Figure 12 ORCx.OUT Trigger Generation**

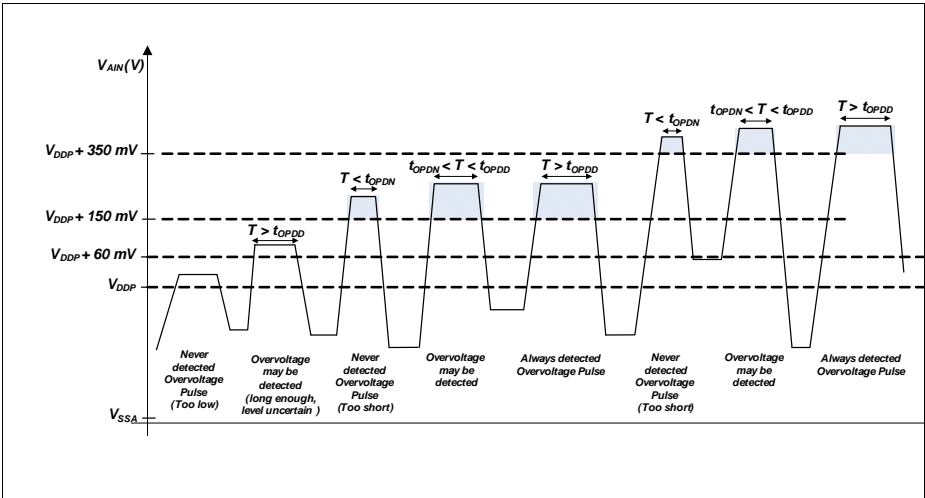


Figure 13 ORC Detection Ranges

### 3.2.4 Analog Comparator Characteristics

**Table 17** below shows the Analog Comparator characteristics.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 17 Analog Comparator Characteristics (Operating Conditions apply)**

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	$V_{CMP}$	SR	-0.05	–	$V_{DDP} + 0.05$	V	
Input Offset	$V_{CMPOFF}$	CC	–	+/-3	–	mV	High power mode $\Delta V_{CMP} < 200$ mV
			–	+/-20	–	mV	Low power mode $\Delta V_{CMP} < 200$ mV
Propagation Delay <sup>1)</sup>	$t_{PDELAY}$	CC	–	25	–	ns	High power mode, $\Delta V_{CMP} = 100$ mV
			–	80	–	ns	High power mode, $\Delta V_{CMP} = 25$ mV
			–	250	–	ns	Low power mode, $\Delta V_{CMP} = 100$ mV
			–	700	–	ns	Low power mode, $\Delta V_{CMP} = 25$ mV
Current Consumption	$I_{ACMP}$	CC	–	100	–	$\mu$ A	First active ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			–	66	–	$\mu$ A	Each additional ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			–	10	–	$\mu$ A	First active ACMP in low power mode
			–	6	–	$\mu$ A	Each additional ACMP in low power mode
Input Hysteresis	$V_{HYS}$	CC	–	+/-15	–	mV	
Filter Delay <sup>1)</sup>	$t_{FDELAY}$	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.



### 3.2.5 Temperature Sensor Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

**Table 18 Temperature Sensor Characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	$t_M$ CC	–	–	10	ms	
Temperature sensor range	$T_{SR}$ SR	-40	–	115	°C	
Sensor Accuracy <sup>1)</sup>	$T_{TSAL}$ CC	-6	–	6	°C	$T_J > 20^\circ\text{C}$
		-10	–	10	°C	$0^\circ\text{C} \leq T_J \leq 20^\circ\text{C}$
		–	-/+8	–	°C	$T_J < 0^\circ\text{C}$
Start-up time after enabling	$t_{TSSTE}$ SR	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

### 3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 19 Power Supply Parameters;  $V_{DDP} = 5V$**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min	Typ. <sup>1)</sup>	Max.		
Active mode current Peripherals enabled $f_{MCLK} / f_{PCLK}$ in MHz <sup>2)</sup>	$I_{DDPAE}$ CC	–	9.2	12	mA	32 / 64
		–	8.1	-	mA	24 / 48
		–	6.6	-	mA	16 / 32
		–	5.5	-	mA	8 / 16
		–	4	-	mA	1 / 1
Active mode current Peripherals disabled $f_{MCLK} / f_{PCLK}$ in MHz <sup>3)</sup>	$I_{DDPAD}$ CC	–	4.8	-	mA	32 / 64
		–	4.1	-	mA	24 / 48
		–	3.3	-	mA	16 / 32
		–	2.7	-	mA	8 / 16
		–	1.5	-	mA	1 / 1
Active mode current Code execution from RAM Flash is powered down $f_{MCLK} / f_{PCLK}$ in MHz	$I_{DDPAR}$ CC	–	7.3	-	mA	32 / 64
		–	6.3	-	mA	24 / 48
		–	5.2	-	mA	16 / 32
		–	4.2	-	mA	8 / 16
		–	3.3	-	mA	1 / 1
Sleep mode current Peripherals clock enabled $f_{MCLK} / f_{PCLK}$ in MHz <sup>4)</sup>	$I_{DDPSE}$ CC	–	6.6	-	mA	32 / 64
			5.8	-	mA	24 / 48
			5.1	-	mA	16 / 32
			4.4	-	mA	8 / 16
			3.7	-	mA	1 / 1

**Table 19 Power Supply Parameters;  $V_{DDP} = 5V$** 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min	Typ. <sup>1)</sup>	Max.		
Sleep mode current Peripherals clock disabled Flash active $f_{MCLK} / f_{PCLK}$ in MHz <sup>5)</sup>	$I_{DDPSD}$ CC	–	1.8	-	mA	32 / 64
			1.7	-	mA	24 / 48
			1.6	-	mA	16 / 32
			1.5	-	mA	8 / 16
			1.4	-	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down $f_{MCLK} / f_{PCLK}$ in MHz <sup>6)</sup>	$I_{DDPSR}$ CC	–	1.2	-	mA	32 / 64
			1.1	-	mA	24 / 48
			1.0	-	mA	16 / 32
			0.8	-	mA	8 / 16
			0.7	-	mA	1 / 1
Deep Sleep mode current <sup>7)</sup>	$I_{DDPDS}$ CC	–	0.24	-	mA	
Wake-up time from Sleep to Active mode <sup>8)</sup>	$t_{SSA}$ CC	–	6	-	cycles	
Wake-up time from Deep Sleep to Active mode <sup>9)</sup>	$t_{DSA}$ CC	–	280	-	μsec	

1) The typical values are measured at  $T_A = +25\text{ °C}$  and  $V_{DDP} = 5V$ .

2) CPU and all peripherals clock enabled, Flash is in active mode.

3) CPU enabled, all peripherals clock disabled, Flash is in active mode.

4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.

5) CPU in sleep, Flash is in active mode.

6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.

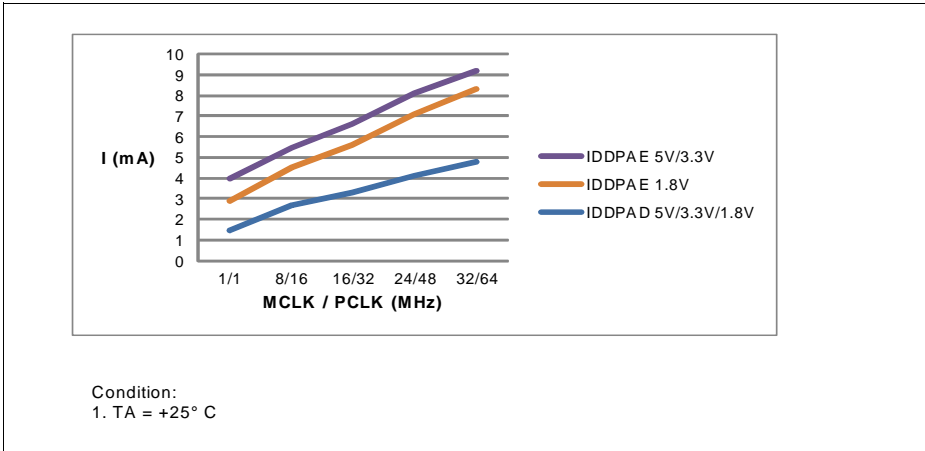
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.

8) CPU in sleep, Flash is in active mode during sleep mode.

9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

**Electrical Parameters**

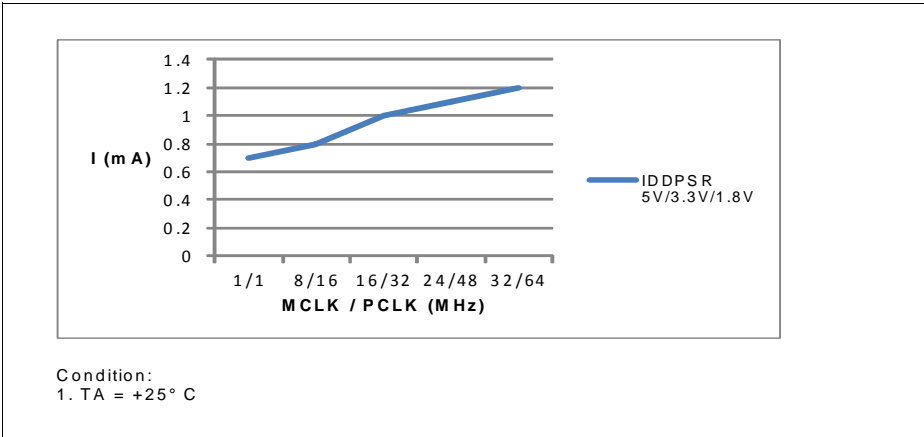
**Figure 14** shows typical graphs for active mode supply current for  $V_{DDP} = 5V$ ,  $V_{DDP} = 3.3V$ ,  $V_{DDP} = 1.8V$  across different clock frequencies.



**Figure 14 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current  $I_{DDPA}$  over supply voltage  $V_{DDP}$  for different clock frequencies**

**Electrical Parameters**

**Figure 15** shows typical graphs for sleep mode current for  $V_{DDP} = 5V$ ,  $V_{DDP} = 3.3V$ ,  $V_{DDP} = 1.8V$  across different clock frequencies.



**Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down:  
Supply current  $I_{DDPSR}$  over supply voltage  $V_{DDP}$  for different clock frequencies**

**Electrical Parameters**

**Table 20** provides the active current consumption of some modules operating at 5 V power supply at 25° C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

**Table 20 Typical Active Current Consumption**

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	$I_{CPUDDC}$	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP <sup>1)</sup>
VADC and SHS	$I_{ADCDCC}$	3.4	mA	Set CGATCLR0.VADC to 1 <sup>2)</sup>
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1 <sup>3)</sup>
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1 <sup>4)</sup>
CCU80	$I_{CCU80DDC}$	0.42	mA	Set CGATCLR0.CCU80 to 1 <sup>5)</sup>
POSIF0	$I_{PIF0DDC}$	0.26	mA	Set CGATCLR0.POSIF0 to 1 <sup>6)</sup>
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1 <sup>7)</sup>
MATH	$I_{MATHDDC}$	0.35	mA	Set CGATCLR0.MATH to 1 <sup>8)</sup>
WDT	$I_{WDTDDC}$	0.03	mA	Set CGATCLR0.WDT to 1 <sup>9)</sup>
RTC	$I_{RTCDCC}$	0.01	mA	Set CGATCLR0.RTC to 1 <sup>10)</sup>

- 1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
- 2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode
- 3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms
- 4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle
- 5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%
- 6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode
- 7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s
- 8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11
- 9) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s
- 10) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

### 3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

**Table 21 Flash Memory Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page / sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSE}} \text{ CC}$	102	152	204	$\mu\text{s}$	
Wake-Up time	$t_{\text{WU}} \text{ CC}$	–	32.2	–	$\mu\text{s}$	
Read time per word	$t_{\text{a}} \text{ CC}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET}} \text{ CC}$	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States <sup>1)</sup>	$N_{\text{WSFLASH}} \text{ CC}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	1.3	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{\text{FWSFLASH}} \text{ SR}$	0	0	1		NVM_CONFIG1.FI XWS = 1 <sub>B</sub> , $f_{\text{MCLK}} \leq 16 \text{ MHz}$
		1	1	1		NVM_CONFIG1.FI XWS = 1 <sub>B</sub> , $16 \text{ MHz} < f_{\text{MCLK}} \leq 32 \text{ MHz}$
Erase Cycles	$N_{\text{ECYC}} \text{ CC}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECYC}} \text{ CC}$	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

### 3.3 AC Parameters

#### 3.3.1 Testing Waveforms

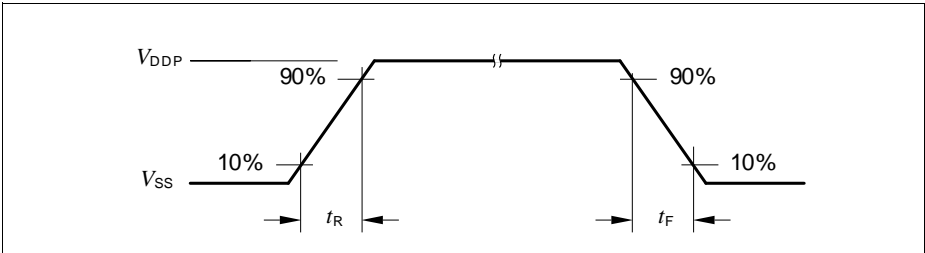


Figure 16 Rise/Fall Time Parameters

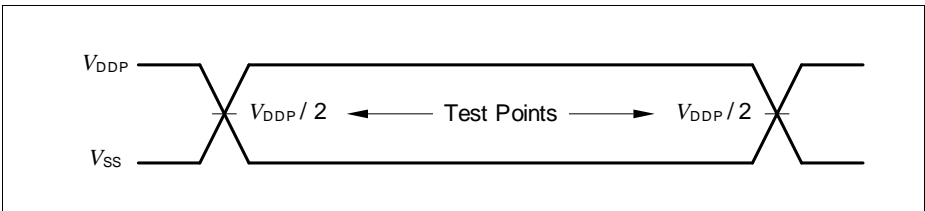


Figure 17 Testing Waveform, Output Delay

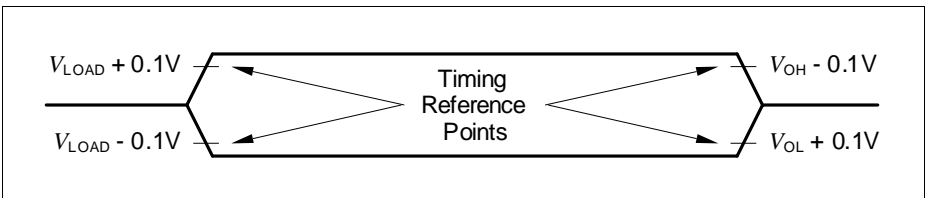


Figure 18 Testing Waveform, Output High Impedance



### 3.3.2 Power-Up and Supply Monitoring Characteristics

**Table 22** provides the characteristics of the power-up and supply monitoring in XMC1300.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while  $V_{DDP}$  is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 22 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)**

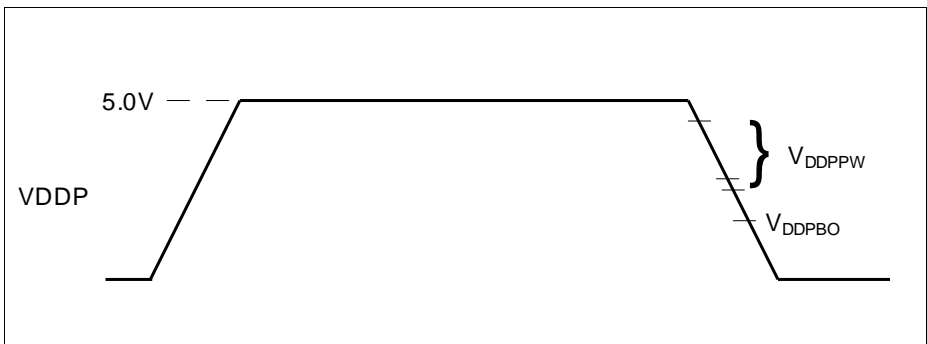
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$V_{DDP}$ ramp-up time	$t_{RAMPUP}$ SR	$V_{DDP}/S_{VDDPrise}$	–	$10^7$	$\mu s$	
$V_{DDP}$ slew rate	$S_{VDDPOP}$ SR	0	–	0.1	$V/\mu s$	Slope during normal operation
	$S_{VDDP10}$ SR	0	–	10	$V/\mu s$	Slope during fast transient within +/- 10% of $V_{DDP}$
	$S_{VDDPrise}$ SR	0	–	10	$V/\mu s$	Slope during power-on or restart after brownout event
	$S_{VDDPfall}^{1)}$ SR	0	–	0.25	$V/\mu s$	Slope during supply falling out of the +/- 10% limits <sup>2)</sup>
$V_{DDP}$ prewarning voltage	$V_{DDPPW}$ CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00 <sub>B</sub>
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01 <sub>B</sub>
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10 <sub>B</sub>

**Electrical Parameters**

**Table 22 Power-Up and Supply Monitoring Parameters (Operating Conditions apply) (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$V_{DDP}$ brownout reset voltage	$V_{DDPBO}$ CC	1.55	1.62	1.75	V	calibrated, before user code starts running
$V_{DDP}$ voltage to ensure defined pad states	$V_{DDPPA}$ CC	–	1.0	–	V	
Start-up time from power-on reset	$t_{SSW}$ SR	–	320	–	$\mu$ s	Time to the first user code instruction <sup>3)</sup>
BMI program time	$t_{BMI}$ SR	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is requested

- 1) A capacitor of at least 100 nF has to be added between VDDP and VSSP to fulfill the requirement as stated for this parameter.
- 2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.
- 3) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.



**Figure 19 Supply Threshold Parameters**

### 3.3.3 On-Chip Oscillator Characteristics

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23** provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

**Table 23 64 MHz DCO1 Characteristics (Operating Conditions apply)**

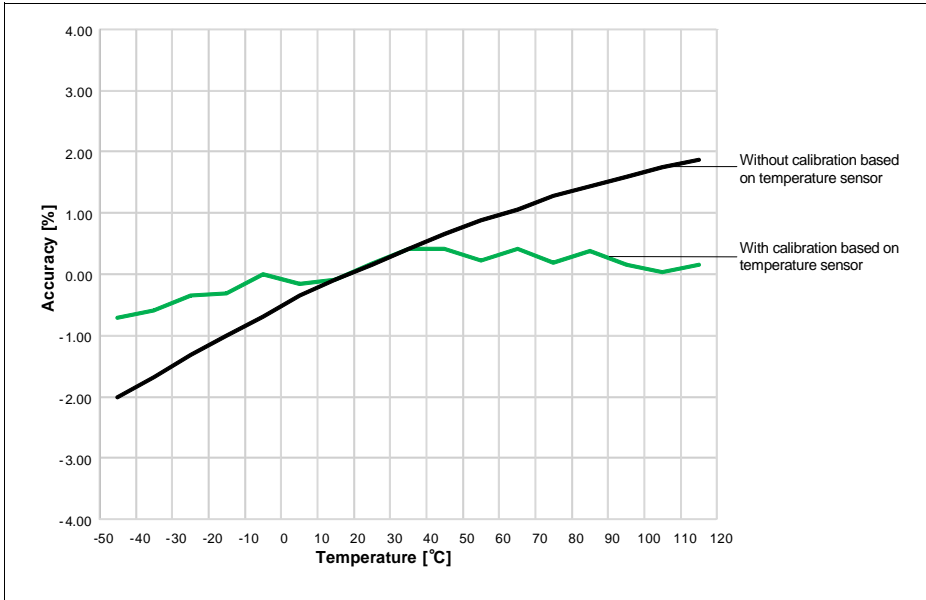
Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	$f_{\text{NOM}}$	CC	–	64	–	MHz	under nominal conditions <sup>1)</sup> after trimming
Accuracy <sup>2)</sup>	$\Delta f_{\text{LT}}$	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$ , over temperature ( $T_{\text{A}} = 0\text{ °C}$ to $85\text{ °C}$ )
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$ , over temperature ( $T_{\text{A}} = -40\text{ °C}$ to $105\text{ °C}$ )

1) The deviation is relative to the factory trimmed frequency at nominal  $V_{\text{DDC}}$  and  $T_{\text{A}} = +25\text{ °C}$ .

2) The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

**Electrical Parameters**

**Figure 20** shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.



**Figure 20 Typical DCO1 accuracy over temperature**

**Table 24** provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

**Table 24 32 kHz DCO2 Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values	Unit			Test Conditions
			Min.	Typ.	Max.	
Nominal frequency	$f_{\text{NOM}}$ CC	–	32.75	–	kHz	under nominal conditions <sup>1)</sup> after trimming
Accuracy	$\Delta f_{\text{LT}}$ CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$ , over temperature (0 °C to 85 °C)
		-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$ , over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal  $V_{\text{DDC}}$  and  $T_{\text{A}} = +25$  °C.

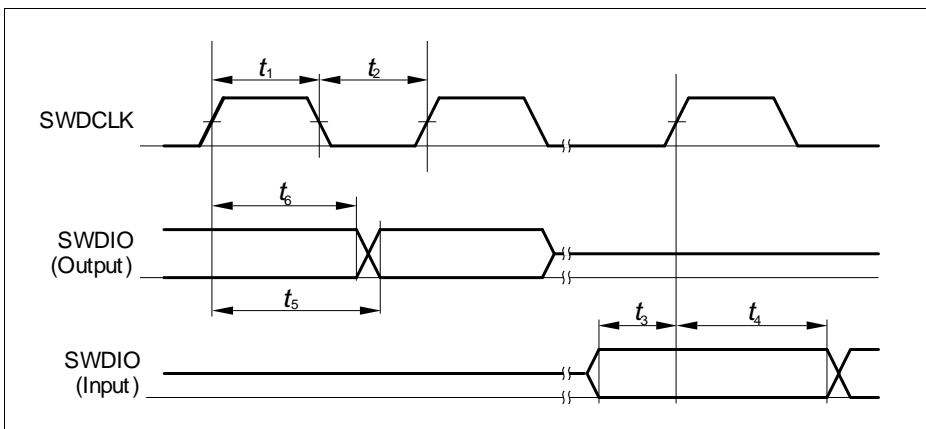
### 3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 25 SWD Interface Timing Parameters(Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	$t_1$ SR	50	–	500000	ns	–
SWDCLK low time	$t_2$ SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	$t_3$ SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	$t_4$ SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	$t_5$ CC	–	–	68	ns	$C_L = 50$ pF
		–	–	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	$t_6$ CC	4	–	–	ns	



**Figure 21 SWD Timing**

### 3.3.5 SPD Timing Requirements

The optimum SPD decision time between  $0_B$  and  $1_B$  is  $0.75 \mu\text{s}$ . With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles ( $0.69 \mu\text{s}$ ).

**Table 26 Optimum Number of Sample Clocks for SPD**

Sample Freq.	Sampling Factor	Sample Clocks $0_B$	Sample Clocks $1_B$	Effective Decision Time <sup>1)</sup>	Remark
8 MHz	4	1 to 5	6 to 12	$0.69 \mu\text{s}$	The other closest option ( $0.81 \mu\text{s}$ ) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with  $0.5 + (\text{max. number of } 0_B \text{ sample clocks})$

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between  $0.69 \mu\text{s}$  and  $0.75 \mu\text{s}$  (calculated with nominal sample frequency)

### 3.3.6 Peripheral Timings

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: Operating Conditions apply.*

**Table 27 USIC SSC Master Mode Timing**

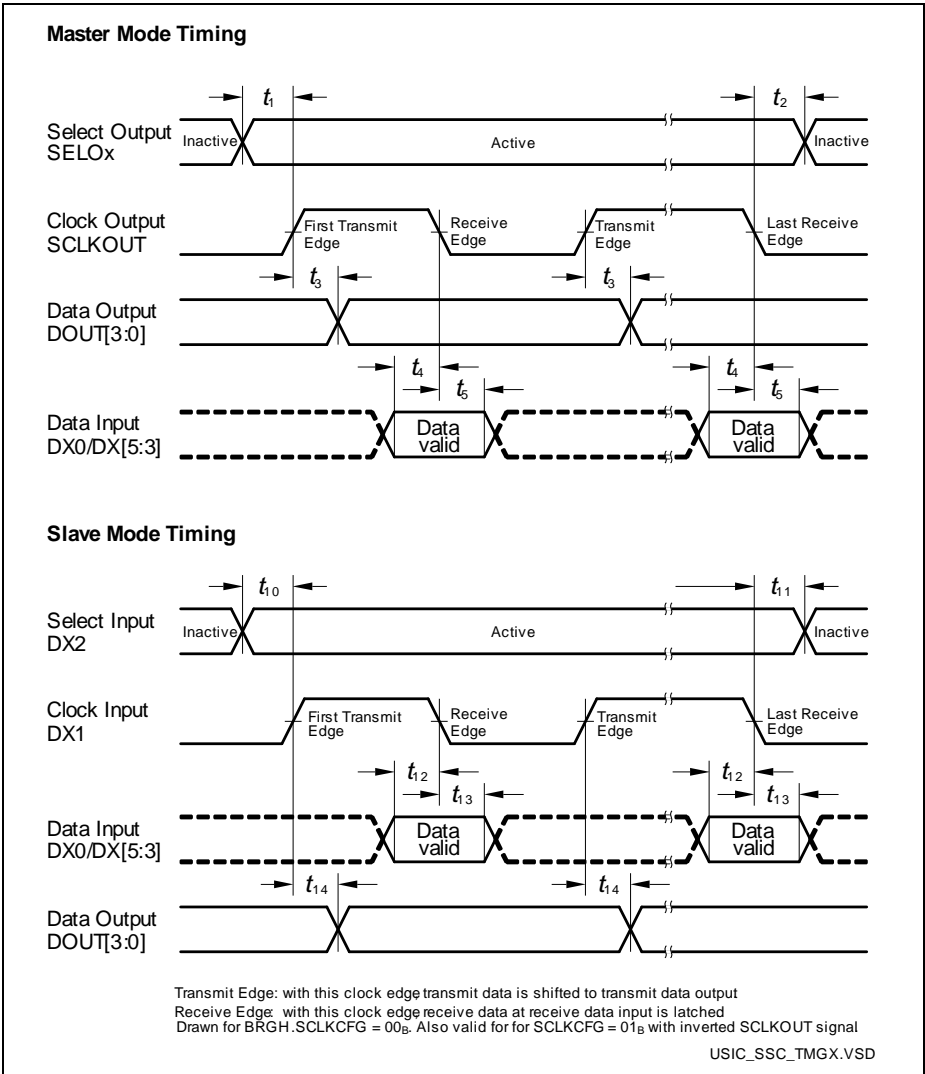
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	$t_{CLK}$ CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	$t_1$ CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	$t_2$ CC	0	–	–	ns	
Data output DOUT[3:0] valid time	$t_3$ CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	$t_4$ SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	$t_5$ SR	0	–	–	ns	

**Table 28 USIC SSC Slave Mode Timing**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	$t_{CLK}$	SR	125	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge <sup>1)</sup>	$t_{10}$	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge <sup>1)</sup>	$t_{11}$	SR	10	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge <sup>1)</sup>	$t_{12}$	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge <sup>1)</sup>	$t_{13}$	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	$t_{14}$	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).





**Figure 22 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

### 3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

*Note: Operating Conditions apply.*

**Table 29 USIC IIC Standard Mode Timing<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$ CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	$t_2$ CC/SR	-	-	1000	ns	
Data hold time	$t_3$ CC/SR	0	-	-	μs	
Data set-up time	$t_4$ CC/SR	250	-	-	ns	
LOW period of SCL clock	$t_5$ CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	$t_6$ CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	$t_7$ CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	$t_8$ CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	$t_9$ CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	$t_{10}$ CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	

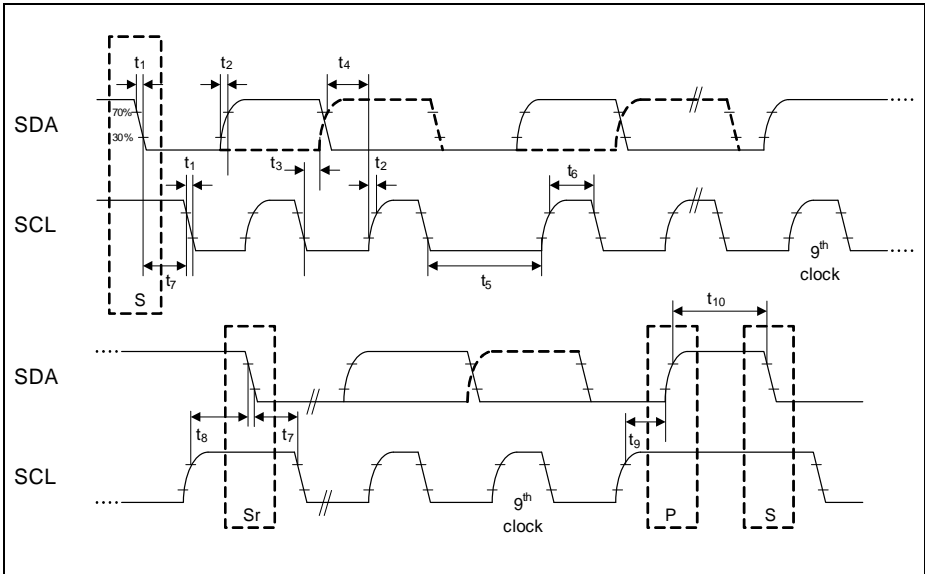
1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

**Table 30 USIC IIC Fast Mode Timing<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$ CC/SR	20 + 0.1 * C <sub>b</sub> <sup>2)</sup>	-	300	ns	
Rise time of both SDA and SCL	$t_2$ CC/SR	20 + 0.1 * C <sub>b</sub>	-	300	ns	
Data hold time	$t_3$ CC/SR	0	-	-	μs	
Data set-up time	$t_4$ CC/SR	100	-	-	ns	
LOW period of SCL clock	$t_5$ CC/SR	1.3	-	-	μs	
HIGH period of SCL clock	$t_6$ CC/SR	0.6	-	-	μs	
Hold time for (repeated) START condition	$t_7$ CC/SR	0.6	-	-	μs	
Set-up time for repeated START condition	$t_8$ CC/SR	0.6	-	-	μs	
Set-up time for STOP condition	$t_9$ CC/SR	0.6	-	-	μs	
Bus free time between a STOP and START condition	$t_{10}$ CC/SR	1.3	-	-	μs	
Capacitive load for each bus line	C <sub>b</sub> SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C<sub>b</sub> refers to the total capacitance of one bus line in pF.



**Figure 23 USIC IIC Stand and Fast Mode Timing**

### 3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 31 USIC IIS Master Transmitter Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_1$ CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3\text{ V}$
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3\text{ V}$
Clock HIGH	$t_2$ CC	$0.35 \times t_{1min}$	-	-	ns	
Clock Low	$t_3$ CC	$0.35 \times t_{1min}$	-	-	ns	
Hold time	$t_4$ CC	0	-	-	ns	
Clock rise time	$t_5$ CC	-	-	$0.15 \times t_{1min}$	ns	

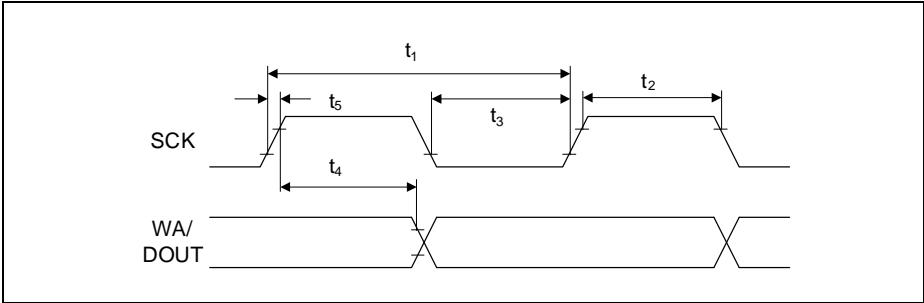


Figure 24 USIC IIS Master Transmitter Timing

Table 32 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_6$ SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	$t_7$ SR	$0.35 \times t_{6min}$	-	-	ns	
Clock Low	$t_8$ SR	$0.35 \times t_{6min}$	-	-	ns	
Set-up time	$t_9$ SR	$0.2 \times t_{6min}$	-	-	ns	
Hold time	$t_{10}$ SR	10	-	-	ns	

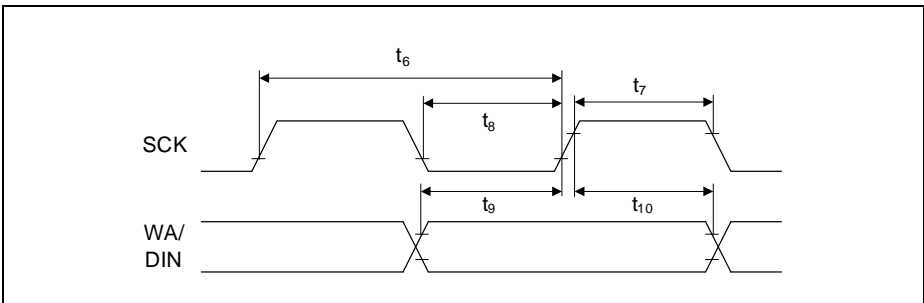


Figure 25 USIC IIS Slave Receiver Timing

## 4 Package and Reliability

The XMC1300 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

### 4.1 Package Parameters

**Table 33** provides the thermal characteristics of the packages used in XMC1300.

**Table 33 Thermal Characteristics of the Packages**

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8 <sup>1)</sup>
		-	83.2	K/W	PG-TSSOP-28-16 <sup>1)</sup>
		-	70.3	K/W	PG-TSSOP-38-9 <sup>1)</sup>
		-	46.0	K/W	PG-VQFN-24-19 <sup>1)</sup>
		-	38.4	K/W	PG-VQFN-40-13 <sup>1)</sup>

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

*Note: For electrical reasons, it is required to connect the exposed pad to the board ground  $V_{SSP}$ , independent of EMC and thermal requirements.*

#### 4.1.1 Thermal Considerations

When operating the XMC1300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance  $R_{\theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by

$$\Delta T = (P_{\text{INT}} + P_{\text{IOSTAT}} + P_{\text{IODYN}}) \times R_{\Theta\text{JA}}$$

The internal power consumption is defined as

$$P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

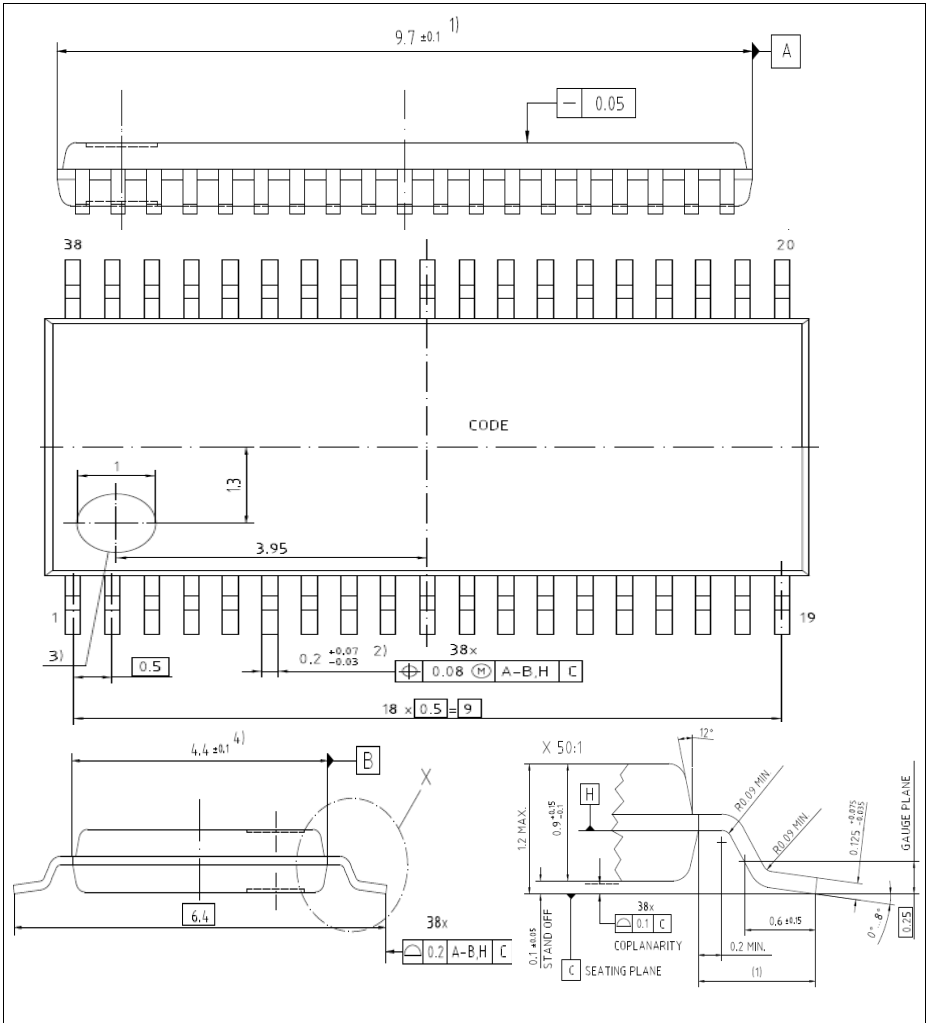
$$P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}} - V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$$

The dynamic external power consumption caused by the output drivers ( $P_{\text{IODYN}}$ ) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce  $V_{\text{DDP}}$ , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

**4.2 Package Outlines**



**Figure 26 PG-TSSOP-38-9**







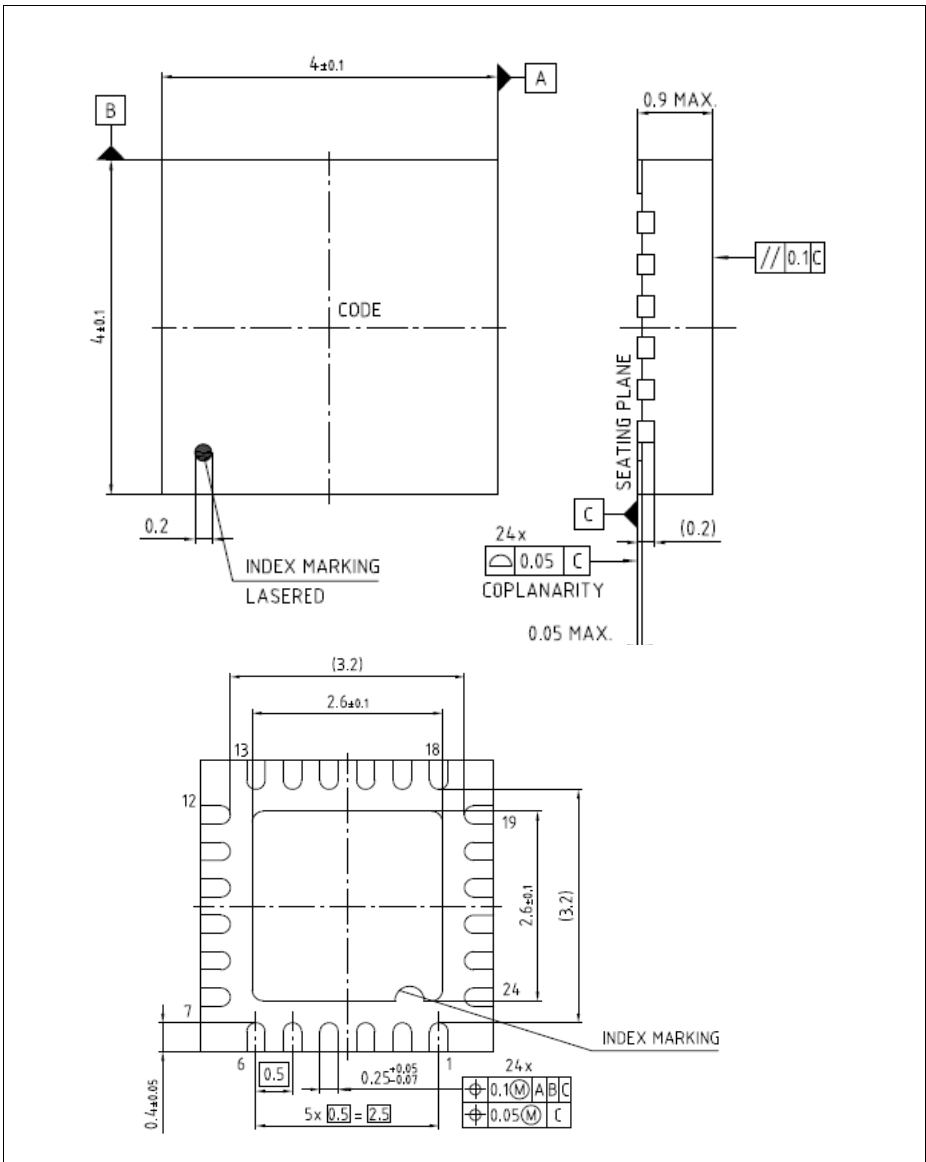
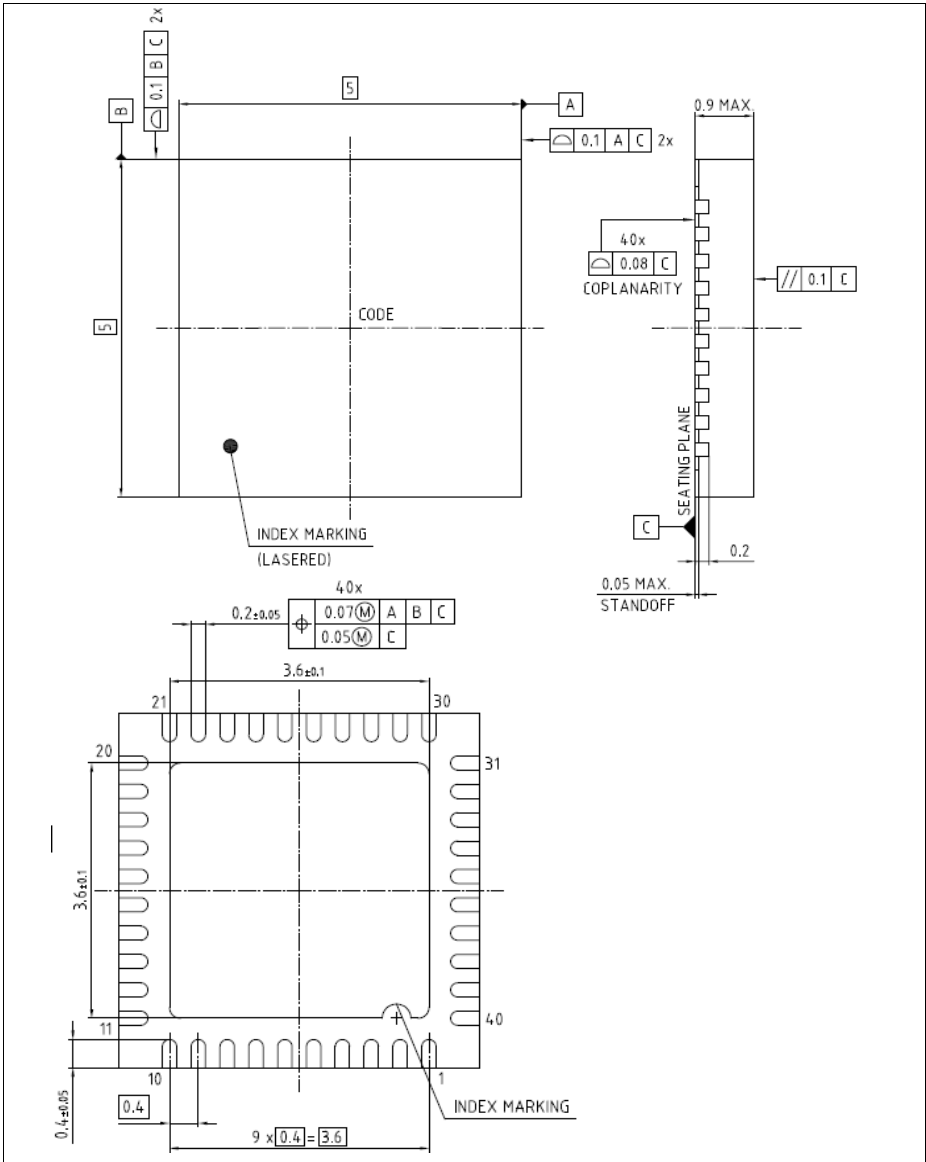


Figure 29 PG-VQFN-24-19



**Figure 30 PG-VQFN-40-13**

All dimensions in mm.

## 5 Quality Declaration

**Table 34** shows the characteristics of the quality parameters in the XMC1300.

**Table 34 Quality Parameters**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	$V_{\text{HBM}}$ SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	$V_{\text{CDM}}$ SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	$MSL$ CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	$T_{\text{SDR}}$ SR	-	260	°C	Profile according to JEDEC J-STD-020D

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[STM32F417VGT6TR](#) [STM32F358CCT6](#) [STM32F302RBT7](#) [MKE06Z64VLD4](#) [MKE04Z128VLD4](#) [MKE02Z16VLC2R](#)  
[MK22FN1M0AVLK12R](#) [MK20DX256VLQ10R](#) [MAX32630IWG+T](#) [MAX32630ICQ+](#) [SIM3L167-C-GQR](#) [STM32L053R6H6](#)  
[STM32L052K8U6](#) [STM32L052K8T7](#)