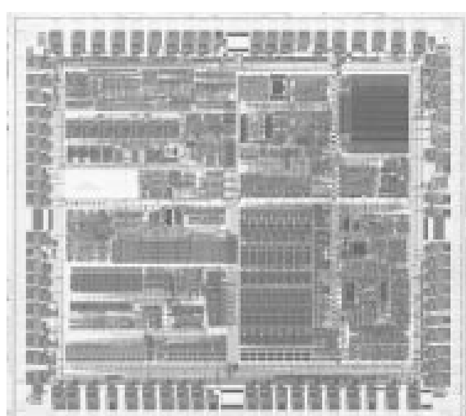
80C186XL/80C188XL
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSORS

- **Low Power, Fully Static Versions of 80C186/80C188**
- **Operation Modes:**
  - **— Enhanced Mode**
    - **— DRAM Refresh Control Unit**
    - **— Power-Save Mode**
    - **— Direct Interface to 80C187 (80C186XL Only)**
  - **— Compatible Mode**
    - **— NMOS 80186/80188 Pin-for-Pin Replacement for Non-Numerics Applications**
- **Integrated Feature Set**
  - **— Static, Modular CPU**
  - **— Clock Generator**
  - **— 2 Independent DMA Channels**
  - **— Programmable Interrupt Controller**
  - **— 3 Programmable 16-Bit Timers**
  - **— Dynamic RAM Refresh Control Unit**
  - **— Programmable Memory and Peripheral Chip Select Logic**
  - **— Programmable Wait State Generator**
  - **— Local Bus Controller**
  - **— Power-Save Mode**
  - **— System-Level Testing Support (High Impedance Test Mode)**
- **Completely Object Code Compatible with Existing 8086/8088 Software and Has 10 Additional Instructions over 8086/8088**
- **Speed Versions Available**
  - **— 25 MHz (80C186XL25/80C188XL25)**
  - **— 20 MHz (80C186XL20/80C188XL20)**
  - **— 12 MHz (80C186XL12/80C188XL12)**
- **Direct Addressing Capability to 1 MByte Memory and 64 Kbyte I/O**
- **Available in 68-Pin:**
  - **— Plastic Leaded Chip Carrier (PLCC)**
  - **— Ceramic Pin Grid Array (PGA)**
  - **— Ceramic Leadless Chip Carrier (JEDEC A Package)**
- **Available in 80-Pin:**
  - **— Quad Flat Pack (EIAJ)**
  - **— Shrink Quad Flat Pack (SGFP)**
- **Available in Extended Temperature Range (−40°C to +85°C)**

The Intel 80C186XL is a Modular Core re-implementation of the 80C186 microprocessor. It offers higher speed and lower power consumption than the standard 80C186 but maintains 100% clock-for-clock functional compatibility. Packaging and pinout are also identical.



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June, 2002 **Order Number: 272431-005**

80C186XL/80C188XL
16-Bit High-Integration Embedded Processors

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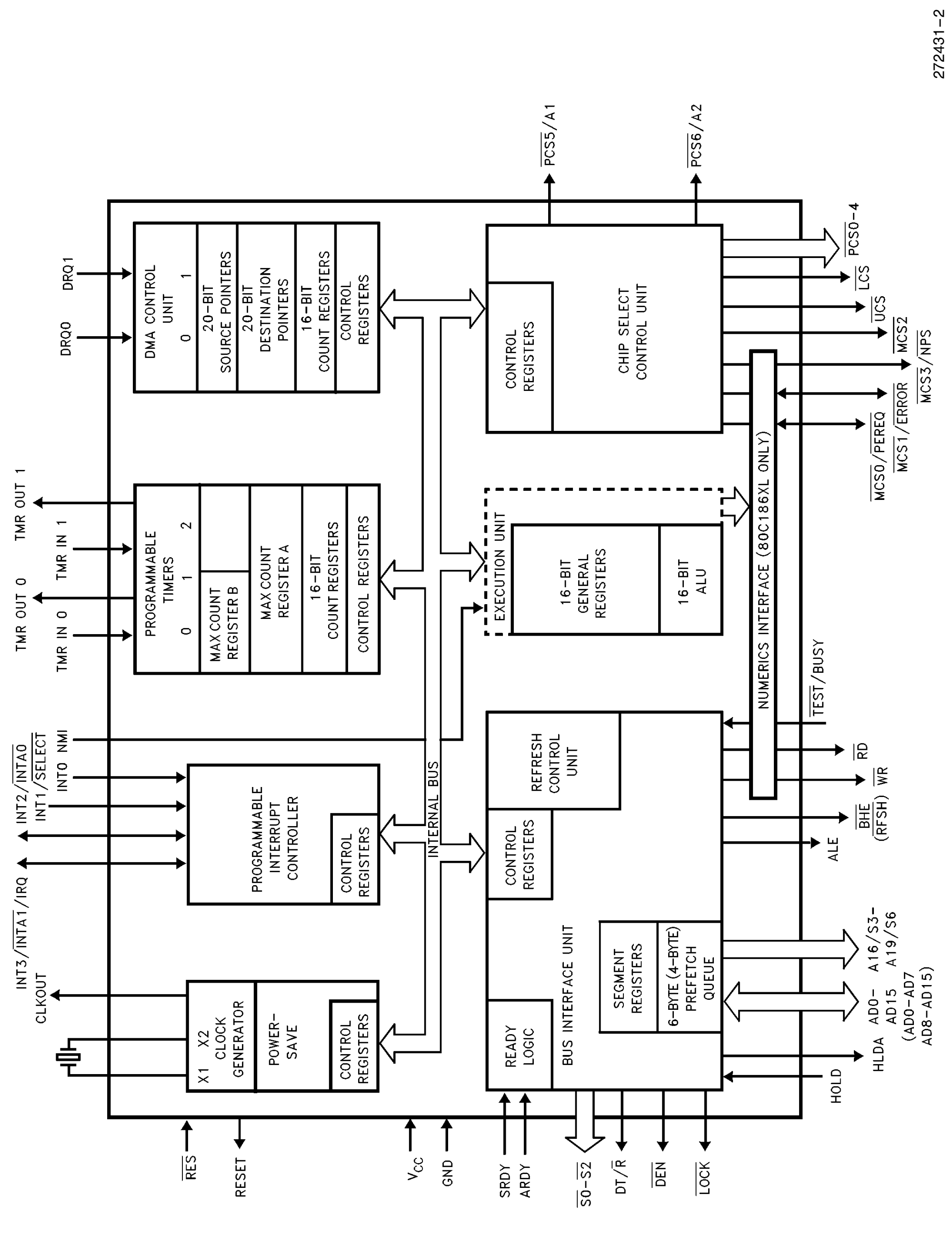
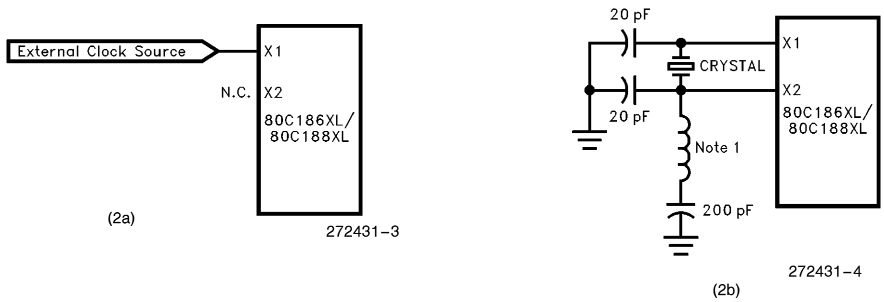


NOTE:
Pin names in parentheses applies to 80C188XL.

Figure 1. 80C186XL/80C188XL Block Diagram



Note 1:

XTAL Frequency	L1 Value
20 MHz	12.0 μH ±20%
25 MHz	8.2 μH ±20%
32 MHz	4.7 μH ±20%
40 MHz	3.0 μH ±20%

LC network is only required when using a third overtone crystal.

Figure 2. Oscillator Configurations (see text)

INTRODUCTION

Unless specifically noted, all references to the 80C186XL apply to the 80C188XL. References to pins that differ between the 80C186XL and the 80C188XL are given in parentheses.

The following Functional Description describes the base architecture of the 80C186XL. The 80C186XL is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip. The 80C186XL is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

The 80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode the 80C186XL is completely compatible with NMOS 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface (80C186XL only).

80C186XL CORE ARCHITECTURE

80C186XL Clock Generator

The 80C186XL provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

The 80C186XL oscillator circuit is designed to be used either with a parallel resonant fundamental or third-overtone mode crystal, depending upon the frequency range of the application. This is used as the time base for the 80C186XL.

The output of the oscillator is not directly available outside the 80C186XL. The recommended crystal configuration is shown in Figure 2b. When used in third-overtone mode, the tank circuit is recommended for stable operation. Alternately, the oscillator may be driven from an external source as shown in Figure 2a.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide by two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC Timings are referenced to CLKOUT.

Intel recommends the following values for crystal selection parameters.

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pF max
C_1 (Load Capacitance):	20 pF ±2 pF
Drive Level:	2 mW max

Bus Interface Unit

The 80C186XL provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the local bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C186XL bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

During RESET the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$ and $\overline{WR}$ HIGH for one clock cycle, then float them.
- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–15 (AD0–8), A16–19 (A9–A19), $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$.
- Drive ALE LOW
- Drive HLDA LOW.

$\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$ and $\overline{TEST}$/BUSY pins have internal pullup devices which are active while $\overline{RES}$ is applied. Excessive loading or grounding certain of these pins causes the 80C186XL to enter an alternative mode of operation:

- $\overline{RD}$/$\overline{QSMD}$ low results in Queue Status Mode.
- $\overline{UCS}$ and $\overline{LCS}$ low results in ONCE Mode.
- $\overline{TEST}$/BUSY low (and high later) results in Enhanced Mode.

80C186XL PERIPHERAL ARCHITECTURE

All the 80C186XL integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. An offset map of the 256-byte control register block is shown in Figure 3.

Chip-Select/Ready Generation Logic

The 80C186XL contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

The 80C186XL provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

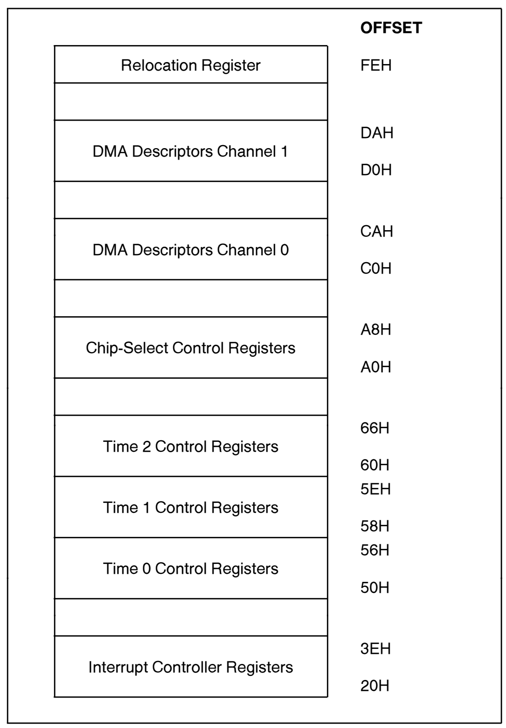


Figure 3. Internal Register Map

The 80C186XL provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80C186XL begins executing at memory location FFFF0H.

The 80C186XL provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The 80C186XL provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80C186XL 1 Mbyte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The 80C186XL can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

The 80C186XL can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80C186XL may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers.

DMA Unit

The 80C186XL DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses.

NOTE:
Only byte transfers are possible on the 80C188XL.

Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data.

Timer/Counter Unit

The 80C186XL provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

Interrupt Control Unit

The 80C186XL can receive interrupts from a number of sources, both internal and external. The 80C186XL has 5 external and 2 internal interrupt sources (Timer/Couners and DMA). The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Enhanced Mode Operation

In Compatible Mode the 80C186XL operates with all the features of the NMOS 80186, with the exception of 8087 support (i.e. no math coprocessing is possible in Compatible Mode). Queue-Status information is still available for design purposes other than 8087 support.

All the Enhanced Mode features are completely masked when in Compatible Mode. A write to any of the Enhanced Mode registers will have no effect, while a read will not return any valid data.

In Enhanced Mode, the 80C186XL will operate with Power-Save, DRAM refresh, and numerics coprocessor support (80C186XL only) in addition to all the Compatible Mode features.

If connected to a math coprocessor (80C186XL only), this mode will be invoked automatically. Without an NPX, this mode can be entered by tying the $\overline{RESET}$ output signal from the 80C186XL to the $\overline{TEST}$/BUSY input.

Queue-Status Mode

The queue-status mode is entered by strapping the $\overline{RD}$ pin low. $\overline{RD}$ is sampled at RESET and if LOW, the 80C186XL will reconfigure the ALE and $\overline{WR}$ pins to be QS0 and QS1 respectively. This mode is available on the 80C186XL in both Compatible and Enhanced Modes.

DRAM Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle.

Power-Save Control

The 80C186XL, when in Enhanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin.

All internal logic, including the Refresh Control Unit and the timers, have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

Interface for 80C187 Math Coprocessor (80C186XL Only)

In Enhanced Mode, three of the mid-range memory chip selects are redefined according to Table 1 for use with the 80C187. The fourth chip select, $\overline{\text{MCS2}}$ functions as in compatible mode, and may be programmed for activity with ready logic and wait states accordingly. As in Compatible Mode, $\overline{\text{MCS2}}$ will function for one-fourth a programmed block size.

Table 1. $\overline{\text{MCS}}$ Assignments

Compatible Mode	Enhanced Mode	
$\overline{\text{MCS0}}$	PEREQ	Processor Extension Request
$\overline{\text{MCS1}}$	$\overline{\text{ERROR}}$	NPX Error
$\overline{\text{MCS2}}$	$\overline{\text{MCS2}}$	Mid-Range Chip Select
$\overline{\text{MCS3}}$	$\overline{\text{NPS}}$	Numeric Processor Select

ONCE Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186XL has a test mode available which allows all pins to be placed in a high-impedance state. ONCE stands for "ON Circuit Emulation". When placed in this mode, the 80C186XL will put all pins in the high-impedance state until RESET.

The ONCE mode is selected by tying the $\overline{\text{UCS}}$ and the $\overline{\text{LCS}}$ LOW during RESET. These pins are sampled on the low-to-high transition of the $\overline{\text{RES}}$ pin. The $\overline{\text{UCS}}$ and the $\overline{\text{LCS}}$ pins have weak internal pull-up resistors similar to the $\overline{\text{RD}}$ and $\overline{\text{TEST}}$/BUSY pins to guarantee ONCE Mode is not entered inadvertently during normal operation. $\overline{\text{LCS}}$ and $\overline{\text{UCS}}$ must be held low at least one clock after $\overline{\text{RES}}$ goes high to guarantee entrance into ONCE Mode.

PACKAGE INFORMATION

This section describes the pin functions, pinout and thermal characteristics for the 80C186XL in the Quad Flat Pack (QFP), Plastic Leaded Chip Carrier (PLCC), Leadless Chip Carrier (LCC) and the Shrink Quad Flat Pack (SQFP). For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 3. There are four columns for each entry in the Pin Description Table. The following sections describe each column.

Column 1: Pin Name

In this column is a mnemonic that describes the pin function. Negation of the signal name (i.e., $\overline{\text{RESIN}}$) implies that the signal is active low.

Column 2: Pin Type

A pin may be either power (P), ground (G), input only (I), output only (O) or input/output (I/O). Please note that some pins have more than one function.

Column 3: Input Type (for I and I/O types only)

These are two different types of input pins on the 80C186XL: asynchronous and synchronous. **Asynchronous** pins require that setup and hold times be met only to *guarantee recognition.* **Synchronous** input pins require that the setup and hold times be met to *guarantee proper operation.* Stated simply, missing a setup or hold on an asynchronous pin will result in something minor (i.e., a timer count will be missed) whereas missing a setup or hold on a synchronous pin result in system failure (the system will "lock up").

An input pin may also be edge or level sensitive.

Column 4: Output States (for O and I/O types only)

The state of an output or I/O pin is dependent on the operating mode of the device. There are four modes of operation that are different from normal active mode: Bus Hold, Reset, Idle Mode, Powerdown Mode. This column describes the output pin state in each of these modes.

The legend for interpreting the information in the Pin Descriptions is shown in Table 2.

As an example, please refer to the table entry for AD7:0. The "I/O" signifies that the pins are bidirectional (i.e., have both an input and output function). The "S" indicates that, as an input the signal must be synchronized to CLKOUT for proper operation. The "H(Z)" indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low.

All pins float while the processor is in the ONCE Mode (with the exception of X2).

Table 2. Pin Description Nomenclature

Symbol	Description
P	Power Pin (apply + V_{CC} voltage)
G	Ground (connect to V_{SS})
I	Input only pin
O	Output only pin
I/O	Input/Output pin
S(E)	Synchronous, edge sensitive
S(L)	Synchronous, level sensitive
A(E)	Asynchronous, edge sensitive
A(L)	Asynchronous, level sensitive
H(1)	Output driven to V_{CC} during bus hold
H(0)	Output driven to V_{SS} during bus hold
H(Z)	Output floats during bus hold
H(Q)	Output remains active during bus hold
H(X)	Output retains current state during bus hold
R(WH)	Output weakly held at V_{CC} during reset
R(1)	Output driven to V_{CC} during reset
R(0)	Output driven to V_{SS} during reset
R(Z)	Output floats during reset
R(Q)	Output remains active during reset
R(X)	Output retains current state during reset

Table 3. Pin Descriptions

Pin Name	Pin Type	Input Type	Output States	Pin Description
V_{CC}	P			System Power: +5 volt power supply.
V_{SS}	G			System Ground.
RESET	O		H(0) R(1)	RESET Output indicates that the CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{\text{RES}}$ signal. Reset goes inactive 2 clockout periods after $\overline{\text{RES}}$ goes inactive. When tied to the $\overline{\text{TEST}}$/BUSY pin, RESET forces the processor into enhanced mode. RESET is not floated during bus hold.
X1	I	A(E)		Crystal Inputs X1 and X2 provide external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can connect to an external clock instead of a crystal. In this case, minimize the capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
X2	O		H(Q) R(Q)	
CLKOUT	O		H(Q) R(Q)	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT is active during reset and bus hold.
$\overline{\text{RES}}$	I	A(L)		An active $\overline{\text{RES}}$ causes the processor to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the clock. The processor begins fetching instructions approximately 6½ clock cycles after $\overline{\text{RES}}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{\text{RES}}$ held LOW. $\overline{\text{RES}}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{\text{RES}}$ generation via an RC network.
$\overline{\text{TEST}}$/BUSY ($\overline{\text{TEST}}$)	I	A(E)		The $\overline{\text{TEST}}$ pin is sampled during and after reset to determine whether the processor is to enter Compatible or Enhanced Mode. Enhanced Mode requires $\overline{\text{TEST}}$ to be HIGH on the rising edge of $\overline{\text{RES}}$ and LOW four CLKOUT cycles later. Any other combination will place the processor in Compatible Mode. During power-up, active $\overline{\text{RES}}$ is required to configure $\overline{\text{TEST}}$/BUSY as an input. A weak internal pullup ensures a HIGH state when the input is not externally driven. $\overline{\text{TEST}}$—In Compatible Mode this pin is configured to operate as $\overline{\text{TEST}}$. This pin is examined by the WAIT instruction. If the $\overline{\text{TEST}}$ input is HIGH when WAIT execution begins, instruction execution will suspend. $\overline{\text{TEST}}$ will be resampled every five clocks until it goes LOW, at which time execution will resume. If interrupts are enabled while the processor is waiting for $\overline{\text{TEST}}$, interrupts will be serviced. BUSY (80C186XL Only)—In Enhanced Mode, this pin is configured to operate as BUSY. The BUSY input is used to notify the 80C186XL of Math Coprocessor activity. Floating point instructions executing in the 80C186XL sample the BUSY pin to determine when the Math Coprocessor is ready to accept a new command. BUSY is active HIGH.

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 3. Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
TMR IN 0 TMR IN 1	I	A(L) A(E)		Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. Timer Inputs must be tied HIGH when not being used as clock or retrigger inputs.
TMR OUT 0 TMR OUT 1	O		H(Q) R(1)	Timer outputs are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected. These outputs are not floated during a bus hold.
DRQ0 DRQ1	I	A(L)		DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	I	A(E)		The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one CLKOUT period. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{SELECT}$	I	A(E) A(L)		Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$/IRQ	I/O	A(E) A(L)	H(1) R(Z)	
A19/S6 A18/S5 A17/S4 A16/S3 (A8–A15)	O		H(Z) R(Z)	Address Bus Outputs and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated or refresh bus cycle. During the same T-states, S3, S4 and S5 are always LOW. On the 80C188XL, A15–A8 provide valid address information for the entire bus cycle.
AD0–AD15 (AD0–AD7)	I/O	S(L)	H(Z) R(Z)	Address/Data Bus signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W and T_4) bus. The bus is active HIGH. For the 80C186XL, A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 3. Pin Descriptions (Continued)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Input Type</th><th>Output States</th><th colspan="3">Pin Description</th></tr>
<tr><td rowspan="7">$\overline{BHE}$
($\overline{RFSH}$)</td><td rowspan="7">O</td><td rowspan="7"></td><td rowspan="7">H(Z)
R(Z)</td><td colspan="3">The $\overline{BHE}$ (Bus High Enable) signal is analogous to A0 in that it is used to enable data on to the most significant half of the data bus, pins D15–D8. $\overline{BHE}$ will be LOW during T_1 when the upper byte is transferred and will remain LOW through T_3 and T_W. $\overline{BHE}$ does not need to be latched. On the 80C188XL, $\overline{RFSH}$ is asserted LOW to indicate a refresh bus cycle.
In Enhanced Mode, $\overline{BHE}$ ($\overline{RFSH}$) will also be used to signify DRAM refresh cycles. A refresh cycle is indicated by both $\overline{BHE}$ ($\overline{RFSH}$) and A0 being HIGH.</td></tr>
<tr><th colspan="3">80C186XL $\overline{BHE}$ and A0 Encodings</th></tr>
<tr><th>$\overline{BHE}$ Value</th><th>A0 Value</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Byte Transfer on upper half of data bus (D15–D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte Transfer on lower half of data bus (D_7–D_0)</td></tr>
<tr><td>1</td><td>1</td><td>Refresh</td></tr>
<tr><td>ALE/QS0</td><td>O</td><td></td><td>H(0)
R(0)</td><td colspan="3">Address Latch Enable/Queue Status 0 is provided by the processor to latch the address. ALE is active HIGH, with addresses guaranteed valid on the trailing edge.</td></tr>
<tr><td rowspan="6">$\overline{WR}$/QS1</td><td rowspan="6">O</td><td rowspan="6"></td><td rowspan="6">H(Z)
R(Z)</td><td colspan="3">Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. It is active LOW. When the processor is in Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.</td></tr>
<tr><th>QS1</th><th>QS0</th><th>Queue Operation</th></tr>
<tr><td>0</td><td>0</td><td>No queue operation</td></tr>
<tr><td>0</td><td>1</td><td>First opcode byte fetched from the queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent byte fetched from the queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the queue</td></tr>
<tr><td>$\overline{RD}$/$\overline{QSMD}$</td><td>O</td><td></td><td>H(Z)
R(1)</td><td colspan="3">Read Strobe is an active LOW signal which indicates that the processor is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$/$\overline{QSMD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the processor is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND.</td></tr>
<tr><td>ARDY</td><td>I</td><td>A(L)
S(L)</td><td></td><td colspan="3">Asynchronous Ready informs the processor that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the processor clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.</td></tr>
</table>

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 3. Pin Descriptions (Continued)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Input Type</th><th>Output States</th><th>Pin Description</th></tr>
<tr><td>SRDY</td><td>I</td><td>S(L)</td><td>—</td><td>Synchronous Ready informs the processor that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchonize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>O</td><td>—</td><td>H(Z)
R(Z)</td><td>$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus. $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction immediately following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted.</td></tr>
<tr><td>$\overline{S0}$
$\overline{S1}$
$\overline{S2}$</td><td>O</td><td>—</td><td>H(Z)
R(1)</td><td>Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information:
<table>
<tr><th colspan="4">Bus Cycle Status Information</th></tr>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Data from Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Data to Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (no bus cycle)</td></tr>
</table>
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.</td></tr>
<tr><td>HOLD</td><td>I</td><td>A(L)</td><td>—</td><td rowspan="2">HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. The processor generates HLDA (HIGH) in response to a HOLD request. Simultaneous with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA. When the processor needs to run another bus cycle, it will again drive the local bus and control lines.

In Enhanced Mode, HLDA will go low when a DRAM refresh cycle is pending in the processor and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the processor may execute the refresh cycle.</td></tr>
<tr><td>HLDA</td><td>O</td><td>—</td><td>H(1)
R(0)</td></tr>
</table>

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 3. Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
$\overline{UCS}$	I/O	A(L)	H(1) R(WH)	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. The address range activating $\overline{UCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the processor will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has a weak internal pullup that is active during RESET to ensure that the processor does not enter ONCE Mode inadvertently.
$\overline{LCS}$	I/O	A(L)	H(1) R(WH)	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. The address range activating $\overline{LCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the processor will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{LCS}$ has a weak internal pullup that is active only during RESET to ensure that the processor does not enter ONCE mode inadvertently.
$\overline{MCS0}$/PEREQ $\overline{MCS1}$/$\overline{ERROR}$	I/O	A(L)	H(1) R(WH)	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). The address ranges activating $\overline{MCS0-3}$ are software programmable. On the 80C186XL, in Enhanced Mode, $\overline{MCS0}$ becomes a PEREQ input (Processor Extension Request). When connected to the Math Coprocessor, this input is used to signal the 80C186XL when to make numeric data transfers to and from the coprocessor. $\overline{MCS3}$ becomes $\overline{NPS}$ (Numeric Processor Select) which may only be activated by communication to the 80C187. $\overline{MCS1}$ becomes $\overline{ERROR}$ in Enhanced Mode and is used to signal numerics coprocessor errors.
$\overline{MCS2}$ $\overline{MCS3}$/$\overline{NPS}$	O		H(1) R(1)	
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	O		H(1) R(1)	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64 Kbyte I/O or 1 MByte memory space). The address ranges activating $\overline{PCS0-4}$ are software programmable.
$\overline{PCS5}$/A1	O		H(1)/H(X) R(1)	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.

NOTE:
Pin names in parentheses apply to the 80C188XL.

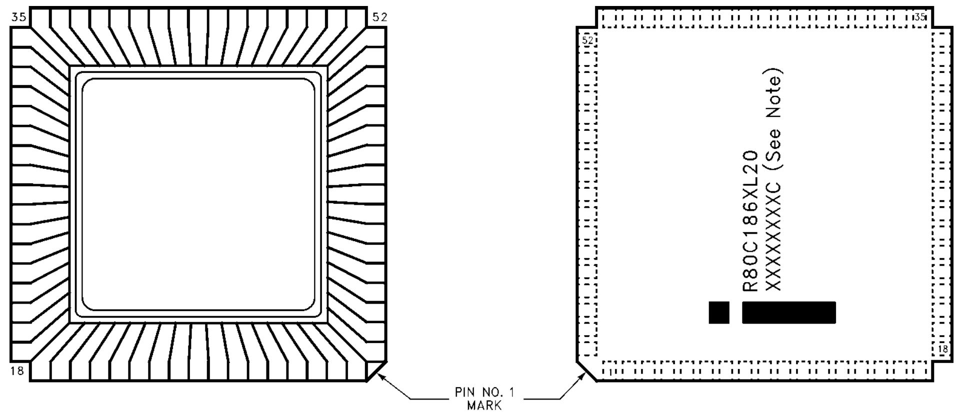
Table 3. Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
$\overline{PCS6}$/A2	O	—	H(1)/H(X) R(1)	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	O	—	H(Z) R(Z)	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the procesor. When HIGH the processor places write data on the data bus.
$\overline{DEN}$	O	—	H(Z) R(1,Z)	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access (including 80C187 access). $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated.
N.C.	—	—	—	Not connected. To maintain compatibility with future products, do not connect to these pins.

NOTE:
Pin names in parentheses apply to the 80C188XL.

Ceramic Leadless Chip Carrier (JEDEC Type A)

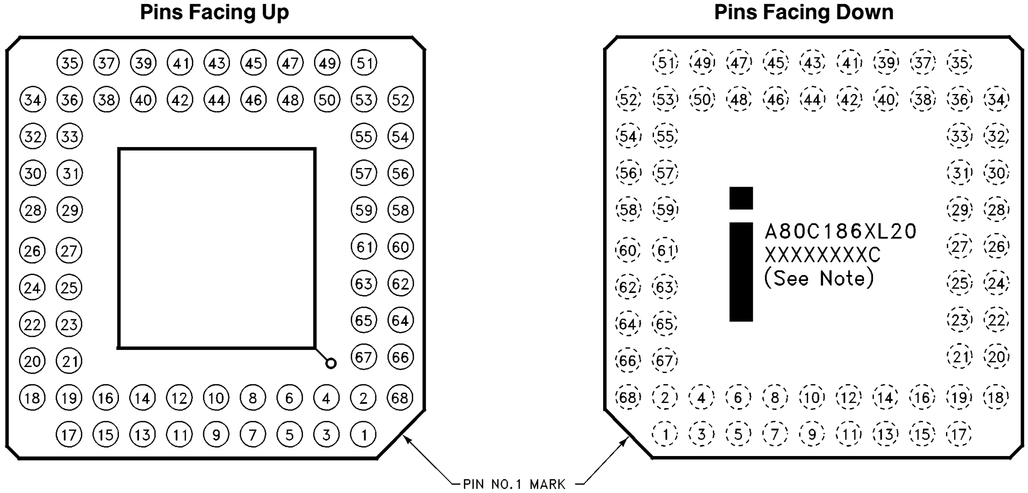
Contacts Facing Up / **Contacts Facing Down**



272431–5

Ceramic Pin Grid Array

Pins Facing Up / **Pins Facing Down**

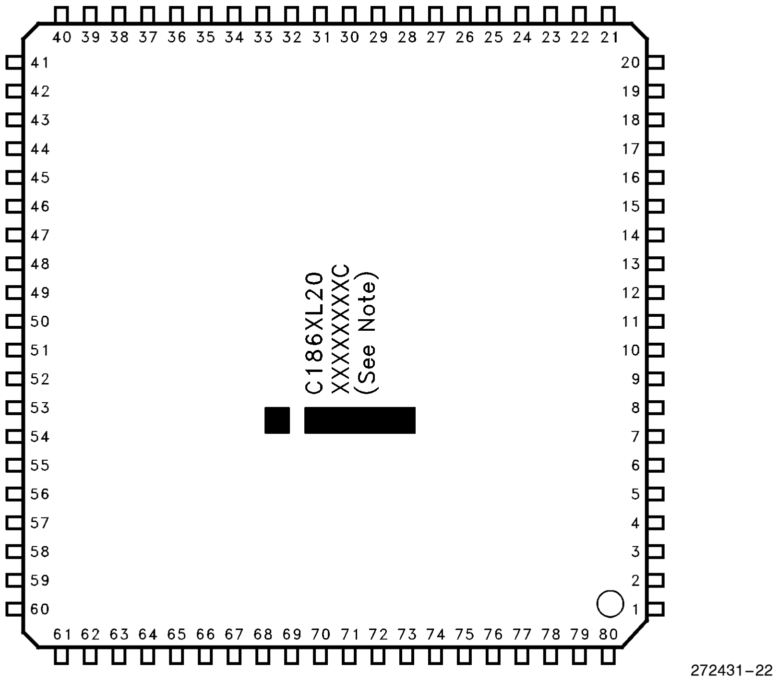


272431–6

NOTE:
XXXXXXXXC indicates the Intel FPO number.

Figure 4. 80C186XL/80C188XL Pinout Diagrams

Shrink Quad Flat Pack

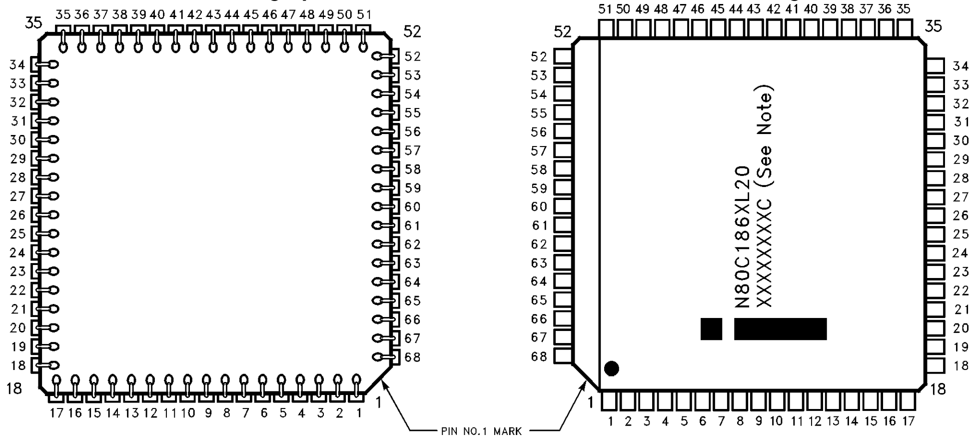


NOTE:
XXXXXXXXC indicates the Intel FPO number.

Figure 4. 80C186XL/80C188XL Pinout Diagrams (Continued)

Plastic Leaded Chip Carrier

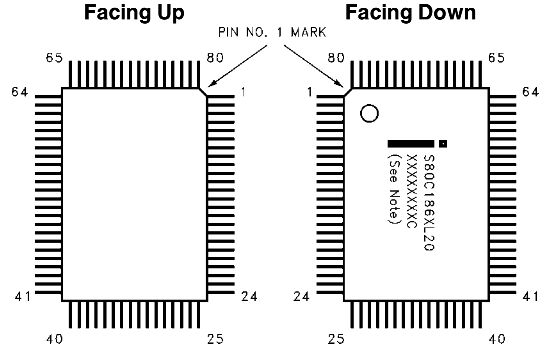
Contacts Facing Up | **Contacts Facing Down**



272431–7

80-Pin Quad Flat Pack (EIAJ)

Contacts Facing Up | **Contacts Facing Down**



272431–8

NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 4. 80C186XL/80C288XL Pinout Diagrams (Continued)

Table 4. LCC/PLCC Pin Functions with Location

AD Bus	
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
AD8 (A8)	16
AD9 (A9)	14
AD10 (A10)	12
AD11 (A11)	10
AD12 (A12)	7
AD13 (A13)	5
AD14 (A14)	3
AD15 (A15)	1
A16/S3	68
A17/S4	67
A18/S5	66
A19/S6	65

Bus Control	
ALE/QS0	61
$\overline{BHE}$ ($\overline{RFSH}$)	64
$\overline{S0}$	52
$\overline{S1}$	53
$\overline{S2}$	54
$\overline{RD}$/$\overline{QSMD}$	62
$\overline{WR}$/QS1	63
ARDY	55
SRDY	49
$\overline{DEN}$	39
DT/$\overline{R}$	40
$\overline{LOCK}$	48
HOLD	50
HLDA	51

Processor Control	
$\overline{RES}$	24
RESET	57
X1	59
X2	58
CLKOUT	56
$\overline{TEST}$/BUSY	47
NMI	46
INT0	45
INT1/$\overline{SELECT}$	44
INT2/$\overline{INTA0}$	42
INT3/$\overline{INTA1}$	41

Power and Ground	
V_{CC}	9
V_{CC}	43
V_{SS}	26
V_{SS}	60

I/O	
$\overline{UCS}$	34
$\overline{LCS}$	33
$\overline{MCS0}$/PEREQ	38
$\overline{MCS1}$/$\overline{ERROR}$	37
$\overline{MCS2}$	36
$\overline{MCS3}$/$\overline{NPS}$	35
$\overline{PCS0}$	25
$\overline{PCS1}$	27
$\overline{PCS2}$	28
$\overline{PCS3}$	29
$\overline{PCS4}$	30
$\overline{PCS5}$/A1	31
$\overline{PCS6}$/A2	32
TMR IN 0	20
TMR IN 1	21
TMR OUT 0	22
TMR OUT 1	23
DRQ0	18
DRQ1	19

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 5. LCC/PGA/PLCC Pin Locations with Pin Names

1	AD15 (A15)	18	DRQ0	35	$\overline{MCS3}$/$\overline{NPS}$	52	$\overline{S0}$
2	AD7	19	DRQ1	36	$\overline{MCS2}$	53	$\overline{S1}$
3	AD14 (A14)	20	TMR IN 0	37	$\overline{MCS1}$/$\overline{ERROR}$	54	$\overline{S2}$
4	AD6	21	TMR IN 1	38	$\overline{MCS0}$/PEREQ	55	ARDY
5	AD13 (A13)	22	TMR OUT 0	39	$\overline{DEN}$	56	CLKOUT
6	AD5	23	TMR OUT 1	40	DT/$\overline{R}$	57	RESET
7	AD12 (A12)	24	$\overline{RES}$	41	INT3/$\overline{INTA1}$	58	X2
8	AD4	25	$\overline{PCS0}$	42	INT2/$\overline{INTA0}$	59	X1
9	V_{CC}	26	V_{SS}	43	V_{CC}	60	V_{SS}
10	AD11 (A11)	27	$\overline{PCS1}$	44	INT1/$\overline{SELECT}$	61	ALE/QS0
11	AD3	28	$\overline{PCS2}$	45	INT0	62	$\overline{RD}$/$\overline{QSMD}$
12	AD10 (A10)	29	$\overline{PCS3}$	46	NMI	63	$\overline{WR}$/QS1
13	AD2	30	$\overline{PCS4}$	47	$\overline{TEST}$/BUSY	64	$\overline{BHE}$ ($\overline{RFSH}$)
14	AD9 (A9)	31	$\overline{PCS5}$/A1	48	$\overline{LOCK}$	65	A19/S2
15	AD1	32	$\overline{PCS6}$/A2	49	SRDY	66	A18/S3
16	AD8 (A8)	33	$\overline{LCS}$	50	HOLD	67	A17/S4
17	AD0	34	$\overline{UCS}$	51	HLDA	68	A16/S3

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 6. QFP Pin Functions with Location

AD Bus	
AD0	64
AD1	66
AD2	68
AD3	70
AD4	74
AD5	76
AD6	78
AD7	80
AD8 (A8)	65
AD9 (A9)	67
AD10 (A10)	69
AD11 (A11)	71
AD12 (A12)	75
AD13 (A13)	77
AD14 (A14)	79
AD15 (A15)	1
A16/S3	3
A17/S4	4
A18/S5	5
A19/S6	6

Bus Control	
ALE/QS0	10
$\overline{BHE}$ ($\overline{RFSH}$)	7
$\overline{S0}$	23
$\overline{S1}$	22
$\overline{S2}$	21
$\overline{RD}$/$\overline{QSMD}$	9
$\overline{WR}$/QS1	8
ARDY	20
SRDY	27
$\overline{DEN}$	38
DT/$\overline{R}$	37
$\overline{LOCK}$	28
HOLD	26
HLDA	25

No Connection	
N.C.	2
N.C.	11
N.C.	14
N.C.	15
N.C.	24
N.C.	43
N.C.	44
N.C.	62
N.C.	63

Processor Control	
$\overline{RES}$	55
RESET	18
X1	16
X2	17
CLKOUT	19
$\overline{TEST}$/BUSY	29
NMI	30
INT0	31
INT1/$\overline{SELECT}$	32
INT2/$\overline{INTA0}$	35
INT3/$\overline{INTA1}$	36

Power and Ground	
V_{CC}	33
V_{CC}	34
V_{CC}	72
V_{CC}	73
V_{SS}	12
V_{SS}	13
V_{SS}	53

I/O	
$\overline{UCS}$	45
$\overline{LCS}$	46
$\overline{MCS0}$/PEREQ	39
$\overline{MCS1}$/$\overline{ERROR}$	40
$\overline{MCS2}$	41
$\overline{MCS3}$/$\overline{NPS}$	42
$\overline{PCS0}$	54
$\overline{PCS1}$	52
$\overline{PCS2}$	51
$\overline{PCS3}$	50
$\overline{PCS4}$	49
$\overline{PCS5}$/A1	48
$\overline{PCS6}$/A2	47
TMR IN 0	59
TMR IN 1	58
TMR OUT 0	57
TMR OUT 1	56
DRQ0	61
DRQ1	60

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 7. QFP Pin Locations with Pin Names

1	AD15 (A15)	21	$\overline{S2}$	41	$\overline{MCS2}$	61	DRQ0
2	N.C.	22	$\overline{S1}$	42	$\overline{MCS3}$/$\overline{NPS}$	62	N.C.
3	A16/S3	23	$\overline{S0}$	43	N.C.	63	N.C.
4	A17/S4	24	N.C.	44	N.C.	64	AD0
5	A18/S5	25	HLDA	45	$\overline{UCS}$	65	AD8 (A8)
6	A19/S6	26	HOLD	46	$\overline{LCS}$	66	AD1
7	$\overline{BHE}$/($\overline{RFSH}$)	27	SRDY	47	$\overline{PCS6}$/A2	67	AD9 (A9)
8	$\overline{WR}$/QS1	28	$\overline{LOCK}$	48	$\overline{PCS5}$/A1	68	AD2
9	$\overline{RD}$/$\overline{QSMD}$	29	$\overline{TEST}$/BUSY	49	$\overline{PCS4}$	69	AD10 (A10)
10	ALE/QS0	30	NMI	50	$\overline{PCS3}$	70	AD3
11	N.C.	31	INT0	51	$\overline{PCS2}$	71	AD11 (A11)
12	V_{SS}	32	INT1/$\overline{SELECT}$	52	$\overline{PCS1}$	72	V_{CC}
13	V_{SS}	33	V_{CC}	53	V_{SS}	73	V_{CC}
14	N.C.	34	V_{CC}	54	$\overline{PCS0}$	74	AD4
15	N.C.	35	INT2/$\overline{INTA0}$	55	$\overline{RES}$	75	AD12 (A12)
16	X1	36	INT3/$\overline{INTA1}$	56	TMR OUT 1	76	AD5
17	X2	37	DT/$\overline{R}$	57	TMR OUT 0	77	AD13 (A13)
18	RESET	38	$\overline{DEN}$	58	TMR IN 1	78	AD6
19	CLKOUT	39	$\overline{MCS0}$/PEREQ	59	TMR IN 0	79	AD14 (A14)
20	ARDY	40	$\overline{MCS1}$/$\overline{ERROR}$	60	DRQ1	80	AD7

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 8. SQFP Pin Functions with Location

AD Bus	
AD0	1
AD1	3
AD2	6
AD3	8
AD4	12
AD5	14
AD6	16
AD7	18
AD8 (A8)	2
AD9 (A9)	5
AD10 (A10)	7
AD11 (A11)	9
AD12 (A12)	13
AD13 (A13)	15
AD14 (A14)	17
AD15 (A15)	19
A16/S3	21
A17/S4	22
A18/S5	23
A19/S6	24

Bus Control	
ALE/QS0	29
$\overline{BHE}$ ($\overline{RFSH}$)	26
$\overline{S0}$	40
$\overline{S1}$	39
$\overline{S2}$	38
$\overline{RD}$/$\overline{QSMD}$	28
$\overline{WR}$/QS1	27
ARDY	37
SRDY	44
$\overline{DEN}$	56
DT/$\overline{R}$	54
$\overline{LOCK}$	45
HOLD	43
HLDA	42

No Connection	
N.C.	4
N.C.	25
N.C.	35
N.C.	55
N.C.	72

Processor Control	
$\overline{RES}$	73
RESET	34
X1	32
X2	33
CLKOUT	36
$\overline{TEST}$/BUSY	46
NMI	47
INT0	48
INT1/$\overline{SELECT}$	49
INT2/$\overline{INTA0}$	52
INT3/$\overline{INTA1}$	53

Power and Ground	
V_{CC}	10
V_{CC}	11
V_{CC}	20
V_{CC}	50
V_{CC}	51
V_{CC}	61
V_{SS}	30
V_{SS}	31
V_{SS}	41
V_{SS}	70
V_{SS}	80

I/O	
$\overline{UCS}$	62
$\overline{LCS}$	63
$\overline{MCS0}$/PEREQ	57
$\overline{MCS1}$/$\overline{ERROR}$	58
$\overline{MCS2}$	59
$\overline{MCS3}$/$\overline{NPS}$	60
$\overline{PCS0}$	71
$\overline{PCS1}$	69
$\overline{PCS2}$	68
$\overline{PCS3}$	67
$\overline{PCS4}$	66
$\overline{PCS5}$/A1	65
$\overline{PCS6}$/A2	64
TMR IN 0	77
TMR IN 1	76
TMR OUT 0	75
TMR OUT 1	74
DRQ0	79
DRQ1	78

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 9. SQFP Pin Locations with Pin Names

1	AD0	21	A16/S3	41	V_{SS}	61	V_{CC}
2	AD8 (A8)	22	A17/S4	42	HLDA	62	$\overline{UCS}$
3	AD1	23	A18/S5	43	HOLD	63	$\overline{LCS}$
4	N.C.	24	A19/S6	44	SRDY	64	$\overline{PCS6}$/A2
5	AD9 (A9)	25	N.C.	45	$\overline{LOCK}$	65	$\overline{PCS5}$/A1
6	AD2	26	$\overline{BHE}$ ($\overline{RFSH}$)	46	$\overline{TEST}$/BUSY	66	$\overline{PCS4}$
7	AD10 (A10)	27	$\overline{WR}$/QS1	47	NMI	67	$\overline{PCS3}$
8	AD3	28	$\overline{RD}$/$\overline{QSMD}$	48	INT0	68	$\overline{PCS2}$
9	AD11 (A11)	29	ALE/QS0	49	INT1/$\overline{SELECT}$	69	$\overline{PCS1}$
10	V_{CC}	30	V_{SS}	50	V_{CC}	70	V_{SS}
11	V_{CC}	31	V_{SS}	51	V_{CC}	71	$\overline{PCS0}$
12	AD4	32	X1	52	INT2/$\overline{INTA0}$	72	N.C.
13	AD12 (A12)	33	X2	53	INT3/$\overline{INTA1}$	73	$\overline{RES}$
14	AD5	34	RESET	54	DT/$\overline{R}$	74	TMR OUT 1
15	AD13 (A13)	35	N.C.	55	N.C.	75	TMR OUT 0
16	AD6	36	CLKOUT	56	$\overline{DEN}$	76	TMR IN 1
17	AD14 (A14)	37	ARDY	57	$\overline{MCS0}$/PEREQ	77	TMR IN 0
18	AD7	38	$\overline{S2}$	58	$\overline{MCS1}$/$\overline{ERROR}$	78	DRQ1
19	AD15 (A15)	39	$\overline{S1}$	59	$\overline{MCS2}$	79	DRQ0
20	V_{CC}	40	$\overline{S0}$	60	$\overline{MCS3}$/$\overline{NPS}$	80	V_{SS}

NOTE:
Pin names in parentheses apply to the 80C188XL.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Ambient Temperature under Bias . . . . 0°C to +70°C

Storage Temperature . . . . −65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . −1.0V to +7.0V

Package Power Dissipation 1W
Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTICE: The specifications are subject to change without notice.

DC SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL1}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V (4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 μA @ V_{CC} −0.5(4)
I_{CC}	Power Supply Current		100	mA	@ 25 MHz, 0°C V_{CC} = 5.5V(3)
			90	mA	@ 20 MHz, 0°C V_{CC} = 5.5V(3)
			62.5	mA	@ 12 MHz, 0°C V_{CC} = 5.5V (3)
			100	μA	@ DC 0°C V_{CC} = 5.5V
I_{LI}	Input Leakage Current		±10	μA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA

DC SPECIFICATIONS (Continued) T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CHO}	Clock Output High	$V_{CC} - 0.5$		V	$I_{CHO} = -500\ \mu A$
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:
1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. RD/QSMD, UCS, LCS, MCS0/PEREQ, MCS1/ERROR and TEST/BUSY pins have internal pullup devices. Loading some of these pins above $I_{OH} = -200\ \mu A$ can cause the processor to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

Power Supply Current

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by I_{CC} = 5 mA × freq. (MHz) + I_{QL}.

I_{QL} is the quiescent leakage current when the clock is static. I_{QL} is typically less than 100 μA.

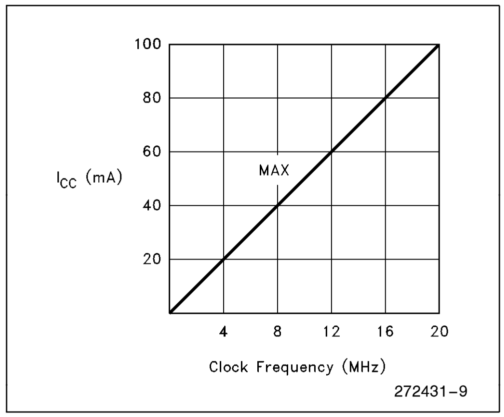


Figure 5. I_{CC} vs Frequency

AC SPECIFICATIONS

MAJOR CYCLE TIMINGS (READ CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	8		10		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	3	20	3	27	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 10$		$T_{CLCH} - 10$		$T_{CLCH} - 15$		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL} - 8$		$T_{CHCL} - 10$		$T_{CHCL} - 15$		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	T_{CLAX}	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	3	25	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	3	20	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	17	3	22	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	17	3	22	3	37	ns	
T_{CHCTV}	Control Active Delay 2	3	20	3	22	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	17	3	22	3	37	ns	

AC SPECIFICATIONS (Continued)

MAJOR CYCLE TIMINGS (READ CYCLE) (Continued)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL TIMING RESPONSES (Read Cycle)									
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	20	3	27	3	37	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL} - 15$		$2T_{CLCL} - 20$		$2T_{CLCL} - 25$		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	20	3	27	3	37	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	$T_{CLCH} - 14$		$T_{CLCH} - 14$		$T_{CLCH} - 14$		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	$T_{CLCL} - 15$		$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	Equal Loading

AC SPECIFICATIONS (Continued)

MAJOR CYCLE TIMINGS (WRITE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	3	20	3	27	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 10		T_{CHCL} − 10		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	20	3	25	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	17	3	25	3	37	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	3	25	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	3	20	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	17	3	22	3	37	ns	
80C186XL TIMING RESPONSES (Write Cycle)									
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ − 15		$2T_{CLCL}$ − 20		$2T_{CLCL}$ − 25		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	T_{CLCL} − 10		T_{CLCL} − 15		T_{CLCL} − 20		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading

AC SPECIFICATIONS (Continued)

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	8		10		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	3	20	3	27	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 10$		$T_{CLCH} - 10$		$T_{CLCH} - 15$		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	$T_{CHCL} - 10$		$T_{CHCL} - 10$		$T_{CHCL} - 15$		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	T_{CLAX}	25	ns	
T_{CVCTV}	Control Active Delay 1	3	17	3	25	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	17	3	25	3	37	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	3	22	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	17	3	22	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	17	3	22	3	37	ns	

AC SPECIFICATIONS (Continued)

SOFTWARE HALT CYCLE TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	3	22	3	37	ns	

AC SPECIFICATIONS (Continued)

CLOCK TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL CLKIN REQUIREMENTS(1)									
T_{CKIN}	CLKIN Period	20	∞	25	∞	40	∞	ns	
T_{CLCK}	CLKIN Low Time	8	∞	10	∞	16	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	8	∞	10	∞	16	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5		5	ns	1.0 to 3.5V
80C186XL CLKOUT TIMING									
T_{CICO}	CLKIN to CLKOUT Skew		17		17		21	ns	
T_{CLCL}	CLKOUT Period	40	∞	50		80	∞	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		6		8		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		6		8		10	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V. T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V. T_A = 0°C.

AC SPECIFICATIONS (Continued)

READY, PERIPHERAL AND QUEUE STATUS TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL READY AND PERIPHERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	8		10		15		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	8		10		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	8		10		15		ns	
T_{CLARX}	ARDY Active Hold Time(1)	8		10		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	8		10		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	10		15		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	8		10		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	8		10		15		ns	
80C186XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES									
T_{CLTMV}	Timer Output Delay		17		22		33	ns	
T_{CHQSV}	Queue Status Delay		22		27		32	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

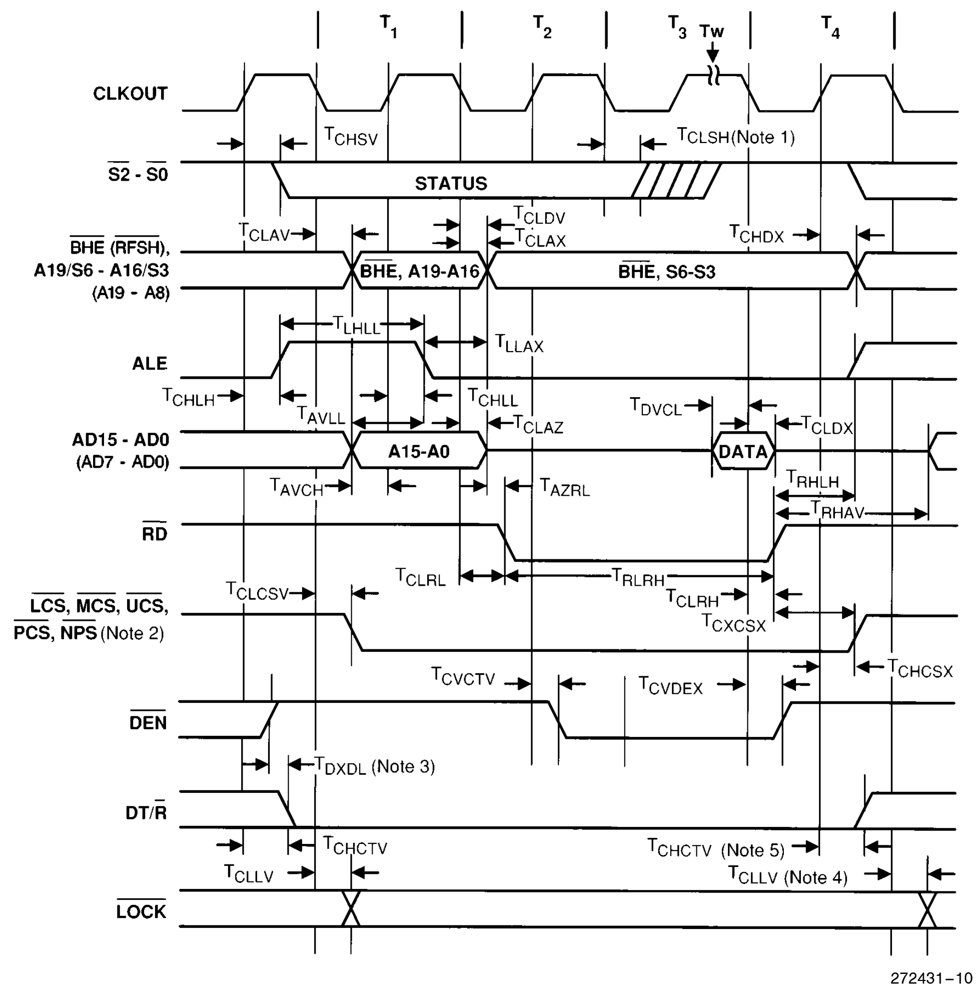
AC SPECIFICATIONS (Continued)

RESET AND HOLD/HLDA TIMINGS
T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL RESET AND HOLD/HLDA TIMING REQUIREMENTS									
T_{RESIN}	$\overline{RES}$ Setup	15		15		15		ns	
T_{HVCL}	HOLD Setup(1)	8		10		15		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	T_{CLAX}	25	ns	
T_{CLAV}	Address Valid Delay	3	20	3	22	3	36	ns	
80C186XL RESET AND HOLD/HLDA TIMING RESPONSES									
T_{CLRO}	Reset Delay		17		22		33	ns	
T_{CLHAV}	HLDA Valid Delay	3	17	3	22	3	33	ns	
T_{CHCZ}	Command Lines Float Delay		22		25		33	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		20		26		36	ns	

NOTE:
1. To guarantee recognition at next clock.

AC SPECIFICATIONS (Continued)

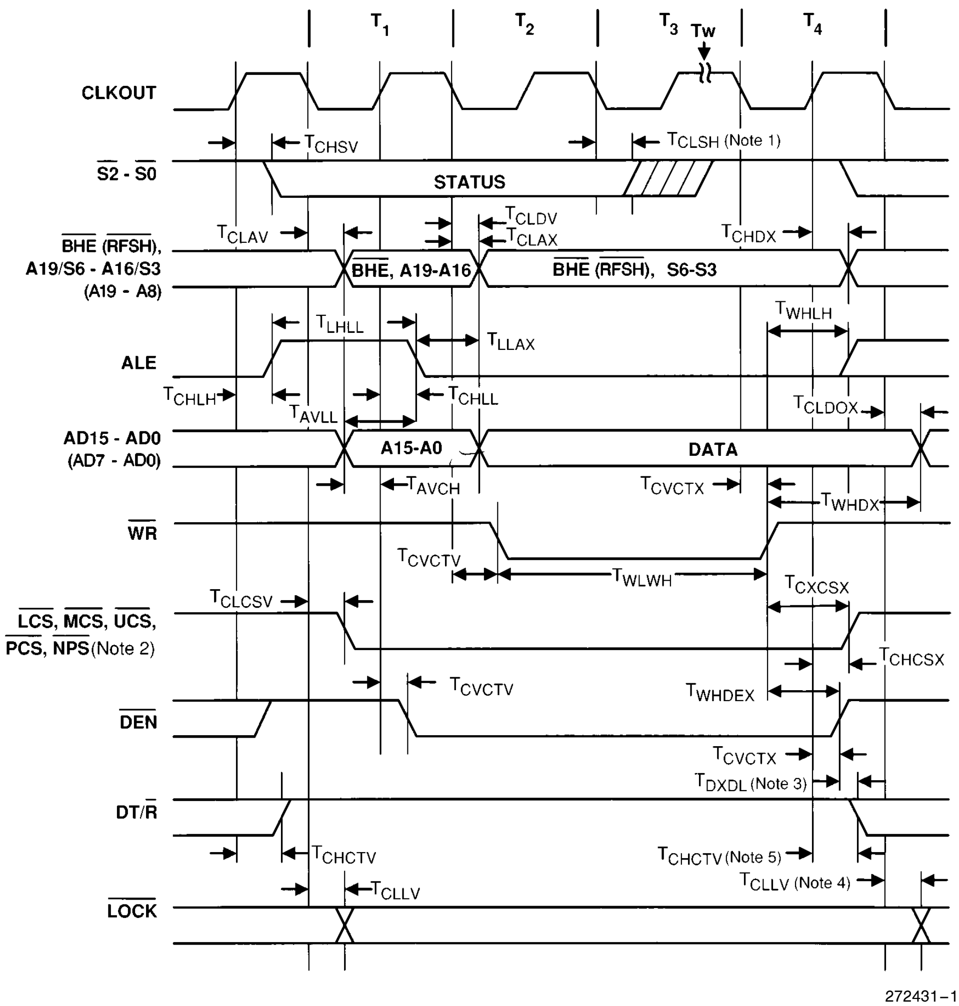


NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.

Pin names in parentheses apply to the 80C188XL.

Figure 6. Read Cycle Waveforms

AC SPECIFICATIONS (Continued)



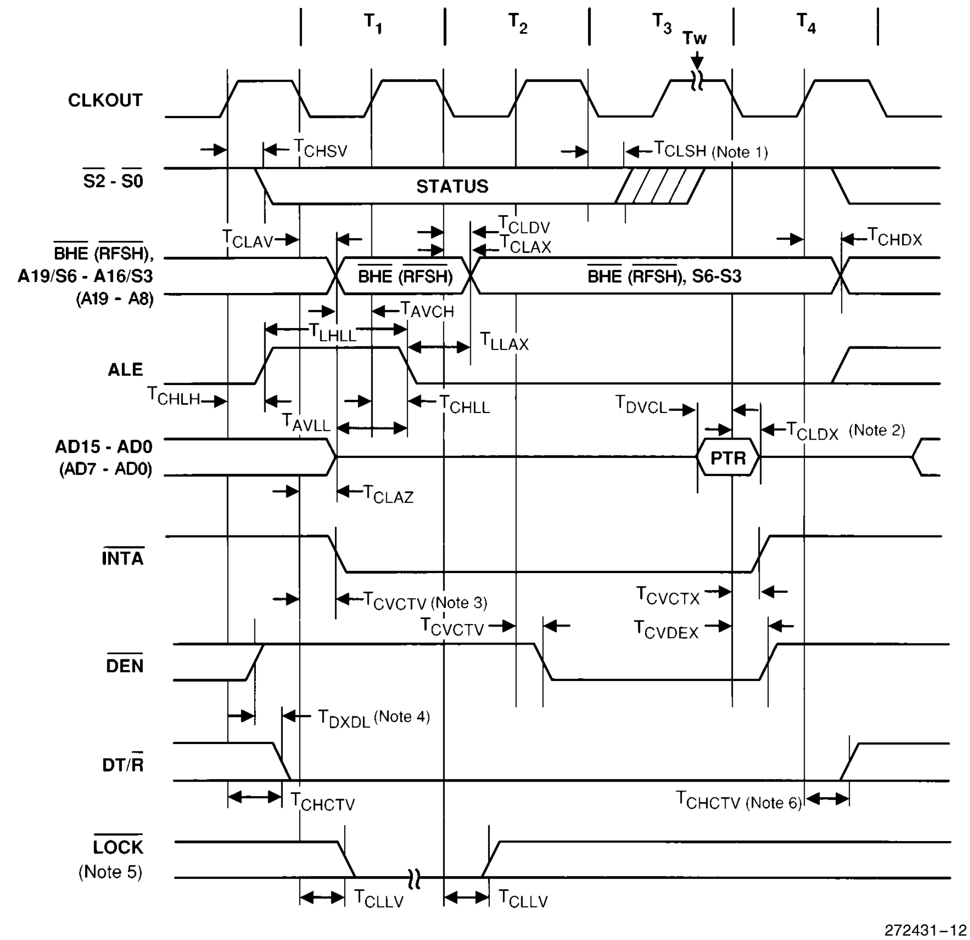
NOTES:

1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

Pin names in parentheses apply to the 80C188XL.

Figure 7. Write Cycle Waveforms

AC SPECIFICATIONS (Continued)



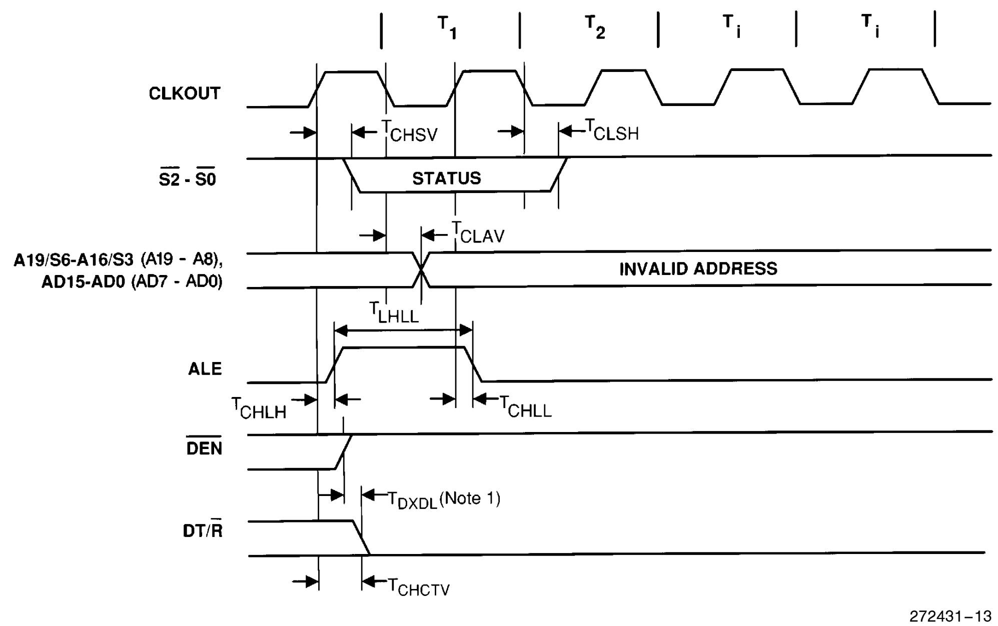
NOTES:

1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX} (min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.
6. Changes in T-state preceding next bus cycle if followed by write.

Pin names in parentheses apply to the 80C188XL.

Figure 8. Interrupt Acknowledge Cycle Waveforms

AC SPECIFICATIONS (Continued)



NOTE:
1. For write cycle followed by halt cycle.
Pin names in parentheses apply to the 80C188XL.

Figure 9. Software Halt Cycle Waveforms

WAVEFORMS

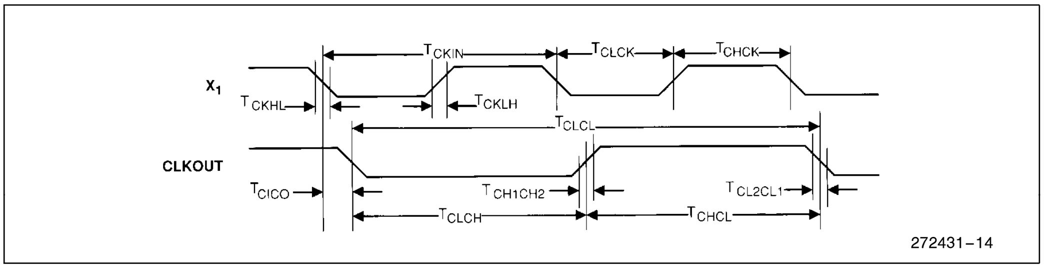


Figure 10. Clock Waveforms

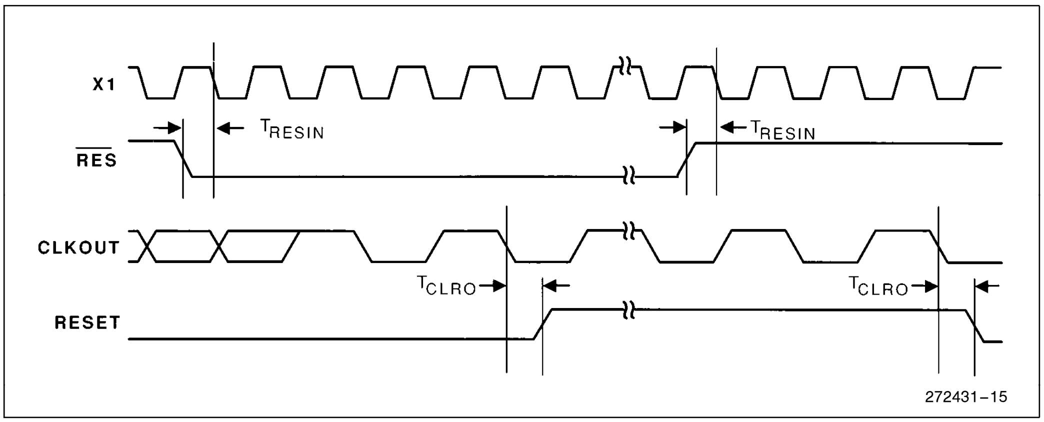


Figure 11. Reset Waveforms

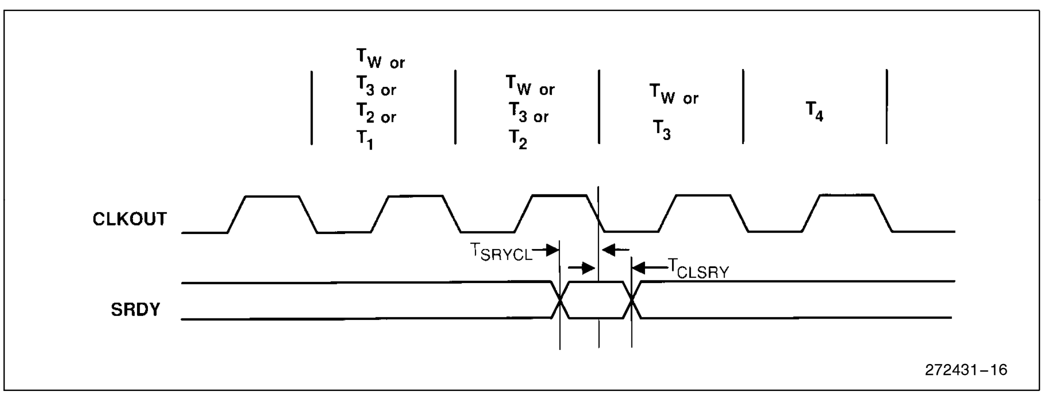


Figure 12. Synchronous Ready (SRDY) Waveforms

AC CHARACTERISTICS

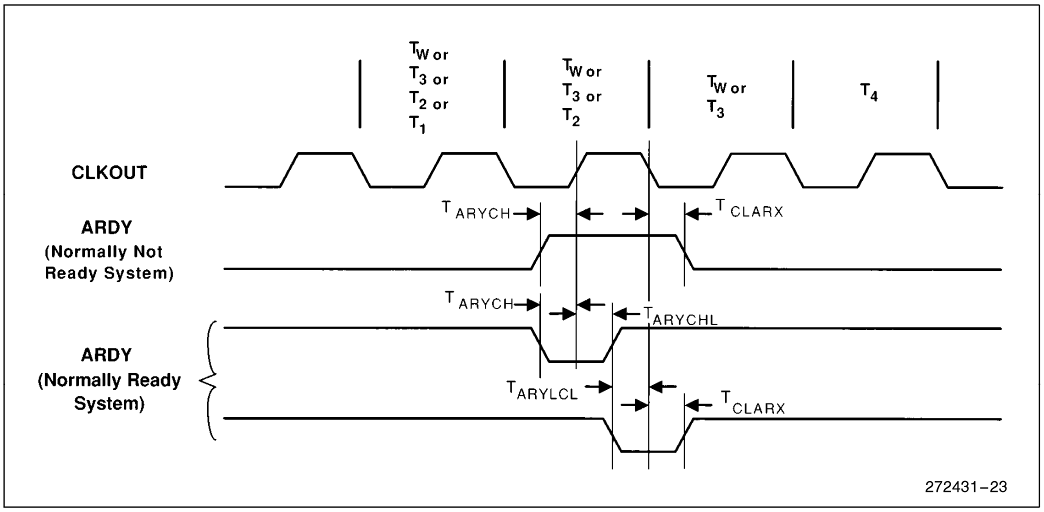


Figure 13. Asynchronous Ready (ARDY) Waveforms

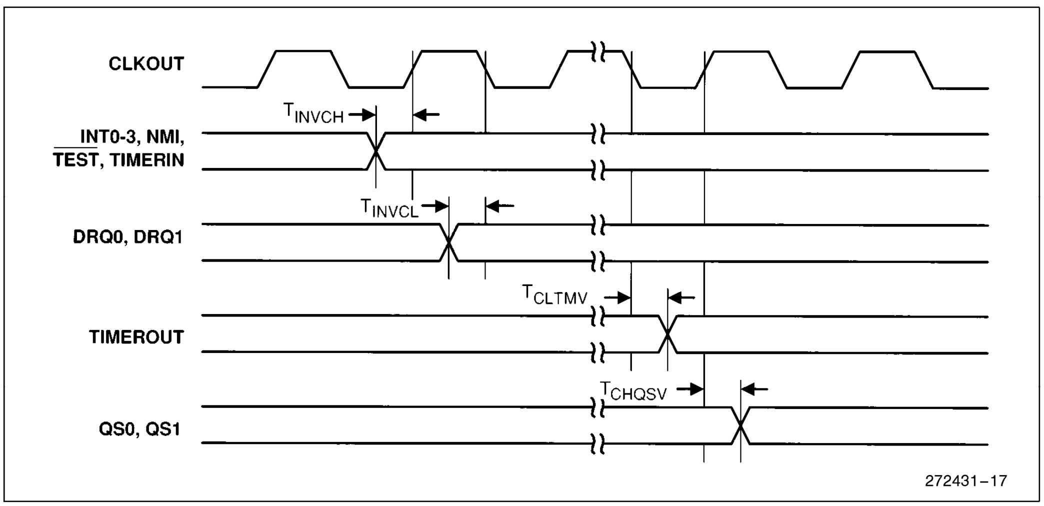


Figure 14. Peripheral and Queue Status Waveforms

AC CHARACTERISTICS (Continued)

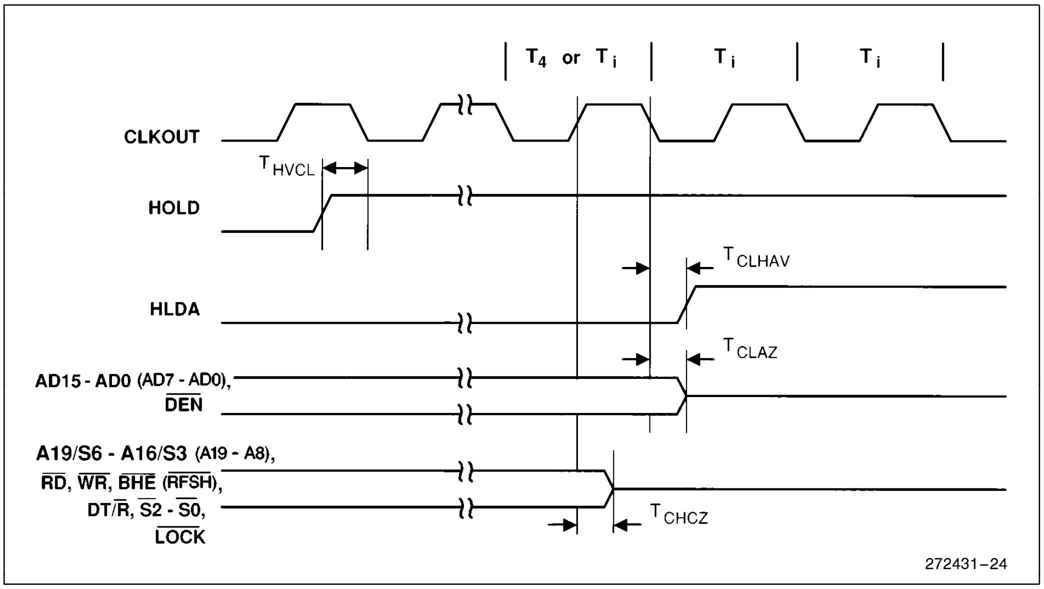


Figure 15. HOLDA/HLDA Waveforms (Entering Hold)

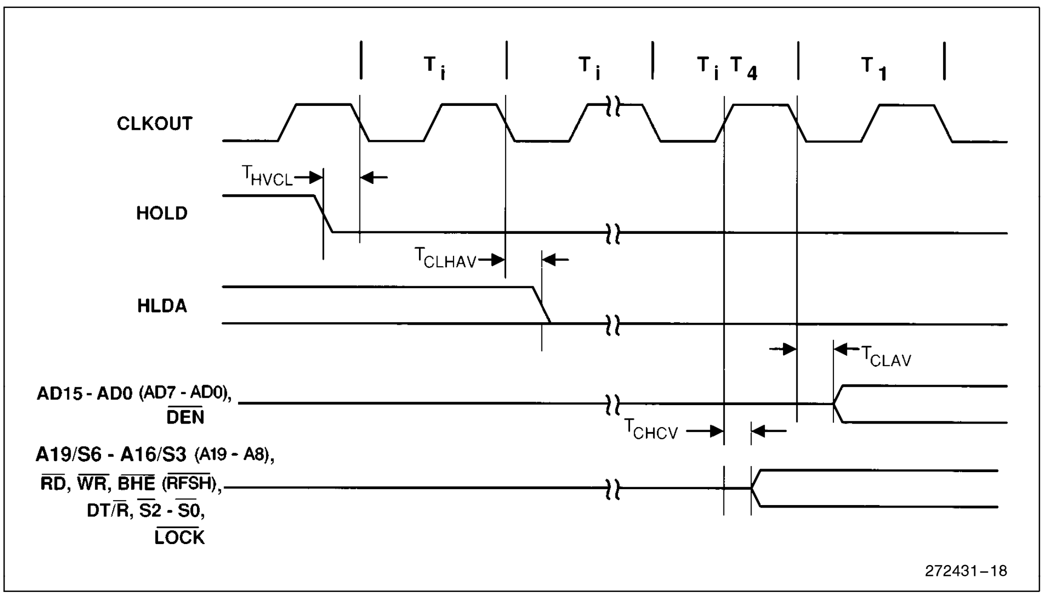


Figure 16. HOLD/HLDA Waveforms (Leaving Hold)

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
OUT: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV} — Time from Clock low to Address valid
T_{CHLH} — Time from Clock high to ALE high
T_{CLCSV} — Time from Clock low to Chip Select valid

DERATING CURVES

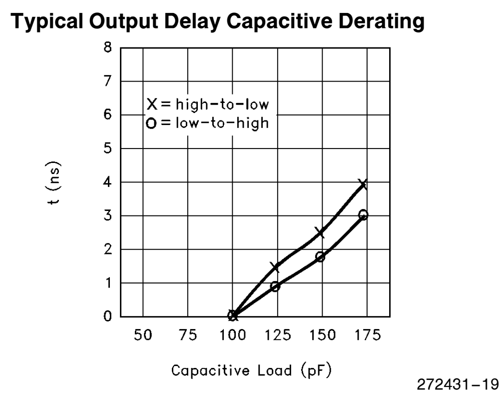


Figure 17. Capacitive Derating Curve

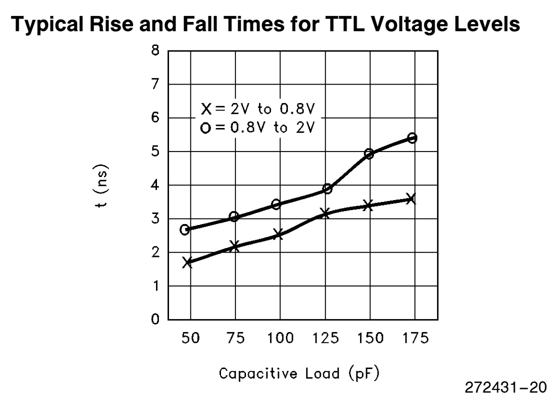


Figure 18. TTL Level Rise and Fall Times for Output Buffers

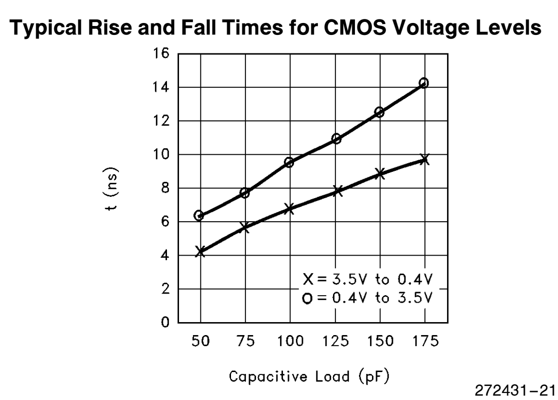


Figure 19. CMOS Level Rise and Fall Times for Output Buffers

80C186XL/80C188XL EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80C186XL microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The 80C186XL EXPRESS program includes an extended temperature range. With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 10. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 10. Prefix Identification

Prefix	Package Type	Temperature Range
A	PGA	Commercial
N	PLCC	Commercial
R	LCC	Commercial
S	QFP	Commercial
SB	SQFP	Commercial
TA	PGA	Extended
TN	PLCC	Extended
TR	LCC	Extended
TS	QFP	Extended

80C186XL/80C188XL EXECUTION TIMINGS

A determination of program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries (80C186XL only).

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186XL has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue (6 bytes) most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

The 80C188XL 8-bit BIU is limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue (4 bytes) much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				80C186XL Clock Cycles	80C188XL Clock Cycles	Comments
DATA TRANSFER							
MOV = Move:							
Register to Register/Memory	1 0 0 0 1 0 0 w	mod reg r/m			2/12	2/12*	
Register/memory to register	1 0 0 0 1 0 1 w	mod reg r/m			2/9	2/9*	
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 000 r/m	data	data if w=1	12/13	12/13	8/16-bit
Immediate to register	1 0 1 1 w reg	data	data if w=1		3/4	3/4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high		8	8*	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high		9	9*	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m			2/9	2/13	
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m			2/11	2/15	
PUSH = Push:							
Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m			16	20	
Register	0 1 0 1 0 reg				10	14	
Segment register	0 0 0 reg 1 1 0				9	13	
Immediate	0 1 1 0 1 0 s 0	data	data if s=0		10	14	
PUSHA = Push All	0 1 1 0 0 0 0 0				36	68	
POP = Pop:							
Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m			20	24	
Register	0 1 0 1 1 reg				10	14	
Segment register	0 0 0 reg 1 1 1	(reg≠01)			8	12	
POPA = Pop All	0 1 1 0 0 0 0 1				51	83	
XCHG = Exchange:							
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m			4/17	4/17*	
Register with accumulator	1 0 0 1 0 reg				3	3	
IN = Input from:							
Fixed port	1 1 1 0 0 1 0 w	port			10	10*	
Variable port	1 1 1 0 1 1 0 w				8	8*	
OUT = Output to:							
Fixed port	1 1 1 0 0 1 1 w	port			9	9*	
Variable port	1 1 1 0 1 1 1 w				7	7*	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1				11	15	
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m			6	6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m	(mod≠11)		18	26	
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m	(mod≠11)		18	26	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1				2	2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0				3	3	
PUSHF = Push flags	1 0 0 1 1 1 0 0				9	13	
POPF = Pop flags	1 0 0 1 1 1 0 1				8	12	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				80C186XL Clock Cycles	80C188XL Clock Cycles	Comments
DATA TRANSFER (Continued)							
SEGMENT = Segment Override:							
CS	0 0 1 0 1 1 1 0				2	2	
SS	0 0 1 1 0 1 1 0				2	2	
DS	0 0 1 1 1 1 1 0				2	2	
ES	0 0 1 0 0 1 1 0				2	2	
ARITHMETIC							
ADD = Add:							
Reg/memory with register to either	0 0 0 0 0 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w = 01	4/16	4/16*	
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w = 1		3/4	3/4	8/16-bit
ADC = Add with carry:							
Reg/memory with register to either	0 0 0 1 0 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w = 01	4/16	4/16*	
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w = 1		3/4	3/4	8/16-bit
INC = Increment:							
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m			3/15	3/15*	
Register	0 1 0 0 0 reg				3	3	
SUB = Subtract:							
Reg/memory and register to either	0 0 1 0 1 0 d w	mod reg r/m			3/10	3/10*	
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w = 01	4/16	4/16*	
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w = 1		3/4	3/4	8/16-bit
SBB = Subtract with borrow:							
Reg/memory and register to either	0 0 0 1 1 0 d w	mod reg r/m			3/10	3/10*	
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s w = 01	4/16	4/16*	
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w = 1		3/4	3/4*	8/16-bit
DEC = Decrement							
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m			3/15	3/15*	
Register	0 1 0 0 1 reg				3	3	
CMP = Compare:							
Register/memory with register	0 0 1 1 1 0 1 w	mod reg r/m			3/10	3/10*	
Register with register/memory	0 0 1 1 1 0 0 w	mod reg r/m			3/10	3/10*	
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s w = 01	3/10	3/10*	
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w = 1		3/4	3/4	8/16-bit
NEG = Change sign register/memory	1 1 1 1 0 1 1 w	mod 0 1 1 r/m			3/10	3/10*	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1				8	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1				4	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1				7	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1				4	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w	mod 100 r/m					
Register-Byte					26–28	26–28	
Register-Word					35–37	35–37	
Memory-Byte					32–34	32–34	
Memory-Word					41–43	41–43*	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				80C186XL Clock Cycles	80C188XL Clock Cycles	Comments
ARITHMETIC (Continued)							
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w	mod 1 0 1 r/m					
Register-Byte					25–28	25–28	
Register-Word					34–37	34–37	
Memory-Byte					31–34	32–34	
Memory-Word					40–43	40–43*	
IMUL = Integer Immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s=0	22–25/ 29–32	22–25/ 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 1 1 0 r/m					
Register-Byte					29	29	
Register-Word					38	38	
Memory-Byte					35	35	
Memory-Word					44	44*	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 1 1 1 r/m					
Register-Byte					44–52	44-52	
Register-Word					53–61	53–61	
Memory-Byte					50–58	50–58	
Memory-Word					59–67	59–67*	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	4	
LOGIC							
Shift/Rotate Instructions:							
Register/Memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15	2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n	5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n	5+n/17+n	
	TTT Instruction						
	0 0 0 ROL						
	0 0 1 ROR						
	0 1 0 RCL						
	0 1 1 RCR						
	1 0 0 SHL/SAL						
	1 0 1 SHR						
	1 1 1 SAR						
AND = And:							
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1	4/16	4/16*	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1		3/4	3/4*	8/16-bit
TEST = And function to flags, no result:							
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	3/10*	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1	4/10	4/10*	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1		3/4	3/4	8/16-bit
OR = Or:							
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1	4/16	4/16*	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1		3/4	3/4*	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				80C186XL Clock Cycles	80C188XL Clock Cycles	Comments
LOGIC (Continued)							
XOR = Exclusive or:							
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1	4/16	4/16*	
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	mod 0 1 0 r/m			3/10	3/10*	
STRING MANIPULATION							
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14	14*	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w				22	22*	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15	15*	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12	12*	
STOS = Store byte/wd from AL/AX	1 0 1 0 1 0 1 w				10	10*	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w				14	14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14	14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)							
MOVS = Move string	1 1 1 1 0 0 1 0	1 0 1 0 0 1 0 w			8 + 8n	8 + 8n*	
CMPS = Compare string	1 1 1 1 0 0 1 z	1 0 1 0 0 1 1 w			5 + 22n	5 + 22n*	
SCAS = Scan string	1 1 1 1 0 0 1 z	1 0 1 0 1 1 1 w			5 + 15n	5 + 15n*	
LODS = Load string	1 1 1 1 0 0 1 0	1 0 1 0 1 1 0 w			6 + 11n	6 + 11n*	
STOS = Store string	1 1 1 1 0 0 1 0	1 0 1 0 1 0 1 w			6 + 9n	6 + 9n*	
INS = Input string	1 1 1 1 0 0 1 0	0 1 1 0 1 1 0 w			8 + 8n	8 + 8n*	
OUTS = Output string	1 1 1 1 0 0 1 0	0 1 1 0 1 1 1 w			8 + 8n	8 + 8n*	
CONTROL TRANSFER							
CALL = Call:							
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high		15	19	
Register/memory indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m			13/19	17/27	
Direct intersegment	1 0 0 1 1 0 1 0	segment offset			23	31	
		segment selector					
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	(mod ≠ 11)		38	54	
JMP = Unconditional jump:							
Short/long	1 1 1 0 1 0 1 1	disp-low			14	14	
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high		14	14	
Register/memory indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m			11/17	11/21	
Direct intersegment	1 1 1 0 1 0 1 0	segment offset			14	14	
		segment selector					
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	(mod ≠ 11)		26	34	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	80C186XL Clock Cycles	80C188XL Clock Cycles	Comments
CONTROL TRANSFER (Continued)				
RET = Return from CALL:				
Within segment	1 1 0 0 0 0 1 1	16	20	
Within seg adding immed to SP	1 1 0 0 0 0 1 0 | data-low | data-high	18	22	
Intersegment	1 1 0 0 1 0 1 1	22	30	
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0 | data-low | data-high	25	33	
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0 | disp	4/13	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0 | disp	4/13	4/13	
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0 | disp	4/13	4/13	
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0 | disp	4/13	4/13	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0 | disp	4/13	4/13	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0 | disp	4/13	4/13	
JO = Jump on overflow	0 1 1 1 0 0 0 0 | disp	4/13	4/13	
JS = Jump on sign	0 1 1 1 1 0 0 0 | disp	4/13	4/13	
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1 | disp	4/13	4/13	
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1 | disp	4/13	4/13	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1 | disp	4/13	4/13	
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1 | disp	4/13	4/13	
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1 | disp	4/13	4/13	
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1 | disp	4/13	4/13	
JNO = Jump on not overflow	0 1 1 1 0 0 0 1 | disp	4/13	4/13	
JNS = Jump on not sign	0 1 1 1 1 0 0 1 | disp	4/13	4/13	
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1 | disp	5/15	5/15	
LOOP = Loop CX times	1 1 1 0 0 0 1 0 | disp	6/16	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1 | disp	6/16	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0 | disp	6/16	6/16	
ENTER = Enter Procedure	1 1 0 0 1 0 0 0 | data-low | data-high | L			
L = 0		15	19	
L = 1		25	29	
L > 1		22 + 16(n − 1)	26 + 20(n − 1)	
LEAVE = Leave Procedure	1 1 0 0 1 0 0 1	8	8	
INT = Interrupt:				
Type specified	1 1 0 0 1 1 0 1 | type	47	47	
Type 3	1 1 0 0 1 1 0 0	45	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	48/4	48/4	
IRET = Interrupt return	1 1 0 0 1 1 1 1	28	28	
BOUND = Detect value out of range	0 1 1 0 0 0 1 0 | mod reg r/m	33–35	33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	80C186XL Clock Cycles	80C188XL Clock Cycles	Comments
PROCESSOR CONTROL				
CLC = Clear carry	1 1 1 1 1 0 0 0	2	2	
CMC = Complement carry	1 1 1 1 0 1 0 1	2	2	
STC = Set carry	1 1 1 1 1 0 0 1	2	2	
CLD = Clear direction	1 1 1 1 1 1 0 0	2	2	
STD = Set direction	1 1 1 1 1 1 0 1	2	2	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	2	2	
STI = Set interrupt	1 1 1 1 1 0 1 1	2	2	
HLT = Halt	1 1 1 1 0 1 0 0	2	2	
WAIT = Wait	1 0 0 1 1 0 1 1	6	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	2	2	
NOP = No Operation	1 0 0 1 0 0 0 0	3	3	
	(TTT LLL are opcode to processor extension)			

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod	=	11 then r/m is treated as a REG field
if mod	=	00 then DISP = 0*, disp-low and disp-high are absent
if mod	=	01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod	=	10 then DISP = disp-high: disp-low
if r/m	=	000 then EA = (BX) + (SI) + DISP
if r/m	=	001 then EA = (BX) + (DI) + DISP
if r/m	=	010 then EA = (BP) + (SI) + DISP
if r/m	=	011 then EA = (BP) + (DI) + DISP
if r/m	=	100 then EA = (SI) + DISP
if r/m	=	101 then EA = (DI) + DISP
if r/m	=	110 then EA = (BP) + DISP*
if r/m	=	111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

This data sheet replaces the following data sheets:
- 272031-002 80C186XL
- 270975-002 80C188XL
- 272309-001 SB80C186XL
- 272310-001 SB80C188XL

ERRATA

An A or B step 80C186XL/80C188XL has the following errata. The A or B step 80C186XL/80C188XL can be identified by the presence of an ''A'' or ''B'' alpha character, respectively, next to the FPO number. The FPO number location is shown in Figure 4.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistently, it is dependent on interrupt timing.

The C step 80C186XL/80C188XL has no known errata. The C step can be identified by the presence of a ''C'' or ''D'' alpha character next to the FPO number. The FPO number location is shown in Figure 4.

PRODUCT IDENTIFICATION

Intel 80C186XL devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (272431-001) is valid for devices with an ''A'', ''B'', ''C'', or ''D'' as the ninth character in the FPO number, as illustrated in Figure 4.