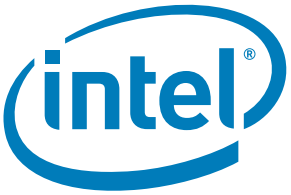


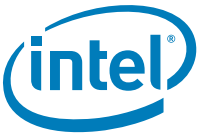
Intel® Celeron® Processor 900 Series and Ultra Low Voltage 700 Series

Datasheet

For platforms based on Mobile Intel® 4 Series Chipset family

February 2010

Document Number: 320389-003



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Revision History

Document Number	Revision Number	Description	Date
320389	001	Initial Release	August 2008
320389	002	Table 6: Added specs for 743 Table 14: Added specs for 743	September 2009
320389	003	Added 900 series specifications	February 2010

1 Introduction

The Intel® Celeron® processor on 45-nanometer process technology in the Intel® Centrino® 2 process technology is the next generation high-performance, low-power mobile processor based on the Intel Core microarchitecture.

In the Centrino 2 process technology platform, the Celeron processor supports the Mobile Intel® 4 Series Express Chipset family and Intel® ICH9M I/O controller. This document contains electrical, mechanical and thermal specifications for:

- Dual-Core and Single-Core Standard Voltage (35W TDP)

In the Montevina SFF platform, the Celeron processor supports the Mobile SFF Intel 4 Series Express Chipset family and Intel® ICH9M SFF I/O controller. This document also contains electrical, mechanical and thermal specifications for:

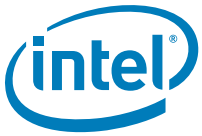
- Single-Core SFF Ultra-Low Voltage (10W TDP)
- Single-Core SFF Ultra-Low Voltage (5.5W TDP)

In this document, Intel® Celeron® processor on 45-nm process will be referred to as the *processor* and Mobile Intel® 4 Series Express Chipset family will be referred to as the *(G)MCH*.

The following list provides some of the key features on this processor:

- Dual-core and single core processors for mobile with enhanced performance
- Supports Intel® architecture with Intel® Wide Dynamic Execution
- Supports L1 cache-to-cache (C2C) transfer
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache in each core
- 1-MB second-level shared cache with Advanced Transfer Cache architecture
- 800-MHz source-synchronous front side bus (FSB)
- Digital thermal sensor (DTS)
- Intel® 64 architecture
- Supports PSI2 functionality
- The processor in SV is offered in 478-pin Micro-FCPGA and 479-ball Micro-FCBGA[1] packaging technologies
- The SFF processor in LV and ULV are offered in 956-ball Micro-FCBGA packaging technologies only
- Execute Disable Bit support for enhanced security
-

1. Micro-FCBGA in standard package available for Embedded only.



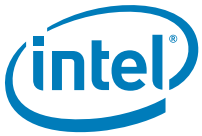
1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
TDP	Thermal Design Power
V_{CC}	The processor core power supply
V_{SS}	The processor ground

1.2 References

The following documents may be beneficial when reading this document.

Document	Document Number[1]
Intel® Core™2 Duo Mobile Processor and Intel® Core 2 Extreme Mobile Processor Specification Update	377039
Mobile Intel® 4 Series Express Chipset Family Datasheet	320122
Mobile Intel® 4 Series Express Chipset Family Graphics Memory Controller Hub Specification Update	320123
Intel® I/O Controller Hub 9 Family Specification Update	605214
Intel® 64 and IA-32 Architectures Software Developer's Manuals	
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669



2 Low Power Features

2.1 Clock Control and Low-Power States

The processor supports low-power states both at the individual core level and the package level for optimal power management.

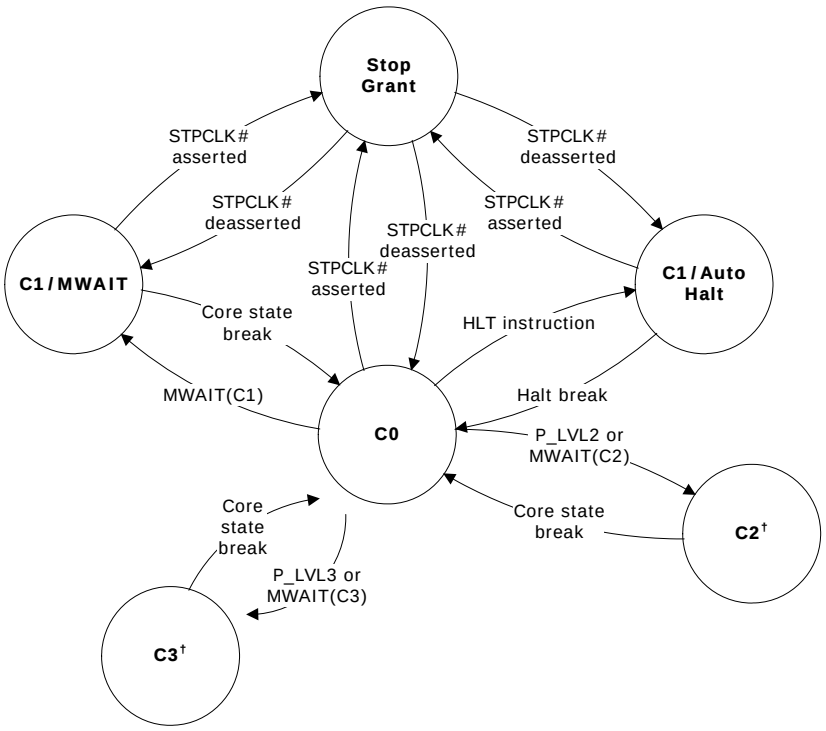
A core may independently enter the C1/AutoHALT, C1/MWAIT, C2, C3. When both cores coincide in a common core low-power state, the central power management logic ensures the entire processor enters the respective package low-power state by initiating a P_LVLx (P_LVL2, P_LVL3) I/O read to the (G)MCH.

The processor implements two software interfaces for requesting low-power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The P_LVLx I/O Monitor address does not need to be set up before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured through the IA32_MISC_ENABLES model specific register (MSR).

If a core encounters a GMCH break event while STPCLK# is asserted, it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that individual cores should return to the C0 state and the processor should return to the Normal state.

Figure 1 shows the core low-power states and Figure 2 shows the package low-power states for the processor. Table 1 maps the core low-power states to package low-power states.

Figure 1. Core Low-Power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no effect if a core is in C2, C3.

Figure 2. Package Low-Power States

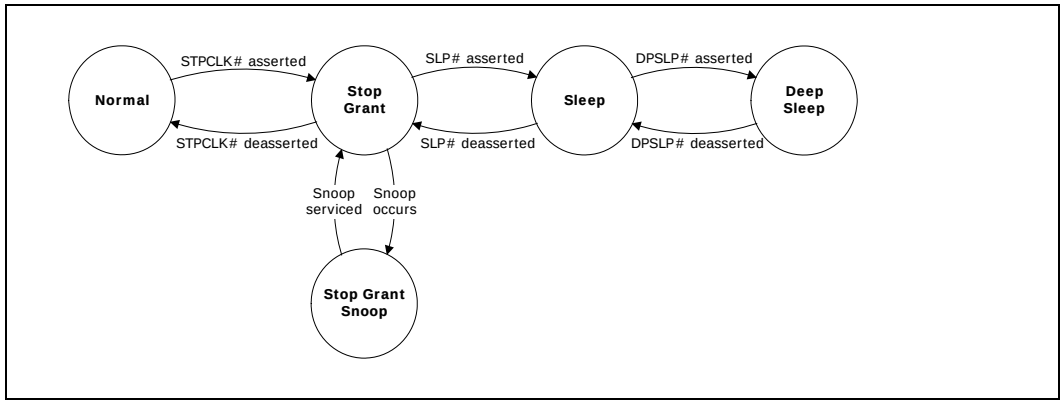


Table 1. Coordination of Core Low-Power States at the Package Level

Package State	Core1 State			
Core0 State	**C0**	**C1[1]**	**C2**	**C3**
C0	Normal	Normal	Normal	Normal
C1[1]	Normal	Normal	Normal	Normal
C2	Normal	Normal	Stop-Grant	Stop-Grant
C3	Normal	Normal	Stop-Grant	Deep Sleep

NOTE:
1. AutoHALT or MWAIT/C1.

2.1.1 Core Low-Power State Descriptions

2.1.1.1 Core C0 State

This is the normal operating state for cores in the processor.

2.1.1.2 Core C1/AutoHALT Powerdown State

C1/AutoHALT is a low-power state entered when a core executes the HALT instruction. The processor core will transition to the C0 state upon occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt messages. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Powerdown state, the dual-core processor will process bus snoops and snoops from the other core. The processor core will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the AutoHALT Powerdown state.

2.1.1.3 Core C1/MWAIT Powerdown State

C1/MWAIT is a low-power state entered when the processor core executes the MWAIT(C1) instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

2.1.1.4 Core C2 State

Individual cores of the dual-core processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the dual-core processor will process bus snoops and snoops from the other core. The processor core will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the C2 state.

2.1.1.5 Core C3 State

Individual cores of the dual-core processor can enter the C3 state by initiating a P_LVL3 I/O read to the P_BLK or an MWAIT(C3) instruction. Before entering C3, the processor core flushes the contents of its L1 caches into the processor's L2 cache. Except for the caches, the processor core maintains all its architectural states in the C3 state. The Monitor remains armed if it is configured. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed the processor keeps the core in the C3 state when the processor detects a snoop on the FSB or when the other core of the dual-core processor accesses cacheable memory. The processor core will transition to the C0 state upon occurrence of a Monitor event, SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor core to immediately initialize itself.

2.1.2 Package Low-Power State Descriptions

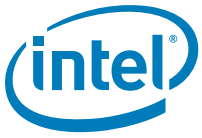
2.1.2.1 Normal State

This is the normal operating state for the processor. The processor remains in the Normal state when at least one of its cores is in the C0, C1/AutoHALT, or C1/MWAIT state.

2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted, each core of the dual-core processor enters the Stop-Grant state within 20 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. Processor cores that are already in the C2, C3 state remain in their current low-power state. When the STPCLK# pin is deasserted, each core returns to its previous core low-power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.



RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSLP# pins must be deasserted prior to RESET# deassertion as per AC Specification T45. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted after the deassertion of SLP# as per AC Specification T75.

While in Stop-Grant state, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT# and LINT[1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 2.1.2.3). A transition to the Sleep state (see Section 2.1.2.4) occurs with the assertion of the SLP# signal.

2.1.2.3 Stop-Grant Snoop State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

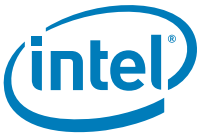
2.1.2.4 Sleep State

The Sleep state is a low-power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through the Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin. While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.



2.2 FSB Low-Power Enhancements

The processor incorporates FSB low power enhancements:

- Dynamic FSB Power Down
- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On-Die Termination disabling
- Low V_{CCP} (I/O termination voltage)

The processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in GMCH address and control input buffers when the processor deasserts its BR0# pin. The On-Die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.3 Processor Power Status Indicator (PSI-2) Signal

The processor incorporates the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve intermediate and light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. Since the processor is single core, the PSI-2 functionality will be limited to the single core operational state.Additionally the voltage regulator may switch to a single phase and/or asynchronous mode when the processor is idle and fused leakage limit is less than or equal to the BIOS threshold value.

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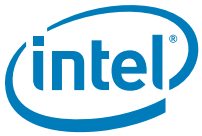


3 Electrical Specifications

3.1 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. Refer to the platform design guides for more details. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.1.1 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous-generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor uses a differential clocking implementation.

3.2 Voltage Identification and Power Sequencing

The processor uses seven voltage identification pins,VID[6:0], to support automatic selection of power supply voltages. The VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A 1 in the table refers to a high-voltage level and a 0 refers to a low-voltage level.

Table 2. Voltage Identification Definition (Sheet 1 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375

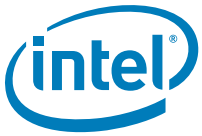


Table 2. Voltage Identification Definition (Sheet 2 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500

Table 2. Voltage Identification Definition (Sheet 3 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

3.3 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 °C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

3.4 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no-connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

The TEST1,TEST2,TEST3,TEST4,TEST5,TEST6 pins are used for test purposes internally and can be left as “No Connects”.

Note: There is no TEST7 pin on the processor.

3.5 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 3.

Table 3. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	L	RESERVED
L	L	H	RESERVED
L	H	H	RESERVED
L	H	L	200 MHz
H	H	L	RESERVED
H	H	H	RESERVED
H	L	H	RESERVED
H	L	L	RESERVED

3.6 FSB Signal Groups

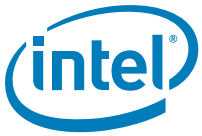
The FSB signals have been combined into groups by buffer type in the following sections. AGTL+ input signals have differential input buffers that use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source-synchronous data bus, two sets of timing parameters need to be specified. One set is for common clock signals, which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.), and the second set is for the source-synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 4 identifies which signals are common clock, source synchronous, and asynchronous.

Table 4. FSB Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, PREQ#[5], RESET#, RS[2:0]#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[3:0]#[3], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#[3], DPWR#
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr><tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
CMOS Input	Asynchronous	A20M#, DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Open Drain Output	Asynchronous	FERR#, IERR#, THERMTRIP#
Open Drain I/O	Asynchronous	PROCHOT#[4]
CMOS Output	Asynchronous	PSI#, VID[6:0], BSEL[2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0]
Power/Other		COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, V_{CC}, V_{CCA}, V_{CCP}, V_{CC_SENSE}, V_{SS}, V_{SS_SENSE}

NOTES:
1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. BPM[2:1]# and PRDY# are AGTL+ output-only signals.
4. PROCHOT# signal type is open drain output and CMOS input.
5. On-die termination differs from other AGTL+ signals.



3.7 CMOS Signals

CMOS input signals are shown in Table 4. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) use Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for more than four BCLKs for the processor to recognize them. See Section 3.9 for the DC and AC specifications for the CMOS signal groups.

3.8 Maximum Ratings

Table 5 specifies absolute maximum and minimum ratings only and these lie outside the functional limits of the processor. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions outside these limits but within the absolute maximum and minimum ratings, the device may be functional but with its lifetime degraded, depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding the absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is subjected to these conditions for any length of time, the device may not function or may not be reliable when returned to conditions within the functional operating condition limits.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 5. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,5]
$T_{STORAGE}$	Processor Storage Temperature	-40	85	°C	2,3,4,6
V_{CC}	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.45	V	
$V_{inAGTL+}$	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.45	V	
$V_{inAsynch\_CMOS}$	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.45	V	

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long-term reliability of the processor.
5. Overshoot and undershoot guidelines for input, output, and I/O signals are in Chapter 4.
6. The min $T_{STORAGE}$ temperature is -25 °C.

3.9 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Table 4 for the pin signal definitions and signal pin assignments.

The tables in this section list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Active mode load line specifications apply in all states except in the Deep Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Maximum Junction Temperature ($T_{J,max}$) values for the processor are documented in Table 16 and Table 17. Read all notes associated with each parameter.

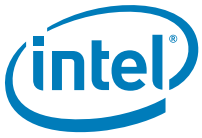


Table 6. Voltage and Current Specifications for the Single-Core Standard Voltage (SV) Processors

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CC}	V_{CC}		0.8		1.25	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.2	—	V	2, 6, 8
V_{CCP}	AGTL+ Termination Voltage		1.0	1.05	1.1	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	47	A	5, 12
I_{CC}	I_{CC} for Processors		—	—	—		
	Processor Number	Core Frequency/Voltage	—	—	—		
	900	2.2 GHz	—	—	47	A	3, 4
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant		—	—	25.4	A	3, 4
I_{SLP}	I_{CC} Sleep		—	—	24.7	A	3, 4
I_{DPSLP}	I_{CC} Deep Sleep		—	—	22.9	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin		—	—	600	mA/µs	7, 9
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CCC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable		—	—	4.5 2.5	A A	10 11

NOTES:.

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (e.g. Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105 °C T_J.
4. Specified at the nominal V_{CC}.
5. Refer to the *RS – Intel® Mobile Voltage Positioning (Intel® MVP) - 6 Mobile Processor and Mobile Chipset Voltage Regulation Specification* for design target capability.
6. Refer to Figure 14 for a waveform illustration of this parameter.
7. Measured at the bulk capacitors on the motherboard.
8. $V_{CC,BOOT}$ tolerance shown in Figure 3.
9. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
10. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
11. This is a steady-state I_{CC}current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
12. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

Table 7. Voltage and Current Specifications for the Single-Core, Ultra Low Voltage (ULV, 10 W) Processor

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CC}	V_{CC}		0.775	—	1.1	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 5
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	18	A	10
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—		
	723	1.2 GHz	—	—	17.6	A	3, 4
	743	1.3 GHz			17.6	A	3, 4
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant		—	—	6.3	A	3, 4
I_{SLP}	I_{CC} Sleep		—	—	5.9	A	3, 4
I_{DPSLP}	I_{CC} Deep Sleep		—	—	5.0	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin		—	—	600	mA/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP}Supply after V_{CC} Stable		—	—	4.5 2.5	A A	8 9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (e.g., Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 3.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels.

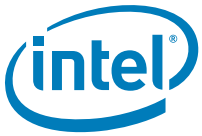


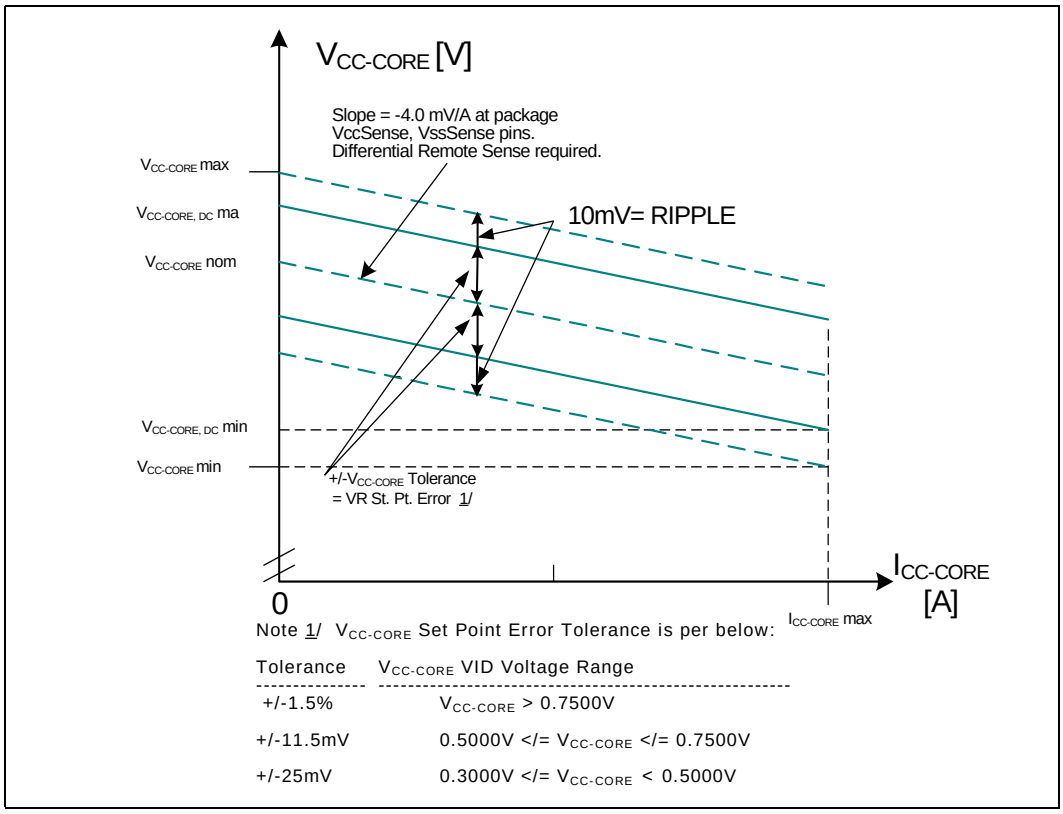
Table 8. Voltage and Current Specifications for the Single-Core Ultra Low Voltage (ULV, 5.5 W) Processors

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CC}	V_{CC}		0.775	—	1.1	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 5
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	9	A	10
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—		
	722	1.2 GHz	—	—	9	A	3, 4
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant		—	—	4.4	A	3, 4
I_{SLP}	I_{CC} Sleep		—	—	4.1	A	3, 4
I_{DPSLP}	I_{CC} Deep Sleep		—	—	3.3	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin		—	—	600	mA/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP}Supply after V_{CC} Stable		—	—	4.5 2.5	A A	8 9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (e.g. Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 3.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels.

Figure 3. Active V_{CC} and I_{CC} Loadline



NOTES:
1. Applies to low-voltage, ultra low-voltage and low-power standard voltage 22-mm (dual-core) processors for Intel® Centrino® processor technology.
2. Active mode tolerance depends on VID value.

Table 9. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CROSS}	Crossing Voltage	0.3	—	0.55	V	2, 7, 8
ΔV_{CROSS}	Range of Crossing Points	—	—	140	mV	2, 7, 5
V_{SWING}	Differential Output Swing	300	—	—	mV	6
I_{LI}	Input Leakage Current	-5	—	+5	µA	3
Cpad	Pad Capacitance	0.95	1.2	1.45	pF	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. For Vin between 0 V and V_{IH}.
4. Cpad includes die capacitance only. No package parasitics are included.
5. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.
6. Measurement taken from differential waveform.
7. Measurement taken from single-ended waveform.
8. Only applies to the differential rising edge (Clock rising and Clock# falling).

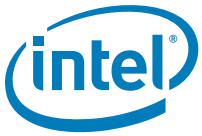


Table 10. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
GTLREF	Reference Voltage	0.65	0.70	0.72	V	6
R_{COMP}	Compensation Resistor	27.23	27.5	27.78	Ω	10
$R_{ODT/A}$	Termination Resistor Address	49	55	63	Ω	11, 12
$R_{ODT/D}$	Termination Resistor Data	49	55	63	Ω	11, 13
$R_{ODT/Cntrl}$	Termination Resistor Control	49	55	63	Ω	11, 14
V_{IH}	Input High Voltage	0.82	1.05	1.20	V	3,6
V_{IL}	Input Low Voltage	-0.10	0	0.55	V	2,4
V_{OH}	Output High Voltage	0.90	V_{CCP}	1.10	V	6
$R_{TT/A}$	Termination Resistance Address	50	55	61	Ω	7, 12
$R_{TT/D}$	Termination Resistance Data	50	55	61	Ω	7, 13
$R_{TT/Cntrl}$	Termination Resistance Control	50	55	61	Ω	7, 14
$R_{ON/A}$	Buffer on Resistance Address	23	25	29	Ω	5, 12
$R_{ON/D}$	Buffer on Resistance Data	23	25	29	Ω	5, 13
$R_{ON/Cntrl}$	Buffer on Resistance Control	23	25	29	Ω	5, 14
I_{LI}	Input Leakage Current	—	—	±100	µA	8
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pulldown driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at $0.31*V_{CCP}$. R_{ON} (min) = $0.418*R_{TT}$, R_{ON} (typ) = $0.455*R_{TT}$, R_{ON} (max) = $0.527*R_{TT}$. R_{TT} typical value of 55 Ω is used for R_{ON} typ/min/max calculations.
6. GTLREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at $0.31*V_{CCP}$. R_{TT} is connected to V_{CCP} on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on-die R_{TT} and R_{ON} turned off. Vin between 0 and V_{CCP}.
9. Cpad includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the comp pins.
11. On-die termination resistance, measured at $0.33*V_{CCP}$.
12. Applies to Signals A[35:3].
13. Applies to Signals D[63:0].
14. Applies to Signals BPRI#, DEFER#, PREQ#, PREST#, RS[2:0]#, TRDY#, ADS#, BNR#, BPM[3:0], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#, DPWR#, DSTB[1:0]#, DSTBP[3:0] and DSTBN[3:0]#.

Table 11. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
V_{IL}	Input Low Voltage CMOS	-0.10	0.00	$0.3*V_{CCP}$	V	2, 3
V_{IH}	Input High Voltage	$0.7*V_{CCP}$	V_{CCP}	$V_{CCP}+0.1$	V	2
V_{OL}	Output Low Voltage	-0.10	0	$0.1*V_{CCP}$	V	2
V_{OH}	Output High Voltage	$0.9*V_{CCP}$	V_{CCP}	$V_{CCP}+0.1$	V	2
I_{OL}	Output Low Current	1.5	—	4.1	mA	4
I_{OH}	Output High Current	1.5	—	4.1	mA	5
I_{LI}	Input Leakage Current	—	—	±100	µA	6
Cpad1	Pad Capacitance	1.80	2.30	2.75	pF	7
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45	pF	8

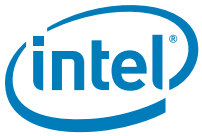
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at 0.1 *V_{CCP}.
5. Measured at 0.9 *V_{CCP}.
6. For Vin between 0 V and V_{CCP}. Measured when the driver is tristated.
7. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 12. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	V_{CCP}–5%	V_{CCP}	$V_{CCP}+5\%$	V	3
V_{OL}	Output Low Voltage	0	—	0.20	V	
I_{OL}	Output Low Current	16	—	50	mA	2
I_{LO}	Output Leakage Current	—	—	±200	µA	4
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V_{OH} is determined by value of the external pull-up resistor to V_{CCP}.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

§



4 Package Mechanical Specifications and Pin Information

4.1 Package Mechanical Specifications

The SV processor is available in 478-pin Micro-FCPGA packages as well as 479-ball Micro-FCBGA packages. The package mechanical dimensions are shown in Figure 4 through Figure 8.

The ULV processor is available 956-ball Micro-FCBGA packages. The package mechanical dimensions are shown in Figure 8.

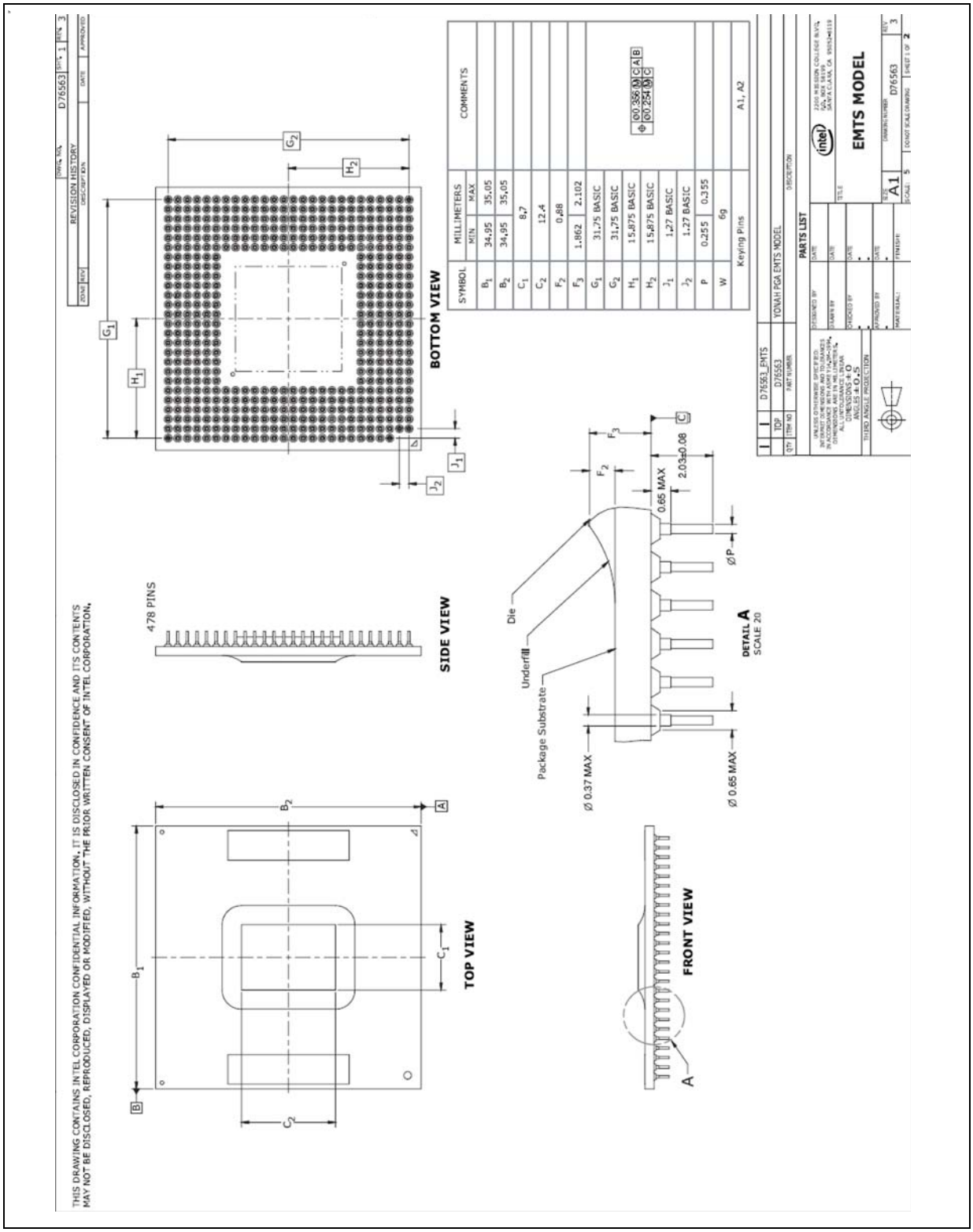
The mechanical package pressure specifications are in a direction normal to the surface of the processor. This requirement is to protect the processor die from fracture risk due to uneven die pressure distribution under tilt, stack-up tolerances and other similar conditions. These specifications assume that a mechanical attach is designed specifically to load one type of processor.

Intel also specifies that 15-lbf load limit should not be exceeded on any of Intel's BGA packages so as to not impact solder joint reliability after reflow. This load limit ensures that impact to the package solder joints due to transient bend, shock, or tensile loading is minimized. The 15-lbf metric should be used **in parallel** with the 689-kPa (100 psi) pressure limit as long as neither limits are exceeded. In some cases, designing to 15 lbf will exceed the pressure specification of 689 kPa (100 psi) and therefore should be reduced to ensure both limits are maintained.

Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

Caution: The Micro-FCBGA package incorporates land-side capacitors. The land-side capacitors are electrically conductive so care should be taken to avoid contacting the capacitors with other electrically conductive materials on the motherboard. Doing so may short the capacitors and possibly damage the device or render it inactive.

Figure 4. 1-MB on 6-MB Die (SV) Micro-FCPGA Package Drawing (Sheet 1 of 2)



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	8.7		
C_2	12.4		
F_2	0.88		
F_3	1.862	2.102	
G_1	31.75 BASIC		
G_2	31.75 BASIC		
H_1	15.875 BASIC		Φ 0.356 M C A B Φ 0.254 M C
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
P	0.255	0.355	
W	6g		
Keying Pins			A1, A2

Figure 5. 1-MB on 6-MB Die (SV) Micro-FCPGA Package Drawing (Sheet 2 of 2)

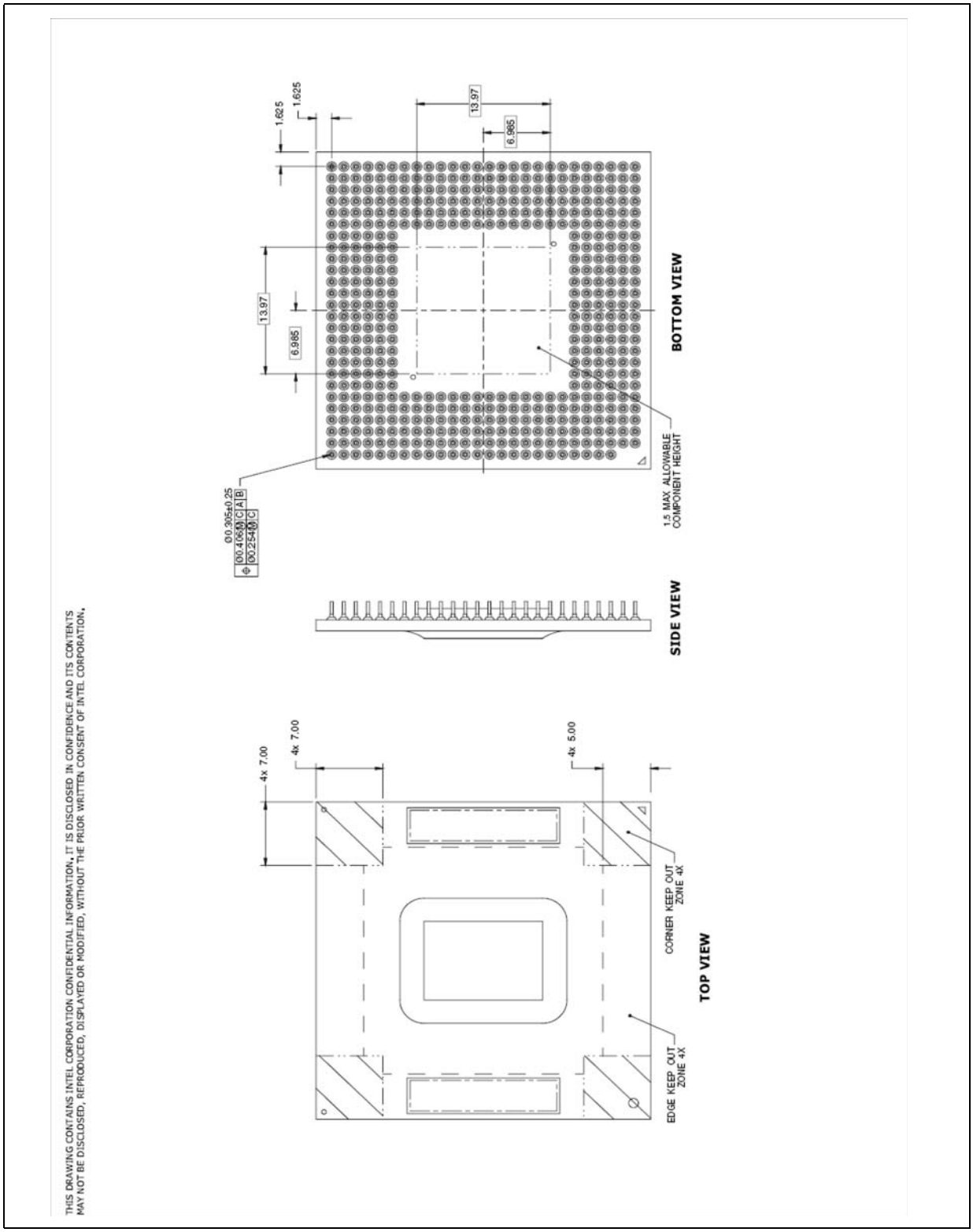


Figure 6. 1-MB on 6-MB Die (SV) Micro-FCBGA Package Drawing (Sheet 1 of 2)

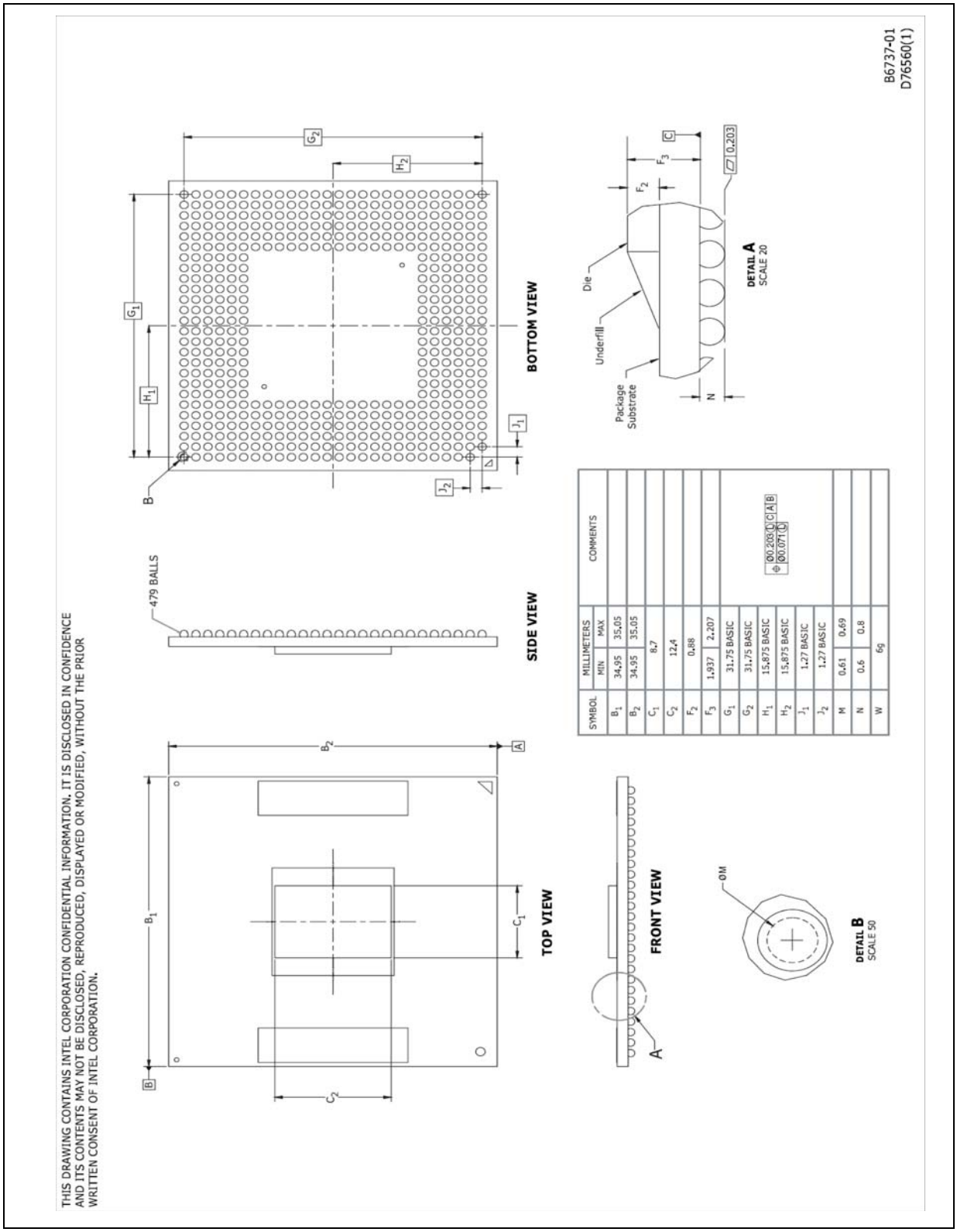


Figure 7. 1-MB on 6-MB Die (SV) Micro-FCBGA Package Drawing (Sheet 2 of 2)

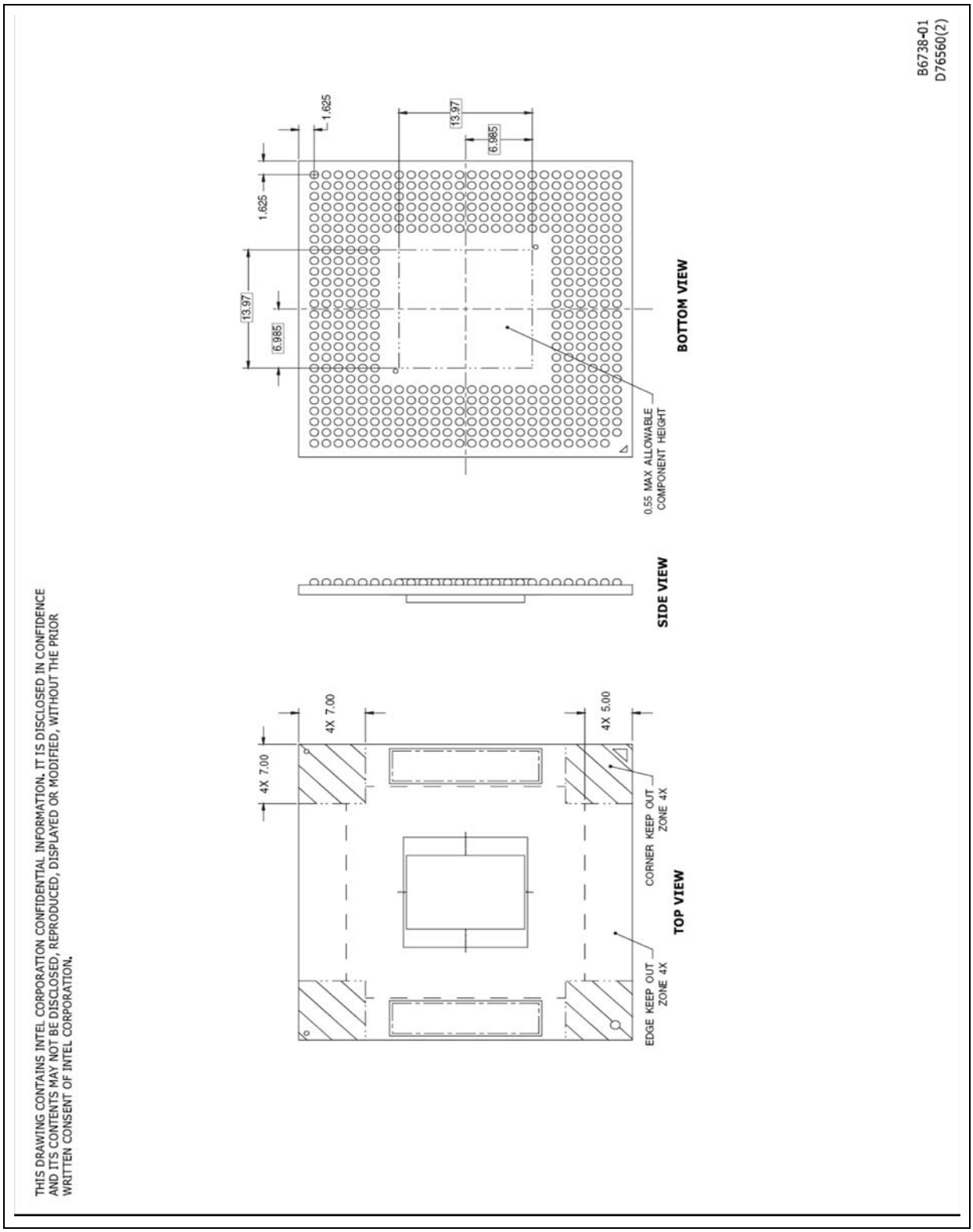
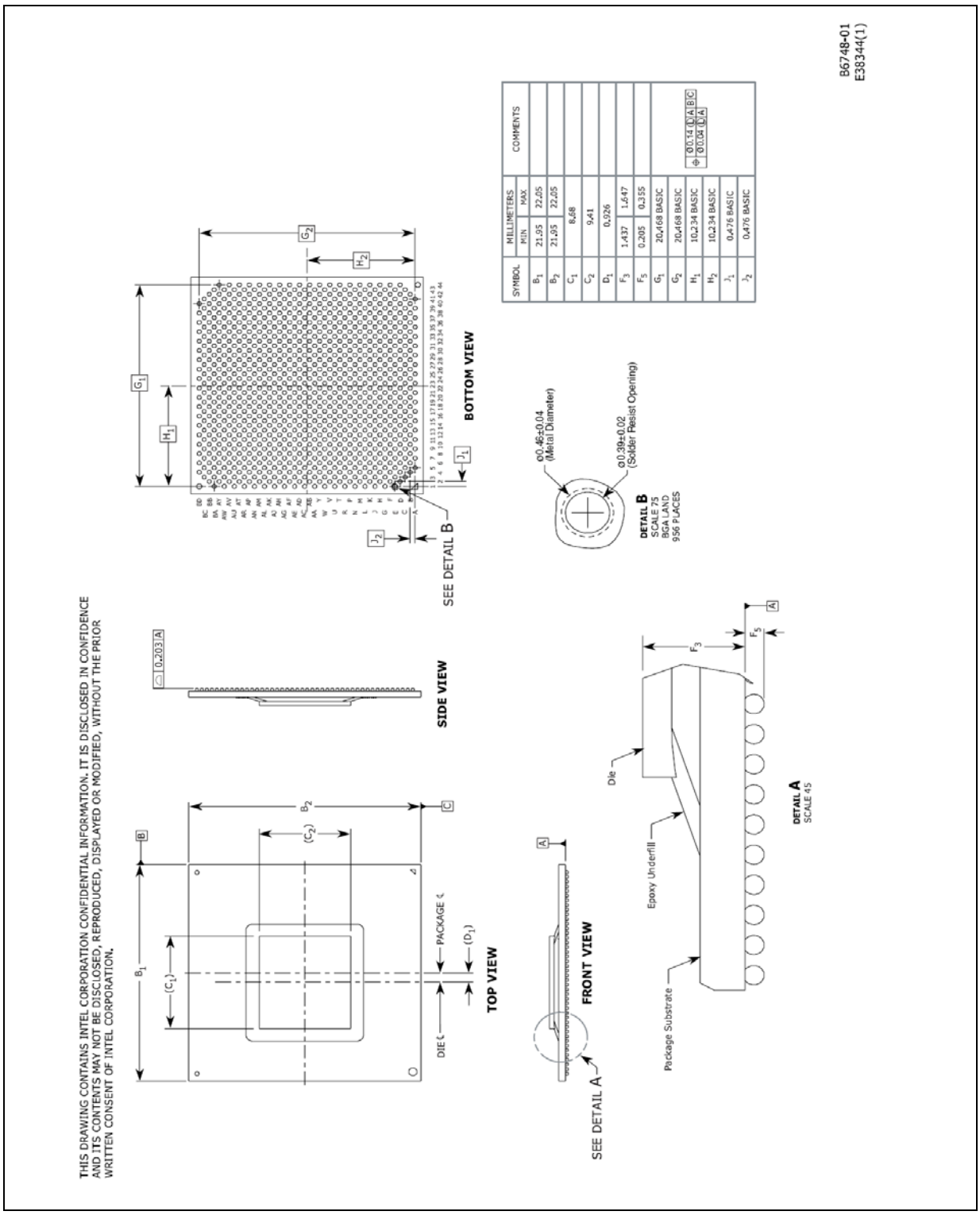


Figure 8. Processor (ULV SC) Die Micro-FCBGA Processor Package Drawing



4.2 Processor Pinout and Pin List

Figure 9 and Figure 10 show the processor (SV) pinout as viewed from the top of the package. Table 14 provides the pin list, arranged numerically by pin number.

Figure 11 through Figure 14 show the top view of the (ULV) processor package. Table 13 lists the processor ballout alphabetically by signal name. For signal descriptions, refer to Section 4.3.

Figure 9. Penryn Processor Pinout (Top Package View, Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A[1]		VSS	SMI#	VSS	FERR#	A20M#	VCC	VSS	VCC	VCC	VSS	VCC	VCC	A
B[2]		RSVD	INIT#	LINT1	DPSLP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	B
C	RESET#	VSS	TEST7	IGNNE#	VSS	LINT0	THERMTRIP#	VSS	VCC	VCC	VSS	VCC	VCC	C
D	VSS	RSVD	RSVD	VSS	STPCLK#	PWRGOOD	SLP#	VSS	VCC	VCC	VSS	VCC	VSS	D
E	DBSY#	BNR#	VSS	HITM#	DPRSTP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	E
F	BR0#	VSS	RS[0]#	RS[1]#	VSS	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VSS	F
G	VSS	TRDY#	RS[2]#	VSS	BPRI#	HIT#								G
H	ADS#	REQ[1]#	VSS	LOCK#	DEFER#	VSS								H
J	A[9]#	VSS	REQ[3]#	A[3]#	VSS	VCCP								J
K	VSS	REQ[2]#	REQ[0]#	VSS	A[6]#	VCCP								K
L	REQ[4]#	A[13]#	VSS	A[5]#	A[4]#	VSS								L
M	ADSTB[0]#	VSS	A[7]#	RSVD	VSS	VCCP								M
N	VSS	A[8]#	A[10]#	VSS	RSVD	VCCP								N
P	A[15]#	A[12]#	VSS	A[14]#	A[11]#	VSS								P
R	A[16]#	VSS	A[19]#	A[24]#	VSS	VCCP								R
T	VSS	RSVD	A[26]#	VSS	A[25]#	VCCP								T
U	A[23]#	A[30]#	VSS	A[21]#	A[18]#	VSS								U
V	ADSTB[1]#	VSS	RSVD	A[31]#	VSS	VCCP								V
W	VSS	A[27]#	A[32]#	VSS	A[28]#	A[20]#								W
Y	COMP[3]	A[17]#	VSS	A[29]#	A[22]#	VSS								Y
AA	COMP[2]	VSS	A[35]#	A[33]#	VSS	TDI	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AA
AB	VSS	A[34]#	TDO	VSS	TMS	TRST#	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AB
AC	PREQ#	PRDY#	VSS	BPM[3]#	TCK	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AC
AD	BPM[2]#	VSS	BPM[1]#	BPM[0]#	VSS	VID[0]	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AD
AE	VSS	VID[6]	VID[4]	VSS	VID[2]	PSI#	VSS SENSE	VSS	VCC	VCC	VSS	VCC	VCC	AE
AF	TEST5	VSS	VID[5]	VID[3]	VID[1]	VSS	VCC SENSE	VSS	VCC	VCC	VSS	VCC	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

1. Keying option for uFCPGA, A1 and B1 are de-populated.
2. Keying option for uFCBGA, A1 is de-populated and B1 is VSS.

Figure 10. Processor Pinout (Top Package View, Right Side)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VCC	VSS	VCC	VCC	VSS	VCC	BCLK[1]	BCLK[0]	VSS	THRMDA	VSS	TEST6	A
B	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	BSEL[0]	BSEL[1]	VSS	THRMDC	VCCA	B
C	VSS	VCC	VSS	VCC	VCC	VSS	DBR#	BSEL[2]	VSS	TEST1	TEST3	VSS	VCCA	C
D	VCC	VCC	VSS	VCC	VCC	VSS	IERR#	PROCHOT#	RSVD	VSS	DPWR#	TEST2	VSS	D
E	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[0]#	D[7]#	VSS	D[6]#	D[2]#	E
F	VCC	VCC	VSS	VCC	VCC	VSS	VCC	DRDY#	VSS	D[4]#	D[1]#	VSS	D[13]#	F
G								VCCP	D[3]#	VSS	D[9]#	D[5]#	VSS	G
H								VSS	D[12]#	D[15]#	VSS	DINV[0]#	DSTBP[0]#	H
J								VCCP	VSS	D[11]#	D[10]#	VSS	DSTBN[0]#	J
K								VCCP	D[14]#	VSS	D[8]#	D[17]#	VSS	K
L								VSS	D[22]#	D[20]#	VSS	D[29]#	DSTBN[1]#	L
M								VCCP	VSS	D[23]#	D[21]#	VSS	DSTBP[1]#	M
N								VCCP	D[16]#	VSS	DINV[1]#	D[31]#	VSS	N
P								VSS	D[26]#	D[25]#	VSS	D[24]#	D[18]#	P
R								VCCP	VSS	D[19]#	D[28]#	VSS	COMP[0]	R
T								VCCP	D[37]#	VSS	D[27]#	D[30]#	VSS	T
U								VSS	DINV[2]#	D[39]#	VSS	D[38]#	COMP[1]	U
V								VCCP	VSS	D[36]#	D[34]#	VSS	D[35]#	V
W								VCCP	D[41]#	VSS	D[43]#	D[44]#	VSS	W
Y								VSS	D[32]#	D[42]#	VSS	D[40]#	DSTBN[2]#	Y
AA	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[50]#	VSS	D[45]#	D[46]#	VSS	DSTBP[2]#	AA
AB	VCC	VCC	VSS	VCC	VCC	VSS	VCC	D[52]#	D[51]#	VSS	D[33]#	D[47]#	VSS	AB
AC	VSS	VCC	VSS	VCC	VCC	VSS	DINV[3]#	VSS	D[60]#	D[63]#	VSS	D[57]#	D[53]#	AC
AD	VCC	VCC	VSS	VCC	VCC	VSS	D[54]#	D[59]#	VSS	D[61]#	D[49]#	VSS	GTLREF	AD
AE	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[58]#	D[55]#	VSS	D[48]#	DSTBN[3]#	VSS	AE
AF	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[62]#	D[56]#	DSTBP[3]#	VSS	TEST4	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

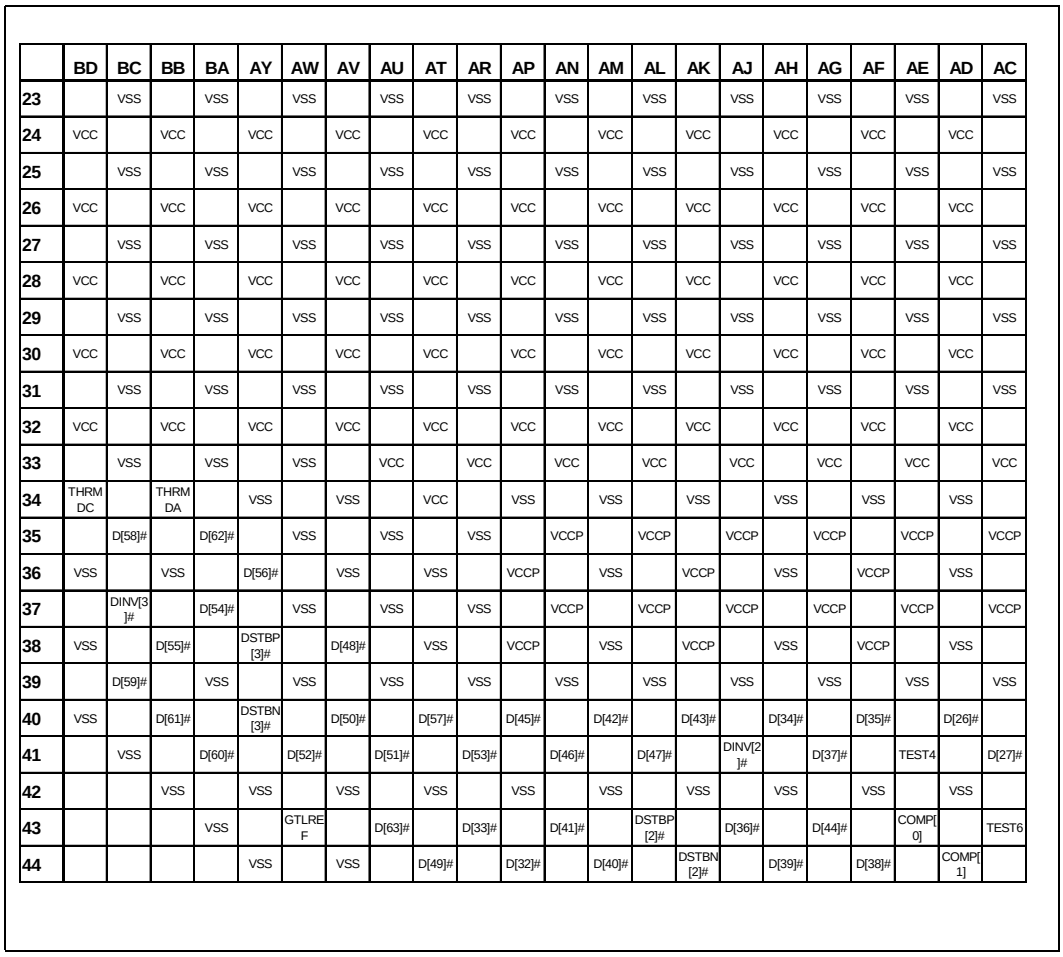
Figure 11. Processor Top View Upper Left Side

	BD	BC	BB	BA	AY	AW	AV	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC
1				VSS		VSS		TDO		A[35]#		A[17]#		A[31]#		A[30]#		A[19]#		COMP[2]		A[16]#
2			VSS		BPM[3]#		PREQ#		A[22]#		A[34]#		A[32]#		A[21]#		A[23]#		COMP[3]		A[11]#	
3		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
4	VSS		VID[5]		VID[6]		TCK		A[20]#		A[28]#		A[27]#		A[18]#		A[26]#		A[24]#		A[12]#	
5		VID[4]		BPM[2]#		TMS		A[33]#		A[29]#		ADSTB[1]#		RSVD04		A[25]#		RSVD03		A[14]#		A[10]#
6	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
7		VID[1]		BPM[1]#		TDI		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
8	VID[0]		VID[3]		BPM[0]#		TRST#		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
9		VSS		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
10	PSI#		VID[2]		TEST5		PRDY#		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
11		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
12	VCCSENSE		VSS		VSS		VSS		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
13		VSSSENSE		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
14	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCCP		VCCP		VCCP		VCCP	
15		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
16	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
17		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
18	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
19		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
20	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
21		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
22	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	

Figure 12. Processor Top View Upper Right Side

	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1		A[7]#		A[5]#		REQ[2]#		REQ[0]#		LOCK#		TRDY#		DBSY#		VSS		VSS				
2	A[15]#		RSVD02		RSVD01		A[9]#		A[3]#		BR0#		RS[0]#		HIT#		HITM#		VSS			
3		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		
4	A[8]#		ADSTB[0]#		A[4]#		A[6]#		REQ[3]#		ADS#		RS[2]#		RS[1]#		RSVD06		FERR#		VSS	
5		A[13]#		REQ[4]#		VSS		REQ[1]#		DEFER#		BPRI#		BNR#		RESET#		SMI#		LINT1		VSS
6	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
7		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		DBR#		DPRSTP#		PWRGOOD		A20M#		VSS
8	VSS		VSS		VSS		VSS		VSS		VSS		VSS		RSVD07		STPCLK#		INIT#		DPSLP#	
9		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		RSVD05		VSS		VSS		LINT0		VSS
10	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS		IGNNE#		SLP#		THERMTRIP#	
11		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VSS		VSS
12	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VCCP		VCCP		VCCP		VCCP	
13		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
14	VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP	
15		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
16	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
17		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
18	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
19		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
20	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
21		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
22	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	

Figure 13. Processor Top View Lower Left Side



	BD	BC	BB	BA	AY	AW	AV	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC
23		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
24	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
25		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
26	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
27		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
28	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
29		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
30	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
31		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
32	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
33		VSS		VSS		VSS		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC
34	THRMDC		THRMDA		VSS		VSS		VCC		VSS		VSS		VSS		VSS		VSS		VSS	
35		D[58]#		D[62]#		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
36	VSS		VSS		D[56]#		VSS		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
37		DINV[3]#		D[54]#		VSS		VSS		VSS		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP
38	VSS		D[55]#		DSTBP[3]#		D[48]#		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS	
39		D[59]#		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
40	VSS		D[61]#		DSTBN[3]#		D[50]#		D[57]#		D[45]#		D[42]#		D[43]#		D[34]#		D[35]#		D[26]#	
41		VSS		D[60]#		D[52]#		D[51]#		D[53]#		D[46]#		D[47]#		DINV[2]#		D[37]#		TEST4		D[27]#
42			VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
43				VSS		GTLREF		D[63]#		D[33]#		D[41]#		DSTBP[2]#		D[36]#		D[44]#		COMP[0]		TEST6
44					VSS		VSS		D[49]#		D[32]#		D[40]#		DSTBN[2]#		D[39]#		D[38]#		COMP[1]	

Figure 14. Processor Top View Lower Right Side

	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
23		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
24	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
25		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
26	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
27		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
28	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
29		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
30	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC	
31		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
32	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCCP		VCCP	
33		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCCP		VCCP		VCCP
34	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VCCP		VCCA		VCCA	
35		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		BCLK[1]		BCLK[0]
36	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VCCP		VCCP		VSS		VSS	
37		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VCCP		VSS		TEST1		BSEL[1]		BSEL[0]
38	VCCP		VSS		VCCP		VSS		VCCP		VSS		VCCP		VSS		DRDY#		PROCHOT#		BSEL[2]	
39		VSS		VSS		VSS		VSS		VSS		VSS		VSS		D[6]#		VSS		VSS		VSS
40	D[25]#		D[29]#		D[17]#		D[11]#		DINV[0]#		D[12]#		DSTBN[0]#		D[4]#		D[0]#		TEST2		IERR#	
41		D[24]#		D[21]#		D[23]#		D[20]#		D[10]#		D[8]#		DSTBP[0]#		D[13]#		D[7]#		DPWR#		VSS
42	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	
43		D[28]#		DSTBP[1]#		DSTBN[1]#		DINV[1]#		D[22]#		D[15]#		D[3]#		D[1]#		D[2]#		TEST3		
44	D[19]#		D[30]#		D[18]#		D[31]#		D[16]#		D[14]#		D[9]#		D[5]#		VSS		VSS			

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
A[3]#	P2
A[4]#	V4
A[5]#	W1
A[6]#	T4
A[7]#	AA1
A[8]#	AB4
A[9]#	T2
A[10]#	AC5
A[11]#	AD2
A[12]#	AD4
A[13]#	AA5
A[14]#	AE5
A[15]#	AB2
A[16]#	AC1
A[17]#	AN1
A[18]#	AK4
A[19]#	AG1
A[20]#	AT4
A[21]#	AK2
A[22]#	AT2
A[23]#	AH2
A[24]#	AF4
A[25]#	AJ5
A[26]#	AH4
A[27]#	AM4
A[28]#	AP4
A[29]#	AR5
A[30]#	AJ1
A[31]#	AL1
A[32]#	AM2
A[33]#	AU5
A[34]#	AP2
A[35]#	AR1
A20M#	C7
ADS#	M4
ADSTB[0]#	Y4
ADSTB[1]#	AN5

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
BCLK[0]	A35
BCLK[1]	C35
BNR#	J5
BPM[0]#	AY8
BPM[1]#	BA7
BPM[2]#	BA5
BPM[3]#	AY2
BPRI#	L5
BR0#	M2
BSEL[0]	A37
BSEL[1]	C37
BSEL[2]	B38
COMP[0]	AE43
COMP[1]	AD44
COMP[2]	AE1
COMP[3]	AF2
D[0]#	F40
D[1]#	G43
D[2]#	E43
D[3]#	J43
D[4]#	H40
D[5]#	H44
D[6]#	G39
D[7]#	E41
D[8]#	L41
D[9]#	K44
D[10]#	N41
D[11]#	T40
D[12]#	M40
D[13]#	G41
D[14]#	M44
D[15]#	L43
D[16]#	P44
D[17]#	V40
D[18]#	V44
D[19]#	AB44
D[20]#	R41

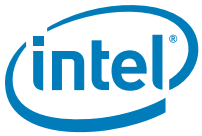


Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
D[21]#	W41
D[22]#	N43
D[23]#	U41
D[24]#	AA41
D[25]#	AB40
D[26]#	AD40
D[27]#	AC41
D[28]#	AA43
D[29]#	Y40
D[30]#	Y44
D[31]#	T44
D[32]#	AP44
D[33]#	AR43
D[34]#	AH40
D[35]#	AF40
D[36]#	AJ43
D[37]#	AG41
D[38]#	AF44
D[39]#	AH44
D[40]#	AM44
D[41]#	AN43
D[42]#	AM40
D[43]#	AK40
D[44]#	AG43
D[45]#	AP40
D[46]#	AN41
D[47]#	AL41
D[48]#	AV38
D[49]#	AT44
D[50]#	AV40
D[51]#	AU41
D[52]#	AW41
D[53]#	AR41
D[54]#	BA37
D[55]#	BB38
D[56]#	AY36
D[57]#	AT40

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
D[58]#	BC35
D[59]#	BC39
D[60]#	BA41
D[61]#	BB40
D[62]#	BA35
D[63]#	AU43
DBR#	J7
DBSY#	J1
DEFER#	N5
DINV[0]#	P40
DINV[1]#	R43
DINV[2]#	AJ41
DINV[3]#	BC37
DPRSTP#	G7
DPSLP#	B8
DPWR#	C41
DRDY#	F38
DSTBN[0]#	K40
DSTBN[1]#	U43
DSTBN[2]#	AK44
DSTBN[3]#	AY40
DSTBP[0]#	J41
DSTBP[1]#	W43
DSTBP[2]#	AL43
DSTBP[3]#	AY38
FERR#	D4
GTLREF	AW43
HIT#	H2
HITM#	F2
IERR#	B40
IGNNE#	F10
INIT#	D8
LINT0	C9
LINT1	C5
LOCK#	N1
PRDY#	AV10
PREQ#	AV2

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
PROCHOT#	D38
PSI#	BD10
PWRGOOD	E7
REQ[0]#	R1
REQ[1]#	R5
REQ[2]#	U1
REQ[3]#	P4
REQ[4]#	W5
RESET#	G5
RS[0]#	K2
RS[1]#	H4
RS[2]#	K4
RSVD01	V2
RSVD02	Y2
RSVD03	AG5
RSVD04	AL5
RSVD05	J9
RSVD06	F4
RSVD07	H8
SLP#	D10
SMI#	E5
STPCLK#	F8
TCK	AV4
TDI	AW7
TDO	AU1
TEST1	E37
TEST2	D40
TEST3	C43
TEST4	AE41
TEST5	AY10
TEST6	AC43
THERMTRIP#	B10
THRMDA	BB34
THRMDC	BD34
TMS	AW5
TRDY#	L1
TRST#	AV8

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCC	AA33
VCC	AB16
VCC	AB18
VCC	AB20
VCC	AB22
VCC	AB24
VCC	AB26
VCC	AB28
VCC	AB30
VCC	AB32
VCC	AC33
VCC	AD16
VCC	AD18
VCC	AD20
VCC	AD22
VCC	AD24
VCC	AD26
VCC	AD28
VCC	AD30
VCC	AD32
VCC	AE33
VCC	AF16
VCC	AF18
VCC	AF20
VCC	AF22
VCC	AF24
VCC	AF26
VCC	AF28
VCC	AF30
VCC	AF32
VCC	AG33
VCC	AH16
VCC	AH18
VCC	AH20
VCC	AH22
VCC	AH24
VCC	AH26

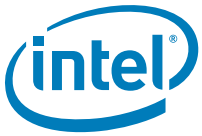


Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCC	AH28
VCC	AH30
VCC	AH32
VCC	AJ33
VCC	AK16
VCC	AK18
VCC	AK20
VCC	AK22
VCC	AK24
VCC	AK26
VCC	AK28
VCC	AK30
VCC	AK32
VCC	AL33
VCC	AM14
VCC	AM16
VCC	AM18
VCC	AM20
VCC	AM22
VCC	AM24
VCC	AM26
VCC	AM28
VCC	AM30
VCC	AM32
VCC	AN33
VCC	AP14
VCC	AP16
VCC	AP18
VCC	AP20
VCC	AP22
VCC	AP24
VCC	AP26
VCC	AP28
VCC	AP30
VCC	AP32
VCC	AR33
VCC	AT14

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCC	AT16
VCC	AT18
VCC	AT20
VCC	AT22
VCC	AT24
VCC	AT26
VCC	AT28
VCC	AT30
VCC	AT32
VCC	AT34
VCC	AU33
VCC	AV14
VCC	AV16
VCC	AV18
VCC	AV20
VCC	AV22
VCC	AV24
VCC	AV26
VCC	AV28
VCC	AV30
VCC	AV32
VCC	AY14
VCC	AY16
VCC	AY18
VCC	AY20
VCC	AY22
VCC	AY24
VCC	AY26
VCC	AY28
VCC	AY30
VCC	AY32
VCC	B16
VCC	B18
VCC	B20
VCC	B22
VCC	B24
VCC	B26

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCC	B28
VCC	B30
VCC	BB14
VCC	BB16
VCC	BB18
VCC	BB20
VCC	BB22
VCC	BB24
VCC	BB26
VCC	BB28
VCC	BB30
VCC	BB32
VCC	BD14
VCC	BD16
VCC	BD18
VCC	BD20
VCC	BD22
VCC	BD24
VCC	BD26
VCC	BD28
VCC	BD30
VCC	BD32
VCC	D16
VCC	D18
VCC	D20
VCC	D22
VCC	D24
VCC	D26
VCC	D28
VCC	D30
VCC	F16
VCC	F18
VCC	F20
VCC	F22
VCC	F24
VCC	F26
VCC	F28

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCC	F30
VCC	F32
VCC	G33
VCC	H16
VCC	H18
VCC	H20
VCC	H22
VCC	H24
VCC	H26
VCC	H28
VCC	H30
VCC	H32
VCC	J33
VCC	K16
VCC	K18
VCC	K20
VCC	K22
VCC	K24
VCC	K26
VCC	K28
VCC	K30
VCC	K32
VCC	L33
VCC	M16
VCC	M18
VCC	M20
VCC	M22
VCC	M24
VCC	M26
VCC	M28
VCC	M30
VCC	M32
VCC	N33
VCC	P16
VCC	P18
VCC	P20
VCC	P22

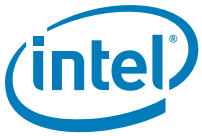


Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCC	P24
VCC	P26
VCC	P28
VCC	P30
VCC	P32
VCC	R33
VCC	T16
VCC	T18
VCC	T20
VCC	T22
VCC	T24
VCC	T26
VCC	T28
VCC	T30
VCC	T32
VCC	U33
VCC	V16
VCC	V18
VCC	V20
VCC	V22
VCC	V24
VCC	V26
VCC	V28
VCC	V30
VCC	V32
VCC	W33
VCC	Y16
VCC	Y18
VCC	Y20
VCC	Y22
VCC	Y24
VCC	Y26
VCC	Y28
VCC	Y30
VCC	Y32
VCCA	B34
VCCA	D34

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCCP	A13
VCCP	A33
VCCP	AA7
VCCP	AA9
VCCP	AA11
VCCP	AA13
VCCP	AA35
VCCP	AA37
VCCP	AB10
VCCP	AB12
VCCP	AB14
VCCP	AB36
VCCP	AB38
VCCP	AC7
VCCP	AC9
VCCP	AC11
VCCP	AC13
VCCP	AC35
VCCP	AC37
VCCP	AD14
VCCP	AE7
VCCP	AE9
VCCP	AE11
VCCP	AE13
VCCP	AE35
VCCP	AE37
VCCP	AF10
VCCP	AF12
VCCP	AF14
VCCP	AF36
VCCP	AF38
VCCP	AG7
VCCP	AG9
VCCP	AG11
VCCP	AG13
VCCP	AG35
VCCP	AG37

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCCP	AH14
VCCP	AJ7
VCCP	AJ9
VCCP	AJ11
VCCP	AJ13
VCCP	AJ35
VCCP	AJ37
VCCP	AK10
VCCP	AK12
VCCP	AK14
VCCP	AK36
VCCP	AK38
VCCP	AL7
VCCP	AL9
VCCP	AL11
VCCP	AL13
VCCP	AL35
VCCP	AL37
VCCP	AN7
VCCP	AN9
VCCP	AN11
VCCP	AN13
VCCP	AN35
VCCP	AN37
VCCP	AP10
VCCP	AP12
VCCP	AP36
VCCP	AP38
VCCP	AR7
VCCP	AR9
VCCP	AR11
VCCP	AR13
VCCP	AU11
VCCP	AU13
VCCP	B12
VCCP	B14
VCCP	B32

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCCP	C13
VCCP	C33
VCCP	D12
VCCP	D14
VCCP	D32
VCCP	E11
VCCP	E13
VCCP	E33
VCCP	E35
VCCP	F12
VCCP	F14
VCCP	F34
VCCP	F36
VCCP	G11
VCCP	G13
VCCP	G35
VCCP	H12
VCCP	H14
VCCP	H36
VCCP	J11
VCCP	J13
VCCP	J35
VCCP	J37
VCCP	K10
VCCP	K12
VCCP	K14
VCCP	K36
VCCP	K38
VCCP	L7
VCCP	L9
VCCP	L11
VCCP	L13
VCCP	L35
VCCP	L37
VCCP	M14
VCCP	N7
VCCP	N9

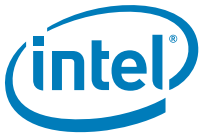


Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VCCP	N11
VCCP	N13
VCCP	N35
VCCP	N37
VCCP	P10
VCCP	P12
VCCP	P14
VCCP	P36
VCCP	P38
VCCP	R7
VCCP	R9
VCCP	R11
VCCP	R13
VCCP	R35
VCCP	R37
VCCP	T14
VCCP	U7
VCCP	U9
VCCP	U11
VCCP	U13
VCCP	U35
VCCP	U37
VCCP	V10
VCCP	V12
VCCP	V14
VCCP	V36
VCCP	V38
VCCP	W7
VCCP	W9
VCCP	W11
VCCP	W13
VCCP	W35
VCCP	W37
VCCP	Y14
VCCSENSE	BD12
VID[0]	BD8
VID[1]	BC7

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VID[2]	BB10
VID[3]	BB8
VID[4]	BC5
VID[5]	BB4
VID[6]	AY4
VSS	A5
VSS	A7
VSS	A9
VSS	A11
VSS	A15
VSS	A17
VSS	A19
VSS	A21
VSS	A23
VSS	A25
VSS	A27
VSS	A29
VSS	A31
VSS	A39
VSS	A41
VSS	AA3
VSS	AA15
VSS	AA17
VSS	AA19
VSS	AA21
VSS	AA23
VSS	AA25
VSS	AA27
VSS	AA29
VSS	AA31
VSS	AA39
VSS	AB6
VSS	AB8
VSS	AB34
VSS	AB42
VSS	AC3
VSS	AC15

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	AC17
VSS	AC19
VSS	AC21
VSS	AC23
VSS	AC25
VSS	AC27
VSS	AC29
VSS	AC31
VSS	AC39
VSS	AD6
VSS	AD8
VSS	AD10
VSS	AD12
VSS	AD34
VSS	AD36
VSS	AD38
VSS	AD42
VSS	AE3
VSS	AE15
VSS	AE17
VSS	AE19
VSS	AE21
VSS	AE23
VSS	AE25
VSS	AE27
VSS	AE29
VSS	AE31
VSS	AE39
VSS	AF6
VSS	AF8
VSS	AF34
VSS	AF42
VSS	AG3
VSS	AG15
VSS	AG17
VSS	AG19
VSS	AG21

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	AG23
VSS	AG25
VSS	AG27
VSS	AG29
VSS	AG31
VSS	AG39
VSS	AH6
VSS	AH8
VSS	AH10
VSS	AH12
VSS	AH34
VSS	AH36
VSS	AH38
VSS	AH42
VSS	AJ3
VSS	AJ15
VSS	AJ17
VSS	AJ19
VSS	AJ21
VSS	AJ23
VSS	AJ25
VSS	AJ27
VSS	AJ29
VSS	AJ31
VSS	AJ39
VSS	AK6
VSS	AK8
VSS	AK34
VSS	AK42
VSS	AL3
VSS	AL15
VSS	AL17
VSS	AL19
VSS	AL21
VSS	AL23
VSS	AL25
VSS	AL27

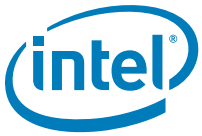


Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	AL29
VSS	AL31
VSS	AL39
VSS	AM6
VSS	AM8
VSS	AM10
VSS	AM12
VSS	AM34
VSS	AM36
VSS	AM38
VSS	AM42
VSS	AN3
VSS	AN15
VSS	AN17
VSS	AN19
VSS	AN21
VSS	AN23
VSS	AN25
VSS	AN27
VSS	AN29
VSS	AN31
VSS	AN39
VSS	AP6
VSS	AP8
VSS	AP34
VSS	AP42
VSS	AR3
VSS	AR15
VSS	AR17
VSS	AR19
VSS	AR21
VSS	AR23
VSS	AR25
VSS	AR27
VSS	AR29
VSS	AR31
VSS	AR35

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	AR37
VSS	AR39
VSS	AT6
VSS	AT8
VSS	AT10
VSS	AT12
VSS	AT36
VSS	AT38
VSS	AT42
VSS	AU3
VSS	AU7
VSS	AU9
VSS	AU15
VSS	AU17
VSS	AU19
VSS	AU21
VSS	AU23
VSS	AU25
VSS	AU27
VSS	AU29
VSS	AU31
VSS	AU35
VSS	AU37
VSS	AU39
VSS	AV6
VSS	AV12
VSS	AV34
VSS	AV36
VSS	AV42
VSS	AV44
VSS	AW1
VSS	AW3
VSS	AW9
VSS	AW11
VSS	AW13
VSS	AW15
VSS	AW17

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	AW19
VSS	AW21
VSS	AW23
VSS	AW25
VSS	AW27
VSS	AW29
VSS	AW31
VSS	AW33
VSS	AW35
VSS	AW37
VSS	AW39
VSS	AY6
VSS	AY12
VSS	AY34
VSS	AY42
VSS	AY44
VSS	B4
VSS	B6
VSS	B36
VSS	B42
VSS	BA1
VSS	BA3
VSS	BA9
VSS	BA11
VSS	BA13
VSS	BA15
VSS	BA17
VSS	BA19
VSS	BA21
VSS	BA23
VSS	BA25
VSS	BA27
VSS	BA29
VSS	BA31
VSS	BA33
VSS	BA39
VSS	BA43

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	BB2
VSS	BB6
VSS	BB12
VSS	BB36
VSS	BB42
VSS	BC3
VSS	BC9
VSS	BC11
VSS	BC15
VSS	BC17
VSS	BC19
VSS	BC21
VSS	BC23
VSS	BC25
VSS	BC27
VSS	BC29
VSS	BC31
VSS	BC33
VSS	BC41
VSS	BD4
VSS	BD6
VSS	BD36
VSS	BD38
VSS	BD40
VSS	C3
VSS	C11
VSS	C15
VSS	C17
VSS	C19
VSS	C21
VSS	C23
VSS	C25
VSS	C27
VSS	C29
VSS	C31
VSS	C39
VSS	D2

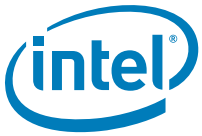


Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	D6
VSS	D36
VSS	D42
VSS	D44
VSS	E1
VSS	E3
VSS	E9
VSS	E15
VSS	E17
VSS	E19
VSS	E21
VSS	E23
VSS	E25
VSS	E27
VSS	E29
VSS	E31
VSS	E39
VSS	F6
VSS	F42
VSS	F44
VSS	G1
VSS	G3
VSS	G9
VSS	G15
VSS	G17
VSS	G19
VSS	G21
VSS	G23
VSS	G25
VSS	G27
VSS	G29
VSS	G31
VSS	G37
VSS	H6
VSS	H10
VSS	H34
VSS	H38

Table 13. Signal Listing by Ball Number

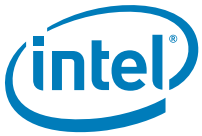
Signal Name	Ball Number
VSS	H42
VSS	J3
VSS	J15
VSS	J17
VSS	J19
VSS	J21
VSS	J23
VSS	J25
VSS	J27
VSS	J29
VSS	J31
VSS	J39
VSS	K6
VSS	K8
VSS	K34
VSS	K42
VSS	L3
VSS	L15
VSS	L17
VSS	L19
VSS	L21
VSS	L23
VSS	L25
VSS	L27
VSS	L29
VSS	L31
VSS	L39
VSS	M6
VSS	M8
VSS	M10
VSS	M12
VSS	M34
VSS	M36
VSS	M38
VSS	M42
VSS	N3
VSS	N15

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	N17
VSS	N19
VSS	N21
VSS	N23
VSS	N25
VSS	N27
VSS	N29
VSS	N31
VSS	N39
VSS	P6
VSS	P8
VSS	P34
VSS	P42
VSS	R3
VSS	R15
VSS	R17
VSS	R19
VSS	R21
VSS	R23
VSS	R25
VSS	R27
VSS	R29
VSS	R31
VSS	R39
VSS	T6
VSS	T8
VSS	T10
VSS	T12
VSS	T34
VSS	T36
VSS	T38
VSS	T42
VSS	U3
VSS	U5
VSS	U15
VSS	U17

Table 13. Signal Listing by Ball Number

Signal Name	Ball Number
VSS	U19
VSS	U21
VSS	U23
VSS	U25
VSS	U27
VSS	U29
VSS	U31
VSS	U39
VSS	V6
VSS	V8
VSS	V34
VSS	V42
VSS	W3
VSS	W15
VSS	W17
VSS	W19
VSS	W21
VSS	W23
VSS	W25
VSS	W27
VSS	W29
VSS	W31
VSS	W39
VSS	Y6
VSS	Y8
VSS	Y10
VSS	Y12
VSS	Y34
VSS	Y36
VSS	Y38
VSS	Y42
VSSSENSE	BC13



4.3 Alphabetical Signals Reference

Table 14. Signal Description (Sheet 1 of 9)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[35:3]# are source-synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps, which are sampled before RESET# is deasserted.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address Bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/ output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[35:17]# — ADSTB[1]#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Table 14. Signal Description (Sheet 2 of 9)

Name	Type	Description
BPM[2:1]# BPM[3,0]#	Output Input/ Output	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all processor FSB agents.This includes debug or performance monitoring tools. Refer to the appropriate *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms for more detailed information*.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and GMCH (High Priority Agent).
BSEL[2:0]	Output	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency.
COMP[3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the appropriate platform design guide for more details on implementation.
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN# / DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.

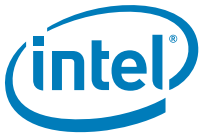


Table 14. Signal Description (Sheet 3 of 9)

Name	Type	Description
DBR#	Output	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or input/ output agent. This signal must connect the appropriate pins of both FSB agents.
DINV[3:0]#	Input/ Output	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** **Bus Signal** — **Data Bus Signals** DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPRSTP#	Input	DPRSTP#, when asserted on the platform, causes the processor to transition from the Deep Sleep State to the Deeper Sleep state or C6 state. To return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the ICH9M chipset.
DPSLP#	Input	DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. To return to the Sleep State, DPSLP# must be deasserted. DPSLP# is driven by the ICH9M chipset.
DPWR#	Input/ Output	DPWR# is a control signal used by the chipset to reduce power on the processor data bus input buffers. The processor drives this pin during dynamic FSB frequency switching.
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.

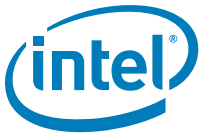


Table 14. Signal Description (Sheet 4 of 9)

Name	Type	Description
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** — **Associated Strobe** D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** — **Associated Strobe** D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#
FERR#/PBE#	Output	FERR# (Floating-point Error)/PBE# (Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel® 387 coprocessor, and is included for compatibility with systems using Microsoft MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volumes 3A and 3B of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *Intel® Processor Identification and CPUID Instruction* application note. Refer to the appropriate platform design guide for termination requirements.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a Logical 0 or Logical 1. Refer to the appropriate platform design guide for details on GTLREF implementation.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall that can be continued by reasserting HIT# and HITM# together.

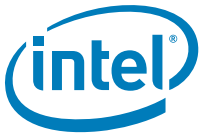


Table 14. Signal Description (Sheet 5 of 9)

Name	Type	Description
IERR#	Output	IERR# (Internal Error) is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. Refer to the appropriate platform design guide for termination requirements.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in Control Register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/ output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active-to-inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST) Refer to the appropriate platform design guide for termination requirements.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward-compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/ INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.

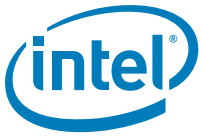


Table 14. Signal Description (Sheet 6 of 9)

Name	Type	Description
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness. Refer to the appropriate *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms for more detailed information.*
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor. Refer to the appropriate *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms for more detailed information.*
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. By default PROCHOT# is configured as an output. The processor must be enabled via the BIOS for PROCHOT# to be configured as bidirectional. Refer to the appropriate platform design guide for termination requirements. This signal may require voltage translation on the motherboard. Refer to the appropriate platform design guide for more details.
PSI#	Output	Processor Power Status Indicator signal. This signal is asserted when the processor is both in the normal state (HFM to LFM) and in lower power states (Deep Sleep and Deeper Sleep). Refer to the *Intel® MVP-6 Mobile Processor and Mobile Chipset Voltage Regulation Specification* for more details on the PSI# signal.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal remains low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. Refer to the appropriate platform design guide for termination requirements.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

Table 14. Signal Description (Sheet 7 of 9)

Name	Type	Description
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. Refer to the appropriate platform design guide for termination requirements and implementation details. There is a 55 Ω (nominal) on die pull-up resistor on this signal.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Refer to the appropriate platform design guide for details.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued and the processor begins program execution from the SMM handler. If an SMI# is asserted during the deassertion of RESET#, then the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.

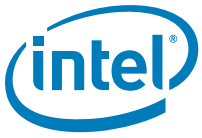


Table 14. Signal Description (Sheet 8 of 9)

Name	Type	Description
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3, TEST4, TEST5, TEST6	Input	Refer to the appropriate platform design guide for further TEST1, TEST2, TEST3, TEST4, TEST5, TEST6 termination requirements and implementation details.
THRMDA	Other	Thermal Diode Anode.
THRMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125 °C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. Refer to the appropriate platform design guide for termination requirements.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Refer to the appropriate *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms for more detailed information.*
V_{CC}	Input	Processor core power supply.
V_{SS}	Input	Processor core ground node.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLLs. Refer to the appropriate platform design guide for complete implementation details.
V_{CCP}	Input	Processor I/O Power Supply.

Table 14. Signal Description (Sheet 9 of 9)

Name	Type	Description
V_{CC_SENSE}	Output	V_{CC_SENSE} together with V_{SS_SENSE} are voltage feedback signals to Intel® MVP6 that control the 2.1 mΩ loadline at the processor die. It should be used to sense voltage near the silicon with little noise. Refer to the platform design guide for termination and routing recommendations.
VID[6:0]	Output	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
V_{SS_SENSE}	Output	V_{SS_SENSE} together with V_{CC_SENSE} are voltage feedback signals to Intel MVP6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense ground near the silicon with little noise. Refer to the platform design guide for termination and routing recommendations.

§

5 Thermal Specifications and Design Considerations

Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete thermal solution includes both component and system-level thermal management features. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding thermal design power (TDP).

Caution: Operating the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system.

Table 15. Power Specifications for the Dual-Core and Single-Core Standard Voltage (SV) Processors

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	900	2.2 GHz	35			W	1, 4, 5
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power		—	—	13.9	W	2, 6
P_{SLP}	Sleep Power		—	—	13.1	W	2, 6
P_{DPSLP}	Deep Sleep Power		—	—	5.5	W	2, 6
T_J	Junction Temperature		0	—	105	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel® Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. At Tj of 105 ^{o}C.
6. At Tj of 50 ^{o}C.

Table 16. Power Specifications for the Single-Core Ultra Low Voltage Processors (ULV, 10 W)

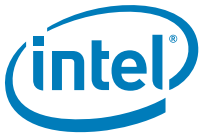
Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	723	1.2 GHz	10			W	1, 4, 5
	743	1.3 GHz	10			W	1, 4, 5
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power		—	—	2.9	W	2, 6
P_{SLP}	Sleep Power		—	—	2.5	W	2, 6
P_{DPSLP}	Deep Sleep Power		—	—	1.3	W	2, 6
T_J	Junction Temperature		0	—	100	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. At Tj of 100 ^{o}C
6. At Tj of 50 °C

Table 17. Power Specifications for the Single-Core Ultra Low Voltage (ULV, 5.5 W) Processors

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	722	1.2 GHz	5.5			W	1, 4, 5
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power		—	—	2.1	W	2, 6
P_{SLP}	Sleep Power		—	—	1.8	W	2, 6
P_{DPSLP}	Deep Sleep Power		—	—	0.7	W	2, 7
T_J	Junction Temperature		0	—	100	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.



4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. At Tj of 100 ^{o}C
6. At Tj of 50 °C
7. At Tj of 35 °C

5.1 Monitoring Die Temperature

The processor incorporates three methods of monitoring die temperature:

- Thermal Diode
- Intel® Thermal Monitor
- Digital Thermal Sensor

5.1.1 Thermal Diode

Intel's processors utilize an SMBus thermal sensor to read back the voltage/current characteristics of a substrate PNP transistor. Since these characteristics are a function of temperature, in principle one can use these parameters to calculate silicon temperature values. For older silicon process technologies (i.e., Intel Core 2 Duo Mobile Processor and earlier processor), it is possible to simplify the voltage/current and temperature relationships by treating the substrate transistor as though it were a simple diffusion diode. In this case, the assumption is that the beta of the transistor does not impact the calculated temperature values. The resultant "diode" model essentially predicts a quasi linear relationship between the base/emitter voltage differential of the PNP transistor and the applied temperature (one of the proportionality constants in this relationship is processor specific, and is known as the diode ideality factor). Realization of this relationship is accomplished with the SMBus thermal sensor that is connected to the transistor.

The processor is built on Intel's advanced 45-nm processor technology. Due to this new highly advanced processor technology, it is no longer possible to model the substrate transistor as a simple diode. To accurately calculate silicon temperature one must use a full bi-polar junction transistor-type model. In this model, the voltage/current and temperature characteristics include an additional process dependant parameter which is known as the transistor "beta". System designers should be aware that the current thermal sensors on Santa Rosa platforms may not be configured to account for "beta" and should work with their SMB thermal sensor vendors to ensure they have a part capable of reading the thermal diode in BJT model.

Offset between the thermal diode-based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the processor Model-Specific Register (MSR).

Table 18 to Table 19 provide the diode interface and transistor model specifications.

Table 18. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	A24	Thermal diode anode
THERMDC	A25	Thermal diode cathode

Table 19. Thermal Diode Parameters Using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	—	200	µA	1
I_E	Emitter Current	5	—	200	µA	1
n_Q	Transistor Ideality	0.997	1.001	1.008		2, 3, 4
Beta		0.1	0.4	0.5		2, 3
R_T	Series Resistance	3.0	4.5	7.0	Ω	2

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50-100 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_Q kT} - 1)$$

where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5.1.2 Intel® Thermal Monitor

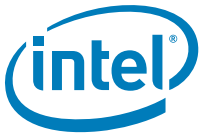
The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power-intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

The automatic mode is called Intel Thermal Monitor 1 (TM1). This modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed-dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip



point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processors.

TM1 features are also referred to as Adaptive Thermal Monitoring features.

The TCC may also be activated via on-demand mode. If Bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via Bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, low-power states, hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low-power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low-power state and the processor junction temperature drops below the thermal trip point. However, PROCHOT# will de-assert for the duration of Intel Deep Power Down (C6) state residency.

If Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

5.1.3 Digital Thermal Sensor

The processor also contains an on-die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). Each core of the processor will have a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the

preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low-power state).

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below $T_{J,max}$. Catastrophic temperature conditions are detectable via an Out Of Specification status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Specification status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor (TM1) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 hardware thermal control mechanism will activate. The DTS and TM1 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

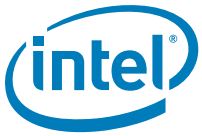
5.2 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shutdown before the THERMTRIP# is activated. If the processor's TM1 are triggered and the temperature remains high, an Out Of Spec status and sticky bit are latched in the status MSR register and generates a thermal interrupt.

5.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals for specific register and programming details.*

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.



Only a single PROCHOT# pin exists at a package level of the processor. When either core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted regardless of which core is above its TCC temperature trip point, and both cores will have their core clocks modulated. It is important to note that Intel recommends TM1 to be enabled in BIOS.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on both cores, then both processor cores will have their core clocks modulated. It should be noted that Force TM1, enabled via BIOS, does not have any effect on external PROCHOT#.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power-intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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