

Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] Processor Family

Datasheet – Volume 1 of 2

Supporting 4th Generation Intel[®] Core[™] processor based on Mobile U-Processor and Y-Processor Lines Supporting Mobile Intel[®] Pentium[®] and Mobile Intel[®] Celeron[®] Processor Families

July 2014

Order No.: 329001-007



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Intel[®] 64 architecture requires a system with a 64-bit enabled processor, chipset, BIOS and software. Performance will vary depending on the specific hardware and software you use. Consult your PC manufacturer for more information. For more information, visit http://www.intel.com/ content/www/us/en/architecture-and-technology/microarchitecture/intel-64-architecture-general.html.

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Intel® Virtualization Technology (Intel® VT) requires a computer system with an enabled Intel® processor, BIOS, and virtual machine monitor (VMM). Functionality, performance or other benefits will vary depending on hardware and software configurations. Software applications may not be compatible with all operating systems. Consult your PC manufacturer. For more information, visit http://www.intel.com/go/virtualization.

Requires a system with Intel® Turbo Boost Technology. Intel Turbo Boost Technology and Intel Turbo Boost Technology 2.0 are only available on select Intel® processors. Consult your PC manufacturer. Performance varies depending on hardware, software, and system configuration. For more information, visit http://www.intel.com/go/turbo.

Requires activation and a system with a corporate network connection, an Intel® AMT-enabled chipset, network hardware and software. For notebooks, Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] Processor Family Datasheet – Volume 1 of 2 2 Intel AMT may be unavailable or limited over a host OS-based VPN, when connecting wirelessly, on battery power, sleeping, hibernating or powered

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	002	 Updated Table 9, Multiple Display Configuration for U-Processor Line Added Table 10, Multiple Display Configuration for Y-Processor Line Updated Table 11, DisplayPort and Embedded DisplayPort* Resolutions per Link Data Rate for U-Processor Line Added Table 12, DisplayPort and Embedded DisplayPort* 	June 2013
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	.003 und	 Added Mobile 4th Generation Intel[®] Core[™] i7-4610Y, i5-4300Y, i5-4302Y, i7-4600U, i5-4300U, i5-4202Y, i5-4210Y, i3-4012Y, i3-4020Y, i3-4005U processors Added Mobile Intel[®] Pentium[®] 3560Y and 3556U processors Added Mobile Intel[®] Celeron[®] 2980U and 2995U processors Added Section 4.2.6, "Package C-States and Display Resolutions". 	September 2013
ned V.	004	Minor edits throughout for clarity	November 2013
indefit	005	 Added Mobile Intel[®] Pentium[®] 3558U and 3561Y processors Added Mobile Intel[®] Celeron[®] 2981U and 2957U processors 	December 2013
tined undefined und	006	 Added Mobile 4th Generation Intel[®] Core[™] i7-4510U, i5-4260U, i5-4210U, i3-4120U, i3-4030U, i3-4025U, i5-4220Y, i3-4030Y processors Updated Section 6.6, Testability Sections. Updated the "Direction/Buffer Type" column in Table 34. 	April 2014 July 2014
	007	 Added Mobile 4th Generation Intel[®] Core[™] i7-4578U, i5-4308U, i5-4278U processors 	July 2014
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Processors—Introduction

1.0 Introduction

The 4th Generation Intel[®] Core[™] processor based on Mobile U-Processor and Y-Processor Lines, Mobile Intel[®] Pentium[®] processor family, and Mobile Intel[®] Celeron[®] processor family are 64-bit, multi-core processors built on 22-nanometer process technology.

The processors are designed for a one-chip platform consisting of a Multi-Chip Package (MCP) processor that includes a low-power Platform Controller Hub (PCH) die on the same package as the processor die. See the following figure.

Throughout this document, the 4th Generation Intel[®] Core[™] processor based on Mobile U-Processor and Y-Processor Lines, Mobile Intel® Pentium® processor family, and Mobile Intel[®] Celeron[®] processor family may be referred to simply as "processor".

Throughout this document, the 4th Generation Intel[®] Core[™] processor based on Mobile U-Processor and Y-Processor Lines refers to the Mobile 4th Generation Intel® Core[™]i7-4650U, i7-4610Y, i7-4600U, i7-4578U, i7-4558U, i7-4550U, i7-4510U, i7-4500U, i5-4350U, i5-4308U, i5-4302Y, i5-4300Y, i5-4300U, i5-4288U, i5-4278U, i5-4260U, i5-4258U, i5-4250U, i5-4210Y, i5-4210U, i5-4202Y, i5-4200U, i5-4200Y, i3-4158U, i3-4120U, i3-4030Y, i3-4030U, i3-4025U, i5-4220Y, i3-4012Y, i3-4005U, i3-4100U, i3-4010U, and i3-4010Y processors.

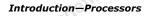
Throughout this document, the Mobile Mobile Intel® Pentium® processor family refers to the Intel[®] Pentium[®] 3561Y, 3560Y, 3558U, and 3556U processors.

Throughout this document, the Mobile Intel[®] Celeron[®] processor family refers to the Intel[®] Celeron[®] 2981U, 2980U, 2957U, and 2955U processors.

Note:

Some processor features are not available on all platforms. Refer to the processor e maennea undermea undermea undermea undermea undermea undermea undermea ame Aundefined undefined undefined undefined undefined Specification Update document for details.

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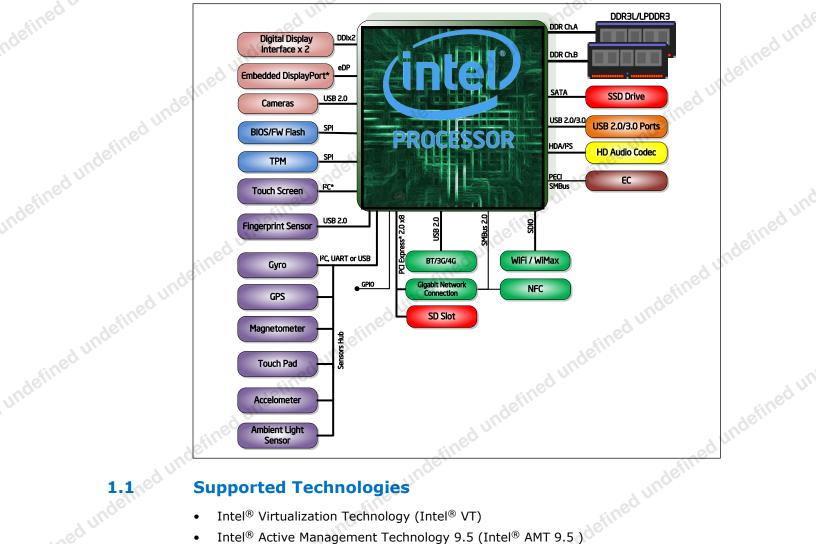
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Platform Block Diagram



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Supported Technologies

- Intel[®] Virtualization Technology (Intel[®] VT)
- Intel[®] Active Management Technology 9.5 (Intel[®] AMT 9.5)
- Intel[®] Trusted Execution Technology (Intel[®] TXT)
- Intel[®] Streaming SIMD Extensions 4.2 (Intel[®] SSE4.2)
- Intel[®] Hyper-Threading Technology (Intel[®] HT Technology)
- Intel[®] 64 Architecture
- Execute Disable Bit
- Intel[®] Turbo Boost Technology 2.0
- Intel[®] Advanced Vector Extensions 2.0 (Intel[®] AVX2)
- Intel[®] Advanced Encryption Standard New Instructions (Intel[®] AES-NI)
- PCLMULQDQ Instruction
- Intel[®] Secure Key

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- Intel® Transactional Synchronization Extensions New Instructions (Intel® TSX-NI)
- PAIR Power Aware Interrupt Routing
- SMEP Supervisor Mode Execution Protection
- Boot Guard

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Note:

1.2

The availability of the features may vary between processor SKUs.

Power Management Support

Processor Core

- Full support of ACPI C-states as implemented by the following processor C-states: undefined undefined — C0, C1, C1E, C3, C6, C7, C8, C9, C10
- Enhanced Intel SpeedStep® Technology

System

S0, S3, S4, S5

Memory Controller

- Conditional self-refresh
- Dynamic power-down

Processor Graphics Controller

- Intel[®] Rapid Memory Power Management (Intel[®] RMPM)
- Intel[®] Smart 2D Display Technology (Intel[®] S2DDT)
- Graphics Render C-state (RC6)
- Intel[®] Seamless Display Refresh Rate Switching with eDP port
- Intel[®] Display Power Saving Technology (Intel[®] DPST)

Thermal Management Support

- **Digital Thermal Sensor**
- Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- **On-Demand Mode**
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS

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Introduction—Processors



1.4

Package Support

The processor is available in the following package:

A 40 mm x 24 mm x 1.5 mm BGA package (BGA1168)

1.5 **Processor Testability**

Terminology

Table 1.

Terminology

Terminolog	y cined u.	
Terminology	Indein	
Term	Description	
APD	Active Power-down	
B/D/F	Bus/Device/Function	196 L
BGA	Ball Grid Array	N.C.
BLC	Backlight Compensation	
BLT	Block Level Transfer	
BPP	Bits per pixel	
СКЕ	Clock Enable	
CLTM	Closed Loop Thermal Management	
DDI	Digital Display Interface	
DDR3	Third-generation Double Data Rate SDRAM memory technology	
DDR3L	DDR3 Low Voltage	Inde
DDR3L-RS	DDR3 Low Voltage Reduced Standby Power	
DLL	Delay-Locked Loop	
DMA	Direct Memory Access	
DLL DMA DP DTS EC	DisplayPort*	
DTS	Digital Thermal Sensor	
EC	Embedded Controller	
ECC	Error Correction Code	1
eDP*	embedded DisplayPort*	nde
EPG	Electrical Power Gating	
ULEU	Execution Unit	1
FMA	Floating-point fused Multiply Add instructions	1
FSC	Fan Speed Control	1
HDCP	High-bandwidth Digital Content Protection	1
HDMI*	High Definition Multimedia Interface	1
HFM	High Frequency Mode	1

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(intel)	Processors—Introduction	
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Term	Description	
iDCT	Inverse Discrete	
IHS	Integrated Heat Spreader	24
GFX	Graphics	sinec
GUI	Graphical User Interface	
ІМС	Integrated Memory Controller	
Intel [®] 64 Technology Intel [®] DPST Intel [®] TSX-NI Intel [®] TXT	64-bit memory extensions to the IA-32 architecture	
Intel [®] DPST	Intel Display Power Saving Technology	
Intel [®] TSX-NI	Intel Transactional Synchronization Extensions - New Instructions	
Intel [®] TXT	Intel Trusted Execution Technology	
Intel [®] VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.	lefined
Intel® VT-d IOV ISI ITPM	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.	unoc
IOV	I/O Virtualization	
ISI	Inter-Symbol Interference	
ITPM	Integrated Trusted Platform Module	
LFM	Low Frequency Mode. LFM is Pn in the P-state table. It can be read at MSR CEh [47:40].	
LFP UNO	Local Flat Panel	stine
LPDDR3	Low-Power Third-generation Double Data Rate SDRAM memory technology	inde
МСР	Multi-Chip Package	
MCP MFM MLE MLC MSI MSL	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].	
MLE	Measured Launched Environment	
MLC	Mid-Level Cache	
MSI	Message Signaled Interrupt	
MSL	Moisture Sensitive Labeling	
MSR	Model Specific Registers	1efine
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.	d unoc
ODT	On-Die Termination	
OLTM	Open Loop Thermal Management	
PCG	Platform Compatibility Guide (PCG) (previously known as FMB) provides a design target for meeting all planned processor frequency requirements.	
OLTM PCG PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features.	All a
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Term	Description
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
PL1, PL2	Power Limit 1 and Power Limit 2
PPD	Pre-charge Power-down
Processor	The 64-bit multi-core component (package)
Processor Core Processor Graphic Rank SCI	The term "processor core" refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Processor Graphic	s Intel Processor Graphics
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDP J	Scenario Design Power
SF	Strips and Fans
SMM	System Management Mode
SMX	Safer Mode Extensions
SMX Storage Condition	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material), the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
SVID	Serial Voltage Identification
TAC	Thermal Averaging Constant
ТАР	Test Access Point
T _{CASE}	The case temperature of the processor, measured at the geometric center of the top- side of the TTV IHS.
тсс	Thermal Control Circuit
TAP T _{CASE} TCC T _{CONTROL}	$T_{CONTROL}$ is a static value that is below the TCC activation temperature and used as a trigger point for fan speed control. When DTS > $T_{CONTROL}$, the processor must comply to the TTV thermal profile.
TDP unde	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
TLB	Translation Look-aside Buffer
VITV	Thermal Test Vehicle. A mechanically equivalent package that contains a resistive heater in the die to evaluate thermal solutions.
ТТV ТМ V _{CC} V _{DDQ} VF VID	Thermal Monitor. A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
V _{CC}	Processor core power supply
V _{DDQ}	DDR3L and LPDDR3 power supply.
VF	Vertex Fetch
VID	Voltage Identification

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Table 2.

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Term	Descript	tion	
VS	Vertex Shader	Index	
VLD	Variable Length Decoding	and the second s	d uno
VMM	Virtual Machine Monitor	// .	sineu
VR	Voltage Regulator	~	
V _{SS}	Processor ground	eq y	
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tined undefined un	Mobile 4th Generation Intel [®] Core [®] Processor Family, Mobile Intel [®] Pentium [®] Processor Family, and Mobile Intel [®] Celeron [®] Processor Family Specification Update	328903	
inder	Mobile 4th Generation Intel [®] Core [®] Processor I/O Family Datasheet	329003	
	Mobile 4th Generation Intel [®] Core [®] Processor I/O Family Specification Update	329004	
file	Advanced Configuration and Power Interface 3.0	http://www.acpi.info/	
	PCI Local Bus Specification 3.0	http:// www.pcisig.com/ specifications	ndefined
	PCI Express Base Specification, Revision 2.0	http://www.pcisig.com	U
20	DDR3 SDRAM Specification	http://www.jedec.org	
	DisplayPort* Specification	http://www.vesa.org	
tined undefined u	Intel [®] 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/ products/processor/ manuals/index.htm	
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System Memory Interface

- Two channels of DDR3L/DDR3L-RS and LPDDR3 memory with Unbuffered Small Outline Dual In-Line Memory Modules (SO-DIMM) with a maximum of one DIMM per channel and memory down.
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR3L/DDR3L-RS I/O Voltage of 1.35V
- 64-bit wide channels
- Non-ECC, Unbuffered DDR3L/DDR3L-RS SO-DIMMs and memory down
- Theoretical maximum memory bandwidth of:
 - 21.3 GB/s in dual-channel mode assuming DDR3L/DDR3L-RS/LPDDR3 1333 MT/s
 - 25.6 GB/s in dual-channel mode assuming DDR3L/DDR3L-RS/LPDDR3 1600 MT/s

undefined undefined un System Memory Technology Supported 2.1.1

The Integrated Memory Controller (IMC) supports DDR3L/DDR3L-RS and LPDDR3 protocols with two independent, 64-bit wide channels. It supports one unbuffered non-ECC DDR3L/DDR3L-RS DIMM per channel; thus, allowing up to two device ranks per channel.

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Processor DIMM Support Summary by Product

			-	-		-
ndefined u	Processors	UTTDP	Graphics Configuration	DIMM Per Channel	DDR3L / DDR3L-RS (MT/s)	LPDDR3 (MT/s)
	inde	28W	GT3	1 DPC	1333/1600	N/A
			GT3	1 DPC	1333/1600	1333/1600
	U-Processor (Dual-Core)	15W	GT2	1 DPC	1333/1600	1333/1600
d Ur	Г.		GT1	1 DPC	1333/1600	1333/1600
ndefinet	Y-Processor (Dual-Core)	11.5W (6W SDP / 4.5W SDP)	GT1, GT2	1 DPC	1333/1600	1333/1600
undefined undefine	Notes: 1. LPDDR3 suppor 2. DDR3L-RS is su and vendor ava	pported as a me			on checkout depe	ends on parts
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Data Transfer Rates:

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- DDR3L-RS is supported as a memory configuration. Actual validation checkout depends on parts and vendor availability.
- 1333 MT/s (PC3-10600)
- 1600 MT/s (PC3-12800)

SO-DIMM Modules:

Standard 2Gb and 4Gb technologies and addressing are supported for x8 and x16 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

LPDDR3 Memory Down:

- Quad Ranked x16
- Single and Dual Ranked x32

Table 4. Supported DDR3L / DDR3L-RS SO-DIMM Module Configurations

		LPDDR5 M	emory Down:					
Jefil'		Quad F	Ranked x16			ed u.		2
		Single	and Dual Ranked	x32				
	Table 4.	Supporte	d DDR3L / DDR3	BL-RS SO-DI	MM Module C	onfiguration	5	Inder
	Raw Card Version	DIMM Capacity	DRAM Organization	# of DRAM Devices	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size	
	A	4 GB	256 M x 16	8	15/10	8	8K	
	della	4 GB	512 M x 8	8	16/10	8	8K	
du	С	2 GB	256 M x 16	4	15/10	8 6	8K	
lefined u	F	4 GB	256 M x 8	16	15/10	8	8K	
	F	8 GB	512 M x 8	16	16/10	8	8K	
	Table 5.	Supporte	d LPDDR3 Memo	ory Down Co	nfigurations			indefille
		KG Type	Die PKG	Dies Per	PKGs per		Banks Page	

Table 5. Supported LPDDR3 Memory Down Configurations

DIMM Capacity	PKG Type (Dies bits x PKG bits)	Die Density	PKG Density	Dies Per Channel	PKGs per Channel	Physical Device Rank	Banks Inside DRAM	Page Size
2 GB	SDP 32 x32	4 Gb	4 Gb	2	2	1	8 3	8К
4 GB	DDP 32 x32	4 Gb	8 Gb	4	2	2	8	8K
8 GB	QDP 16 x32	4 Gb	16 Gb	8	2	2	8	8K
Note: SDP	= Single Die Pack	kage, DDP =	Dual Die Pac	kage, QDP = Q	uad Die Package	0.0		

Table 6. Supported DDR3L / DDR3L-RS Memory Down Configurations

able 6.	Support	ed DDR3	L / DDR	BL-RS Me	emory De	own Conf	iguration	S		1 efil
System Capacity	DRAM Organization	Dies Per Package	PKG Density	Die Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size	d unoe
2 GB	128 M x 16	SDP	2 Gb	2 Gb	J 4	4	1	8	8К	
4 GB	256 M x 16	SDP	4 Gb	4 Gb	4	4	1	8 0	8К	
8 GB	256 M x 16	DDP	8 Gb 🔬	4 Gb	8	4	2	8	8K	

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2.1.2

System Memory Timing Support

The IMC supports the following DDR3L/DDR3L-RS Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
 - tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1N indicates a new command may be issued every clock and 2N indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

idefined undefined un **DRAM System Memory Timing Support**

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Tab	ble 7.	DRAM System Memory Timing Support										
	nde	Segment	DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC (SO- DIMM Only)	CMD Mode	ndefin	
	ned UN		DDR3L/ DDR3L-RS	1333	8/9	8/9	8/9	7	1 nd	1N/2N		
dell	¢.	U-Processor /	LPDDR3	1333	10	12	12	7	e ⁰ 1	0.5N		
defined undefi		Y-Processor (Dual Core)	DDR3L/ DDR3L-RS	1600	10/11	10/11	10/11	88	1	1N/2N		
dell			LPDDR3	1600	12	15	15	8	1	0.5N	24	
)//·	1.3	System M	lemory 0	rganizat	ion Mo	odes ¹⁰	elli				definect	

2.1.3

System Memory Organization Modes

The Integrated Memory Controller (IMC) supports two memory organization modes single-channel and dual-channel. Depending upon how the DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel[®] Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into symmetric and asymmetric zones. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

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Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

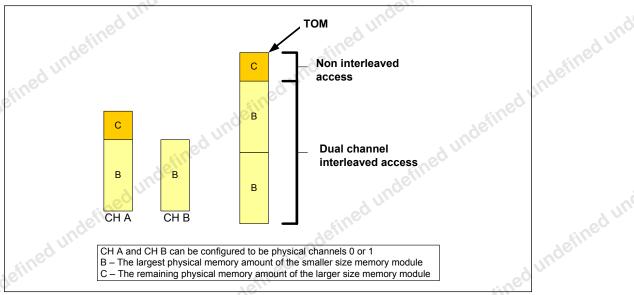
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Figure 2. Intel[®] Flex Memory Technology Operations



Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, the IMC operates completely in Dual-Channel Symmetric mode.

Note:

The DRAM device technology and width may vary from one channel to the other.

2.1.4 System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For dual-channel mode both channels must have a DIMM connector populated. For single-channel mode, only a single channel can have a DIMM connector populated.

2.1.5

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Intel[®] Fast Memory Access (Intel[®] FMA) Technology Enhancements

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

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Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, the requests can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back-to-back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt, which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result, the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.

2.1.7 DRAM Clock Generation

Every supported DIMM has two differential clock pairs. There are a total of four clock pairs driven directly by the processor to two DIMMs.

2.1.8 DRAM Reference Voltage Generation

The memory controller has the capability of generating the DDR3L/DDR3L-RS Reference Voltage (VREF) internally for both read (RDVREF) and write (VREFDQ) operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced DDR3L/DDR3L-RS training procedures to provide the best voltage and signal margins.

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2.3.

Processor Graphics

The processor graphics contains a generation 7.5 graphics core architecture. This enables substantial gains in performance and lower power consumption over previous generations. Up to 40 Execution Units are supported depending on the processor SKU.

- Next Generation Intel Clear Video Technology HD Support is a collection of video playback and enhancement features that improve the end user's viewing experience
 - Encode / transcode HD content
 - Playback of high definition content including Blu-ray Disc*
 - Superior image quality with sharper, more colorful images
 - Playback of Blu-ray* disc S3D content using HDMI (1.4a specification compliant with 3D)
- DirectX* Video Acceleration (DXVA) support for accelerating video processing
 - Full AVC/VC1/MPEG2 HW Decode
 - Advanced Scheduler 2.0, 1.0, XPDM support
 - Windows* 8, Windows* 7, OSX, Linux* operating system support
 - DirectX* 11.1, DirectX* 11, DirectX* 10.1, DirectX* 10, DirectX* 9 support.
- OpenGL* 4.0, support

Processor Graphics Controller (GT)

The Graphics Engine Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and "PCI-like" traffic in and out.

3D and Video Engines for Graphics Processing

The Gen 7.5 3D engine provides the following performance and power-management enhancements.

3D Pipeline

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine.

3D Engine Execution Units

- Supports up to 40 EUs. . The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

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Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

Windower / IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in hardware.

2D Engine

The 2D Engine contains BLT (Block Level Transfer) functionality and an extensive set of 2D instructions. To take advantage of the 3D during engine's functionality, some BLT functions make use of the 3D renderer.

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Logical 128-Bit Fixed BLT and 256 Fill Engine

This BLT engine accelerates the GUI of Microsoft Windows* operating systems. The 128-bit BLT engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment

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To perform logical operations (raster ops)

The rectangular block of data does not change, as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern is always 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine expands monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the BLT engine specifies which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (source, pattern, and destination) defined by Microsoft*, including transparent BLT.

The BLT engine has instructions to invoke BLT and stretch BLT operations, permitting ned undefined software to set up instruction buffers and use batch processing. The BLT engine can perform hardware clipping during BLTs.

2.4 Digital Display Interface (DDI)

The processor supports:

- Two Digital Display (x4 DDI) interfaces that can be configured as DisplayPort*, HDMI*. The DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate of RBR (1.62 GT/s), HBR (2.97 GT/s), and HBR2 (5.4 GT/s). When configured as HDMI*, the DDIx4 port can support 2.97 GT/s.
- One dedicated x4 embedded DisplayPort* (eDP*). Built-in displays are only supported on eDP.
- The HDMI* interface supports HDMI with 3D, 4K, Deep Color, and x.v.Color. The DisplayPort* interface supports the VESA DisplayPort* Standard Version 1, Revision 2.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high-definition content playback over digital interfaces.
- The processor also integrates dedicated a Mini HD audio controller to drive audio on integrated digital display interfaces, such as HDMI* and DisplayPort*. The HD audio controller on the PCH would continue to support down CODECs, and so on. ined undefined The processor Mini HD audio controller supports two High-Definition Audio streams simultaneously on any of the three digital ports.

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Figure 3.

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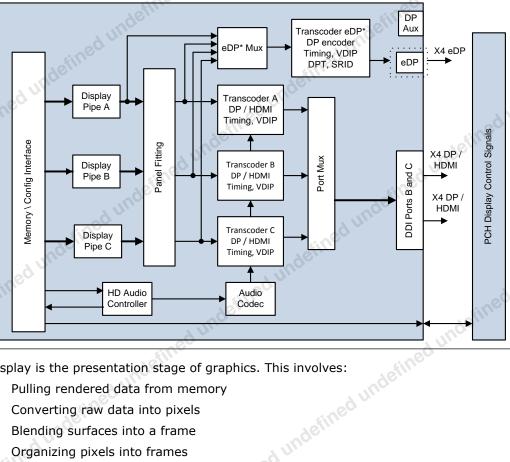


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- a undefined undefined The processor supports streaming any 3 independent and simultaneous display combination of DisplayPort*/HDMI*/eDP*/ monitors. In the case of 3 ined undefined und simultaneous displays, two High Definition Audio streams over the digital display interfaces are supported.
- Each digital port is capable of driving resolutions up to 3200x2000 at 60 Hz through DisplayPort* and 4096x2304 at 24 Hz using HDMI*.
- DisplayPort* Aux CH, DDC channel, Panel power sequencing, and HPD are supported through the PCH.

Processor Display Architecture for U- and Y- Processor Lines



undefined undefined und Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard

DisplayPort*

DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

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Processors—Interfaces

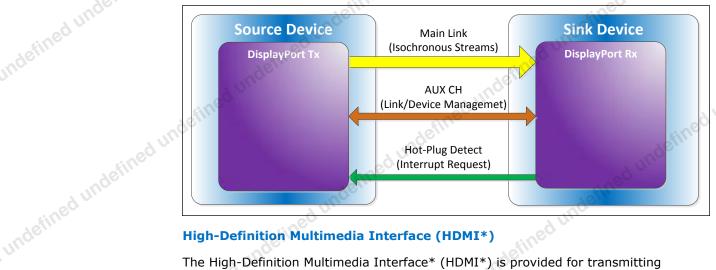
A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance with the VESA DisplayPort* Standard Version 1.2a. The processor supports VESA DisplayPort* PHY Compliance Test Specification 1.2a and VESA DisplayPort* Link Layer Compliance Test Specification 1.2a.



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DisplayPort* Overview



High-Definition Multimedia Interface (HDMI*)

The High-Definition Multimedia Interface* (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audiovisual sources to television sets, projectors, and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels — TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface with 3D, 4K, Deep Color, and x.v.Color.

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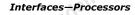
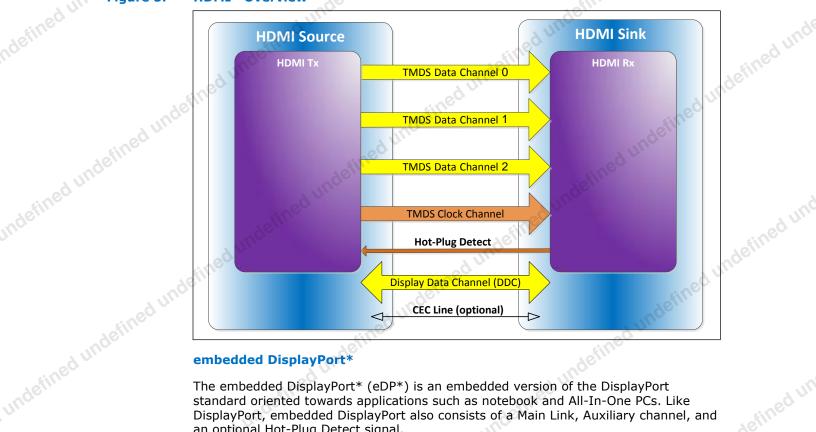




Figure 5. **HDMI*** Overview



embedded DisplayPort*

ed undefined The embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. Like DisplayPort, embedded DisplayPort also consists of a Main Link, Auxiliary channel, and an optional Hot-Plug Detect signal.

Integrated Audio

- HDMI and display port interfaces carry audio along with video.
- Processor supports two DMA controllers to output two High Definition audio streams on two digital ports simultaneously.
- Supports only the internal HDMI and DP CODECs.

undefined undefined

Processor Supported Audio Formats over HDMI*and DisplayPort*

	Audio Formats	HDMI*	DisplayPort*	
	AC-3 Dolby* Digital	Yes	Yes	nder
	Dolby Digital Plus	Yes	Yes	
2 U	DTS-HD*	Yes	Yes	
	LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes	
d under	Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes	
Jefined under	defined	tined uf	10.	
	and une	d under.		ndef

Processors—Interfaces

red undefined undefine The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI and DisplayPort monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

Multiple Display Configurations

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The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort*/HDMI. The following table shows examples of valid three display configurations through the processor.

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Multiple Display Configuration for U-Processor Line

Display 1	Display 2	Display 3	Maximum Resolution Display 1	Maximum Resolution Display 2	Maximum Resolution Display 3
HDMI	НДМІ	eDP	4096x2304	3200x2000 @ 60 Hz	
DP	DP	eDP	3200x2000	@ 60 Hz	3200x2000 @ 60 Hz
HDMI	DP	eDP	4096x2304 @ 24Hz	3200x2000 @ 60 Hz	
Note: DP an	d eDP resolution	ns in this table	are supported for 4 lane	es with link data rate H	IBR2 at 24 bits per

pixel (bpp) and single stream mode of operation.

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Multiple Display Configuration for Y-Processor Line

	Display 1	Display 2	Display 3	Maximum Resolution Display 1	Maximum Resolution Display 2	Maximum Resolution Display 3
	HDMI	HDMI	eDP	4096x2304	l @ 24 Hz	2880x1620 @ 60 Hz
აი	DP	DP	eDP	2880×1620) @ 60 Hz	2880x1620 @ 60 Hz
	HDMI	DP	eDP	4096x2304 @ 24 Hz	2880x1620 @ 60 Hz	2880x1620 @ 60 Hz
1				ble are supported for 4 n mode of operation.	lanes with link data r	ate HBR2 at 24 bits

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Interfaces—Processors



Table 11.

L. DisplayPort and embedded DisplayPort* Resolutions per Link Data Rate for U-Processor Line

0-FIOCESSOI LINE							
Link Data Rate		Lane Count					
dein	1	2	4	ined t			
RBR	1064×600	1400×1050	2240x1400	defin			
HBR	1280x960	1920x1200	2880×1800				
HBR2	1920x1200	2880x1800	3200×2000				
			Xo				

Note: The above resolutions are valid at 60 Hz refresh rate and 24 bits per pixel (bpp).

Table 12.

. DisplayPort and embedded DisplayPort* Resolutions per Link Data Rate for Y-Processor Line

Link Data Rate		Lane Count	
defin	1	(12) (C	4
RBR	1064x600	1400x1050	2240x1400
HBR	1280x960	1920x1200	2880x1620 @ 60 Hz
	X /		

Note: The above resolutions are valid at 60 Hz refresh rate and 24 bits per pixel (bpp).

High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 1.4 for content protection over wired displays (HDMI* and DisplayPort*).

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

2.5

Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components, like Super I/O (SIO) and Embedded Controllers (EC), to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

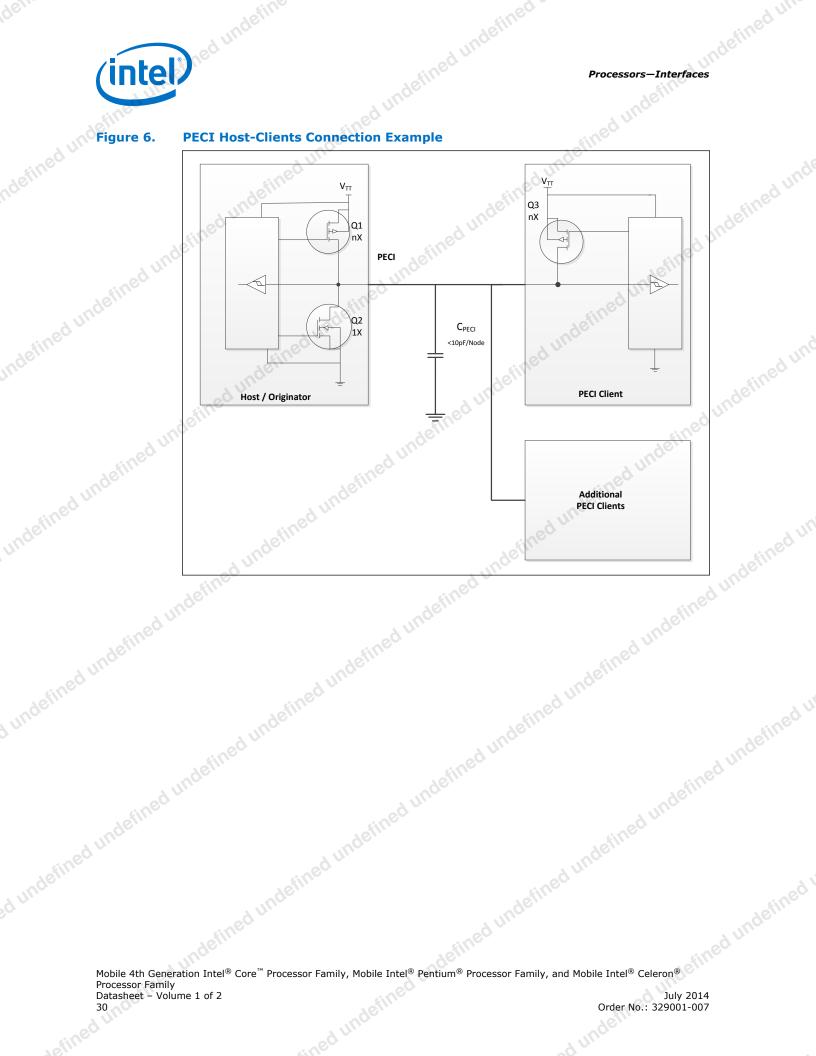
2.5.1 PECI Bus Architecture

The PECI architecture is based on a wired-OR bus that the clients (as processor PECI) can pull up high (with strong drive).

The idle state on the bus is near zero.

The following figure demonstrates PECI design and connectivity. While the host/ originator can be a third party PECI host, one of the PECI clients is a processor PECI device.

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3.0 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

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Intel[®] Virtualization Technology (Intel[®] VT)

Intel[®] Virtualization Technology (Intel[®] VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel[®] Virtualization Technology (Intel[®] VT) for IA-32, Intel[®] 64 and Intel[®] Architecture (Intel[®] VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel[®] Virtualization Technology for Directed I/O (Intel VT-d) extends Intel[®] VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel[®] VT-x specifications and functional descriptions are included in the *Intel*[®] 64 and *IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other Intel VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

https://sharedspaces.intel.com/sites/PCDC/SitePages/Ingredients/ingredient.aspx? ing=VT

Intel[®] VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- Robust: VMMs no longer need to use paravirtualization or binary translation. This
 means that off-the-shelf operating systems and applications can be run without
 any special steps.
- Enhanced: Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.

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- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- ined undefined **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

Intel[®] VT-x Features

The processor supports the following Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
 - EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as defragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.

Extended Page Table Pointer (EPTP) switching

- EPTP switching is a specific VM function. EPTP switching allows guest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX nonroot operation can request a change of EPTP without a VM exit. Software can choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
 - Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
 - EPT is hardware assisted page table virtualization.
 - It eliminates VM exits from the guest operating system to the VMM for shadow page-table maintenance.
- Virtual Processor IDs (VPID)
 - Ability to assign a VM ID to tag processor core hardware structures (such as TLBs).
 - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
 - Guest Preemption Timer
 - Mechanism for a VMM to preempt the execution of a guest operating system after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
 - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees.

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- **Descriptor-Table Exiting**
 - Descriptor-table exiting allows a VMM to protect a quest operating system from an internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).

A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

Intel[®] VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for a virtualized platform and provides software with the following capabilities:

- I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.
- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel VT-d accomplishes address translation by associating a transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between the device's PCI Express* Bus/Device/Function (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Ner Table) that contains Guest specific address translations.

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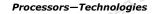
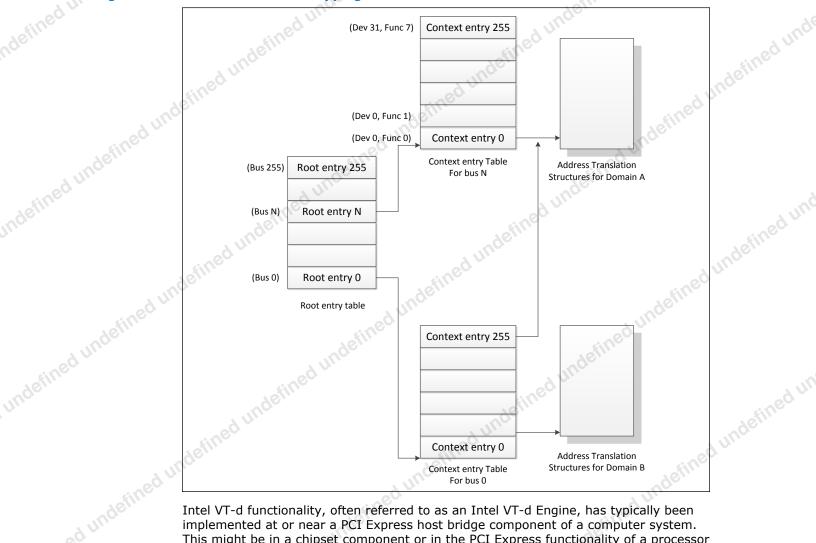




Figure 7.

Device to Domain Mapping Structures



Intel VT-d functionality, often referred to as an Intel VT-d Engine, has typically been implemented at or near a PCI Express host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such Intel VT-d engine receives a PCI Express transaction from a PCI Express bus, it uses the B/D/F number associated with the transaction to search for an Intel VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel VT-d fault. If Intel VT-d translation is required, the Intel VT-d engine performs an N-level table walk.

For more information, refer to *Intel*[®] *Virtualization Technology for Directed I/O Architecture Specification* http://download.intel.com/technology/computing/vptech/ Intel(r)_VT_for_Direct_IO.pdf

Intel[®] VT-d Features

The processor supports the following Intel VT-d features:

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- Memory controller and processor graphics comply with the Intel VT-d 1.2 Specification
- Two Intel VT-d DMA remap engines
 - iGFX DMA remap engine
 - Default DMA remap engine (covers all devices except iGFX)
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4 KB page sizes
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware-based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for Global, Domain specific, and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxh) not translated
 - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents; PEG/DMI interfaces return unsupported request status
- Interrupt remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

- 4-level Intel VT-d Page walk: Both default Intel VT-d engine, as well as the IGD Intel VT-d engine, are upgraded to support 4-level Intel VT-d tables (adjusted guest address width 48 bits)
- Intel VT-d superpage: support of Intel VT-d superpage (2 MB, 1 GB) for the default Intel VT-d engine (that covers all devices except IGD)

IGD Intel VT-d engine does not support superpage and BIOS should disable superpage in default Intel VT-d engine when iGFX is enabled.

Note:

3.2

Intel VT-d Technology may not be available on all SKUs.

Intel[®] Trusted Execution Technology (Intel[®] TXT)

Intel Trusted Execution Technology (Intel TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

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Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs both VLWs and IPI

For the above features, BIOS must test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the Intel[®] Trusted Execution Technology Measured Launched Environment Programming Guide.

3.3

Intel[®] Hyper-Threading Technology (Intel[®] HT Technology)

The processor supports Intel Hyper-Threading Technology (Intel HT Technology) that allows an execution core to function as two logical processors. While some execution resources, such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

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ad undefined undefi Intel recommends enabling Intel HT Technology with Microsoft Windows* 8 and Microsoft Windows* 7 and disabling Intel HT Technology using the BIOS for all undefined un previous versions of Windows* operating systems. For more information on Intel HT Technology, see http://www.intel.com/technology/platform-technology/hyperthreading/

3.4

Intel[®] Turbo Boost Technology 2.0

The Intel Turbo Boost Technology 2.0 allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock, if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology 2.0 feature is designed to increase performance of both multi-threaded and single-threaded workloads.

Compared with previous generation products, Intel Turbo Boost Technology 2.0 will ned undefined increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note:

Intel Turbo Boost Technology 2.0 may not be available on all SKUs.

Intel[®] Turbo Boost Technology 2.0 Frequency

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:

- The number of cores operating in the C0 state.
- The estimated core current consumption.
- The estimated package prior and present power consumption.
- The package temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay within its TDP limit. Turbo processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states, see Power Management on page 42.

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Intel[®] Advanced Vector Extensions 2.0 (Intel[®] AVX2)

Intel Advanced Vector Extensions 2.0 (Intel AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software.

For more information on Intel AVX, see http://www.intel.com/software/avx

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red undefined undefi Intel[®] Advanced Encryption Standard New Instructions (Intel[®] AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/ decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULODO. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

Intel[®] Secure Key

The processor supports Intel[®] Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure storage, and so on.

Intel[®] 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
 - Delivery modes
 - Interrupt and processor priorities
 - Interrupt sources
 - Interrupt destination types

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- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
 - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
 - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt deliverv.

Increased range of processor addressability in x2APIC mode:

- Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32bits in a software transparent fashion.
- Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields – a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, $((2^20) - 16)$ processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers:
 - To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.
- The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the "x2APIC" mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
- The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations.

Intel x2APIC Technology may not be available on all SKUs.

For more information, see the Intel® 64 Architecture x2APIC Specification at http:// www.intel.com/products/processor/manuals/.

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Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active cores without waking the deep idle cores. For performance, it routes the interrupt to the idle (C1) cores without interrupting the already heavily loaded cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on.

Execute Disable Bit

The Execute Disable Bit allows memory to be marked as executable when combined with a supporting operating system. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the Intel® 64 and IA-32 Architectures Software Developer's Manuals for more detailed information.

Intel[®] Boot Guard 3.10

Intel[®] Boot Guard can help protect the platform boot integrity by preventing execution of unauthorized boot blocks. With Intel® Boot Guard, platform manufacturers can create boot policies such that invocation of an unauthorized (or untrusted) boot block will trigger the platform protection per the manufacturer's defined policy.

With verification based in the hardware, Intel® Boot Guard extends the trust boundary of the platform boot process down to the hardware level.

Intel[®] Boot Guard accomplishes this by:

- Providing hardware-based Static Root of Trust for Measurement (S-RTM) and the Root of Trust for Verification (RTV) using Intel architectural components.
- Providing architectural definition for platform manufacturer Boot Policy.
- Enforcing manufacture provided Boot Policy using Intel architectural components.

Benefits of this protection is that Intel[®] Boot Guard can help maintain platform integrity by preventing re-purposing of the manufacturer's hardware to run an unauthorized software stack.

Note:

Intel[®] Boot Guard technology availability may vary between the different SKUs.

Supervisor Mode Execution Protection (SMEP) 3.11

Supervisor Mode Execution Protection provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, refer to $Intel^{(R)} 64$ and IA-32 Architectures Software Developer's Manual, Volume 3A at: http:// www.intel.com/Assets/PDF/manual/253668.pdf

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Intel[®] Transactional Synchronization Extensions - New Instructions (Intel[®] TSX-NI)

New on the processor are the Intel Transactional Synchronization Extensions - New Instructions (Intel TSX-NI). Intel TSX-NI provides a set of instruction extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the performance of fine-grain , inte , locking while actually programming using coarse-grain locks. Details on Intel TSX-NI are in the Intel[®] Architecture Instruction Set Extensions Programming Reference.

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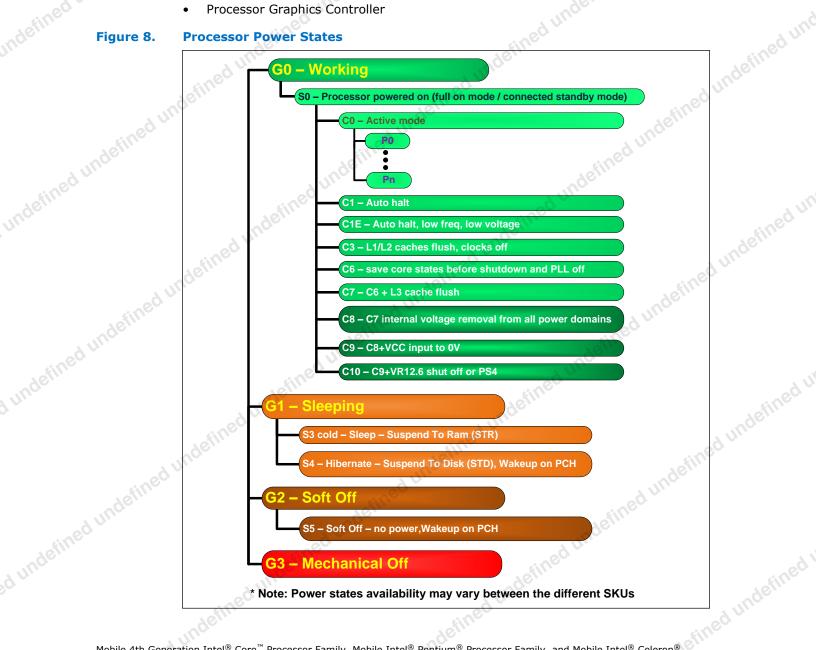
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Power Management 4.0

undefined This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor Core
- Integrated Memory Controller (IMC)
- Processor Graphics Controller

Figure 8. **Processor Power States**



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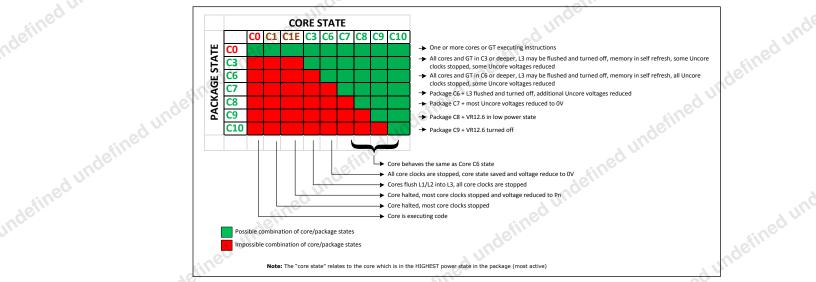
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Figure 9.

4.1

Processor Package and Core C-States



Advanced Configuration and Power Interface (ACPI) **States Supported**

This section describes the ACPI states supported by the processor.

Table 13. System States

State	Description	sineu
G0/S0	Full On Mode, Display On.	dell
G0/S0	Connected Standby Mode, Display Off.	
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot state is not supported by the processor).	
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).	
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.	
G3	Mechanical off. All power removed from system.	

undefined undefined un **Processor Core / Package State Support**

sinec	G3	Mechanical off. All power removed from system.	
unden Table 14.	Processor C	ore / Package State Support	ined u
0	State	Description	defin
	C0	Active mode, processor executing code.	Un
, un	C1	AutoHALT state.	
aned	C1E	AutoHALT state with lowest frequency and voltage operating point.	
unden.	C3	Execution cores in C3 state flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.	
ined -	C6	Execution cores in this state save their architectural state before removing core voltage.	
defin		continued	
ed une	defined un	ider fined undefine	d undefined
Mahiladah	Concention Intel®	Cara [™] Dracescar Femily, Mabile Intel [®] Pantium [®] Dracescar Femily, and Mabile Intel [®] Caleran [®]	

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der	od undef	IUC
(int	el ned undef	
unde	State	
ndefined undefined	C7	Exc rec flu: wil

StateDescriptionC7Execution cores in this state behave similarly to the C6 state. If all execution cores request C7 state, L3 cache ways are flushed until it is cleared. If the entire L3 cache is flushed, voltage will be removed from the L3 cache. Power removal to SA, Cores and L3 will reduce power consumption.C8C7 state plus voltage is removed from all power domains after required state is saved. PLL is powered down.C9C8 state plus processor V _{CC} input voltage at 0 V.C10C9 state plus VR12.6 is set to low-power state, near shut off.	ed undefil	ie undefined	defined une
C7Execution cores in this state behave similarly to the C6 state. If all execution cores request C7 state, L3 cache ways are flushed until it is cleared. If the entire L3 cache is flushed, voltage will be removed from the L3 cache. Power removal to SA, Cores and L3 will reduce power consumption.C8C7 state plus voltage is removed from all power domains after required state is saved. PLL is powered down.C9C8 state plus processor V _{CC} input voltage at 0 V.	Nec	Processors—Power Management	ne
C7 request C7 state, L3 cache ways are flushed until it is cleared. If the entire L3 cache is flushed, voltage will be removed from the L3 cache. Power removal to SA, Cores and L3 will reduce power consumption. C8 C7 state plus voltage is removed from all power domains after required state is saved. PLL is powered down. C9 C8 state plus processor V _{CC} input voltage at 0 V.	State	Description	
C8 is powered down. C9 C8 state plus processor V _{CC} input voltage at 0 V.	C7	request C7 state, L3 cache ways are flushed until it is cleared. If the entire L3 cache is flushed, voltage will be removed from the L3 cache. Power removal to SA, Cores and L3	uned une
	C8		indefill
C10 C9 state plus VR12.6 is set to low-power state, near shut off.	C9	C8 state plus processor V _{CC} input voltage at 0 V.	
	C10	C9 state plus VR12.6 is set to low-power state, near shut off.	1

Table 15.

Integrated Memory Controller States

State	Description	
Power up	CKE asserted. Active mode.	ind
Pre-charge Power-down	CKE de-asserted (not self-refresh) with all banks closed.	sined L
Active Power- down	CKE de-asserted (not self-refresh) with minimum one bank active.	under
Self-Refresh	CKE de-asserted using device self-refresh.	

Table 16. G, S, and C Interface State Combinations

Idefined underty To.	Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
defin	G0	S0	C0	Full On	On	Full On
	G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
	G0	S0	C3	Deep Sleep	On	Deep Sleep
	G0	S0	C6/C7	Deep Power- down	On	Deep Power-dow
ndefined undefined ut	G0	S0	C8/C9/C10		On	Deeper Power- down
	G1	S3	Power off		Off, except RTC	Suspend to RAM
ed u.	G1	S4	Power off		Off, except RTC	Suspend to Disk
define	G2	S5	Power off		Off, except RTC	Soft Off
no	G3	NA	Power off		Power off	Hard off

4.2

4.2.1

Processor Core Power Management

While executing code, Enhanced Intel SpeedStep® Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

Enhanced Intel[®] SpeedStep[®] Technology Key Features

The following are the key features of Enhanced Intel SpeedStep Technology:

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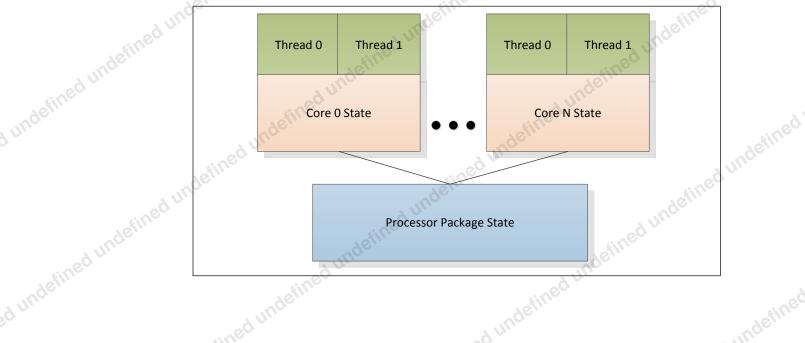
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor cores.
 - Once the voltage is established, the PLL locks on to the target frequency.
 - All active processor cores share the same frequency and voltage. In a multicore processor, the highest frequency P-state requested among all active cores is selected.
 - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- undefined Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

Low-Power Idle States 4.2.2

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

undefined undefin Caution: Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 10. Idle Power Management Breakdown of the Processor Cores



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While individual threads can request low-power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

4.2.3 **Requesting Low-Power Idle States**

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. The reads fall through like a normal I/O instruction.

When P LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wakeup on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 **Core C-State Rules**

The following are general rules for all core C-states, unless specified otherwise:

- A core C-state is determined by the lowest numerical thread state (such as Thread 0 requests C1E state while Thread 1 requests C3 state, resulting in a core C1E state). See the G, S, and C Interface State Combinations table.
- A core transitions to C0 state when:
 - An interrupt occurs
 - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
 - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes only that thread.
 - If any thread in a core is in active (in C0 state), the core's C-state will resolve to C0 state.
- Any interrupt coming into the processor package may wake any core
- A system reset re-initializes all processor cores.

Core CO State

The normal operating state of a core where code is being executed.

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Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the Intel® 64 and IA-32 Architectures Software Developer's Manual for more information.

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E state, see Package C-States on page 48.

Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

Core C6 State

Individual threads of a core can enter the C6 state by initiating a P LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6 state, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

Core C7-C10 States

Individual threads of a core can enter the C7, C8, C9, or C10 state by initiating a P LVL4, P LVL5, P LVL6, P LVL7 I/O read (respectively) to the P BLK or by an MWAIT(C7/C8/C9/C10) instruction. The core C7–C10 state exhibits the same behavior as the core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7 state, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. fined undefine Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-state auto-demotion options:

- C7/C6 to C3 state
- C7/C6/C3 To C1 state

The decision to demote a core from C6/C7 to C3 or C3/C6/C7 to C1 state is based on each core's immediate residency history and interrupt rate . If the interrupt rate experienced on a core is high and the residence in a deep C-state between such interrupts is low, the core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a core to C1 state as compared to C3 state.

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ed undefined undefin This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 **Package C-States**

The processor supports C0, C1/C1E, C3, C6, C7, C8, C9, and C10 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states, unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
 - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
 - The platform may allow additional power savings to be realized in the processor.
 - For package C-states, the processor is not required to enter C0 state before entering any other C-state.
 - Entry into a package C-state may be subject to auto-demotion that is, the processor may keep the package in a deeper package C-state than requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
 - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0 state.
 - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request,
 - But the platform did not request to keep the processor in a higher package Cstate, the package returns to its previous C-state.
 - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power Cstate.

The following table shows package C-state resolution for a dual-core processor. The . The undefined undefined undefined following figure summarizes package C-state transitions.

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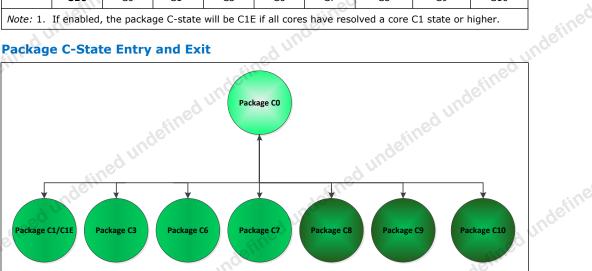


										-
Package	C-State	y un.			C	ore 1	nde			
	fine	СО	C1	C3	C6	C7	C8	С9	C10	sined und
7.	СО	C0	C0	C0	C0	C0	C0	C0	C0	sineu
red un	C1	C0	C1 ¹	C11	C1 ¹	1961				
	С3	C0	C1 ¹	C3	C3	C3	C3	C3	C3]
Coro 0	C6	C0	C1 ¹	С3	C6	C6	C6	C6	C6	
Core 0	C7	C0	C1 ¹	C3	C6	C7	C7	C7	C7	
	C8	C0	C1 ¹	C3	C6	C7	C8	C8	C8	
	C9	C0	C11	C3	C6	C7	C8	C9	C9	1
	C10	C0	C11	C3	C6	C7	C8	C9	C10	710 - 11
Note: 1 I	if enabled	the nacka	no C-stato	will be C1F	if all core	s have reso	lved a core	C1 state or l	higher	ed v

Table 17. Coordination of Core Power States at the Package Level

Note: 1. If enabled, the package C-state will be C1E if all cores have resolved a core C1 state or higher.

Figure 11.



Package C0 State

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low-power state. Individual cores may be in lower power idle states while the package is in C0 state.

Package C1/C1E State

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low-power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or deeper power state.

The package enters the C1E state when:

All cores have directly requested C1E using MWAIT(C1) with a C1E sub-state hint.

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- All cores are in a power state deeper than C1/C1E state; however, the package low-power state is limited to C1/C1E using the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 state using HLT or MWAIT(C1) and C1E autopromotion is enabled in IA32 MISC ENABLES.

No notification to the system occurs upon entry to C1/C1E state.

Package C2 State

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Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when:

- All cores and graphics have requested a C3 or deeper power state; however, constraints (LTR, programmed timer events in the near future, and so on) prevent entry to any state deeper than C 2 state. Or,
- All cores and graphics are in the C3 or deeper power states, and a memory access ined undefined request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low-power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 state or deeper power state and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 or deeper state, however, has allowed a package C6 state.

In package C3 state, the L3 shared cache is valid.

Package C6 State

A processor enters the package C6 low-power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or deeper power state and the processor has been granted permission by the platform.
- The platform has not granted a package C7 state or deeper request; however, has allowed a package C6 state.
- If the cores are requesting C7 state, but the platform is limiting to a package C6 state, the last level cache in this case can be flushed.

In package C6 state all cores have saved their architectural state and have had their core voltages reduced to zero volts. It is possible the L3 shared cache is flushed and turned off in package C6 state. If at least one core is requesting C6 state, the L3 cache will not be flushed.

Package C7 State

The processor enters the package C7 low-power state when all cores are in the C7 state. In package C7, the processor will take action to remove power from portions of the system agent.

Core break events are handled the same way as in package C3 or C6 state.

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Package C8 State

The processor enters C8 states when the core with the highest state is C8.

The package C8 state is similar to package C7 state; however, in addition, all internally generated voltage rails are turned off and the input V_{CC} is reduced to 1.15 V to 1.3 V.

Package C9 State

The processor enters package C9 states when the core with the highest state is C9.

The package C9 state is similar to package C8 state; in addition, the input V_{CC} is changed to 0 V.

Package C10 State

The processor enters C10 states when the core with the highest state is C10.

The package C10 state is similar to the package C9 state; in addition, the VR12.6 is in PS4 low-power state, which is near to shut off of the VR12.6.

Dynamic L3 Cache Sizing

When all cores request C7 or deeper C-state, internal heuristics is dynamically flushes the L3 cache. Once the cores enter a deep C-state, depending on their MWAIT substate request, the L3 cache is either gradually flushed N-ways at a time or flushed all at once. Upon the cores exiting to C0, the L3 cache is gradually expanded based on internal heuristics.

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Package C-States and Display Resolutions

The integrated graphics engine has the frame buffer located in system memory. When the display is updated, the graphics engine fetches display data from system memory. Different screen resolutions and refresh rates have different memory latency requirements. These requirements may limit the deepest Package C-state the processor can enter. Other elements that may affect the deepest Package C-state available are the following:

- Display is on or off
- Single or multiple displays
- Native or non-native resolution
- Panel Self Refresh (PSR) technology

Note:

Display resolution is not the only factor influencing the deepest Package C-state the processor can get into. Device latencies, interrupt response latencies, and core C-states are among other factors that influence the final package C-state the processor can enter.

The following table lists display resolutions and deepest available package C-State. The display resolutions are examples using common values for blanking and pixel rate. Actual results will vary. The table shows the deepest possible Package C-state. System workload, system idle, and AC or DC power also affect the deepest possible Package C-state.

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Jed undefined undefined Deepest Package C-State Available – U-Processor Line and Y-Processor Line

Panel Self Refresh (PSR)	Number of Displays ¹	Native Resolution ²	Deepest Available Package C-State	
Disabled	Single	800x600 60 Hz	PC7	
Disabled	Single	1024x768 60 Hz	PC7	
Disabled	Single	1280x1024 60 Hz	PC7	Ŋ
Disabled Disabled Disabled Disabled Disabled Disabled Disabled	Single	1920x1080 60 Hz	PC7	
Disabled	Single	1920x1200 60 Hz	PC7	
Disabled	Single	1920x1440 60 Hz	PC6	
Disabled	Single	2048x1536 60 Hz	PC6	
Disabled	Single	2560x1600 60 Hz	PC6	
Disabled	Single	2560x1920 60 Hz	PC2	
Disabled	Single	2880x1620 60 Hz	PC2	
Disabled	Single	2880x1800 60 Hz ³	PC2	
Disabled	Single	3200x1800 60 Hz ³	PC2	
Disabled	Single	3200x2000 60 Hz ³	PC2	
Disabled Disabled Disabled Disabled Disabled Disabled Disabled	Single	3840x2160 30 Hz	PC2	
Disabled	Single	4096x2160 24 Hz	PC2	
Disabled	Multiple	800x600 60 Hz	PC7	
Disabled	Multiple	1024x768 60 Hz	PC6	
Disabled	Multiple	1280x1024 60 Hz	PC6	
Disabled	Multiple	1920x1080 60 Hz	PC2	
Disabled	Multiple	1920x1200 60 Hz	PC2	2
Disabled	Multiple	1920x1440 60 Hz	PC2	
Disabled	Multiple	2048x1536 60 Hz	PC2	
Disabled	Multiple	2560x1600 60 Hz	PC2	
Disabled	Multiple	2560x1920 60 Hz	PC2	
Disabled Disabled Disabled Disabled Disabled Disabled Disabled	Multiple	2880x1620 60 Hz	PC2	
Disabled	Multiple	2880x1800 60 Hz ³	PC2	
Disabled	Multiple	3200×1800 60 Hz ³	PC2	
Disabled	Multiple	3200x2000 60 Hz ³	PC2	١ç
Disabled	Multiple	3840x2160 30 Hz	PC2	5
Disabled Disabled	Multiple	4096x2160 24 Hz	PC2	
	ed underinee	etined undefined u	continued	

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Panel Self Refresh (PSR)	Number of Displays ¹	Native Resolution ²	Deepest Available Package C-State
Enabled	Single	Any native resolution ⁴	PC7
Enabled	Multiple	Any native resolution ¹	Same as PSR disabled for the given resolution with multiple displays

- Notes: 1. For multiple display cases, the resolution listed is the highest native resolution of all enabled displays, and PSR is internally disabled; that is, dual display with one 800x600 60 Hz display and one 2560x1600 60 Hz display will result in a deepest available package C-state of PC2.
 - 2. For non-native resolutions, PSR is internally disabled, and the deepest available package C-State will be between that of the PSR disabled native resolution and the PSR disabled non-native resolution.; that is, a native 3200x1800 60 Hz panel using non-native 1920x1080 60 Hz resolution will result in a deepest available package C-State between PC2 and PC7.
 - 3. Resolution not supported by Y-Processor line.
 - 4. Microcode Update rev 00000010 or newer must be used.

Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACP Cx states.

4.3

Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory in which it is not connected to any actual memory devices is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially unterminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be determined that the rows are not populated. This is due to the fact that when CKE is tri-stated with DRAMs present, the DRAMs are not ensured to maintain data integrity. CKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

CKE tristate should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

DRAM Power Management and Initialization

The processor implements extensive support for power management on the memory interface. The processor drives four CKE pins, one per rank.

The CKE is one of the power-save means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification.

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The processor supports four different types of power-down modes in package C0. The different power-down modes can be enabled through configuring "PM_PDWN_config_0_0_0_MCHBAR". The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN_idle_counter (bits 11:0). The different power-down modes supported are:

No power-down (CKE disable)

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- Active power-down (APD): This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is defined by tXP small number of cycles. For this mode, DRAM DLL must be on.
- PPD/DLL-off: In this mode the data-in DLLs on DDR are off. Power-saving in this
 mode is the best among all power modes. Power consumption is defined by
 IDD2P1. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to
 DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL
 must be off.
 - **Pre-charged power-down (PPD):** This mode is entered if all banks in DDR are pre-charged when de-asserting CKE. Power saving in this mode is intermediate better than APD, but less than DLL-off. Power consumption is defined by IDD2P1. Exiting this mode is defined by tXP. The difference from APD mode is that when waking-up all page-buffers are empty.) The LPDDR does not have a DLL. As a result, the power savings are as good as PPD/DLL-off, but will have lower exit latency and higher performance.

The CKE is determined per rank, whenever it is inactive. Each rank has an idlecounter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to the DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-offs of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue – use no power-down
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible PPD/DLL-off with a low idle timer value
- In high-performance systems with dense packaging (that is, tricky thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

The default value that BIOS configures in "PM_PDWN_config_0_0_0_MCHBAR" is 6080h – that is, PPD/DLL-off mode with idle timer of 80h, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCKLs that a rank is idle that causes entry to the selected powermode. As this timer is set to a shorter time, the IMC will have more opportunities to put DDR in power-down. There is no BIOS hook to set this

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register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 **Initialization Role of CKE**

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the DDR3L/DDR3L-RS reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

fined undefine **Conditional Self-Refresh** 4.3.2.2

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Intel® Rapid Memory Power Management (Intel® RMPM) for more details on conditional selfrefresh with Intel HD Graphics enabled.

When entering the S3 - Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor core flushes pending cycles and then enters SDRAM ranks that are not used by Intel graphics memory into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service. The target usage is shown in the following table.

undefined undefined Table 19. **Targeted Memory State Conditions**

Fargeted	Memory State Conditions	Inde	
Mode	Memory State with Processor Graphics	Memory State with External Graphics	Juc
C0, C1, C1E	Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.	
C3, C6, C7 or deeper	If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise, use dynamic memory rank power-down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise, use dynamic memory rank power-down based on idle conditions.	
S3	Self-Refresh Mode	Self-Refresh Mode	
S4	Memory power-down (contents lost)	Memory power-down (contents lost)	

Dynamic Power-Down 4.3.2.3

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor core controller can be configured to put the devices in active powerdown (CKE de-assertion with open pages) or pre-charge power-down (CKE deassertion with all pages closed). Pre-charge power-down provides greater power savings, but has a bigger performance impact since all pages will first be closed before putting the devices in power-down mode.

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If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODE, and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.3.3 DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates V_{DDQ} for the majority of the logic to reduce idle power while keeping all critical DDR pins such as CKE and VREF in the appropriate state.

In C7 or deeper power state, the processor internally gates Vcc_{ST} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

4.4 Graphics Power Management

4.4.1

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Intel[®] Rapid Memory Power Management (Intel[®] RMPM)

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow the system to remain in the lower power states longer for memory not reserved for graphics memory. Intel RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

4.4.2 Graphics Render C-State

Render C-state (RC6) is a technique designed to optimize the average power to the graphics render engine during times of idleness. RC6 is entered when the graphics render engine, blitter engine, and the video engine have no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the processor graphics will program the graphics render engine internal power rail into a low voltage state.

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Intel[®] Smart 2D Display Technology (Intel[®] S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

Intel[®] Graphics Dynamic Frequency

Intel Graphics Dynamic Frequency Technology is the ability of the processor and graphics cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel Graphics Dynamic Frequency Technology is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always try to place the graphics engine in the most energy efficient P-state.

undefined undefined Intel[®] Display Power Saving Technology (Intel[®] DPST)

The Intel DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

- 1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
- 2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
- 3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in. ined undefi

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Intel[®] Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the backlight setting.

Intel[®] Seamless Display Refresh Rate Technology (Intel[®] SDRRS Technology)

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when plugged in with an AC power adaptor or when the end user has not selected/enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the notebook is on battery power and when the user has selected/enabled this feature. There are two distinct implementations of Intel DRRS - static and seamless. The static Intel DRRS method uses a mode change to assign the new refresh rate. The seamless Intel DRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode et change (SetMode) method.

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5.0 Thermal Management

The thermal solution provides both component-level and system-level thermal management. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature (Tj_{Max}) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skintemperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP represents an expected maximum sustained power from realistic applications. TDP may be exceeded for short periods of time or if running a "power virus" workload.

The processor integrates multiple processing and graphics cores and PCH on a single package. This may result in differences in the power distribution across the die and must be considered when designing the thermal solution.

Intel[®] Turbo Boost Technology 2.0 allows processor cores and processor graphics cores to run faster than the guaranteed frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current specification limits. When Intel Turbo Boost Technology 2.0 is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of available TDP headroom in the processor package.
- The processor may exceed the TDP for short durations to use any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues since more applications will tend to run at or near TDP for significant periods of time.

Note:

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Intel Turbo Boost Technology 2.0 availability may vary between the different SKUs.

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5.2

5.3

Intel[®] Turbo Boost Technology 2.0 Power Monitoring

undefined und When operating in turbo mode, the processor monitors its own power and adjusts the turbo frequencies to maintain the average power within limits over a thermally significant time period. The processor calculates the package power that consists of the processor core power and graphics core power. In the event that a workload causes the power to exceed program power limits, the processor will protect itself using the Adaptive Thermal Monitor.

Intel[®] Turbo Boost Technology 2.0 Power Control

Illustration of Intel Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing for customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces

5.3.1 **Package Power Control**

The package power control allows for customization to implement optimal turbo within platform power delivery and package thermal solution limitations.

Table 20. Intel[®] Turbo Boost Technology 2.0 Package Power Control Settings

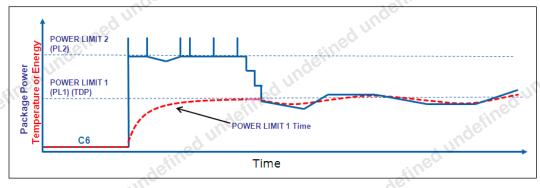
MSR: Address:	MSR_TUR 610h	BO_POWER_LIM	adefine	
Control	Bit	Default	Description	. U
POWER_LIMIT_1 (PL1)	14:0	SKU TDP	 This value sets the average power limit over a long time period. This is normally aligned to the TDP of the part and steady-state cooling capability of the thermal solution. The default value is the TDP for the SKU. PL1 limit may be set lower than TDP in real time for specific needs, such as responding to a thermal event. If it is set lower than TDP, the processor may require to use frequencies below the guaranteed P1 frequency to control the low-power limits. The PL1 Clamp bit [16] should be set to enable the processor to use frequencies below P1 to control the set-power limit. PL1 limit may be set higher than TDP. If set higher than TDP, the processor could stay at that power level continuously and cooling solution improvements may be required. 	Jundefineo
POWER_LIMIT_1_TIME (Turbo Time Parameter)	23:17	1 sec	This value is a time parameter that adjusts the algorithm behavior to maintain time averaged power at or below PL1. The hardware default value is 1 second; however, 28 seconds is recommended for most mobile applications.	Indefined
POWER_LIMIT_2 (PL2)	46:32	1.25 x TDP	PL2 establishes the upper power limit of turbo operation above TDP, primarily for platform power supply considerations. Power may exceed this limit for up to 10 ms. The default for this limit is 1.25 x TDP; however, the BIOS may reprogram the default value to maximize the performance within platform power supply considerations. Setting this limit to TDP will limit the processor to only operate up to the TDP. It does not disable turbo because turbo is opportunistic and power/temperature dependent. Many workloads will allow some turbo frequencies for powers at or below TDP.	jd t
Sine	d under		ed undefine	d undefined
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Figure 12. Package Power Control



Jefined und 5.3.2 Turbo Time Parameter

Turbo Time Parameter is a mathematical parameter (units in seconds) that controls the Intel Turbo Boost Technology 2.0 algorithm using moving average of energy usage. During a maximum power turbo event of about 1.25 x TDP, the processor could sustain PL2 for up to approximately 1.5 times the Turbo Time Parameter. If the power value and/or Turbo Time Parameter is changed during runtime, it may take approximately 3 to 5 times the Turbo Time Parameter for the algorithm to settle at the new control limits. The time varies depending on the magnitude of the change and other factors. There is an individual Turbo Time Parameter associated with Package Power Control.

Configurable TDP (cTDP) and Low-Power Mode

Configurable TDP (cTDP) and Low-Power Mode (LPM) form a design vector where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low-Power Mode technologies offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configuration and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to PL1 and associated frequencies for the scenario with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in OS power policies or hardware events such as docking a system, flipping a switch or pressing a button. cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

Note:

5.4

Configurable TDP and Low-Power Mode technologies are not battery life improvement technologies.

Configurable TDP

Note:

5.4.1

Configurable TDP

Configurable TDP availability may vary between the different SKUs.

With cTDP, the processor is now capable of altering the maximum sustained power with an alternate IA core base frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

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cTDP consists of three modes as shown in the following table.

Table 21. **Configurable TDP Modes**

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Configurable TI	DP Modes	
Mode	Description	d un.
Nominal	This is the processor's rated frequency and TDP.	etine
TDP-Up	When extra cooling is available, this mode specifies a higher TDP and higher guaranteed frequency versus the nominal mode.	anoc
TDP-Down	When a cooler or quieter mode of operation is desired, this mode specifies a lower TDP and lower guaranteed frequency versus the nominal mode.	

In each mode, the Intel Turbo Boost Technology 2.0 power and frequency ranges are reprogrammed and the OS is given a new effective HFM operating point. The Intel DPTF driver assists in all these operations. The cTDP mode does not change the max per-core turbo frequency.

ndefined undefined und 5.4.2 **Low-Power Mode**

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Low-Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

Through the DPTF driver, LPM can be configured to use each of the following methods to reduce active power:

- Restricting Intel Turbo Boost Power limits and IA core Turbo Boost availability
- Off-Lining core activity (Move processor traffic to a subset of cores)
- Placing an IA Core at LFM or LSF (Lowest Supported Frequency)
- Utilizing IA clock modulation
- Reducing number of active EUs to GT2 equivalent (Applicable for GT3 SKUs Only)
- LPM power as listed in the TDP Specifications table is defined at a point which IA cores working at MFM, GT = RPn and 1 core active

Off-lining core activity is the ability to dynamically scale a workload to a limited subset of cores in conjunction with a lower turbo power limit. It is one of the main vectors available to reduce active power. However, not all processor activity is ensured to be able to shift to a subset of cores. Shifting a workload to a limited subset of cores allows other cores to remain idle and save power. Therefore, when LPM is enabled, less power is consumed at equivalent frequencies.

Minimum Frequency Mode (MFM) of operation, which is the lowest supported frequency (LSF) at the LFM voltage, has been made available for use under LPM for further reduction in active power beyond LFM capability to enable cooler and quieter modes of operation.

Thermal and Power Specifications

The following notes apply to Table 22 on page 63 and Table 23 on page 64.

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Note	Definition
Note 1	The TDPs given are not the maximum power the processor can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time.
2	TDP workload may consist of a combination of processor-core intensive and graphics-core intensive applications.
3	The thermal solution needs to ensure that the processor temperature does not exceed the maximum junction temperature (Tj_{MAX}) limit, as measured by the DTS and the critical temperature bit.
4	The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Digital Thermal Sensor Accuracy (Taccuracy) on page 68.
efins	Digital Thermal Sensor (DTS) based fan speed control is required to achieve optimal thermal performance. Intel recommends full cooling capability well before the DTS reading reaches Tj_{MAX} . An example of this is $Tj_{MAX} - 10$ °C.
6	The idle power specifications are not 100% tested. These power specifications are determined by the characterization at higher temperatures and extrapolating the values for the junction temperature indicated.
7	At Tj of Tj _{MAX}
8	At Tj of 50 °C
9	At Tj of 35 °C
10	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.
112d	'Turbo Time Parameter' is a mathematical parameter (unit in seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. Refer to Turbo Time Parameter on page 61 for further information.
12	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
13	Processor will be controlled to specified power limit as described in Intel Turbo Boost Technology 2.0 Power Monitoring on page 60. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
14	This is a hardware default setting and not a behavioral characteristic of the part.
15	For controllable turbo workloads, limit may be exceeded for up to 10 ms.
16	Refer to Table 21 on page 62 for the definitions of 'TDP-Nominal', 'TDP-Up', 'TDP-Down'.
17	LPM power level is an opportunistic power and is not a guaranteed value as usages and implementations may vary.
18	Power limits may vary depending on if the product supports the 'TDP-up' and/or 'TDP-down' modes. Default power limits can be found in the PKG_PWR_SKU MSR (614h).
19	May vary based on SKU.
18 19 20	cTDP down power is based on GT2 equivalent graphics configuration. cTDP down does not decrease the number of active Processor Graphics EUs, but relies on Power Budget Management (PL1) to achieve the specified power level.
21	Hardware default values might be overridden by the BIOS.

Table 22. **Thermal Design Power (TDP) Specifications**

				76.				
	Segment	State	Processor Core Frequency	Processor Graphics Core Frequency	Thermal Design Power	Units	Notes	
ed u	U-Processor	TDP-Nominal / HFM	2.0 GHz up to 2.8 GHz	200 MHz up to	28	IUC	1, 2, 7,	
indefine	(Dual Core) 28W GT3	TDP-Down / LFM	800 MHz	1200 MHz	23	W	1, 2, 7, 16, 17, 18	d
d U.		LPM	800 MHz	200 MHz	22.5			etine
		0			UN .	cont	inued	100
		ndefine		definer				U
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(intel	ine ^o		d undefined un	Processors—Ti	nermal Mai		
defined und	Segment	State	Processor Core Frequency	Processor Graphics Core Frequency	Thermal Design Power	Units	Notes	ó
ndetti	U-Processor (Dual Core) 15W	TDP Nominal / HFM TDP-Down /	1.3 GHz up to 1.7 GHz 800 MHz	200 MHz up to 1100 MHz	11.5	W	1, 2, 7, 16, 17, 18	defined und
	GT3	LFM	800 MHz	200 MHz	11		18	and
	U-Processor	TDP-Up TDP Nominal / HFM	1.6 GHz up to 2.3 GHz	200 MHz up to	25 15	d und	1, 2, 7,	-
Lefined un	(Dual Core) 15W GT2	TDP-Down / LFM	800 MHz	1100 MHz	11.5 ndefin	w	1, 2, 7, 16, 17, 18	
-gein,	1	LPM	800 MHz	200 MHz	11			JUN
TUC	Y-Processor (Dual Core)	TDP Nominal / HFM	1.3 GHz up to 1.4 GHz	200 MHz up to	indefinition 11.5			defineu
	11.5W (6W SDP / 4.5W	TDP-Down / LFM	800 MHz	850 MHz	9.5 (6W SDP / 4.5W SDP)	w	19	UNC
	SDP)	LPM	600 MHz	200 MHz	9	2	elli	

Table 23. **Junction Temperature Specification**

Segment	Symbol	Package Turbo Parameter	Min	Default	Max	Units	Notes	
U-Processor (Dual Core)	Тј	Junction temperature limit	0	_	100	٥C	3, 4, 5	e e
(-Processor (Dual Core)	Tig	Junction temperature limit	0	- 10	100	٥C	3, 4, 5	ndefine

Maximum Idle Power Specification Table 24.

		-								811.	-
	Symbol	Parameter		cessor ith GT3		cessor vith GT3	6W S 4.5W	Cessor DP / SDP GT2	Unit	Note	
red		d un	Min	Max	Min	Max	Min	Max			
undefined	P _{PACKAGE} (C7)	Package power in Package C7 state	_	0.95	-	1.5	eq.	0.85	w	1, 3	ed ut
ð. ⁻	P _{PACKAGE} (C8)	Package power in Package C8 state	_	0.12		0.18	_	0.1	w	1	ndefine
	Ppackage(C9)	Package power in Package C9 state	_	0.052	sinec.	0.1	_	0.04	w	1	d U.
	P _{PACKAGE} (C10)	Package power in Package C10 state	-	0.052	-	0.1	_	0.04	w	1, 4	-
ed l	P _{PACKAGE} (Sx/M3) INT_SUS	Package power in System S3/S4/S5 and M3 state (internal Suspend)	defin	60	_	60	-	60	mW	1, 2	
d undefined	P _{PACKAGE} (Sx/Moff) INT_SUS	Package power in System S3/S4/S5 and Moff state (internal Suspend)	_	50	_	50	nedv	50	mW	1, 2	sined "
300			I			ino	1	1	contin	nued	derr
			Malaila Ta		etined			- 1-11- T-1-			led une
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Thermal Management—Processors



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	Thermal Manage	ment—Processors	ed un	defined					int	el)	
defined unde	Symbol	Parameter		ocessor vith GT3		ocessor vith GT3	6W 9 4.5W	cessor SDP / / SDP i GT2	Unit	Note	und
noc		delli	Min	Max	Min	Max	Min	Max]		ed
	Ppackage(sx/m3) ext_sus	Package power in System S3/S4/S5 and M3 state (external Suspend)	_	51	d unde	51	_	51	mW	1, 2	definit
	Ppackage(sx/moff) ext_sus	Package power in System S3/S4/S5 and Moff state (external Suspend)	-d un	de ¹ 33	_	33	_	33	mW	1, 2	
und	PPACKAGE(Deep Sx)	Package power in System Deep Sx state	<u>06</u>	19	_	19	-	19	mW	1, 2	
ined .	Notes: 1. Packag	ge power includes both MCP compor	nents: pro	cessor and	J PCH.	<u>.</u>	noe				

2. Measured at Tj = 35 °C.

3. The C7 power is measured with LLC ON.

4. The C10 power is measured with LAN disabled.

5.6 Thermal Management Features

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. To protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

undefined undefined Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor core power consumption and temperature until it operates at or below its maximum operating temperature. Processor core power reduction is achieved by:

- Adjusting the operating frequency (using the core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor core clocks (duty cycle).

The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS) meets or exceeds its maximum operating temperature. The maximum operating temperature implies either maximum junction temperature T_{MAX} , or T_{MAX} minus TCC Activation offset.

Exceeding the maximum operating temperature activates the thermal control circuit (TCC), if enabled. When activated the thermal control circuit (TCC) causes both the processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature exceeds its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Tj_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE TARGET (0x1A2) MSR, bits [23:16]. The TEMPERATURE_TARGET value stays the same when TCC Activation offset is enabled.

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Processors—Thermal Management

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain undefined un processor TDP. The system design should provide a thermal solution that can maintain TDP within its intended usage range.

Note:

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Adaptive Thermal Monitor protection is always enabled.

5.6.1.1 Thermal Control Circuit (TCC) Activation Offset

TCC Activation Offset can be used to activate the Adaptive Thermal Monitor at temperatures lower than Tj_{MAX}. It is the preferred thermal protection mechanism for Intel Turbo Boost Technology 2.0 operation since ACPI passive throttling states will pull the processor out of turbo mode operation when triggered. An offset (in degrees Celsius) can be written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24]. This value will be subtracted from the value found in bits [23:16]. The default offset is 0 °C, TCC activation will occur at Tj_{MAX}. The offset should be set lower than any other protection such as ACPI _PSV trip points.

5.6.1.2 Frequency / Voltage Control

Upon Adaptive Thermal Monitor activation, the processor core attempts to dynamically reduce processor core power by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the core bus ratio, and number of cores in deep C-states.
- The core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the maximum operating temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor core will transition to the new target automatically.

- On an upward operating point transition, the voltage transition precedes the frequency transition.
- On a downward transition, the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor core optimized target frequency, the processor will transition to the P-state operating point.

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Thermal Management—Processors



5.6.1.3

Clock Modulation If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased by the same amount as the duty cycle when undefined clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

Digital Thermal Sensor

Each processor execution core has an on-die Digital Thermal Sensor (DTS) that detects the core's instantaneous temperature. The DTS is the preferred method of monitoring processor die temperature because:

- It is located near the hottest portions of the die.
- It can accurately track the die temperature and ensure that the Adaptive Thermal Monitor is not excessively activated.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Platform Environmental Control Interface (PECI) on page 29.

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given core. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE THERM STATUS MSR 1B1h and IA32 THERM STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C-states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (T_{MAX}), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from Tj_{MAX}. The DTS does not report temperatures greater than Tj_{MAX}. The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package

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5.6.2



Processors—Thermal Management

DTS indicates that it has reached the TCC activation (a reading of 0h, except when the TCC activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the core's local APIC. Refer to the Intel[®] 64 and IA-32 Architectures Software Developer's Manual for specific register and programming details.

1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ± 5 °C within the entire operating range.

5.6.2.2 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability well before the DTS reading reaches T_{JMAX} .

5.6.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted when the processor temperature has reached its maximum operating temperature (Tj_{MAX}). Only a single PROCHOT# pin exists at a package level. When any core arrives at the TCC activation point, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

5.6.3.1 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to bi-directional. However, it is recommended to configure the signal as an input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components in case the components overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system de-asserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

Note:

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When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced; however, the reduction rate is slower than the system PROCHOT# response of < 100 us. The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

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5.6.3.2

Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.6.3.3 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

Indefined undefined Low-Power States and PROCHOT# Behavior 5.6.3.4

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wakeup, if the processor is still hot, the PROCHOT# will re-assert, although typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.6.3.5 **THERMTRIP#** Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point the THERMTRIP# signal will go active.

Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE THERM STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the Intel® 64 and IA-32 Architectures Software Developer's Manual.

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Processors—Thermal Management

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On-Demand Mode The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.6.4.1 **MSR Based On-Demand Mode**

If Bit 4 of the IA32 CLOCK MODULATION MSR is set to a 1, the processor will immediately reduce its power consumption using modulation of the internal core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32 CLOCK MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor core's clock independently.

5.6.4.2 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system ned undefined software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor cores simultaneously.

Intel[®] Memory Thermal Management 5.6.5

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor – either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

Memory temperature can be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reported to the processor through the PECI 3.0 interface. This methodology is known as PECI injected temperatures and is a method of Closed Loop Thermal Management (CLTM). CLTM requires the use of a physical thermal sensor. EXTTS# is another method of CLTM; however, it is only capable of reporting memory thermal status to the processor. EXTTS# consists of two GPIO pins on the PCH where the state of the pins is communicated internally to the processor.

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Thermal Management—Processors



red undefined undefine When a physical thermal sensor is not available to report temperature, the processor supports Open Loop Thermal Management (OLTM) that estimates the power consumed per rank of the memory using the processor DRAM power meter. A per rank power is associated with the warm and hot thresholds that, when exceeded, may trigger memory thermal throttling.

Scenario Design Power (SDP)

Scenario Design Power (SDP) is a usage-based design specification, and provides an additional reference design point for power constrained platforms. SDP is a specified power level under a specific scenario workload, temperature, and frequency.

Intel recommends setting POWER_LIMIT_1 (PL1) to the system cooling capability (SDP level, or higher). While the SDP specification is characterized at Tj of 80 °C, the functional limit for the product remains at Tj_{MAX}. Customers may choose to have the processor invoke TCC Activation Throttling at 80 °C, but is not required.

The processors that have SDP specified can still exceed SDP under certain workloads, such as TDP workloads. TDP power dissipation is still possible with the intended usage models, and protection mechanisms to handle levels beyond cooling capabilities are recommended. Intel recommends using such thermal control mechanisms to manage situations where power may exceed the thermal design capability.

Note: undefined und

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Note:

cTDP-Down mode is required for Intel[®] Core[™] processor products in order to achieve SDP.

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Processors—Signal Description



Signal Description 6.0

This chapter describes the processor signals. The signals are arranged in functional groups according to the associated interface or category. The following notations are used to describe the signal type.

Notation	Signal Type	
I	Input pin	
0	Output pin	
I/O	Bi-directional Input/Output pin	6
(see the followi	ription also includes the type of buffer used for the particular signal ng table).	undefill
Signal	Description]

Table 25. Signal Description Buffer Types

Signal	Description
CMOS	CMOS buffers. 1.05V- tolerant
DDR3L/DDR3L- RS	DDR3L/DDR3L-RS buffers: 1.35 V-tolerant
LPDDR3	LPDDR3 buffers: 1.2 V- tolerant
A ed uno	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
VR Enable CMOS	Voltage Regulator Asynchronous CMOS output
Ref	Voltage reference signal
Asynchronous ¹	Signal has no timing relationship with any reference clock.
1. Qualifier for a	buffer type.

undefined undefined un **System Memory Interface Signals**

Table 26.

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DDR3L/ DDR3L-RS Memory Channel A Interface (Memory-Down / SO-DIMM) **Signals**

Signal Name	Description	Direction / Buffer Type	
SA_BS[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank.	sined o	
SA_WE#	Write Enable Control Signal: This signal is used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	0	
ACC		continued	e
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derr	ad undefine	a effined	
	tion–Processors	ed undefined undefined	(intel)
ndefined undefined une	Signal Name	Description	Direction / Buffer Type
ndefinec	SA_RAS#	RAS Control Signal: This signal is used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	0
	SA_CAS#	CAS Control Signal: This signal is used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	0 U
undefined undefined und	SA_DQSP[7:0] SA_DQSN[7:0]	Data Strobes: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS#[7:0] during read and write transactions.	I/O
ad unoc	SA_DQ[63:0]	Data Bus: Channel A data signal interface to the SDRAM data bus.	I/O
adefine	SA_MA[15:0]	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.	0
21.	SA_CKP[1:0] SA_CKN[1:0]	SDRAM Differential Clock: Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CKP and the negative edge of its complement SA_CKN are used to sample the command and control signals on the SDRAM.	0
ined und	SA_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	moetines
undefined undefined un	SA_CKE[3:0]	 Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up Power down SDRAM ranks Place all SDRAM ranks into and out of self-refresh during STR When 1R DDR3L (SODIMM/MD) CKE[0] is used When 2R DDR3L (SODIMM/MD) CKE[1:0] are used 	0
	SA_ODT	On Die Termination: Active Termination Control.	0

- 2: undefined undefined Table 27.

DDR3L / DDR3L-RS Memory Channel B Interface (Memory-Down / SO-DIMM) Signals

Indefil	Signal Name	Description	Direction / Buffer Type
ndefined undefine	SB_BS[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank.	0
d under	SB_WE#	Write Enable Control Signal: This signal is used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	0
11	SB_RAS#	RAS Control Signal: This signal is used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	o sineč
defined t	SB_CAS#	CAS Control Signal: This signal is used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	ed Voder
ndefined undefine	SB_DQSP[7:0] SB_DQSN[7:0]	Data Strobes: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS#[7:0] during read and write transactions.	I/O
ed un	SB_DQ[63:0]	Data Bus: Channel A data signal interface to the SDRAM data bus.	I/O
	- nev		continued

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undefined un Processors—Signal Description

inte	ned undefine
ndefined undefine	Signal Name
define	SB_MA[15:0]

der	ed undefine	undefined	
intel		Processo	rs—Signal Description
ad unde	Signal Name	Description	Direction / Buffer Type
define	SB_MA[15:0]	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.	0
	SB_CKP[1:0] SB_CKN[1:0]	SDRAM Differential Clock: Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CKP and the negative edge of its complement SB_CKN are used to sample the command and control signals on the SDRAM.	0
sined uno	SB_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	nostines
undefined undefin	SB_CKE[3:0]	 Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up Power down SDRAM ranks Place all SDRAM ranks into and out of self-refresh during STR When 1R DDR3L (SODIMM/MD) CKE[0] is used When 2R DDR3L (SODIMM/MD) CKE[1:0] are used 	o
	SB_ODT	On Die Termination: Active Termination Control.	0

undefined undefined

Table 28. LPDDR3 Memory Channel A Interface (Memory-Down) Signals

	SB_ODT	On Die Termination: Active Termination Control.	0	UN
Table 28.	LPDDR3 Memor	y Channel A Interface (Memory-Down) Signal	s stineo	
defined -	Signal Name	Description	Direction / Buffer Type	
ed und	SA_DQ[63:0]	Data Bus: Channel A data signal interface to the SDRAM data bus.	I/O	
undefined undefined u.	SA_DQSP[7:0] SA_DQSN[7:0]	Data Strobes: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS#[7:0] during read and write transactions.	I/O	terined un
	SA_CAA[9:0]	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.	0	unou
edu	SA_CAB[9:0]	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.	odefine	
undefined undefinet.	SA_CKP[1:0] SA_CKN[1:0]	SDRAM Differential Clock: Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CKP and the negative edge of its complement SA_CKN are used to sample the command and control signals on the SDRAM.	stined un	
undefine	SA_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	ined u
sined	SA_CKE[3:0]	 Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up Power down SDRAM ranks Place all SDRAM ranks into and out of self-refresh during STR When 1R LPDDR3 CKE[0] and CKE[2] are used for Rank 0 	ondefine	d undefin.
unden.		When 2R LPDDR3 CKE[0] and CKE[2] are used for Rank 0 & CKE[1] and CKE[3] are used for Rank 1	efined	
	SA_ODT	On Die Termination: Active Termination Control.	0	
d undefined undefined	red und	atime d undefined t		indefined
	ndefill	define c		led u.
Mobile 4th Gener	ration Intel [®] Core [™] Proc	essor Family, Mobile Intel ${}^{\otimes}$ Pentium ${}^{\otimes}$ Processor Family, and Mobil	e Intel [®] Celeron [®]	

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Signal Description—Processors

Table 29.

LPDDR3 Memory Channel B Interface (Memory-Down) Signals

	Signal Name	Description	Direction / Buffer Type	
	SB_DQ[63:0]	Data Bus: Channel A data signal interface to the SDRAM data bus.	I/O	ni)
unde	SB_DQSP[7:0] SB_DQSN[7:0]	Data Strobes: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS#[7:0] during read and write transactions.	I/O	19e.
atined	SB_CAA[9:0]	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.	d undo	
d unde.	SB_CAB[9:0]	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.	0	
definer	SB_CKP[1:0] SB_CKN[1:0]	SDRAM Differential Clock: Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CKP and the negative edge of its complement SB_CKN are used to sample the command and control signals on the SDRAM.	0	
6	SB_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	uder
efined une		 Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up Power down SDRAM ranks. 	dundefit	
defined unot	SB_CKE[3:0]	 Place all SDRAM into and out of self-refresh during STR. When 1R LPDDR3 CKE[0] and CKE[2] are used for Rank0 When 2R LPDDR3 CKE[0] and CKE[2] are used for Rank 0 and CKE[1] and CKE[3] are used for Rank 1 	0	
	SB_ODT	On Die Termination: Active Termination Control.	0	

Memory Compensation and Miscellaneous Signals 6.2

LPDDR3 / DDR3L / DDR3L-RS Reference and Compensation Signals

	Signal Name	Description	Direction / Buffer Type	
dunc	SM_RCOMP[2:0]	System Memory Impedance Compensation:	I	1
	SM_VREF_CA SM_VREF_DQ0 SM_VREF_DQ1	Memory Channel A/B DIMM DQ Voltage Reference: The output pins are connected to the MD/DIMMs, and holds VDDQ/2 as reference voltage.	0	
	SM_PG_CNTL1	System Memory Power Gate Control: This signal disables the platform memory VTT regulator in C8 and deeper and S3 states.	CMOS OUTPUT	unde
undefined u	.00-	defined under	ned undefine	
eined L		d une under		

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undefined un Processors—Signal Description

hed undefined undefined **Reset and Miscellaneous Signals**

Table 31. **Reset and Miscellaneous Signals**

ble 31. Reset and Mi	scellaneous Signals	
Signal Nam	Description	Direction / Buffer Type
CFG[19:0]	 Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. CFG[3]: MSR Privacy Bit Feature 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden CFG[4]: eDP enable 	I/O GTL
under under	 - 1 = Disabled - 0 = Enabled • CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands. 	
CFG_RCOMP	Configuration resistance compensation. Use a 49.9 Ω ±1% resistor to ground.	
FC_x	FC (Future Compatibility) signals are signals that are available fo compatibility with other processors. A test point may be placed on the board for these lands.	r under
FC_x IST_TRIGGER	Signal is for IFDIM testing only.	I CMOS
IVR_ERROR	Signal is for debug. If both THERMTRIP# and this signal are simultaneously asserted, the processor has encountered an unrecoverable power delivery fault and has engaged automatic shutdown as a result.	O CMOS
RSVD RSVD_TP RSVD_NCTF	RESERVED: All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.	No Connect Test Point Non-Critical to Function
TESTLO_X	TESTLO should be individually connected to V_{SS} through a resistor.	ed un
ndefined un	defined undefined undefined undefined	-
TESTLO_x	TESTLO should be individually connected to V _{SS} through a resistor.	ned undefin

ined undefined undef Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] Processor Family Datasheet - Volume 1 of 2 76 , o

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Signal Description—Processors

red undefined undefined embedded DisplayPort* (eDP*) Signals

embedded Display Port* Signals Table 32.

	ble 32.	embedded Display	Description	Direction / Puffer Tyre	21
		Signal Name	2011	Direction / Buffer Type	
	<i></i>	eDP_TXP[3:0] eDP_TXN[3:0]	embedded DisplayPort Transmit Differential Pair	O eDP	
	d under	eDP_AUXP eDP_AUXN	embedded DisplayPort Auxiliary Differential Pair	O eDP	
defil	1ec	eDP_RCOMP	embedded DisplayPort Current Compensation	I/O A	
efined unc		eDP_DISP_UTIL	Low voltage multipurpose DISP_UTIL pin on the processor for backlight modulation control of embedded panels and S3D device control for active shutter glasses. This pin will co-exist with functionality similar to existing BKLTCTL pin on the PCH.	O Asynchronous CMOS	sined
6.		Display Interfa	4 Unco		dell

6.5

Display Interface Signals

Table 33.

Display Interface Signals

Signal Name	Description	Direction / Buffer Type	
DDIB_TXP[3:0] DDIB_TXN[3:0]	Digital Display Interface Transmit Differential Pair	O DP*/HDMI*	
DDIC_TXP[3:0] DDIC_TXN[3:0]	Digital Display Interface Transmit Differential Pair	O DP*/HDMI*	sined un
Testability Sign Testability Signals	nals	defined	under
Signal Name	Description	Direction / Buffer	

6.6

Table 34.

Testability Signals

Testability Signals

ndefine	Signal Name	Description	Direction / Buffer Type
ndefined undefine	BPM#[7:0]	Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O GTL
, U.	PRDY#	Processor Ready: This signal is a processor output used by debug tools to determine processor debug readiness.	O GTL
A UN	PREQ#	Processor Request: This signal is used by debug tools to request debug operation of the processor.	I GTL GTL
a undefined	PROC_TCK	Test Clock: This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal must be driven low or allowed to float during power on Reset.	stined Under
Indefinet	PROC_TDI	Processor Test Data In: This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I GTL
90.		AC1.	continued
	odefined	Lefined unc	

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undefined un Processors—Signal Description

6	ned undefine	Aetined undefined Processo	ors—Signal Description
	Signal Name	Jeffned Unor	Direction / Buffer
	Signar Name	Inoc Description	Туре
	PROC_TDO	Processor Test Data Out: This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O Open Drain
	PROC_TMS	Processor Test Mode Select: This is a JTAG specification supported signal used by debug tools.	I GTL
	PROC_TRST#	Processor Test Reset: This signal resets the Test Access Port (TAP) logic. This signal must be driven low during power on Reset.	I GTL
		ermal Protection Signals	inedur
	Signal Name	Description	Direction / Buffer

Error and Thermal Protection Signals

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Signal Name	Description	Direction / Buffer Type	
PECI PROCHOT#	Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	O GTL	Indefi
PECI	Platform Environment Control Interface: A serial sideband interface to the processor, it is used primarily for thermal, power, and error management.	I/O Asynchronous	
sineu	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	GTL Input Open-Drain Output	undef
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O Asynchronous OD	
undefined undefined undef	THERMTRIP# pin.		de
d undefine	Indefined	define	d une
undefine	indefined t	efinedunt	
2	stined the unc		ed und

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Signal Description—Processors



ined undefined undefined **Power Sequencing Signals**

Table 36. **Power Sequencing Signals**

	ed uno.		unden.		
ed u	6.8 Table 36.	Power Sequencing	~9°C	ed un	
defin	Table 50.	Signal Name	Description	Direction / Buffer Type	sined un
unde	stined unde	PROCPWRGD	The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until the supplies come within specification. The signal must then transition monotonically to a high state.	I Asynchronous CMOS	
ndefined	6	VCCST_PWRGD	The processor requires this input signal to be a clean indication that the V_{CCST} and V_{DDQ} power supplies are stable and within specifications. This single must have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until the supplies come within specification. The signal must then transition monotonically to a high state."	I Asynchronous CMOS	ndefined
und	lefined un	PROC_DETECT#	(Processor Detect): This signal is pulled down directly (0 Ohms) on the processor package to ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	med undert	
ndefineo	6.9	Processor Pow	er Signals	,	ed'
	Table 37.	Processor Power Si	gnals		define
		Signal Name	Description	Direction / Buffer	711-

undefined undefined undf **Processor Power Signals**

Table 37. **Processor Power Signals**

Processor Pow	d une										
	ver Signals		6								
Processor Power S	Processor Power Signals										
Signal Name	Description	Direction / Buffer Type	unc								
VCC	Processor main power rail.	Ref									
VDDQ	Processor I/O supply voltage for DDR3L/DDR3L-RS/ LPDDR3.	Ref									
VCCST	Sustain voltage for the processor in standby modes	Ref									
VIDSOUT VIDSCLK VIDALERT#	VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.	I/O CMOS O CMOS I CMOS	sined								
VR_EN	Sideband output from the processor which controls disabling of the VR when the processor is in the C10 state. This signal will be used to disable the VR only if the processor is configured to support VR disabling using VR_CURRENT_CONFIG MSR (601h).	O VR Enable CMOS	under								
VR_READY	Sideband signal which indicates to the processor that the external voltage regulator for the V_{CC} power rail is valid.	I CMOS									
adefined undefine	d uns	ge.	d undefine								
	Signal Name VCC VDDQ VCCST VIDSOUT VIDSCLK VIDALERT# VR_EN	Signal NameDescriptionVCCProcessor main power rail.VDDQProcessor I/O supply voltage for DDR3L/DDR3L-RS/ LPDDR3.VCCSTSustain voltage for the processor in standby modesVIDSOUT VIDSCLK VIDALERT#,VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.Sideband output from the processor is in the C10	Signal NameDescriptionDirection / Buffer TypeVCCProcessor main power rail.RefVDDQProcessor I/O supply voltage for DDR3L/DDR3L-RS/ LPDDR3.RefVCCSTSustain voltage for the processor in standby modesRefVIDSOUT VIDSCLK VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.I/O CMOS O CMOS I CMOSSideband output from the processor which controls disabling of the VR when the processor is in the C10O								

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Processors—Signal Description

6.10 **Sense Signals**

Table 38. **Sense Signals**

Sense Signals	defined unc	under	
Sense Signals	dunde		inde
Signal Name	Description	Direction / Buffer Type	sined U.
VCC_SENSE VSS_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low- impedance connection to the processor input V_{CC} voltage and ground. The signals can be used to sense or measure voltage near the silicon.	O A	under
	-d un	inder	1

Ground and Non-Critical to Function (NCTF) Signals

6.11

Ground and Non-Critical to Function (NCTF) Signals

	Signal Name		Description	Direction / Buffer Type	ed un
	VSS	Processor ground node	nder	GND	Jefine
	VSS_NCTF	Non-Critical to Funct mechanical reliability.	ion: These signals are for	package _	Junoc
Jefined un	DAISY_CHAIN_NCTF_[Ball	for BGA solder joint rel function. These signals are conn follows: Package A1 Corner DAISY_CHAIN_NCT DAISY_CHAIN_NCT DAISY_CHAIN_NCT DAISY_CHAIN_NCT DAISY_CHAIN_NCT DAISY_CHAIN_NCT Package AY1 Corne DAISY_CHAIN_NCT DAISY_CHAIN_NCT	F_A62 to DAISY_CHAIN_N F_B61 to DAISY_CHAIN_N F_B63 to DAISY_CHAIN_N F_AW1 to DAISY_CHAIN_N F_AY3 to DAISY_CHAIN_N F_AY2 to DAISY_CHAIN_N er F_AY60 to F_AW61 F_AW61 F_AW62 F_AW62 F_AY62 to	TF_C1 CTF_C1 CTF_B3 CTF_A4 CTF_A61 CTF_B62 CTF_A60 NCTF_AW3 CTF_AW2	ad undefined u
2	Processor Inte	rnal Pull-Up /d	Pull-Down Ter	minations	led u.
40.	Processor Internal	JINC.		, under	
	Signal Name	Pull Up / Pull Down	Rail	Value	7

Processor Internal Pull-Up / Pull-Down Terminations 6.12

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Processor Internal Pull-Up / Pull-Down Terminations

				1
Signal Name	Pull Up / Pull Down	Rail	Value	
BPM[7:0]	Pull Up	Vcc _{IO}	40-60 Ω	
PREQ#	Pull Up	Vcc _{IO}	40-60 Ω	
PROC_TDI	Pull Up	Vcc _{st}	30-70 Ω	5 N 2
20.			continued	Ye,
defines		sined t		ed une
inv	8	S/,		
tion Intel [®] Core [™] Process	or Family, Mobile Intel [®] Pentiur	m [®] Processor Family, and M	Nobile Intel [®] Celeron [®]	

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Per.	scription-Processors	Pull Up / Pull Down	defined .	intel	sined un-
	stined un	used u	noc	lintal	qe _{tt} .
Signal De	scription—Processors	defill		Inter	
Signal De		red un		d une	
under	Signal Name	Pull Up / Pull Down	Rail	Value	
	PROC_TMS	Pull Up	Vcc _{ST}	30-70 Ω	6
dein	CFG[19:0]	Pull Up	Vcc _{ST}	5–8 kΩ	d une
	CATERR#	Pull Up	Vcc _{ST}	30-70 Ω	stines
undefined l	Indein	odefined undefines		stined undefined.	
ndefineo	sined undefined	⁷ /1,	undefined uno		undefined un
od undefined	under	undefined undefine		lefined undefined	
undefine	defined undefined		d undefined un		undefined
ndefined undefined	Signal Name PROC_TMS CFG[19:0] CATERR#	undefined unde.	med un	Idefined undefin	
, UI .	d undefined under	ed undefine	ed undefit.	undefine	d undefines

ined underned underned underned underned underned underned underned under ned under ne tel® Per Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] Processor Family .ub. July 2014 Datasheet - Volume 1 of 2 -4 undefir Order No.: 329001-007 81



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Processors—Electrical Specifications

7.0 Electrical Specifications

This chapter provides the processor electrical specifications including integrated voltage regulator (VR), V_{CC} Voltage Identification (VID), reserved and unused signals, signal groups, Test Access Points (TAP), and DC specifications.

Integrated Voltage Regulator

A new feature to the processor is the integration of platform voltage regulators into the processor. Due to this integration, the processor has one main voltage rail (V_{CC}) and a voltage rail for the memory interface (V_{DDQ}), compared to six voltage rails on previous processors. The V_{CC} voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, system agent, and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The processor V_{CC} rail will remain a VID-based voltage with a loadline similar to the core voltage rail (also called V_{CC}) in previous processors.

Power and Ground Pins

The processor has VCC, VDDQ, and VSS (ground) pins for on-chip power distribution. All power pins must be connected to their respective processor power planes; all VSS pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The VCC pins must be supplied with the voltage determined by the processor **S**erial **V**oltage **ID**entification (SVID) interface. Table 41 on page 83 specifies the voltage level for the various VIDs.

V_{CC} Voltage Identification (VID)

The processor uses three signals for the serial voltage identification interface to support automatic selection of voltages. The following table specifies the voltage level corresponding to the 8-bit VID value transmitted over serial VID. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. VID signals are CMOS push/pull drivers. See the *Voltage and Current Specifications* section for the DC specifications for these signals. The VID codes will change due to temperature and/or current load changes to minimize the power of the part. A voltage range is provided in the *Voltage and Current Specifications* section. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in the *Voltage and Current Specifications* section. The processor provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

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a uno	Ta	ble	41	L.		Vo	Ita	ige	Regulato	or (VR) 12.5 Vo	lta	ge	Id	en	tifi	cat	tio	n		stine		1
defined undef	B i t 7	B i t 6	B i t 5	B i t 4	B i t 3	i t	: t	B E i i t 1 1 (sineo	U ^{III} V _{cc}		B i t 7	B i t 6	B i t 5	B i t 4	B i t 3	B i t 2	B i t 1	B i t 0	Hex	V _{cc}	defined
	0	0	0	0	0	+	-			0.0000	-	0	0	1	0	0	0	0	1	21h	0.8200	etinec
	0	0	0	0	0	-	20			0.5000	-	0	0	1	0	0	0	1	0	22h	0.8300	100
	0	0	0	0	0	1	_	_		0.5100		0	0	1	0	0	0	1	1	23h	0.8400	
	0	0	0	0	0	-	-	_		0.5200	0	0	0	1	0	0	1	0	0	24h	0.8500	
26	0	0	0	0	0	1	. 0	5 () 04h	0.5300		0	0	1	0	0	1	0	1	25h	0.8600	
y uno.	0	0	0	0	0	1	. 0) :	. 05h	0.5400	_	0	0	1	0	0	1	1	0	26h	0.8700	
defined und	0	0	0	0	0	1	. 1	1 () 06h	0.5500		0	0	1	0	0	1	1	1	27h	0.8800	
9err	0	0	0	0	0	1	. 1	1	. 07h	0.5600		0	0	1	0	1	0	0	0	28h	0.8900	5
	0	0	0	0	1	0	0) () 08h	0.5700		0	0	1	0	1	0	0	1	29h	0.9000	etines
	0	0	0	0	1	0	0) :	09h	0.5800		0	0	1	0	1	0	1	0	2Ah	0.9100	nac
	0	0	0	0	1	0	1	1 (0Ah	0.5900		0	0	1	0	1	0	1	1	2Bh	0.9200	1
	0	0	0	0	1	0) 1	1 :	. 0Bh	0.6000	20	0	0	1	0	1	1	0	0	2Ch	0.9300	
	0	0	0	0	1	1	. 0) (0Ch	0.6100		0	0	1	0	1	1	0	1	2Dh	0.9400	
, unc	0	0	0	0	1	1	. 0) :	0Dh	0.6200		0	0	1	0	1	1	1	0	2Eh	0.9500	
	0	0	0	0	1	1	. 1	1 (0Eh	0.6300		0	0	1	0	1	1	1	1	2Fh	0.9600	
ndefined unc	0	0	0	0	1	1	. 1	1	. 0Fh	0.6400		0	0	1	1	0	0	0	0	30h	0.9700	
	0	0	0	1	0	0	0) כ) 10h	0.6500		0	0	1	1	0	0	0	1	31h	0.9800	stine
	0	0	0	1	0	0	0) • :	. 11h	0.6600		0	0	1	1	0	0	1	0	32h	0.9900	Inde
	0	0	0	1	0	0	1	1 () 12h	0.6700		0	0	1	1	0	0	1	1	33h	1.0000	
	0	0	0	1	0	0	1	1	. 13h	0.6800	20	0	0	1	1	0	1	0	0	34h	1.0100	
	0	0	0	1	0	1	0) () 14h	0.6900		0	0	1	1	0	1	0	1	35h	1.0200	
nu .	0	0	0	1	0	1	0) :	. 15h	0.7000		0	0	1	1	0	1	1	0	36h	1.0300	
	0	0	0	1	0	1	. 1	L () 16h	0.7100		0	0	1	1	0	1	1	1	37h	1.0400	
undefined L	0	0	0	1	0	1	. 1	1 :	. 17h	0.7200		0	0	1	1	1	0	0	0	38h	1.0500	ndefin
UI.	0	0	0	1	1	0	0) () 18h	0.7300		0	0	1	1	1	0	0	1	39h	1.0600	nije.
	0	0	0	1	1	0	0	D C	19h	0.7400		0	0	1	1	1	0	1	0	3Ah	1.0700	inde.
	0	0	0	1	1	0	1	1 () 1Ah	0.7500		0	0	Cl.	1	1	0	1	1	3Bh	1.0800	
	0	0	0	1	1	0	1	1 :	. 1Bh	0.7600		0	0	1	1	1	1	0	0	3Ch	1.0900	
	0	0	0	1	1	1	. 0) () 1Ch	0.7700		0	0	1	1	1	1	0	1	3Dh	1.1000	
	0	0	0	1	1	1	0) :		0.7800		0	0	1	1	1	1	1	0	3Eh	1.1100	
	0	0	0	1	1	1	. 1	1 (0.7900		0	0	1	1	1	1	1	1	3Fh	1.1200	
undefined	0	0	0	1	1	1	_			0.8000		0	1	0	0	0	0	0	0	40h	1.1300	
Un	0	0	1	0	0	0	0) () 20h	0.8100 <i>continued</i>		0	1	0	0	0	0	0	1	41h	1.1400 <i>continued</i>	d undefil
									0	continueu					-	3.0					continueu	, '9e'.

led undefined undefined Table 41 Voltage Regulator (VR) 12 5 Voltage Identification

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		20	0	11.						tined
6	В	в	В	в	В	В	в	В	Hex	ine-
lefined und	i t 7	i t 6	i t 5	i t 4	i t 3	i t 2	i t 1	i t 0	ilex 0	undvcc
	0	1	0	0	0	0	1	0	42h	1.1500
	0	1	0	0	0	0	1	1	43h	1.1600
	0	1	0	0	0	1	0	0	44h	1.1700
	0	1	0	0	0	1	0	1	45h	1.1800
	0	1	0	0	0	1	1	0	46h	1.1900
	0	1	0	0	0	1	1	1	47h	1.2000
defined un	0	1	0	0	1	0	0	0	48h	1.2100
	0	1	0	0	1	0	0	1	49h	1.2200
	0	1	0	0	1	0	1	0	4Ah	1.2300
	0	1	0	0	1	0	1	1	4Bh	1.2400
	0	1	0	0	1	1	0	0	4Ch	1.2500
	0	1	0	0	1	1	0	1	4Dh	1.2600
	0	1	0	0	1	1	1	0	4Eh	1.2700
	0	1	0	0	1	1	1	1	4Fh	1.2800
, ul	0	1	0	1	0	0	0	0	50h	1.2900
idefined un	0	1	0	1	0	0	0	1	51h	1.3000
dein	0	1	0	1	0	0	1	0	52h	1.3100
	0	1	0	1	0	0	1	1	53h	1.3200
	0	1	0	1	0	1	0	0	54h	1.3300
	0	1	0	1	0	1	0	1	55h	1.3400
	0	1	0	1	0	1	1	0	56h	1.3500
	0	1	0	1	0	1	1	1	57h	1.3600
	0	1	0	1	1	0	0	0	58h	1.3700
	0	1	0	1	1	0	0	1	59h	1.3800
defille	0	1	0	1	1	0	1	0	5Ah 🔬	1.3900
ndefined	0	1	0	1	1	0	1	1	5Bh	1.4000
	0	1	0	1	1	1	0	0	5Ch	1.4100
	0	1	0	1	1	1	0	1	5Dh	1.4200
	0	1	0	1	1	1	1	0	5Eh	1.4300
	0	1	0	9	1	1	1	1	5Fh	1.4400
	0	ae	1	0	0	0	0	0	60h	1.4500
undefined	0	1	1	0	0	0	0	1	61h	1.4600
1etine	0	1	1	0	0	0	1	0	62h	1.4700
una-	0	1	1	0	0	0	1	1	63h	1.4800
									201	continued

							in	65			
Vcc				<i>,d '</i>	JUL			Pro	ces	sors—Elect	rical Specification
ined u	, n ^c										d undefine
Vcc		B i t 7	Bit6	Bit5	B i t 4	B i t 3	B i t 2	B i t	B i t 0	Hex	V _{CC} 1.4900 1.5000 1.5100
)0		0	1	1	0	0	1	0	0	64h	1.4900
00		0	1	1	0	0	1	0	1	65h	1.5000
00		0	1	1	0	0	1	1	0	66h	1.5100
00		0	1	1	0	0	1	1	1	67h	1.5200
00	20	0	1	1	0	1	0	0	0	68h	1.5300
00 sineo	1	0	1	1	0	1	0	0	1	69h	1.5400
00	1	0	1	1	0	1	0	1	0	6Ah	1.5500
00	1	0	1	1	0	1	0	1	1	6Bh	1.5600
00	1	0	1	1	0	1	1	0	0	6Ch	1.5700
00	1	0	1	1	0	1	1	0	1	6Dh	1.5800
00	1	0	1	1	0	1	1	1	0	6Eh	1.5900
00		0	1	1	0	1	1	1	1	6Fh	1.6000
00	5	0	1	1	1	0	0	0	0	70h	1.6100
00 000		0	1	1	1	0	0	0	1	71h	1.6200
00	1	0	1	1	1	0	0	1	0	72h	1.6300
00	1	0	1	1	1	0	0	1	1	73h	1.6400
00	1	0	1	1	1	0	1	0	0	74h	1.6500
00	1	0	1	1	1	0	1	0	1	75h	1.6600
00	1	0	1	1	1	0	1	1	0	76h	1.6700
00	1	0	1	1	1	0	1	1	1	77h	1.6800
00		0	1	1	1	1	0	0	0	78h	1.6900
00	þ.	0	1	1	1	1	0	0	1	79h	1.7000
00 00	1	0	1	1	1	1	0	1	0	7Ah	1.7100
00	1	0	1	1	1	1	0	1	1	7Bh	1.7200
00	1	0	1	1	1	1	1	0	0	7Ch	1.7300
00	1	0	1	1	1	1	1	0	1	7Dh	1.7400
00	1	0	1	1	1	1	1	1	0	7Eh	1.7500
00	1	0	1	1	1	1	1	1	1	7Fh	1.7200 1.7300 1.7400 1.7500 1.7600 1.7700 1.7800
00	1	1	0	0	0	0	0	0	0	80h	1.7700
00	6	1	0	0	0	0	0	0	1	81h	1.7800
00 6111		1	0	0	0	0	0	1	0	82h	1.7900
00,1100	1	1	0	0	0	0	0	1	1	83h	1.8000
00	1	1	0	0	0	0	1	0	0	84h	1.8100
00		1	0	0	0	0	1	0	1	85h	1.8200
continued							0				continued

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der	sined undefine						eed undefined undefined											defined un				
	ned un						d unde												Jefill			
	Ele	ctri	cal i	Spe					ocessors			10									(intel)	
	in	e9	10							dun											meetin	
de	В	в	В	В	В	В	В	в	Нех] [В	в	в	В	В	В	В	В	Hex	V.	
ndefined undef	i t 7	i t 6	i t 5	i t 4	i t 3	i t 2	i t	i t 0	nex	undevcc		i t 7	i t 6	i t 5	i t 4	i t 3	1 i i	i t 1	i t 0	Jenex	V _{cc}	mð
nde	1	0	0	0	0	1	1	0	86h	1.8300		1	0	1	0	1	0	0	0	A8h	2.1700	ned u.
Į	1	0	0	0	0	1	1	1	87h	1.8400		1	0	1	0	1	0	0	1	A9h	2.1800	defin
ļ	1	0	0	0	1	0	0	0	88h	1.8500		1	0	1	0	1	0	1	0	AAh	2.1900	
Ĩ	1	0	0	0	1	0	0	1	89h	1.8600	6	1	0	1	0	1	0	1	1	ABh	2.2000	
Į	1	0	0	0	1	0	1	0	8Ah	1.8700		1	0	1	0	1	1	0	0	ACh	2.2100	
6	1	0	0	0	1	0	1	1	8Bh	1.8800		1	0	1	0	1	1	0	1	ADh	2.2200	
-d une	1	0	0	0	1	1	0	0	8Ch	1.8900		1	0	1	0	1	1	1	0	AEh	2.2300	
finet	1	0	0	0	1	1	0	1	8Dh	1.9000		1	0	1	0	1	1	1	1	AFh	2.2400	
undefined unde	1	0	0	0	1	1	1	0	8Eh	1.9100		1	0	1	1	0	0	0	0	B0h	2.2500	ndefined uni
	1	0	0	0	1	1	1	1	8Fh	1.9200		1	0	1	1	0	0	0	1	B1h	2.2600	define
	1	0	0	1	0	0	0	0	90h	1.9300		1	0	1	1	0	0	1	0	B2h	2.2700	
	1	0	0	1	0	0	0	1	91h	1.9400	2	1	0	1	1	0	0	1	1	B3h	2.2800	
	1	0	0	1	0	0	1	0	92h	1.9500	<u>, </u>	1	0	1	1	0	1	0	0	B4h	2.2900	
الح	1	0	0	1	0	0	1	1	93h	1.9600		1	0	1	1	0	1	0	1	B5h	2.3000	
undefined une	1	0	0	1	0	1	0	0	94h	1.9700		1	0	1	1	0	1	1	0	B6h	2.3100	
sineu	1	0	0	1	0	1	0	1	95h	1.9800		1	0	1	1	0	1	1	1	B7h	2.3200	
nder	1	0	0	1	0	1	1	0	96h	1.9900		1	0	1	1	1	0	0	0	B8h	2.3300	indefined un
0.	1	0	0	1	0	1	1	1	97h	2.0000		1	0	1	1	1	0	0	1	B9h	2.3400	etines
	1	0	0	1	1	0	0	0	98h	2.0100		1	0	1	1	1	0	1	0	BAh	2.3500	INOR
	1	0	0	1	1	0	0	1	99h	2.0200		1	0	1	1	1	0	1	1	BBh	2.3600	
	1	0	0	1	1	0	1	0	9Ah	2.0300	20	9	0	1	1	1	1	0	0	BCh	2.3700	
	1	0	0	1	1	0	1	1	9Bh	2.0400		1	0	1	1	1	1	0	1	BDh	2.3800	
74.	1	0	0	1	1	1	0	0	9Ch	2.0500		1	0	1	1	1	1	1	0	BEh	2.3900	
undefined un	1	0	0	1	1	1	0	1	9Dh	2.0600		1	0	1	1	1	1	1	1	BFh	2.4000	
detti	1	0	0	1	1	1	1	0	9Eh	2.0700		1	1	0	0	0	0	0	0	C0h	2.4100	20
Juli	1	0	0	1	1	1	1	1	9Fh	2.0800		1	1	0	0	0	0	0	1	C1h	2.4200	undefined
	1	0	1	0	0	0	0	0	A0h	2.0900		1	1	0	0	0	0	1	0	C2h	2.4300	unde.
	1	0	1	0	0	0	0	1	A1h	2.1000		1	1	0	0	0	0	1	1	C3h	2.4400	
	1	0	1	0	0	0	1	0	A2h	2.1100		1	1	0	0	0	1	0	0	C4h	2.4500	
ļ	1	0	ſ	0	0	0	1	1	A3h	2.1200		1	1	0	0	0	1	0	1	C5h	2.4600	
	1	0	1	0	0	1	0	0	A4h	2.1300		1	1	0	0	0	1	1	0	C6h	2.4700	
ed v	1	0	1	0	0	1	0	1	A5h	2.1400		1	1	0	0	0	1	1	1	C7h	2.4800	
defill	1	0	1	0	0	1	1	0	A6h	2.1500		1	1	0	0	1	0	0	0	C8h	2.4900	2
d undefined u	1	0	1	0	0	1	1	1	A7h	2.1600] [1	1	0	0	1	0	0	1	C9h	2.5000	
							117	ed	0.	continued] [69	01	10.				continued	d undefined
		M	lohil	0 4+	л h С	de	ratio	n In	tal® Cara™	Processor Family, Mo	bilo	Int	ol®	Don	tiun	n® ⊑	Proce		r E 2	mily and M	abila Intol® Coloran®	

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		20	0	N.						atined "
Jefined und	B i t	B i t	B i t	B i t	B i t	B i t	B i t	B i t	Hex	undvcc
	7 1	6 1	5 0	4 0	3 1	2 0	1 1	0	CAh	2.5100
	1	1	0	0	1	0	1	Y	CBh	2.5200
	1	1	0	0	1	1	0	0	CCh	2.5300
	1	1	0	0	À	1	0	1	CDh	2.5400
	1	1	0	0	1	1	1	0	CEh	2.5500
	1	1	0	0	1	1	1	1	CFh	2.5600
	1	1	0	1	0	0	0	0	D0h	2.5700
	1	1	0	1	0	0	0	1	D1h	2.5800
defined un	1	1	0	1	0	0	1	0	D2h	2.5900
	1	1	0	1	0	0	1	1	D3h	2.6000
	1	1	0	1	0	1	0	0	D4h	2.6100
	1	1	0	1	0	1	0	1	D5h	2.6200
	1	1	0	1	0	1	1	0	D6h	2.6300
	1	1	0	1	0	1	1	1	D7h	2.6400
. JI	1	1	0	1	1	0	0	0	D8h	2.6500
ndefined ut	1	1	0	1	1	0	0	1	D9h	2.6600
detin	1	1	0	1	1	0	1	0	DAh	2.6700
	1	1	0	1	1	0	1	1	DBh	2.6800
	1	1	0	1	1	1	0	0	DCh	2.6900
	1	1	0	1	1	1	0	1	DDh	2.7000
	1	1	0	1	1	1	1	0	DEh	2.7100
	1	1	0	1	1	1	1	1	DFh	2.7200
	1	1	1	0	0	0	0	0	E0h	2.7300
	1	1	1	0	0	0	0	1	E1h	2.7400
Indefined	1	1	1	0	0	0	1	0	E2h	2.7500
	1	1	1	0	0	0	1	1	E3h	2.7600
	1	1	1	0	0	1	0	0	E4h	2.7700
	1	1	1	0	0	1	0	1	E5h	2.7800
	1	1	1	0	0	1	1	0	E6h	2.7900
	1	1	1	0	0	1	1	1	E7h	2.8000
	1	a	1	0	1	0	0	0	E8h	2.8100
undefined	1	1	1	0	1	0	0	1	E9h	2.8200
define	1	1	1	0	1	0	1	0	EAh	2.8300
uno	1	1	1	0	1	0	1	1	EBh	2.8400
		•	•	•	•	•	•	•	101	continued

Vcc						e	Ine	,d			undefined un	
				2	7.0,						nder	
								Pro	ces	sors–Elect	trical Specifications	
<i>b.</i> .	<i>0</i> 0										defille	
ined -											d une	
V _{cc}		B i	B i	B	B i	B i	B	B	B	Hex	V _{cc}	
		t 7	t 6	t 5	t 4	t 3	t 2	t 1	t	noc	2.8500 2.8600 2.8700	
0		1	1	1	0	1	1	0	0	ECh	2.8500	
C		1	1	1	0	1	1	0	1	EDh	2.8600	
D		1	1	P	0	1	1	1	0	EEh	2.8700	
0		1	1	1	0	1	1	1	1	EFh	2.8800	
0	YU	1	1	1	1	0	0	0	0	F0h	2.8900	
osine		1	1	1	1	0	0	0	1	F1h	2.9000	
		1	1	1	1	0	0	1	0	F2h	2.9100	
C		1	1	1	1	0	0	1	1	F3h	2.9200 2.9300 2.9400 2.9500	
D		1	1	1	1	0	1	0	0	F4h	2.9300	
D		1	1	1	1	0	1	0	1	F5h	2.9400	
C		1	1	1	1	0	1	1	0	F6h	2.9500	
D		1	1	1	1	0	1	1	1	F7h	2.9600	
0	5	1	1	1	1	1	0	0	0	F8h	2.9700	
o sineu		1	1	1	1	1	0	0	1	F9h	2.9800	
29 ₆		1	1	1	1	1	0	1	0	FAh	2.9900	
D		1	1	1	1	1	0	1	1	FBh	3.0000	
D		1	1	1	1	1	1	0	0	FCh	3.0100	11
D		1	1	1	1	1	1	0	1	FDh	3.0000 3.0100 3.0200 3.0300 3.0400	
D		1	1	1	3	1	1	1	0	FEh	3.0300	
D		1	1	1	1	1	1	1	1	FFh	3.0400	
		n_c									3.0300 3.0400	
											dun.	
o derri										ik.	We.	
0										unde		
D								1.1				JU'
0							.6	S, I,			atine	
D						U.					inde.	
0				117							red	
D		77,									defini	
0											dun	
											tined undefined undefined	

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7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD these signals should not be connected
- RSVD_TP these signals should be routed to a test point
- RSVD_NCTF these signals are non-critical to function and may be left unconnected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Signal Description on page 72 for a pin listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (VSS). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in the following table. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals and selected DDR3L/DDR3L-RS/LPDDR3 and Control Sideband signals have On-Die Termination (ODT) resistors. Some signals do not have ODT and need to be terminated on the board.

Note:

All Control Sideband Asynchronous signals are required to be asserted/de-asserted for at least 10 BCLKs with maximum Trise/Tfall of 6 ns for the processor to recognize the proper signal state. See the DC Specifications section and AC Specifications section.

Table 42. Signal Groups

				CAN Y
ndefined une	Signal Group	Туре	Sig	nals
efine	DDR3L / DDR3L-R	S / LPDDR3 Referen	ce Clocks ²	UI.
	Differential	DDR3L/DDR3L-RS/ LPDDR3 Output	SA_CKP[1:0], SA_CKN[1:0], SE	3_CKP[1:0], SB_CKN[1:0]
	DDR3L / DDR3L-R	S/LPDDR3 Command	l Signals ²	
	Single ended	DDR3L/DDR3L-RS/	DDR3L/DDR3L-RS Mode	LPDDR3 Mode
ned u		LPDDR3 Output	SA_BS2, SB_BS2	SA_CAA5, SB_CAA5
			SA_BS1, SB_BS1	SA_CAB6, SB_CAB6
		defin	SA_BS0, SB_BS0	SA_CAB4, SB_CAB4
		dune	SA_WE#, SB_WE#	SA_CAB2, SB_CAB2
etinec		iner	SA_RAS#, SB_RAS#	SA_CAB3, SB_CAB3
	inde		SA_CAS#, SB_CAS#	SA_CAB1, SB_CAB1
			- In-	continued

ined

den	ned undefine
Intel	
unos	Signal Group
ndefined undefinet u	undefine

ned undefine	sined "	Indefined undefined Proce	ed unoc
Signal Group	Туре	Sig	Inals
	d UI	SA_MA15, SB_MA15	SA_CAA8, SB_CAA8
efined undefin		SA_MA14, SB_MA14	SA_CAA8, SB_CAA8SA_CAA9, SB_CAA9SA_CAB0, SB_CAB0SA_CAA6, SB_CAA6
unoc		SA_MA13, SB_MA13	SA_CAB0, SB_CAB0
		SA_MA12, SB_MA12	SA_CAA6, SB_CAA6
		SA_MA11, SB_MA11	SA_CAA7, SB_CAA7
		SA_MA10, SB_MA10	SA_CAB7, SB_CAB7
	ed	SA_MA9, SB_MA9	SA_CAA1, SB_CAA1
	defill	SA_MA8, SB_MA8	SA_CAA3, SB_CAA3
	d unc	SA_MA7, SB_MA7	SA_CAA4, SB_CAA4
	er	SA_MA6, SB_MA6	SA_CAA2, SB_CAA2
etined undefit DDR3L / DDR3L-R		SA_MA5, SB_MA5	SA_CAA4, SB_CAA4 SA_CAA2, SB_CAA2 SA_CAA0, SB_CAA0 N/A
ed u.		SA_MA4, SB_MA4	N/A
efine		SA_MA3, SB_MA3	N/A
		SA_MA2, SB_MA2	SA_CAB5, SB_CAB5
	e de la companya de la	SA_MA1, SB_MA1	SA_CAB8, SB_CAB8
	18fine	SA_MA0, SB_MA0	SA_CAB9, SB_CAB9
DDR3L / DDR3L-R	5 Control Signals ²		den
Single ended	DDR3L/DDR3L-RS Output	SA_CKE[3:0], SB_CKE[3:0], SA SA_ODT0, SB_ODT0, SM_PG_C	_CS#[1:0], SB_CS#[1:0], NTL1
DDR3L / DDR3L-R	S Data Signals ²	dell	
Single ended	DDR3L/DDR3L-RS Bi-directional	SA_DQ[63:0], SB_DQ[63:0]	
Differential	DDR3L/DDR3L-RS Bi-directional	SA_DQSP[7:0], SA_DQSN[7:0]	, SB_DQSP[7:0], SB_DQSN[7:0]
DDR3L / DDR3L-R	S Reference Voltage	Signals	dull
	DDR3L/DDR3L-RS Output	SM_VREF_CA, SM_VREF_DQ1,	SM_VREF_DQ0
Testability (ITP/XI	DP)		du.
Single ended	GTL Input	PROC_TCK, PROC_TDI, PROC_T	MS, PROC_TRST#
Single ended	GTL	PROC_TDO	
Single ended	GTL	BPM#[7:0]	
Single ended	GTL	PREQ#	nin
Single ended	GTL	PRDY#	inde
Control Sideband	nip.	<u> </u>	ed v
Single ended	GTL Input/Open Drain Output	PROCHOT#	ndefili
Single ended	Asynchronous CMOS Output	IVR_ERROR	led .
Single ended	Open Drain Output	THERMTRIP#	
defines		sined b.	continued

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		d ^{un}	de
Electrical Specifications—Proc	essors	defined une (intel	
Signal Gro Single ended Single ended	ined un	ion of milester	
Signal Gro	оир Туре	Signals	
Single ended	GTL	CATERR#	
Single ended	Asynchronous CMOS Input	RESET#, PROCPWRGD, PWR_DEBUG# , VCCST_PWRGD	
Single ended	Asynchronous Bi- directional	PECI	Sn.
Single ended	GTL Bi-directional	CFG[19:0]	
Voltage Reg	ulator	nde defin.	
Voltage Reg Single ended Single ended Single ended Single ended	VR Enable CMOS Output	VR_EN	
Single ended	CMOS Input	VR_READY	
Single ended	CMOS Input	VIDALERT#	
Single ended	Open Drain Output	VIDSCLK	
Single ended	CMOS I/O	VIDSOUT	
Differential	Analog Output	VCC_SENSE, VSS_SENSE	J
Power / Gro	und / Other	Jefin sinel	1
Single ended	Power	VCC, VDDQ, VCCST	
	Ground	VSS, VSS_NCTF ³	
	No Connect	RSVD, RSVD_NCTF	
	Test Point	RSVD_TP	
	Other	DAISY_CHAIN_NCTF_[ball #]	
Single ended Digital Displ	ay Interface	den	
Differential	DDI Output	DDIB_TXP[3:0], DDIB_TXN[3:0], DDIC_TXP[3:0], DDIC_TXN[3:0]]	20
		72 for signal description details. 3L-RS Channel A and DDR3L/DDR3L-RS Channel B.	

Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

The processor supports Boundary Scan (JTAG) IEEE 1149.1-2001 and IEEE 1149.6-2003 standards. A few of the I/O pins may support only one of those standards.

DC Specifications

undefined un**7.6**

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise. See Signal Description on page 72 for the processor pin listings and signal definitions.

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- The DC specifications for the DDR3L/DDR3L-RS/LPDDR3 signals are listed in the Voltage and Current Specifications section.
- undefined undefined unde The Voltage and Current Specifications section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

Voltage and Current Specifications

Table 43. Processor Core Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ¹	
Operating Voltage	Voltage Range for Processor Active Operating Mode	All	1.6	definer	1.84	V	1, 2, 7	undefine
Idle Voltage	Voltage Range for Processor Idle Mode (Package C6/C7)	All	1.5	_	1.65	V	1, 2, 7	unos
		U- Processors 28W	_	-	40	ed un	9e.	
I _{CCMAX}	Maximum Processor Core I _{CC}	U- Processors 15W	_	_	32	A	4, 6, 7	
aneu	Jetti.	Y-Processors 11.5W (6W SDP / 4.5W SDP)	-0 1	ndefine	25			undefine
TO	Voltaga Talaranga	PS0, PS1	in-	_	±20	m)/	6.00	
IULVCC		PS2, PS3	-	—	±20	IIIV	0, 8	
	2	PS0	_	—	±15	du		
Pinnlo	Ripple Tolerance	PS1	-	—	±15		6 0	
Ripple		PS2	-	—	+50/-15	111V	0,0	
		PS3		-	+60/-15			
R_DC_LL	Loadline slope within the VR regulation loop capability	_	ed	- 2.0	_	mV	_	d undefin
R_AC_LL	Loadline slope in response to dynamic load increase events	- und	-	- 7.0	_	mΩ	undefine	
					. /	cor	ntinued	
	adefined un	stined under						. o. al
defined	1.	sined under						ed undefil
	Operating Voltage Idle Voltage Iccmax TOL _{VCC} Ripple R_DC_LL R_AC_LL	Operating VoltageVoltage Range for Processor Active Operating ModeIdle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)ICCMAXMaximum Processor Core ICCTOL_VCCVoltage ToleranceRippleRipple ToleranceR_DC_LLLoadline slope within the VR regulation loop capabilityR_AC_LLLoadline slope in response to dynamic load increase events	Operating VoltageVoltage Range for Processor Active Operating ModeAllIdle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)AllIVoltage Range for Processor Idle Mode (Package C6/C7)AllIMaximum Processor Core IccU- Processors 28WIMaximum Processor Core IccU- Processors 15WTOLvccVoltage TolerancePS0, PS1 PS2, PS3TOLvccLoadline slope within the VR regulation loop capabilityPS0R_DC_LLLoadline slope in response to dynamic load increase events-R_AC_LLLoadline slope in response to dynamic load increase events-	Operating VoltageVoltage Range for Processor Active Operating ModeAll1.6Idle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)All1.5Idle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)All1.5IccmaxMaximum Processor Core IccU- Processors 15W-Voltage ToleranceU- Processors 1.5W-TOLvccVoltage TolerancePS0, PS1-RippleNotage TolerancePS2, PS3-RippleLoadline slope within the VR regulation loop capabilityR_AC_LLLoadline slope in response to dynamic load increase eventsULoadline slope in response to dynamic load increase events	Operating VoltageVoltage Range for Processor Active Operating ModeAll1.6Idle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)All1.5Idle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)All1.5IccmaxMaximum Processor Core IccU- Processors 11.5WVoltage ToleranceV- Processors 11.5W (6W SDP / 4.5W SDP)TOLyccVoltage TolerancePS0, PS1RippleRipple TolerancePS0PS1PS3R_DC_LLLoadline slope within the VR response to dynamic load increase events2.0R_AC_LLLoadline slope in response to dynamic load increase events	Operating VoltageVoltage Range for Processor Active Operating ModeAll1.61.84Idle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)All1.51.65Idle VoltageVoltage Range for Processor Idle Mode (Package C6/C7)All1.51.65IccmaxMaximum Processor Core Icc U^{-} Processors 15W40Voltage Tolerance U^{-} Processors 15W32TOLvccVoltage TolerancePS0, PS1±20PS2, PS3±20PS2, PS3±15PS1±15PS3±15PS2±15PS3±60/-15R_DC_LLLoadline slope dynamic load increase events2.0R_AC_LLLoadline slope in response to dynamic load increase events7.0	$\begin{array}{ c c c c c c } \hline Voltage Range for \\Voltage \\ \hline Operating Mode \\ \hline Operating Mode \\ \hline Voltage Range for \\Processor Active \\Operating Mode \\ \hline Idle Voltage \\ \hline Voltage Range for \\Processor Idle Mode \\(Package C6/C7) \\ \hline Hall \\ \hline Idle Voltage \\ \hline Voltage Range for \\Processor Idle Mode \\(Package C6/C7) \\ \hline Processor \\I $	ICCMAX Maximum Processor Core ICC U- Processors 28W 40 A 4, 6, 7 ICCMAX Maximum Processor Core ICC $\frac{U}{Processors}$ 15W 40 A 4, 6, 7 Processors Core ICC $\frac{U}{Processors}$ 11.5W (6W SDP / 4.5W SDP / 4.5W SDP) 32 A 4, 6, 7 TOLvcc Voltage Tolerance PS0, PS1 25 mV 6, 8 Ripple PS0, PS1 ±20 mV 6, 8 Ripple Tolerance PS0 ±15 mV 6, 8 PS1 ±15 mV 6, 8 6, 8 Ripple Tolerance PS1 ±15 mV 6, 8 Ripple Tolerance PS3 ±60/-15 mV 6, 8 R_DC_LL Loadline slope in response to increase to increase events mV

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Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ¹
T_OVS_Max	Max Overshoot time	_	_	- 0	500	μs	-
v_ovs	Max Overshoot	-	-	dine .	200	mV	_

Notes: 1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data.

- 2. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low-Power States).
- 3. The voltage specification requirements are measured across VCC SENSE and VSS SENSE lands at the socket with a 20 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 ined undefined un $M\Omega$ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
- 4. Processor core VR to be designed to electrically support this current.
- 5. Processor core VR to be designed to thermally support this current indefinitely.
- 6. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
- Long term reliability cannot be assured in conditions above or below Maximum/Minimum 7. functional limits.
- 8. PSx refers to the voltage regulator power state as set by the SVID protocol.

Table 44. Memory Controller (V_{DDO}) Supply DC Voltage and Current Specifications

Parameter	Min	Тур	Max	Unit	Note	
Processor I/O supply voltage for DDR3L/DDR3L- RS	_	1.35	unoc	V	2, 3	d un
Processor I/O supply voltage for LPDDR3	7	1.20	_	V	2, 3	defines
VDDQ Tolerance (AC+DC)	-5	_	5	%	2, 3	ULL
Max Current for V _{DDQ} Rail (DDR3L/DDR3L-RS)	-	_	1.4	А	defines	
Max Current for V _{DDQ} Rail (LPDDR3)	_	_	1.1	A UI	1	
	Processor I/O supply voltage for DDR3L/DDR3L- RS Processor I/O supply voltage for LPDDR3 VDDQ Tolerance (AC+DC) Max Current for V _{DDQ} Rail (DDR3L/DDR3L-RS) Max Current for V _{DDQ} Rail	Processor I/O supply voltage for DDR3L/DDR3L- RS - Processor I/O supply voltage for LPDDR3 - VDDQ Tolerance (AC+DC) -5 Max Current for V _{DDQ} Rail (DDR3L/DDR3L-RS) - Max Current for V _{DDQ} Rail -	Processor I/O supply voltage for DDR3L/DDR3L- RS - 1.35 Processor I/O supply voltage for LPDDR3 - 1.20 VDDQ Tolerance (AC+DC) -5 - Max Current for V _{DDQ} Rail (DDR3L/DDR3L-RS) - -	Processor I/O supply voltage for DDR3L/DDR3L- RS - 1.35 - Processor I/O supply voltage for LPDDR3 - 1.20 - VDDQ Tolerance (AC+DC) -5 - 5 Max Current for V _{DDQ} Rail (DDR3L/DDR3L-RS) - - 1.4	Processor I/O supply voltage for DDR3L/DDR3L- RS - 1.35 - V Processor I/O supply voltage for LPDDR3 - 1.20 - V VDDQ Tolerance (AC+DC) -5 - 5 % Max Current for V _{DDQ} Rail (DDR3L/DDR3L-RS) - - 1.4 A	Processor I/O supply voltage for DDR3L/DDR3L- RS-1.35-V2, 3Processor I/O supply voltage for LPDDR3-1.20-V2, 3VDDQ Tolerance (AC+DC)-5-5%2, 3Max Current for VDDQ Rail (DDR3L/DDR3L-RS)1.4A1

Notes: 1. The current supplied to the DIMM modules is not included in this specification.

undefined undefined und Vcc Sustain (Vcc_{ST}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Тур	Max	Units	Notes	unos
/cc _{ST}	Processor Vcc Sustain supply voltage	- 5%	1.05	+ 5%	V	1etinec	
CC _{MAX_VccST}	Maximum Current for Vcc _{ST}	0 0 -	_	100	mA	nos	
	d under.						
	definec			tined u.			
	TUC						efin

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ned undefined undefined DDR3L / DDR3L-RS Signal Group DC Specifications

2 ^{d lu}	DDR3L / DDR3L Symbol V _{IL}	RS Signal Group Parameter				d unde		
d un ^{de} Table 46.	Symbol		DC Specifi					
^y d ^u	Symbol		-	ications				
-	VIL	raianietei	Min	Тур	Max	Units	Notes ¹	
_		Input Low Voltage	_	V _{DDQ} /2	0.43*V _{DDQ}	V	2, 4, 11	
	VIH INDE	Input High Voltage	0.57*V _{DDQ}	V _{DDQ} /2	-	V	3, 11	ndefined
_	VIL	Input Low Voltage (SM_DRAMPWROK)	-ed u	· -	0.15*V _{DDQ}	v		Inder
d unde	V _{IH}	Input High Voltage (SM_DRAMPWROK)	0.45*V _{DDQ}	_	1.0	v	10, 12	
d unde	R _{ON_UP(DQ)}	DDR3L/DDR3L-RS Data Buffer pull-up Resistance	20	26	32	o nuc	5, 11	
	R _{ON_DN(DQ)}	DDR3L/DDR3L-RS Data Buffer pull-down Resistance	20	26	32	Ω	5, 11	
	KODT(DQ)	DDR3L/DDR3L-RS On- die termination equivalent resistance for data signals	38	und ^{efin} 50	62	Ω	11	undefine
Juno	V _{odt(dc)}	DDR3L/DDR3L-RS On- die termination DC working point (driver set to receive mode)	0.45*V _{DDQ}	0.5*V _{DDQ}	0.55*V _{DDQ}	vun	defineu	
	R _{on_up(ck)}	DDR3L/DDR3L-RS Clock Buffer pull-up Resistance	20	26	32	Ω	5, 11, 13	
	Ron_dn(ck)	DDR3L/DDR3L-RS Clock Buffer pull-down Resistance	20	26	32	Ω	5, 11, 13	undefin
	R _{ON_UP} (cmd)	DDR3L/DDR3L-RS Command Buffer pull- up Resistance	15 ed	20	25	Ω	5, 11, 13	unde.
9 nu	R _{ON_DN} (cmd)	DDR3L/DDR3L-RS Command Buffer pull- down Resistance	15	20	25	Ω	5, 11, 13	
	R _{ON_UP(CTL)}	DDR3L/DDR3L-RS Control Buffer pull-up Resistance	19	25	31 defi	Ω	5, 11, 13	
	Ron_dn(ctl)	DDR3L/DDR3L-RS Control Buffer pull-down Resistance	19	25	ed 31	Ω	5, 11, 13	d undefil
	Ron_up(sm_pg_cntl1)	System Memory Power Gate Control Buffer Pull-Up Resistance	40 61110	80	130	Ω	13	d under
20 1	Ron_dn(sm_pg_cntl1)	System Memory Power Gate Control Buffer Pull-Down Resistance	40 40	80	130	Ω	13	
ned ut	ILI	Input Leakage Current (DQ, CK) 0V 0.2*V _{DDQ} 0.8*V _{DDQ}	-	-	0.7	mA	-	
	June			uge,		con	tinued	ref
	ndefiner		1efin	ed u.				ed undef
oile 4th Generat	ion Intel [®] Core [™] Proc	essor Family, Mobile Intel®	[®] Pentium [®] Pr	rocessor Fami	ly, and Mobile I	ntel [®] Cele	eron®	
ssor Family heet – Volum	e 1 of 2				-	6	July 2014	
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	ed undern			defined				
Electrical Spec	cifications—Processor	s ed unde	ined.			(in	tel)	
under	Symbol	Parameter	Min	Тур	Max	Units	Notes ¹	
	Iu undefine	Input Leakage Current (CMD, CTL) 0V 0.2*V _{DDQ} 0.8*V _{DDQ}	-	defined	1.0	mA	-	defined und
	SM_RCOMP0	Command COMP Resistance	198	200	202	Ω	8 11	
dune	SM_RCOMP1	Data COMP Resistance	118.8	120	121.2	Ω	8	
sinet	SM_RCOMP2	ODT COMP Resistance	99	100	101	Ω	8	
undefined under	 V_{IL} is def logical lo V_{IH} is de logical hi V_{IH} and V with the 	therwise noted, all specificat fined as the maximum volta- w value. fined as the minimum voltag gh value. V _{OH} may experience excursio signal quality specifications.	ge level at a r ge level at a r ons above V _{DI}	receiving agen	t that will be in t that will be in	nterpreted	as a as a	lefined un

- 5. This is the pull up/down driver resistance.
- 6. R_{TERM} is the termination on the DIMM and in not controlled by the processor.
- 7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
- 8. SM_RCOMPx resistance must be provided on the system board with 1% resistors. SM_RCOMPx resistors are to V_{SS}.
- 9. SM_DRAMPWROK rise and fall time must be < 50 ns measured between V_{DDO} *0.15 and V_{DDO} *0.47.
- 10.SM_VREF is defined as $V_{DDO}/2$.
- 11. Maximum-minimum range is correct; however, center point is subject to change during MRC boot training.
- 12. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
- 13. The MRC during boot training might optimize R_{ON} outside the range specified.

Table 47. LPDDR3 Signal Group DC Specifications Jundefined undefined une

undefinec	11.Max boo 12.Pro	ximum-minimum range is corr bt training. Incessor may be damaged if V _{IH} e MRC during boot training mig	exceeds the ma	aximum voltage	for extended pe	5	ЧRC	fined un
Table 47.	LPDDR3 Si	gnal Group DC Specif	ications	UUr.				under.
, unc	Symbol	Parameter	Min	Тур.	Max	Unit	Note	
sineo -	V _{IL}	Input Low Voltage	7// -	V _{DDQ} /2	0.43*V _{DDQ}	V	2, 4, 12	
den	V _{IH}	Input High Voltage	0.57*V _{DDQ}	V _{DDQ} /2		О v	3, 11	
undefined undefined un	V _{IL}	Input Low Voltage (SM_DRAMPWROK)	—	_	0.15*V _{DDQ}	V	_	
	V _{IH}	Input High Voltage (SM_DRAMPWROK)	0.45*V _{DDQ}	-tine	1.0*V _{DDQ}	v	10, 12	ned u
2	R _{ON_UP(DQ)}	LPDDR3 Data Buffer pull- up Resistance	30	40	50	Ω	5, 11	indefill
un.	R _{ON_DN(DQ)}	LPDDR3 Data Buffer pull- down Resistance	30	40	50	Ω	5, 11	
adefined	R _{ODT(DQ)}	LPDDR3 On-die termination equivalent resistance for data signals	150	200	250	Ω	11	
d undefined undefined un	V _{ODT(DC)}	LPDDR3 On-die termination DC working point (driver set to receive mode)	0.45*V _{DDQ}	0.5*V _{DDQ}	0.55*V _{DDQ}	v	11	2,
ed un	R _{ON_UP(CK)}	LPDDR3 Clock Buffer pull- up Resistance	30	40	50	Ω	5, 11	definer
	cine-			9		con	tinued	un.
	nde.		define				stine	

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(intel.	Suc		etineo	Proce	ssors—Electri	ical Spe		
afine un		thed u	nde			unde		
Inde	Symbol	Parameter	Min	Тур.	Max	Unit	Note	
undefine	R _{ON_DN(CK)}	LPDDR3 Clock Buffer pull- down Resistance	30	40	JIN050	Ω	5, 11	ndefined un
	R _{ON_UP(CMD)}	LPDDR3 Command Buffer pull-up Resistance	19	25	31	Ω	5, 11	fined
Ro	R _{ON_DN(CMD)}	LPDDR3 Command Buffer pull-down Resistance	19	25	31	Ω	5, 11	nde.
a undefined und	R _{ON_UP(CTL)}	LPDDR3 Control Buffer pull-up Resistance	19	25	31	Ω	5, 11	
define	R _{ON_DN(CTL)}	LPDDR3 Control Buffer pull-down Resistance	19	25	31	Ω	5, 11	
	R _{ON_UP(RST)}	LPDDR3 Reset Buffer pull- up Resistance	40	80	130	Ω	_	
Ron	R _{ON_DN(RST)}	LPDDR3 Reset Buffer pull- up Resistance	40	80	130	Ω	_	ed u
ed undefined und	Juined un	Input Leakage Current (DQ, CK) OV 0.2* V _{DDQ} 0.8*V _{DDQ}	ndefined	under	0.4	mA	efined	undefined
definec	ILI	Input Leakage Current (CMD,CTL) 0V 0.2*V _{DDQ} 0.8*V _{DDQ}	-	_	0.6	mA	_	
	SM_RCOMP0	ODT COMP Resistance	198	200	202	Ω	8	6
	SM_RCOMP1	Data COMP Resistance	118.8	120	121.2	Ω	8	efine
	SM_RCOMP2	Command COMP Resistance	99	100	101	Ω	8	undefined

2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.

- 3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
- 5. This is the pull up/down driver resistance.
- 6. RTERM is the termination on the DIMM and in not controlled by the processor.
- 7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
- 8. SM_RCOMPx resistance must be provided on the system board with 1% resistors. SM_RCOMPx resistors are to V_{SS}.
- 9. SM_DRAMPWROK must have a maximum of 15 ns rise or fall time over V_{DDQ} * 0.30 ±100 mV and the edge must be monotonic.
- 10.SM_VREF is defined as $V_{DDQ}/2$
- 11. Maximum-minimum range is correct; however, center point is subject to change during MRC boot training.
- 12. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.

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Table 48.

led undefined undefine **Digital Display Interface Group DC Specifications**

VIL HPD Input Low Vol VIH HPD Input High V	5	- 2.25	9~-	0.8	V	
	oltage	2.25				
			-	3.6	V	sineu
Vaux(Tx) Aux peak-to-peak device	voltage at transmitting	0.39	_	1.38	V UY	ger.
Vaux(Rx) Aux peak-to-peak device	voltage at receiving	0.32	_	1.36	stinv	

embedded DisplayPort* (eDP*) Group DC Specifications

	Vaux(Tx)	Aux peak-to-peak voltage at transmitting device	0.39	_	1.38	v	lge.
dunde	Vaux(Rx)	Aux peak-to-peak voltage at receiving device	0.32	_	1.36	stinv	
	embedded	DisplayPort* (eDP*) Group DC	Specifica	ations	ed une		
d une	Symbol	Parameter	Min	Тур	Max	Units	
whited une	V _{OL}	eDP_DISP_UTIL Output Low Voltage	0.1*V _{CC}	2 UD	-	V	.nd
inde.	V _{OH}	eDP_DISP_UTIL Output High Voltage	0.9*V _{CC}		-	V	ed un
0.	R _{UP}	eDP_DISP_UTIL Internal pull-up	100	_	-	Ω	18fine
	R _{DOWN}	eDP_DISP_UTIL Internal pull-down	100	_	-	Ω	nor
d unde	Vaux(Tx)	Aux peak-to-peak voltage at transmitting device	0.39	-	1.38	etilveo	
med undefined und	Vaux(Rx)	Aux peak-to-peak voltage at receiving device	0.32		1.36	V	
d unc	eDP_RCOMP	COMP Resistance	24.75	25	25.25	Ω	
sineu	Note: 1. COMF	Presistance is to VCOMP_OUT.		unos			

undefined undefined unde **CMOS Signal Group DC Specifications**

		Note: 1. COMF	P resistance is to VCOMP_C	DUT.	uno			
Table 50.		CMOS Signal Group DC Specifications						ined
		Symbol	Parameter	Min	Max	Units	Notes ¹	dein
	\$	V _{IL}	Input Low Voltage	cine ⁰	Vcc _{ST} * 0.3	V	2	ULL
	, un ^c	VIH	Input High Voltage	Vcc _{ST} * 0.7	_	V	2, 4	
		V _{OL}	Output Low Voltage	1 UT -	Vcc _{ST} * 0.1	V	2	
		V _{OH}	Output High Voltage	Vcc _{ST} * 0.9	_	eov	2, 4	
0		R _{ON}	Buffer on Resistance	23	73	Ω	-	
defined		ILI	Input Leakage Current	_	±150	μA	3	
THE		2. The	ss otherwise noted, all spe Vcc _{ST} referred to in these	specifications refers to ins	tantaneous VCCIO_OL			define

- 2. The Vcc_ST referred to in these specifications refers to instantaneous $\mathsf{VCCIO}_\mathsf{OUT}.$
- 3. For VIN between ``0'' V and Vcc_{ST}. Measured when the driver is tri-stated.
- 4. V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers must comply with the signal quality specifications.

Table 51.

GTL Signal Group and Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes ¹	
V _{IL}	Input Low Voltage (TAP, except PROC_TCK, PROC_TRST#)	-	Vcc _{ST} * 0.6	V	2	
V _{IH}	Input High Voltage (TAP, except PROC_TCK, PROC_TRST#)	Vcc _{ST} * 0.72	finec -	v	2, 4	siner
6-	0.		1	con	tinued	76,
defines						dunc
					113	

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Processors—Electrical Specifications

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(intel	ned und			Processors—Electr	ical Spe	cifications	no.
		red unde.			unde	fill	
unde	Symbol	Parameter	Min	Max	Units	Notes ¹	
afined undefine	V _{IL}	Input Low Voltage (PROC_TCK, PROC_TRST#)	_	Vcc _{ST} * 0.3	V	2	
	V _{IH}	Input High Voltage (PROC_TCK, PROC_TRST#)	Vcc _{ST} * 0.7	_	V	2, 4	sined
	V _{HYSTERESIS}	Hysteresis Voltage	Vcc _{sT} * 0.2	_	V	-	inde.
	R _{ON}	Buffer on Resistance (TDO)	ine 7	17	Ω	65	
dun	V _{IL}	Input Low Voltage (other GTL)	_	Vcc _{ST} * 0.6	V	2	
stines	V _{IH}	Input High Voltage (other GTL)	Vcc _{ST} * 0.72	_	V	2, 4	
tined undefined und	R _{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	_	
	R _{ON}	Buffer on Resistance (other GTL)	12	28	Ω	_	
	ILI	Input Leakage Current	_	±150	μA	3	

- 2. The Vcc_{ST} referred to in these specifications refers to instantaneous Vcc_{ST} .
- 3. For VIN between 0 V and Vcc_{ST}. Measured when the driver is tri-stated.
- 4. V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers must comply with the signal quality specifications.

Table 52.

VR Enable CMOS Signal Group DC Specification

Symbol	Parameter	Min	Max	Units	Notes	
R _{ON}	Buffer on Resistance	30	70	Ω		
V _{HYSTERESIS}	Hysteresis Voltage	0.15* Vcc _{ST}	9 u	v		, (j
VCOMP_OU	T and VCCIO_TERM	under				define
Symbol	Parameter	СТур	Max	Units	Notes	Juli
0						1

Table 53.

VCOMP_OUT and VCCIO_TERM

Symbol	Parameter	Тур	Max	Units	Notes
VCOMP_OUT	Termination Voltage	1.0	_	V	1
VCCIO_TERM	Termination Voltage	1.0	_	V	2
Notes: 1. VCOM	P OUT may only be used to connect eDP I	RCOMP.		00	

2. Internal processor power for signal termination.

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Platform Environment Control Interface (PECI) DC Characteristics

The PECI interface operates at a nominal voltage set by Vcc_{ST}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc_{ST} interface supply.

Vcc_{ST} nominal levels will vary between processor families. All PECI devices will operate at the Vcc_{ST} level determined by the processor installed in the system.

Table 54.

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Platform Environment Control Interface (PECI) DC Electrical Limits

Symbol	Definition and Conditions	Min	Max	Units	Notes ¹
R _{up}	Internal pull up resistance	15	45	Ω	3
Vin	Input Voltage Range	-0.15	Vcc _{ST}	V	-
		6		со	ntinued

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	ed unde.		4 undefi	in-			defined
Electrical Specin	fications—Process	sors			(ir	tel	
unde	Symbol	Definition and Conditions	Min	Max	Units	Notes ¹	
	V _{hysteresis}	Hysteresis	0.1 * Vcc _{ST}	N/A	V	_	
	V _n	Negative-Edge Threshold Voltage	0.275 * Vcc _{ST}	0.500 * Vcc _{ST}	V	_	ined un
	Vp	Positive-Edge Threshold Voltage	0.550 * Vcc _{ST}	0.725 * Vcc _{ST}	V		deth
	C _{bus}	Bus Capacitance per Node	N/A	10	pF	ine ^O	
d un.	C _{pad}	Pad Capacitance	0.7	1.8	pF	- "'	
efine	Ileak000	leakage current at 0 V	-	0.6	mA	-	
Idefined undefined unde	Ileak025	leakage current at 0.25* Vcc _{ST}	_	0.4	mA	_	
define	Ileak050	leakage current at 0.50* Vcc _{ST}	_	0.2	mA	_	du
2	Ileak075	leakage current at 0.75* Vcc _{ST}	-unde	0.13	mA	_	definec
	Ileak100	leakage current at Vcc _{ST}	<u>d</u>	0.10	mA	1	n-

Notes: 1. Vcc_{ST} supplies the PECI interface. PECI behavior does not affect Vcc_{ST} minimum / maximum specifications.

The leakage specification applies to powered devices on the PECI bus. 2.

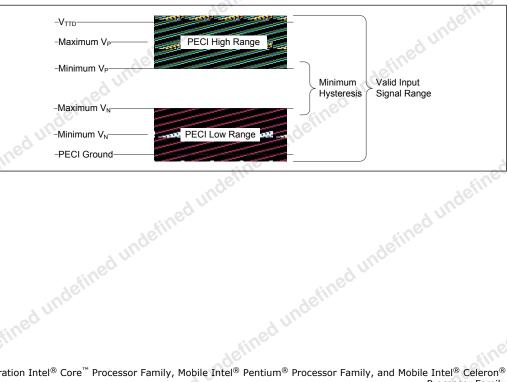
3. The PECI buffer internal pull-up resistance measured at 0.75* Vccst.

undefined undefined ur **Input Device Hysteresis**

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.

Figure 13. **Input Device Hysteresis**

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8.1

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Package Specifications 8.0

Package Mechanical Attributes

The U-Processor Line and Y-Processor Line use a Flip Chip technology and Multi-Chip package (MCP) available in a Ball Grid Array (BGA) package. The following table provides an overview of the mechanical attributes of this package.

Table 55. **Package Mechanical Attributes**

Package Me	chanical Attributes	med u.	d un
uno	Parameter	U-Processor Line and Y-Processor Line	sines
ined	Package Type	Flip Chip Ball Grid Array	
Package Technology	Interconnect	Ball Grid Array (BGA)	
	Lead Free	Yes	
	Halogenated Flame Retardant Free	Yes	
	Solder Ball Composition	SAC 405	
	Ball/Pin Count	1168	
Package	Grid Array Pattern	Balls Anywhere	ن _م
Configuration	Land Side Capacitors	Yes	sineo
	Die Side Capacitors	No	dell
lefine	Die Configuration	Multi-Chip Package (MCP) / 2 dies	Ult
Package	Nominal Package Size	40.0 mm x 24.0 mm	
Dimensions	Min Ball/Pin pitch	0.65 mm	

8.2

Table 56.

Package Loading Specifications

Package Loading Specifications

Maximum Static Normal Load	Limit	Notes
Y-Processor Line	22 N (15 lbf)	1, 2, 3
U-Processor Line/ Y-Processor Line BGA	67 N (15 lbf)	1, 2, 3

Notes: 1. The thermal solution attach mechanism must not induce continuous stress to the package. It may only apply a uniform load to the die to maintain a thermal interface.

- 2. This specification applies to the uniform compressive load in the direction perpendicular to the dies' top surface.
- 3. This specification is based on limited testing for design characterization.

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Package Specifications—Processors



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Red undefined undefined Package Storage Specifications

Table 57. **Package Storage Specifications**

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d uno 8.3	Package Stor	age Specifications	efine			
Table 57.	Package Storage	Specifications				
	Parameter	Description	Min	Max	Notes	
	TABSOLUTE STORAGE	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time.	-25 °C	125 °C	1, 2, 3	defilit
ined un	T _{SUSTAINED} STORAGE	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5	
undefin	RH _{SUSTAINED} STORAGE	The maximum device storage relative humidity for a sustained period of time.	60% @	24 °C	5, 6	
	TIMESUSTAINED STORAGE	A prolonged or extended period of time: typically associated with customer shelf life.	0 months	6 months	6	

- 2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified by applicable JEDEC standards.
- 3. T_{ABSOLUTE STORAGE} applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
- 4. Intel-branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
- 5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
- The undefined un

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Processors Processor Ball and Signal Information

Processor Ball and Signal Information 9.0

This chapter provides the processor Ball information.

Table 58.

Ball List by Signal Name f

Table 58.	Ball List by Sig	nal Name
defill	Signal Name	Ball #
lable 58.	ACPRESENT / GPIO31	AJ8 und
	APWROK	AB5
	BATLOW# / GPIO72	AN4
	BMBUSY# / GPIO76	P1
a un	BPM#0	J60
led undefined un	BPM#1	H60
nder	BPM#2	H61
du.	BPM#3	H62
	BPM#4	К59
	BPM#5	H63
	BPM#6	К60
	BPM#7	J61
	CATERR#	K61
	CFG[0]	AC60
	CFG[1]	AC62
UI	CFG[10]	V60
d undefined u	CFG[11]	U60
	CFG[12]	Т63
	CFG[13]	Т62
	CFG[14]	T61
	CFG[15]	Т60
ed	CFG[16]	AA62
defill	CFG[17]	AA61
dune	CFG[18]	U63
	CFG[19]	U62
ed undefined	CFG[2]	AC63
	CFG[3]	AA63
	ndefineu ca	ontinued

Signal Name	Ball #
CFG[4]	AA60
CFG[5]	Y62
CFG[6]	Y61
CFG[7]	Y60
CFG[8]	V62
CFG[9]	V61
CFG_RCOMP	V63
CL_CLK	AF2
CL_DATA	AD2
CL_RST#	AF4
CLKOUT_ITPXDP_N	B35
CLKOUT_ITPXDP_P	A35
CLKOUT_LPC_0	AN15
CLKOUT_LPC_1	AP15
CLKOUT_PCIE_N0	C43
CLKOUT_PCIE_N1	B41
CLKOUT_PCIE_N2	C41
CLKOUT_PCIE_N3	B38
CLKOUT_PCIE_N4	A39
CLKOUT_PCIE_N5	B37
CLKOUT_PCIE_P0	C42
CLKOUT_PCIE_P1	A41
CLKOUT_PCIE_P2	B42
CLKOUT_PCIE_P3	C37
CLKOUT_PCIE_P4	B39
CLKOUT_PCIE_P5	A37
CLKRUN# / GPIO32	V5
CC	ontinued.
	nedun

Signal Name	Ball #	
DAISY_CHAIN_NCT F_A3	A3	1
DAISY_CHAIN_NCT F_A4	A4	und
DAISY_CHAIN_NCT F_A60	A60	60.
DAISY_CHAIN_NCT F_A61	A61	U.
DAISY_CHAIN_NCT F_A62	A62	
DAISY_CHAIN_NCT F_AV1	AV1	
DAISY_CHAIN_NCT F_AW1	AW1	1
DAISY_CHAIN_NCT F_AW2	AW2	Jun
DAISY_CHAIN_NCT F_AW3	AW3	June
DAISY_CHAIN_NCT F_AW61	AW61	1
DAISY_CHAIN_NCT F_AW62	AW62	1
DAISY_CHAIN_NCT F_AW63	AW63	1
DAISY_CHAIN_NCT F_AY2	AY2]
DAISY_CHAIN_NCT F_AY3	AY3	d un
DAISY_CHAIN_NCT F_AY60	AY60	0
DAISY_CHAIN_NCT F_AY61	AY61]
DAISY_CHAIN_NCT F_AY62	AY62	
DAISY_CHAIN_NCT F_B2	B2	led U
co	ntinued	1

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Processor Ball and Signal Information—Processors



	Signal Name	Ball #
defin	DAISY_CHAIN_NCT F_B3	B3
	DAISY_CHAIN_NCT F_B61	B61
	DAISY_CHAIN_NCT F_B62	B62
defined undef	DAISY_CHAIN_NCT F_B63	B63
lefine	DAISY_CHAIN_NCT F_C1	C1
	DAISY_CHAIN_NCT F_C2	C2
	DCPRTC	AE7
	DCPSUS1	AD10
		AD8
26	DCPSUS2	AH13
4 UNC	DCPSUS3	J13
	DCPSUS4	AB8
)e	DCPSUSBYP	AG19
defined unde	DCPSUSBYP	AG20
	DDI1_TXN[0]	C54
	DDI1_TXN[1]	B58
	DDI1_TXN[2]	B55
	DDI1_TXN[3]	A57
, uno	DDI1_TXP[0]	C55
	DDI1_TXP[1]	C58
defined und	DDI1_TXP[2]	A55
	DDI1_TXP[3]	B57
	DDI2_TXN[0]	C51
	DDI2_TXN[1]	C53
	DDI2_TXN[2]	C49
	DDI2_TXN[3]	A53
71.	DDI2_TXP[0]	C50
redv	DDI2_TXP[1]	B54
defin	DDI2_TXP[2]	B50
	DDI2_TXP[3]	B53
ndefined un	DDPB_AUXN	C5
	DDPB_AUXP	В5
	DDPB_CTRLCLK	B9
	defined c	ontinued

s undefined un	define	
d ul		
s letine		
unac		
Signal Name	Ball #	9
DDPB_CTRLDATA	C9	GPI
DDPB_HPD	C8	GPI
DDPC_AUXN	B6	GPI
DDPC_AUXP	A6	GPI
DDPC_CTRLCLK	D9	GPI
DDPC_CTRLDATA	D11	GPI
DDPC_HPD	A8	GPI
DEVSLP0 / GPIO33	P2	GPI
DEVSLP1 / GPIO38	L2	GPI
DEVSLP2 / GPIO39	N5	GPI
DIFFCLK_BIASREF	C26	GPI
DPWROK	AV5	GPI
DSWVRMEN	AW7	GPI
EDP_AUXN	A45	GPI
EDP_AUXP	B45	GPI
eDP_BKLCTL	B8	GPI
eDP_BKLEN	A9	GPI
EDP_DISP_UTIL	A43	GPI
EDP_HPD	D6	GPI
EDP_RCOMP	D20	GPI
EDP_TXN0	C45	GPI
EDP TXN1	A47	GPI
EDP_TXN2	C47	GSI
EDP_TXN3	A49	GPI
EDP TXP0	B46	GSF GPI
EDP_TXP1	B47	GSF
EDP_TXP2	C46	GPI
EDP_TXP3	B49	GSF GPI
eDP_VDDEN	C6	GSI
GPIO10	AM2	GPI
GPIO13	AT3	GSF GPI
GPIO14	AH4	
GPIO15	AD6	GSF GPI
GPIO16	Y1	GSF
GPIO17	ТЗ	GPI
GPIO24	AD5	HD/ I2S
	ontinued	

nal Name Ball # defined unde AM4 AN3 AN5 AD7 AK4 AG5 AG3 AB6 ndefined und U4 8 Y3 P3 R5 L1 L4 3 L3 U7 AG6 undefined un AP1 AL4 8 AT5 ۵ AU2 AM3 MOSI / K2 CLK / L6 undefined u CS# / R6 MISO / N6 L8 MOSI / CLK / L5 R7 CS# / MISO / N7 ed undefined AW8 CLK / SCLK continued...

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led under	Signal Name	Ball #
	HDA_DOCK_EN# / I2S1_TXD	AW10
	HDA_DOCK_RST# / I2S1_SFRM	AV10
	HDA_RST# / I2S_MCLK	AU8
defined und	HDA_SDI0 / I2S0_RXD	AY10
Jefines	HDA_SDI1 / I2S1_RXD	AU12
	HDA_SDO / I2S0_TXD	AU11
	HDA_SYNC / I2S0_SFRM	AV11
	HSIOPC / GPIO71	Y2
	I2C0_SCL / GPIO5	F3
ndefined und	I2C0_SDA / GPIO4	F2
ed u	I2C1_SCL / GPIO7	F1
defin	I2C1_SDA / GPIO6	G4
, O	I2S1_SCLK	AY8
	INTRUDER#	AU6
	INTVRMEN	AV7
	JTAGX	AE63
	LAD0	AU14
	LAD1	AW12
ed un	LAD2	AY12
Jefine -	LAD3	AW11
defined un	LAN_PHY_PWR_CT RL / GPIO12	AM7
	LFRAME#	AV12
	OC0# / GPIO40	AL3
	OC1# / GPIO41	AT1
	OC2# / GPIO42	AH2
	OC3# / GPIO43	AV3
ndefined	PCH_OPI_RCOMP	AW15
dem	PCH_PWROK	AY7
•	PCH_TCK	AE62
	PCH_TDI	AD61
	PCH_TDO	AE61
	PCH_TMS	AD62
	ndefine	ntinued

	Indefined
	essors—Proc
Signal Name	Ball #
PCH_TRST#	AU62
PCIE_IREF	B27
PCIE_RCOMP	A27
PCIECLKRQ0# / GPIO18	U2
PCIECLKRQ1# / GPIO19	Y5
PCIECLKRQ2# / GPIO20	AD1
PCIECLKRQ3# / GPIO21	N1
PCIECLKRQ4# / GPIO22	U5
PCIECLKRQ5# / GPIO23	T2nde
PECI	N62
PERn1 / USB3Rn3	G17
PERn2 / USB3Rn4	F15
PERn3	G11
PERn4	F13
PERn5_L0	F10
PERn5_L1	F8
PERn5_L2	H10
PERn5_L3	E6
PERp1 / USB3Rp3	F17
PERp2 / USB3Rp4	G15
PERp3	F11
PERp4	G13
PERp5_L0	E10
PERp5_L1	E8
PERp5_L2	G10
PERp5_L3	F6
PETn1 / USB3Tn3	C30
PETn2 / USB3Tn4	B31
PETn3	C29
PETn4	B29
PETn5_L0	C23
PETn5_L1	B23
PETn5_L2	B21
	60

Signal Name	Ball #
n5_L3	B22
ETp1 / USB3Tp3	C31
ETp2 / USB3Tp4	A31
ETp3	B30
ETp4	A29
ETp5_L0	C22
ETp5_L1	A23
ETp5_L2	C21
ETp5_L3	A21
IRQA# / GPIO77	U6
IRQB# / GPIO78	P4
IRQC# / GPIO79	N4
IRQD# / GPIO80	N2
LTRST#	AG7
ME#	AD4
RDY#	J62
REQ#	K62
ROC_DETECT#	D61
ROC_OPI_RCOMP	AY15
ROC_TCK	E60
ROC_TDI	F63
ROC_TDO	F62
ROC_TMS	E61
ROC_TRST#	E59
ROCHOT#	K63
ROCPWRGD	C61
WR_DEBUG#	H59
WRBTN#	AL7
CIN# / GPIO82	V4
SMRST#	AW6
SVD	W23
SVD	Y22
SVD	B43
SVD	Т59
SVD SVD cc	AD60
SVD	AD59
cc	ntinued

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	Signal Name	Ball #
	RSVD	AA59
undefit	RSVD	AE60
	RSVD	AC59
	RSVD	AG58
	RSVD	V59
undefined und	RSVD	U59
	RSVD	AL1
inder	RSVD	AP7
	RSVD	AM11
	RSVD	AV62
	RSVD	D58
	KJVD	P20
	RSVD	R20
, un	RSVD	N60
	RSVD	AV2
ndein	RSVD	AF20
ed undefined un	RSVD	AB21
	RSVD	AY14
	RSVD	AW14
	RSVD	E15
	RSVD	E13
	RSVD	AL11
	RSVD	AC4
defin	RSVD	A5
dune	RSVD	N23
	RSVD	T23
	RSVD	U10
ed undefined u	RSVD	R23
	RSVD	L11
ned undefined l	RSVD	К10
ed	RSVD	F22
defille	RSVD	H22
d une	RSVD	J21
	RSVD	AT2
	RSVD	AU44
	RSVD	AV44
		continued.

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essors	undefined un	~		(Ū	ntel
	Signal Name	Ball #		Signal Name	Ball #
	RSVD	D15		RTCX1	AW5
	RSVD	AU10	5	RTCX2	AY5
	RSVD	AU15		SA_BA0	AU35
	RSVD	E1		SA_BA1	AV35
	RSVD	D1		SA_BA2	AY41
	RSVD	J20		SA_CAS#	AU34
_0	RSVD	H18		SA_CKE0	AU43
et l'	RSVD	AN10		SA_CKE1	AW43
	RSVD	AM10		SA_CKE2	AY42
	RSVD	L59	6	SA_CKE3	AY43
	RSVD	J58		SA_CLK#0	AU37
	RSVD	Y20		SA_CLK#1	AW36
	RSVD	AC20		SA_CLK0	AV37
	RSVD	V21		SA_CLK1	AY36
	RSVD	N58		SA_CS#0	AP33
11	RSVD	AC58		SA_CS#1	AR32
2.0	RSVD	AB23		SA_DQ0	AH63
	RSVD	AD23	6	SA_DQ1	AH62
	RSVD	AA23	80	SA_DQ10	AP63
	RSVD	AE59		SA_DQ11	AP62
	RSVD	K18		SA_DQ12	AM61
	RSVD	M20		SA_DQ13	AM60
	RSVD	K21		SA_DQ14	AP61
12	RSVD	M21		SA_DQ15	AP60
98,	RSVD_TP	AV63		SA_DQ32	AY58
	RSVD_TP	AU63		SA_DQ33	AW58
	RSVD_TP	C63	e	SA_DQ34	AY56
	RSVD_TP	C62		SA_DQ35	AW56
	RSVD_TP	A51		SA_DQ2	AK63
	RSVD_TP	B51		SA_DQ36	AV58
	RSVD_TP	P60		SA_DQ37	AU58
	RSVD_TP	P61	1	SA_DQ38	AV56
de	IVR_ERROR	N59	1	SA_DQ39	AU56
	IST_TRIGGER	N61	1	SA_DQ40	AY54
	RSVD_TP	L60		SA_DQ41	AW54
	RTCRST#	AU7		SA_DQ42	AY52
	co	ontinued			continued

Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] a matundefine **Processor Family** Datasheet - Volume 1 of 2 - undefit 103

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unc	Signal Name	Ball #
atined under.	SA_DQ43	AW52
	SA_DQ44	AV54
	SA_DQ45	AU54
	SA_DQ3	AK62
lefined undefined un	SA_DQ46	AV52
d un	SA_DQ47	AU52
	SB_DQ0	AY31
nder	SB_DQ1	AW31
ed u.	SB_DQ2	AY29
Inc	SB_DQ3	AW29
	SB_DQ4	AV31
	SB_DQ5	AU31
	SB_DQ6	AV29
tined undefined un	SB_DQ7	AU29
	SA_DQ4	AH61
detin	SB_DQ8	AY27
dun	SB_DQ9	AW27
INec	SB_DQ10	AY25
	SB_DQ11	AW25
	SB_DQ12	AV27
	SB_DQ13	AU27
	SB_DQ14	AV25
ed '	SB_DQ15	AU25
defill	SB_DQ32	AY23
d une.	SB_DQ33	AW23
afined undefined t	SA_DQ5	AH60
	SB_DQ34	AY21
	SB_DQ35	AW21
	SB_DQ36	AV23
	SB_DQ37	AU23
efined undefined	SB_DQ38	AV21
Lefine	SB_DQ39	AU21
uno	SB_DQ40	AY19
	SB_DQ41	AW19
61	SB_DQ42	AY17
	SB_DQ43	AW17
		continued

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ed undefine	rocessors—Pro
Signal Name	Ball #
SA_DQ6	AK61
SB_DQ44	AV19
SB_DQ45	AU19
SB_DQ46	AV17
SB_DQ47	AU17
SA_DQ7	AK60
SA_DQ8	AM63
SA_DQ9	AM62
SA_DQSN0	AJ61
SA_DQSN1	AN62
SA_DQSN4	AV57
SA_DQSN5	AV53
SB_DQSN0	AW30
SB_DQSN1	AV26
SB_DQSN4	AW22
SB_DQSN5	AV18
SA_DQSP0	AJ62
SA_DQSP1	AN61
SA_DQSP4	AW57
SA_DQSP5	AW53
SB_DQSP0	AV30
SB_DQSP1	AW26
SB_DQSP4	AV22
SB_DQSP5	AW18
SA_MA0	AU36
SA_MA1	AY37
SA_MA10	AP35
SA_MA11	AW41
SA_MA12	AU41
SA_MA13	AR35
SA_MA14	AV42
SA_MA15	AU42
SA_MA2	AR38
SA_MA3	AP36
SA_MA4	AU39
SA_MA5	AR36
	continued

Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] Processor Family e and undefine Datasheet - Volume 1 of 2 104

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	Signal Name	Ball #
	SATA2GP / GPIO36	V6
iii.	SATA3GP / GPIO37	AC1
	SATALED#	U3
	SB_BA0	AL35
	SB_BA1	AM36
d une	SB_BA2	AU49
	SB_CAS#	AM33
3	SB_CK#0	AM38
atined undef	SB_CK#1	AK38
	SB_CK0	AN38
	SB_CK1	AL38
	3D_UKLU	AY49
20	SB_CKE1	AU50
, uno	SB_CKE2	AW49
	SB_CKE3	AV50
lefined unde	SB_CS#0	AM32
	SB_CS#1	АК32
	SA_DQ16	AP58
	SA_DQ17	AR58
	SA_DQ26	AM54
*	SA_DQ27	AK54
ind	SA_DQ28	AL55
ed v	SA_DQ29	AK55
defined und	SA_DQ30	AR54
	SA_DQ31	AN54
	SA_DQ48	AK40
	SA_DQ49	AK42
	SA_DQ50	AM43
	SA_DQ51	AM45
ndefined un	SA_DQ18	AM57
ed u	SA_DQ52	AK45
defin	SA_DQ53	AK43
	SA_DQ54	AM40
	SA_DQ55	AM42
	SA_DQ56	AM46
	SA_DQ57	AK46
		ontinued

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inde.			elli
		d une	
Signal Name	Ball #	Signal Name	Ba
SA_DQ58	AM49	SB_DQ59	AL18
SA_DQ59	AK49	SA_DQ22	AR57
SA_DQ60	AM48	SB_DQ60	AK20
SA_DQ61	AK48	SB_DQ61	AM20
SA_DQ19	AK57	SB_DQ62	AR18
SA_DQ62	AM51	SB_DQ63	AP18
SA_DQ63	AK51	SA_DQ23	AN57
SB_DQ16	AM29	SA_DQ24	AP55
SB_DQ17	AK29	SA_DQ25	AR55
SB_DQ18	AL28	SA_DQSN2	AM58
SB_DQ19	AK28	SA_DQSN3	AM5
SB_DQ20	AR29	SA_DQSN6	AL43
SB_DQ21	AN29	SA_DQSN7	AL48
SB_DQ22	AR28	SB_DQSN2	AN28
SB_DQ23	AP28	SB_DQSN3	AN25
SA_DQ20	AL58	SB_DQSN6	AN21
SB_DQ24	AN26	SB_DQSN7	AN18
SB_DQ25	AR26	SA_DQSP2	AN58
SB_DQ26	AR25	SA_DQSP3	AN55
SB_DQ27	AP25	SA_DQSP6	AL42
SB_DQ28	AK26	SA_DQSP7	AL49
SB_DQ29	AM26	SB_DQSP2	AM28
SB_DQ30	AK25	SB_DQSP3	AM25
SB_DQ31	AL25	SB_DQSP6	AM2
SB_DQ48	AR21	SB_DQSP7	AM18
SB_DQ49	AR22	SB_MA0	AP40
SA_DQ21	AK58	SB_MA1	AR40
SB_DQ50	AL21	SB_MA10	AK36
SB_DQ51	AM22	SB_MA11	AV47
SB_DQ52	AN22	SB_MA12	AU47
SB_DQ53	AP21	SB_MA13	AK33
SB_DQ54	AK21	SB_MA14	AR46
SB_DQ55	AK22	SB_MA15	AP46
SB_DQ56	AN20	SB_MA2	AP42
SB_DQ57	AR20	SB_MA3	AR42
SB_DQ58	AK18	SB_MA4	AR45
C	continued		continu

Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] **Processor Family** July 2014 Datasheet - Volume 1 of 2 -A undefir

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Signal Name Ball # AP45 SB_MA5 SB_MA6 AW46 SB_MA7 AY46 SB MA8 AY47 SB MA9 AU46 SB ODT0 AL32 SB RAS# AM35 SB_WE# AK35 SDIO_CLK / E3 GPIO64 SDIO_CMD / F4 GPIO65 D3 SDIO_D0 / GPIO66 E4 SDIO_D1 / GPIO67 SDIO_D2 / GPIO68 C3 SDIO_D3 / GPIO69 E2 C4 SDIO_POWER_EN / GPI070 SERIRQ Τ4 SLP_A# AL5 SLP_LAN# AJ7 SLP_SO# AF3 SLP_S3# AT4 SLP S4# AJ6 SLP S5# / GPIO63 AP5 SLP_SUS# AP4 SLP_WLAN# / AM5 GPIO29 SM_DRAMRST# AV15 SM_PG_CNTL1 AV61 SM_RCOMP0 AU60 SM_RCOMP1 AV60 AU61 SM_RCOMP2 AP49 SM_VREF_CA SM_VREF_DQ0 AR51 SM_VREF_DQ1 AP51 SMBALERT# / AN2 GPIO11 continued...

0-	
Signal Name	Ball #
SMBCLK	AP2
SMBDATA	AH1
SML0ALERT# / GPIO60	AL2
SMLOCLK	AN1
SMLODATA	AK1
SML1ALERT# / PCHHOT# / GPIO73	AU4
SML1CLK / GPI075	AU3
SML1DATA / GPIO74	AH3
SPI_CLK	AA3
SPI_CS0#	Y7
SPI_CS1#	Y4
SPI_CS2#	AC2
SPI_IO2	Y6
SPI_IO3	AF1
SPI_MISO	AA4
SPI_MOSI	AA2
SPKR / GPIO81	V2
SRTCRST#	AV6
SUS_STAT# / GPIO61	AG4
SUSACK#	AK2
SUSCLK / GPIO62	AE6
SUSWARN# / SUSPWRDNACK / GPIO30	AV4
SYS_PWROK	AG2
SYS_RESET#	AC3
TD_IREF	B12
TESTLOW_AK8	AK8
TESTLOW_AL8	AL8
TESTLOW_C34	C34
TESTLOW_C35	C35
THERMTRIP#	D60
	G1
UART0_CTS# / GPIO94	01

Signal Name	Ball #	7
RT0_RTS# / 1093	J2	
ART0_RXD / PIO91	J1	und
ART0_TXD / PIO92	К3	unde
ART1_CTS# / PIO3	J4 ine	
ART1_RST# / PIO2	33	
ART1_RXD / PIO0	К4	
ART1_TXD / PIO1	G2	und
SB2n0	AN8	6
SB2n1	AR7	June
SB2n2	AR8	
SB2n3	AR10	
SB2n4	AM15	
SB2n5	AM13]
SB2n6	AP11	
SB2n7	AR13]
SB2p0	AM8	7
SB2p1	AT7	un
SB2p2	AP8	30 T
SB2p3	AT10	
SB2p4	AL15	7
SB2p5	AN13	1
SB2p6	AN11	7
SB2p7	AP13	7
SB3Rn1	G20	7
SB3Rn2	E18	
SB3Rp1	H20	ed ut
SB3Rp2	F18	Ť
SB3Tn1	C33	1
SB3Tn2	B33	1
SB3Tp1	B34	1
SB3Tp2	A33	1
SB3Tp2 SBRBIAS c	AJ11	1
c	ontinued	

Processors—Processor Ball and Signal Information

Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] undefine **Processor Family** Datasheet - Volume 1 of 2 106

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ino-	Signal Name	Ball #
	USBRBIAS#	AJ10
Indefilit	VCC	F59
	VCC	AB57
	VCC	AD57
tined un	vcc	AG57
d un	VCC	C24
160.	VCC	C28
	VCC	C32
	VCC	C36
	VCC	C40
	vcc	C44
	VCC	C48
	VCC	C52
ndefined u	vcc	C56
	VCC	E23
9611.	VCC	E25
	VCC	E27
	VCC	E29
	vcc	E31
	VCC	E33
	VCC	E35
	vcc	E37
, red	VCC	E39
defill	VCC	E41
	VCC	E43
Indefined	VCC	E45
	VCC	E47
	VCC	E49
	VCC	E51
undefined	VCC	E53
60	VCC	E55
retine	VCC	E57
	VCC	F24
	VCC	F28
	VCC	F32
	VCC	F36
	0	continued.

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Signal Name	Ball #	Signal Name	Ba
VCC	F40	VCC1_05	AE8
VCC	F44	VCC1_05	AF22
VCC	F48	 VCC1_05	H11
VCC	F52	VCC1_05	H15
VCC	F56	 VCC1_05	J11
VCC	G23	VCC1_05	AG16
VCC	G25	VCC1_05	AG17
VCC	G27	VCC3_3	V8
VCC	G29	VCC3_3	W9
VCC	G31	VCC3_3	K14
VCC	G33	VCC3_3	K16
VCC	G35	VCCACLKPLL	A20
vcc	G37	VCCAPLL	AA21
VCC	G39	VCCAPLL	W21
VCC	G41	VCCASW	AE9
VCC	G43	VCCASW	AF9
VCC	G45	VCCASW	AG8
VCC	G47	VCCASW	AG13
VCC	G49	VCCASW	AG14
VCC	G51	VCCCLK	J18
VCC	G53	VCCCLK	K19
VCC	G55	VCCCLK	J17
VCC	G57	VCCCLK	T21
VCC	H23	VCCCLK	R21
VCC	J23	VCCDSW3_3	AH10
VCC	К23	VCCHDA	AH14
VCC	K57	VCCHSIO	M9
VCC	L22	VCCHSIO	К9
VCC	M23	VCCHSIO	L10
vcc	M57	VCCIO_OUT	A59
VCC	P57	VCOMP_OUT	E20
VCC	U57	VCCRTC	AG10
VCC	W57	VCCSATA3PLL	B11
VCC_SENSE	E63	VCCSDIO	U8
VCC1_05	P9	VCCSDIO	Т9
VCC1_05	N8 6	VCCSPI	Y8
continued co		continu	

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afined under.	Signal Name	Ball #
	VCCST	AC22
	VCCST	AE22
	VCCST	AE23
	VCCST_PWRGD	B59
	VCCSUS3_3	AH11
d un	VCCSUS3_3	AA9
	VCCSUS3_3	AC9
ned undefined un	VCCSUS3_3	AE20
dui	VCCSUS3_3	AE21
	VCCTS1_5	J15
	VCCUSB3PLL	B18
	VDDQ	AH26
	VDDQ	AJ31
	VDDQ	AJ33
	VDDQ	AJ37
defin	VDDQ	AN33
d un-	VDDQ	AP43
med undefined un	VDDQ	AR48
	VDDQ	AY35
	VDDQ	AY40
	VDDQ	AY44
	VDDQ	AY50
tined undefined u	VIDALERT#	L62
defili	VIDSCLK	N63
d une	VIDSOUT	L63
inec	VR_EN	F60
	VR_READY	C59
	VSS JINO	P62
	VSS	D63
	VSS	P22
od	VSS	N21
10fine	VSS	A11
4 UNO-	VSS	A14
stined undefined	VSS	A18
N	VSS	A24
	VSS	A28
	sined a	continued

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	ed underinger	vecessors—Proce	ssor
é	Signal Name	Ball #	
<u> </u>	VSS	A32	VS
	VSS	A36	vs
	VSS	A40	VS
	VSS	A48	VS
	VSS	A52	VS
	VSS	A56	VS
	VSS	AA1	VS
2011	VSS	A44	VS
9	VSS	AA58	VS
	VSS	AB10	VS
	VSS	AB20	VS
	VSS	AE5	VS
	VSS	AB22	VS
	VSS	AB7	VS
	VSS	AC61	VS
	VSS	AD3	VS
10	VSS	AD63	VS
	VSS	AE10	VS
	VSS	AD21	VS
	VSS	AE58	VS
	VSS	AR43	VS
	VSS	C39	VS
	VSS	AF11	VS
	VSS	AF12	VS
00	VSS	AF14	VS
	VSS	AF15	VS
	VSS	AF17	VS
	VSS	AF18	VS
	VSS	AG21	VS
	vss	AG23	VS
	VSS	AG1	VS
	VSS	AG11	VS
5.	VSS	AG60	VS
U,	VSS	AG61	VS
\neg	VSS	AG62	VS
	VSS	AG63	vs
		continued	

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Signal Name	Ball #	
VSS	AH17	
VSS	AH19	
VSS	AH20	
VSS	AH22	
VSS	AH24	
VSS	AH28	
vss	AH30	
VSS	AH32	
VSS	AH34	
VSS	AH36	
VSS	AH38	
VSS	AH40	
VSS	AH42	
VSS	AH44	
VSS	AH49	
vss	AH51	
VSS	AH53	
VSS	AH55	
VSS	AH57	
VSS	AJ13	
VSS	AJ14	
VSS	AJ23	
VSS	AJ25	
vss	AJ27	
VSS	AJ29	
VSS	AJ35	
VSS	AJ39	
/SS	AJ41	
VSS	AJ43	
VSS	AJ45	
VSS	AJ47	
vss 👌	AJ50	
VSS	AJ52	
VSS	AJ54	
VSS	AJ56	
VSS	AJ58	
	ontinued	

 AG63
 VSS
 AJ56

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 Processor Family

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Processor Ball and Signal Information—Processors



Ball #

AR49 AR5 AR52

AT13 AT35 AT37 AT40 AT42

AT43 AT46 AT49 AT61

AT62 AT63 AU1 AU16 AU18

AU20 AU22 AU24

AU26 AU28 AU30 AU33 AU51

AU53 AU55 AU57 AU59

AV14 D62 AV16 AV20 AV24

AV28 AV33 continued... defined unde

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	Signal Name	Ball #
	VSS	AJ60
ndefille	VSS	AJ63
	VSS	AK23
	VSS	AK3
afined unde	VSS	AK52
d une	VSS	AL10
	VSS	AL13
	VSS	AL17
	VSS	AL20
	VSS	AL22
	VSS	AL23
	VSS	AL26
1	VSS	AL29
, unc	VSS	AL31
ndefined und	VSS	AL33
den	VSS	AL36
N7.	VSS	AL39
	VSS	AL40
	VSS	AL45
	VSS	AL46
	VSS	AL51
77.	VSS	AL52
ned u	VSS	AL54
defini	VSS	AL57
undefined un	VSS	AL60
	VSS	AL61
	VSS	AM1
	VSS	AM17
	VSS	AM23
	VSS	AM31
undefined ut	VSS	AM52
define	VSS	AN17
nu	VSS	AN23
	VSS	AN31
	VSS	AN32
	VSS	AN35

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Signal Name	Ball #	Signal
VSS	AN36	VSS
VSS	AN39	VSS
VSS	AN40	VSS
VSS	AN42	VSS
VSS	AN43	VSS
VSS	AN45	VSS
VSS	AN46	VSS
VSS	AN48	VSS
VSS	AN49	VSS
VSS	AN51	VSS
VSS	AN52	VSS
VSS	AN60	VSS
VSS	AN63	VSS
VSS	AN7	VSS
VSS	AP10	VSS
VSS	AP10 AP17	VSS
VSS	AP17 AP20	VSS
VSS	AP20 AP22	VSS
VSS	AP22 AP23	VSS
	AP23	
VSS	<u></u>	VSS
VSS	AP29	VSS
VSS	AP3	VSS
VSS	AP31	VSS
VSS	AP38	VSS
VSS	AP39	VSS
VSS	AP52	VSS
VSS	AP54	VSS
VSS	AP57	VSS
VSS	AR11	VSS
VSS	AR15	VSS
VSS	AR17	VSS
VSS	AR23	VSS
VSS	AR31	VSS
VSS	AR33	VSS
VSS	AR39	VSS
VSS	AP48	VSS
	continued	

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unos	Signal Name	Ball #
	VSS	AV34
ined under	VSS	AV36
	VSS	AV39
	VSS	AV41
ned undefined un	VSS	AV43
d un	VSS	AV46
	VSS	AV49
nder	VSS	AV51
edu	VSS	AV55
	VSS	AV59
	VSS	AV8
	VSS	AW16
	VSS	AW24
. u	VSS	AW33
	VSS	AW35
den	VSS	AW37
ined undefined ut	VSS	AW4
ne	VSS	AW40
	VSS	AW42
	VSS	AW44
	VSS	AW47
	VSS	AW50
tined undefined i	VSS	AW51
defill	VSS	AW59
d une	VSS	AW60
	VSS	AY11
	VSS	AY16
	VSS	AY18
	VSS	AY22
	VSS	AY24
atined undefined	VSS	AY26
Aefine	VSS	AY30
4 uno	VSS	AY33
	VSS	AY51
	VSS	AY53
	VSS	AY57

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1	Signal Name	Ball #	
	VSS	AY59	VS
	VSS	AY6	VS
	VSS	AY4	VS
	VSS	B20	VS
	VSS	B24	VS
	VSS	B26	VS
	VSS	B28	VS
S. N	VSS	B32	VS
	VSS	C38	VS
	VSS	B36	VS
	VSS	B4	VS
	VSS	B40	VS
	VSS	B44	VS
	VSS	C14	VS
	VSS	B48	VS
Ś	VSS	B52	VS
	VSS	B56	VS
	VSS	B60	VS
	VSS	C11	VS
	VSS	C18	VS
	VSS	C20	VS
	VSS	C25	VS
	VSS	C27	VS
	VSS	D12	VS
9e	VSS	D14	VS
	VSS	D18	VS
	VSS	D21	VS
	VSS	D23	VS
1	VSS	D25	VS
	VSS	D26	VS
	VSS	D27	VS
1	VSS	D29	VS
6	VSS	D2	VS
	VSS	D30	VS
	VSS	D31	VS
	VSS	D33	VS
	C	ontinued	

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Signal Name	Ball #	7	
/SS	D34		
VSS	D35		
VSS	D37		
VSS	D38		
VSS	D39		
VSS	D41		
vss	D42		
VSS	D43	-	
/SS	D45		
VSS	D46	Jun	
VSS	D47	-	
VSS	D49	_	6
VSS	D50	100	
VSS	D51	<u> </u>	
VSS	D53	-	
VSS	D54	-	
vss	D55	-	
VSS	D57	-	
VSS	D59		
VSS	E11	-	
VSS	E17	1	5
VSS	F42	ज ि	
VSS	F20	-	
/SS	D5	-	
VSS	F26	-	
VSS	F30	-	
/SS	F30		
/SS	F34 F38	_	
		_	
VSS	G6	60	
VSS	F46		
VSS	F50	_	
VSS	F54	_	
VSS	F58	_	
VSS	F61	_	
VSS	G18	_	
VSS	G22 ontinued	_	

 U33
 USS
 G22

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Sig VSS VSS VSS	nal Name	Ball #	Sig	nal Name	Ball #	undefi
VSS		G3	VSS		V3	unde
VSS	stine	G5	VSS		V7	3
VSS	Inoc	G8	VSS		W20	
VSS		H13	VSS		Y10	
VSS		H17	VSS	sine	U9	
VSS		H57	VSS	96.	Y59	undefin d undefi
VSS		J10	VSS		Y63	
VSS		J22	VSS		W22	(A)
VSS VSS VSS VSS VSS VSS VSS VSS		J59	VSS		V58	nder
VSS	ein ^e	J63	VSS		AH46	d'u'
VSS	nder	K1	VSS		V23	1
V55		K12	VSS	4	AH16	1
VSS		R22	VSS_S	SENSE	E62	d undefi
VSS		L13	WAKE	#0 ⁶¹	AJ5	1
vss		L15	XTAL2	4_IN	A25	1
VSS		L17	XTAL2	4_OUT	B25	1
VSS VSS VSS VSS VSS VSS VSS VSS VSS		L18	·			
VSS		L20	-			d une
VSS	defit	L58	-			
VSS	JUNC	L61	-		ude.	
VSS		L7				
VSS		M22	-	define		
vss		N10		JUC		
VSS		N3	sineo			
VSS		C57	57.			
VSS		P59	-			, uno.
VSS	181	P63	1			
VSS VSS VSS VSS VSS VSS VSS VSS VSS	, uno-	R10	1		det	*
VSS	2 0 _	R8	1		dun	
VSS		T1	1	Sine		
VSS		T58		unde		
VSS		D8	, red			
VSS		U20	etni			ned under
VSS		U22	Ĩ			
VSS VSS VSS VSS VSS VSS VSS	3	U61	1			edu
	76		-			111
VSS		V10				

tofined U

undefined ut Signal Name	Ball #	undefined			
VSS	V3	inde			
VSS	V7				2
VSS	W20				ver
VSS	Y10				
VSS	U9			du.	
VSS	Y59		Aetin		
VSS	Y63	2	unc		
VSS	W22				
VSS	V58	nder			
VSS	AH46	undefined			
VSS	V23				
VSS	AH16			dei	
VSS_SENSE	E62			d un.	
WAKE#	AJ5		1 efil		
XTAL24_IN	A25		unoc		
XTAL24_OUT	B25				
VSS VSS VSS VSS VSS VSS_SENSE WAKE# XTAL24_IN XTAL24_OUT	undefin	ed undefine	undefi	ned unde	stine

tel® Per Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] **Processor Family** July 2014 Datasheet - Volume 1 of 2 .e. Order No.: 329001-007 111



Processors-Processor Ball and Signal Information

Table 59.

Ball List by Signal Name for LPDDR3 Configuration

	Signal Name	Ball #
	ACPRESENT / GPIO31	AJ8
	APWROK	AB5
6	BATLOW# / GPIO72	AN4
defined und	BMBUSY# / GPIO76	P1
Jefill	BPM#0	J60
	BPM#1	нео
	BPM#2	H61
	BPM#3	H62
	BPM#4	К59
	BPM#5	H63
	BPM#6	К60
ed un	BPM#7	J61
undefined un	CATERR#	K61
	CFG[0]	AC60
	CFG[1]	AC62
	CFG[10]	V60
	CFG[11]	U60
	CFG[12]	Т63
	CFG[13]	T62
-d ur	CFG[14]	T61
undefined ur	CFG[15]	Т60
unde	CFG[16]	AA62
	CFG[17]	AA61
	CFG[18]	U63
	CFG[19]	U62
	CFG[2]	AC63
	CFG[3]	AA63
24	CFG[4]	AA60
undefined	CFG[5]	Y62
ude.	CFG[6]	Y61
	CFG[7]	Y60
	CFG[8]	V62
	CFG[9]	V61
	sined u co	ontinued

CLACL_CLKACL_DATAACL_RST#ACLKOUT_ITPXDP_NBCLKOUT_LPC_0ACLKOUT_LPC_1ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P4ACLKOUT_PCIE_P4ACLKOUT_PCIE_P5ACLKRUN# / GPI032ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	63 F2 D2 F4 35 35 N15
CL_DATAACL_RST#ACLKOUT_ITPXDP_NBCLKOUT_ITPXDP_PACLKOUT_LPC_0ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P1ACLKOUT_PCIE_P3CCLKOUT_PCIE_P1ACLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P3ACLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPI032ADAISY_CHAIN_NCTA<	D2 F4 35 35
CL_DATAACL_RST#ACLKOUT_ITPXDP_NBCLKOUT_ITPXDP_PACLKOUT_LPC_0ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P1ACLKOUT_PCIE_P3CCLKOUT_PCIE_P1ACLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P3ACLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPI032ADAISY_CHAIN_NCTA<	F4 35 35
CLACLKOUT_ITPXDP_NBCLKOUT_ITPXDP_PACLKOUT_LPC_0ACLKOUT_LPC_1ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P4ACLKOUT_PCIE_P5ACLKRUN# / GPI032ADAISY_CHAIN_NCTAPAISY_CHAIN_NCTAPAISY_CHAIN_NCTADAISY_CHAIN_NCTA<	F4 35 35
CLKOUT_ITPXDP_NBCLKOUT_ITPXDP_PACLKOUT_LPC_0ACLKOUT_LPC_1ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32CDAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	35
CLKOUT_ITPXDP_PACLKOUT_LPC_0ACLKOUT_LPC_1ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKRUN# / GPI032ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	
CLKOUT_LPC_0ACLKOUT_LPC_1ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P3ACLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P3ACLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT 	
CLKOUT_LPC_1ACLKOUT_PCIE_N0CCLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKRUN# / GPI032CDAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	NT J
CLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_P0CCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	P15
CLKOUT_PCIE_N1BCLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_N4ACLKOUT_PCIE_P0CCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	43
CLKOUT_PCIE_N2CCLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P0CCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	41
CLKOUT_PCIE_N3BCLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P0CCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	41
CLKOUT_PCIE_N4ACLKOUT_PCIE_N5BCLKOUT_PCIE_P0CCLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	38
CLKOUT_PCIE_N5BCLKOUT_PCIE_P0CCLKOUT_PCIE_P1ACLKOUT_PCIE_P1BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKOUT_PCIE_P5ACLKRUN# / GPI032VDAISY_CHAIN_NCT F_A4ADAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	39
CLKOUT_PCIE_P1ACLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P4ACLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCTAPAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	37
CLKOUT_PCIE_P2BCLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A4ADAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	42
CLKOUT_PCIE_P3CCLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCTADAISY_CHAIN_NCTADAISY_CHAIN_NCTADAISY_CHAIN_NCTADAISY_CHAIN_NCTAF_A60ADAISY_CHAIN_NCTAF_A61ADAISY_CHAIN_NCTA	41
CLKOUT_PCIE_P4BCLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCT F_A4ADAISY_CHAIN_NCT F_A60ADAISY_CHAIN_NCT F_A61ADAISY_CHAIN_NCT F_A61A	42
CLKOUT_PCIE_P5ACLKRUN# / GPIO32VDAISY_CHAIN_NCTAF_A3ADAISY_CHAIN_NCTAF_A4ADAISY_CHAIN_NCTAF_A60ADAISY_CHAIN_NCTAF_A61ADAISY_CHAIN_NCTAF_A61A	37
CLKRUN# / GPI032 V DAISY_CHAIN_NCT A F_A3 A DAISY_CHAIN_NCT A F_A4 A DAISY_CHAIN_NCT A F_A60 A DAISY_CHAIN_NCT A F_A61 A	39
GPI032DAISY_CHAIN_NCTAF_A3ADAISY_CHAIN_NCTAF_A4ADAISY_CHAIN_NCTAF_A60ADAISY_CHAIN_NCTAF_A61ADAISY_CHAIN_NCTA	37
F_A3DAISY_CHAIN_NCTF_A4DAISY_CHAIN_NCTF_A60DAISY_CHAIN_NCTAF_A61DAISY_CHAIN_NCTAF_A61	5
F_A4 DAISY_CHAIN_NCT F_A60 DAISY_CHAIN_NCT A F_A61 DAISY_CHAIN_NCT A	3
F_A60 DAISY_CHAIN_NCT F_A61 DAISY_CHAIN_NCT	4
F_A61 DAISY_CHAIN_NCT A	60
	61,00
1_A02	
DAISY_CHAIN_NCT A F_AV1	62
DAISY_CHAIN_NCT A F_AW1	62 V1
DAISY_CHAIN_NCT A F_AW2	
DAISY_CHAIN_NCT A F_AW3	V1

fined und		
sineu		
Signal Name	Ball #	
DAISY_CHAIN_NCT _AW61	AW61	Ind
DAISY_CHAIN_NCT _AW62	AW62	, nd
DAISY_CHAIN_NCT _AW63	AW63	Ъ.
DAISY_CHAIN_NCT _AY2	AY2	
DAISY_CHAIN_NCT	AY3	
DAISY_CHAIN_NCT	AY60	
DAISY_CHAIN_NCT	AY61	un
DAISY_CHAIN_NCT E_AY62	AY62	un
DAISY_CHAIN_NCT =_B2	B2	
DAISY_CHAIN_NCT	В3	
DAISY_CHAIN_NCT	B61	-
DAISY_CHAIN_NCT _B62	B62	U
DAISY_CHAIN_NCT E_B63	B63	<u>ار ا</u>
AISY_CHAIN_NCT	C1	Ģ
DAISY_CHAIN_NCT	C2	
OCPRTC	AE7	1
OCPSUS1	AD10	1
OCPSUS1	AD8	1
CPSUS2	AH13	1
CPSUS3	J13	ed 1
CPSUS4	AB8	<u> </u>
CPSUSBYP	AG19	1
CPSUSBYP	AG20	1
DI1_TXN[0]	C54	1
DDI1_TXN[1]	B58	1
DDI1_TXN[2]	B55	1
DDI1_TXN[2] DDI1_TXN[3] cc	A57	1
cc	ontinued	-

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ned undefilit	Signal Name	Ball #
	DDI1_TXP[0]	C55
	DDI1_TXP[1]	C58
	DDI1_TXP[2]	A55
	DDI1_TXP[3]	B57
undefined undef	DDI2_TXN[0]	C51
d unc	DDI2_TXN[1]	C53
	DDI2_TXN[2]	C49
9er.	DDI2_TXN[3]	A53
	DDI2_TXP[0]	C50
	DDI2_TXP[1]	B54
	DDI2_TXP[2]	B50
		B53
50	DDPB_AUXN	C5
ndefined unde	DDPB_AUXP	B5
	DDPB_CTRLCLK	B9
der.	DDPB_CTRLDATA	C9
Ŧ	DDPB_HPD	C8
	DDPC_AUXN	B6
	DDPC_AUXP	A6
	DDPC_CTRLCLK	D9
	DDPC_CTRLDATA	D11
ind	DDPC_HPD	A8
ned v	DEVSLP0 / GPIO33	P2
defin	DEVSLP1 / GPIO38	L2
	DEVSLP2 / GPIO39	N5 0
	DIFFCLK_BIASREF	C26
	DPWROK	AV5
ndefined und	DSWVRMEN	AW7
	EDP_AUXN	A45
27.	EDP_AUXP	B45
undefined un	eDP_BKLCTL	B8
defilit	eDP_BKLEN	A9
	EDP_DISP_UTIL	A43
	EDP_HPD	D6
	EDP_RCOMP	D20
	EDP_TXN0	C45
	0 00	ontinued

	ndefill	
ors undefin	ed undefined	
Signal Na		Si
EDP_TXN1	A47	GPIO
EDP_TXN2	C47	GSPI GPIO
EDP_TXN3	A49	GSPI
EDP_TXP0	B46	GPIO
EDP_TXP1	B47	GSPI GPIO
EDP_TXP2	C46	GSPI
EDP_TXP3	B49	GPIO
eDP_VDDEN	C6	GSPI GPIO
GPIO10	AM2	GSPI
GPI013	AT3	GPIO
GPIO14	AH4	GSPI GPIO
GPIO15	AD6	GSPI
GPIO16	Y1	GPIO
GPIO17	T3	HDA_ I2S0
GPIO24	AD5	HDA
GPIO25	AM4	I2S1
GPIO26	AN3	HDA_ / I2S
GPIO27	AN5	HDA
GPIO28	AD7	I2S_
GPIO44	AK4	HDA_ I2S0
GPIO45	AG5	HDA
GPIO46	AG3	I2S1
GPIO47	AB6	HDA_
GPIO48	U4	I2S0
GPIO49	Y3	HDA_ I2S0
GPIO50	P3	HSIO
GPIO51	R5	12C0
GPIO52	Linos	12C0
GPIO53		I2C1
GPIO54	L3	I2C1
GPIO55	U7	I2S1_
GPIO56	AG6	INTR
GPIO57	AP1	INTV
GPIO58	AL4	JTAG
GPIO59	AT5	LADO
GPIO8	AU2 continued	
	Continueum	

	Signal Name	Ball #
GP	109	AM3
	PI_MOSI / IO90	К2
	PI0_CLK / IO84	L6
	PI0_CS# / IO83	R6
	PIO_MISO / IO85	N6
	PI0_MOSI / IO86	L8
	PI1_CLK / IO88	L5
	PI1_CS# / IO87	R7
	PI1_MISO / IO89	N7
	A_BCLK / 60_SCLK	AW8
	A_DOCK_EN# / S1_TXD	AW10
	A_DOCK_RST# 2S1_SFRM	AV10
	A_RST# / S_MCLK	AU8
	A_SDI0 / 60_RXD	AY10
	A_SDI1 / S1_RXD	AU12
	A_SDO /	AU11
	A_SYNC / 50_SFRM	AV11
нs	IOPC / GPIO71	Y2
120	CO_SCL / GPIO5	F3
120	CO_SDA / GPIO4	F2
120	C1_SCL / GPIO7	F1
120	C1_SDA / GPIO6	G4
125	S1_SCLK	AY8
IN	TRUDER#	AU6
IN	IVRMEN	AV7
JTA	AGX	AE63
LAI	D0	AE63 AU14 Intinued
	co	ntinued

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der.	Signal Name	Ball #
	LAD1	AW12
	LAD2	AY12
	LAD3	AW11
	LAN_PHY_PWR_CT RL / GPIO12	AM7
ned und	LFRAME#	AV12
	OC0# / GPIO40	AL3
	OC1# / GPIO41	AT1
	OC2# / GPIO42	AH2
	OC3# / GPIO43	AV3
	PCH_OPI_RCOMP	AW15
	PCH_PWROK	AY7
	РСН_ТСК	AE62
efined unr	PCH_TDI	AD61
d un	PCH_TDO	AE61
stine	PCH_TMS	AD62
	PCH_TRST#	AU62
	PCIE_IREF	B27
	PCIE_RCOMP	A27
	PCIECLKRQ0# / GPIO18	U2
	PCIECLKRQ1# / GPIO19	Y5
nedu	PCIECLKRQ2# / GPIO20	AD1
	PCIECLKRQ3# / GPIO21	N1
	PCIECLKRQ4# / GPIO22	U5 UI
Jeffned un	PCIECLKRQ5# / GPIO23	T2
	PECI	N62
	PERn1 / USB3Rn3	G17
20	PERn2 / USB3Rn4	F15
siner	PERn3	G11
idefined u	PERn4	F13
	PERn5_L0	F10
	PERn5_L1	F8
	PERn5_L2	H10
	cd	ntinued

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Proc	essors–Pro	
d undefin Proc		
dun		
Signal Name	Ball #	
PERn5_L3	E6	
PERp1 / USB3Rp3	F17	
PERp2 / USB3Rp4	G15	
PERp3	F11	
PERp4	G13	
PERp5_L0	E10	
PERp5_L1	E8	
PERp5_L2	G10	
PERp5_L3	F6	
PETn1 / USB3Tn3	C30	
PETn2 / USB3Tn4	B31	
PETn3	C29	
PETn4	B29	
PETn5_L0	C23	
PETn5_L1	B23	
PETn5 L2	B21	
PETn5_L3	B22	
PETp1 / USB3Tp3	C31	
PETp2 / USB3Tp4	A31 📢	
PETp3	B30	
PETp4	A29	
PETp5_L0	C22	
PETp5_L1	A23	
PETp5_L2	C21	
PETp5_L3	A21	
PIRQA# / GPI077	U6	
PIRQB# / GPIO78	P4	
PIRQC# / GPIO79	N4	
PIRQD# / GPIO80	_N2	
PLTRST#	AG7	
PME#	AD4	
PRDY#	J62	
PREQ#	K62	
PROC_DETECT#	D61	
PROC_OPI_RCOMP	AY15	
PROC_TCK	E60	
	ntinued	

Signal Name	Ball #
ROC_TDI	F63
ROC_TDO	F62
ROC_TMS	E61
ROC_TRST#	E59
ROCHOT#	К63
ROCPWRGD	C61
WR_DEBUG#	Н59
WRBTN#	AL7
CIN# / GPIO82	V4
SMRST#	AW6
SVD	W23
SVD	Y22
SVD	B43
SVD	Т59
SVD	AD60
SVD	AD59
SVD	AA59
SVD	AE60
SVD	AC59
SVD	AG58
SVD	V59
SVD	U59
SVD	AL1
SVD	AP7
SVD	AM11
SVD	AV62
SVD	D58
SVD	P20
SVD	R20
SVD	N60
SVD	AV2
SVD	AF20
SVD	AB21
SVD	AY14
ISVD ISVD and Mobile Intel [®] Ce	AW14
SVD	E15
co	ntinued

Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] e undefine Datasheet - Volume 1 of 2 114

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	Signal Name	Ball :
	RSVD	E13
ndefill	RSVD	AL11
	RSVD	AC4
	RSVD	A5
	RSVD	N23
4 UN	RSVD	T23
ndefined un	RSVD	U10
ge.	RSVD	R23
	RSVD	L11
	RSVD	К10
	RSVD	F22
	KSVD	H22
	RSVD	J21
undefined un	RSVD	AT2
	RSVD	AU44
odein.	RSVD	AV44
011.	RSVD	D15
	RSVD	AU10
	RSVD	AU15
	RSVD	E1
	RSVD	D1
	RSVD	J20
red	RSVD	H18
defill	RSVD	AN10
UNC	RSVD	AM10
	RSVD	L59
undefined	RSVD	J58
	RSVD	Y20
	RSVD	AC20
	RSVD	V21
60	RSVD	N58
ed undefined	RSVD	AC58
4 UNC	RSVD	AB23
	RSVD	AD23
	RSVD	AA23
	RSVD	AE59
	odefined	continued

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ed ui			
Jefine -		(nte
unoc			6.11.
b	1 1	ed un.	
Signal Name	Ball #	Signal Name	Ba
RSVD	K18	SA_DQ12	AM6
RSVD	M20	SA_DQ13	AM6
RSVD	K21	SA_DQ14	AP61
RSVD	M21	SA_DQ15	AP60
RSVD_TP	AV63	SA_DQ32	AY58
RSVD_TP	AU63	SA_DQ33	AW5
RSVD_TP	C63	SA_DQ34	AY56
RSVD_TP	C62	SA_DQ35	AW5
RSVD_TP	A51	SA_DQ2	AK6
RSVD_TP	B51	SA_DQ36	AV5
RSVD_TP	P60	SA_DQ37	AU5
RSVD_TP	P61	SA_DQ38	AV5
IVR_ERROR	N59	SA_DQ39	AU5
IST_TRIGGER	N61	SA_DQ40	AY54
RSVD_TP	L60	SA_DQ41	AW5
RTCRST#	AU7	SA_DQ42	AY52
RTCX1	AW5	SA_DQ43	AW5
RTCX2	AY5	SA_DQ44	AV54
SA_CAB4	AU35	SA_DQ45	AU5
SA_CAB6	AV35	SA_DQ3	AK62
SA_CAA5	AY41	SA_DQ46	AV52
SA_CAB1	AU34	SA_DQ47	AU5
SA_CKE0	AU43	SB_DQ0	AY3
SA_CKE1	AW43	SB_DQ1	AW3
SA_CKE2	AY42	SB_DQ2	AY29
SA_CKE3	AY43	SB_DQ3	AW2
SA_CLK#0	AU37	SB_DQ4	AV3
SA_CLK#1	AW36	SB_DQ5	AU3
SA_CLK0	AV37	SB_DQ6	AV29
SA_CLK1	AY36	SB_DQ7	AU29
SA_CS#0	AP33	SA_DQ4	AH6
SA_CS#1	AR32	SB_DQ8	AY27
SA_DQ0	AH63	SB_DQ9	AW2
SA_DQ1	AH62	SB_DQ10	AY25
SA_DQ10	AP63	SB_DQ11	AW2
SA_DQ10 SA_DQ11	AP62	SB_DQ12	AV2
=	ontinued		continu

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ed undert	Signal Name	Ball #
	SB_DQ13	AU27
	SB_DQ14	AV25
	SB_DQ15	AU25
	SB_DQ32	AY23
defined un	SB_DQ33	AW23
A UN	SA_DQ5	AH60
	SB_DQ34	AY21
Jer.	SB_DQ35	AW21
	SB_DQ36	AV23
	SB_DQ37	AU23
	SB_DQ38	AV21
	SB_DQ39	AU21
	SB_DQ40	AY19
ndefined	SB_DQ41	AW19
	SB_DQ42	AY17
Jen.	SB_DQ43	AW17
	SA_DQ6	AK61
	SB_DQ44	AV19
	SB_DQ45	AU19
	SB_DQ46	AV17
	SB_DQ47	AU17
	SA_DQ7	AK60
ed	SA_DQ8	AM63
	SA_DQ9	AM62
	SA_DQSN0	AJ61
	SA_DQSN1	AN62
	SA_DQSN4	AV57
defined	SA_DQSN5	AV53
	SB_DQSN0	AW30
	SB_DQSN1	AV26
Indefined	SB_DQSN4	AW22
Jefine	SB_DQSN5	AV18
	SA_DQSP0	AJ62
	SA_DQSP1	AN61
	SA_DQSP4	AW57
	SA_DQSP5	AW53
	0	continued

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			essors—Proces	550
e		Signal Name	Ball #	
		SB_DQSP0	AV30	S
		SB_DQSP1	AW26	PE
		SB_DQSP4	AV22	S/ PE
		SB_DQSP5	AW18	S
		SA_CAB9	AU36	PE
		SA_CAB8	AY37	S/ PE
		SA_CAB7	AP35	S
26	511	SA_CAA7	AW41	PE
		SA_CAA6	AU41	S/ PE
		SA_CAB0	AR35	S
		SA_CAA9	AV42	PE
		SA_CAA8	AU42	S/
		SA_CAB5	AR38	S
		NOT USED	AP36	PE
		NOT USED	AU39	S
	Ň	SA_CAA0	AR36	S
20		SA_CAA2	AV40	S
		SA_CAA4	AW39	S
		SA_CAA3	AY39	S
		SA_CAA1	AU40	SI
		SA_ODT0	AP32	SI
		SA_CAB3	AY34	SI
		SA_CAB2	AW34	SI
		SATA_IREF	A12	SI
0	96	SATA_RCOMP	C12	SI
		SATA_Rn0 / PERn6_L3	35	SI
		SATA_Rn1 / PERn6_L2	J8	SI
		SATA_Rn2 / PERn6_L1	J6	SI
		 SATA_Rn3 / PERn6_L0	F5	SI
		SATA Rp0 /	H5	SI
	6	PERp6_L3		SI
S,		SATA_Rp1 / PERp6_L2	H8	S
		SATA_Rp2 / PERp6_L1	H6	S
		co	ontinued	

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Signal Name	Ball #
SATA_Rp3 /	E5
PERp6_L0	
SATA_Tn0 / PETn6_L3	B15
SATA_Tn1 / PETn6_L2	A17
SATA_Tn2 / PETn6_L1	B14
SATA_Tn3 / PETn6_L0	C17
SATA_Tp0 / PETp6_L3	A15
SATA_Tp1 / PETp6_L2	B17
SATA_Tp2 / PETp6_L1	C15
SATA_Tp3 / PETp6_L0	D17
SATA0GP / GPIO34	V1
SATA1GP / GPIO35	U1
SATA2GP / GPIO36	V6
SATA3GP / GPIO37	AC1
SATALED#	U3
SB_CAB4	AL35
SB_CAB6	AM36
SB_CAA5	AU49
SB_CAB1	AM33
SB_CK#0	AM38
SB_CK#1	AK38
SB_CK0	AN38
SB_CK1	AL38
SB_CKE0	AY49
SB_CKE1	AU50
SB_CKE2	AW49
SB_CKE3	AV50
SB_CS#0	AM32
SB_CS#1	AK32
SA_DQ16	AP58
SA_DQ17	AR58
SA_DQ26	AM54
CC	ontinued

 Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®]

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ed undefine	Signal Name	Ball #	[
	SA_DQ27	AK54	
	SA_DQ28	AL55	
	SA_DQ29	AK55	
	SA_DQ30	AR54	
	SA_DQ31	AN54	
Un	SA_DQ48	AK40	
	SA_DQ49	AK42	a
	SA_DQ50	AM43	
	SA_DQ51	AM45	
	SA_DQ18	AM57	
ed und	SA_DQ52	AK45	
	SA_DQ53	AK43	
	SA_DQ54	AM40	
nu ,	SA_DQ55	AM42	
efined un	SA_DQ56	AM46	
	SA_DQ57	AK46	
	SA_DQ58	AM49	
	SA_DQ59	AK49	
	SA_DQ60	AM48	
	SA_DQ61	AK48	
	SA_DQ19	AK57	
	SA_DQ62	AM51	
. red v	SA_DQ63	AK51	
afined ut	SB_DQ16	AM29	112
	SB_DQ17	AK29	8)-
	SB_DQ18	AL28	
	SB_DQ19	AK28	
	SB_DQ20	AR29	
	SB_DQ21	AN29	
Jefined	SB_DQ22	AR28	
60	SB_DQ23	AP28	
etine	SA_DQ20	AL58	- 65
	SB_DQ24	AN26	et
	SB_DQ25	AR26	
	SB_DQ26	AR25	
	SB_DQ27	AP25	
	ed a	continued	

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ors			
	inder		
] [Signal Name	Ball #	Γ
	SB_DQ28	AK26	
	SB_DQ29	AM26	
	SB_DQ30	AK25	
	SB_DQ31	AL25	
	SB_DQ48	AR21	F
	SB_DQ49	AR22	F
	SA_DQ21	AK58	
Ue	SB_DQ50	AL21	
	SB_DQ51	AM22	F
	SB_DQ52	AN22	Ý
	SB_DQ53	AP21	
	SB_DQ54	AK21	
	SB_DQ55	AK22	F
	SB_DQ56	AN20	F
	SB_DQ57	AR20	F
1)	SB_DQ58	AK18	F
	SB_DQ59	AL18	F
	SA_DQ22	AR57	2
	SB_DQ60	AK20	
	SB_DQ61	AM20	
	SB_DQ62	AR18	F
	SB_DQ63	AP18	F
	SA_DQ23	AN57	F
2	SA_DQ24	AP55	F
8	SA_DQ25	AR55	
	SA_DQSN2	AM58	
	SA_DQSN3	AM55	sb
	SA_DQSN6	AL43	F
	SA_DQSN7	AL48	F
	SB_DQSN2	AN28	F
	SB_DQSN3	AN25	F
	SB_DQSN6	AN21	
e	SB_DQSN7	AN18	
1	SA_DQSP2	AN58	
1	SA_DQSP3	AN55	e
1	SA_DQSP6	AL42	
		continued	

Signal Name	Ball #
SA_DQSP7	AL49
SB_DQSP2	AM28
SB_DQSP3	AM25
SB_DQSP6	AM21
SB_DQSP7	AM18
SB_CAB9	AP40
SB_CAB8	AR40
SB_CAB7	AK36
SB_CAA7	AV47
SB_CAA6	AU47
SB_CAB0	AK33
SB_CAA9	AR46
SB_CAA8	AP46
SB_CAB5	AP42
NOT USED	AR42
NOT USED	AR45
SB_CAA0	AP45
SB_CAA2	AW46
SB_CAA4	AY46
SB_CAA3	AY47
SB_CAA1	AU46 🔬
SB_ODT0	AL32
SB_CAB3	AM35
SB_CAB2	AK35
SDIO_CLK / GPIO64	E3
SDIO_CMD / GPIO65	F4
SDIO_D0 / GPIO66	D3
SDIO_D1 / GPIO67	E4
SDIO_D2 / GPIO68	C3
SDIO_D3 / GPIO69	E2
SDIO_POWER_EN / GPIO70	C4
SERIRQ	Т4
SLP_A#	AL5
SLP_LAN#	AL5 AJ7 Intinued
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Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] e and undefine Processor Family Datasheet – Volume 1 of 2 July 2014 - undefin Order No.: 329001-007

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	Signal Name	Ball #
	SLP_S0#	AF3
ndell	SLP_S3#	AT4
	SLP_S4#	AJ6
	SLP_S5# / GPIO63	AP5
2	SLP_SUS#	AP4
efined und	SLP_WLAN# / GPIO29	AM5
efill	SM_DRAMRST#	AV15
	SM_PG_CNTL1	AV61
	SM_RCOMP0	AU60
	SM_RCOMP1	AV60
	SM_RCOMP2	AU61
	SM_VREF_CA	AP49
	SM_VREF_DQ0	AR51
ed un	SM_VREF_DQ1	AP51
defined un	SMBALERT# / GPIO11	AN2
	SMBCLK	AP2
	SMBDATA	AH1
	SML0ALERT# / GPIO60	AL2
	SMLOCLK	AN1
	SMLODATA	AK1
Jefined ut	SML1ALERT# / PCHHOT# / GPIO73	AU4
100	SML1CLK / GPI075	AU3
	SML1DATA / GPI074	AH3
	SPI_CLK	AA3
	SPI_CS0#	Y7
	SPI_CS1#	Y4
	SPI_CS2#	AC2
ed '	SPI_IO2	Y6
defin	SPI_IO3	AF1
Indefined	SPI_MISO	AA4
	SPI_MOSI	AA2
	SPKR / GPIO81	V2

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		essors—Proc	esso
	Signal Name	Ball #	
	SUS_STAT# / GPIO61	AG4	U
	SUSACK#	AK2	U
	SUSCLK / GPIO62	AE6	_
	SUSWARN# / SUSPWRDNACK / GPIO30	AV4	
	SYS_PWROK	AG2	U
	SYS_RESET#	AC3	U
	TD_IREF	B12	U
	TESTLOW_AK8	AK8	U
	TESTLOW_AL8	AL8	24
	TESTLOW_C34	C34	U
	TESTLOW_C35	C35	U
	THERMTRIP#	D60	U
	UART0_CTS# / GPIO94	G1	U U
S.	UARTO_RTS# / GPIO93	J2	U V
	UART0_RXD / GPIO91	J1	v
	UART0_TXD / GPIO92	K3 defi	V
	UART1_CTS# / GPIO3	J4	v
	UART1_RST# / GPIO2]3	V
e	UART1_RXD / GPIO0	К4	V
	UART1_TXD / GPIO1	G2	v v
	USB2n0	AN8	v
	USB2n1	AR7	V
	USB2n2	AR8	V
	USB2n3	AR10	V
	USB2n4	AM15	V
	USB2n5	AM13	V
6	USB2n6	AP11	V
	USB2n7	AR13	V
	USB2p0	AM8	v
	USB2p1	AT7 Intinued	V
		d	

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Signal Name	Ball #
USB2p2	AP8
USB2p3	AT10
USB2p4	AL15
USB2p5	AN13
USB2p6	AN11 0
USB2p7	AP13
USB3Rn1	G20
USB3Rn2	E18
USB3Rp1	H20
USB3Rp2	F18
USB3Tn1	C33
USB3Tn2	B33
USB3Tp1	B34
USB3Tp2	A33
USBRBIAS	AJ11
USBRBIAS#	AJ10
VCC	F59
vcc	AB57
VCC	AD57
VCC	AG57
VCC	C24
VCC	C28
VCC	C32
vcc	C36
VCC	C40
vcc	C44
vcc	C48
VCC	C52
VCC	C56
VCC	E23
VCC	E25
vcc	E27
VCC	E29
VCC	E31
VCC	E33
VCC	E35
	1

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Mobile 4th Generation Intel[®] Core[™] Processor Family, Mobile Intel[®] Pentium[®] Processor Family, and Mobile Intel[®] Celeron[®] Processor Family Datasheet - Volume 1 of 2 118

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	Signal Name	Ball #
	VCC	E37
ndefille	VCC	E39
	VCC	E41
	VCC	E43
ndefined unde	vcc	E45
d une	VCC	E47
sineu	VCC	E49
Je.	VCC	E51
	VCC	E53
	VCC	E55
	vcc	E57
	VCC	F24
undefined und	VCC	F28
, unc	VCC	F32
	VCC	F36
dell	VCC	F40
	VCC	F44
	VCC	F48
	vcc	F52
	vcc	F56
	VCC	G23
711	vcc	G25
ed u	VCC	G27
defin	VCC	G29
undefined un	VCC	G31
	VCC	G33
	VCC	G35
	VCC	G37
	VCC	G39
d undefined ut	vcc	G41
red	VCC	G43
defill	VCC	G45
une	VCC	G47
	VCC	G49
	VCC	G51
	VCC	G53

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inde			2111
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Signal Name	Ball #	Signal Name	Bal
VCC	G55	VCCCLK	J17
VCC	G57	VCCCLK	T21
VCC	H23	VCCCLK	R21
VCC	J23	VCCDSW3_3	AH10
VCC	K23	VCCHDA	AH14
VCC	К57	VCCHSIO	M9
VCC	L22	VCCHSIO	К9
VCC	M23	VCCHSIO	L10
VCC	M57	VCCIO_OUT	A59
VCC	P57	VCOMP_OUT	E20
VCC	U57	VCCRTC	AG10
VCC	W57	VCCSATA3PLL	B11
VCC_SENSE	E63	VCCSDIO	U8
VCC1_05	P9	VCCSDIO	Т9
VCC1_05	N8	VCCSPI	Y8
VCC1_05	AE8	VCCST	AC22
VCC1_05	AF22	VCCST	AE22
VCC1_05	H11	VCCST	AE23
VCC1_05	H15	VCCST_PWRGD	B59
VCC1_05	J11	VCCSUS3_3	AH11
VCC1_05	AG16	VCCSUS3_3	AA9
VCC1_05	AG17	VCCSUS3_3	AC9
VCC3_3	V8	VCCSUS3_3	AE20
VCC3_3	W9	VCCSUS3_3	AE21
VCC3_3	K14	VCCTS1_5	J15
VCC3_3	K16	VCCUSB3PLL	B18
VCCACLKPLL	A20	VDDQ	AH26
VCCAPLL	AA21	VDDQ	AJ31
VCCAPLL	W21	VDDQ	AJ33
VCCASW	AE9	VDDQ	AJ37
VCCASW	AF9	VDDQ	AN33
VCCASW	AG8	VDDQ	AP43
VCCASW	AG13	VDDQ	AR48
VCCASW	AG14	VDDQ	AY35
VCCCLK	J18	VDDQ	AY40
VCCCLK	K19	VDDQ	AY44
	continued		continue

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Signal Name	Ball #
VDDQ	AY50
VIDALERT#	L62
VIDSCLK	N63
VIDSOUT	L63
VR_EN	F60
VR_READY	C59
VSS	P62
VSS	D63
VSS	P22
VSS	N21
VSS	A11
VSS	A14
VSS	A18
VSS	A24
VSS	A28
VSS	A32
VSS	A36
VSS	A40
vss	A48
VSS	A52
VSS	A56
VSS	AA1
VSS	A44
VSS	AA58
VSS	AB10
VSS	AB20
VSS	AE5
VSS	AB22
VSS	AB7
VSS	AC61
VSS	AD3
VSS	AD63
VSS	AE10
VSS	AD21
VSS	AE58
	VDDQ VIDALERT# VIDSOUT VR_EN VR_READY VSS VSS </td

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Signal Name	Ball #	
VSS	C39	V
VSS	AF11	V
VSS	AF12	VS
VSS	AF14	V
VSS	AF15	VS
VSS	AF17	V
VSS	AF18	V
VSS	AG21	VS
VSS	AG23	V
VSS	AG1	V
VSS	AG11	V
VSS	AG60	VS
VSS	AG61	V
VSS	AG62	VS
VSS	AG63	VS
VSS	AH17	VS
VSS	AH19	VS
VSS	AH20	V
VSS	AH22	V
VSS	AH24	V
VSS	AH28	VS
VSS	AH30	VS
VSS	AH32	V
VSS	AH34	VS
VSS	AH36	V
VSS	AH38	V
VSS	AH40	V
VSS	AH42	V
VSS	AH44	V
VSS	AH49	V
VSS JNC	AH51	VS
VSS	AH53	VS
VSS	AH55	VS
VSS	AH57	VS
VSS	AJ13	V
VSS	AJ14	VS
C	ontinued	

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Signal Name	Ball #
VSS	AJ23
VSS	AJ25
VSS	AJ27
VSS	AJ29
VSS	AJ35
VSS	AJ39
vss	AJ41
VSS	AJ43
VSS	AJ45
VSS	AJ47
/SS	AJ50
VSS	AJ52
VSS	AJ54
VSS	AJ56
VSS	AJ58
vss	AJ60
/ss	AJ63
VSS	AK23
VSS	АКЗ
VSS	AK52
VSS	AL10
VSS	AL13
VSS	AL17
/ss	AL17 AL20
	AL20 AL22
vss vss	AL22 AL23
/SS	AL23 AL26
/SS	AL20 AL29
vss VSS	AL29 AL31
VSS	AL33
VSS	AL36
VSS	AL39
VSS	AL40
VSS	AL45
VSS	AL46
VSS	AL51

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Ball #

AU28 AU30 AU33

AU51 AU53 AU55 AU57 AU59

AV14 D62 AV16 AV20

AV24 AV28 AV33 AV34 AV36

AV39 AV41 AV43

AV46 AV49 AV51 AV55 AV59

AV8 AW16 AW24 AW33

AW35 AW37 AW4 AW40 AW42

AW44 AW47 continued... defined unde

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	Signal Name	Ball #
	VSS	AL52
	VSS	AL54
Jeffin	VSS	AL57
	VSS	AL60
	VSS	AL61
d une	VSS	AM1
sinec	VSS	AM17
nde	VSS	AM23
	VSS	AM31
	VSS	AM52
ndefined unde	vss de	AN17
	V33	AN23
4	VSS	AN31
+ uno	VSS	AN32
a undefined und	VSS	AN35
ndell	VSS	AN36
0.	VSS	AN39
	VSS	AN40
	VSS	AN42
	VSS	AN43
	VSS	AN45
	VSS	AN46
Jundefined un	VSS	AN48
defin	VSS	AN49
Un	VSS	AN51
	VSS	AN52
	VSS	AN60
	VSS	AN63
	VSS	AN7
	VSS	AP10
ad undefined ut	VSS	AP17
define	VSS	AP20
4 Une	VSS	AP22
	VSS	AP23
	VSS	AP26

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	Juli			un
	Signal Name	Ball #	Signal N	ame
	VSS	AP3	VSS	
	VSS	AP31	VSS	
	VSS	AP38	VSS	
	VSS	AP39	VSS	
	VSS	AP52	VSS	
	VSS	AP54	VSS	
	VSS	AP57	VSS	ي رير
	VSS	AR11	VSS	0
	VSS	AR15	VSS	
	VSS	AR17	VSS	
	VSS	AR23	VSS	
	VSS	AR31	VSS	
	VSS	AR33	VSS	
	VSS de	AR39	VSS	
	VSS	AP48	VSS	
211	VSS	AR49	VSS	20
	VSS	AR5	VSS	
	VSS	AR52	VSS	
	VSS	AT13	VSS	
	VSS	AT35	VSS	
	VSS	AT37	VSS	
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	VSS	AT42	VSS	
12	VSS	AT43	VSS	ed
26,	VSS	AT46	VSS	
	VSS	AT49	VSS	
	VSS	AT61	VSS	
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-	VSS	AU18	VSS	6
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undefined un Processor Ball and Signal Information

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efined undefine	Signal Name	Ball #
ined t	VSS	AW50
	VSS	AW51
	VSS	AW59
	VSS	AW60
	VSS	AY11
	VSS	AY16
	VSS	AY18
ude.	VSS	AY22
defined undefine	VSS	AY24
4efill.	VSS	AY26
	VSS	AY30
	VSS	AY33
	VSS	AY51
	VSS	AY53
	VSS	AY57
ndefined undefin	VSS	AY59
ed un	VSS	AY6
Jefine .	VSS	AY4
100	VSS	B20
	VSS	B24
	VSS	B26
	VSS	B28
	VSS	B32
detti	VSS	C38
Indefined undefin	VSS	B36
stine	VSS	B4
	VSS	B40
	VSS	B44
	VSS	C14
	VSS	B48
	VSS	B52
	VSS	B56
undefined undef	VSS	B60
	VSS	C11 0
nder	VSS	C18
O .	VSS	C20

	d undefined		
red undef	Processors—Proce		
Signal N	lame Ball #		
VSS	C25	VSS	
VSS	C27	VSS	
VSS	D12	VSS	
VSS	D14	VSS	
VSS	D18	VSS	
VSS	D21	VSS	
VSS	D23	VSS	
VSS	D25	VSS	
VSS	D26	VSS	
VSS	D27	VSS	
VSS	D29	VSS	
VSS	D2	VSS	
VSS	D30	VSS	
VSS	D31	VSS	
VSS	D33	VSS	
VSS	D34	VSS	
VSS	D35	VSS	
VSS	D37	VSS	
VSS	D38	VSS	
VSS	D39	VSS	
VSS	D41	VSS	
VSS	D42	VSS	
VSS	D43	VSS	
VSS	D45	VSS	
VSS	D46	VSS	
VSS	D47	VSS	
VSS	D49	VSS	
VSS	D50	VSS	
VSS	D51	VSS	
VSS	D53	VSS	
VSS	D54	VSS	
VSS	D55	VSS	
VSS	D57	VSS	
VSS	D59	VSS	
VSS	E11	VSS	
VSS	E17	VSS	
	continued		

Signal Name	Ball #
'SS	F42
'SS	F20
/SS	D5
/SS	F26
/SS	F30
/SS	F34
'ss	F38
'SS	G6
'SS	F46
/SS	F50
/SS	F54
/SS	F58
/SS	F61
/SS	G18
/SS	G22
/SS	G3
/SS	G5
/SS	G8
/SS	H13
/SS	H17
/SS	H57
/SS	J10
/SS	J22
rss 👌	J59
/SS	J63
/SS	К1
/SS	K12
/SS	R22
/SS	L13
/SS	L15
/SS	L17
/SS	L18
rss since	L20
/SS	L58
'SS	L61

 L61

 L7

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 VSS

 L7

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 antml:image>data:image/s3,anthropic-data-us-east-2/u/marker_images/sfishman-markermapper-09261351/de627b005214aa2cd061ae90f8275cfc.jpeg</antml:image>

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	VSS	M22	d unc
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	VSS	N3	nden
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	VSS	P59	define sineo
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Mobile 4th 0	Generation Intel [®] Core	e [™] Processor F	Family, Mobile Intel [®] Pentium [®] Processor Family, and Mobile Intel [®] Celeron [®]
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