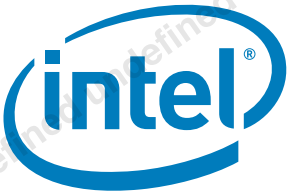

6th Generation Intel® Processor Families for H-Platforms

Datasheet, Volume 1 of 2

Supporting the 6th Generation Intel® Core™ Processor and Intel® Xeon® Processor E3-1500 v5 Product Families based on the H-Platform

July 2020

Order Number: 332986-011EN

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Revision History

Revision Number	Description	Revision Date
001	• Initial release	October 2015
002	• Updated Table 1-1, Processor Lines • Updated Table 7-11, DDR3L/-RS Signal Group DC Specifications • Updated Table 7-12, DDR4/-RS Signal Group DC Specifications	October 2015
003	• Updated Section 5.2 Notes • Updated Table 5-2 and Table 5-3	December 2015
004	• Updated Section 2.1, System Memory Interface • Updated note for Table 2-14, Hardware Accelerated Video Encode • Updated Table 2-16, GT2/3/4 Graphics Frequency (H-Processor) • Added Table 2-17, Embedded DisplayPort* (eDP*)/DDI Ports Availability • Updated Table 2-18, Display Resolutions and Link Bandwidth for Mulit-Stream Transport Calculations. • Added Table 2-19, Display Resolutions and Link Bandwidth for Multi-Stream Transport calculations • Added Section 2.5.7, Multiple Display Configurations (Single Channel DDR) • Added Table 2-26, HDCP DIsplay Supported Implications • Updated Section 3.3.2.1, Intel® Turbo Boost Technology 2.0 Frequency • Updated Table 5-2, TDP Specifications (H-Processor Line) • Updated Table 6-4, System Memory Reference and Compensation Signals • Updated Table 6-13, Power Sequencing Signals • Updated Table 6-14, Processor Power Rails Signals • Updated Table 7-1, Processor Power Rails • Updated Table 7-2, Processor IA Core (Vcc) Active and Idle Mode DC Voltage and Current Specifications • Updated Table 7-3, Processor Graphics ($Vccc_{GT}$ and Vcc_{GT-X}) Supply DC Voltage and Current Specifications • Updated Table 7-4, Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications • Updated Table 7-5, System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications • Added Section 7.2.1.6, Vcc_{OPC} DC Specifications • Added Section 7.2.1.7, Vcc_{EOPIO} DC Specifications • Added Section 7.2.1.8, VCC_OPC_1p8 DC Specifications • Updated Table 7-15, Processor PLL OC (Vcc_{PLL_OC}) Supply DC Voltage and Current Specifications • Updated Table 7-17, DDR/-RS Signal Group DC Specifications • Updated Table 7-20, embedded Display* (eDP*) Group DC Specifications • Updated Table 7-23, PECI DC Electrical Limits • Updated Table 8-1, Package Mechanical Attributes	January 2016

Revision Number	Description	Revision Date
005	• Added 6th Generation Intel® Core™ processor SKUs i5-6685R, i5-6585R, and i7-6785R • Updated Table 2-3, "Supported DDR4 Non-ECC SODIMM Module", Added Raw Card C (2GB) • Updated Table 2-5, "Supported DDR4 Memory Down Device Configurations". Added x16 DDP support. • Updated Section 2.1.2, "System Memory Timing Support". • Updated Section 2.5.7, "Multiple Display Configurations (Single Channel DDR)" • Updated Table 6-13, "Power Sequencing Signals", ZVM# signal. • Updated Table 7-2, "Processor IA Core (Vcc) Active and Idle Mode DC Voltage and Current Specifications", Note 3. • Updated Table 7-4, "Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications" • Updated Section 7.2.1.7, first paragraph. • Updated Table 7-10, "Processor EOPIO (Vcc_{EOPIO}) Supply DC Voltage and Current Specifications", $TOB_{VCCEOPIO}$ • Updated Table 7-12, "VCC Sustain (Vcc_{ST}) DC Voltage and Current Specifications", TOB_{ST} • Updated Table 7-13, "Vcc Sustain Gated (VccSTG) Supply DC Voltage and Current Specifications", TOB_{STG} • Updated Table 7-14, "Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications", TOB_{CCPLL} • Updated Table 7-15, "Processor PLL OC (VccPLL_OC) Supply DC Voltage and Current Specifications", TOB_{CCPLL_OC} • Minor edits throughout for clarity.	May 2016
006	• Added Intel® Xeon® processors E3-1585 v5, E3-1585L v5, E3-1565L v5, E3-1578L v5, E3-1558L v5 • Updated Table 5-2, "TDP Specifications". Added Quad Core GT4 35W with OPC • Updated Table 7-2, "Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications". Added H(35W) to I_{CCMAX} • Updated Table 7-3, "Processor Graphics (VccGT and VccGT-X) Supply DC Voltage and Current Specifications". Added H(35W) to $I_{CCMax\_GT}/I_{CCMax\_GTx}$	May 2016
007	• Minor updates for clarity • Added Chapter 9, Ballout Information	January 2017
08	• Updated Table 2-3, "Supported DDR4 ECC SODIMM Module Configurations" • Updated Table 2-4, Supported DDR4 Memory Down Module Configurations". Added notes.	August 2017
009	• Removed Section 2.4.1 "Operating Systems Support" • Added Section 1.1.1 "Operating Systems Support"	May 2018
010	• Updated Section 1.1.1 "Operating Systems Support"	August 2018
011	• Updated Chapter 7, Electrical Specifications Section 7.1.2 VCC Voltage Identification (VID)	July 2020

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1 Introduction

The 6th Generation Intel® Core™ processor family and Intel® Xeon® processor E3-1500 v5 product family for H-Platforms are a 64-bit, multi-core processor built on 14-nanometer process technology.

The H-Processor Lines are offered in a 2-Chip Platform and are connected to a discrete Intel® 100 Series Chipset Family Platform Controller Hub (PCH) chip on the motherboard. See the following figure.

Some of the processor SKUs are offered with On-Package Cache.

This document covers the H-Processor Line.

Table 1-1. H-Processor Lines

Processor Line[1]	Package	SKU Name	Base TDP	Processor IA Cores	Graphics Configuration	On Package Cache	Platform Type
H-Processor Line	BGA1440	SKL-H 35W	35W	2	GT2	N/A	2-Chip
		SKL-H 45W	45W	4	GT2	N/A	
		SKU-H 35W, 45W, 65W	35W, 45W, 65W		GT4	128MB	

Note:
1. Processor lines offering may change.

Throughout this document, the 6th Generation Intel® Core™ processor family and Intel® Xeon® processor E3-1500 v5 family may be referred to simply as "processor".

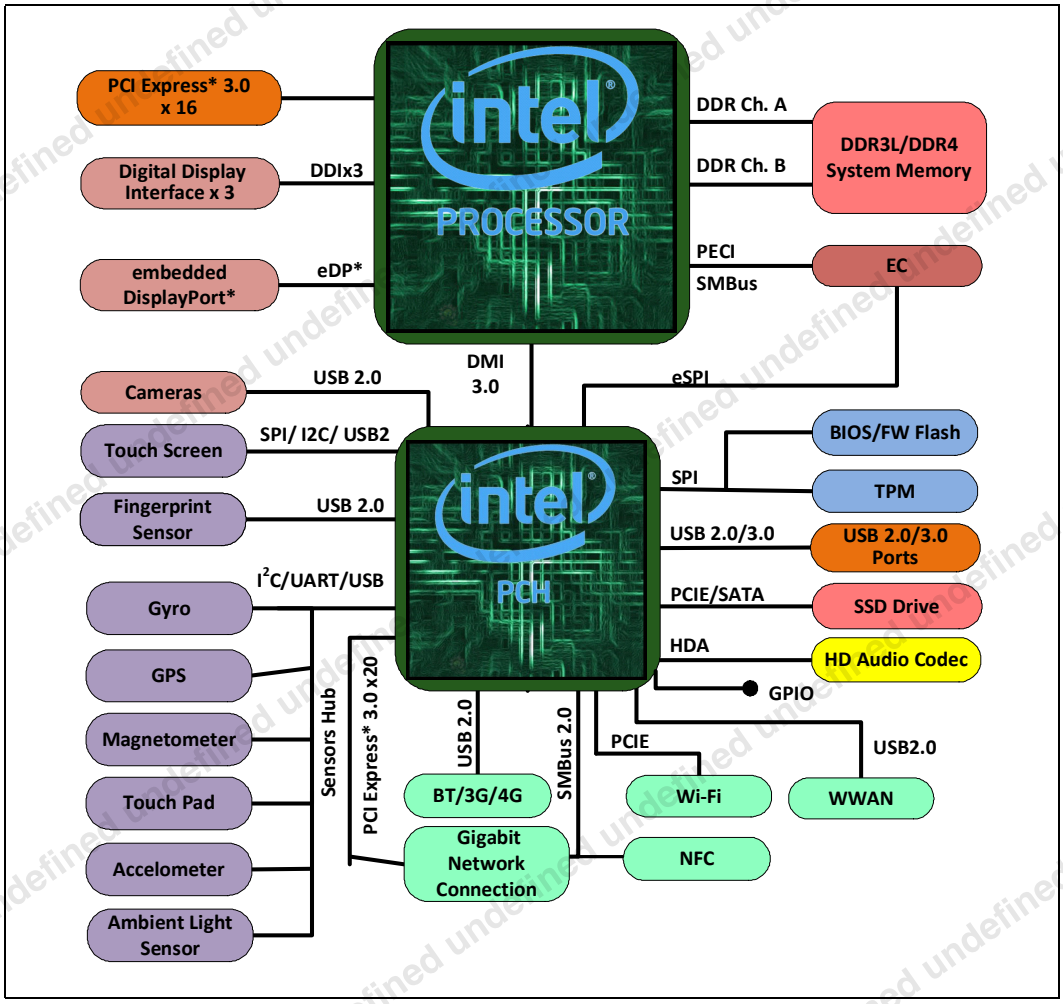
Throughout this document, the Intel® 100 Series Chipset Family Platform Controller Hub (PCH) chip may be referred to simply as "PCH".

This document is for the following SKUs:

- 6th Generation Intel® Core™ processor family H-Processors
  - i7-6920HQ, i7-6820HQ, i7-6820HK, i7-6700HQ, i5-6440HQ, i5-6300HQ, i3-6100H, i7-6970HQ, i7-6870HQ, i7-6770HQ, i5-6350HQ, i5-6685R, i5-6585R, i7-6785R
- Intel® Xeon® processor E3-1500 v5 product family H-Processors
  - E3-1575M v5, E3-1545M v5, E3-1515M v5, E3-1535M v5, E3-1505M v5, E3-1585 v5, E3-1585L v5, E3-1565L v5, E3-1578L v5, E3-1558L v5

Not all processor interfaces and features are present in all SKUs. For details, refer to the Specification Update.

Figure 1-1. H-Processor Line Platforms



1.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT)
- Intel® Active Management Technology 11.0 (Intel® AMT 11.0)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® Advanced Vector Extensions 2 (Intel® AVX2)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction
- Intel® Secure Key
- Intel® Transactional Synchronization Extensions (Intel® TSX-NI)
- PAIR – Power Aware Interrupt Routing
- SMEP – Supervisor Mode Execution Protection
- Intel® Boot Guard
- On-package Cache Memory
- Intel® Software Guard Extensions (Intel® SGX)
- Intel® Memory Protection Extensions (Intel® MPX)
- Intel® Processor Trace

Note: The availability of the features may vary between processor SKUs.

Refer to Chapter 3 for more information.

1.1.1 Operating Systems Support

Processor Line	Windows* 10 64-bit	Windows* 8.1 64-bit	Windows* 7 64- & 32-bit	OS X	Linux* OS	Chrome* OS
H-Processor Line	Yes	Yes	Yes	Yes	Yes	No

1.2 Power Management Support

1.2.1 Processor Core Power Management

- Full support of ACPI C-states as implemented by the following processor C-states:
  - C0, C1, C1E, C3, C6, C7, C8, C9, C10
- Enhanced Intel SpeedStep® Technology

Refer to Section 4.2 for more information.

1.2.2 System Power Management

- S0/S0ix, S3, S4, S5

Refer to Chapter 4, "Power Management" for more information.

1.2.3 Memory Controller Power Management

- Disabling Unused System Memory Outputs
- DRAM Power Management and Initialization
- Initialization Role of CKE
- Conditional Self-Refresh
- Dynamic Power Down
- DRAM I/O Power Management
- DDR Electrical Power Gating (EPG)
- Power training

Refer to Section 4.3 for more information.

1.2.4 Processor Graphics Power Management

1.2.4.1 Memory Power Savings Technologies

- Intel® Rapid Memory Power Management (Intel® RMPM)
- Intel® Smart 2D Display Technology (Intel® S2DDT)

1.2.4.2 Display Power Savings Technologies

- Intel® (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* port
- Intel® Automatic Display Brightness
- Smooth Brightness
- Intel® Display Power Saving Technology (Intel® DPST 6)
- Panel Self-Refresh 2 (PSR 2)
- Low Power Single Pipe (LPSP)

1.2.4.3 Graphics Core Power Savings Technologies

- Intel® Graphics Dynamic Frequency
- Intel® Graphics Render Standby Technology (Intel® GRST)
- Dynamic FPS (Intel® DFPS)

Refer to Section 4.6 for more information.

1.3 Thermal Management Support

- Digital Thermal Sensor
- Intel® Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS
- Intel® Turbo Boost Technology 2.0 Power Control

Refer to Chapter 5, "Thermal Management" for more information.

1.4 Package Support

The processor is available in the following packages:

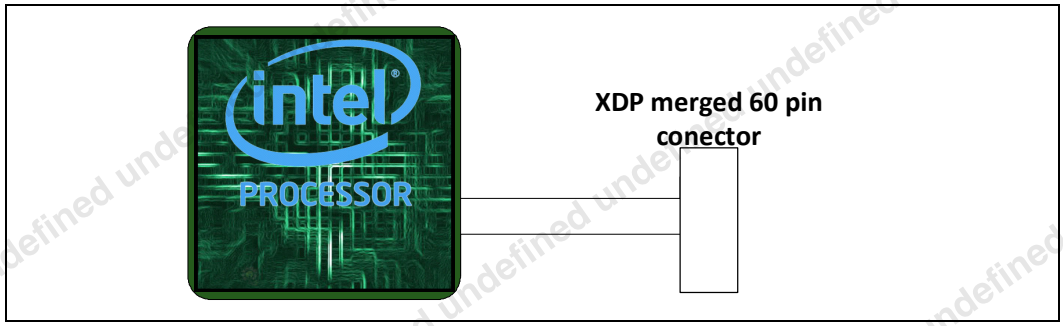
- A 42 mm x 28 mm BGA package (BGA1440) for H-processor line

1.5 Processor Testability

An XDP on-board connector is a must to enable the processor full debug capabilities. For the processor SKUs, a merged XDP connector is highly recommended to enable lower C-state debug.

Note: When separate XDP connectors will be used at C8–C10 states, the processor will need to be waked up using the PCH.

Figure 1-2. Merged XDP Connector for Processor and PCH



The processor includes boundary-scan for board and system level testability.

1.6 Terminology

Table 1-2. Terminology (Sheet 1 of 3)

Term	Description
4K	Ultra High Definition (UHD)
AES	Advanced Encryption Standard
AGC	Adaptive Gain Control
BLT	Block Level Transfer
BPP	Bits per pixel
CDR	Clock and Data Recovery
CTLE	Continuous Time Linear Equalizer
DDI	Digital Display Interface for DP or HDMI/DVI
DDR3	Third-generation Double Data Rate SDRAM memory technology
DDR3L/RS	DDR3 Low Voltage Reduced Standby Power
DDR4	Fourth-Generation Double Data Rate SDRAM Memory Technology
DFE	decision feedback equalizer
DMA	Direct Memory Access
DMI	Direct Media Interface
DP	DisplayPort*
DTS	Digital Thermal Sensor
ECC	Error Correction Code - used to fix DDR transactions errors
eDP*	embedded DisplayPort*
EU	Execution Unit in the Processor Graphics
GSA	Graphics in System Agent
HDCP	High-bandwidth Digital Content Protection
HDMI*	High Definition Multimedia Interface
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® DPST	Intel Display Power Saving Technology
Intel® PTT	Intel Platform Trust Technology
Intel® TSX-NI	Intel Transactional Synchronization Extensions
Intel® TXT	Intel Trusted Execution Technology
Intel® VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
ISP	Image Signal Processor
LFM	Low Frequency Mode. corresponding to the Enhanced Intel SpeedStep® Technology's lowest voltage/frequency pair. It can be read at MSR CEh [47:40].
LLC	Last Level Cache

Table 1-2. Terminology (Sheet 2 of 3)

Term	Description
LPM	Low-Power Mode.The LPM Frequency is less than or equal to the LFM Frequency. The LPM TDP is lower than the LFM TDP as the LPM configuration limits the processor to single thread operation
LPSP	Low-Power Single Pipe
MCP	Multi Chip Package - includes the processor and the PCH. In some SKU's it might have additional On-Package Cache.
LSF	Lowest Supported Frequency.This frequency is the lowest frequency where manufacturing confirms logical functionality under the set of operating conditions.
MFM	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].
MLC	Mid-Level Cache
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved balls/lands, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
PAG	Platform Power Architecture Guide (formerly PDDG)
PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features. The PCH may also be referred as "chipset".
PECI	Platform Environment Control Interface
PEG	PCI Express Graphics
PL1, PL2, PL3	Power Limit 1, Power Limit 2, Power Limit 3
Processor	The 64-bit multi-core component (package)
Processor Core	The term "processor core" refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the LLC.
Processor Graphics	Intel Processor Graphics
PSR	Panel Self-Refresh
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SODIMM.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDP	Scenario Design Power. The Power consumed by a typical scenario. For more information, refer to the *Scenario Design Power (SDP) Implementation Considerations* document (see Related Documents section).
SGX	Software Guard Extension
SHA	Secure Hash Algorithm
SSC	Spread Spectrum Clock
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material), the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
STR	Suspend to RAM
TAC	Thermal Averaging Constant
TCC	Thermal Control Circuit
TDP	Thermal Design Power
TTV TDP	Thermal Test Vehicle TDP

Table 1-2. Terminology (Sheet 3 of 3)

Term	Description
V_{CC}	Processor core power supply
V_{CCGT}	Processor Graphics Power Supply
V_{CCIO}	I/O Power Supply
V_{CCSA}	System Agent Power Supply
V_{CCST}	Vcc Sustain Power Supply
V_{DDQ}	DDR Power Supply
VLD	Variable Length Decoding
VPID	Virtual Processor ID
V_{SS}	Processor Ground
OPC	On Package Cache

1.7 Related Documents

Table 1-3. Related Documents

Document	Document Number/Location
6th Generation Intel® Processor Datasheet for H-Platforms, Volume 2 of 2	332987
6th Generation Intel® Processor Family Specification Update	332689
Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH), Volume 1 of 2	332690
Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH), Volume 2 of 2	332691
Advanced Configuration and Power Interface 3.0	http://www.acpi.info/
DDR3 SDRAM Specification	http://www.jedec.org
LPDDR3 Specification	http://www.jedec.org
DDR4 Specification	http://www.jedec.org
High Definition Multimedia Interface specification revision 1.4	http://www.hdmi.org/manufacturer/specification.aspx
Embedded DisplayPort* Specification revision 1.4	http://www.vesa.org/vesa.standards/
DisplayPort* Specification revision 1.2	http://www.vesa.org/vesa.standards/
PCI Express* Base Specification Revision 3.0	http://www.pcisig.com/specifications
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm

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2 Interfaces

2.1 System Memory Interface

- Two channels ofLPDDR3 and DDR4 memory with a maximum of two DIMMs per channel. DDR technologies, number of DIMMs per channel, number of ranks per channel are SKU dependent.
- UDIMM, SODIMM, and Memory Down support (based on SKU)
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- LPDDR3 I/O voltage of 1.2V
- DDR4 I/O Voltage of 1.2V
- 64-bit wide channels
- ECC/Non-ECC UDIMM and SODIMM DDR4 support (based on SKU)
- Theoretical maximum memory bandwidth of:
  - — 20.8 GB/s in dual-channel mode assuming 1333 MT/s
  - — 25.0 GB/s in dual-channel mode assuming 1600 MT/s
  - — 29.1 GB/s in dual-channel mode assuming 1866 MT/s
  - — 33.3 GB/s in dual-channel mode assuming 2133 MT/s

Note: Memory down of all technologies (DDR4/LPDDR3) should be implemented homogeneously, which means that all DRAM devices should be from the same vendor and have the same part number. Implementing a mix of DRAM devices may cause serious signal integrity and functional issues.

Note: If the H-processor line memory interface is configured to one DIMM per Channel, the processor can use either of the DIMMs, DIMM0, or DIMM1, signals CTRL[1:0] or CTRL[3:2].

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports LPDDR3 and DDR4 protocols with two independent, 64-bit wide channels.

Table 2-1. Processor DRAM Support Matrix

Processor Line	DPC[1]	DDR3L/-RS	DDR4	LPDDR3
H-processor line	2	N/A	1866/2133	1600/1866

Notes:
1. DPC = DIMM Per Channel.
2. Increasing the LPDDR3 rate to 1866 MT/s may lead to TDP power penalty up to 320mW, and 5-7% battery life impact.
3. Increasing the LPDDR3 rate to 1866 MT/s may lead to TDP power penalty up to 300mW, and 5-7% battery life impact.
4. Increasing the DDR4 rate to 2133 MT/s may lead to TDP power penalty up to 400mW, and 5-10% battery life impact.

- DDR4 Data Transfer Rates:
  - 1866 MT/s (PC4-1866)
  - 2133 MT/s (PC4-2133)
- LPDDR3 Data Transfer Rates:
  - 1600 MT/s
  - 1866 MT/s

DDR4 SODIMM/UDIMM Modules:

- Standard 4-Gb and 8-Gb technologies and addressing are supported for x8 and x16 devices.

There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

- DDR4 Memory Down: Single rank x8, x16 (based on SKU)
- LPDDR3 Memory Down: Single and Dual Rank x32/x64 (based on SKU)

Table 2-2. Supported DDR4 Non-ECC SODIMM Module Configurations (H-Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	4GB	4Gb	512M x 8	8	1	15/10	16	8K
A	8GB	8Gb	1024M x 8	8	1	16/10	16	8K
B	8GB	4Gb	512M x 8	16	2	15/10	16	8K
B	16GB	8Gb	1024M x 8	16	2	16/10	16	8K
C	2GB	4Gb	256M x 16	4	1	15/10	8	8K
C	4GB	8Gb	512M x 16	4	1	16/10	8	8K
E	8GB	4Gb	512M x 8	16	2	15/10	16	8K
E	16GB	8Gb	1024M x 8	16	2	16/10	16	8K

Table 2-3. Supported DDR4 ECC SODIMM Module Configurations (H-Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
D	4GB	4Gb	512M x 8	9	1	15/10	16	8K
D	8GB	8Gb	1024M x 8	9	1	16/10	16	8K
G	8GB	4Gb	512M x 8	18	2	15/10	16	8K
G	16GB	8Gb	1024M x 8	18	2	16/10	16	8K
H	8GB	4Gb	512M x 8	18	2	15/10	16	8K
H	16GB	8Gb	1024M x 8	18	2	16/10	16	8K

Table 2-4. Supported DDR4 Memory Down Module Configurations (H-Processor Line)

Max. System Capacity	PKG Type (Dies bits x PKG bits)	DRAM Organization /PKG Type	PKG Density	Die Density	Dies Per Channel	Rank Per Channel	PKGs Per channel	Physical Device Rank	Banks Inside DRAM	Page Size
16GB	SDP 8x8	512M x 8	4Gb	4Gb	16	2	16	1	16	8K
32GB	SDP 8x8	1024M x 8	8Gb	8Gb	16	2	16	1	16	8K
4GB	SDP 16x16	256M x 16	4Gb	4Gb	4	1	8	1	8	8K
8GB	SDP 16x16	512M x 16	8Gb	8Gb	4	1	8	1	8	8K
16GB	DDP 8x16	1024M x 16	16GB	8GB	8	1	4	1	16	8k

Notes:
1. The maximum system capacity for x8 devices refers to 2 channels, 2 ranks systems.
2. The maximum system capacity for x16 devices refers to 2 channels, 1 rank systems.

2.1.1.1 LPDDR3 Supported Memory Devices

Table 2-5. Supported LPDDR3 x32 DRAMs Configurations (H-Processor Line)

Max. System Capacity	PKG Type (Dies bits x PKG bits)	DRAM Organization /PKG Type	Die Density	PKG Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size
2 GB	SDP 32x32	128Mx32	4 Gb	4Gb	2	2	1	8	8K
4 GB	DDP 32x32	256Mx32	4 Gb	8Gb	4	2	2	8	8K
8 GB	QDP 16x32	512Mx32	4 Gb	16Gb	8	2	2	8	8K
4 GB	SDP 32x32	256Mx32	8 Gb	8Gb	2	2	1	8	8K
8 GB	DDP 32x32	512Mx32	8 Gb	16Gb	4	2	2	8	8K
16 GB	QDP 16x32	1024Mx32	8 Gb	32Gb	8	2	2	8	8K

Notes:
1. x32 devices are 178 balls.
2. SDP = Single Die Package, DDP = Dual Die Package, QDP = Quad Die Package

2.1.2 System Memory Timing Support

The IMC supports the following DDR Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes:
  - — 1N indicates a new DDR4 command may be issued every clock
  - — 2N indicates a new DDR4 command may be issued every 2 clocks

Table 2-6. DRAM System Memory Timing Support

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC (SODIMM Only)	CMD Mode
DDR4	1866	12/13/14	12/13/14	12/13/14	10/12/12	1 or 2	1N/2N
	2133	14/15/16	14/15/16	14/15/16	11/14/14	1 or 2	1N/2N
LPDDR3	1333	10	12	12	7	1	0.5N
	1600	12	15	15	8	1	0.5N

Table 2-7. DRAM System Memory Timing Support (LPDDR3)

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRPpb[1] (tCK)	tRPab[2] (tCK)	CWL (tCK)
LPDDR3	1333	10	12	12	14	8
	1600	12	15	15	18	9
	1866	14	17	17	20	11
	2133	16	20	20	23	13

Notes:
1. tRPpb = Row Precharge typical time (single bank)
2. tRPab = Row Precharge typical time (all banks)

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the DDR Schema and DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

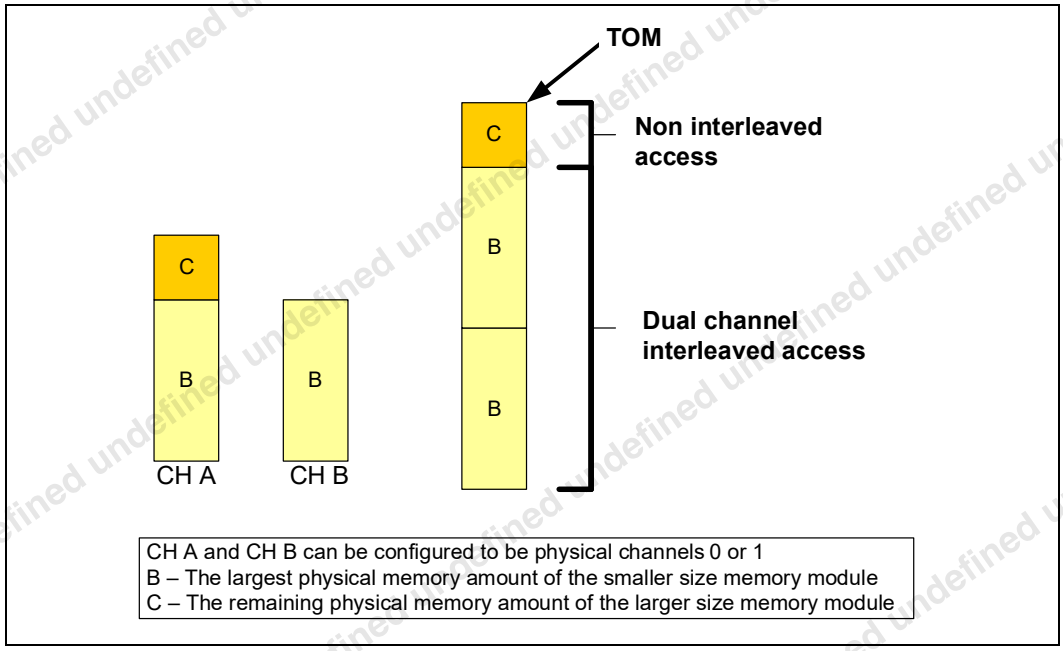
In this mode, all memory cycles are directed to a single channel. Single-Channel mode is used when either the Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

Figure 2-1. Intel® Flex Memory Technology Operations



Dual-Channel Symmetric Mode (Interleaved Mode)

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For Dual-Channel modes both channels must have a DIMM connector populated. For Single-Channel mode, only a single channel can have a DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.

2.1.7 ECC H-Matrix Syndrome Codes

Table 2-8. ECC H-Matrix Syndrome Codes (Sheet 1 of 2)

Syndrome Value	Flipped Bit	Syndrome Value	Flipped Bit	Syndrome Value	Flipped Bit	Syndrome Value	Flipped Bit
0				No Error			
1	64	37	26	81	2	146	53
2	65	38	46	82	18	148	4
4	66	41	61	84	34	152	20

Table 2-8. ECC H-Matrix Syndrome Codes (Sheet 2 of 2)

Syndrome Value	Flipped Bit	Syndrome Value	Flipped Bit	Syndrome Value	Flipped Bit	Syndrome Value	Flipped Bit
7	60	42	9	88	50	161	49
8	67	44	16	97	21	162	1
11	36	47	23	98	38	164	17
13	27	49	63	100	54	168	33
14	3	50	47	104	5	176	44
16	68	52	14	112	52	193	8
19	55	56	30	128	71	194	24
21	10	64	70	131	22	196	40
22	29	67	6	133	58	200	56
25	45	69	42	134	13	208	19
26	57	70	62	137	28	224	11
28	0	73	12	138	41	241	7
31	15	74	25	140	48	242	31
32	69	76	32	143	43	244	59
35	39	79	51	145	37	248	35

Notes:
1. All other syndrome values indicate unrecoverable error (more than one error).
2. This table is relevant only for H-Processor ECC supported SKUs.

2.1.8 DDR I/O Interleaving

The processor supports I/O interleaving, which has the ability to swap DDR bytes for routing considerations. BIOS configures the I/O interleaving mode before DDR training.

There are 2 supported modes:

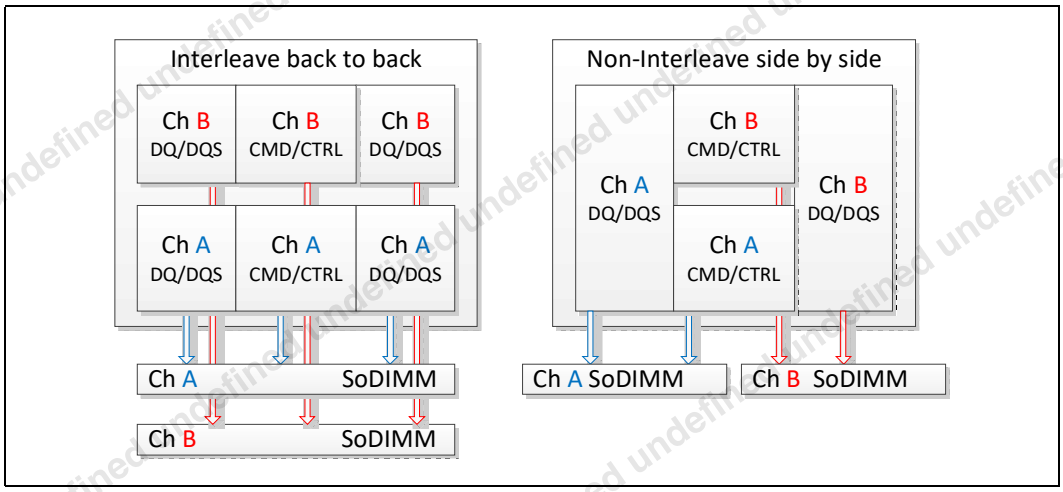
- Interleave (IL)
- Non-Interleave (NIL)

The following table and figure describe the pin mapping between the IL and NIL modes.

Table 2-9. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

IL		NIL	
Channel	**Byte**	**Channel**	**Byte**
DDR0	Byte0	DDR0	Byte0
DDR0	Byte1	DDR0	Byte1
DDR0	Byte2	DDR0	Byte4
DDR0	Byte3	DDR0	Byte5
DDR0	Byte4	DDR1	Byte0
DDR0	Byte5	DDR1	Byte1
DDR0	Byte6	DDR1	Byte4
DDR0	Byte7	DDR1	Byte5
DDR1	Byte0	DDR0	Byte2
DDR1	Byte1	DDR0	Byte3
DDR1	Byte2	DDR0	Byte6
DDR1	Byte3	DDR0	Byte7
DDR1	Byte4	DDR1	Byte2
DDR1	Byte5	DDR1	Byte3
DDR1	Byte6	DDR1	Byte6
DDR1	Byte7	DDR1	Byte7

Figure 2-2. Interleave (IL) and Non-Interleave (NIL) Modes Mapping



2.1.9 Data Swapping

By default, the processor supports on-board data swapping in two manners (for all segments and DRAM technologies):

- byte (DQ+DQS) swapping between bytes in the same channel.
- bit swapping within specific byte.

2.1.10 DRAM Clock Generation

Every supported rank has a differential clock pair. There are a total of four clock pairs driven directly by the processor to DRAM.

2.1.11 DRAM Reference Voltage Generation

The memory controller has the capability of generating the LPDDR3 and DDR4 Reference Voltage (VREF) internally for both read and write operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced training procedures in order to provide the best voltage to achieve the best signal margins.

2.1.12 Data Swizzling

H-processor line 4+2 does not have die-to-package DDR swizzling.

Table 2-10. H-Processor Line 4+4e Die-to-Package DDR Data Swizzling (Sheet 1 of 2)

Pkg Pin#	Package Pin/Net Name	Die bump
W8	DDRDQ_IL15_NIL13[0]	XXDDRDQ_IL15_NIL13[6]
W7	DDRDQ_IL15_NIL13[1]	XXDDRDQ_IL15_NIL13[7]
V10	DDRDQ_IL15_NIL13[2]	XXDDRDQ_IL15_NIL13[1]
V11	DDRDQ_IL15_NIL13[3]	XXDDRDQ_IL15_NIL13[0]
W11	DDRDQ_IL15_NIL13[4]	XXDDRDQ_IL15_NIL13[4]
W10	DDRDQ_IL15_NIL13[5]	XXDDRDQ_IL15_NIL13[5]
V7	DDRDQ_IL15_NIL13[6]	XXDDRDQ_IL15_NIL13[3]
V8	DDRDQ_IL15_NIL13[7]	XXDDRDQ_IL15_NIL13[2]
R11	DDRDQ_IL16_NIL16[0]	XXDDRDQ_IL16_NIL16[7]
P11	DDRDQ_IL16_NIL16[1]	XXDDRDQ_IL16_NIL16[1]
P7	DDRDQ_IL16_NIL16[2]	XXDDRDQ_IL16_NIL16[2]
R8	DDRDQ_IL16_NIL16[3]	XXDDRDQ_IL16_NIL16[0]
R10	DDRDQ_IL16_NIL16[4]	XXDDRDQ_IL16_NIL16[3]
P10	DDRDQ_IL16_NIL16[5]	XXDDRDQ_IL16_NIL16[5]
R7	DDRDQ_IL16_NIL16[6]	XXDDRDQ_IL16_NIL16[6]
P8	DDRDQ_IL16_NIL16[7]	XXDDRDQ_IL16_NIL16[4]
L11	DDRDQ_IL17_NIL17[0]	XXDDRDQ_IL17_NIL17[7]
M11	DDRDQ_IL17_NIL17[1]	XXDDRDQ_IL17_NIL17[1]

Table 2-10. H-Processor Line 4+4e Die-to-Package DDR Data Swizzling (Sheet 2 of 2)

Pkg Pin#	Package Pin/Net Name	Die bump
L7	DDRDQ_IL17_NIL17[2]	XXDDRDQ_IL17_NIL17[2]
M8	DDRDQ_IL17_NIL17[3]	XXDDRDQ_IL17_NIL17[0]
L10	DDRDQ_IL17_NIL17[4]	XXDDRDQ_IL17_NIL17[3]
M10	DDRDQ_IL17_NIL17[5]	XXDDRDQ_IL17_NIL17[5]
M7	DDRDQ_IL17_NIL17[6]	XXDDRDQ_IL17_NIL17[6]
L8	DDRDQ_IL17_NIL17[7]	XXDDRDQ_IL17_NIL17[4]

2.2 PCI Express* Graphics Interface (PEG)

Note: The processor's PCI Express* interface is present only in 2-Chip platform processors.

This section describes the PCI Express* interface capabilities of the processor. See the *PCI Express Base* Specification 3.0* for details on PCI Express*.

2.2.1 PCI Express* Support

The processor's PCI Express* interface is a 16-lane (x16) port that can also be configured as multiple ports at narrower widths (see Table 2-11, Table 2-12).

The processor supports the configurations shown in the following table.

Table 2-11. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			Config. Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. For CFG bus further details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.
4. For Reversal lanes, For example:
   - When using 1x8, the 8 lane device must use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
   - When using 1x4, the 4 lane device must use lanes 12:15, so lane 15 will be connected to lane 0 of the Device.
   - When using 1x2, the 4 lane device must use lanes 14:15, so lane 15 will be connected to lane 0 of the Device.

The processor supports the following:

- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset.
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0: DMI -> PCI Express* Port 0
- 64-bit downstream address format, but the processor never generates an address above 512 GB (Bits 63:39 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 512 GB (addresses where any of Bits 63:39 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 512 GB will be dropped.
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- PCI Express* reference clock is 100-MHz differential clock
- Power Management Event (PME) functions
- Dynamic width capability
- Message Signaled Interrupt (MSI and MSI-X) messages
- Lane reversal
- Full Advance Error Reporting (AER) and control capabilities

The following table summarizes the transfer rates and theoretical bandwidth of PCI Express* link.

Table 2-12. PCI Express* Maximum Transfer Rates and Theoretical Bandwidth

PCI Express* Gen	Encoding	Maximum Transfer Rate [GT/s]	Theoretical Bandwidth [GB/s]				
			x1	x2	x4	x8	x16
Gen 1	8b/10b	2.5	0.25	0.5	1.0	2.0	4.0
Gen 2	8b/10b	5	0.5	1.0	2.0	4.0	8.0
Gen 3	128b/130b	8	1.0	2.0	3.9	7.9	15.8

Note: The processor has limited support for Hot-Plug, for details refer to Section 4.4.

2.2.2 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express* configuration uses standard mechanisms as defined in the PCI Plug and-Play specification. The processor PCI Express* ports support Gen 3.
At 8 GT/s, Gen 3 operation results in twice as much bandwidth per lane as compared to Gen 2 operation. The 16 lanes port can operate at 2.5 GT/s, 5 GT/s, or 8 GT/s.

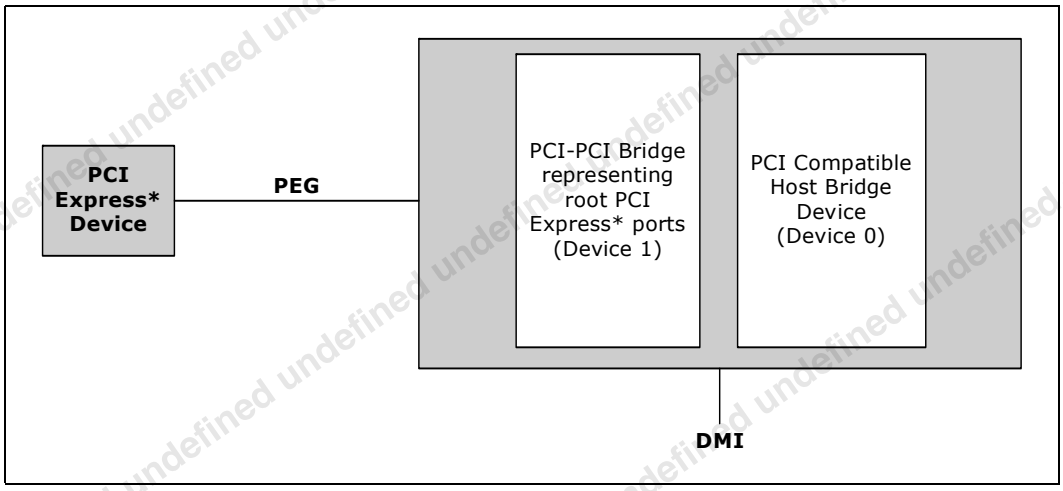
Gen 3 PCI Express* uses a 128b/130b encoding which is about 23% more efficient than the 8b/10b encoding used in Gen 1 and Gen 2.

The PCI Express* architecture is specified in three layers – Transaction Layer, Data Link Layer, and Physical Layer. See the *PCI Express Base Specification 3.0* for details of PCI Express* architecture.

2.2.3 PCI Express* Configuration Mechanism

The PCI Express* (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 2-3. PCI Express* Related Register Structures in the Processor



PCI Express* extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the conventional PCI specification. PCI Express* configuration space is divided into a PCI-compatible region (that consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express* region (that consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express* configuration access mechanism described in the PCI Express* Enhanced Configuration Mechanism section.

The PCI Express* Host Bridge is required to translate the memory-mapped PCI Express* configuration space accesses from the host processor to PCI Express* configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the PCI Express Base Specification for details of both the PCI-compatible and PCI Express* Enhanced configuration mechanisms and transaction rules.

2.2.4 PCI Express* Equalization Methodology

The equalization of link requires equalization for both TX and RX sides for the processor and for the End point device.

Adjusting transmitter and receiver of the lanes is done to improve signal reception quality and for improving link robustness and electrical margin.

The link timing margins and voltage margins are strongly dependent on equalization of the link.

The processor supports the following:

- Full TX Equalization: Three Taps Linear Equalization (Pre, Current and Post cursors), with FS/LF (Full Swing /Low Frequency) 24/8 values respectively.
- Full RX Equalization and acquisition for: AGC (Adaptive Gain Control), CDR (Clock and Data Recovery), adaptive DFE (decision feedback equalizer) and adaptive CTLE peaking (continuous time linear equalizer).
- Full adaptive phase 3 EQ compliant with PCI Express* Gen 3 specification

See the *PCI Express* Base Specification 3.0* for details on PCI Express* equalization.

2.3 Direct Media Interface (DMI)

Note: The DMI interface is only present in 2-Chip platform processors.

Direct Media Interface (DMI) connects the processor and the PCH.

Main characteristics:

- 4 lanes Gen 3 DMI support
- 8 GT/s point-to-point DMI interface to PCH
- DC coupling - no capacitors between the processor and the PCH
- PCH end-to-end lane reversal across the link
- Half-Swing support (low-power/low-voltage)

Note: Only DMI x4 configuration is supported.

Note: Polarity Inversion on DMI Link is not allowed on both sides of the processor and the PCH.

2.3.1 DMI Error Flow

DMI can only generate SERR in response to errors; never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

2.3.2 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This link behavior is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Processor Graphics

The processor graphics is based on GEN 9 (generation 9) graphics core architecture that enables substantial gains in performance and lower-power consumption over prior generations. GEN 9 architecture supports up to 72 Execution Units (EUs) with On-Package Cache depending on the processor SKU.

The new processor graphics architecture delivers high dynamic range of scaling to address segments spanning low power to high power, increased performance per watt, support for next generation of APIs and extends heterogeneous programmability with IA core/GPU and Shared Virtual memory (SVM). GEN 9 scalable architecture is partitioned by usage domains along Render/Geometry, Media, and Display. The architecture also delivers very low-power video playback and next generation analytics and filters for imaging related applications. The new Graphics Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and "PCI-like" traffic in and out.

The display engine supports the latest display standards such as eDP* 1.3, DP* 1.2, HDMI* 1.4, HW support for blend, scale, rotate, compress, high PPI support, and advanced SRD2 display power management.

2.4.1 API Support (Windows*)

- Direct3D* 12, Direct3D* 11.3, Direct3D* 11.2, Direct3D 11.1, Direct3D 9, Direct3D 10, Direct2D
- OpenGL* 4.4
- OpenCL* 2.1, OpenCL* 2.0, OpenCL* 1.2

Direct3D* 11.x extensions:

- PixelSync, InstantAccess.

Gen 9 architecture delivers hardware acceleration of Direct X* 11 Render pipeline comprising of the following stages: Vertex Fetch, Vertex Shader, Hull Shader, Tesselation, Domain Shader, Geometry Shader, Rasterizer, Pixel Shader, Pixel Output. The Direct X* 12 API is supported at feature level 12_1.

2.4.2 Media Support (Intel® QuickSync & Clear Video Technology HD)

GEN 9 implements multiple media video codecs in hardware as well as a rich set of image processing algorithms.

Note: All supported media codecs operate on 8 bpc, YCbCr 4:2:0 video profiles.

2.4.2.1 Hardware Accelerated Video Decode

GEN 9 implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW decode is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2)
- Direct3D11 Video API
- Intel Media SDK
- MFT (Media Foundation Transform) filters.

GEN 9 supports full HW accelerated video decoding for AVC/VC1/MPEG2/HEVC/VP8/JPEG.

Note: HEVC – 8 bit support.

Table 2-13. Hardware Accelerated Video Decoding

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	Main High	1080p
VC1/WMV9	Advanced Main Simple	L3 High Simple	3840x3840
AVC/H264	High Main MVC & stereo	L5.1	2160p(4K)
VP8	0	Unified level	1080p
JPEG/MJPEG	Baseline	Unified level	16k x16k
HEVC/H265	Main	L5.1	2160(4K)
VP9*	0 (4:2:0 Chroma 8-bit)	Unified level	ULT, 4k 24fps @15Mbps ULX, 1080p 30fps @ 10Mbps

Expected performance:

- More than 16 simultaneous decode streams @ 1080p.

Note: Actual performance depends on the processor SKU, content bit rate, and memory frequency. Hardware decode for H264 SVC is not supported.

2.4.2.2 Hardware Accelerated Video Encode

GEN 9 implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW encode is exposed by the graphics driver using the following APIs:

- Intel Media SDK
- MFT (Media Foundation Transform) filters

GEN 9 supports full HW accelerated video encoding for AVC/MPEG2/HEVC/VP8/JPEG.

Table 2-14. Hardware Accelerated Video Encode

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	High	1080p
AVC/H264	Main High	L5.1	2160p(4K)
VP8	Unified profile	Unified level	—
JPEG	Baseline	—	16Kx16K
HEVC/H265	Main	L5.1	2160p(4K)
VP9	Support 8 bits 4:2:0 BT2020 may be obtained the pre/ post processing	—	—

Note: Hardware encode for H264 SVC is not supported.

2.4.2.3 Hardware Accelerated Video Processing

There is hardware support for image processing functions such as De-interlacing, Film cadence detection, Advanced Video Scaler (AVS), detail enhancement, image stabilization, gamut compression, HD adaptive contrast enhancement, skin tone enhancement, total color control, Chroma de-noise, SFC pipe (Scalar and Format Conversion), memory compression, Localized Adaptive Contrast Enhancement (LACE), spatial de-noise, Out-Of-Loop De-blocking (from AVC decoder), 16 bpc support for de-noise/de-mosaic.

There is support for Hardware assisted Motion Estimation engine for AVC/MPEG2 encode, True Motion, and Image stabilization applications.

The HW video processing is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2).
- Direct3D* 11 Video API.
- Intel Media SDK.
- MFT (Media Foundation Transform) filters.
- Intel CUI SDK.

Note: Not all features are supported by all the above APIs. Refer to the relevant documentation for more details.

2.4.2.4 Hardware Accelerated Transcoding

Transcoding is a combination of decode video processing (optional) and encode. Using the above hardware capabilities can accomplish a high-performance transcode pipeline. There is not a dedicated API for transcoding.

The processor graphics supports the following transcoding features:

- Low-power and low-latency AVC encoder for video conferencing and Wireless Display applications.
- Lossless memory compression for media engine to reduce media power.
- HW assisted Advanced Video Scaler.
- Low power Scaler and Format Converter.

Expected performance:

- 18x 1080p30 RT (same as previous generation).

Note: Actual performance depends on processor line, video processing algorithms used, content bit rate, and memory frequency.

2.4.3 Camera Pipe Support

Camera pipe functions such as de-mosaic, white balance, defect pixel correction, black level correction, gamma correction, LGCA, vignette control, Front end Color Space Converter (CSC), Image Enhancement Color Processing (IECP).

2.4.4 Switchable/Hybrid graphics

The processor supports Switchable/Hybrid graphics.

Switchable graphics: The Switchable Graphics feature allows you to switch between using the Intel integrated graphics and a discrete graphics card. The Intel Integrated Graphics driver will control the switching between the modes. In most cases it will operate as follows: when connected to AC power - Discrete graphic card; when connected to DC (battery) - Intel integrated GFX

Hybrid graphics: Intel integrated graphics and a discrete graphics card work cooperatively to achieve enhanced power and performance.

Table 2-15. Switchable/Hybrid Graphics Support

Operating System	Hybrid Graphics	Switchable Graphics[2]
Windows* 7	N/A	Yes[1]
Windows* 8.1	Yes[1]	N/A
Windows* 10	Yes[1]	N/A

Note:
1. Contact your graphics vendor to check for support.
2. Intel does not validate any SG configurations on Win8.1 or Win10.

2.4.5 GEN 9 Video Analytics

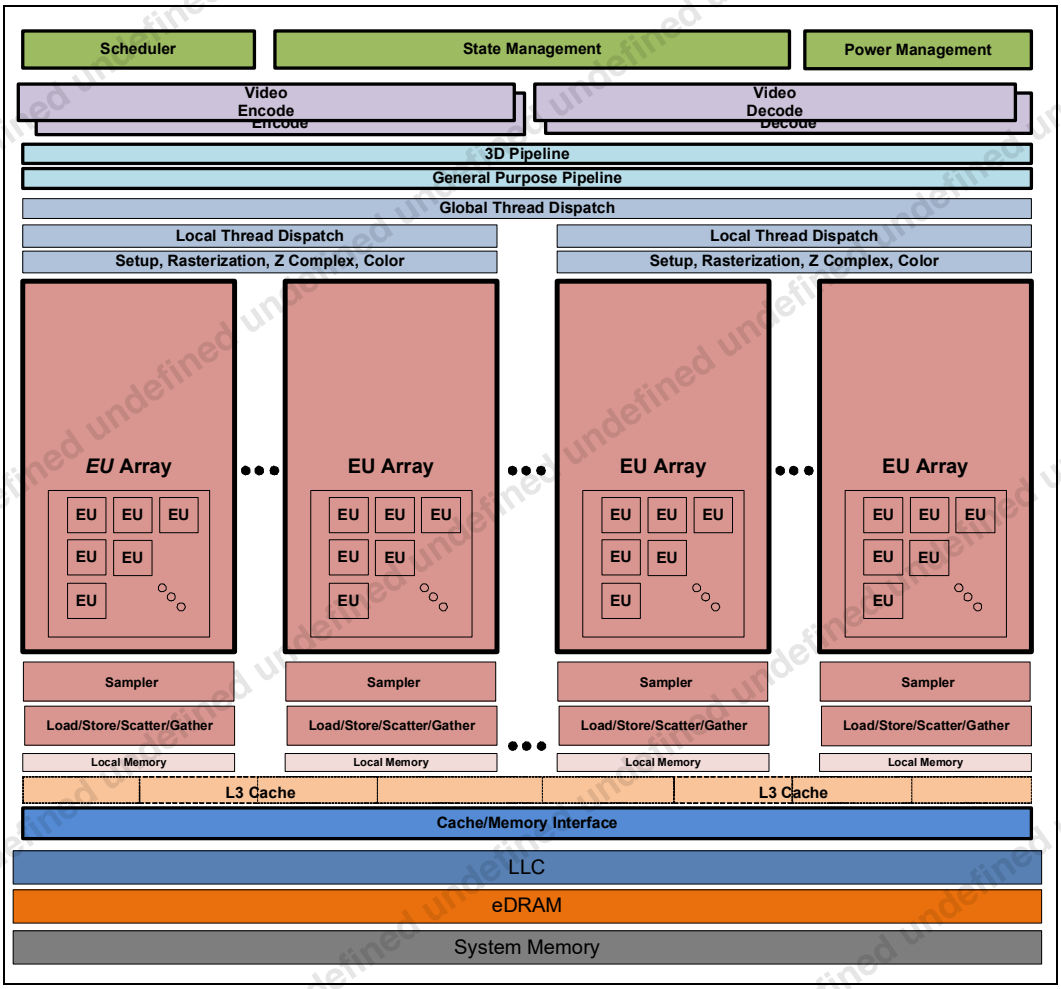
There is HW assist for video analytics filters such as scaling, convolve 2D/1D, minmax, 1P filter, erode, dilate, centroid, motion estimation, flood fill, cross correlation, Local Binary Pattern (LBP).

Figure 2-4. Video Analytics Common Use Cases

Usage	Scaling	Convolve 2D / 1D	MinMax Filter	Erode	Dilate	Centroid	Motion Estimation	Floodfill	Cross Correlation	LBP Creation
Face Detection	■	■	■	■	■	■				
Face Expressions	■	■	■			■				
Face Recognition	■	■				■				■
Face Tracking		■	■				■			
Gesture Detection	■	■	■	■	■	■		■		
Gesture Tracking		■	■				■			
Scene Identification	■	■	■			■				
2D to 3D Video	■	■	■				■			■
Object Detection	■	■	■	■	■	■			■	
Object Tracking		■	■				■			
Video Enhancement	■	■	■	■	■	■	■			
Video Segmentation	■	■	■				■			
Visual Search	■	■	■	■	■	■				
Stereo	■	■					■	■	■	■
Superes	■	■							■	

2.4.6 GEN 9 (Generation 9) Block Diagram

Figure 2-5. GEN 9 Block Diagram



2.4.7 GT2/3/4 Graphics Frequency

Table 2-16. GT2/3/4 Graphics Frequency (H-Processor Line)

Segment	GT Unslice	GT Unslice + 1 GT Slice	GT Unslice + 2 GT Slice	GT Unslice + 3 GT Slice
H - quad core GT2	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	—	—
H - quad core GT4+OPC	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	[GT Unslice + 1 Slice] - (1or2)BIN	[GT Unslice + 2 Slice] - (1or2)BIN

2.5 Display Interfaces

The processor supports single eDP* interface and 2 or 3 DDI interfaces (depends on segment):

- DDI interface can be configured as DisplayPort* or HDMI*.
- Each DDI can support dual mode (DP++).
- Each DDI can support DVI (DVI max resolution is 1920x1200 @ 60 Hz).
- The DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate.
- DDI ports notated as: DDI B, C, D.
- H-processor line processors supports eDP and up to 3 DDI supporting DP/HDMI.
- AUX/DDC signals are valid for each DDI Port. (three for H-processor line)
- Total Five dedicated HPD (Hot-plug detect signals) are valid for all processor SKUs.

Note: SSC is supported in eDP*/DP for all processor lines.

- DDI ports (B, C, and D) are disabled if No Connect Pull-Up resistor on following PCH signals: DDPB_CTRLDATA, DDPC_CTRLDATA and DDPD_CTRLDATA accordingly.
- eDP port is Disabled if No Connect Pull-Down resistor on CFG[4].
- SW strap can override HW strap.

Note: The processor platform supports DP Type-C implementation with additional discrete components.

- eDP* bifurcation:
  - eDP* bifurcation for H-processor line can be used for: DP x2 upper lanes (DDIE) for VGA support and eDP* x2 lower lanes. Both eDP* ports can be used simultaneously.

Table 2-17. VGA and Embedded DisplayPort* (eDP*) Bifurcation Summary

Port	H-Processor Line
eDP - DDIA (eDP lower x2 lanes, [1:0])	Yes
VGA - DDIE (DP upper x2 lanes, [3:2])	Yes[1]

Notes:
3. Requires a DP to VGA converter
4. DP-to-VGA converter on processor DDI ports is supported using External Dongle only, display driver software treat these VGA dongles as a DP Branch device

The technologies supported by the processor are listed in the following table.

Table 2-18. Embedded DisplayPort* (eDP*)/DDI Ports Availability

Ports	Port name in VBT	H-Processor Line [2,3]
DDI0 - eDP	Port A	Yes
DDI1	Port B	Yes
DDI2	Port C	Yes
DDI3	Port D	Yes
DDI4 - eDP/VGA	Port E	Yes[1]

Notes:
1. Port E is bifurcated from eDP; when VGA is used, need to use available AUX (if HDMI is in use).
   a. For example, DT can use eDP_AUX for VGA converter which is available as free Design but HPD must be used as DDPE_HPD3.
2. 3xDDC (DDPB, DDPC, DDPD) are valid for all processor SKUs.
3. 5xHPD (PCH) inputs (eDP_HPD, DDPB_HPD0, DDPC_HPD1, DDPD_HPD2, DDPE_HPD3) are valid for all processor SKUs.
4. N/A.
5. VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on how the aux channel lines are connected physically on the board

Table 2-19. Display Technologies Support

Technology	Standard
eDP* 1.3	VESA* Embedded DisplayPort* Standard 1.3
DisplayPort* 1.2	VESA DisplayPort* Standard 1.2 VESA DisplayPort* PHY Compliance Test Specification 1.2 VESA DisplayPort* Link Layer Compliance Test Specification 1.2
HDMI* 1.4[1]	High-Definition Multimedia Interface Specification Version 1.4

Notes:
1. HDMI* 2.0 support is possible using LS-Pcon converter chip connected to the DP port. The LS-Pcon supports 2 modes:
   a. Level shifter for HDMI 1.4 resolutions.
   b. DP-HDMI 2.0 protocol converter for HDMI 2.0 resolutions.

- The HDMI* interface supports HDMI with 3D, 4Kx2K@24Hz, Deep Color, and x.v.Color.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high definition content playback over digital interfaces, HDCP is not supported for eDP*.
- The processor supports eDP* display authentication: Alternate Scrambler Seed Reset (ASSR).
- The processor supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector.
  The max MST DP supported resolution for H-processor line is:

Table 2-20. Display Resolutions and Link Bandwidth for Multi-Stream Transport calculations (Sheet 1 of 2)

Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]
640	480	60	25.2	0.76
800	600	60	40	1.20
1024	768	60	65	1.95

Table 2-20. Display Resolutions and Link Bandwidth for Multi-Stream Transport calculations (Sheet 2 of 2)

Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]
1280	720	60	74.25	2.23
1280	768	60	68.25	2.05
1360	768	60	85.5	2.57
1280	1024	60	108	3.24
1400	1050	60	101	3.03
1680	1050	60	119	3.57
1920	1080	60	148.5	4.46
1920	1200	60	154	4.62
2048	1152	60	156.75	4.70
2048	1280	60	174.25	5.23
2048	1536	60	209.25	6.28
2304	1440	60	218.75	6.56
2560	1440	60	241.5	7.25
3840	2160	30	262.75	7.88
2560	1600	60	268.5	8.06
2880	1800	60	337.5	10.13
3200	2400	60	497.75	14.93
3840	2160	60	533.25	16.00
4096	2160	60	556.75	17.02
4096	2304	60	605	18.15

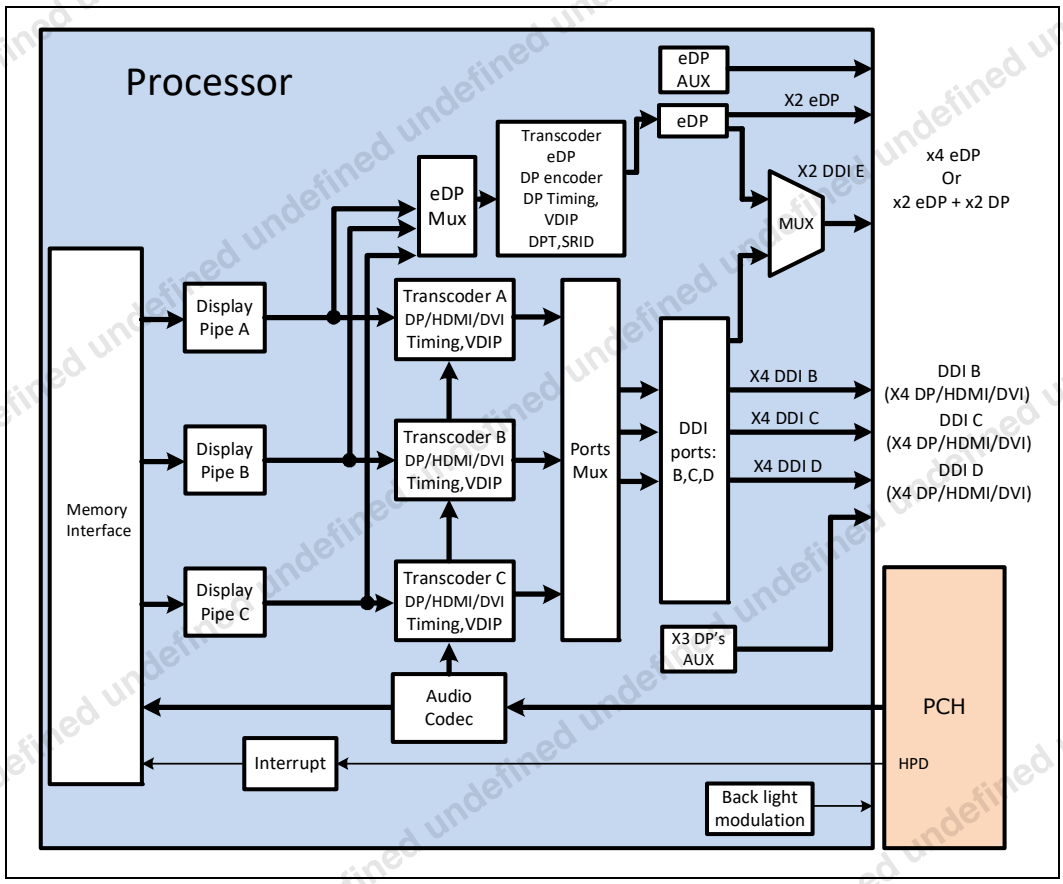
Notes:

1. All above is related to bit depth of 24.
2. The data rate for a given video mode can be calculated as: Data Rate = Pixel Frequency * Bit Depth.
3. The bandwidth requirements for a given video mode can be calculated as: Bandwidth = Data Rate * 1.25 (for 8B/10B coding overhead).
4. The Table above is partial List of the common Display resolutions just for example.
   The Link Bandwidth depends if the standards is Reduced Blanking or not.
   If the Standard is Not reduced blanking - the expected Bandwidth will be higher.
   For more details, refer to VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT). Version 1.0, Rev. 13 February 8, 2013
   To calculate what are the resolutions that can be supported in MST configurations, follow the below guidelines:
   a. Identify what is the Link Bandwidth (column right) according the requested Display resolution.
   b. Summarize the Bandwidth for Two of three Displays accordingly, and make sure the final result is below 21.6Gbps. (for HBR2, four lanes)
   c. For special cases when x2 lanes are used or HBR or RBR used, refer to the tables in Section 2.5.11 accordingly.
5. For examples:
   a. Docking Two displays: 3840x2160@60hz + 1920x1200@60Hz = 16 + 4.62 = 20.62Gbps [Supported]
   b. Docking Three Displays: 3840x2160@30hz + 3840x2160@30Hz + 1920x1080@60hz = 7.88 + 7.88 + 4.16 = 19.92Gbps [Supported]
6. Consider also the supported resolutions as mentioned in Section 2.5.6 and Section 2.5.7.

- The processor supports only 3 streaming independent and simultaneous display combinations of DisplayPort*/eDP*/HDMI/DVI monitors. In the case where 4 monitors are plugged in, the software policy will determine which 3 will be used.
- Three High Definition Audio streams over the digital display interfaces are supported.
- For display resolutions driving capability see Section 2-22.

- DisplayPort* Aux CH supported by the processor, while DDC channel, Panel power sequencing, and HPD are supported through the PCH. Refer to the appropriate Platform Controller Hub (PCH) datasheet (see related documents) for more information.

Figure 2-6. Processor Display Architecture (with 3 DDI Ports as an Example)



Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard

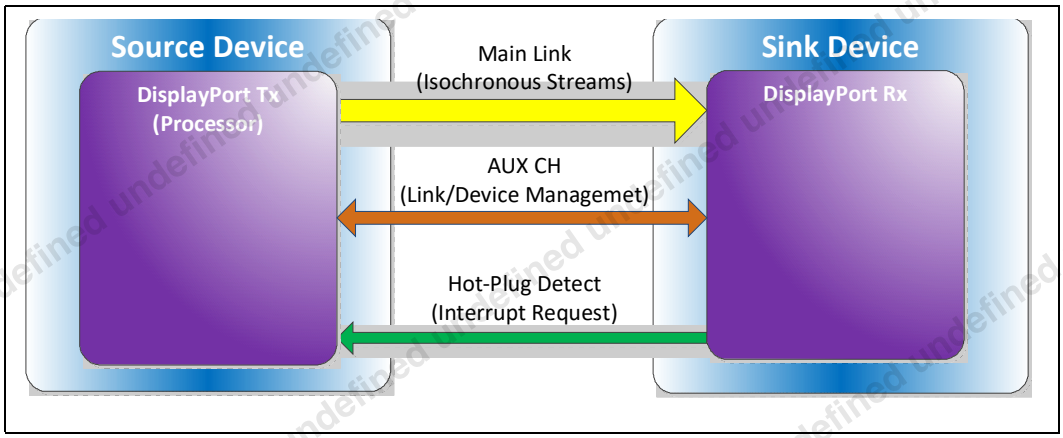
2.5.1 DisplayPort*

The DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance to VESA* DisplayPort* specification. Refer to Table 2-19.

Figure 2-7. DisplayPort* Overview



2.5.2 High-Definition Multimedia Interface (HDMI*)

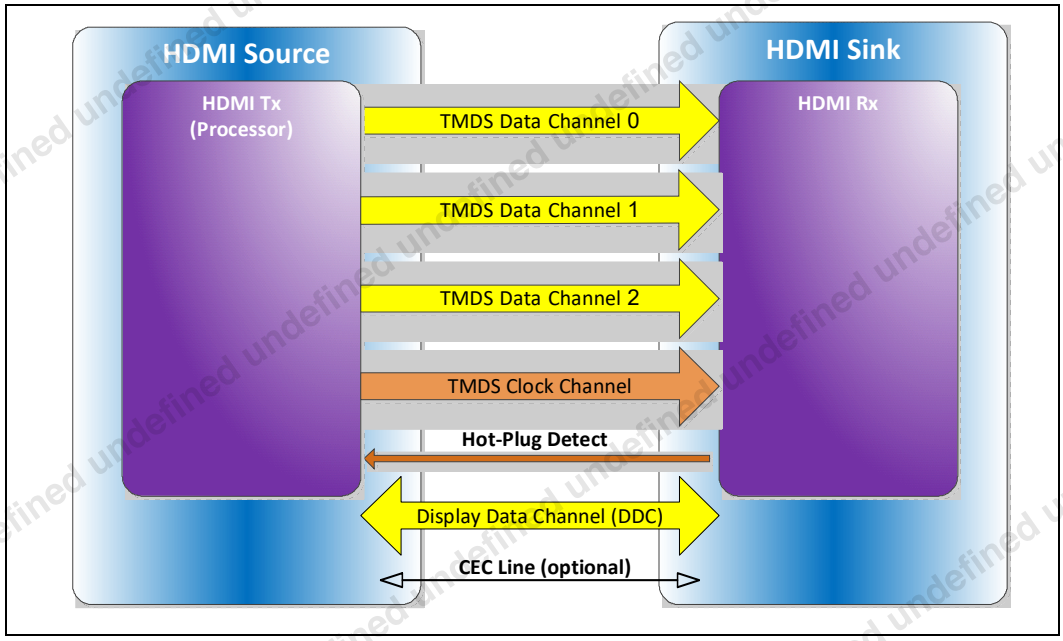
The High-Definition Multimedia Interface (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface.

Figure 2-8. HDMI* Overview



2.5.3 Digital Video Interface (DVI)

The processor Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol except for the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. The digital display data signals driven natively through the processor are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

2.5.4 embedded DisplayPort* (eDP*)

The embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. Like DisplayPort, embedded DisplayPort* also consists of a Main Link, Auxiliary channel, and an optional Hot-Plug Detect signal. eDP* can be bifurcated in order to support VGA display.

2.5.5 Integrated Audio

- HDMI* and display port interfaces carry audio along with video.
- The processor supports 3 High Definition audio streams on 3 digital ports simultaneously (the DMA controllers are in PCH).
- The integrated audio processing (DSP) is performed by the PCH, and delivered to the processor using the AUDIO_SDI and AUDIO_CLK inputs pins.
- AUDIO_SDO output pin is used to carry responses back to the PCH
- Supports only the internal HDMI and DP CODECs.

Table 2-21. Processor Supported Audio Formats over HDMI and DisplayPort*

Audio Formats	HDMI*	DisplayPort*
AC-3 Dolby* Digital	Yes	Yes
Dolby Digital Plus	Yes	Yes
DTS-HD*	Yes	Yes
LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes
Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI* and DisplayPort* monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

2.5.6 Multiple Display Configurations (Dual Channel DDR)

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort/HDMI/DVI. The following table shows examples of valid three display configurations through the processor.

Table 2-22. Display Resolution (Sheet 1 of 2)

Standard	-Processor Line (display 1,2,3,4)	Notes
eDP*	4096x2304 @ 60Hz, 24bpp	1,2,3
DP*	4096x2304 @ 60Hz, 24bpp	1,2,3

Table 2-22. Display Resolution (Sheet 2 of 2)

Standard	-Processor Line (display 1,2,3,4)	Notes
HDMI* 1.4 (native)	4096x2160 @ 24 Hz, 24 bpp	1,2,3
HDMI 2.0 (Via LS-Pcon)	4096x2160 @ 60Hz, 24bpp	1,2,3,7

Notes:
1. Maximum resolution is based on implementation of 4 lanes with HBR2 link data rate.
2. bpp - bit per pixel.
3. support up to 4 displays but only three can be active at the same time.
4. The resolutions are assumed at max VCC_{SA}, additional power penalty of ~0.26W per one Display Port. Final resolutions depends on overall power specifications/limitations.
5. In case of connecting more than one active display port the processor frequency may be lower than base frequency at thermally limited scenario.
6. Supporting 4K display required two DDR channels of same size. Performance degradations exists in the processor platforms while running 4K content for system using single channel system memory (compared to using dual channel).
7. HDMI2.0 implemented via LSPCON device. Only one LSPCON with HDCP2.2 support is supported per processor platform.

2.5.7 Multiple Display Configurations (Single Channel DDR)

Table 2-23. H-Processor line Display Resolution Configuration

Minimum DDR Speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @60 Hz (Primary)	DP @ 60 Hz / HDMI[1] @ 30 Hz (Secondary 1)	DP @ 60 Hz / HDMI[1] @ 30 Hz (Secondary 2)
1333	4096 x 2304	Not Connected	Not Connected
	2560 x 1440	4096 x 2304	Not Connected
1600	3840 x 2160	4096 x 2304	Not Connected
1866	2560 x 1440	4096 x 2304	4096 x 2304
2133	3840 x 2160	4096 x 2304	4096 x 2304

Notes:
1. HDMI@30Hz Maximum resolution is: 4096 x 2160

Table 2-24. H-Processor line Display Resolution Configuration when DP @ 30 Hz

Minimum DDR Speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @ 60 Hz (Primary)	DP @ 30 Hz (Secondary 1)	DP @30 Hz (Secondary 2)
1333	3840x 2160	Not Connected	Not Connected
	3840 x 2160	4096 x 2304	Not Connected
1600	3840 x 2160	4096 x 2304	4096 x 2304

2.5.8 High-Bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 1.4 for content protection over wired or wireless displays (HDMI*, DVI, and DisplayPort*).

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

Table 2-25. HDCP Display supported Implications

Display Support		Content Protection Implications
HDCP 1.4	HDMI 1.4	Native FHD Only
	Display Port	Native FHD Only
HDCP 2.2	HDMI 1.4	LSPCON UHD 2160p30
	HDMI 2.0	LSPCON UHD 2160p60
	HDMI 2.0a	Not Supported
	Display Port	Not Supported

2.5.9 Display Link Data Rate Support

Table 2-26. Display Link Data Rate Support

Technology	Link Data Rate
eDP*	RBR (1.62 GT/s) HBR (2.7 GT/s) HBR2 (5.4 GT/s)
DisplayPort*	RBR (1.62 GT/s) HBR (2.7 GT/s) HBR2 (5.4 GT/s)
HDMI*	2.97 Gb/s

Table 2-27. Display Resolution and Link Rate Support

Resolution	Link Rate Support	High Definition
4096x2304	5.4 (HBR2)	UHD (4K)
3840x2160	5.4 (HBR2)	UHD (4K)
3200x2000	5.4 (HBR2)	QHD+
3200x1800	5.4 (HBR2)	QHD+
2880x1800	2.7 (HBR)	QHD
2880x1620	2.7 (HBR)	QHD
2560x1600	2.7 (HBR)	QHD
2560x1440	2.7 (HBR)	QHD
1920x1080	1.62 (RBR)	FHD

2.5.10 Display Bit Per Pixel (BPP) Support

Table 2-28. Display Bit Per Pixel (BPP) Support

Technology	Bit Per Pixel (bpp)
eDP*	24,30,36
DisplayPort*	24,30,36
HDMI*	24,36

2.5.11 Display Resolution per Link Width

Table 2-29. Supported Resolutions[1] for HBR2 (5.4Gbps) by link width

Link Width	Max. Link Bandwidth [Gbps]	Max. Pixel Clock (Theoretical) [MHz]	H-Processor Line
4 lanes	21.6	720[2]	See
2 lanes	10.8	360	2880x1800@60Hz, 24bpp
1 lane	5.4	180	2048x1280@60Hz, 24bpp
Notes: 1. The examples assumed 60 Hz refresh rate and 24 bpp. 2. The actual Max pixel clock for HBR2 is limited by the CD clock to 675 MHz for H-processor line.			

Table 2-30. Supported Resolutions[1] for HBR (2.7Gbps) By Link Width

Link Width	Max. Link Bandwidth [Gbps]	Max. Pixel Clock (theoretical) [MHz]	H-processor line
4 lanes	10.8	360	2880x1800@60Hz, 24bpp
2 lanes	5.4	180	2048x1280@60Hz, 24bpp
1 lane	2.7	90	1280x960@60Hz, 24bpp
Notes: 1. The examples assumed 60 Hz refresh rate and 24 bpp.			

2.6 Platform Environmental Control Interface (PECI)

Table 2-31. Display Bit Per Pixel (BPP) Support

Technology	Bit Per Pixel (bpp)
eDP*	24,30,36
DisplayPort*	24,30,36
HDMI*	24,36

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components like Super IO (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

2.6.1 PECI Bus Architecture

The PECI architecture is based on a wired OR bus that the clients (as processor PECI) can pull up (with strong drive).

The idle state on the bus is near zero.

The following figures demonstrates PECI design and connectivity:

- PECI Host-Clients Connection: While the host/originator can be third party PECI host and one of the PECI client is a processor PECI device.
- PECI EC Connection.

Figure 2-9. Example for PECI Host-Clients Connection

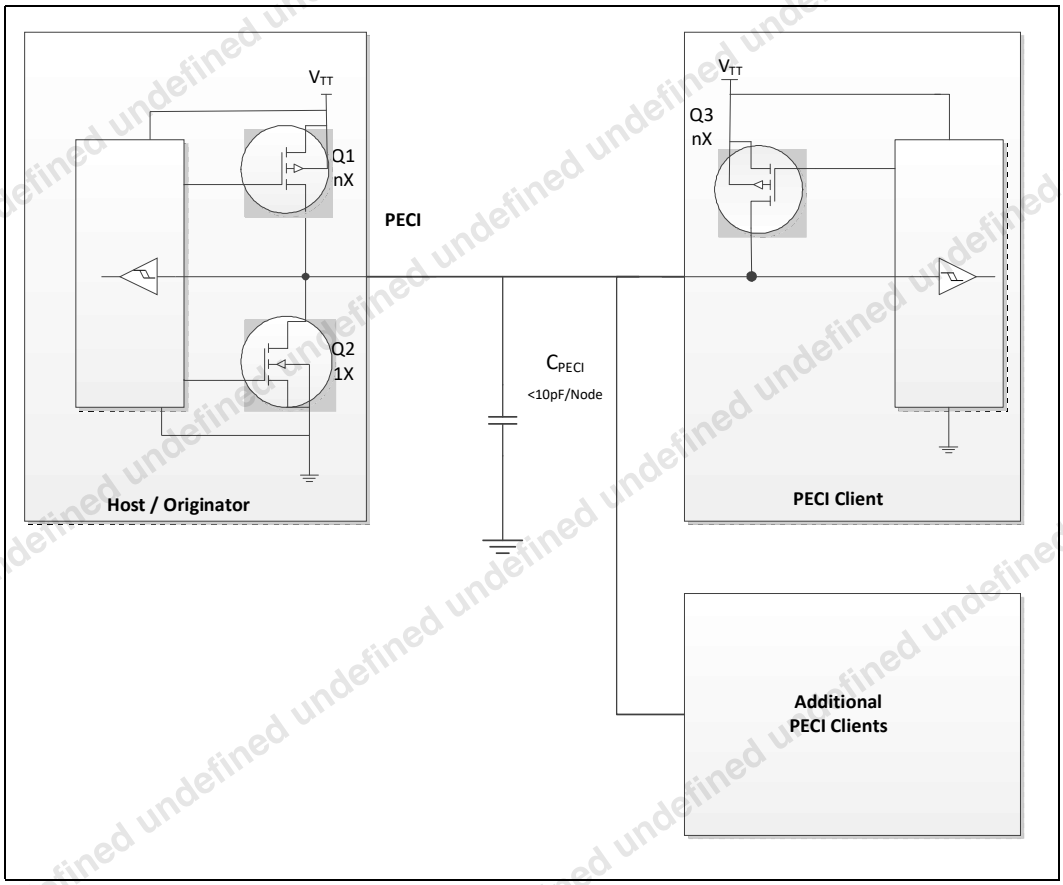
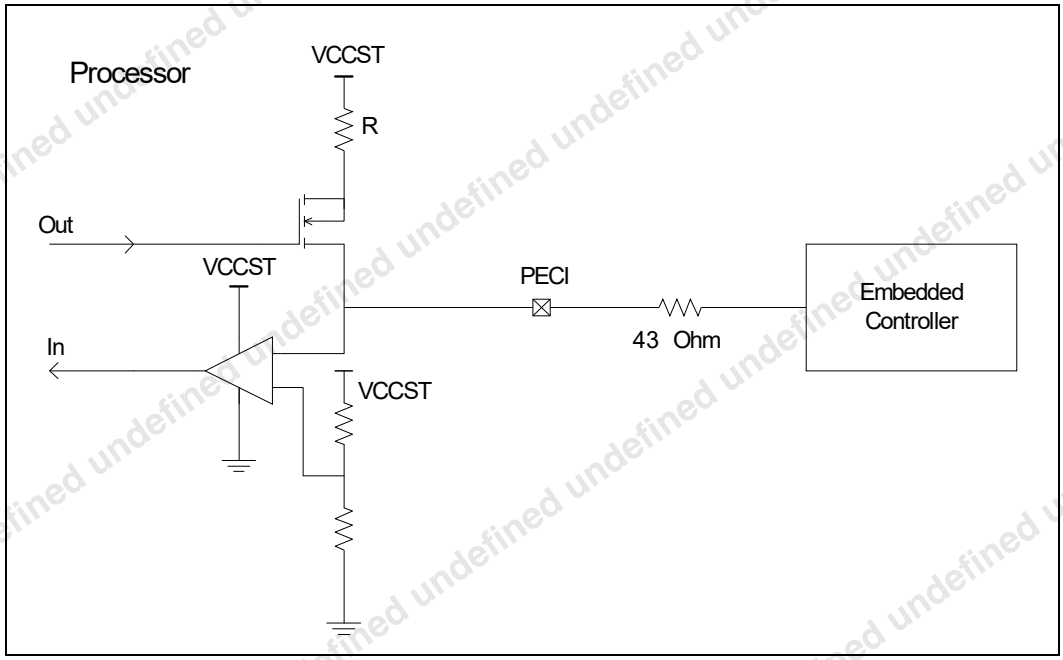


Figure 2-10. Example for PECI EC Connection



§ §

3 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel Virtualization Technology (Intel VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel® Virtualization Technology for Directed I/O (Intel® VT-d) extends Intel VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3*. Available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

3.1.1 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-X)

Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that VMMs will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

Intel® VT-x Key Features

The processor supports the following added new Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
  - EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as de-fragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.
- EPTP (EPT pointer) switching
  - EPTP switching is a specific VM function. EPTP switching allows guest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX non-root operation can request a change of EPTP without a VM exit. Software will be able to choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
  - Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

The processor IA core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
  - EPT is hardware assisted page table virtualization
  - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor IA core hardware structures (such as TLBs)
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.2 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)

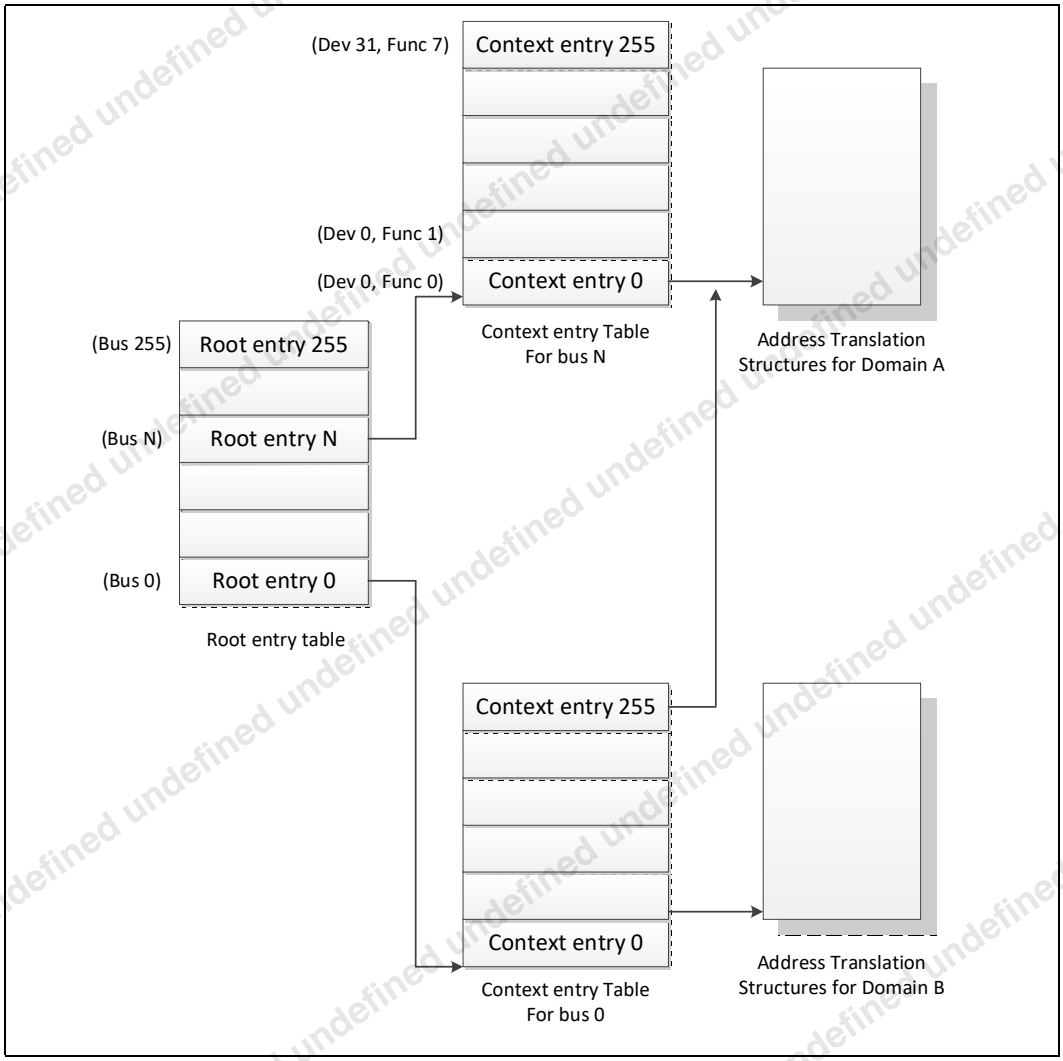
Intel® VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for a virtualized platform and provides software with the following capabilities:

- I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.
- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel® VT-d accomplishes address translation by associating transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between the device's PCI Express* Bus/Device/Function (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Table) that contains Guest specific address translations.

Figure 3-1. Device to Domain Mapping Structures



Intel® VT-d functionality, often referred to as an Intel® VT-d Engine, has typically been implemented at or near a PCI Express* host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such VT-d engine receives a PCI Express transaction from a PCI Express bus, it uses the B/D/F number associated with the transaction to search for an Intel® VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel® VT-d fault. If Intel VT-d translation is required, the Intel® VT-d engine performs an N-level table walk.

For more information, refer to *Intel Virtualization Technology for Directed I/O Architecture Specification* http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/vt-directed-io-spec.pdf

Intel® VT-d Key Features

The processor supports the following Intel® VT-d features:

- Memory controller and processor graphics comply with the Intel VT-d 2.1 Specification.
- Two Intel VT-d DMA remap engines.
  - — iGFX DMA remap engine
  - — Default DMA remap engine (covers all devices except iGFX)
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for Global, Domain specific and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxxh) not translated
  - — Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

- 4-level Intel VT-d Page walk – both default Intel VT-d engine as well as the IGD VT-d engine are upgraded to support 4-level Intel VT-d tables (adjusted guest address width of 48 bits)
- Intel VT-d superpage – support of Intel VT-d superpage (2 MB, 1 GB) for default Intel VT-d engine (that covers all devices except IGD)

  IGD Intel VT-d engine does not support superpage and BIOS should disable superpage in default Intel® VT-d engine when iGfx is enabled.

Note: Intel VT-d Technology may not be available on all SKUs.

3.2 Security Technologies

3.2.1 Intel® Trusted Execution Technology (Intel® TXT)

Intel® Trusted Execution Technology (Intel TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs, both VLWs and IPI

For the above features, BIOS must test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the *Intel® Trusted Execution Technology Measured Launched Environment Programming Guide*

Note: Intel TXT Technology may not be available on all SKUs.

3.2.2 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

Note: Intel AES-NI Technology may not be available on all SKUs.

3.2.3 PCLMULQDQ (Perform Carry-Less Multiplication Quad Word) Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.2.4 Intel® Secure Key

The processor supports Intel Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure storage, and so on.

3.2.5 Execute Disable Bit

The Execute Disable Bit allows memory to be marked as non executable when combined with a supporting operating system. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can, thus, help improve the overall security of the system.

See the *Intel 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.

3.2.6 Boot Guard Technology

Boot Guard technology is a part of boot integrity protection technology. Boot Guard can help protect the platform boot integrity by preventing execution of unauthorized boot blocks. With Boot Guard, platform manufacturers can create boot policies such that invocation of an unauthorized (or untrusted) boot block will trigger the platform protection per the manufacturer's defined policy.

With verification based in the hardware, Boot Guard extends the trust boundary of the platform boot process down to the hardware level.

Boot Guard accomplishes this by:

- Providing of hardware-based Static Root of Trust for Measurement (S-RTM) and the Root of Trust for Verification (RTV) using Intel architectural components.
- Providing of architectural definition for platform manufacturer Boot Policy.
- Enforcing of manufacture provided Boot Policy using Intel architectural components.

Benefits of this protection is that Boot Guard can help maintain platform integrity by preventing re-purposing of the manufacturer’s hardware to run an unauthorized software stack.

Note: Boot Guard availability may vary between the different SKUs.

3.2.7 Supervisor Mode Execution Protection (SMEP)

Intel® Supervisor Mode Execution Protection (SMEP) is a mechanism that provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, refer to *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A* at: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.8 Intel Supervisor Mode Access Protection (SMAP)

Intel Supervisor Mode Access Protection (SMAP) is a mechanism that provides next level of system protection by blocking a malicious user from tricking the operating system into branching off user data. This technology shuts down very popular attack vectors against operating systems.

For more information, refer to the *Intel ® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.9 Intel® Memory Protection Extensions (Intel® MPX)

Intel® MPX provides hardware accelerated mechanism for memory testing (heap and stack) buffer boundaries in order to identify buffer overflow attacks.

An Intel® MPX enabled compiler inserts new instructions that tests memory boundaries prior to a buffer access. Other Intel® MPX commands are used to modify a database of memory regions used by the boundary checker instructions.

The Intel® MPX ISA is designed for backward compatibility and will be treated as no-operation instructions (NOPs) on older processors.

Intel® MPX can be used for:

- Efficient runtime memory boundary checks for security-sensitive portions of the application.
- As part of a memory checker tool for finding difficult memory access errors. Intel® MPX is significantly of magnitude faster than software implementations.

Intel® MPX emulation (without hardware acceleration) is available with the Intel® C++ Compiler 13.0 or newer.

For more information, refer to the Intel® MPX documentation.

3.2.10 Intel® Software Guard Extensions (Intel® SGX)

Software Guard Extensions (SGX) is a processor enhancement designed to help protect application integrity and confidentiality of secrets and withstands software and certain hardware attacks.

Software Guard Extensions (SGX) creates and operates in protected regions of memory named Enclaves.

Enclave code can be accessed using new special ISA commands that jump into per Enclave predefined addresses. Data within an Enclave can only be accessed from that same Enclave code.

The latter security statements hold under all privilege levels including supervisor mode (ring-0), System Management Mode (SMM) and other Enclaves.

Software Guard Extensions (SGX) features a memory encryption engine that both encrypt Enclave memory as well as protect it from corruption and replay attacks.

Software Guard Extensions (SGX) benefits over alternative Trusted Execution Environments (TEEs) are:

- Enclaves are written using C/C++ using industry standard build tools.
- High processing power as they run on the processor.
- Large amount of memory are available as well as non-volatile storage (such as disk drives).
- Simple to maintain and debug using standard IDEs (Integrated Development Environment)
- Scalable to a larger number of applications and vendors running concurrently

For more information, refer to the Intel® SGX DOC.

3.2.11 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)

Refer to Section 3.1.2 Intel® VT-d for detail.

3.3 Power and Performance Technologies

3.3.1 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution processor IA core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

Intel recommends enabling Intel Hyper-Threading Technology with Microsoft* Windows* 8 and Microsoft Windows 7 and disabling Intel Hyper-Threading Technology using the BIOS for all previous versions of Windows* operating systems. For more information on Intel Hyper-Threading Technology, see http://www.intel.com/technology/platform-technology/hyper-threading/.

Note: Intel® HT Technology may not be available on all SKUs.

3.3.2 Intel® Turbo Boost Technology 2.0

The Intel® Turbo Boost Technology 2.0 allows the processor IA core/processor graphics core to opportunistically and automatically run faster than the processor IA core base frequency/processor graphics base frequency if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology 2.0 feature is designed to increase performance of both multi-threaded and single-threaded workloads.

Compared with previous generation products, Intel Turbo Boost Technology 2.0 will increase the ratio of application power towards TDP and also allows to increase power above TDP as high as PL2 for short periods of time. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology 2.0 may not be available on all SKUs.

3.3.2.1 Intel® Turbo Boost Technology 2.0 Frequency

To determine the highest performance frequency amongst active processor IA cores, the processor takes the following into consideration:

- The number of processor IA cores operating in the C0 state.
- The estimated processor IA core current consumption and I_{CCMax} register settings.
- The estimated package prior and present power consumption and turbo power limits.
- The package temperature.
- Sustained turbo residencies at high voltages and temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay within its TDP limit. Turbo processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states, see Power Management.

3.3.3 Intel® Advanced Vector Extensions 2 (Intel® AVX2)

Intel® Advanced Vector Extensions 2.0 (Intel® AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel® AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software.

For more information on Intel AVX, see http://www.intel.com/software/avx

Note: Intel AVX2 Technology may not be available on all SKUs.

3.3.4 Intel® 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
  - Delivery modes
  - Interrupt and processor priorities
  - Interrupt sources
  - Interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
  - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
  - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.

- Increased range of processor addressability in x2APIC mode:
  - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32-bits in a software transparent fashion.
  - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields – a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) - 16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers:
  - To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.
- The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the "x2APIC" mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
- The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations.

Note: Intel x2APIC Technology may not be available on all SKUs.

For more information, see the Intel® *64 Architecture x2APIC Specification* at http://www.intel.com/products/processor/manuals/.

3.3.5 Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or processor IA cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active processor IA cores without waking the deep idle processor IA cores. For performance, it routes the interrupt to the idle (C1) processor IA cores without interrupting the already heavily loaded processor IA cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on.

3.3.6 Intel® Transactional Synchronization Extensions (Intel® TSX-NI)

Intel® Transactional Synchronization Extensions (Intel® TSX-NI) provides a set of instruction set extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the performance of fine-grain locking while actually programming using coarse-grain locks. Details on Intel TSX-NI may be found in *Intel® Architecture Instruction Set Extensions Programming Reference*.

Note: Intel® TSX-NI may not be available on all SKUs.

3.4 Intel® Image Signal Processor (Intel® ISP)

3.4.1 Platform Imaging Infrastructure

The imaging infrastructure is based on a number of hardware components as shown in Figure 3-3. The three major components of the system are:

- **Camera SubSystem:** Located in the lid of the system and contains CMOS sensor, flash, LED, I/O interface (MIPI* CSI-2 and I^{2}C*), Focus control and other components.
- **Camera I/O controller:** The I/O controller is located in the PCH and contains a MIPI-CSI2 Host controller. The host controller is a PCI device (independent of the ISP device). The CSI-2 HCI brings imaging data from an external imager into the system and provides a command and control channel for the imager using I^{2}C.
- **Intel® ISP (Image Signal Processor):** The ISP processes the images captured by Bayer sensors to be used by still or video applications (such as, JPEG, H.264, and so on).

Figure 3-2. Processor Camera System

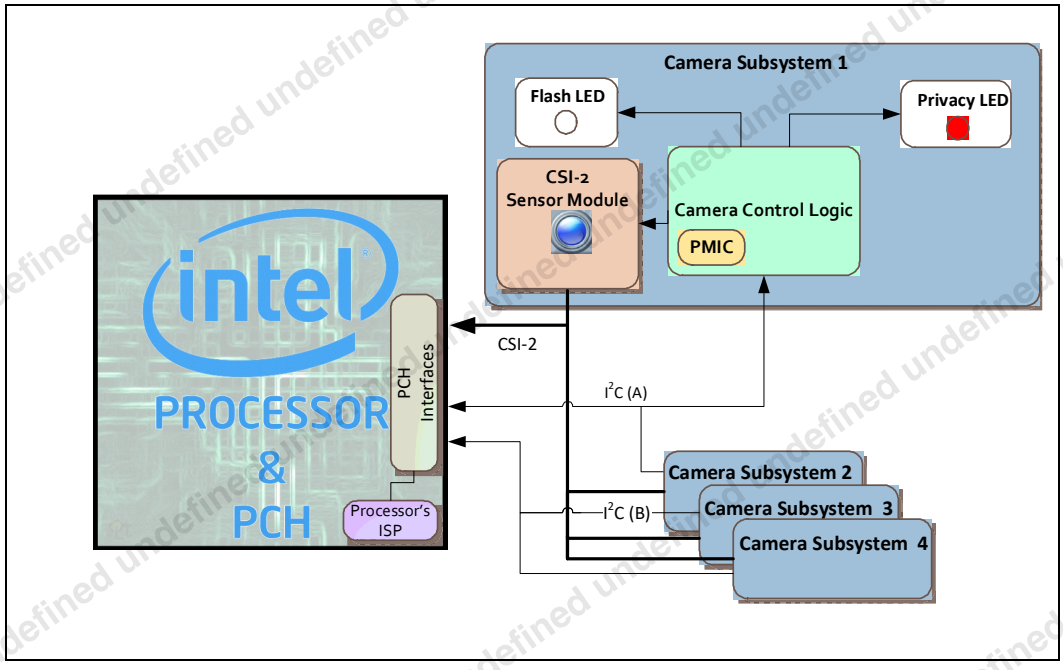
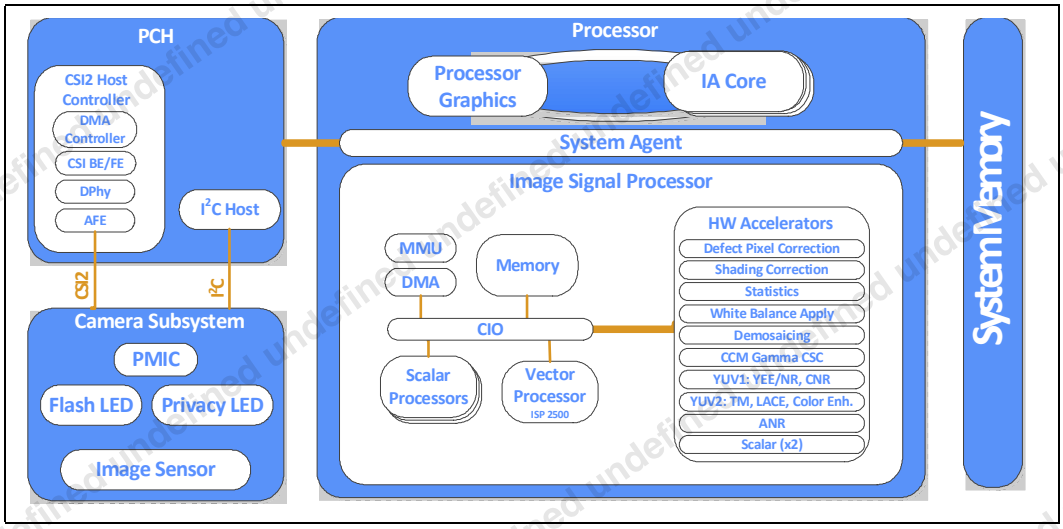


Figure 3-3. Platform Imaging Infrastructure



3.5 Debug Technologies

3.5.1 Intel® Processor Trace

Intel® Processor Trace (Intel® PT) is a new tracing capability added to Intel® Architecture, for use in software debug and profiling. Intel PT provides the capability for more precise software control flow and timing information, with limited impact to software execution. This provides enhanced ability to debug software crashes, hangs, or other anomalies, as well as responsiveness and short-duration performance issues.

Intel® VTune™ Amplifier for Systems and the Intel® System Debugger are part of Intel® System Studio 2015, which includes updates for new debug and trace features on this latest platform, including Intel PT and Intel® Trace Hub.

An update to the Linux perf utility, with support for Intel PT, is available for download at https://github.com/virtuoso/linux-perf/tree/intel_pt. It requires rebuilding the kernel and the perf utility.

§ §

4 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor IA Core Power Management
- Integrated Memory Controller (IMC) Power Management
- PCI Express* Power Management
- Direct Media Interface (DMI) Power Management
- Processor Graphics Power Management

Figure 4-1. Processor Power States

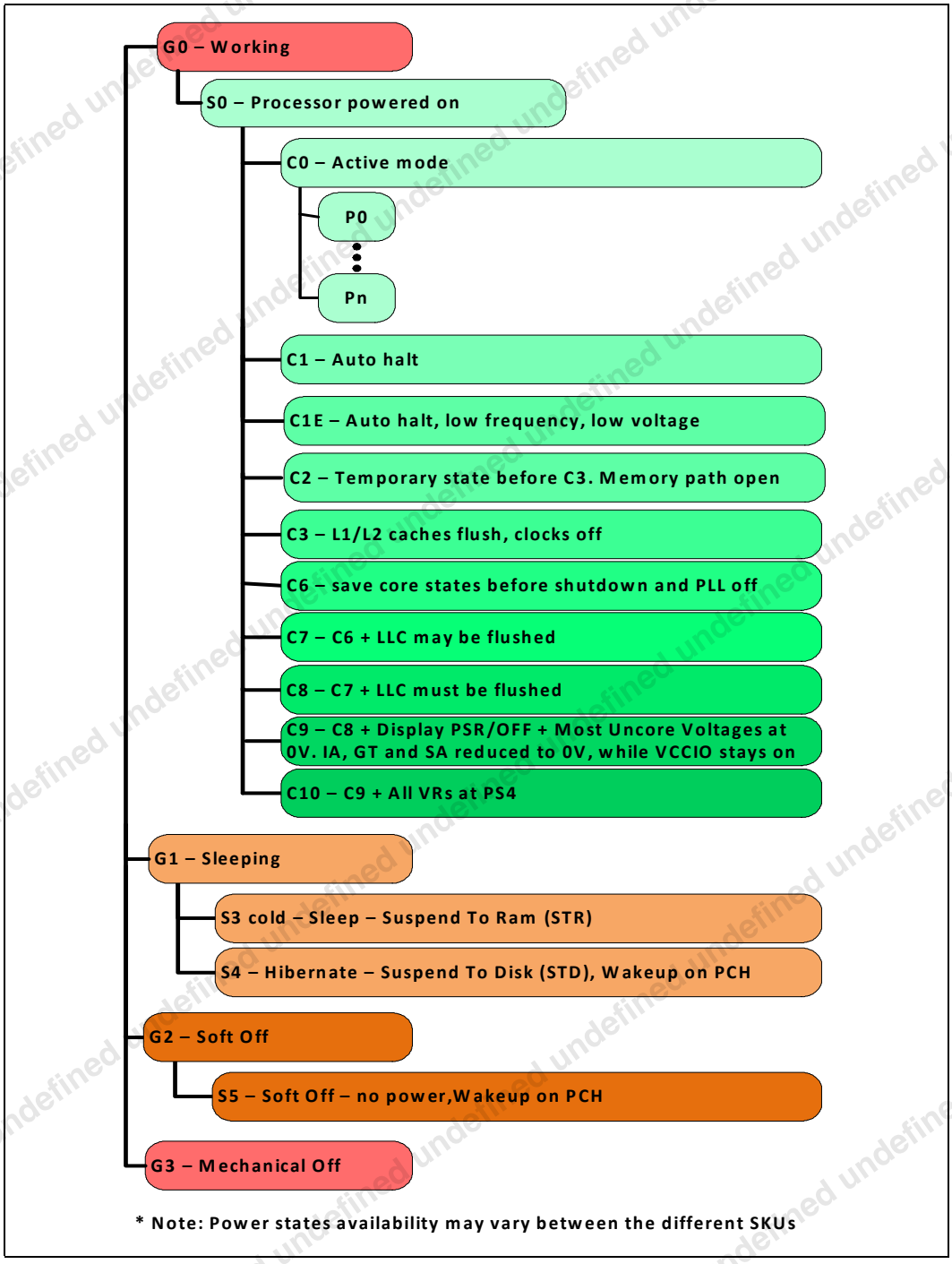
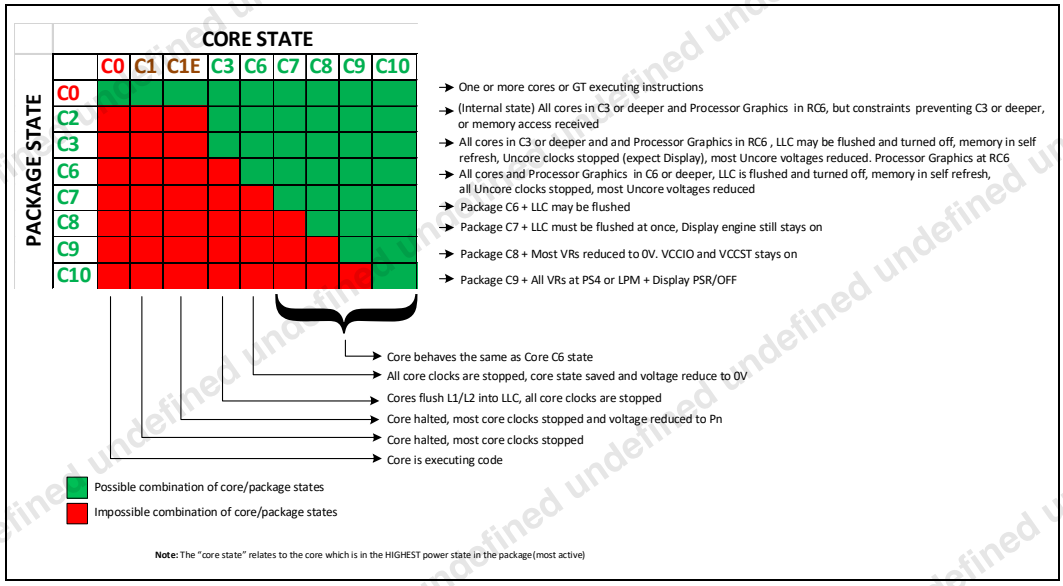


Figure 4-2. Processor Package and IA Core C-States



4.1 Advanced Configuration and Power Interface (ACPI) States Supported

This section describes the ACPI states supported by the processor.

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wake-up on PCH).
G2/S5	Soft off. All power lost (except wake-up on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

Processor IA Core/Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT processor IA core state (package C0 state).
C1E	AutoHALT processor IA core state with lowest frequency and voltage operating point (package C0 state).
C2	All processor IA cores in C3 or deeper. Memory path open. Temporary state before Package C3 or deeper.
C3	Processor IA execution cores in C3 or deeper, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache. LLC may be flushed. Clocks are shut off to each core.
C6	Processor IA execution cores in this state save their architectural state before removing core voltage. BCLK is off.
C7	Processor IA execution cores in this state behave similarly to the C6 state. If all execution cores request C7, LLC ways may be flushed until it is cleared. If the entire LLC is flushed, voltage will be removed from the LLC.
C8	C7 plus LLC must be flushed.
C9	C8 plus most Uncore voltages at 0V. IA, GT and SA reduced to 0V, while Vcc_{IO} stays on.
C10	C9 plus all VRs at PS4 or LPM. 24MHz clock off

Table 4-2. Integrated Memory Controller (IMC) States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE de-asserted (not self-refresh) with all banks closed.
Active Power down	CKE de-asserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE de-asserted using device self-refresh.

Table 4-3. PCI Express* Link States

State	Description
L0	Full on – Active transfer state.
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

Table 4-4. Direct Media Interface (DMI) States

State	Description
L0	Full on – Active transfer state
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

Table 4-5. G, S, and C Interface State Combinations

Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power Down	On	Deep Power Down
G0	S0	C8/C9/C10	Off	On	Deeper Power Down
G1	S3	Power off	Off	Off, except RTC	Suspend to RAM
G1	S4	Power off	Off	Off, except RTC	Suspend to Disk
G2	S5	Power off	Off	Off, except RTC	Soft Off
G3	N/A	Power off	Off	Power off	Hard off

4.2 Processor IA Core Power Management

While executing code, Enhanced Intel SpeedStep® Technology and Hardware-controlled P-states optimizes the processor's IA core frequency and voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

4.2.1 OS/HW controlled P-states

4.2.1.1 Enhanced Intel SpeedStep® Technology

Enhanced Intel SpeedStep® Technology enables OS to control and select P-state. The following are the key features of Enhanced Intel SpeedStep® Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor IA cores.
  - Once the voltage is established, the PLL locks on to the target frequency.
  - All active processor IA cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested among all active IA cores is selected.
  - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.1.2 Intel® Speed Shift Technology

Hardware-controlled P-states are an energy efficient method of frequency control by the hardware rather than relying on OS control. OS is aware of available hardware P-states and request a desired P-state or it can let Hardware determine the P-state. The OS request is based on its workload requirements and awareness of processor capabilities. Processor decision is based on the different system constraints for example: Workload demand, thermal limits while taking into consideration the minimum and maximum levels and activity window of performance requested by the Operating System.

For more details, refer to the following document (see related documents section):

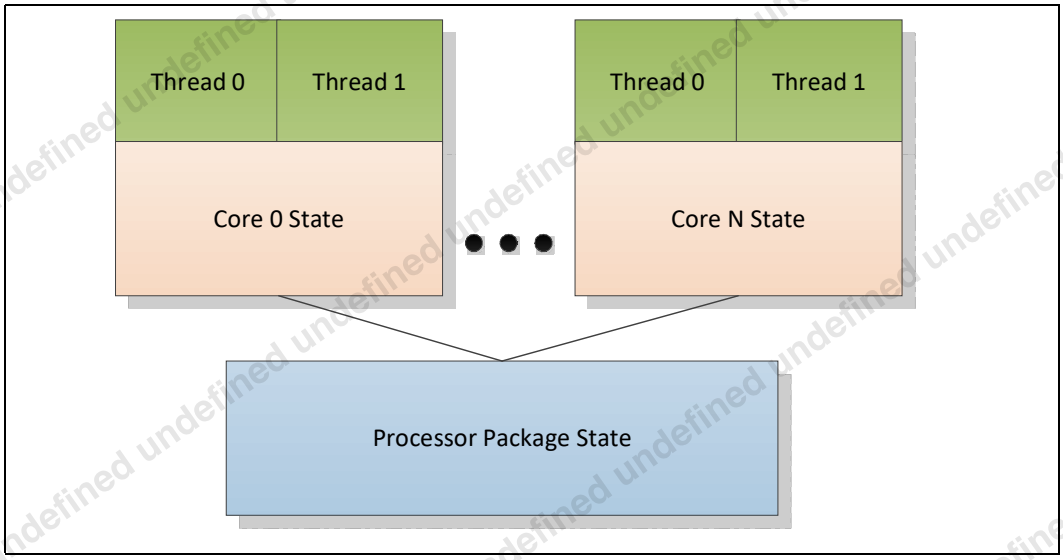
- Intel® 64 and IA-32 Architectures Software Developer's Manual (SDM), volume 3B.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, deeper C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor IA core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Caution: Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 4-3. Idle Power Management Breakdown of the Processor IA Cores



While individual threads can request low-power C-states, power saving actions only take place once the processor IA core C-state is resolved. processor IA core C-states are automatically resolved by the processor. For thread and processor IA core C-states, a transition to and from C0 state is required before entering any other C-state.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

When P_LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wake up on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Processor IA Core C-State Rules

The following are general rules for all processor IA core C-states, unless specified otherwise:

- A processor IA core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3 state, resulting in a processor IA core C1E state). See the *G, S, and C Interface State Combinations* table.
- A processor IA core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
  - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes up only that thread.
- If any thread in a processor IA core is active (in C0 state), the core's C-state will resolve to C0.
- Any interrupt coming into the processor package may wake any processor IA core.
- A system reset re-initializes all processor IA cores.

Processor IA core C0 State

The normal operating state of a processor IA core where code is being executed.

Processor IA core C1/C1E State

C1/C1E is a low-power state entered when all threads within a processor IA core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel 64 and IA-32 Architectures Software Developer's Manual* for more information.

While a processor IA core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5.

Processor IA core C3 State

Individual threads of a processor IA core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A processor IA core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared LLC, while maintaining its architectural state. All processor IA core clocks are stopped at this point. Because the processor IA core's caches are flushed, the processor does not wake any processor IA core that is in the C3 state when either a snoop is detected or when another processor IA core accesses cacheable memory.

Processor IA core C6 State

Individual threads of a processor IA core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering processor IA core C6 state, the processor IA core will save its architectural state to a dedicated SRAM. Once complete, a processor IA core will have its voltage reduced to zero volts. During exit, the processor IA core is powered on and its architectural state is restored.

Processor IA core C7-C10 States

Individual threads of a processor IA core can enter the C7, C8, C9, or C10 state by initiating a P_LVL4, P_LVL5, P_LVL6, P_LVL7 I/O read (respectively) to the P_BLK or by an MWAIT(C7/C8/C9/C10) instruction. The processor IA core C7-C10 state exhibits the same behavior as the processor IA core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C7/C6 to C3
- C7/C6/C3 To C1

The decision to demote a processor IA core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each processor IA core's immediate residency history. Upon each processor IA core C6/C7 request, the processor IA core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a processor IA core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually. If the interrupt rate experienced on a processor IA core is high and the processor IA core is rarely in a deep C-state between such interrupts, the processor IA core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a processor IA core to C1 as compared to C3.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

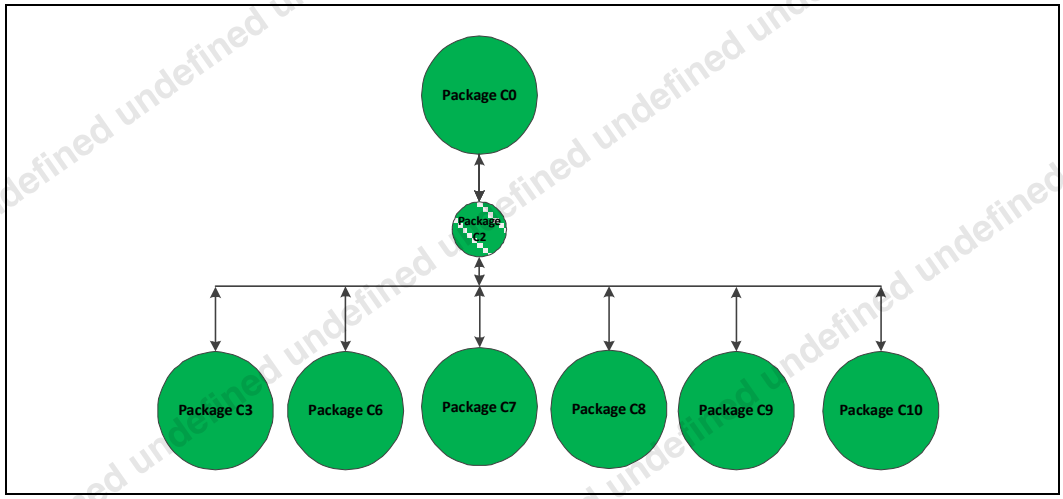
The processor supports C0, C1/C1E, C3, C6, C7, C8, C9, and C10 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states, unless specified otherwise:

- A package C-state request is determined by the lowest numerical processor IA core C-state amongst all processor IA cores.
- A package C-state is automatically resolved by the processor depending on the processor IA core idle power states and the status of the platform components.
  - Each processor IA core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor.
  - For package C-states, the processor is not required to enter C0 before entering any other C-state.
  - Entry into a package C-state may be subject to auto-demotion – that is, the processor may keep the package in a deeper package C-state then requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a processor IA core break event is received, the target processor IA core is activated and the break event message is forwarded to the target processor IA core.
  - If the break event is not masked, the target processor IA core enters the processor IA core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request,
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

Figure 4-4. Package C-State Entry and Exit



Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its processor IA cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low-power state. Individual processor IA cores may be in deeper power idle states while the package is in C0 state.

Package C2 State

Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when either:

- All processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6, but constraints (LTR, programmed timer events in the near future, and so forth) prevent entry to any state deeper than C2 state.
- Or, all processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6 and a memory access request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low-power state when:

- At least one processor IA core is in the C3 state.
- The other processor IA cores are in a C3 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 state or deeper state but has allowed a package C3 state.

In package C3-state, the LLC shared cache is valid.

Package C6 State

A processor enters the package C6 low-power state when:

- At least one processor IA core is in the C6 state.
- The other processor IA cores are in a C6 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 or deeper request but has allowed a C6 package state.

In package C6 state, all processor IA cores have saved their architectural state and have had their voltages reduced to zero volts. It is possible the LLC shared cache is flushed and turned off in package C6 state.

Package C7 State

The processor enters the package C7 low-power state when all processor IA cores are in the C7 or deeper state and the operating system may request that the LLC will be flushed.

processor IA core break events are handled the same way as in package C3 or C6.

Upon exit of the package C7 state, the LLC will be partially enabled once a processor IA core wakes up if it was fully flushed, and will be fully enabled once the processor has stayed out of C7 for a preset amount of time. Power is saved since this prevents the LLC from being re-populated only to be immediately flushed again. Some VRs are reduce to 0V.

Package C8 State

The processor enters C8 states when the processor IA cores lower numerical state is C8.

The C8 state is similar to C7 state, but in addition, the LLC is flushed in a single step, Vcc and Vcc_{GT} are reduced to 0V. The display engine stays on.

Package C9 State

The processor enters C9 states when the processor IA cores lower numerical state is C9.

Package C9 state is similar to C8 state; the VRs are off, Vcc, Vcc_{GT} and Vcc_{SA} at 0V, Vcc_{IO} and Vcc_{ST} stays on.

Package C10 State

The processor enters C10 states when the processor IA cores lower numerical state is C10.

Package C10 state is similar to the package C9 state, but in addition the IMVP8 VR is in PS4 low-power state, which is near to shut off of the IMVP8 VR. The Vcc_{IO} is in low-power mode as well. Package C10 is the processor package state regardless of InstantGo support/implementation.

InstantGo

InstantGo is a platform state. On display time out the OS requests the processor to enter package C10 and platform devices at RTD3 (or disabled) in order to attain low power in idle. InstantGo requires proper BIOS and OS configuration.

Dynamic LLC Sizing

When all processor IA cores request C7 or deeper C-state, internal heuristics dynamically flushes the LLC. Once the processor IA cores enter a deep C-state, depending on their MWAIT sub-state request, the LLC is either gradually flushed N-ways at a time or flushed all at once. Upon the processor IA cores exiting to C0 state, the LLC is gradually expanded based on internal heuristics.

4.2.6 Package C-States and Display Resolutions

The integrated graphics engine has the frame buffer located in system memory. When the display is updated, the graphics engine fetches display data from system memory. Different screen resolutions and refresh rates have different memory latency requirements. These requirements may limit the deepest Package C-state the processor can enter. Other elements that may affect the deepest Package C-state available are the following:

- Display is on or off
- Single or multiple displays
- Native or non-native resolution

- Panel Self Refresh (PSR) technology

Note: Display resolution is not the only factor influencing the deepest Package C-state the processor can get into. Device latencies, interrupt response latencies, and core C-states are among other factors that influence the final package C-state the processor can enter.

The following table lists display resolutions and deepest available package C-State.The display resolutions are examples using common values for blanking and pixel rate. Actual results will vary. The table shows the deepest possible Package C-state.System workload, system idle, and AC or DC power also affect the deepest possible Package C-state.

4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI C-states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory in which it is not connected to any actual memory devices (such as SODIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding control signals (CLK_P/CLK_N/CKE/ODT/CS) are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with a DRAMs present, the DRAMs are not ensured to maintain data integrity. CKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the memory interface.Each channel drives 4 CKE pins, one per rank.

The CKE is one of the power-saving means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification.

The processor supports four different types of power-down modes in package C0 state. The different power-down modes can be enabled through configuring PM PDWN config register. The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN_idle_counter (bits 11:0). The different power-down modes supported are:

- **No power-down** (CKE disable)

- **Active power-down (APD):** This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is fined by tXP – small number of cycles. For this mode, DRAM DLL must be on.
- **PPD/DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power modes. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL must be off.
- **Precharged power-down (PPD):** This mode is entered if all banks in DDR are precharged when de-asserting CKE. Power-saving in this mode is intermediate – better than APD, but less than DLL-off. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP. The difference from APD mode is that when waking-up, all page-buffers are empty.) The LPDDR does not have a DLL. As a result, the power savings are as good as PPD/DDL-off but will have lower exit latency and higher performance.

The CKE is determined per rank, whenever it is inactive. Each rank has an idle counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-off of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible – PPD/DLL-off with a low idle timer value
- In high-performance systems with dense packaging (that is, tricky thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

The default value that BIOS configures in PM PDWN config register is 6080 – that is, PPD/DLL-off mode with idle timer of 0x80, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCLKs that a rank is idle that causes entry to the selected power mode. As this timer is set to a shorter time the IMC will have more opportunities to put the DDR in power-down. There is no BIOS hook to set this register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up.

CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Section 4.6.1.1 for more details on conditional self-refresh with Intel HD Graphics enabled.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor IA core flushes pending cycles and then enters SDRAM ranks that are not used by the processor graphics into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service.

Table 4-6. Targeted Memory State Conditions

State	Memory State with Processor Graphics	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.
C3, C6, C7 or deeper	If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.
S3	Self-Refresh Mode	Self-Refresh Mode
S4	Memory power-down (contents lost)	Memory power-down (contents lost)

4.3.2.3 Dynamic Power-Down

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor IA core controller can be configured to put the devices in active power-down (CKE de-assertion with open pages) or precharge power-down (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODT and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.3.3 DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates VDDQ for the majority of the logic to reduce idle power while keeping all critical DDR pins such as CKE and VREF in the appropriate state.

In C7 or deeper power state, the processor internally gates V_{CCIO} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

4.3.4 Power Training

BIOS MRC performing Power Training steps to reduce DDR I/O power while keeping reasonable operational margins still guaranteeing platform operation. The algorithms attempt to weaken ODT, driver strength and the related buffers parameters both on the MC and the DRAM side and find the best possible trade-off between the total I/O power and the operational margins using advanced mathematical models.

4.4 PCI Express* Power Management

- Active power management support using L1 state.
- All inputs and outputs disabled in L2/L3 Ready state.

Note: Processor PEG-PCIe interface does not support Hot-Plug.

Hot Plug like* is only supported at Processor PEG-PCIe using Thunderbolt Device.

* Turning Thunderbolt power on and Off electrically RTD3 Like

Note: The PCI Express* and DMI interfaces are present only in 2-Chip platform processors.

An increase in power consumption may be observed when PCI Express* ASPM capabilities are disabled.

4.5 Direct Media Interface (DMI) Power Management

- Active power management support using L1 state.

Note: The PCI Express* and DMI interfaces are present only in 2-Chip platform processors.

4.6 Processor Graphics Power Management

4.6.1 Memory Power Savings Technologies

4.6.1.1 Intel® Rapid Memory Power Management (Intel® RMPM)

Intel® Rapid Memory Power Management (Intel® RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow the system to remain in the deeper power states longer for memory not reserved for graphics memory. Intel® RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

4.6.1.2 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel® S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel® S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Examples where Intel S2DDT is less effective are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Examples where Intel S2DDT is less effective are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.6.2 Display Power Savings Technologies

4.6.2.1 Intel® (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* Port

Intel® DRRS provides a mechanism where the monitor is placed in a slower refresh rate (the rate at which the display is updated). The system is smart enough to know that the user is not displaying either 3D or media like a movie where specific refresh rates are required. The technology is very useful in an environment such as a plane where the user is in battery mode doing E-mail, or other standard office applications. It is also useful where the user may be viewing web pages or social media sites while in battery mode.

4.6.2.2 Intel® Automatic Display Brightness

Intel® Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel® Automatic Display Brightness increases the backlight setting.

4.6.2.3 Smooth Brightness

The Smooth Brightness feature is the ability to make fine grained changes to the screen brightness. All Windows* 8 system that support brightness control are required to support Smooth Brightness control and it should be supporting 101 levels of brightness control. Apart from the Graphics driver changes, there may be few System BIOS changes required to make this feature functional.

4.6.2.4 Intel® Display Power Saving Technology (Intel® DPST) 6.0

The Intel® DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel® DPST subsystem. An interrupt to Intel® DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel® DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
2. Intel® DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel® DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

4.6.2.5 Low-Power Single Pipe (LPSP)

Low-power single pipe is a power conservation feature that helps save power by keeping the inactive pipes powered OFF. This feature is enabled only in a single display configuration without any scaling functionalities. This feature is supported from 4th Generation Intel® Core™ processor family onwards. LPSP is achieved by keeping a single pipe enabled during eDP* only with minimal display pipeline support. This feature is panel independent and works with any eDP panel (port A) in single display mode.

4.6.3 Processor Graphics Core Power Savings Technologies

4.6.3.1 Intel® Graphics Dynamic Frequency

Intel® Turbo Boost Technology 2.0 is the ability of the processor IA cores and graphics (Graphics Dynamic Frequency) cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel® Graphics Dynamic Frequency is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor IA core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power,

and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State. Intel® Graphics Dynamic Frequency requires BIOS support. Additional power and thermal budget must be available.

4.6.3.2 Intel® Graphics Render Standby Technology (Intel® GRST)

The final power savings technology from Intel happens while the system is asleep. This is another technology where the voltage is adjusted down. For RC6 the voltage is adjusted very low, or very close to zero, what may reduced power by over 1000.

4.6.3.3 Dynamic FPS (DFPS)

Dynamic FPS (DFPS) or dynamic frame-rate control is a runtime feature for improving power-efficiency for 3D workloads. Its purpose is to limit the frame-rate of full screen 3D applications without compromising on user experience. By limiting the frame rate, the load on the graphics engine is reduced, giving an opportunity to run the Processor Graphics at lower speeds, resulting in power savings. This feature works in both AC/DC modes.

4.7 Voltage Optimization

Voltage Optimization opportunistically provides reduction in power consumption; that is, a boost in performance at a given PL1. Over time the benefit is reduced. There is no change to base frequency or turbo frequency. During system validation and tuning, this feature should be disabled to reflect processor power and performance that is expected over time.

This feature is available on selected SKUs.

§ §

5 Thermal Management

5.1 Processor Thermal Management

The thermal solution provides both component-level and system-level thermal management. To allow optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature (Tj_{MAX}) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1.1 Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP is a power dissipation and junction temperature operating condition limit, specified in this document, that is validated during manufacturing for the base configuration when executing a near worst case commercially available workload as specified by Intel for the SKU segment. TDP may be exceeded for short periods of time or if running a very high power workload.

The processor integrates multiple processing IA cores, graphics cores and for some SKUs a PCH and/or OPC on a single package. This may result in power distribution differences across the package and must be considered when designing the thermal solution.

Intel® Turbo Boost Technology 2.0 allows processor IA cores to run faster than the base frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current control limits. When Intel® Turbo Boost Technology 2.0 is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of estimated available energy budget in the processor package.
- The processor may exceed the TDP for short durations to utilize any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Graphics peak frequency operation is based on the assumption of only one of the graphics domains (GT/GTx) being active. This definition is similar to the IA core Turbo concept, where peak turbo frequency can be achieved when only one IA core is active. Depending on the workload being applied and the distribution across the graphics domains the user may not observe peak graphics frequency for a given workload or benchmark

- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues.

Note: Intel® Turbo Boost Technology 2.0 availability may vary between the different SKUs.

5.1.2 Intel® Turbo Boost Technology 2.0 Power Monitoring

When operating in turbo mode, the processor monitors its own power and adjusts the processor and graphics frequencies to maintain the average power within limits over a thermally significant time period. The processor estimates the package power for all components on package. In the event that a workload causes the temperature to exceed program temperature limits, the processor will protect itself using the Adaptive Thermal Monitor.

5.1.3 Intel® Turbo Boost Technology 2.0 Power Control

Illustration of Intel® Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces.

5.1.3.1 Package Power Control

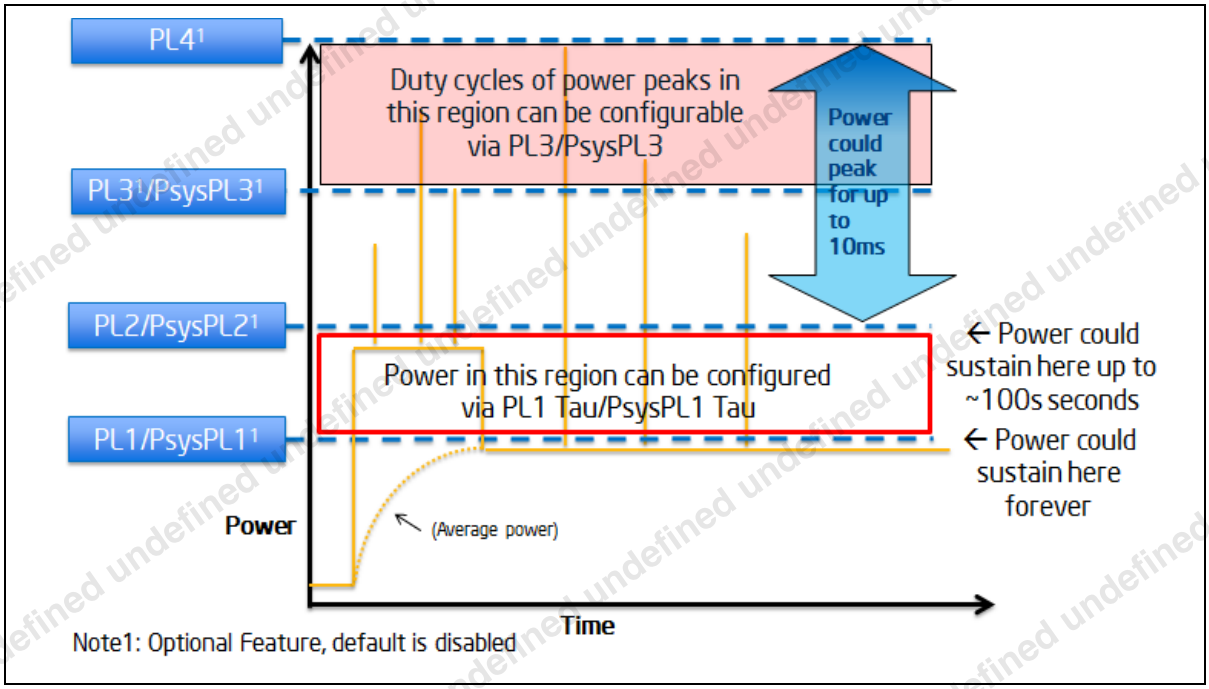
The package power control settings of PL1, PL2, PL3, PL4 and Tau allow the designer to configure Intel® Turbo Boost Technology 2.0 to match the platform power delivery and package thermal solution limitations.

- Power Limit 1 (PL1): A threshold for average power that will not exceed - recommend to set to equal TDP power. PL1 should not be set higher than thermal solution cooling limits.
- Power Limit 2 (PL2): A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2.
- Power Limit 3 (PL3): A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency. This is an optional setting
- Power Limit 4 (PL4): A limit that will not be exceeded, the PL4 power limiting algorithms will preemptively limit frequency to prevent spikes above PL4.
- Turbo Time Parameter (Tau): An averaging constant used for PL1 exponential weighted moving average (EWMA) power calculation.

Note: Implementation of Intel® Turbo Boost Technology 2.0 only requires configuring PL1, PL1 Tau and PL2.

Note: PL3 and PL4 are disabled by default.

Figure 5-1. Package Power Control



5.1.3.2 Platform Power Control

The processor introduces Psys (Platform Power) to enhance processor power management. The Psys signal needs to be sourced from a compatible charger circuit and routed to the IMVP8 (voltage regulator). This signal will provide the total thermally relevant platform power consumption (processor and rest of platform) using SVID to the processor.

When the Psys signal is properly implemented, the system designer can utilize the package power control settings of PsysPL1/Tau, PsysPL2 and PsysPL3 for additional manageability to match the platform power delivery and platform thermal solution limitations for Intel® Turbo Boost Technology 2.0. The operation of the PsysPL1/tau, PsysPL2 and PsysPL3 is analogous to the processor power limits described in Section 5.1.3.1.

- Platform Power Limit 1 (PsysPL1): A threshold for average platform power that will not be exceeded - recommend to set to equal platform thermal capability.
- Platform Power Limit 2 (PsysPL2): A threshold that if exceeded, the PsysPL2 rapid power limiting algorithms will attempt to limit the spikes above PsysPL2.
- Platform Power Limit 3 (PsysPL3): A threshold that if exceeded, the PsysPL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PsysPL3 by reactively limiting frequency.
- PsysPL1 Tau: An averaging constant used for PsysPL1 exponential weighted moving average (EWMA) power calculation.
- The Psys signal and associated power limits/Tau are optional for the system designer and disabled by default.
- The Psys data will not include power consumption for charging.

5.1.3.3 Turbo Time Parameter (Tau)

Turbo Time Parameter (Tau) is a mathematical parameter (units of seconds) that controls the Intel® Turbo Boost Technology 2.0 algorithm. During a maximum power turbo event, the processor could sustain PL2 for a duration longer than the Turbo Time Parameter. If the power value and/or Turbo Time Parameter is changed during runtime, it may take some time based on the new Turbo Time Parameter level for the algorithm to settle at the new control limits. The time varies depending on the magnitude of the change, power limits and other factors. There is an individual Turbo Time Parameter associated with Package Power Control and Platform Power Control.

5.1.4 Configurable TDP (cTDP) and Low-Power Mode

Configurable TDP (cTDP) and Low-Power Mode (LPM) form a design option where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low-Power Mode technologies offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configuration and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to PL1 and associated frequencies for the scenario with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in OS power policies or hardware events such as docking a system, flipping a switch or pressing a button. cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

Note: Configurable TDP and Low-Power Mode technologies are not battery life improvement technologies.

5.1.4.1 Configurable TDP

Note: Configurable TDP availability may vary between the different SKUs.

With cTDP, the processor is now capable of altering the maximum sustained power with an alternate processor IA core base frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

cTDP consists of three modes as shown in the following table.

Table 5-1. Configurable TDP Modes

Mode	Description
Base	The average power dissipation and junction temperature operating condition limit, specified in Table 5-2 for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.
TDP-Up	The SKU-specific processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Up configuration in Table 5-2. The Configurable TDP-Up Frequency and corresponding TDP is higher than the processor IA core Base Frequency and SKU Segment Base TDP.
TDP-Down	The processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Down configuration in Table 5-2. The Configurable TDP-Down Frequency and corresponding TDP is lower than the processor IA core Base Frequency and SKU Segment Base TDP.

In each mode, the Intel® Turbo Boost Technology 2.0 power limits are reprogrammed along with a new OS controlled frequency range. The DPTF driver assists in all these operations. The cTDP mode does not change the max per-processor IA core turbo frequency.

5.1.4.2 Low-Power Mode

Low-Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

Through the DPTF driver, LPM can be configured to use each of the following methods to reduce active power:

- Restricting package power control limits and Intel® Turbo Boost Technology availability
- Off-Lining processor IA core activity (Move processor traffic to a subset of cores)
- Placing a processor IA Core at LFM or LSF (Lowest Supported Frequency)
- Utilizing IA clock modulation
- Reducing number of active EUs to GT2 equivalent (applicable for GT3 SKUs Only)
- LPM power as listed in the *TDP Specifications* table is defined at point which processor IA core working at LSF, GT = RPn and 1 IA core active

Off-lining processor IA core activity is the ability to dynamically scale a workload to a limited subset of cores in conjunction with a lower turbo power limit. It is one of the main vectors available to reduce active power. However, not all processor activity is ensured to be able to shift to a subset of cores. Shifting a workload to a limited subset of cores allows other processor IA cores to remain idle and save power. Therefore, when LPM is enabled, less power is consumed at equivalent frequencies.

Minimum Frequency Mode MFM of operation, which is the lowest supported frequency (LSF) at the LFM voltage, has been made available for use under LPM for further reduction in active power beyond LFM capability to enable cooler and quieter modes of operation.

5.1.5 Thermal Management Features

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. In order to protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

5.1.5.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor IA core power consumption and temperature until it operates below its maximum operating temperature. Processor IA core power reduction is achieved by:

- Adjusting the operating frequency (using the processor IA core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor IA core clocks (duty cycle).

The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS), meets its maximum operating temperature. The maximum operating temperature implies maximum junction temperature Tj_{MAX}.

Reaching the maximum operating temperature activates the Thermal Control Circuit (TCC). When activated the TCC causes both the processor IA core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Tj_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE_TARGET (0x1A2) MSR, bits [23:16].

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain processor thermal control to PL1 = TDP. The system design should provide a thermal solution that can maintain normal operation when PL1 = TDP within the intended usage range.

Adaptive Thermal Monitor protection is always enabled.

5.1.5.1.1 TCC Activation Offset

TCC Activation Offset can be set as an offset from Tj_max to lower the onset of TCC and Adaptive Thermal Monitor. In addition, the processor has added an optional time window (Tau) to manage processor performance at the TCC Activation offset value using an EWMA (Exponential Weighted Moving Average) of temperature.

TCC Activation Offset with Tau=0

An offset (degrees Celsius) can be written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], the offset value will be subtracted from the value found in bits [23:16]. When the time window (Tau) is set to zero, there will be no averaging, the offset, will be subtracted from the Tjmax value and used as a new max temperature set point for

Adaptive Thermal Monitoring. This will have the same behavior as in prior products to have TCC activation and Adaptive Thermal Monitor to occur at this lower target silicon temperature.

If enabled, the offset should be set lower than any other passive protection such as ACPI _PSV trip points

TCC Activation Offset with Tau

To manage the processor with the EWMA (Exponential Weighted Moving Average) of temperature, an offset (degrees Celsius) is written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], and the time window (Tau) is written to the TEMPERATURE_TARGET (0x1A2) MSR [6:0]. The Offset value will be subtracted from the value found in bits [23:16] and be the temperature.

The processor will manage to this average temperature by adjusting the frequency of the various domains. The instantaneous Tj can briefly exceed the average temperature. The magnitude and duration of the overshoot is managed by the time window value (Tau).

This averaged temperature thermal management mechanism is in addition, and not instead of Tjmax thermal management. That is, whether the TCC activation offset is 0 or not, TCC Activation will occur at TjMAX.

5.1.5.1.2 Frequency/Voltage Control

Upon Adaptive Thermal Monitor activation, the processor attempts to dynamically reduce processor temperature by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor IA core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor IA core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the processor IA core bus ratio and number of processor IA cores in deep C-states.
- The processor IA core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the trigger temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor IA core will transition to the new target automatically.

- On an upward operating point transition the voltage transition precedes the frequency transition.
- On a downward transition the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor IA core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.

- If the P-state target frequency is lower than the processor IA core optimized target frequency, the processor will transition to the P-state operating point.

5.1.5.1.3 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

Clock modulation will not be activated by the Package average temperature control mechanism.

5.1.5.2 Digital Thermal Sensor

Each processor has multiple on-die Digital Thermal Sensor (DTS) that detects the processor IA, GT and other areas of interest instantaneous temperature.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Platform Environmental Control Interface (PECI).

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given DTS. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE_THERM_STATUS MSR 1B1h and IA32_THERM_STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C- states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (Tj_{MAX}), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from Tj_{MAX}. The DTS does not report temperatures greater than Tj_{MAX}. The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0x0, except when the TCC

activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both processor IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the processor IA core's local APIC. Refer to the *Intel 64 and IA-32 Architectures Software Developer's Manual* for specific register and programming details.

5.1.5.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ±5 °C within the entire operating range.

5.1.5.2.2 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability before the DTS reading reaches Tj_{MAX}.

5.1.5.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

5.1.5.4 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system de-asserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced but the reduction rate is slower than the system PROCHOT# response of < 100 us. The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

5.1.5.5 Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.1.5.6 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

5.1.5.7 Low-Power States and PROCHOT# Behavior

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wake up, if the processor is still hot, the PROCHOT# will re-assert, although typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor IA core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.1.5.8 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point the THERMTRIP# signal will go active.

5.1.5.9 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE_THERM_STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual*.

5.1.5.10 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.1.5.11 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to 1, the processor will immediately reduce its power consumption using modulation of the internal processor IA core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor IA core's clock independently.

5.1.5.12 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor IA cores simultaneously.

5.1.6 Intel® Memory Thermal Management

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor, either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

Memory temperature can be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reports to the processor through the PECI 3.1 interface. This methodology is known as PECI injected temperatures, this is a method of Closed Loop Thermal Management (CLTM). CLTM requires the use of a physical thermal sensor. EXTTS# is another method of CLTM but it is only capable of reporting memory thermal status to the processor. EXTTS# consists of two GPIO pins on the PCH, where the state of the pins is communicated internally to the processor.

When a physical thermal sensor is not available to report temperature, the processor supports Open Loop Thermal Management (OLTM) that estimates the power consumed per rank of the memory using the processor's DRAM power meter. A per rank power is associated with the warm and hot thresholds that, when exceeded, may trigger memory thermal throttling.

5.1.7 Scenario Design Power (SDP)

Scenario Design Power (SDP) is a usage-based design specification, and provides additional guidance for an average power dissipation and junction temperature operating condition limit.

SDP requires that the POWER_LIMIT_1 (PL1) to be set to the cooling level capability (SDP level, or higher). While the SDP specification is characterized at Tj of 80 °C, the functional limit for the product remains at Tj_{MAX}. Customers may choose to program the TCC Offset to have TCC Activation at 80 °C, but it is not required.

The processors that have SDP specified can still exceed SDP under certain workloads such as TDP workloads. TDP power dissipation is still possible with the intended usage models, and protection mechanisms to handle levels beyond cooling capabilities are recommended. Intel recommends using such thermal control mechanisms to manage situations where power may exceed the thermal design capability.

Note: cTDP-Down mode is required for Intel Core products in order to achieve SDP.

Note: Although SDP is defined at 80 °C the TCC activation temperature is Tj_{MAX}.

5.2 H-Processor Line Thermal and Power Specifications

The following notes apply to Table 5-2 and Table 5-3.

Note	Definition
1	The TDP and Configurable TDP values are the average power dissipation in junction temperature operating condition limit, for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.
2	TDP workload may consist of a combination of processor IA core intensive and graphics core intensive applications.
3	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.
4	'Turbo Time Parameter' is a mathematical parameter (units of seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. refer to Section 5.1.3.2 for further information.
5	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
6	Processor will be controlled to specified power limit as described in Section 5.1.2. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
7	This is a hardware default setting and not a behavioral characteristic of the part.
8	For controllable turbo workloads, the PL2 limit may be exceeded for up to 10 ms.
9	Refer to Table 5-1 for the definitions of 'base', 'TDP-Up' and 'TDP-Down'.
10	LPM power level is an opportunistic power and is not a guaranteed value as usages and implementations may vary.
11	Power limits may vary depending on if the product supports the 'TDP-up' and/or 'TDP-down' modes. Default power limits can be found in the PKG_PWR_SKU MSR (614h).
12	The processor die and OPCM die do not reach maximum sustained power simultaneously since the sum of the 2 die's estimated power budget is controlled to be equal to or less than the package TDP (PL1) limit. For additional information, refer to the appropriate Mobile TMDG for more information (see Related Documents).

Note	Definition
13	cTDP down power is based on GT2 equivalent graphics configuration. cTDP down does not decrease the number of active Processor Graphics EUs, but relies on Power Budget Management (PL1) to achieve the specified power level.
14	May vary based on SKU.
15	cTDP Down = 3.5W for M5/M7 products, cTDP Down = 3.8W for M3 product.
16	Sustained residencies at high voltages and temperatures may temporarily limit turbo frequency.

Table 5-2. TDP Specifications (H-Processor Line)

Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Configuration	Processor IA Core Frequency	Graphics Core Frequency	Thermal Design Power (TDP) [w]	Scenario Design Power (SDP) [w]	Notes
H-Processor Line BGA	Quad Core GT4 65W with OPC	Base	2.8 GHz to 3.3 GHz	350 MHz to 1.15 GHz	65	N/A	1,9,10, 11,12, 16
		LPM	800 MHz	350 MHz	64.5		
	Quad Core GT4 45W with OPC	Base	2.3 GHz to 3.0 GHz	350 MHz to 1.05 GHz	45	N/A	1,9,10, 11,12, 16
		Configurable TDP Down/LFM	1.9 GHz to 2.5 GHz		35		
		LPM	800 MHz	350 MHz	34.5		
	Quad Core GT4 35W with OPC	Base	2.5 GHz to 3.5 GHz	350 MHz to 1.15 GHz	35	N/A	1,9,10, 11,12, 16
		LPM	800 MHz	350 MHz	34.5		
	Quad Core GT2 45W	Base	2.3 GHz to 2.9 GHz	350 MHz to 1.05 GHz	45	N/A	1, 9, 10, 11, 16
		Configurable TDP-Down/LFM	1.6 GHz to 2.4 GHz	350 MHz	35		
		LPM	800 MHz	350 MHz	34.5		
	Quad Core GT2 35W	Base	2.7 GHz	350 GHz to 0.9 GHz	35	N/A	1,9,10, 11,12, 16
		LPM	800 MHz	350 MHz	34.5		

Table 5-3. Junction Temperature Specifications (H-Processor Line)

Segment	Symbol	Package Turbo Parameter	Temperature Range		TDP Specification Temperature Range		Units	Notes
			Min.	Max.	Min.	Max.		
H-processor line BGA	T_j	Junction temperature limit	0	100	0	100	ºC	1, 2

Notes:
1. The thermal solution needs to ensure that the processor temperature does not exceed the TDP Specification Temperature.
2. The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Section 5.1.5.2.1.
3. For this SKU to be specification compliance to the 90 ºC TDP specification temperature, a TCC Offset = 10 and a Tau value must be programed into MSR 1A2h. The recommended TCC_Offset averaging Tau value is 5s.

6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The notations in the following table are used to describe the signal type.

The signal description also includes the type of buffer used for the particular signal (see the following table).

Table 6-1. Signal Tables Terminology

Notation	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
SE	Single Ended Link
Diff	Differential Link
CMOS	CMOS buffers. 1.05V- tolerant
OD	Open Drain buffer
LPDDR3	LPDDR3 buffers: 1.2V- tolerant
DDR4	DDR4 buffers: 1.2V-tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
Ref	Voltage reference signal
Availability	Signal Availability condition - based on segment, SKU, platform type or any other factor
Asynchronous [1]	Signal has no timing relationship with any reference clock.
Note: 1. Qualifier for a buffer type.	

6.1 System Memory Interface

Table 6-2. LPDDR3 Memory Interface (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	**Data Buses:** Data signals interface to the SDRAM data buses.	I/O	LPDDR3	SE	All processor lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	LPDDR3	Diff	All processor lines

Table 6-2. LPDDR3 Memory Interface (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/ DDR1_CKP and the negative edge of their complement DDR0_CKN /DDR1_CKN are used to sample the command and control signals on the SDRAM.	O	LPDDR3	Diff	All processor lines
DDR0_CKE[3:0] DDR1_CKE[3:0]	**Clock Enable:** (1 per rank) These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR.	O	LPDDR3	SE	All processor lines.
DDR0_CS#[1:0] DDR1_CS#[1:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	LPDDR3	SE	All processor lines
DDR0_ODT[3:0] DDR1_ODT[3:0]	**On Die Termination:** Active Termination Control.	O	LPDDR3	SE	All processor lines
DDR0_CAA[9:0] DDR1_CAA[9:0]	**Command Address:** These signals are used to provide the multiplexed command and address to the SDRAM.	O	LPDDR3	SE	All processor lines
DDR0_CAB[9:0] DDR1_CAB[9:0]	**Command Address:** These signals are used to provide the multiplexed command and address to the SDRAM.	O	LPDDR3	SE	All processor lines
DDR0_VREF_DQ DDR1_VREF_DQ	**Memory Reference Voltage for DQ:**	O	A	SE	All processor lines
DDR_VREF_CA	**Memory Reference Voltage for Command & Address:**	O	A	SE	All processor lines
DDR_VTT_CNTL	**System Memory Power Gate Control:** When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and deeper and S3.	O	LPDDR3	SE	All processor lines

Table 6-3. DDR4 Memory Interface (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_ECC[7:0] DDR1_ECC[7:0]	**ECC Data Buses:** Data buses for ECC Check Byte.	I/O	DDR4	SE	ECC UDIMM/SODIM Modules with H-processor line processors
DDR0_DQ[63:0] DDR1_DQ[63:0]	**Data Buses:** Data signals interface to the SDRAM data buses.	I/O	DDR4	SE	All processor lines
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in H-processor line processors
DDR0_CKN[3:0] DDR0_CKP[3:0] DDR1_CKN[3:0] DDR1_CKP[3:0]	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/ DDR1_CKP and the negative edge of their complement DDR0_CKN /DDR1_CKN are used to sample the command and control signals on the SDRAM.	O	DDR4	Diff	[1:0] applicable for All processor lines. [3:2] applicable only in H-processor line processors
DDR0_CKE[3:0] DDR1_CKE[3:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).	O	DDR4	SE	[1:0] applicable for All processor lines. [3:2] applicable only in H-processor line processors.
DDR0_CS#[3:0] DDR1_CS#[3:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	DDR4	SE	[1:0] applicable for All processor lines. [3:2] applicable only H-processor line processors
DDR0_ODT[3:0] DDR1_ODT[3:0]	**On Die Termination:** (1 per rank). Active SDRAM Termination Control.	O	DDR4	SE	[0] applicable for All processor lines. [1] applicable for H - processor line processors. [3:2] H-processor line processors
DDR0_MA[16:0] DDR1_MA[16:0]	**Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. • A[16:14] use also as command signals, see ACT# signal description. • A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge). • A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. • A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH, no burst chop; LOW: burst chopped).	O	DDR4	SE	All processor lines

Table 6-3. DDR4 Memory Interface (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_ACT# DDR1_ACT#	**Activation Command:** ACT# HIGH along with CS# determines that the signals addresses below have command functionality. A16 use as RAS# signal A15 use as CAS# signal A14 use as WE# signal	O	DDR4	SE	All processor lines
DDR0_BG[1:0] DDR1_BG[1:0]	**Bank Group:** BG[0:1] define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.	O	DDR4	SE	All processor lines x8 DRAM device use BG[1:0], x16 use only BG[0].
DDR0_BA[1:0] DDR1_BA[1:0]	**Bank Address:** BA[1:0] define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.	O	DDR4	SE	All processor lines
DDR0_ALERT# DDR1_ALERT#	**Alert:** This signal is used at command training only. It is getting the Command and Address Parity error flag during training. CRC feature is not supported.	I	DDR4	SE	All processor lines
DDR0_PAR DDR1_PAR	**Command and Address Parity:** These signals are used for parity check.	O	DDR4	SE	All processor lines
DDR_VREF_CA	**Memory Reference Voltage for Command & Address:**	O	A	SE	All processor lines
DDR_VTT_CNTL	**System Memory Power Gate Control:** When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and deeper and S3.	O	DDR4	SE	All processor lines

Table 6-4. System Memory Reference and Compensation Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR_RCOMP[2:0]	**System Memory Resistance Compensation:**	N/A	A	SE	All processor lines
OPC_RCOMP	**On Package Cache resistance Compensation from processor:**	N/A	A	SE	H-Processor lines with On Package Cache
OPCE_RCOMP	**On Package Cache resistance Compensation from OPC:**	N/A	A	SE	H-Processor lines with On Package Cache

6.2 PCI Express* Graphics (PEG) Signals

Table 6-5. PCI Express* Interface

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PEG_RCOMP	Resistance Compensation for PCI Express channels PEG and DMI.	N/A	A	SE	H-processor line
PEG_RXP[15:0] PEG_RXN[15:0]	PCI Express Receive Differential Pairs.	I	PCI Express*	Diff	
PEG_TXP[15:0] PEG_TXN[15:0]	PCI Express Transmit Differential Pairs.	O	PCI Express*	Diff	

6.3 Direct Media Interface (DMI) Signals

Table 6-6. DMI Interface Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DMI_RXP[3:0] DMI_RXN[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pairs.	I	DMI	Diff	H-processor line
DMI_TXP[3:0] DMI_TXN[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pairs.	O	DMI	Diff	

6.4 Reset and Miscellaneous Signals

Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	All processor lines.
CFG_RCOMP	**Configuration Resistance Compensation**	N/A	N/A	SE	All processor lines
RESET#	Platform Reset pin driven by the PCH.	I	CMOS	SE	H-processor line
PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for the processor.			N/A	All processor lines
PROC_TRIGIN	Debug pin.	I	CMOS	SE	H-processor line
PROC_TRIGOUT	Debug pin.	O	CMOS	SE	H-processor line
PROC_AUDIO_SDI	**Processor Audio Serial Data Input:** This signal is an input to the processor from the PCH.	I	AUD	SE	H-processor line
PROC_AUDIO_SDO	**Processor Audio Serial Data Output:** This signal is an output from the processor to the PCH.	O	AUD	SE	
PROC_AUDIO_CLK	**Processor Audio Clock**	I	AUD	SE	

6.5 embedded DisplayPort* (eDP*) Signals

Table 6-8. embedded DisplayPort* Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
eDP_TXP[3:0] eDP_TXN[3:0]	**embedded DisplayPort Transmit:** differential pair	O	eDP	Diff	All processor lines
eDP_AUXP eDP_AUXN	**embedded DisplayPort Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair.	O	eDP	Diff	All processor lines
eDP_DISP_UTIL	**embedded DisplayPort Utility:** Output control signal used for brightness correction of embedded LCD displays with backlight modulation. This pin will co-exist with functionality similar to existing BKLTCTL pin on PCH	O	Async CMOS	SE	All processor lines
eDP_RCOMP	**DDI IO Compensation resistor, supporting DP*, eDP* and HDMI* channels.**	N/A	A	SE	All processor lines
Note: 1. When using eDP* bifurcation: — x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1]) — x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])					

6.6 Display Interface Signals

Table 6-9. Display Interface Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDI1_TXP[3:0] DDI1_TXN[3:0] DDI2_TXP[3:0] DDI2_TXN[3:0] DDI3_TXP[3:0] DDI3_TXN[3:0]	**Digital Display Interface Transmit:** Differential Pairs	O	DP/HDMI*	Diff	All processor lines. DDI3_TXP[3:0] DDI3_TXN[3:0] DDI3_AUXP DDI3_AUXN are present in H processor line.
DDI1_AUXP DDI1_AUXN DDI2_AUXP DDI2_AUXN DDI3_AUXP DDI3_AUXN	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	O	DP/HDMI*	Diff	

6.7 Processor Clocking Signals

Table 6-10. Processor Clocking Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H-processor line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

6.8 Testability Signals

Table 6-11. Testability Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	All processor lines
PROC_PRDY#	**Probe Mode Ready:** PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	All processor lines
PROC_PREQ#	**Probe Mode Request:** PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	All processor lines
PROC_TCK	**Test Clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal must be driven low or allowed to float during power on Reset.	I	GTL	SE	All processor lines
PROC_TDI	**Test Data In:** This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	All processor lines
PROC_TDO	**Test Data Out:** This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	All processor lines
PROC_TMS	**Test Mode Select:** A JTAG specification support signal used by debug tools.	I	GTL	SE	All processor lines
PROC_TRST#	**Test Reset:** Resets the Test Access Port (TAP) logic. This signal must be driven low during power on Reset.	I	GTL	SE	All processor lines

6.9 Error and Thermal Protection Signals

Table 6-12. Error and Thermal Protection Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	O	OD	SE	All processor lines
PECI	**Platform Environment Control Interface:** A serial sideband interface to the processor. It is used primarily for thermal, power, and error management.	I/O	PECI, Async	SE	All processor lines
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O	OD	SE	All processor lines

6.10 Power Sequencing Signals

Table 6-13. Power Sequencing Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PROCPWRGD	**Processor Power Good:** The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.	I	CMOS	SE	All processor lines
VCCST_PWRGD	**VCCST Power Good:** The processor requires this input signal to be a clean indication that the VCCST and VDDQ power supplies are stable and within specifications. This signal must have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.	I	CMOS	SE	All processor lines
PROC_DETECT#/SKTOCC#	**Processor Detect/Socket Occupied:** Pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	N/A	N/A	SE	All processor lines
VIDSOUT VIDSCK VIDALERT#	**VIDSOUT, VIDSCK, VIDALERT#:** These signals comprise a three-signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.	I/O O I	OD (open drain)	SE	All processor lines
PM_SYNC	**Power Management Sync:** A sideband signal to communicate power management status from the PCH to the processor. PCH report EXTTS#/EVENT# status to the processor.	I	CMOS	SE	H-processor line
PM_DOWN	**Power Management Down:** Sideband to PCH. Indicates processor wake up event EXTTS# on PCH. The processor combines the pin status into the OLTM/CLTM.	O	CMOS	SE	H-processor line
MSM#	**Minimum Speed Mode:** Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).	O	CMOS	SE	Processors w/ on package cache
ZVM#	**Zero Voltage Mode:** Control Signal to OPC and EOPIO VRs, when low OPC and EOPIO VRs output is 0V. ZVM# high voltage level is VDDQ.	O	CMOS	SE	Processors w/ on package cache

6.11 Processor Power Rails

Table 6-14. Processor Power Rails Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
Vcc	Processor IA cores power rail	I	Power	-	All processor lines
Vcc_{GT}	Processor Graphics power rail	I	Power	-	All processor lines
Vcc_{GTX}	Processor Graphics power rail (extension)	I	Power	-	Processors w/ GT3/4
V_{DDQ}	System Memory power rail	I	Power	-	All processor lines
V_{DDQC}	System Memory clock power rail, feeds from VDDQ through LP filter.	I	Power	-	H-processor lines
Vcc_{SA}	Processor System Agent power rail	I	Power	-	All processor lines
Vcc_{IO}	Processor I/O power rail.Consists of V_{CCIO} and V_{CCIO_DDR}. V_{CCIO} and V_{CCIO_DDR} should be isolated from each other.	I	Power	-	All processor lines
Vcc_{ST}	Sustain voltage for processor standby modes	I	Power	-	All processor lines
Vcc_{STG}	Gated sustain voltage for processor standby modes	I	Power	-	H-processor lines
Vcc_{PLL}	Processor PLLs power rails	I	Power	-	All processor lines
Vcc_{PLL_OC}	Processor PLLs power rails	I	Power	-	All processor lines
Vcc_{OPC}	Processor OPC power rails	I	Power	-	Processors w/ on package cache
Vcc_{OPC_1p8}	Processor OPC power rails	I	Power	-	Processors w/ on package cache
Vcc_{EOPIO}	Processor OPC power rails	I	Power	-	Processors w/ on package cache
Vcc_SENSE Vss_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	-	All processor lines
Vcc_{GT}_SENSE Vss_{GT}_SENSE					All processor lines
Vcc_{GTx}_SENSE Vss_{GTx}_SENSE					Processors w/ GT3/4
Vcc_{IO}_SENSE Vss_{IO}_SENSE					All processor lines
Vcc_{SA}_SENSE Vss_{SA}_SENSE					All processor lines
Vcc_{OPC}_SENSE Vss_{OPC}_SENSE					Processors w/ on package cache
Vcc_{EOPIO}_SENSE Vss_{EOPIO}_SENSE					Processors w/ on package cache

6.12 Ground, Reserved and Non-Critical to Function (NCTF) Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Table 6-15.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground the resistor can also be used for system testability.

Table 6-15. GND, RSVD, and NCTF Signals

Signal Name	Description
Vss	Processor ground node
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.

6.13 Processor Internal Pull-Up/Pull-Down Terminations

Table 6-16. Processor Internal Pull-Up/Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	Vcc_{IO}	16-60 Ω
PREQ#	Pull Up	Vcc_{ST}	3 kΩ
PROC_TDI	Pull Up	Vcc_{STG}	3 kΩ
PROC_TMS	Pull Up	Vcc_{SGT}	3 kΩ
PROC_TRST#	Pull Down	-	3 kΩ
CFG[19:0]	Pull Up	Vcc_{IO}	3 kΩ

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7 Electrical Specifications

7.1 Processor Power Rails

Table 7-1. Processor Power Rails

Power Rail	Description	Control	Availability
V_{CC}	Processor IA Cores Power Rail	SVID	All processor lines
Vcc_{GT}	Processor Graphics Power Rails	SVID	All processor lines
Vcc_{GTX} Note 2,6	Processor Graphics Extended Power Rail	SVID	Processors w/ GT3/4
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)	All processor lines
Vcc_{IO}	IO Power Rail	Fixed	All processor lines
Vcc_{ST}	Sustain Power Rail	Fixed	All processor lines
Vcc_{STG} Note 5	Sustain Gated Power Rail	Fixed	H-processor lines
Vcc_{PLL}	Processor PLLs power Rail	Fixed	All processor lines
Vcc_{PLL_OC} Note 4	Processor PLLs OC power Rail	Fixed	All processor lines
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	All processor lines
Vcc_{OPC} Note 3	Processor OPC power Rail	Fixed	Processors w/OPC
Vcc_{OPC_1P8} Note 3	Processor OPC power Rail	Fixed	Processors w/OPC
Vcc_{EOPIO} Note 3	Processor EOPIO power Rail	Fixed	Processors w/OPC

Notes:
1. N/A
2. Rail is unconnected for Processors without GT3/4.
3. Rail is unconnected for Processors without OPC.
4. VCC_{PLL_OC} power rail should be sourced from the VDDQ VR. The connection can be direct or through a load switch, depending desired power optimization. In case of direct connection (VCC_{PLL_OC} is shorted to VDDQ, no load switch), platform should ensure that Vcc_{ST} is ON (high) while VCC_{PLL_OC} is ON (high).
5. VCC_{STG} power rail should be sourced from the VR as VCC_{ST}. The connection can be direct or through a load switch, depending desired power optimization.
6. N/A

7.1.1 Power and Ground Pins

All power pins must be connected to their respective processor power planes, while all VSS pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop.

7.1.2 V_{CC} Voltage Identification (VID)

Intel processors/chipsets are individually calibrated in the factory to operate on a specific voltage/frequency and operating-condition curve specified for that individual processor. In normal operation, the processor autonomously issues voltage control requests according to this calibrated curve using the serial voltage-identifier (SVID) interface. Altering the voltage applied at the processor/chipset causing operation outside of this calibrated curve is considered out-of-specification operation.

The SVID bus consists of three open-drain signals: clock, data, and alert# to both set voltage-levels and gather telemetry data from the voltage regulators. Voltages are controlled per an 8-bit integer value, called a VID, that maps to an analog voltage level. An offset field also exists that allows altering the VID table. Alert can be used to inform the processor that a voltage-change request has been completed or to interrupt the processor with a fault notification.

For VID coding and further details, refer to the IMVP8 PWM Specification.

7.2 DC Specifications

The processor DC specifications in this section are defined at the processor signal pins, unless noted otherwise.

- The DC specifications for the /LPDDR3/DDR4 signals are listed in the *Voltage and Current Specifications* section.
- The *Voltage and Current Specifications* section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

7.2.1 Processor Power Rails DC Specifications

7.2.1.1 Vcc DC Specifications

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1]
Operating Voltage	Voltage Range for Processor Active Operating Mode	All	0.55	—	1.52	V	1,2,3, 7,12
Idle Voltage	Voltage Range for Processor Idle Mode (Package C6/ C7)	All	0	—	0.55	V	1,2,3, 7
I_{CCMAX}	Maximum Processor IA Core I_{CC}	H(35W) - quad core GT2	—	—	60	A	4,6,7, 11
		H(45W) - quad core GT2	—	—	68		
		H(35W) - quad core GT4+OPC	—	—	66		
		H(45,65W) - quad core GT4+OPC	—	—	74		
TOB_{VCC}	Voltage Tolerance	PS0, PS1	—	—	±20	mV	3, 6, 8
		PS2, PS3	—	—	±20		

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min.	Typ.	Max.			Unit	Note[1]
					$I_L \leq 0.5$	$0.5<I_L<I_{CCTDC}$	$I_{CCTDC}<I_L<I_{CCMax}$		
Ripple	Ripple Tolerance	PS0	—	—	+30/-10	±10	±15	mV	3, 6, 8
		PS1	—	—	+30/-10	±15	±15		
		PS2	—	—	+30/-10	+30/-10	+30/-10		
		PS3	—	—	+30/-10	+30/-10	+30/-10		
DC_LL	Loadline slope within the VR regulation loop capability	H-dual/quad core GT2 H-quad core GT4+OPC	—	—	1.8 1.6			mΩ	10,13, 14
AC_LL	AC Loadline	H-processor line	—	—	Same as Max DC_LL (up to 400 KHz)			mΩ	10,13, 14
T_OVS_TDP_Max	Max Overshoot time **TDP/virus mode**	—	—	—	10/30			µs	
V_OVS TDP_Max/ virus_Max	Max Overshoot at **TDP/virus mode**	—	—	—	70/200			mV	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep® Technology, or low-power states).
3. The voltage specification requirements are measured across Vcc_SENSE and Vss_SENSE as near as possible to the processor with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Processor IA core VR to be designed to electrically support this current.
5. Processor IA core VR to be designed to thermally support this current indefinitely.
6. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
7. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
8. PSx refers to the voltage regulator power state as set by the SVID protocol.
9. N/A
10. LL measured at sense points.
11. Typ column represents ICCmax for commercial application it is NOT a specification - it is a characterization of limited samples using limited set of benchmarks that can be exceeded.
12. Operating voltage range in steady state.
13. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
14. By Improving Load Line (Lower LL than datasheet values, and reporting it to BIOS), customers may obtain slightly better performance; although, the frequencies will not be changed.

7.2.1.2 Vcc_{GT} and Vcc_{GTX} DC Specifications

Table 7-3. Processor Graphics (Vcc_{GT} and Vcc_{GT-X}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.			Unit	Note[1]
Operating voltage	Active voltage Range for Vcc_{GT}	All	0.55	—	1.52			V	2,3,6,8
Idle voltage	Processor Graphics core idle voltage	All	0	—	0.55			V	3
I_{CCMax_GT}/ I_{CCMax_GTx}	Max Current for Processor Graphics Rail	H(35W)-dual core GT2 H(45W)-quad core GT2 H(35W) - quad core GT4+OPC H(45W) - quad core GT4+OPC H(65W) - quad core GT4+OPC	— — — — —	— — — — —	55 55 94/20(GTx) 94/20(GTx) 105/24(GTx)			A	6
TOB_{GT}	Vcc_{GT} Tolerance	PS0,PS1	—	—	±20			mV	3,4
		PS2,PS3	—	—	±20			mV	3,4
Ripple	Ripple Tolerance	—			$I_L \le 0.5$	$0.5<I_L<I_{CCTDC}$	$I_{CCTDC}<I_L<IccMax$	mV	3,4
		PS0	—	—	+30/-10	±10	±15		
		PS1	—	—	+30/-10	±15	±15		
		PS2	—	—	+30/-10	+30/-10	+30/-10		
		PS3	—	—	+30/-10	+30/-10	+30/-10		
DC_LL	vcc_{GT} Loadline slope	H-quad core GT2 H-quad core GT4+OPC	— —	— —	2.65 1.4/6.0(GTx)			mΩ	7,9,10
AC_LL	AC Loadline	H	—	—	Same as Max DC_LL (up to 400 KHz)			mΩ	7,9,10
T_OVS_Max	Max Overshoot time	—	—	—	10			µs	
V_OVS_Max	Max Overshoot	—	—	—	70			mV	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep® Technology, or low-power states).
3. The voltage specification requirements are measured across Vcc_{GT}_SENSE and Vss_{GT}_SENSE as near as possible to the processor with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep® Technology, or low-power states).
6. N/A
7. LL measured at sense points.
8. Operating voltage range in steady state.
9. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
10. By Improving Load Line (Lower LL than datasheet values, and reporting it to BIOS), customers may obtain slightly better performance, although the frequencies will not be changed.
11. N/A
12. For merged GT/GTx rails, the sense point need to be taken from VCCGT_SENSE/VSSGT_SENSE, the VCCGTx_SENSE/VSSGTx_SENSE should be unconnected (not connected). For merged VRs, IccMAX=GT+GTx IccMAX = 57A+7A=64A."

7.2.1.3 V_{DDQ} DC Specifications

Table 7-4. Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1]
$V_{DDQ\ (LPDDR3)}$	Processor I/O supply voltage for LPDDR3	All	Typ-5%	1.20	Typ+5%	V	3,4
$V_{DDQ\ (DDR4)}$	Processor I/O supply voltage for DDR4	All	Typ-5%	1.20	Typ+5%	V	3,4
TOB_{VDDQ}	VDDQ Tolerance	All	AC+DC:± 5			%	3,4
$Icc_{MAX\_VDDQ\ (LPDDR3)}$	Max Current for V_{DDQ} Rail (LPDDR3)	H	—	—	2.8	A	2
$Icc_{MAX\_VDDQ\ (DDR4)}$	Max Current for V_{DDQ} Rail (DDR4)	H	—	—	2.8	A	2

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. The current supplied to the DIMM modules is not included in this specification.
3. No requirement on the breakdown of AC versus DC noise.
4. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

7.2.1.4 Vcc_{SA} DC Specifications

Table 7-5. System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min.	Typ.	Max.			Unit	Note[1,2]
Vcc_{SA}	Voltage for the System Agent	H-processor line	0.55	—	1.52			V	3,5
TOB_{VCCSA}	V_{CCSA} Tolerance	H-processor lines	±20					mV	3
I_{CCMAX_VCCSA}	Max Current for V_{CCSA} Rail	H-quad core GT2 H-quad core GT4+OPC	—	—	11.1 8			A	
DC_LL	vcc_{SA} Loadline	H-quad core GT2 H-quad core GT4+OPC	—	—	10 6			mΩ	6,7
AC_LL	AC Loadline	H	—	—	Same as Max DC_LL (up to 400 KHz)			mΩ	6,7
Ripple	Ripple Tolerance	H-Processor			$I_L \le 0.5$	$0.5 < I_L < I_{CCTDC}$	$I_{CCTDC} < I_L <$ Icc Max	mV	3, 4
		PS0	—	—	+30/ -10	±10	±15		
		PS1	—	—	+30/ -10	±15	±15		
		PS2	—	—	+30/ -10	+30/-10	+30/-10		
		PS3	—	—	+30/ -10	+30/-10	+30/-10		

Table 7-5. System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1,2]
T_OVS_Max	Max Overshoot time	—	—	—	10	µs	
V_OVS_Max	Max Overshoot	—	—	—	70	mV	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on Vcc_{SA}_SENSE and Vss_{SA}_SENSE with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. VCC_{SA} voltage during boot (Vboot)1.05V for a duration of 2 seconds.
6. LL measured at sense points.
7. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.

7.2.1.5 Vcc_{IO} DC Specifications

Table 7-6. Processor I/O (Vcc_{IO}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1,2]
V_{CCIO}	Voltage for the memory controller and shared cache	H	—	0.95	—	V	3,4,5,6
TOB_{VCCIO}	V_{CCIO} Tolerance	All	AC+DC: ±50			mV	3
I_{CCMAX_VCCIO}	Max Current for V_{CCIO} Rail	H	—	—	5.5	A	
T_OVS_Max	Max Overshoot time	All	—	—	100	µs	7
V_OVS_Max	Max Overshoot at TDP	All	—	—	20	mV	7

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc_{IO}_SENSE and Vss_{IO}_SENSE as near as possible to the processor with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. For low BW bus connection between processor and PCH -> VCCIO=0.85V.
5. For high BW bus connection between processor and PCH -> VCCIO=0.95V.
6. OS occurs during power on only. **not** during normal operation

7.2.1.6 Vcc_{OPC} DC Specifications

OPC VR output voltage is fixed to 1V, the processor can drive VR to LPM (Low Power Mode), which sets VR output to 0V using ZVM# signal as shown below.

Table 7-7. VCC_{OPC} Voltage levels

ZVM# state	VCC_{OPC}	Units
0	0	V
1	1.0/1.05 (Based on SKU)	V

Table 7-8. Processor OPC (Vcc_{OPC}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1,2]
V_{CCOPC}	Voltage for the On Package Cache	Processor line w/OPC: H	—	1.05	—	V	3,5
TOB_{VCCOPC}	V_{CCOPC} Tolerance	Processor line w/OPC	AC+DC: ±5			%	3
I_{CCMAX_VCCOPC}	Max. Current for V_{CCOPC} Rail	H	—	—	4.7	A	5
T_OVS_Max	Max. Overshoot time	All	—	—	100	uS	4
V_OVS_Max	Max. Overshoot at TDP	All	—	—	20	mV	4

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max./Min. functional limits.
3. The voltage specification requirements are measured on VccOPC_ESNSE and VssOPC_SENSE as near as possible to the processor with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-M ? minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. OS occurs during power on only. **not** during normal operation
5. For H-processor line, in order to increase BW, the option of VCCOPC=1.1V is under evaluation.

7.2.1.7 Vcc_{EOPIO} DC Specifications

VCC_{EOPIO} may be connected to OPC VR. The processor can drive VR to LPM (Low-Power Mode), which sets VR output to 0V using ZVM# signal (as shown in VCC_{EOPIO} Voltage levels in the following table).

Table 7-9. VCC_{EOPIO} Voltage Levels (Separate VR)

ZVM# State	MSM# State	VCC_{EOPIO}	Units
0	X	0	V
1	1	1.0/1.1 (Based on SKU)	V

Table 7-10. Processor EOPIO (Vcc_{EOPIO}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ.	Max	Unit	Note[1,2]
$V_{CCEOPIO}$	Voltage for the EOPIO interface	Processor line w/OPC: H	—	1.1	—	V	3
$TOB_{VCCEOPIO}$	$V_{CCEOPIO}$ Tolerance	Processor line w/OPC	AC+DC: ±5			%	3
$I_{CCMAX\_VCCEOPIO}$	Max Current for $V_{CCEOPIO}$ Rail	H	—	—	2.8	A	

Table 7-10. Processor EOPIO (Vcc_{EOPIO}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ.	Max	Unit	Note[1,2]
T_OVS_Max	Max Overshoot time	All	—	—	100	uS	4
V_OVS_Max	Max Overshoot at TDP	All	—	—	20	mV	4

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on VccEOPIO_ESNSE and VssEOPIO_SENSE with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. OS occurs during power on only; **not** during normal operation.

7.2.1.8 VCC_OPC_1p8 DC Specifications

Table 7-11. Processor OPC (VCC_OPC_1p8) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1,2]
$V_{CC\_OPC\_1p8}$	Voltage for the On Package Cache	Processor line w/OPC	—	1.8	—	V	3
$TOB_{VCC\_OPC\_1p8}$	$V_{CC\_OPC\_1p8}$ Tolerance	Processor line w/OPC	AC+DC:± 5			%	3
$I_{CCMAX\_VCC\_OPC\_1p8}$	Max Current for $V_{CC\_OPC\_1p8}$ Rail	H	—	—	50	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

7.2.1.9 Vcc_{ST} DC Specifications

Table 7-12. Vcc Sustain (Vcc_{ST}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Units	Notes [1,2]
Vcc_{ST}	Processor Vcc Sustain supply voltage	All	—	1.0	—	V	3
TOB_{ST}	Vcc_{ST} Tolerance	All	AC+DC:± 5			%	3
Icc_{MAX_ST}	Max Current for Vcc_{ST}	H	—	—	60	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

Table 7-13. Vcc Sustain Gated (Vcc_{STG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Units	Notes [1,2]
Vcc_{STG}	Processor Vcc Sustain Gated supply voltage	All	—	1.0	—	V	3
TOB_{STG}	V_{CCSTG} Tolerance	All	AC+DC: ±5			%	3
Icc_{MAX_STG}	Max Current for Vcc_{STG}	H	—	—	20	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

7.2.1.10 Vcc_{PLL} DC Specifications

Table 7-14. Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Notes[1,2]
V_{CCPLL}	PLL supply voltage (DC + AC specification)	All	—	1.0	—	V	3
TOB_{CCPLL}	V_{CCPLL} Tolerance	All	AC+DC:± 5			%	3
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail	H	—	—	150	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

Table 7-15. Processor PLL OC (Vcc_{PLL_OC}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Notes[1,2]
V_{CCPLL_OC}	PLL OC supply voltage (DC + AC specification)	All	—	VDDQ	—	V	3
TOB_{CCPLL_OC}	V_{CCPLL_OC} Tolerance	All	AC+DC:± 5			%	3
$I_{CCMAX\_VCCPLL\_OC}$	Max Current for V_{CCPLL_OC} Rail	H-quad core GT2 H-quad core GT4+OPC	—	—	130 150	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

7.2.2 Processor Interfaces DC Specifications

7.2.2.1 LPDDR3 DC Specifications

Table 7-16. LPDDR3 Signal Group DC Specifications

Symbol	Parameter	U and Y-Processor Line			Unit	Notes
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	—	V_{DDQ} /2	0.43*V_{DDQ}	V	2, 4, 10
V_{IH}	Input High Voltage	0.57*V_{DDQ}	V_{DDQ} /2	—	V	3, 4, 10
$R_{ON\_UP/DN(DQ)}$	LPDDR3 Data Buffer pull-up/ down Resistance	Trainable			Ω	12
$R_{ODT(DQ)}$	LPDDR3 On-die termination equivalent resistance for data signals	Trainable			Ω	12
$V_{ODT(DC)}$	LPDDR3 On-die termination DC working point (driver set to receive mode)	0.45*V_{DDQ}	0.5*V_{DDQ}	0.55*V_{DDQ}	V	10
$R_{ON\_UP/DN(CK)}$	LPDDR3 Clock Buffer pull-up/ down Resistance	30	—	50	Ω	5, 12
$R_{ON\_UP/DN(CMD)}$	LPDDR3 Command Buffer pull-up/ down Resistance	Trainable			Ω	12
$R_{ON\_UP/DN(CTL)}$	LPDDR3 Control Buffer pull-up/ down Resistance	20	—	50	Ω	5, 12
$R_{ON\_UP/DN}$ (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up Resistance	40	—	140	Ω	-
I_{LI}	Input Leakage Current (DQ, CK) 0V 0.2* V_{DDQ} 0.8*V_{DDQ}	—	—	0.75	mA	-
I_{LI}	Input Leakage Current (CMD,CTL) 0V 0.2*V_{DDQ} 0.8*V_{DDQ}	—	—	0.9	mA	-
DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	Trainable	VDDQ/2	Trainable	V	13,14
DDR_RCOMP[0]	ODT resistance compensation	RCOMP values are memory topology dependent.			Ω	6
DDR_RCOMP[1]	Data resistance compensation				Ω	6
DDR_RCOMP[2]	Command resistance compensation				Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{IL} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.
6. DDR_RCOMP resistance must be provided on the system board with ±1% resistors. DDR_RCOMP resistors are to V_{SS}.
7. DDR_DRAMPWROK must have a maximum of 15 ns rise or fall time over V_{DDQ} * 0.30 ±100 mV and the edge must be monotonic.
8. DDR_VREF is defined as V_{DDQ}/2 for LPDDR3
9. N/A
10. Max-min range is correct but center point is subject to change during MRC boot training.
11. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
12. Final value determined by BIOS power training, values might vary between bytes and/or units.
13. VREF values determined by BIOS training, values might vary between units.
14. DDR0_Vref_DQ - Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0.

7.2.2.2 DDR4 DC Specifications

Table 7-17. DDR4 Signal Group DC Specifications

Symbol	Parameter	H-Processor Line			Units	Notes[1]
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	—	VREF(INT)	VREF(INT) - 0.07*VDDQ	V	2, 4, 10, 14
V_{IH}	Input High Voltage	VREF(INT) + 0.07*VDDQ	VREF(INT)	—	V	3, 4, 10, 14
$R_{ON\_UP/DN(DQ)}$	DDR4 Data Buffer pull-up/ down Resistance	Trainable			Ω	12
$R_{ODT(DQ)}$	DDR4 On-die termination equivalent resistance for data signals	Trainable			Ω	12
$V_{ODT(DC)}$	DDR4 On-die termination DC working point (driver set to receive mode)	0.45* V_{DDQ}	0.5* V_{DDQ}	0.55* V_{DDQ}	V	10
$R_{ON\_UP/DN(CK)}$	DDR4 Clock Buffer pull-up/ down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 12
$R_{ON\_UP/DN(CMD)}$	DDR4 Command Buffer pull-up/down Resistance	0.8*Typ	20	1.2*Typ	Ω	12
$R_{ON\_UP/DN(CTL)}$	DDR4 Control Buffer pull-up/down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 12
$R_{ON\_UP/DN}$ (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	—	140	Ω	-
I_{LI}	Input Leakage Current (DQ, CK) 0 V 0.2*V_{DDQ} 0.8*V_{DDQ}	—	—	1	mA	-
DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	Trainable	VDDQ/2	Trainable	V	13,15
DDR_RCOMP[0]	ODT resistance compensation	RCOMP values are memory topology dependent.			Ω	6
DDR_RCOMP[1]	Data resistance compensation				Ω	6
DDR_RCOMP[2]	Command resistance compensation				Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{IL} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.
6. DDR_RCOMP resistance must be provided on the system board with ±1% resistors installed on package). DDR_RCOMP resistors are to V_{SS}.
7. DDR_DRAMPWROK must have a maximum of 15 ns rise or fall time over V_{DDQ} * 0.30 ±100 mV and the edge must be monotonic.
8. DDR_VREF is defined as $V_{DDQ}/2$ for DDR4
9. N/A
10. Max-min range is correct but center point is subject to change during MRC boot training.
11. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
12. Final value determined by BIOS power training, values might vary between bytes and/or units.
13. VREF values determined by BIOS training, values might vary between units.
14. VREF(INT) is a trainable parameter where the value is determined by BIOS for margin optimization.
15. DDR0_Vref_DQ - Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0

7.2.2.3 PCI Express* Graphics (PEG) DC Specifications

Table 7-18. PCI Express* Graphics (PEG) Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes[1]
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω	1, 5
Z_{RX-DC}	DC Common Mode Rx Impedance	40	50	60	Ω	1, 4
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance	80	—	120	Ω	1
PEG_RCOMP	resistance compensation	24.75	25	25.25	Ω	2, 3

Notes:
1. Refer to the PCI Express Base Specification for more details.
2. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
3. PEG_RCOMP resistance must be provided on the system board with 1% resistors. COMP resistors are to VCCIO. PEG_RCOMP- Intel allows using 24.9 Ω 1% resistors.
4. DC impedance limits are needed to ensure Receiver detect.
5. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly.Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.

7.2.2.4 Digital Display Interface (DDI) DC Specifications

Table 7-19. Digital Display Interface Group DC Specifications (DP*/HDMI*)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes[1]
V_{IL}	Aux Input Low Voltage	—	—	0.8	V	
V_{IH}	Aux Input High Voltage	2.25	—	3.6	V	
V_{OL}	DDIB_TXC[3:0] Output Low Voltage DDIC_TXC[3:0] Output Low Voltage DDID_TXC[3:0] Output Low Voltage	—	—	$0.25*V_{CCIO}$	V	1,2
V_{OH}	DDIB_TXC[3:0] Output High Voltage DDIC_TXC[3:0] Output High Voltage DDID_TXC[3:0] Output High Voltage	$0.75*V_{CCIO}$	—	—	V	1,2
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	100		120	Ω	

Notes:
1. VCCIO depends on segment.
2. V_{OL} and V_{OH} levels depends on the level chosen by the Platform.

7.2.2.5 embedded DisplayPort* (eDP*) DC Specification

Table 7-20. embedded DisplayPort* (eDP*) Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{OL}	eDP_DISP_UTIL Output Low Voltage	—	—	$0.1*V_{CCIO}$	V
V_{OH}	eDP_DISP_UTIL Output High Voltage	$0.9*V_{CCIO}$	—	—	V
R_{UP}	eDP_DISP_UTIL Internal pull-up	100	—	—	Ω
R_{DOWN}	eDP_DISP_UTIL Internal pull-down	100	—	—	Ω

Table 7-20. embedded DisplayPort* (eDP*) Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Units
eDP_RCOMP	eDP resistance compensation	24.75	25	25.25	Ω
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω

Notes:
1. COMP resistance is to VCOMP_OUT.
2. eDP_RCOMP resistor must be provided on the system board.

7.2.2.6 CMOS DC Specifications

Table 7-21. CMOS Signal Group DC Specifications

Symbol	Parameter	Min.	Max.	Units	Notes[1]
V_{IL}	Input Low Voltage	—	Vcc * 0.3	V	2
V_{IH}	Input High Voltage	Vcc * 0.7	—	V	2, 4
V_{OL}	Output Low Voltage	—	Vcc * 0.1	V	2
V_{OH}	Output High Voltage	Vcc * 0.9	—	V	2, 4
R_{ON}	Buffer on Resistance	23	73	Ω	-
I_{LI}	Input Leakage Current	—	±150	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The Vcc referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$.
3. For VIN between "0" V and Vcc_{ST}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers must comply with the signal quality specifications.
5. N/A

7.2.2.7 GTL and OD DC Specifications

Table 7-22. GTL Signal Group and Open Drain Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min.	Max.	Units	Notes[1]
V_{IL}	Input Low Voltage (TAP, except PROC_TCK, PROC_TRST#)	—	Vcc * 0.6	V	2
V_{IH}	Input High Voltage (TAP, except PROC_TCK, PROC_TRST#)	Vcc * 0.72	—	V	2, 4
V_{IL}	Input Low Voltage (PROC_TCK,PROC_TRST#)	—	Vcc * 0.3	V	2
V_{IH}	Input High Voltage (PROC_TCK,PROC_TRST#)	Vcc * 0.3	—	V	2, 4
$V_{HYSTERESIS}$	Hysteresis Voltage	Vcc * 0.2	—	V	-
R_{ON}	Buffer on Resistance (TDO)	7	17	Ω	-
V_{IL}	Input Low Voltage (other GTL)	—	Vcc * 0.6	V	2
V_{IH}	Input High Voltage (other GTL)	Vcc * 0.72	—	V	2, 4
R_{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	-

Table 7-22. GTL Signal Group and Open Drain Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min.	Max.	Units	Notes[1]
R_{ON}	Buffer on Resistance (other GTL)	12	28	Ω	-
I_{LI}	Input Leakage Current	—	±150	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The Vcc_{ST} referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$.
3. For VIN between 0 V and Vcc_{ST}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers must comply with the signal quality specifications.
5. N/A
6. Those V_{IL}/V_{IH} values are based on ODT disabled (ODT Pull-up not exist).

7.2.2.8 PECI DC Characteristics

The PECI interface operates at a nominal voltage set by Vcc_{ST}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc_{ST} interface supply.

Vcc_{ST} nominal levels will vary between processor families. All PECI devices will operate at the Vcc_{ST} level determined by the processor installed in the system.

Table 7-23. PECI DC Electrical Limits

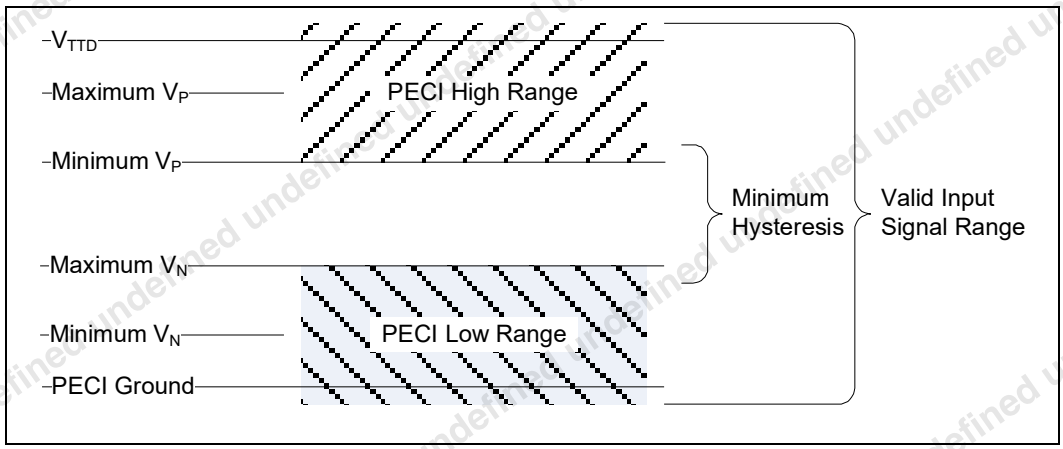
Symbol	Definition and Conditions	Min.	Max.	Units	Notes[1]
R_{up}	Internal pull up resistance	15	45	Ω	3
V_{in}	Input Voltage Range	-0.15	Vcc_{ST} + 0.15	V	-
$V_{hysteresis}$	Hysteresis	0.15 * Vcc_{ST}	—	V	-
V_{IL}	Input Voltage Low- Edge Threshold Voltage	—	0.3 * Vcc_{ST}	V	-
V_{IH}	Input Voltage High- Edge Threshold Voltage	0.7 * Vcc_{ST}	—	V	-
C_{bus}	Bus Capacitance per Node	N/A	10	pF	-
C_{pad}	Pad Capacitance	0.7	1.8	pF	-
Ileak000	leakage current @ 0V	—	0.6	mA	-
Ileak025	leakage current @ 0.25* Vcc_{ST}	—	0.4	mA	-
Ileak050	leakage current @ 0.50* Vcc_{ST}	—	0.2	mA	-
Ileak075	leakage current @ 0.75* Vcc_{ST}	—	0.13	mA	-
Ileak100	leakage current @ Vcc_{ST}	—	0.10	mA	-

Notes:
1. Vcc_{ST} supplies the PECI interface. PECI behavior does not affect Vcc_{ST} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull up resistance measured at 0.75* Vcc_{ST}.

Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.

Figure 7-1. Input Device Hysteresis



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8 Package Mechanical Specifications

8.1 Package Mechanical Attributes

The H-processor line use a Flip Chip technology available in a Ball Grid Array (BGA) package. The following table provides an overview of the mechanical attributes of the package. For specific dimensions (die size, die location, and so on), refer to the processor package mechanical drawings (see Related Documents section).

Table 8-1. Package Mechanical Attributes

Package	Parameter	H-Processor Line	
		Quad Core GT4+OPC	Quad Core GT2
Package Technology	Package Type	Flip Chip Ball Grid Array	
	Interconnect	Ball Grid Array (BGA)	
	Lead Free	Yes	
	Halogenated Flame Retardant Free	Yes	
Package Configuration	Solder Ball Composition	SAC405	
	Ball/Pin Count	1440	
	Grid Array Pattern	Balls Anywhere	
	Land Side Capacitors	Yes	
	Die Side Capacitors	Yes	
	Die Configuration	2 Dies MCP	1 Die Single-Chip Package
Package Dimensions	Nominal Package Size	42x28mm	
	Min Ball/Pin pitch	0.65	

8.2 Package Loading Specifications

Table 8-2. Package Loading Specifications

Maximum Static Normal Load	Limit	Minimum PCB Thickness Assumptions	Notes
H-processor line	67 N (15 lbf)	1.0 mm	1, 2, 3
	111 N (25 lbf)	1.0 mm	1, 2, 3

Notes:
1. The thermal solution attach mechanism must not induce continuous stress to the package. It may only apply a uniform load to the die to maintain a thermal interface.
2. This specification applies to the uniform compressive load in the direction perpendicular to the dies' top surface. Load should be centered on processor die center.
3. This specification is based on limited testing for design characterization.
4. This load limit assumes the use of a backing plate.

8.3 Package Storage Specifications

Table 8-3. Package Storage Specifications

Parameter	Description	Min.	Max.	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time.	-25 °C	125 °C	1, 2, 3
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		5, 6
$TIME_{SUSTAINED\ STORAGE}$	A prolonged or extended period of time: typically associated with customer shelf life.	0 months	6 months	6

Notes:
1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC standards.
3. $T_{ABSOLUTE\ STORAGE}$ applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel-branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{SUSTAINED\ STORAGE}$ and customer shelf life in applicable Intel boxes and bags.

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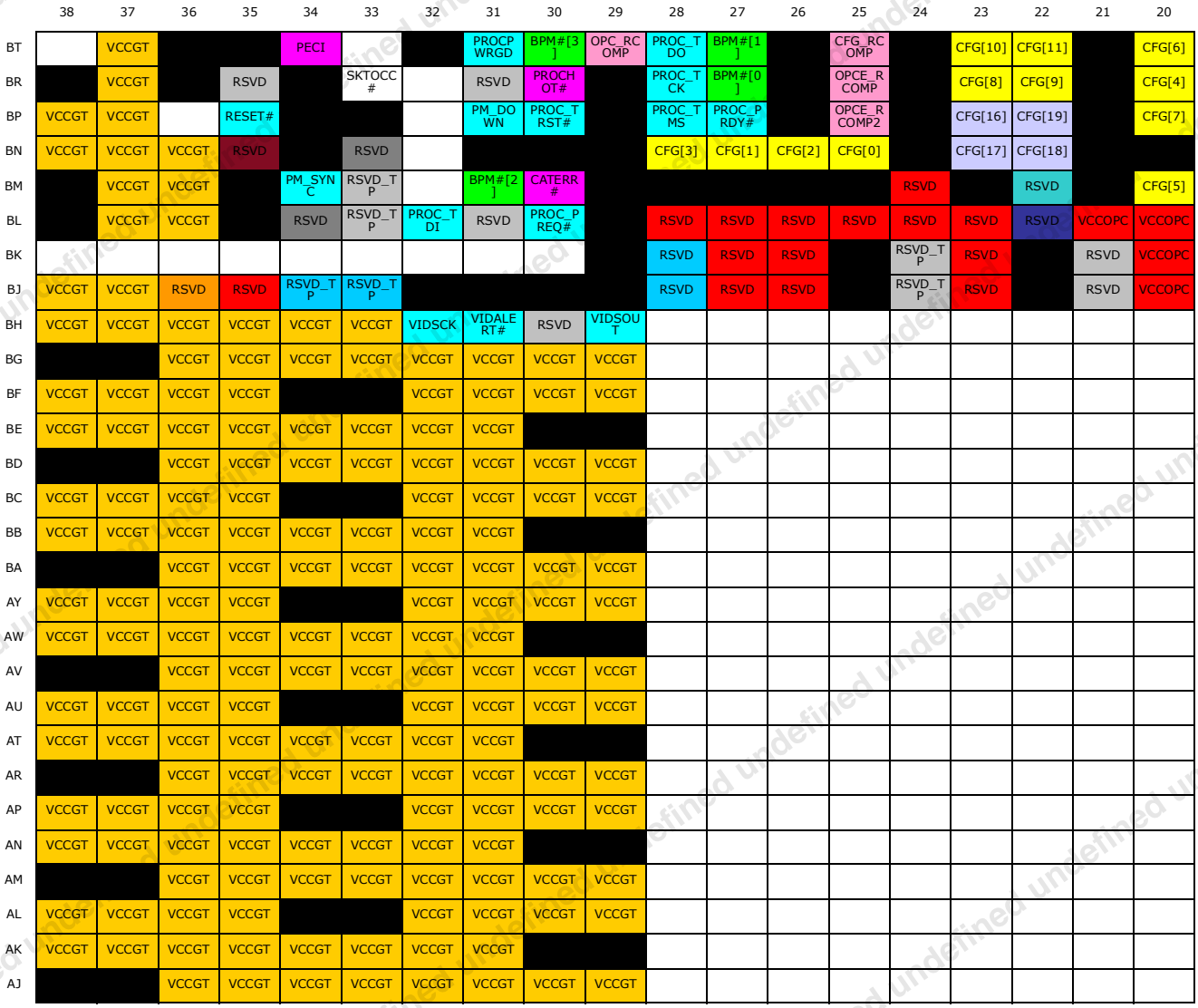
9 Processor Ball Information

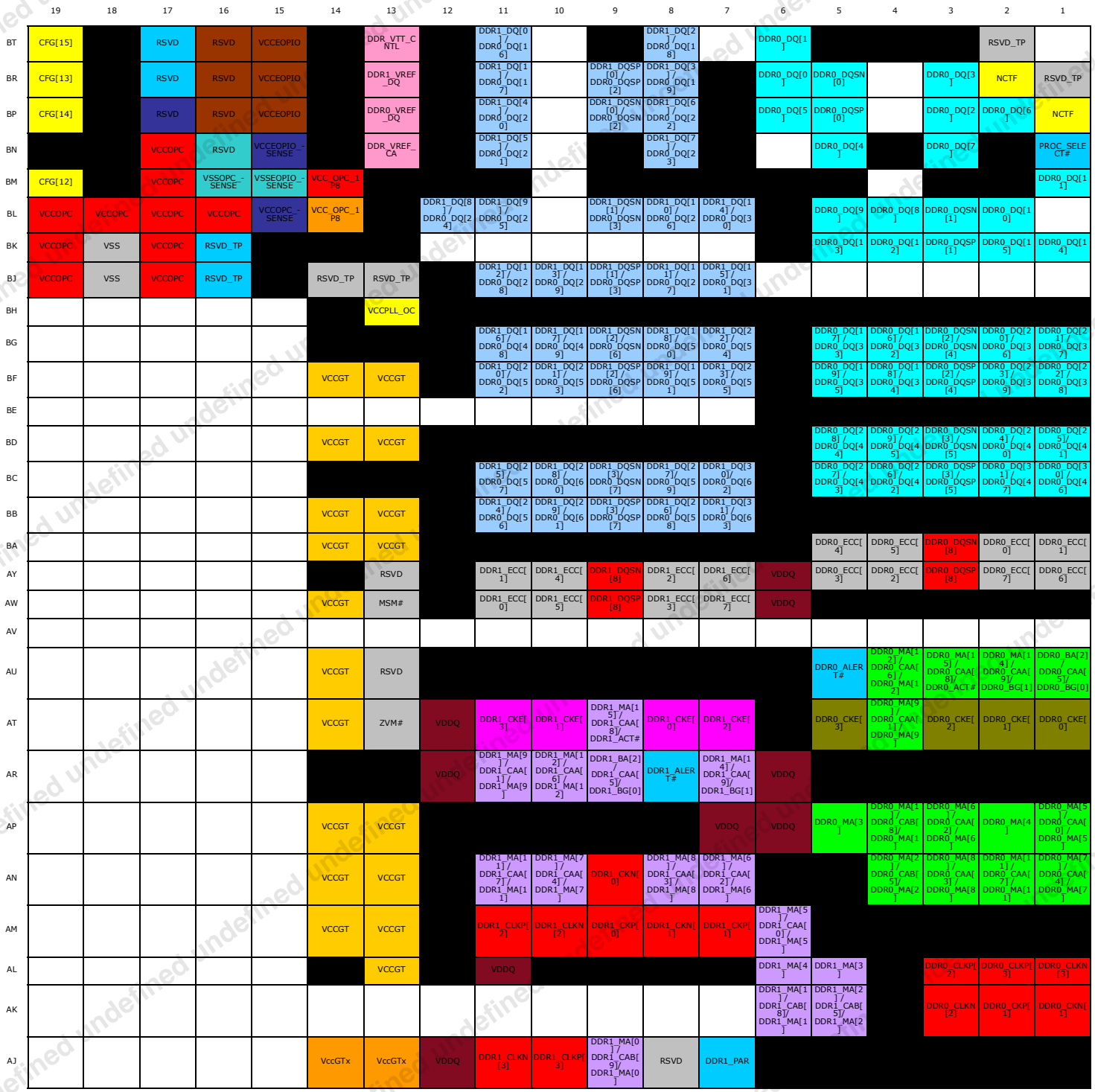
The processor is available in the BGA package (BGA1440). Figure 9-1, Figure 9-2, Figure 9-3, and Figure 9-4 provide a top view of the ball map per quadrant. Table 9-1 provides the ball list.

Figure 9-1. Ball Map (Top View, Upper-Left Quadrant)



	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
BT		VCCGT			PECI			PROCP WRGD	BPM#[3]	OPC_RCOMP	PROC_TDO	BPM#[1]		CFG_RCOMP		CFG[10]	CFG[11]		CFG[6]
BR		VCCGT		RSVD		SKTOCC#		RSVD	PROCHOT#		PROC_TCK	BPM#[0]		OPCE_RCOMP		CFG[8]	CFG[9]		CFG[4]
BP	VCCGT	VCCGT		RESET#				PM_DOWN	PROC_TRST#		PROC_TMS	PROC_PRDY#		OPCE_RCOMP2		CFG[16]	CFG[19]		CFG[7]
BN	VCCGT	VCCGT	VCCGT	RSVD		RSVD					CFG[3]	CFG[1]	CFG[2]	CFG[0]		CFG[17]	CFG[18]		
BM		VCCGT	VCCGT		PM_SYNC	RSVD_TP		BPM#[2]	CATERR#						RSVD		RSVD		CFG[5]
BL		VCCGT	VCCGT		RSVD	RSVD_TP	PROC_TDI	RSVD	PROC_PREQ#		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VCCOPC	VCCOPC
BK											RSVD	RSVD	RSVD		RSVD_TP	RSVD		RSVD	VCCOPC
BJ	VCCGT	VCCGT	RSVD	RSVD	RSVD_TP	RSVD_TP					RSVD	RSVD	RSVD		RSVD_TP	RSVD		RSVD	VCCOPC
BH	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VIDSCK	VIDALERT#	RSVD	VIDSOUT									
BG			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									
BF	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	VCCGT	VCCGT									
BE	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT											
BD			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									
BC	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	VCCGT	VCCGT									
BB	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT											
BA			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									
AY	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	VCCGT	VCCGT									
AW	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT											
AV			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									
AU	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	VCCGT	VCCGT									
AT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT											
AR			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									
AP	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	VCCGT	VCCGT									
AN	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT											
AM			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									
AL	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	VCCGT	VCCGT									
AK	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT											
AJ			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT									

Figure 9-2. Ball Map (Top View, Upper-Right Quadrant)



	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BT	CFG[15]		RSVD	RSVD	VCCEOPIO		DDR_VTT_CNTL		DDR1_DQ[0] / DDR0_DQ[16]			DDR1_DQ[2] / DDR0_DQ[18]		DDR0_DQ[1]				RSVD_TP	
BR	CFG[13]		RSVD	RSVD	VCCEOPIO		DDR1_VREF_DQ		DDR1_DQ[1] / DDR0_DQ[17]		DDR1_DQSP[0] / DDR0_DQSP[2]	DDR1_DQ[3] / DDR0_DQ[19]		DDR0_DQ[0]	DDR0_DQSN[0]		DDR0_DQ[3]	NCTF	RSVD_TP
BP	CFG[14]		RSVD	RSVD	VCCEOPIO		DDR0_VREF_DQ		DDR1_DQ[4] / DDR0_DQ[20]		DDR1_DQSN[0] / DDR0_DQSN[2]	DDR1_DQ[6] / DDR0_DQ[22]		DDR0_DQ[5]	DDR0_DQSP[0]		DDR0_DQ[2]	DDR0_DQ[6]	NCTF
BN			VCCOPC	RSVD	VCCEOPIO_SENSE		DDR_VREF_CA		DDR1_DQ[5] / DDR0_DQ[21]			DDR1_DQ[7] / DDR0_DQ[23]			DDR0_DQ[4]		DDR0_DQ[7]		PROC_SELECT#
BM	CFG[12]		VCCOPC	VSSOPC_SENSE	VSSEOPIO_SENSE	VCC_OPC_1P8													DDR0_DQ[11]
BL	VCCOPC	VCCOPC	VCCOPC	VCCOPC	VCCOPC_SENSE	VCC_OPC_1P8		DDR1_DQ[8] / DDR0_DQ[24]	DDR1_DQ[9] / DDR0_DQ[25]		DDR1_DQSN[1] / DDR0_DQSN[3]	DDR1_DQ[10] / DDR0_DQ[26]	DDR1_DQ[14] / DDR0_DQ[30]		DDR0_DQ[9]	DDR0_DQ[8]	DDR0_DQSN[1]	DDR0_DQ[10]	
BK	VCCOPC	VSS	VCCOPC	RSVD_TP											DDR0_DQ[13]	DDR0_DQ[12]	DDR0_DQSP[1]	DDR0_DQ[15]	DDR0_DQ[14]
BJ	VCCOPC	VSS	VCCOPC	RSVD_TP		RSVD_TP	RSVD_TP		DDR1_DQ[12] / DDR0_DQ[28]	DDR1_DQ[13] / DDR0_DQ[29]	DDR1_DQSP[1] / DDR0_DQSP[3]	DDR1_DQ[11] / DDR0_DQ[27]	DDR1_DQ[15] / DDR0_DQ[31]						
BH							VCCPLL_OC												
BG									DDR1_DQ[16] / DDR0_DQ[48]	DDR1_DQ[17] / DDR0_DQ[49]	DDR1_DQSN[2] / DDR0_DQSN[6]	DDR1_DQ[18] / DDR0_DQ[50]	DDR1_DQ[22] / DDR0_DQ[54]		DDR0_DQ[17] / DDR0_DQ[33]	DDR0_DQ[16] / DDR0_DQ[32]	DDR0_DQSN[2] / DDR0_DQSN[4]	DDR0_DQ[20] / DDR0_DQ[36]	DDR0_DQ[21] / DDR0_DQ[37]
BF						VCCGT	VCCGT		DDR1_DQ[20] / DDR0_DQ[52]	DDR1_DQ[21] / DDR0_DQ[53]	DDR1_DQSP[2] / DDR0_DQSP[6]	DDR1_DQ[19] / DDR0_DQ[51]	DDR1_DQ[23] / DDR0_DQ[55]		DDR0_DQ[19] / DDR0_DQ[35]	DDR0_DQ[18] / DDR0_DQ[34]	DDR0_DQSP[2] / DDR0_DQSP[4]	DDR0_DQ[23] / DDR0_DQ[39]	DDR0_DQ[22] / DDR0_DQ[38]
BE																			
BD						VCCGT	VCCGT								DDR0_DQ[28] / DDR0_DQ[44]	DDR0_DQ[29] / DDR0_DQ[45]	DDR0_DQSN[3] / DDR0_DQSN[5]	DDR0_DQ[24] / DDR0_DQ[40]	DDR0_DQ[25] / DDR0_DQ[41]
BC									DDR1_DQ[25] / DDR0_DQ[57]	DDR1_DQ[28] / DDR0_DQ[60]	DDR1_DQSN[3] / DDR0_DQSN[7]	DDR1_DQ[27] / DDR0_DQ[59]	DDR1_DQ[30] / DDR0_DQ[62]		DDR0_DQ[27] / DDR0_DQ[43]	DDR0_DQ[26] / DDR0_DQ[42]	DDR0_DQSP[3] / DDR0_DQSP[5]	DDR0_DQ[31] / DDR0_DQ[47]	DDR0_DQ[30] / DDR0_DQ[46]
BB						VCCGT	VCCGT		DDR1_DQ[24] / DDR0_DQ[56]	DDR1_DQ[29] / DDR0_DQ[61]	DDR1_DQSP[3] / DDR0_DQSP[7]	DDR1_DQ[26] / DDR0_DQ[58]	DDR1_DQ[31] / DDR0_DQ[63]						
BA						VCCGT	VCCGT								DDR0_ECC[4]	DDR0_ECC[5]	DDR0_DQSN[8]	DDR0_ECC[0]	DDR0_ECC[1]
AY							RSVD		DDR1_ECC[1]	DDR1_ECC[4]	DDR1_DQSN[8]	DDR1_ECC[2]	DDR1_ECC[6]	VDDQ	DDR0_ECC[3]	DDR0_ECC[2]	DDR0_DQSP[8]	DDR0_ECC[7]	DDR0_ECC[6]
AW						VCCGT	MSM#		DDR1_ECC[0]	DDR1_ECC[5]	DDR1_DQSP[8]	DDR1_ECC[3]	DDR1_ECC[7]	VDDQ					
AV																			
AU						VCCGT	RSVD								DDR0_ALERT#	DDR0_MA[12] / DDR0_CAA[6] / DDR0_MA[12]	DDR0_MA[15] / DDR0_CAA[8] / DDR0_ACT#	DDR0_MA[14] / DDR0_CAA[9] / DDR0_BG[1]	DDR0_BA[2] / DDR0_CAA[5] / DDR0_BG[0]
AT						VCCGT	ZVM#	VDDQ	DDR1_CKE[3]	DDR1_CKE[1]	DDR1_MA[15] / DDR1_CAA[8] / DDR1_ACT#	DDR1_CKE[0]	DDR1_CKE[2]		DDR0_CKE[3]	DDR0_MA[9] / DDR0_CAA[1] / DDR0_MA[9]	DDR0_CKE[2]	DDR0_CKE[1]	DDR0_CKE[0]
AR								VDDQ	DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]	DDR1_MA[12] / DDR1_CAA[6] / DDR1_MA[12]	DDR1_BA[2] / DDR1_CAA[5] / DDR1_BG[0]	DDR1_ALERT#	DDR1_MA[14] / DDR1_CAA[9] / DDR1_BG[1]	VDDQ					
AP						VCCGT	VCCGT						VDDQ	VDDQ	DDR0_MA[3]	DDR0_MA[11] / DDR0_CAB[8] / DDR0_MA[11]	DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]	DDR0_MA[4]	DDR0_MA[5] / DDR0_CAA[0] / DDR0_MA[5]
AN						VCCGT	VCCGT		DDR1_MA[11] / DDR1_CAA[7] / DDR1_MA[11]	DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]	DDR1_CKN[0]	DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]	DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]		DDR0_MA[2] / DDR0_CAB[5] / DDR0_MA[2]	DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]	DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]	DDR0_MA[7] / DDR0_CAA[4] / DDR0_MA[7]
AM						VCCGT	VCCGT		DDR1_CLKP[2]	DDR1_CLKN[2]	DDR1_CKP[0]	DDR1_CKN[1]	DDR1_CKP[1]	DDR1_MA[5] / DDR1_CAA[0] / DDR1_MA[5]					
AL							VCCGT		VDDQ					DDR1_MA[4]	DDR1_MA[3]		DDR0_CLKP[2]	DDR0_CLKP[3]	DDR0_CLKN[3]
AK														DDR1_MA[1] / DDR1_CAB[8] / DDR1_MA[1]	DDR1_MA[2] / DDR1_CAB[5] / DDR1_MA[2]		DDR0_CLKN[2]	DDR0_CKP[1]	DDR0_CKN[1]
AJ						VccGTx	VccGTx	VDDQ	DDR1_CLKN[3]	DDR1_CLKP[3]	DDR1_MA[0] / DDR1_CAB[9] / DDR1_MA[0]	RSVD	DDR1_PAR						

Figure 9-3. Ball Map (Top View, Lower-Left Quadrant)

	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
AH	VCCGT_SENSE	VSSGT_SENSE	VCCGTx-_SENSE	VSSGTx-_SENSE			VccGTx	VccGTx	VccGTx	VccGTx									
AG	VSS_SENSE	VCC_SENSE	VccGTx	VccGTx	VccGTx	VccGTx	VccGTx	VccGTx											
AF	VCC	VCC	VCC	VCC	VccGTx	VccGTx	VccGTx	VccGTx	VccGTx	VccGTx									
AE	VCC	VCC	VCC	VCC			VCC	VCC	VCC	RSVD									
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC											
AC			VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC									
AB	VCC	VCC	VCC	VCC			VCC	VCC	VCC	VCC									
AA	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC											
Y			VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC									
W	VCC	VCC	VCC	VCC			VCC	VCC	VCC	VCC									
V	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC											
U			VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC									
T	VCC	VCC	VCC	VCC			VCC	VCC	VCC	VCC									
R	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC											
P			VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC									
N	VCC	VCC	VCC	VCC			VCC	VCC	VCC	RSVD									
M	VCCSA_SENSE	VSSSA_SENSE	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA									
L	VCCSA	VCCSA	VCCSA	VCCSA			VCCSA	VCCSA											
K		DDI1_TXN[0]	DDI1_TXP[0]	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA	VCCSA									
J	DDI1_TXN[3]	DDI1_TXP[3]		DDI1_TXP[1]	DDI1_TXN[1]			THERMTRIP#	VCCSA		VccPLL	VCCIO	VCCIO		RSVD	PROC_TRIGOUT		VCCIO	VCCIO
H		DDI1_TXP[2]	DDI1_TXN[2]		DDI2_TXP[0]	DDI2_TXN[0]			VCCST	VCCSTG	VccPLL	VCCIO	VCCIO		RSVD	PROC_TRIGIN		VCCIO	VCCIO
G	DDI2_TXN[1]								VCCSTG	PROC_AUDIO_SDO		PROC_AUDIO_CLK		PROC_AUDIO_SDI				VCCIO	
F		DDI2_TXP[1]		DDI2_TXN[2]	DDI2_TXP[2]	DDI3_TXP[2]			RSVD		EDP_TXP[1]		DDI2_AUXP		PEG_RXN[1]		PEG_RXN[3]		PEG_RXN[5]
E		DDI2_TXP[3]	DDI2_TXN[3]			DDI3_TXN[2]		CLK24P	RSVD	EDP_TXN[0]	EDP_TXN[1]	DDI1_AUXN	DDI2_AUXN	PEG_RXP[0]	PEG_RXP[1]	PEG_RXP[2]	PEG_RXP[3]	PEG_RXP[4]	PEG_RXP[5]
D		eDP_RCOMP		PCI_BCLKP	DDI3_TXN[0]			CLK24N		EDP_TXP[0]		DDI1_AUXP		PEG_RXN[0]		PEG_RXN[2]		PEG_RXN[4]	
C	NCTF		PCI_BCLKN		DDI3_TXP[0]	DDI3_TXP[3]			RSVD		EDP_TXP[3]		EDP_AUXP		PEG_TXN[1]		PEG_TXN[3]		PEG_TXN[5]
B	NCTF		DDI3_TXP[1]		DDI3_TXN[1]	DDI3_TXN[3]		BCLKP	RSVD	EDP_TXN[2]	EDP_TXN[3]	DDI3_AUXN	EDP_AUXN	PEG_TXP[0]	PEG_TXP[1]	PEG_TXP[2]	PEG_TXP[3]	PEG_TXP[4]	PEG_TXP[5]
A						EDP_DISP_UTIL	BCLKN			EDP_TXP[2]		DDI3_AUXP		PEG_TXN[0]		PEG_TXN[2]		PEG_TXN[4]	

Figure 9-4. Ball Map (Top View, Lower-Right Quadrant)

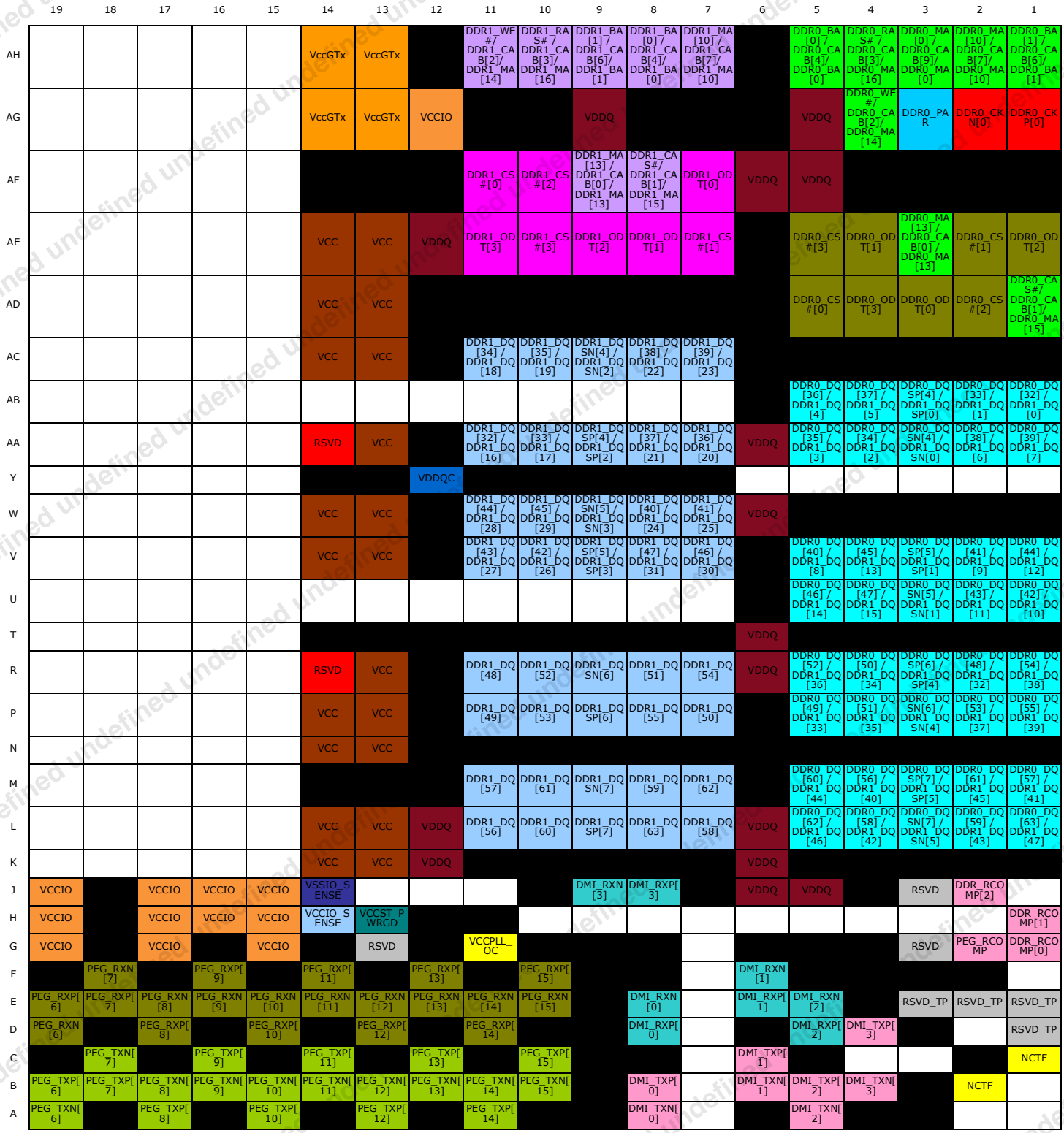


Table 9-1. Processor Ball List (Sheet 1 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AA3	DDR0_DQSN[4] / DDR1_DQSN[0]				DDR0_DQSN[4]	DDR1_DQSN[0]	12013.69	-6295.14
AB3	DDR0_DQSP[4] / DDR1_DQSP[0]				DDR0_DQSP[4]	DDR1_DQSP[0]	12013.69	-5558.54
AK1	DDR0_CKN[1]						13314.17	1248.66
AK2	DDR0_CKP[1]						12663.93	1248.66
AM7	DDR1_CKP[1]						9403.08	2463.55
AM8	DDR1_CKN[1]						8752.84	2463.55
L3	DDR0_DQSN[7] / DDR1_DQSN[5]				DDR0_DQSN[7]	DDR1_DQSN[5]	12013.69	-13838.9
M3	DDR0_DQSP[7] / DDR1_DQSP[5]				DDR0_DQSP[7]	DDR1_DQSP[5]	12013.69	-13102.3
P3	DDR0_DQSN[6] / DDR1_DQSN[4]				DDR0_DQSN[6]	DDR1_DQSN[4]	12013.69	-11324.3
R3	DDR0_DQSP[6] / DDR1_DQSP[4]				DDR0_DQSP[6]	DDR1_DQSP[4]	12013.69	-10587.7
U3	DDR0_DQSN[5] / DDR1_DQSN[1]				DDR0_DQSN[5]	DDR1_DQSN[1]	12013.69	-8809.74
V3	DDR0_DQSP[5] / DDR1_DQSP[1]				DDR0_DQSP[5]	DDR1_DQSP[1]	12013.69	-8073.14
A10	VSS						7421.37	-20314.2
A11	PEG_TXP[14]						6633.97	-20314.2
A12	VSS						5846.57	-20314.2
A13	PEG_TXP[12]						5059.17	-20314.2
A14	VSS						4271.77	-20314.2
A15	PEG_TXP[10]						3484.37	-20314.2
A16	VSS						2696.97	-20314.2
A17	PEG_TXP[8]						1909.57	-20314.2
A18	VSS						1122.17	-20314.2
A19	PEG_TXN[6]						334.77	-20314.2
A20	VSS						-452.63	-20314.2
A21	PEG_TXN[4]						-1240.03	-20314.2
A22	VSS						-2027.43	-20314.2
A23	PEG_TXN[2]						-2814.83	-20314.2
A24	VSS						-3602.23	-20314.2
A25	PEG_TXN[0]						-4389.63	-20314.2
A26	VSS						-5177.03	-20314.2
A27	DDI3_AUXP						-5964.43	-20314.2
A28	VSS						-6751.83	-20314.2
A29	EDP_TXP[2]						-7539.23	-20314.2
A3	NCTFVSS						12059.92	-20314.2
A30	VSS						-8529.83	-20314.2
A32	BCLKN						-9558.02	-20314.2

Table 9-1. Processor Ball List (Sheet 2 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
A33	EDP_DISP_UTIL						-10345.4	-20314.2
A34	NCTFVSS						-11145.5	-20314.2
A36	VSS						-11958.3	-20314.2
A37	VSS						-12739.4	-20314.2
A4	NCTFVSS						11343.13	-20314.2
A5	DMI_TXN[2]						10543.03	-20314.2
A6	VSS						9768.33	-20314.2
A8	DMI_TXN[0]						8996.17	-20314.2
A9	VSS						8208.77	-20314.2
AA1	DDR0_DQ[39] / DDR1_DQ[7]				DDR0_DQ[39]	DDR1_DQ[7]	13314.17	-6295.14
AA10	DDR1_DQ[33] / DDR1_DQ[17]				DDR1_DQ[33]	DDR1_DQ[17]	7452.36	-5766.05
AA11	DDR1_DQ[32] / DDR1_DQ[16]				DDR1_DQ[32]	DDR1_DQ[16]	6802.12	-5766.05
AA12	VSS						6151.88	-5766.05
AA13	VCC						5501.64	-5766.05
AA14	RSVD						4851.4	-5766.05
AA2	DDR0_DQ[38] / DDR1_DQ[6]				DDR0_DQ[38]	DDR1_DQ[6]	12663.93	-6295.14
AA29	VSS						-7411.21	-5898.9
AA30	VSS						-8061.45	-5898.9
AA31	VCC						-8762.49	-5898.9
AA32	VCC						-9412.73	-5898.9
AA33	VCC						-10063	-5898.9
AA34	VCC						-10713.2	-5898.9
AA35	VCC						-11363.5	-5898.9
AA36	VCC						-12013.7	-5898.9
AA37	VCC						-12663.9	-5898.9
AA38	VCC						-13314.2	-5898.9
AA4	DDR0_DQ[34] / DDR1_DQ[2]				DDR0_DQ[34]	DDR1_DQ[2]	11363.45	-6295.14
AA5	DDR0_DQ[35] / DDR1_DQ[3]				DDR0_DQ[35]	DDR1_DQ[3]	10713.21	-6295.14
AA6	VDDQ						10062.97	-6345.94
AA7	DDR1_DQ[36] / DDR1_DQ[20]				DDR1_DQ[36]	DDR1_DQ[20]	9403.08	-5766.05
AA8	DDR1_DQ[37] / DDR1_DQ[21]				DDR1_DQ[37]	DDR1_DQ[21]	8752.84	-5766.05
AA9	DDR1_DQSP[4] / DDR1_DQSP[2]				DDR1_DQSP[4]	DDR1_DQSP[2]	8102.6	-5766.05
AB1	DDR0_DQ[32] / DDR1_DQ[0]				DDR0_DQ[32]	DDR1_DQ[0]	13314.17	-5558.54
AB2	DDR0_DQ[33] / DDR1_DQ[1]				DDR0_DQ[33]	DDR1_DQ[1]	12663.93	-5558.54

Table 9-1. Processor Ball List (Sheet 3 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AB29	VCC						-7411.21	-5111.5
AB30	VCC						-8061.45	-5111.5
AB31	VCC						-8762.49	-5111.5
AB32	VCC						-9412.73	-5111.5
AB33	VSS						-10063	-5111.5
AB34	VSS						-10713.2	-5111.5
AB35	VCC						-11363.5	-5111.5
AB36	VCC						-12013.7	-5111.5
AB37	VCC						-12663.9	-5111.5
AB38	VCC						-13314.2	-5111.5
AB4	DDR0_DQ[37] / DDR1_DQ[5]				DDR0_DQ[37]	DDR1_DQ[5]	11363.45	-5558.54
AB5	DDR0_DQ[36] / DDR1_DQ[4]				DDR0_DQ[36]	DDR1_DQ[4]	10713.21	-5558.54
AB6	VSS						10062.97	-5507.74
AC1	VSS						13314.17	-4669.54
AC10	DDR1_DQ[35] / DDR1_DQ[19]				DDR1_DQ[35]	DDR1_DQ[19]	7452.36	-4851.65
AC11	DDR1_DQ[34] / DDR1_DQ[18]				DDR1_DQ[34]	DDR1_DQ[18]	6802.12	-4851.65
AC12	VSS						6151.88	-4851.65
AC13	VCC						5501.64	-4851.65
AC14	VCC						4851.4	-4851.65
AC2	VSS						12663.93	-4669.54
AC29	VCC						-7411.21	-4324.1
AC3	VSS						12013.69	-4669.54
AC30	VCC						-8061.45	-4324.1
AC31	VCC						-8762.49	-4324.1
AC32	VCC						-9412.73	-4324.1
AC33	VCC						-10063	-4324.1
AC34	VCC						-10713.2	-4324.1
AC35	VCC						-11363.5	-4324.1
AC36	VCC						-12013.7	-4324.1
AC37	VSS						-12663.9	-4324.1
AC38	VSS						-13314.2	-4324.1
AC4	VSS						11363.45	-4669.54
AC5	VSS						10713.21	-4669.54
AC6	VSS						10062.97	-4669.54
AC7	DDR1_DQ[39] / DDR1_DQ[23]				DDR1_DQ[39]	DDR1_DQ[23]	9403.08	-4851.65
AC8	DDR1_DQ[38] / DDR1_DQ[22]				DDR1_DQ[38]	DDR1_DQ[22]	8752.84	-4851.65

Table 9-1. Processor Ball List (Sheet 4 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AC9	DDR1_DQSN[4] / DDR1_DQSN[2]				DDR1_DQSN[4]	DDR1_DQSN[2]	8102.6	-4851.65
AD1	DDR0_CAS#/ DDR0_CAB[1]/ DDR0_MA[15]	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]			13314.17	-3780.54
AD10	VSS						7452.36	-3937.25
AD11	VSS						6802.12	-3937.25
AD12	VSS						6151.88	-3937.25
AD13	VCC						5501.64	-3937.25
AD14	VCC						4851.4	-3937.25
AD2	DDR0_CS#[2]						12663.93	-3780.54
AD29	VSS						-7411.21	-3536.7
AD3	DDR0_ODT[0]						12013.69	-3780.54
AD30	VSS						-8061.45	-3536.7
AD31	VCC						-8762.49	-3536.7
AD32	VCC						-9412.73	-3536.7
AD33	VCC						-10063	-3536.7
AD34	VCC						-10713.2	-3536.7
AD35	VCC						-11363.5	-3536.7
AD36	VCC						-12013.7	-3536.7
AD37	VCC						-12663.9	-3536.7
AD38	VCC						-13314.2	-3536.7
AD4	DDR0_ODT[3]						11363.45	-3780.54
AD5	DDR0_CS#[0]						10713.21	-3780.54
AD6	VSS						10062.97	-3831.34
AD7	VSS						9403.08	-3937.25
AD8	VSS						8752.84	-3937.25
AD9	VSS						8102.6	-3937.25
AE1	DDR0_ODT[2]						13314.17	-3043.94
AE10	DDR1_CS#[3]						7452.36	-3022.85
AE11	DDR1_ODT[3]						6802.12	-3022.85
AE12	VDDQ						6151.88	-3022.85
AE13	VCC						5501.64	-3022.85
AE14	VCC						4851.4	-3022.85
AE2	DDR0_CS#[1]						12663.93	-3043.94
AE29	RSVD						-7411.21	-2749.3
AE3	DDR0_MA[13] / DDR0_CAB[0] / DDR0_MA[13]	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]			12013.69	-3043.94
AE30	VCC						-8061.45	-2749.3
AE31	VCC						-8762.49	-2749.3

Table 9-1. Processor Ball List (Sheet 5 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AE32	VCC						-9412.73	-2749.3
AE33	VSS						-10063	-2749.3
AE34	VSS						-10713.2	-2749.3
AE35	VCC						-11363.5	-2749.3
AE36	VCC						-12013.7	-2749.3
AE37	VCC						-12663.9	-2749.3
AE38	VCC						-13314.2	-2749.3
AE4	DDR0_ODT[1]						11363.45	-3043.94
AE5	DDR0_CS#[3]						10713.21	-3043.94
AE6	VSS						10062.97	-2993.14
AE7	DDR1_CS#[1]						9403.08	-3022.85
AE8	DDR1_ODT[1]						8752.84	-3022.85
AE9	DDR1_ODT[2]						8102.6	-3022.85
AF1	VSS						13314.17	-2154.94
AF10	DDR1_CS#[2]						7452.36	-2108.45
AF11	DDR1_CS#[0]						6802.12	-2108.45
AF12	VSS						6151.88	-2108.45
AF13	VSS						5501.64	-2108.45
AF14	VSS						4851.4	-2108.45
AF2	VSS						12663.93	-2154.94
AF29	VccGTx						-7411.21	-1961.9
AF3	VSS						12013.69	-2154.94
AF30	VccGTx						-8061.45	-1961.9
AF31	VccGTx						-8762.49	-1961.9
AF32	VccGTx						-9412.73	-1961.9
AF33	VccGTx						-10063	-1961.9
AF34	VccGTx						-10713.2	-1961.9
AF35	VCC						-11363.5	-1961.9
AF36	VCC						-12013.7	-1961.9
AF37	VCC						-12663.9	-1961.9
AF38	VCC						-13314.2	-1961.9
AF4	VSS						11363.45	-2154.94
AF5	VDDQ						10713.21	-2154.94
AF6	VDDQ						10062.97	-2154.94
AF7	DDR1_ODT[0]						9403.08	-2108.45
AF8	DDR1_CAS#/ DDR1_CAB[1]/ DDR1_MA[15]	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]			8752.84	-2108.45

Table 9-1. Processor Ball List (Sheet 6 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AF9	DDR1_MA[13] / DDR1_CAB[0] / DDR1_MA[13]	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]			8102.6	-2108.45
AG1	DDR0_CKP[0]						13314.17	-1265.94
AG10	VSS						7452.36	-1194.05
AG11	VSS						6802.12	-1194.05
AG12	VCCIO						6151.88	-1194.05
AG13	VccGTx						5501.64	-1194.05
AG14	VccGTx						4851.4	-1194.05
AG2	DDR0_CKN[0]						12663.93	-1265.94
AG29	VSS						-7411.21	-1174.5
AG3	DDR0_PAR						12013.69	-1265.94
AG30	VSS						-8061.45	-1174.5
AG31	VccGTx						-8762.49	-1174.5
AG32	VccGTx						-9412.73	-1174.5
AG33	VccGTx						-10063	-1174.5
AG34	VccGTx						-10713.2	-1174.5
AG35	VccGTx						-11363.5	-1174.5
AG36	VccGTx						-12013.7	-1174.5
AG37	VCC_SENSE						-12663.9	-1174.5
AG38	VSS_SENSE						-13314.2	-1174.5
AG4	DDR0_WE#/ DDR0_CAB[2]/ DDR0_MA[14]	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]			11363.45	-1265.94
AG5	VDDQ						10713.21	-1265.94
AG6	VSS						10062.97	-1316.74
AG7	VSS						9403.08	-1194.05
AG8	VSS						8752.84	-1194.05
AG9	VDDQ						8102.6	-1194.05
AH1	DDR0_BA[1] / DDR0_CAB[6]/ DDR0_BA[1]	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]			13314.17	-529.34
AH10	DDR1_RAS# / DDR1_CAB[3]/ DDR1_MA[16]	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]			7452.36	-279.65
AH11	DDR1_WE#/ DDR1_CAB[2]/ DDR1_MA[14]	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]			6802.12	-279.65
AH12	VSS						6151.88	-279.65
AH13	VccGTx						5501.64	-279.65
AH14	VccGTx						4851.4	-279.65
AH2	DDR0_MA[10] / DDR0_CAB[7]/ DDR0_MA[10]	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]			12663.93	-529.34

Table 9-1. Processor Ball List (Sheet 7 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AH29	VccGTx						-7411.21	-387.1
AH3	DDR0_MA[0] / DDR0_CAB[9]/ DDR0_MA[0]	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]			12013.69	-529.34
AH30	VccGTx						-8061.45	-387.1
AH31	VccGTx						-8762.49	-387.1
AH32	VccGTx						-9412.73	-387.1
AH33	VSS						-10063	-387.1
AH34	VSS						-10713.2	-387.1
AH35	VSSGTx_SENSE						-11363.5	-387.1
AH36	VCCGTx_SENSE						-12013.7	-387.1
AH37	VSSGT_SENSE						-12663.9	-387.1
AH38	VCCGT_SENSE						-13314.2	-387.1
AH4	DDR0_RAS# / DDR0_CAB[3]/ DDR0_MA[16]	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]			11363.45	-529.34
AH5	DDR0_BA[0] / DDR0_CAB[4]/ DDR0_BA[0]	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]			10713.21	-529.34
AH6	VSS						10062.97	-478.54
AH7	DDR1_MA[10] / DDR1_CAB[7]/ DDR1_MA[10]	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]			9403.08	-279.65
AH8	DDR1_BA[0] / DDR1_CAB[4]/ DDR1_BA[0]	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]			8752.84	-279.65
AH9	DDR1_BA[1] / DDR1_CAB[6]/ DDR1_BA[1]	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]			8102.6	-279.65
AJ1	VSS						13314.17	359.66
AJ10	DDR1_CLKP[3]						7452.36	634.75
AJ11	DDR1_CLKN[3]						6802.12	634.75
AJ12	VDDQ						6151.88	634.75
AJ13	VccGTx						5501.64	634.75
AJ14	VccGTx						4851.4	634.75
AJ2	VSS						12663.93	359.66
AJ29	VCCGT						-7411.21	400.3
AJ3	VSS						12013.69	359.66
AJ30	VCCGT						-8061.45	400.3
AJ31	VCCGT						-8762.49	400.3
AJ32	VCCGT						-9412.73	400.3
AJ33	VCCGT						-10063	400.3
AJ34	VCCGT						-10713.2	400.3
AJ35	VCCGT						-11363.5	400.3

Table 9-1. Processor Ball List (Sheet 8 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AJ36	VCCGT						-12013.7	400.3
AJ37	VSS						-12663.9	400.3
AJ38	VSS						-13314.2	400.3
AJ4	VSS						11363.45	359.66
AJ5	VSS						10713.21	359.66
AJ6	VSS						10062.97	359.66
AJ7	DDR1_PAR						9403.08	634.75
AJ8	RSVD						8752.84	634.75
AJ9	DDR1_MA[0] / DDR1_CAB[9]/ DDR1_MA[0]	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]			8102.6	634.75
AK29	VSS						-7411.21	1187.7
AK3	DDR0_CLKN[2]						12013.69	1248.66
AK30	VSS						-8061.45	1187.7
AK31	VCCGT						-8762.49	1187.7
AK32	VCCGT						-9412.73	1187.7
AK33	VCCGT						-10063	1187.7
AK34	VCCGT						-10713.2	1187.7
AK35	VCCGT						-11363.5	1187.7
AK36	VCCGT						-12013.7	1187.7
AK37	VCCGT						-12663.9	1187.7
AK38	VCCGT						-13314.2	1187.7
AK4	VSS						11363.45	1248.66
AK5	DDR1_MA[2] / DDR1_CAB[5]/ DDR1_MA[2]	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]			10713.21	1248.66
AK6	DDR1_MA[1] / DDR1_CAB[8]/ DDR1_MA[1]	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]			10062.97	1197.86
AL1	DDR0_CLKN[3]						13314.17	1985.26
AL10	VSS						7452.36	1549.15
AL11	VDDQ						6802.12	1549.15
AL12	VSS						6151.88	1549.15
AL13	VCCGT						5501.64	1549.15
AL14	VSS						4851.4	1549.15
AL2	DDR0_CLKP[3]						12663.93	1985.26
AL29	VCCGT						-7411.21	1975.1
AL3	DDR0_CLKP[2]						12013.69	1985.26
AL30	VCCGT						-8061.45	1975.1
AL31	VCCGT						-8762.49	1975.1
AL32	VCCGT						-9412.73	1975.1

Table 9-1. Processor Ball List (Sheet 9 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AL33	VSS						-10063	1975.1
AL34	VSS						-10713.2	1975.1
AL35	VCCGT						-11363.5	1975.1
AL36	VCCGT						-12013.7	1975.1
AL37	VCCGT						-12663.9	1975.1
AL38	VCCGT						-13314.2	1975.1
AL4	VSS						11363.45	1985.26
AL5	DDR1_MA[3]						10713.21	1985.26
AL6	DDR1_MA[4]						10062.97	2036.06
AL7	VSS						9403.08	1549.15
AL8	VSS						8752.84	1549.15
AL9	VSS						8102.6	1549.15
AM1	VSS						13314.17	2874.26
AM10	DDR1_CLKN[2]						7452.36	2463.55
AM11	DDR1_CLKP[2]						6802.12	2463.55
AM12	VSS						6151.88	2463.55
AM13	VCCGT						5501.64	2463.55
AM14	VCCGT						4851.4	2463.55
AM2	VSS						12663.93	2874.26
AM29	VCCGT						-7411.21	2762.5
AM3	VSS						12013.69	2874.26
AM30	VCCGT						-8061.45	2762.5
AM31	VCCGT						-8762.49	2762.5
AM32	VCCGT						-9412.73	2762.5
AM33	VCCGT						-10063	2762.5
AM34	VCCGT						-10713.2	2762.5
AM35	VCCGT						-11363.5	2762.5
AM36	VCCGT						-12013.7	2762.5
AM37	VSS						-12663.9	2762.5
AM38	VSS						-13314.2	2762.5
AM4	VSS						11363.45	2874.26
AM5	VSS						10713.21	2874.26
AM6	DDR1_MA[5] / DDR1_CAA[0] / DDR1_MA[5]	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]			10062.97	2874.26
AM9	DDR1_CKP[0]						8102.6	2463.55
AN1	DDR0_MA[7] / DDR0_CAA[4] / DDR0_MA[7]	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]			13314.17	3763.26

Table 9-1. Processor Ball List (Sheet 10 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AN10	DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]			7452.36	3377.95
AN11	DDR1_MA[11] / DDR1_CAA[7] / DDR1_MA[11]	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]			6802.12	3377.95
AN12	VSS						6151.88	3377.95
AN13	VCCGT						5501.64	3377.95
AN14	VCCGT						4851.4	3377.95
AN2	DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]			12663.93	3763.26
AN29	VSS						-7411.21	3549.9
AN3	DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]			12013.69	3763.26
AN30	VSS						-8061.45	3549.9
AN31	VCCGT						-8762.49	3549.9
AN32	VCCGT						-9412.73	3549.9
AN33	VCCGT						-10063	3549.9
AN34	VCCGT						-10713.2	3549.9
AN35	VCCGT						-11363.5	3549.9
AN36	VCCGT						-12013.7	3549.9
AN37	VCCGT						-12663.9	3549.9
AN38	VCCGT						-13314.2	3549.9
AN4	DDR0_MA[2] / DDR0_CAB[5]/ DDR0_MA[2]	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]			11363.45	3763.26
AN5	VSS						10713.21	3763.26
AN6	VSS						10062.97	3712.46
AN7	DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]			9403.08	3377.95
AN8	DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]			8752.84	3377.95
AN9	DDR1_CKN[0]						8102.6	3377.95
AP1	DDR0_MA[5] / DDR0_CAA[0] / DDR0_MA[5]	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]			13314.17	4499.86
AP10	VSS						7452.36	4292.35
AP11	VSS						6802.12	4292.35
AP12	VSS						6151.88	4292.35
AP13	VCCGT						5501.64	4292.35
AP14	VCCGT						4851.4	4292.35
AP2	DDR0_MA[4]						12663.93	4499.86
AP29	VCCGT						-7411.21	4337.3

Table 9-1. Processor Ball List (Sheet 11 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AP3	DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]			12013.69	4499.86
AP30	VCCGT						-8061.45	4337.3
AP31	VCCGT						-8762.49	4337.3
AP32	VCCGT						-9412.73	4337.3
AP33	VSS						-10063	4337.3
AP34	VSS						-10713.2	4337.3
AP35	VCCGT						-11363.5	4337.3
AP36	VCCGT						-12013.7	4337.3
AP37	VCCGT						-12663.9	4337.3
AP38	VCCGT						-13314.2	4337.3
AP4	DDR0_MA[1] / DDR0_CAB[8]/ DDR0_MA[1]	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]			11363.45	4499.86
AP5	DDR0_MA[3]						10713.21	4499.86
AP6	VDDQ						10062.97	4550.66
AP7	VDDQ						9403.08	4292.35
AP8	VSS						8752.84	4292.35
AP9	VSS						8102.6	4292.35
AR1	VSS						13314.17	5388.86
AR10	DDR1_MA[12] / DDR1_CAA[6] / DDR1_MA[12]	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]			7452.36	5206.75
AR11	DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]			6802.12	5206.75
AR12	VDDQ						6151.88	5206.75
AR13	VSS						5501.64	5206.75
AR14	VSS						4851.4	5206.75
AR2	VSS						12663.93	5388.86
AR29	VCCGT						-7411.21	5124.7
AR3	VSS						12013.69	5388.86
AR30	VCCGT						-8061.45	5124.7
AR31	VCCGT						-8762.49	5124.7
AR32	VCCGT						-9412.73	5124.7
AR33	VCCGT						-10063	5124.7
AR34	VCCGT						-10713.2	5124.7
AR35	VCCGT						-11363.5	5124.7
AR36	VCCGT						-12013.7	5124.7
AR37	VSS						-12663.9	5124.7
AR38	VSS						-13314.2	5124.7

Table 9-1. Processor Ball List (Sheet 12 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AR4	VSS						11363.45	5388.86
AR5	VSS						10713.21	5388.86
AR6	VDDQ						10062.97	5388.86
AR7	DDR1_MA[14] / DDR1_CAA[9]/ DDR1_BG[1]	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]			9403.08	5206.75
AR8	DDR1_ALERT#						8752.84	5206.75
AR9	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]			8102.6	5206.75
AT1	DDR0_CKE[0]						13314.17	6277.86
AT10	DDR1_CKE[1]						7452.36	6121.15
AT11	DDR1_CKE[3]						6802.12	6121.15
AT12	VDDQ						6151.88	6121.15
AT13	ZVM#						5501.64	6121.15
AT14	VCCGT						4851.4	6121.15
AT2	DDR0_CKE[1]						12663.93	6277.86
AT29	VSS						-7411.21	5912.1
AT3	DDR0_CKE[2]						12013.69	6277.86
AT30	VSS						-8061.45	5912.1
AT31	VCCGT						-8762.49	5912.1
AT32	VCCGT						-9412.73	5912.1
AT33	VCCGT						-10063	5912.1
AT34	VCCGT						-10713.2	5912.1
AT35	VCCGT						-11363.5	5912.1
AT36	VCCGT						-12013.7	5912.1
AT37	VCCGT						-12663.9	5912.1
AT38	VCCGT						-13314.2	5912.1
AT4	DDR0_MA[9] / DDR0_CAA[1] / DDR0_MA[9]	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]			11363.45	6277.86
AT5	DDR0_CKE[3]						10713.21	6277.86
AT6	VSS						10062.97	6227.06
AT7	DDR1_CKE[2]						9403.08	6121.15
AT8	DDR1_CKE[0]						8752.84	6121.15
AT9	DDR1_MA[15] / DDR1_CAA[8]/ DDR1_ACT#	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#			8102.6	6121.15
AU1	DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]			13314.17	7014.46
AU10	VSS						7452.36	7035.55
AU11	VSS						6802.12	7035.55

Table 9-1. Processor Ball List (Sheet 13 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AU12	VSS						6151.88	7035.55
AU13	RSVD						5501.64	7035.55
AU14	VCCGT						4851.4	7035.55
AU2	DDR0_MA[14] / DDR0_CAA[9]/ DDR0_BG[1]	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]			12663.93	7014.46
AU29	VCCGT						-7411.21	6699.5
AU3	DDR0_MA[15] / DDR0_CAA[8]/ DDR0_ACT#	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#			12013.69	7014.46
AU30	VCCGT						-8061.45	6699.5
AU31	VCCGT						-8762.49	6699.5
AU32	VCCGT						-9412.73	6699.5
AU33	VSS						-10063	6699.5
AU34	VSS						-10713.2	6699.5
AU35	VCCGT						-11363.5	6699.5
AU36	VCCGT						-12013.7	6699.5
AU37	VCCGT						-12663.9	6699.5
AU38	VCCGT						-13314.2	6699.5
AU4	DDR0_MA[12] / DDR0_CAA[6] / DDR0_MA[12]	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]			11363.45	7014.46
AU5	DDR0_ALERT#						10713.21	7014.46
AU6	VSS						10062.97	7065.26
AU7	VSS						9403.08	7035.55
AU8	VSS						8752.84	7035.55
AU9	VSS						8102.6	7035.55
AV29	VCCGT						-7411.21	7486.9
AV30	VCCGT						-8061.45	7486.9
AV31	VCCGT						-8762.49	7486.9
AV32	VCCGT						-9412.73	7486.9
AV33	VCCGT						-10063	7486.9
AV34	VCCGT						-10713.2	7486.9
AV35	VCCGT						-11363.5	7486.9
AV36	VCCGT						-12013.7	7486.9
AV37	VSS						-12663.9	7486.9
AV38	VSS						-13314.2	7486.9
AW1	VSS						13314.17	7903.46
AW10	DDR1_ECC[5]						7452.36	7949.95
AW11	DDR1_ECC[0]						6802.12	7949.95
AW12	VSS						6151.88	7949.95

Table 9-1. Processor Ball List (Sheet 14 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AW13	MSM#						5501.64	7949.95
AW14	VCCGT						4851.4	7949.95
AW2	VSS						12663.93	7903.46
AW29	VSS						-7411.21	8274.3
AW3	VSS						12013.69	7903.46
AW30	VSS						-8061.45	8274.3
AW31	VCCGT						-8762.49	8274.3
AW32	VCCGT						-9412.73	8274.3
AW33	VCCGT						-10063	8274.3
AW34	VCCGT						-10713.2	8274.3
AW35	VCCGT						-11363.5	8274.3
AW36	VCCGT						-12013.7	8274.3
AW37	VCCGT						-12663.9	8274.3
AW38	VCCGT						-13314.2	8274.3
AW4	VSS						11363.45	7903.46
AW5	VSS						10713.21	7903.46
AW6	VDDQ						10062.97	7903.46
AW7	DDR1_ECC[7]						9403.08	7949.95
AW8	DDR1_ECC[3]						8752.84	7949.95
AW9	DDR1_DQSP[8]						8102.6	7949.95
AY1	DDR0_ECC[6]						13314.17	8792.46
AY10	DDR1_ECC[4]						7452.36	8864.35
AY11	DDR1_ECC[1]						6802.12	8864.35
AY12	VSS						6151.88	8864.35
AY13	RSVD						5501.64	8864.35
AY14	VSS						4851.4	8864.35
AY2	DDR0_ECC[7]						12663.93	8792.46
AY29	VCCGT						-7411.21	9061.7
AY3	DDR0_DQSP[8]						12013.69	8792.46
AY30	VCCGT						-8061.45	9061.7
AY31	VCCGT						-8762.49	9061.7
AY32	VCCGT						-9412.73	9061.7
AY33	VSS						-10063	9061.7
AY34	VSS						-10713.2	9061.7
AY35	VCCGT						-11363.5	9061.7
AY36	VCCGT						-12013.7	9061.7
AY37	VCCGT						-12663.9	9061.7
AY38	VCCGT						-13314.2	9061.7

Table 9-1. Processor Ball List (Sheet 15 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
AY4	DDR0_ECC[2]						11363.45	8792.46
AY5	DDR0_ECC[3]						10713.21	8792.46
AY6	VDDQ						10062.97	8741.66
AY7	DDR1_ECC[6]						9403.08	8864.35
AY8	DDR1_ECC[2]						8752.84	8864.35
AY9	DDR1_DQSN[8]						8102.6	8864.35
B10	PEG_TXN[15]						7421.37	-19663.9
B11	PEG_TXN[14]						6633.97	-19663.9
B12	PEG_TXN[13]						5846.57	-19663.9
B13	PEG_TXN[12]						5059.17	-19663.9
B14	PEG_TXN[11]						4271.77	-19663.9
B15	PEG_TXN[10]						3484.37	-19663.9
B16	PEG_TXN[9]						2696.97	-19663.9
B17	PEG_TXN[8]						1909.57	-19663.9
B18	PEG_TXP[7]						1122.17	-19663.9
B19	PEG_TXP[6]						334.77	-19663.9
B2	NCTF						12653.77	-19653.8
B20	PEG_TXP[5]						-452.63	-19663.9
B21	PEG_TXP[4]						-1240.03	-19663.9
B22	PEG_TXP[3]						-2027.43	-19663.9
B23	PEG_TXP[2]						-2814.83	-19663.9
B24	PEG_TXP[1]						-3602.23	-19663.9
B25	PEG_TXP[0]						-4389.63	-19663.9
B26	EDP_AUXN						-5177.03	-19663.9
B27	DDI3_AUXN						-5964.43	-19663.9
B28	EDP_TXN[3]						-6751.83	-19663.9
B29	EDP_TXN[2]						-7539.23	-19663.9
B3	NCTFVSS						11932.73	-19615.7
B30	RSVD						-8326.63	-19663.9
B31	BCLKP						-9114.03	-19663.9
B33	DDI3_TXN[3]						-9901.43	-19663.9
B34	DDI3_TXN[1]						-11128.8	-19644.6
B36	DDI3_TXP[1]						-11884.1	-19613.1
B37	NCTFVSS						-12594.5	-19611.6
B38	NCTF						-13314.2	-19761.2
B4	DMI_TXN[3]						11283.51	-19343.6
B5	DMI_TXP[2]						10570.97	-19663.9
B6	DMI_TXN[1]						9783.57	-19663.9

Table 9-1. Processor Ball List (Sheet 16 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
B8	DMI_TXP[0]						8996.17	-19663.9
B9	VSS						8208.77	-19663.9
BA1	DDR0_ECC[1]						13314.17	9529.06
BA10	VSS						7452.36	9778.75
BA11	VSS						6802.12	9778.75
BA12	VSS						6151.88	9778.75
BA13	VCCGT						5501.64	9778.75
BA14	VCCGT						4851.4	9778.75
BA2	DDR0_ECC[0]						12663.93	9529.06
BA29	VCCGT						-7411.21	9849.1
BA3	DDR0_DQSN[8]						12013.69	9529.06
BA30	VCCGT						-8061.45	9849.1
BA31	VCCGT						-8762.49	9849.1
BA32	VCCGT						-9412.73	9849.1
BA33	VCCGT						-10063	9849.1
BA34	VCCGT						-10713.2	9849.1
BA35	VCCGT						-11363.5	9849.1
BA36	VCCGT						-12013.7	9849.1
BA37	VSS						-12663.9	9849.1
BA38	VSS						-13314.2	9849.1
BA4	DDR0_ECC[5]						11363.45	9529.06
BA5	DDR0_ECC[4]						10713.21	9529.06
BA6	VSS						10062.97	9579.86
BA7	VSS						9403.08	9778.75
BA8	VSS						8752.84	9778.75
BA9	VSS						8102.6	9778.75
BB1	VSS						13314.17	10418.06
BB10	DDR1_DQ[29] / DDR0_DQ[61]				DDR1_DQ[29]	DDR0_DQ[61]	7452.36	10693.15
BB11	DDR1_DQ[24] / DDR0_DQ[56]				DDR1_DQ[24]	DDR0_DQ[56]	6802.12	10693.15
BB12	VSS						6151.88	10693.15
BB13	VCCGT						5501.64	10693.15
BB14	VCCGT						4851.4	10693.15
BB2	VSS						12663.93	10418.06
BB29	VSS						-7411.21	10636.5
BB3	VSS						12013.69	10418.06
BB30	VSS						-8061.45	10636.5
BB31	VCCGT						-8762.49	10636.5

Table 9-1. Processor Ball List (Sheet 17 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BB32	VCCGT						-9412.73	10636.5
BB33	VCCGT						-10063	10636.5
BB34	VCCGT						-10713.2	10636.5
BB35	VCCGT						-11363.5	10636.5
BB36	VCCGT						-12013.7	10636.5
BB37	VCCGT						-12663.9	10636.5
BB38	VCCGT						-13314.2	10636.5
BB4	VSS						11363.45	10418.06
BB5	VSS						10713.21	10418.06
BB6	VSS						10062.97	10418.06
BB7	DDR1_DQ[31] / DDR0_DQ[63]				DDR1_DQ[31]	DDR0_DQ[63]	9403.08	10693.15
BB8	DDR1_DQ[26] / DDR0_DQ[58]				DDR1_DQ[26]	DDR0_DQ[58]	8752.84	10693.15
BB9	DDR1_DQSP[3] / DDR0_DQSP[7]				DDR1_DQSP[3]	DDR0_DQSP[7]	8102.6	10693.15
BC1	DDR0_DQ[30] / DDR0_DQ[46]				DDR0_DQ[30]	DDR0_DQ[46]	13314.17	11307.06
BC10	DDR1_DQ[28] / DDR0_DQ[60]				DDR1_DQ[28]	DDR0_DQ[60]	7452.36	11607.55
BC11	DDR1_DQ[25] / DDR0_DQ[57]				DDR1_DQ[25]	DDR0_DQ[57]	6802.12	11607.55
BC12	VSS						6151.88	11607.55
BC13	VSS						5501.64	11607.55
BC14	VSS						4851.4	11607.55
BC2	DDR0_DQ[31] / DDR0_DQ[47]				DDR0_DQ[31]	DDR0_DQ[47]	12663.93	11307.06
BC29	VCCGT						-7411.21	11423.9
BC3	DDR0_DQSP[3] / DDR0_DQSP[5]				DDR0_DQSP[3]	DDR0_DQSP[5]	12013.69	11307.06
BC30	VCCGT						-8061.45	11423.9
BC31	VCCGT						-8762.49	11423.9
BC32	VCCGT						-9412.73	11423.9
BC33	VSS						-10063	11423.9
BC34	VSS						-10713.2	11423.9
BC35	VCCGT						-11363.5	11423.9
BC36	VCCGT						-12013.7	11423.9
BC37	VCCGT						-12663.9	11423.9
BC38	VCCGT						-13314.2	11423.9
BC4	DDR0_DQ[26] / DDR0_DQ[42]				DDR0_DQ[26]	DDR0_DQ[42]	11363.45	11307.06
BC5	DDR0_DQ[27] / DDR0_DQ[43]				DDR0_DQ[27]	DDR0_DQ[43]	10713.21	11307.06
BC6	VSS						10062.97	11256.26

Table 9-1. Processor Ball List (Sheet 18 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BC7	DDR1_DQ[30]/ DDR0_DQ[62]				DDR1_DQ[30]	DDR0_DQ[62]	9403.08	11607.55
BC8	DDR1_DQ[27]/ DDR0_DQ[59]				DDR1_DQ[27]	DDR0_DQ[59]	8752.84	11607.55
BC9	DDR1_DQSN[3]/ DDR0_DQSN[7]				DDR1_DQSN[3]	DDR0_DQSN[7]	8102.6	11607.55
BD1	DDR0_DQ[25]/ DDR0_DQ[41]				DDR0_DQ[25]	DDR0_DQ[41]	13314.17	12043.66
BD10	VSS						7452.36	12521.95
BD11	VSS						6802.12	12521.95
BD12	VSS						6151.88	12521.95
BD13	VCCGT						5501.64	12521.95
BD14	VCCGT						4851.4	12521.95
BD2	DDR0_DQ[24] / DDR0_DQ[40]				DDR0_DQ[24]	DDR0_DQ[40]	12663.93	12043.66
BD29	VCCGT						-7411.21	12211.3
BD3	DDR0_DQSN[3] / DDR0_DQSN[5]				DDR0_DQSN[3]	DDR0_DQSN[5]	12013.69	12043.66
BD30	VCCGT						-8061.45	12211.3
BD31	VCCGT						-8762.49	12211.3
BD32	VCCGT						-9412.73	12211.3
BD33	VCCGT						-10063	12211.3
BD34	VCCGT						-10713.2	12211.3
BD35	VCCGT						-11363.5	12211.3
BD36	VCCGT						-12013.7	12211.3
BD37	VSS						-12663.9	12211.3
BD38	VSS						-13314.2	12211.3
BD4	DDR0_DQ[29] / DDR0_DQ[45]				DDR0_DQ[29]	DDR0_DQ[45]	11363.45	12043.66
BD5	DDR0_DQ[28] / DDR0_DQ[44]				DDR0_DQ[28]	DDR0_DQ[44]	10713.21	12043.66
BD6	VSS						10062.97	12094.46
BD7	VSS						9403.08	12521.95
BD8	VSS						8752.84	12521.95
BD9	VSS						8102.6	12521.95
BE1	VSS						13314.17	12932.66
BE2	VSS						12663.93	12932.66
BE29	VSS						-7411.21	12998.7
BE3	VSS						12013.69	12932.66
BE30	VSS						-8061.45	12998.7
BE31	VCCGT						-8762.49	12998.7
BE32	VCCGT						-9412.73	12998.7
BE33	VCCGT						-10063	12998.7

Table 9-1. Processor Ball List (Sheet 19 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BE34	VCCGT						-10713.2	12998.7
BE35	VCCGT						-11363.5	12998.7
BE36	VCCGT						-12013.7	12998.7
BE37	VCCGT						-12663.9	12998.7
BE38	VCCGT						-13314.2	12998.7
BE4	VSS						11363.45	12932.66
BE5	VSS						10713.21	12932.66
BE6	VSS						10062.97	12932.66
BF1	DDR0_DQ[22] / DDR0_DQ[38]				DDR0_DQ[22]	DDR0_DQ[38]	13314.17	13821.66
BF10	DDR1_DQ[21] / DDR0_DQ[53]				DDR1_DQ[21]	DDR0_DQ[53]	7452.36	13436.35
BF11	DDR1_DQ[20] / DDR0_DQ[52]				DDR1_DQ[20]	DDR0_DQ[52]	6802.12	13436.35
BF12	VSS						6151.88	13436.35
BF13	VCCGT						5501.64	13436.35
BF14	VCCGT						4851.4	13436.35
BF2	DDR0_DQ[23] / DDR0_DQ[39]				DDR0_DQ[23]	DDR0_DQ[39]	12663.93	13821.66
BF29	VCCGT						-7411.21	13786.1
BF3	DDR0_DQSP[2] / DDR0_DQSP[4]				DDR0_DQSP[2]	DDR0_DQSP[4]	12013.69	13821.66
BF30	VCCGT						-8061.45	13786.1
BF31	VCCGT						-8762.49	13786.1
BF32	VCCGT						-9412.73	13786.1
BF33	VSS						-10063	13786.1
BF34	VSS						-10713.2	13786.1
BF35	VCCGT						-11363.5	13786.1
BF36	VCCGT						-12013.7	13786.1
BF37	VCCGT						-12663.9	13786.1
BF38	VCCGT						-13314.2	13786.1
BF4	DDR0_DQ[18] / DDR0_DQ[34]				DDR0_DQ[18]	DDR0_DQ[34]	11363.45	13821.66
BF5	DDR0_DQ[19] / DDR0_DQ[35]				DDR0_DQ[19]	DDR0_DQ[35]	10713.21	13821.66
BF6	VSS						10062.97	13770.86
BF7	DDR1_DQ[23] / DDR0_DQ[55]				DDR1_DQ[23]	DDR0_DQ[55]	9403.08	13436.35
BF8	DDR1_DQ[19] / DDR0_DQ[51]				DDR1_DQ[19]	DDR0_DQ[51]	8752.84	13436.35
BF9	DDR1_DQSP[2] / DDR0_DQSP[6]				DDR1_DQSP[2]	DDR0_DQSP[6]	8102.6	13436.35
BG1	DDR0_DQ[21] / DDR0_DQ[37]				DDR0_DQ[21]	DDR0_DQ[37]	13314.17	14558.26
BG10	DDR1_DQ[17] / DDR0_DQ[49]				DDR1_DQ[17]	DDR0_DQ[49]	7452.36	14350.75

Table 9-1. Processor Ball List (Sheet 20 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BG11	DDR1_DQ[16] / DDR0_DQ[48]				DDR1_DQ[16]	DDR0_DQ[48]	6802.12	14350.75
BG12	VSS						6151.88	14350.75
BG13	VSS						5501.64	14350.75
BG14	VSS						4851.4	14350.75
BG2	DDR0_DQ[20] / DDR0_DQ[36]				DDR0_DQ[20]	DDR0_DQ[36]	12663.93	14558.26
BG29	VCCGT						-7411.21	14573.5
BG3	DDR0_DQSN[2] / DDR0_DQSN[4]				DDR0_DQSN[2]	DDR0_DQSN[4]	12013.69	14558.26
BG30	VCCGT						-8061.45	14573.5
BG31	VCCGT						-8762.49	14573.5
BG32	VCCGT						-9412.73	14573.5
BG33	VCCGT						-10063	14573.5
BG34	VCCGT						-10713.2	14573.5
BG35	VCCGT						-11363.5	14573.5
BG36	VCCGT						-12013.7	14573.5
BG37	VSS						-12663.9	14573.5
BG38	VSS						-13314.2	14573.5
BG4	DDR0_DQ[16] / DDR0_DQ[32]				DDR0_DQ[16]	DDR0_DQ[32]	11363.45	14558.26
BG5	DDR0_DQ[17] / DDR0_DQ[33]				DDR0_DQ[17]	DDR0_DQ[33]	10713.21	14558.26
BG6	VSS						10062.97	14609.06
BG7	DDR1_DQ[22] / DDR0_DQ[54]				DDR1_DQ[22]	DDR0_DQ[54]	9403.08	14350.75
BG8	DDR1_DQ[18] / DDR0_DQ[50]				DDR1_DQ[18]	DDR0_DQ[50]	8752.84	14350.75
BG9	DDR1_DQSN[2] / DDR0_DQSN[6]				DDR1_DQSN[2]	DDR0_DQSN[6]	8102.6	14350.75
BH1	VSS						13314.17	15701.26
BH10	VSS						7452.36	15265.15
BH11	VSS						6802.12	15265.15
BH12	VSS						6151.88	15265.15
BH13	VCCPLL_OC						5501.64	15265.15
BH14	VSS						4851.4	15227.05
BH2	VSS						12663.93	15447.26
BH29	VIDSOUT						-7411.21	15233.9
BH3	VSS						12013.69	15447.26
BH30	RSVD						-8061.45	15360.9
BH31	VIDALERT#						-8762.49	15360.9
BH32	VIDSCK						-9412.73	15360.9
BH33	VCCGT						-10063	15360.9

Table 9-1. Processor Ball List (Sheet 21 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BH34	VCCGT						-10713.2	15360.9
BH35	VCCGT						-11363.5	15360.9
BH36	VCCGT						-12013.7	15360.9
BH37	VCCGT						-12663.9	15360.9
BH38	VCCGT						-13314.2	15360.9
BH4	VSS						11363.45	15447.26
BH5	VSS						10713.21	15447.26
BH6	VSS						10062.97	15447.26
BH7	VSS						9403.08	15265.15
BH8	VSS						8752.84	15265.15
BH9	VSS						8102.6	15265.15
BJ10	DDR1_DQ[13] / DDR0_DQ[29]				DDR1_DQ[13]	DDR0_DQ[29]	7452.36	16179.55
BJ11	DDR1_DQ[12] / DDR0_DQ[28]				DDR1_DQ[12]	DDR0_DQ[28]	6802.12	16179.55
BJ12	VSS						6032.5	16090.9
BJ13	RSVD_TP						5143.5	15811.5
BJ14	RSVD_TP						4462.78	15762.48
BJ15	VSS						3713.48	15762.48
BJ16	RSVD_TP						2926.08	15762.48
BJ17	VCCOPC						2138.68	15762.48
BJ18	VSS						1351.28	15762.48
BJ19	VCCOPC						563.88	15762.48
BJ20	VCCOPC						-223.52	15762.48
BJ21	RSVD						-1010.92	15762.48
BJ22	VSS						-1798.32	15762.48
BJ23	RSVD						-2585.72	15762.48
BJ24	RSVD_TP						-3373.12	15762.48
BJ25	VSS						-4160.52	15762.48
BJ26	RSVD						-4947.92	15762.48
BJ27	RSVD						-5735.32	15762.48
BJ28	RSVD						-6522.72	15762.48
BJ29	VSS						-7183.12	15843.76
BJ30	VSS						-8039.1	16014.7
BJ31	VSS						-8762.49	16148.3
BJ32	VSS						-9412.73	16148.3
BJ33	RSVD_TP						-10063	16148.3
BJ34	RSVD_TP						-10713.2	16148.3
BJ35	RSVD						-11363.5	16148.3

Table 9-1. Processor Ball List (Sheet 22 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BJ36	RSVD						-12013.7	16148.3
BJ37	VCCGT						-12663.9	16148.3
BJ38	VCCGT						-13314.2	16097.5
BJ7	DDR1_DQ[15] / DDR0_DQ[31]				DDR1_DQ[15]	DDR0_DQ[31]	9403.08	16179.55
BJ8	DDR1_DQ[11] / DDR0_DQ[27]				DDR1_DQ[11]	DDR0_DQ[27]	8752.84	16179.55
BJ9	DDR1_DQSP[1] / DDR0_DQSP[3]				DDR1_DQSP[1]	DDR0_DQSP[3]	8102.6	16179.55
BK1	DDR0_DQ[14]						13314.17	16722.34
BK13	VSS						5415.28	16412.72
BK14	VSS						4500.88	16412.72
BK15	VSS						3713.48	16412.72
BK16	RSVD_TP						2926.08	16412.72
BK17	VCCOPC						2138.68	16412.72
BK18	VSS						1351.28	16412.72
BK19	VCCOPC						563.88	16412.72
BK2	DDR0_DQ[15]						12663.93	16285.46
BK20	VCCOPC						-223.52	16412.72
BK21	RSVD						-1010.92	16412.72
BK22	VSS						-1798.32	16412.72
BK23	RSVD						-2585.72	16412.72
BK24	RSVD_TP						-3373.12	16412.72
BK25	VSS						-4160.52	16412.72
BK26	RSVD						-4947.92	16412.72
BK27	RSVD						-5735.32	16412.72
BK28	RSVD						-6522.72	16412.72
BK29	VSS						-7518.4	16421.1
BK3	DDR0_DQSP[1]						12013.69	16285.46
BK4	DDR0_DQ[12]						11363.45	16285.46
BK5	DDR0_DQ[13]						10713.21	16285.46
BK6	VSS						10062.97	16285.46
BL11	DDR1_DQ[9] / DDR0_DQ[25]				DDR1_DQ[9]	DDR0_DQ[25]	6863.08	17062.96
BL12	DDR1_DQ[8] / DDR0_DQ[24]				DDR1_DQ[8]	DDR0_DQ[24]	6075.68	17062.96
BL13	VSS						5288.28	17062.96
BL14	VCC_OPC_1P8						4500.88	17062.96
BL15	VCCOPC_SENSE						3713.48	17062.96
BL16	VCCOPC						2926.08	17062.96
BL17	VCCOPC						2138.68	17062.96

Table 9-1. Processor Ball List (Sheet 23 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BL18	VCCOPC						1351.28	17062.96
BL19	VCCOPC						563.88	17062.96
BL2	DDR0_DQ[10]						12663.93	17123.66
BL20	VCCOPC						-223.52	17062.96
BL21	VCCOPC						-1010.92	17062.96
BL22	RSVD						-1798.32	17062.96
BL23	RSVD						-2585.72	17062.96
BL24	RSVD						-3373.12	17062.96
BL25	RSVD						-4160.52	17062.96
BL26	RSVD						-4947.92	17062.96
BL27	RSVD						-5735.32	17062.96
BL28	RSVD						-6522.72	17062.96
BL29	VSS						-7310.12	17062.96
BL3	DDR0_DQSN[1]						12013.69	17072.86
BL30	PROC_PREQ#						-8112.25	16935.7
BL31	RSVD						-8762.49	16935.7
BL32	PROC_TDI						-9412.73	16935.7
BL33	RSVD_TP						-10063	16935.7
BL34	RSVD						-10713.2	16935.7
BL35	VSS						-11363.5	16935.7
BL36	VCCGT						-12013.7	16935.7
BL37	VCCGT						-12663.9	16935.7
BL38	VSS						-13314.2	16862.04
BL4	DDR0_DQ[8]						11363.45	17072.86
BL5	DDR0_DQ[9]						10713.21	17072.86
BL6	VSS						10062.97	17123.66
BL7	DDR1_DQ[14] / DDR0_DQ[30]				DDR1_DQ[14]	DDR0_DQ[30]	9326.88	17068.55
BL8	DDR1_DQ[10] / DDR0_DQ[26]				DDR1_DQ[10]	DDR0_DQ[26]	8437.88	17062.96
BL9	DDR1_DQSN[1] / DDR0_DQSN[3]				DDR1_DQSN[1]	DDR0_DQSN[3]	7650.48	17062.96
BM1	DDR0_DQ[11]						13314.17	17499.58
BM11	VSS						6863.08	17713.2
BM12	VSS						6075.68	17713.2
BM13	VSS						5288.28	17713.2
BM14	VCC_OPC_1P8						4500.88	17713.2
BM15	VSSEOPIO_SENSE						3713.48	17713.2
BM16	VSSOPC_SENSE						2926.08	17713.2
BM17	VCCOPC						2138.68	17713.2

Table 9-1. Processor Ball List (Sheet 24 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BM18	VSS						1351.28	17713.2
BM19	CFG[12]						563.88	17713.2
BM2	VSS						12351.51	17738.34
BM20	CFG[5]						-223.52	17713.2
BM21	VSS						-1010.92	17713.2
BM22	RSVD						-1798.32	17713.2
BM23	VSS						-2585.72	17713.2
BM24	RSVD						-3373.12	17713.2
BM25	VSS						-4160.52	17713.2
BM26	VSS						-4947.92	17713.2
BM27	VSS						-5735.32	17713.2
BM28	VSS						-6522.72	17713.2
BM29	VSS						-7310.12	17713.2
BM3	VSS						11701.27	17814.54
BM30	CATERR#						-8097.52	17713.2
BM31	BPM#[2]						-8884.92	17713.2
BM33	RSVD_TP						-9672.32	17713.2
BM34	PM_SYNC						-10459.7	17713.2
BM35	VSS						-11247.1	17713.2
BM36	VCCGT						-12013.7	17672.3
BM37	VCCGT						-12663.9	17672.3
BM38	VSS						-13314.2	17573.5
BM5	VSS						10788.9	17814.54
BM6	VSS						10144.76	17916.4
BM7	VSS						9225.28	17713.2
BM8	VSS						8437.88	17713.2
BM9	VSS						7650.48	17713.2
BN1	PROC_SELECT#						13314.17	18299.68
BN11	DDR1_DQ[5] / DDR0_DQ[21]				DDR1_DQ[5]	DDR0_DQ[21]	6863.08	18363.44
BN12	VSS						6075.68	18363.44
BN13	DDR_VREF_CA						5288.28	18363.44
BN14	VSS						4500.88	18363.44
BN15	VCCEOPIO_SENSE						3713.48	18363.44
BN16	RSVD						2926.08	18363.44
BN17	VCCOPC						2138.68	18363.44
BN18	VSS						1351.28	18363.44
BN19	VSS						563.88	18363.44
BN2	VSS						12663.93	18327.62

Table 9-1. Processor Ball List (Sheet 25 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BN20	VSS						-223.52	18363.44
BN21	VSS						-1010.92	18363.44
BN22	CFG[18]						-1798.32	18363.44
BN23	CFG[17]						-2585.72	18363.44
BN24	VSS						-3373.12	18363.44
BN25	CFG[0]						-4160.52	18363.44
BN26	CFG[2]						-4947.92	18363.44
BN27	CFG[1]						-5735.32	18363.44
BN28	CFG[3]						-6522.72	18363.44
BN29	VSS						-7310.12	18363.44
BN3	DDR0_DQ[7]						12014.2	18387.06
BN30	VSS						-8097.52	18363.44
BN31	VSS						-8884.92	18363.44
BN33	RSVD						-9672.32	18363.44
BN34	VSS						-10459.7	18363.44
BN35	RSVD						-11247.6	18363.44
BN36	VCCGT						-11999.5	18323.81
BN37	VCCGT						-12651.2	18350.48
BN38	VCCGT						-13314.2	18284.7
BN4	VSS						11208.51	18314.92
BN5	DDR0_DQ[4]						10566.4	18478.5
BN7	VSS						9225.28	18363.44
BN8	DDR1_DQ[7] / DDR0_DQ[23]				DDR1_DQ[7]	DDR0_DQ[23]	8437.88	18363.44
BN9	VSS						7650.48	18363.44
BP1	NCTF						13314.17	19023.58
BP11	DDR1_DQ[4] / DDR0_DQ[20]				DDR1_DQ[4]	DDR0_DQ[20]	6863.08	19013.68
BP12	VSS						6075.68	19013.68
BP13	DDR0_VREF_DQ						5288.28	19013.68
BP14	VSS						4500.88	19013.68
BP15	VCCEOPIO						3713.48	19013.68
BP16	RSVD						2926.08	19013.68
BP17	RSVD						2138.68	19013.68
BP18	VSS						1351.28	19013.68
BP19	CFG[14]						563.88	19013.68
BP2	DDR0_DQ[6]						12486.13	18965.42
BP20	CFG[7]						-223.52	19013.68
BP21	VSS						-1010.92	19013.68

Table 9-1. Processor Ball List (Sheet 26 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BP22	CFG[19]						-1798.32	19013.68
BP23	CFG[16]						-2585.72	19013.68
BP24	VSS						-3373.12	19013.68
BP25	OPCE_RCOMP2						-4160.52	19013.68
BP26	VSS						-4947.92	19013.68
BP27	PROC_PRDY#						-5735.32	19013.68
BP28	PROC_TMS						-6522.72	19013.68
BP29	VSS						-7310.12	19013.68
BP3	DDR0_DQ[2]						11831.32	19019.52
BP30	PROC_TRST#						-8097.52	19013.68
BP31	PM_DOWN						-8884.92	19013.68
BP33	VSS						-9672.32	19013.68
BP34	VSS						-10459.7	19013.68
BP35	RESET#						-11247.1	19013.68
BP37	VCCGT						-12374.4	18942.56
BP38	VCCGT						-13314.2	18995.9
BP5	DDR0_DQSP[0]						10939.78	19037.3
BP6	DDR0_DQ[5]						10020.3	18973.8
BP7	VSS						9225.28	19013.68
BP8	DDR1_DQ[6] / DDR0_DQ[22]				DDR1_DQ[6]	DDR0_DQ[22]	8437.88	19013.68
BP9	DDR1_DQSN[0] / DDR0_DQSN[2]				DDR1_DQSN[0]	DDR0_DQSN[2]	7650.48	19013.68
BR1	RSVD_TP						13314.17	19747.74
BR11	DDR1_DQ[1] / DDR0_DQ[17]				DDR1_DQ[1]	DDR0_DQ[17]	6863.08	19663.92
BR12	VSS						6075.68	19663.92
BR13	DDR1_VREF_DQ						5288.28	19663.92
BR14	VSS						4500.88	19663.92
BR15	VCCEOPIO						3713.48	19663.92
BR16	RSVD						2926.08	19663.92
BR17	RSVD						2138.68	19663.92
BR18	VSS						1351.28	19663.92
BR19	CFG[13]						563.88	19663.92
BR2	NCTF						12595.48	19619.47
BR20	CFG[4]						-223.52	19663.92
BR21	VSS						-1010.92	19663.92
BR22	CFG[9]						-1798.32	19663.92
BR23	CFG[8]						-2585.72	19663.92
BR24	VSS						-3373.12	19663.92

Table 9-1. Processor Ball List (Sheet 27 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BR25	OPCE_RCOMP						-4160.52	19663.92
BR26	VSS						-4947.92	19663.92
BR27	BPM#[0]						-5735.32	19663.92
BR28	PROC_TCK						-6522.72	19663.92
BR29	VSS						-7310.12	19663.92
BR3	DDR0_DQ[3]						11927.33	19663.92
BR30	PROCHOT#						-8097.52	19663.92
BR31	RSVD						-8884.92	19663.92
BR33	SKTOCC#						-9672.32	19663.92
BR34	VSS						-10459.7	19663.92
BR35	RSVD						-11221.7	19663.92
BR36	VSS						-11879.1	19656.92
BR37	VCCGT						-12590.3	19613.12
BR38	NCTFVSS						-13314.2	19722.34
BR5	DDR0_DQSN[0]						11148.06	19669.76
BR6	DDR0_DQ[0]						10121.9	19646.9
BR7	VSS						9225.28	19663.92
BR8	DDR1_DQ[3] / DDR0_DQ[19]				DDR1_DQ[3]	DDR0_DQ[19]	8437.88	19663.92
BR9	DDR1_DQSP[0] / DDR0_DQSP[2]				DDR1_DQSP[0]	DDR0_DQSP[2]	7650.48	19663.92
BT11	DDR1_DQ[0] / DDR0_DQ[16]				DDR1_DQ[0]	DDR0_DQ[16]	6863.08	20314.16
BT12	VSS						6075.68	20314.16
BT13	DDR_VTT_CNTL						5288.28	20314.16
BT14	VSS						4500.88	20314.16
BT15	VCCEOPIO						3713.48	20314.16
BT16	RSVD						2926.08	20314.16
BT17	RSVD						2138.68	20314.16
BT18	VSS						1351.28	20314.16
BT19	CFG[15]						563.88	20314.16
BT2	RSVD_TP						12743.18	20314.16
BT20	CFG[6]						-223.52	20314.16
BT21	VSS						-1010.92	20314.16
BT22	CFG[11]						-1798.32	20314.16
BT23	CFG[10]						-2585.72	20314.16
BT24	VSS						-3373.12	20314.16
BT25	CFG_RCOMP						-4160.52	20314.16
BT26	VSS						-4947.92	20314.16
BT27	BPM#[1]						-5735.32	20314.16

Table 9-1. Processor Ball List (Sheet 28 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
BT28	PROC_TDO						-6522.72	20314.16
BT29	OPC_RCOMP						-7310.12	20314.16
BT3	NCTFVSS						12019.28	20314.16
BT30	BPM#[3]						-8097.52	20314.16
BT31	PROCPWRGD						-8859.52	20314.16
BT32	VSS						-9608.82	20314.16
BT34	PECI						-10383.5	20314.16
BT35	NCTFVSS						-11183.6	20314.16
BT36	NCTFVSS						-11996.4	20314.16
BT37	VCCGT						-12722.4	20314.16
BT4	NCTFVSS						11295.38	20314.16
BT5	VSS						10495.28	20314.16
BT6	DDR0_DQ[1]						9720.58	20314.16
BT8	DDR1_DQ[2] / DDR0_DQ[18]				DDR1_DQ[2]	DDR0_DQ[18]	8666.48	20314.16
BT9	VSS						7650.48	20314.16
C1	NCTF						13314.17	-19047
C10	PEG_TXP[15]						7421.37	-19013.7
C11	VSS						6633.97	-19013.7
C12	PEG_TXP[13]						5846.57	-19013.7
C13	VSS						5059.17	-19013.7
C14	PEG_TXP[11]						4271.77	-19013.7
C15	VSS						3484.37	-19013.7
C16	PEG_TXP[9]						2696.97	-19013.7
C17	VSS						1909.57	-19013.7
C18	PEG_TXN[7]						1122.17	-19013.7
C19	VSS						334.77	-19013.7
C2	NCTFVSS						12615.67	-18952.7
C20	PEG_TXN[5]						-452.63	-19013.7
C21	VSS						-1240.03	-19013.7
C22	PEG_TXN[3]						-2027.43	-19013.7
C23	VSS						-2814.83	-19013.7
C24	PEG_TXN[1]						-3602.23	-19013.7
C25	VSS						-4389.63	-19013.7
C26	EDP_AUXP						-5177.03	-19013.7
C27	VSS						-5964.43	-19013.7
C28	EDP_TXP[3]						-6751.83	-19013.7
C29	VSS						-7539.23	-19013.7
C30	RSVD						-8326.63	-19013.7

Table 9-1. Processor Ball List (Sheet 29 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
C31	VSS						-9114.03	-19013.7
C33	DDI3_TXP[3]						-9901.43	-19013.7
C34	DDI3_TXP[0]						-10697	-19024.6
C36	PCI_BCLKN						-11831.3	-18925.8
C37	VSS						-12594.1	-18911.8
C38	NCTF						-13314.2	-18980.2
C5	VSS						10570.97	-19013.7
C6	DMI_TXP[1]						9783.57	-19013.7
C8	VSS						8996.17	-19013.7
C9	VSS						8208.77	-19013.7
D1	RSVD_TP						13314.17	-18323.1
D10	VSS						7421.37	-18363.4
D11	PEG_RXP[14]						6633.97	-18363.4
D12	VSS						5846.57	-18363.4
D13	PEG_RXP[12]						5059.17	-18363.4
D14	VSS						4271.77	-18363.4
D15	PEG_RXP[10]						3484.37	-18363.4
D16	VSS						2696.97	-18363.4
D17	PEG_RXP[8]						1909.57	-18363.4
D18	VSS						1122.17	-18363.4
D19	PEG_RXN[6]						334.77	-18363.4
D20	VSS						-452.63	-18363.4
D21	PEG_RXN[4]						-1240.03	-18363.4
D22	VSS						-2027.43	-18363.4
D23	PEG_RXN[2]						-2814.83	-18363.4
D24	VSS						-3602.23	-18363.4
D25	PEG_RXN[0]						-4389.63	-18363.4
D26	VSS						-5177.03	-18363.4
D27	DDI1_AUXP						-5964.43	-18363.4
D28	VSS						-6751.83	-18363.4
D29	EDP_TXP[0]						-7539.23	-18363.4
D3	VSS						12080.75	-18491.7
D30	VSS						-8326.63	-18363.4
D31	CLK24N						-9114.03	-18363.4
D33	VSS						-9901.43	-18363.4
D34	DDI3_TXN[0]						-10688.8	-18363.4
D35	PCI_BCLKP						-11341.1	-18453.1
D37	eDP_RCOMP						-12288.5	-18328.9

Table 9-1. Processor Ball List (Sheet 30 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
D38	NCTFVSS						-13314.2	-18217.6
D4	DMI_TXP[3]						11420.09	-18659.6
D5	DMI_RXP[2]						10570.97	-18363.4
D6	VSS						9783.57	-18363.4
D8	DMI_RXP[0]						8996.17	-18363.4
D9	VSS						8208.77	-18363.4
E1	RSVD_TP						13314.17	-17535.7
E10	PEG_RXN[15]						7421.37	-17713.2
E11	PEG_RXN[14]						6633.97	-17713.2
E12	PEG_RXN[13]						5846.57	-17713.2
E13	PEG_RXN[12]						5059.17	-17713.2
E14	PEG_RXN[11]						4271.77	-17713.2
E15	PEG_RXN[10]						3484.37	-17713.2
E16	PEG_RXN[9]						2696.97	-17713.2
E17	PEG_RXN[8]						1909.57	-17713.2
E18	PEG_RXP[7]						1122.17	-17713.2
E19	PEG_RXP[6]						334.77	-17713.2
E2	RSVD_TP						12663.93	-17840.5
E20	PEG_RXP[5]						-452.63	-17713.2
E21	PEG_RXP[4]						-1240.03	-17713.2
E22	PEG_RXP[3]						-2027.43	-17713.2
E23	PEG_RXP[2]						-2814.83	-17713.2
E24	PEG_RXP[1]						-3602.23	-17713.2
E25	PEG_RXP[0]						-4389.63	-17713.2
E26	DDI2_AUXN						-5177.03	-17713.2
E27	DDI1_AUXN						-5964.43	-17713.2
E28	EDP_TXN[1]						-6751.83	-17713.2
E29	EDP_TXN[0]						-7539.23	-17713.2
E3	RSVD_TP						12013.69	-17840.5
E30	RSVD						-8326.63	-17713.2
E31	CLK24P						-9114.03	-17713.2
E33	DDI3_TXN[2]						-9901.43	-17713.2
E34	VSS						-10688.8	-17713.2
E35	VSS						-11363.5	-17709.9
E36	DDI2_TXN[3]						-12013.7	-17709.9
E37	DDI2_TXP[3]						-12663.9	-17709.9
E38	VSS						-13314.2	-17417.5
E4	VSS						11363.45	-17738.9

Table 9-1. Processor Ball List (Sheet 31 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
E5	DMI_RXN[2]						10570.97	-17713.2
E6	DMI_RXP[1]						9783.57	-17713.2
E8	DMI_RXN[0]						8996.17	-17713.2
E9	VSS						8208.77	-17713.2
F10	PEG_RXP[15]						7421.37	-17063
F11	VSS						6633.97	-17063
F12	PEG_RXP[13]						5846.57	-17063
F13	VSS						5059.17	-17063
F14	PEG_RXP[11]						4271.77	-17063
F15	VSS						3484.37	-17063
F16	PEG_RXP[9]						2696.97	-17063
F17	VSS						1909.57	-17063
F18	PEG_RXN[7]						1122.17	-17063
F19	VSS						334.77	-17063
F2	VSS						12663.93	-17154.7
F20	PEG_RXN[5]						-452.63	-17063
F21	VSS						-1240.03	-17063
F22	PEG_RXN[3]						-2027.43	-17063
F23	VSS						-2814.83	-17063
F24	PEG_RXN[1]						-3602.23	-17063
F25	VSS						-4389.63	-17063
F26	DDI2_AUXP						-5177.03	-17063
F27	VSS						-5964.43	-17063
F28	EDP_TXP[1]						-6751.83	-17063
F29	VSS						-7539.23	-17063
F3	VSS						12013.69	-17154.7
F30	RSVD						-8326.63	-17063
F31	VSS						-9114.03	-17063
F33	DDI3_TXP[2]						-9901.43	-17063
F34	DDI2_TXP[2]						-10713.2	-16922.5
F35	DDI2_TXN[2]						-11363.5	-16922.5
F36	VSS						-12013.7	-16922.5
F37	DDI2_TXP[1]						-12663.9	-16922.5
F4	VSS						11363.45	-17053.1
F5	VSS						10570.97	-17041.4
F6	DMI_RXN[1]						9783.57	-17041.4
F8	VSS						8996.17	-17063
F9	VSS						8208.77	-17063

Table 9-1. Processor Ball List (Sheet 32 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
G1	DDR_RCOMP[0]						13314.17	-16733
G10	VSS						7421.37	-16412.7
G11	VCCPLL_OC						6633.97	-16412.7
G12	VSS						5846.57	-16412.7
G13	RSVD						5059.17	-16412.7
G14	VSS						4271.77	-16412.7
G15	VCCIO						3484.37	-16412.7
G16	VSS						2696.97	-16412.7
G17	VCCIO						1909.57	-16412.7
G18	VSS						1122.17	-16412.7
G19	VCCIO						334.77	-16412.7
G2	PEG_RCOMP						12663.93	-16367.3
G20	VSS						-452.63	-16412.7
G21	VCCIO						-1240.03	-16412.7
G22	VSS						-2027.43	-16412.7
G23	VSS						-2814.83	-16412.7
G24	VSS						-3602.23	-16412.7
G25	PROC_AUDIO_SDI						-4389.63	-16412.7
G26	VSS						-5177.03	-16412.7
G27	PROC_AUDIO_CLK						-5964.43	-16412.7
G28	VSS						-6751.83	-16412.7
G29	PROC_AUDIO_SDO						-7539.23	-16412.7
G3	RSVD						12013.69	-16367.3
G30	VCCSTG						-8326.63	-16412.7
G38	DDI2_TXN[1]						-13314.2	-16642.8
G4	VSS						11363.45	-16367.3
G5	VSS						10713.21	-16367.3
G6	VSS						10062.97	-16367.3
G8	VSS						8996.17	-16412.7
G9	VSS						8208.77	-16412.7
H1	DDR_RCOMP[1]						13314.17	-15870.9
H11	VSS						6633.97	-15762.5
H12	VSS						5846.57	-15762.5
H13	VCCST_PWRGD						5059.17	-15711.7
H14	VCCIO_SENSE						4271.77	-15711.7
H15	VCCIO						3484.37	-15711.7
H16	VCCIO						2696.97	-15711.7
H17	VCCIO						1909.57	-15711.7

Table 9-1. Processor Ball List (Sheet 33 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
H18	VSS						1122.17	-15711.7
H19	VCCIO						334.77	-15711.7
H20	VCCIO						-452.63	-15711.7
H21	VCCIO						-1240.03	-15711.7
H22	VSS						-2027.43	-15711.7
H23	PROC_TRIGIN						-2814.83	-15711.7
H24	RSVD						-3602.23	-15711.7
H25	VSS						-4389.63	-15711.7
H26	VCCIO						-5177.03	-15711.7
H27	VCCIO						-5964.43	-15711.7
H28	VccPLL						-6751.83	-15711.7
H29	VCCSTG						-7539.23	-15762.5
H30	VCCST						-8288.53	-15762.5
H32	VSS						-9412.73	-16135.1
H33	DDI2_TXN[0]						-10063	-16135.1
H34	DDI2_TXP[0]						-10713.2	-16135.1
H35	VSS						-11363.5	-16135.1
H36	DDI1_TXN[2]						-12013.7	-16135.1
H37	DDI1_TXP[2]						-12663.9	-16135.1
J10	VSS						7421.37	-15686.3
J14	VSSIO_SENSE						4271.77	-15061.4
J15	VCCIO						3484.37	-15061.4
J16	VCCIO						2696.97	-15061.4
J17	VCCIO						1909.57	-15061.4
J18	VSS						1122.17	-15061.4
J19	VCCIO						334.77	-15061.4
J2	DDR_RCOMP[2]						12663.93	-15566.1
J20	VCCIO						-452.63	-15061.4
J21	VCCIO						-1240.03	-15061.4
J22	VSS						-2027.43	-15061.4
J23	PROC_TRIGOUT						-2814.83	-15061.4
J24	RSVD						-3602.23	-15061.4
J25	VSS						-4389.63	-15061.4
J26	VCCIO						-5177.03	-15061.4
J27	VCCIO						-5964.43	-15061.4
J28	VccPLL						-6751.83	-15061.4
J3	RSVD						12013.69	-15566.1
J30	VCCSA						-7747	-15146

Table 9-1. Processor Ball List (Sheet 34 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
J31	THERMTRIP#						-8762.49	-15309.6
J32	VSS						-9412.73	-15347.7
J33	VSS						-10063	-15347.7
J34	DDI1_TXN[1]						-10713.2	-15347.7
J35	DDI1_TXP[1]						-11363.5	-15347.7
J36	VSS						-12013.7	-15347.7
J37	DDI1_TXP[3]						-12663.9	-15347.7
J38	DDI1_TXN[3]						-13314.2	-15601.7
J4	VSS						11363.45	-15566.1
J5	VDDQ						10713.21	-15566.1
J6	VDDQ						10062.97	-15566.1
J7	VSS						9420.86	-15694.9
J8	DMI_RXP[3]						8773.16	-15598.4
J9	DMI_RXN[3]						8102.6	-15621.3
K1	VSS						13314.17	-14727.9
K10	VSS						7452.36	-14833.9
K11	VSS						6802.12	-14833.9
K12	VDDQ						6151.88	-14833.9
K13	VCC						5435.6	-15138.4
K14	VCC						4851.4	-14656.1
K2	VSS						12663.93	-14727.9
K29	VCCSA						-7411.21	-14560.3
K3	VSS						12013.69	-14727.9
K30	VCCSA						-8061.45	-14560.3
K31	VCCSA						-8762.49	-14560.3
K32	VCCSA						-9412.73	-14560.3
K33	VCCSA						-10063	-14560.3
K34	VCCSA						-10713.2	-14560.3
K35	VCCSA						-11363.5	-14560.3
K36	DDI1_TXP[0]						-12013.7	-14560.3
K37	DDI1_TXN[0]						-12663.9	-14560.3
K38	VSS						-13314.2	-14560.3
K4	VSS						11363.45	-14727.9
K5	VSS						10713.21	-14727.9
K6	VDDQ						10062.97	-14727.9
K7	VSS						9403.08	-14757.7
K8	VSS						8752.84	-14833.9
K9	VSS						8102.6	-14833.9

Table 9-1. Processor Ball List (Sheet 35 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
L1	DDR0_DQ[63] / DDR1_DQ[47]				DDR0_DQ[63]	DDR1_DQ[47]	13314.17	-13838.9
L10	DDR1_DQ[60]						7452.36	-13995.7
L11	DDR1_DQ[56]						6802.12	-13995.7
L12	VDDQ						6151.88	-13995.7
L13	VCC						5501.64	-13995.7
L14	VCC						4851.4	-13995.7
L2	DDR0_DQ[59] / DDR1_DQ[43]				DDR0_DQ[59]	DDR1_DQ[43]	12663.93	-13838.9
L29	VSS						-7411.21	-13772.9
L30	VSS						-8061.45	-13772.9
L31	VCCSA						-8762.49	-13772.9
L32	VCCSA						-9412.73	-13772.9
L33	VSS						-10063	-13772.9
L34	VSS						-10713.2	-13772.9
L35	VCCSA						-11363.5	-13772.9
L36	VCCSA						-12013.7	-13772.9
L37	VCCSA						-12663.9	-13772.9
L38	VCCSA						-13314.2	-13772.9
L4	DDR0_DQ[58] / DDR1_DQ[42]				DDR0_DQ[58]	DDR1_DQ[42]	11363.45	-13838.9
L5	DDR0_DQ[62] / DDR1_DQ[46]				DDR0_DQ[62]	DDR1_DQ[46]	10713.21	-13838.9
L6	VDDQ						10062.97	-13889.7
L7	DDR1_DQ[58]						9403.08	-13919.5
L8	DDR1_DQ[63]						8752.84	-13970.3
L9	DDR1_DQSP[7]						8102.6	-13995.7
M1	DDR0_DQ[57] / DDR1_DQ[41]				DDR0_DQ[57]	DDR1_DQ[41]	13314.17	-13102.3
M10	DDR1_DQ[61]						7452.36	-13081.3
M11	DDR1_DQ[57]						6802.12	-13081.3
M12	VSS						6151.88	-13081.3
M13	VSS						5501.64	-13081.3
M14	VSS						4851.4	-13081.3
M2	DDR0_DQ[61] / DDR1_DQ[45]				DDR0_DQ[61]	DDR1_DQ[45]	12663.93	-13102.3
M29	VCCSA						-7411.21	-12985.5
M30	VCCSA						-8061.45	-12985.5
M31	VCCSA						-8762.49	-12985.5
M32	VCCSA						-9412.73	-12985.5
M33	VCCSA						-10063	-12985.5
M34	VCCSA						-10713.2	-12985.5

Table 9-1. Processor Ball List (Sheet 36 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
M35	VCCSA						-11363.5	-12985.5
M36	VCCSA						-12013.7	-12985.5
M37	VSSSA_SENSE						-12663.9	-12985.5
M38	VCCSA_SENSE						-13314.2	-12985.5
M4	DDR0_DQ[56] / DDR1_DQ[40]				DDR0_DQ[56]	DDR1_DQ[40]	11363.45	-13102.3
M5	DDR0_DQ[60] / DDR1_DQ[44]				DDR0_DQ[60]	DDR1_DQ[44]	10713.21	-13102.3
M6	VSS						10062.97	-13051.5
M7	DDR1_DQ[62]						9403.08	-13081.3
M8	DDR1_DQ[59]						8752.84	-13081.3
M9	DDR1_DQSN[7]						8102.6	-13081.3
N1	VSS						13314.17	-12213.3
N10	VSS						7452.36	-12166.9
N11	VSS						6802.12	-12166.9
N12	VSS						6151.88	-12166.9
N13	VCC						5501.64	-12166.9
N14	VCC						4851.4	-12166.9
N2	VSS						12663.93	-12213.3
N29	RSVD						-7411.21	-12198.1
N3	VSS						12013.69	-12213.3
N30	VCC						-8061.45	-12198.1
N31	VCC						-8762.49	-12198.1
N32	VCC						-9412.73	-12198.1
N33	VSS						-10063	-12198.1
N34	VSS						-10713.2	-12198.1
N35	VCC						-11363.5	-12198.1
N36	VCC						-12013.7	-12198.1
N37	VCC						-12663.9	-12198.1
N38	VCC						-13314.2	-12198.1
N4	VSS						11363.45	-12213.3
N5	VSS						10713.21	-12213.3
N6	VSS						10062.97	-12213.3
N7	VSS						9403.08	-12166.9
N8	VSS						8752.84	-12166.9
N9	VSS						8102.6	-12166.9
P1	DDR0_DQ[55] / DDR1_DQ[39]				DDR0_DQ[55]	DDR1_DQ[39]	13314.17	-11324.3
P10	DDR1_DQ[53]						7452.36	-11252.5
P11	DDR1_DQ[49]						6802.12	-11252.5

Table 9-1. Processor Ball List (Sheet 37 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
P12	VSS						6151.88	-11252.5
P13	VCC						5501.64	-11252.5
P14	VCC						4851.4	-11252.5
P2	DDR0_DQ[53] / DDR1_DQ[37]				DDR0_DQ[53]	DDR1_DQ[37]	12663.93	-11324.3
P29	VCC						-7411.21	-11410.7
P30	VCC						-8061.45	-11410.7
P31	VCC						-8762.49	-11410.7
P32	VCC						-9412.73	-11410.7
P33	VCC						-10063	-11410.7
P34	VCC						-10713.2	-11410.7
P35	VCC						-11363.5	-11410.7
P36	VCC						-12013.7	-11410.7
P37	VSS						-12663.9	-11410.7
P38	VSS						-13314.2	-11410.7
P4	DDR0_DQ[51] / DDR1_DQ[35]				DDR0_DQ[51]	DDR1_DQ[35]	11363.45	-11324.3
P5	DDR0_DQ[49] / DDR1_DQ[33]				DDR0_DQ[49]	DDR1_DQ[33]	10713.21	-11324.3
P6	VSS						10062.97	-11375.1
P7	DDR1_DQ[50]						9403.08	-11252.5
P8	DDR1_DQ[55]						8752.84	-11252.5
P9	DDR1_DQSP[6]						8102.6	-11252.5
R1	DDR0_DQ[54] / DDR1_DQ[38]				DDR0_DQ[54]	DDR1_DQ[38]	13314.17	-10587.7
R10	DDR1_DQ[52]						7452.36	-10338.1
R11	DDR1_DQ[48]						6802.12	-10338.1
R12	VSS						6151.88	-10338.1
R13	VCC						5501.64	-10338.1
R14	RSVD						4851.4	-10338.1
R2	DDR0_DQ[48] / DDR1_DQ[32]				DDR0_DQ[48]	DDR1_DQ[32]	12663.93	-10587.7
R29	VSS						-7411.21	-10623.3
R30	VSS						-8061.45	-10623.3
R31	VCC						-8762.49	-10623.3
R32	VCC						-9412.73	-10623.3
R33	VCC						-10063	-10623.3
R34	VCC						-10713.2	-10623.3
R35	VCC						-11363.5	-10623.3
R36	VCC						-12013.7	-10623.3
R37	VCC						-12663.9	-10623.3

Table 9-1. Processor Ball List (Sheet 38 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
R38	VCC						-13314.2	-10623.3
R4	DDR0_DQ[50] / DDR1_DQ[34]				DDR0_DQ[50]	DDR1_DQ[34]	11363.45	-10587.7
R5	DDR0_DQ[52] / DDR1_DQ[36]				DDR0_DQ[52]	DDR1_DQ[36]	10713.21	-10587.7
R6	VDDQ						10062.97	-10536.9
R7	DDR1_DQ[54]						9403.08	-10338.1
R8	DDR1_DQ[51]						8752.84	-10338.1
R9	DDR1_DQSN[6]						8102.6	-10338.1
T1	VSS						13314.17	-9698.74
T10	VSS						7452.36	-9423.65
T11	VSS						6802.12	-9423.65
T12	VSS						6151.88	-9423.65
T13	VSS						5501.64	-9423.65
T14	VSS						4851.4	-9423.65
T2	VSS						12663.93	-9698.74
T29	VCC						-7411.21	-9835.9
T3	VSS						12013.69	-9698.74
T30	VCC						-8061.45	-9835.9
T31	VCC						-8762.49	-9835.9
T32	VCC						-9412.73	-9835.9
T33	VSS						-10063	-9835.9
T34	VSS						-10713.2	-9835.9
T35	VCC						-11363.5	-9835.9
T36	VCC						-12013.7	-9835.9
T37	VCC						-12663.9	-9835.9
T38	VCC						-13314.2	-9835.9
T4	VSS						11363.45	-9698.74
T5	VSS						10713.21	-9698.74
T6	VDDQ						10062.97	-9698.74
T7	VSS						9403.08	-9423.65
T8	VSS						8752.84	-9423.65
T9	VSS						8102.6	-9423.65
U1	DDR0_DQ[42] / DDR1_DQ[10]				DDR0_DQ[42]	DDR1_DQ[10]	13314.17	-8809.74
U2	DDR0_DQ[43] / DDR1_DQ[11]				DDR0_DQ[43]	DDR1_DQ[11]	12663.93	-8809.74
U29	VCC						-7411.21	-9048.5
U30	VCC						-8061.45	-9048.5
U31	VCC						-8762.49	-9048.5
U32	VCC						-9412.73	-9048.5

Table 9-1. Processor Ball List (Sheet 39 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
U33	VCC						-10063	-9048.5
U34	VCC						-10713.2	-9048.5
U35	VCC						-11363.5	-9048.5
U36	VCC						-12013.7	-9048.5
U37	VSS						-12663.9	-9048.5
U38	VSS						-13314.2	-9048.5
U4	DDR0_DQ[47] / DDR1_DQ[15]				DDR0_DQ[47]	DDR1_DQ[15]	11363.45	-8809.74
U5	DDR0_DQ[46] / DDR1_DQ[14]				DDR0_DQ[46]	DDR1_DQ[14]	10713.21	-8809.74
U6	VSS						10062.97	-8860.54
V1	DDR0_DQ[44] / DDR1_DQ[12]				DDR0_DQ[44]	DDR1_DQ[12]	13314.17	-8073.14
V10	DDR1_DQ[42] / DDR1_DQ[26]				DDR1_DQ[42]	DDR1_DQ[26]	7452.36	-8509.25
V11	DDR1_DQ[43] / DDR1_DQ[27]				DDR1_DQ[43]	DDR1_DQ[27]	6802.12	-8509.25
V12	VSS						6151.88	-8509.25
V13	VCC						5501.64	-8509.25
V14	VCC						4851.4	-8509.25
V2	DDR0_DQ[41] / DDR1_DQ[9]				DDR0_DQ[41]	DDR1_DQ[9]	12663.93	-8073.14
V29	VSS						-7411.21	-8261.1
V30	VSS						-8061.45	-8261.1
V31	VCC						-8762.49	-8261.1
V32	VCC						-9412.73	-8261.1
V33	VCC						-10063	-8261.1
V34	VCC						-10713.2	-8261.1
V35	VCC						-11363.5	-8261.1
V36	VCC						-12013.7	-8261.1
V37	VCC						-12663.9	-8261.1
V38	VCC						-13314.2	-8261.1
V4	DDR0_DQ[45] / DDR1_DQ[13]				DDR0_DQ[45]	DDR1_DQ[13]	11363.45	-8073.14
V5	DDR0_DQ[40] / DDR1_DQ[8]				DDR0_DQ[40]	DDR1_DQ[8]	10713.21	-8073.14
V6	VSS						10062.97	-8022.34
V7	DDR1_DQ[46] / DDR1_DQ[30]				DDR1_DQ[46]	DDR1_DQ[30]	9403.08	-8509.25
V8	DDR1_DQ[47] / DDR1_DQ[31]				DDR1_DQ[47]	DDR1_DQ[31]	8752.84	-8509.25
V9	DDR1_DQSP[5] / DDR1_DQSP[3]				DDR1_DQSP[5]	DDR1_DQSP[3]	8102.6	-8509.25
W1	VSS						13314.17	-7184.14
W10	DDR1_DQ[45] / DDR1_DQ[29]				DDR1_DQ[45]	DDR1_DQ[29]	7452.36	-7594.85

Table 9-1. Processor Ball List (Sheet 40 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
W11	DDR1_DQ[44] / DDR1_DQ[28]				DDR1_DQ[44]	DDR1_DQ[28]	6802.12	-7594.85
W12	VSS						6151.88	-7594.85
W13	VCC						5501.64	-7594.85
W14	VCC						4851.4	-7594.85
W2	VSS						12663.93	-7184.14
W29	VCC						-7411.21	-7473.7
W3	VSS						12013.69	-7184.14
W30	VCC						-8061.45	-7473.7
W31	VCC						-8762.49	-7473.7
W32	VCC						-9412.73	-7473.7
W33	VSS						-10063	-7473.7
W34	VSS						-10713.2	-7473.7
W35	VCC						-11363.5	-7473.7
W36	VCC						-12013.7	-7473.7
W37	VCC						-12663.9	-7473.7
W38	VCC						-13314.2	-7473.7
W4	VSS						11363.45	-7184.14
W5	VSS						10713.21	-7184.14
W6	VDDQ						10062.97	-7184.14
W7	DDR1_DQ[41] / DDR1_DQ[25]				DDR1_DQ[41]	DDR1_DQ[25]	9403.08	-7594.85
W8	DDR1_DQ[40] / DDR1_DQ[24]				DDR1_DQ[40]	DDR1_DQ[24]	8752.84	-7594.85
W9	DDR1_DQSN[5] / DDR1_DQSN[3]				DDR1_DQSN[5]	DDR1_DQSN[3]	8102.6	-7594.85
Y10	VSS						7452.36	-6680.45
Y11	VSS						6802.12	-6680.45
Y12	VDDQC						6151.88	-6680.45
Y13	VSS						5501.64	-6680.45
Y14	VSS						4851.4	-6680.45
Y29	VCC						-7411.21	-6686.3
Y30	VCC						-8061.45	-6686.3
Y31	VCC						-8762.49	-6686.3
Y32	VCC						-9412.73	-6686.3
Y33	VCC						-10063	-6686.3
Y34	VCC						-10713.2	-6686.3
Y35	VCC						-11363.5	-6686.3
Y36	VCC						-12013.7	-6686.3
Y37	VSS						-12663.9	-6686.3
Y38	VSS						-13314.2	-6686.3

Table 9-1. Processor Ball List (Sheet 41 of 41)

Ball #	Ball Name	DDR3	LPDDR3	DDR4	Interleaved (IL)	Non-interleaved (NIL)	PIN_X (um)	PIN_Y (um)
Y7	VSS						9403.08	-6680.45
Y8	VSS						8752.84	-6680.45
Y9	VSS						8102.6	-6680.45

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