Intel® Agilex™ F-Series Transceiver-SoC Development Kit User Guide

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1. Overview

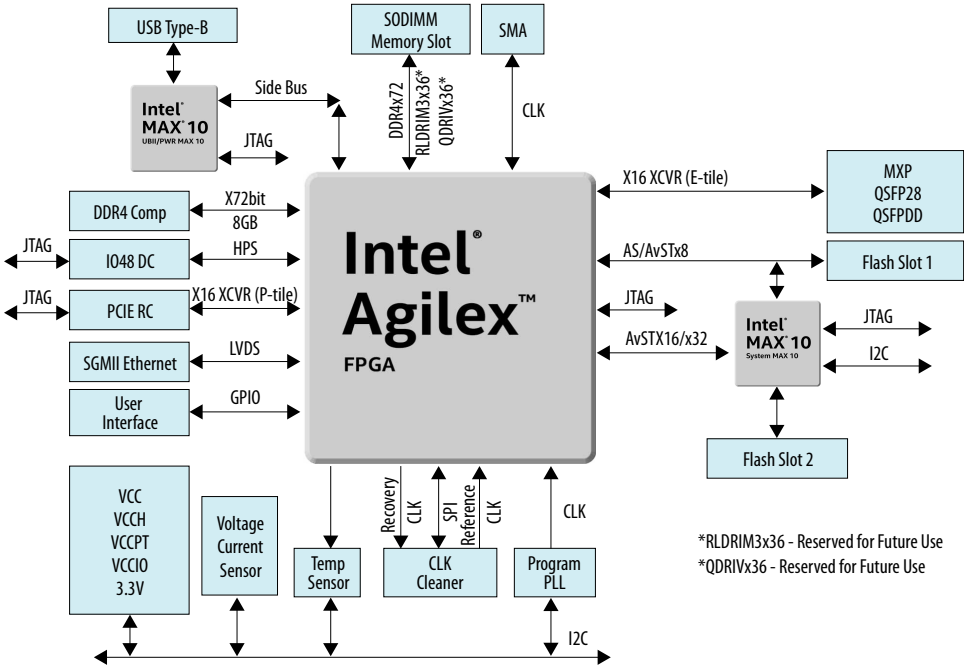
Intel® Agilex™ F-Series Transceiver-SoC Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Agilex F-Series FPGA designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Intel Agilex F-Series Transceiver-SoC designs.

Table 1. Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Intel Agilex F-Series Transceiver-SoC Development Kit (ES)	DK-SI-AGF014E3ES	AGFB014R24A2E3VR0	Under 500
Intel Agilex F-Series Transceiver-SoC Development Kit (Production)	DK-SI-AGF014EA	AGFB014R24B2E2V	Above 1000

1.1. Block Diagram

Figure 1. Intel Agilex F-Series Transceiver-SoC Development Kit Block Diagram



1.2. Feature Summary

- Intel Agilex F-Series FPGA, 1400 KLE, 2486A package
- 16 E-tile transceiver channels fan out to Multi-Speed Port (MXP), Quad Small Form Factor Double Density (QSFPDD) and Quad Small Form-Factor Pluggable 28 (QSFP28) interfaces
- 16 P-tile channels fan out to PCIe Root complex interface which can run up to Gen4 depending on FPGA core fabric speed grade
- 8 GB Double Data Rate 4 (DDR4) component interface for either FPGA fabric or HPS
- Small Outline Dual In-line Memory Module (SODIMM) interface for single-rank DDR4 and customized QDRIV/RLDRAM3 modules
- IO48 interface for HPS OOBE (Out of Box Experience) and NAND daughter cards
- Flash slot 1 interface for Queued Serial Peripheral Interface (QSPI) and Secure Digital and MultiMediaCard (SDMMC) flash daughter cards (AS and SD/MMC configuration modes)
- Flash slot 2 interface for QSPI and CFI NOR flash daughter cards (AvST configuration mode)
- Dual-channel network synchronizer clock circuit for both Synchronous Ethernet and IEEE 1588

1.3. Box Contents

- Intel Agilex F-Series Transceiver-SoC Development Kit
- Single-rank DDR4 SODIMM module
- QSPI flash daughter card with GHRD design pre-programmed
- HPS IO48 OOBE and NAND daughter cards
- USB2.0 Type B cable
- Ethernet cable
- 240W power adapter and NA/EU/JP/UK cords
- ATX power convert cable - 24 pin to 6 pin

1.4. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range of Values
Ambient operating temperature range	0 °C to 45 °C
ICC load current	100 A
ICC load transient percentage	200 A/µs
FPGA maximum power supported by active heatsink/fan	120 W

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the development kit.

Caution: This development kit should not be operated in a vibration environment.

2. Getting Started

2.1. Intel Quartus® Prime Software and Driver Installation

Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs. Intel Quartus Prime Pro Edition software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Intel Agilex, Intel Stratix® 10, Intel Arria® 10 and Intel Cyclone® 10 GX device families.

Intel Agilex F-Series Transceiver-SoC Development Kit includes on-board Intel FPGA Download Cable circuits for FPGA and system Intel MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer. Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

The Intel SoC EDS is a comprehensive software tool suite for embedded software development on Intel SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm* Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Intel's SoC FPGAs.

For more information and steps to install the Intel SoC EDS Tool Suite refer to the links below.

Related Information

- Quick-Start for Intel Quartus Prime Pro Edition Software
- Intel Quartus Prime Pro Edition User Guide: Getting Started
- Arm DS-5 Intel SoC FPGA Edition Toolkit
- Intel SoC FPGA Embedded Development Suite User Guide

2.2. Quick Start Guide

Refer to the *Intel Agilex F-Series Development Kit Quick Start Guide* to learn how the development kit works by default after power up.

2.3. Design Examples

Unzip the install package which includes board design files, documents and examples directories. The table below lists the file directory names and a description of their contents.

Table 3. Installed Development Kit Directory Structure

Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
`documents`	Contains the development kit documentation – quick start guides and user guide
`examples`	Contains: • The original data programmed into flash and system Intel MAX 10 before shipment. Use this data to restore the board with its original factory contents. • QSPI image, system Intel MAX 10 image • Board Test System (BTS), clock and power GUI • Design Examples: Configuration, Golden Top, XCVR, EMIF, Ethernet, System Intel MAX 10

3. Power Up the Development Kit

The instructions in this chapter explain how to setup the Intel Agilex F-Series Transceiver-SoC Development Kit for specific use cases.

3.1. Default Settings

The Intel Agilex F-Series Transceiver-SoC Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table to return to its factory settings before proceeding ahead.

Note: X refers to Don't Care in the table below.

Table 4. Factory Default Switch Settings

Switch	Default Position	Default Function
SW1 [1:4]	ON/OFF/OFF/X	Configuration mode setting bits AS - Normal mode
SW2 [1:8]	X/X/X/X/X/X/X/X	FPGA user dipswitch
SW3 [1:8]	OFF/OFF/X/X/ON/ON/ON/ON	6:8 - JTAG chain setting bits FPGA SDM and HPS are chained internally 1:5 - JTAG slave node bypass control FPGA SDM/HPS and system Intel MAX 10 are in JTAG chain PCIe is bypassed
SW4 [1:4]	X/OFF/OFF/OFF	UB2/PWR Intel MAX 10 Pin Strap Settings 2 - VCCFUSEWR_SDM_FPGA_2.4V rail is set to 1.8 V 3 - Regulator U60 drive VCCL_HPS_FPGA_0.9V rail. Turn off U60 by this dipswitch bit as this rail source from VCC_FPGA_VID 4 - LMK05028 is active by default
SW5 [1:4]	OFF/OFF/X/X	System Intel MAX 10 Pin Strap Settings 1 - Factory Load = 0 2 - Si549 instead of SMA connectors supply clock to Si53311
SW6 [1:4]	OFF/OFF/OFF/X	FPGA core regulators' I^2C bus chain settings

continued...

Switch	Default Position	Default Function
		1:3 - Core regulators' I^2C Bus is isolated from main I^2C bus
SW8	OFF	Power slide switch
SW10 [1:2]	OFF/ON	System Intel MAX 10 Pin Strap Settings 1 - I2C_3.3V_EN is high by default 2 - CLKCleaner_IO_TSn is low

3.2. Power Up

To power up the development kit:

1. Use the provided 240 W power adapter to supply power through **J37**. If your application consumes more than 240 W, for example supply power for PCIe add-in card, a more powerful ATX power module plus the provided 24 pin to 6 pin convert cable is recommended for use.
2. After power adapter is plugged into **J37** and **SW8** is set to the **ON** position, two green LEDs (**D19** and **D20**) illuminate and one red LED (**D23**) extinguishes indicating that the board power up successfully. If the red LED (**D23**) illuminates, it indicates that one or more power supply is incorrect.

3.3. Perform board restore

This development kit ships with GHRD design examples stored in the QSPI flash device and system Intel MAX 10 pre-programmed. You must perform board restore by using the restore menu under BTS GUI, or using below instructions through Intel Quartus Prime Programmer GUI.

3.3.1. Restore board System Intel MAX 10 with default factory image

1. Open Intel Quartus Prime Programmer GUI, detect JTAG chain after System Intel MAX 10 is restored.
2. Attach System Intel MAX 10 image on System Intel MAX 10 part.
3. Select programming options and click program button.

   Note: Once you plug Intel FPGA Download Cable between **J19** and **PC**, the Intel on-board download cable circuit is disabled automatically.

3.3.2. Restore board QSPI flash with the default factory image

1. Plug QSPI flash card into J11 slot, ensure MSEL[2:0] are OFF (AvSTx32) mode before power up the board.
2. Open Intel Quartus Prime Programmer GUI, detect JTAG chain after System Intel MAX 10 is restored.
3. Attached AvSTx32 image (BTS/image/ES/QSPI folder) on QSPI flash which is under System Intel MAX 10 part.
4. Select programming options and click program button.

Note: QSPI flash is pre-programmed with GHRD image. It is overwritten by AvSTx32 image after above steps. Refer to https://rocketboards.org/ to recover and update GHRD image on QSPI flash.

3.4. Control on-board clock through Clock Controller GUI

The Clock Controller GUI application can change on-board Si549 programmable oscillators to any customized frequency between 0.2 MHz and 800 MHz. The default clock frequency value is 156.25MHz. It can also change both Si5338K programmable PLLs to any frequency between 0.17 MHz and 710 MHz.

To change LMK05028 input/output frequency plan, you should:

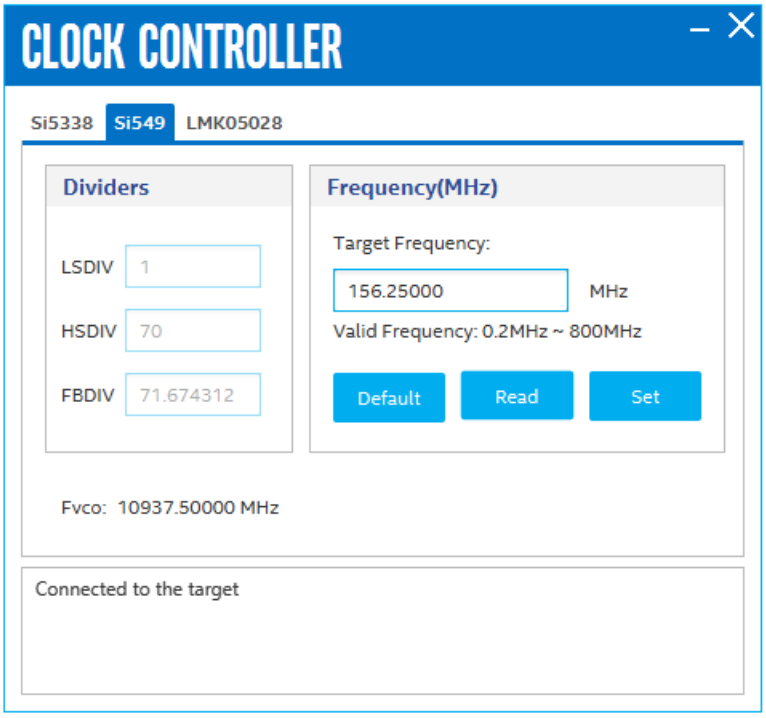
1. Connect J51.2 to J26.19, J51.1 to J26.17 by duban wires, connect J26.12 to J26.11 by jumper. This set LMK05028 work at I^2C mode and put it into I^2C chain. Ensure **SW10.2** is set to ON and SW4.4 is set to OFF.
2. Generate the register file by using TICS Pro tools and MATLAB Runtime v9.0 (2015b, 64-bit).
3. Import generated register file into on-board chip through Clock Controller GUI.

The Clock Controller GUI application (`ClockControl.exe`) runs as a stand-alone application and resides in the `<package dir>\examples\board_test_system` directory.

The Clock Controller GUI communicates with the system Intel MAX 10 device through either USB port **CN1** or 10-pin JTAG header **J19**. Then system Intel MAX 10 controls these programmable clock parts through a 2-wire serial bus.

Attention: You cannot run the stand-alone Clock Controller GUI application when the Board Test System (BTS) or Power Monitor GUI is running at the same time.

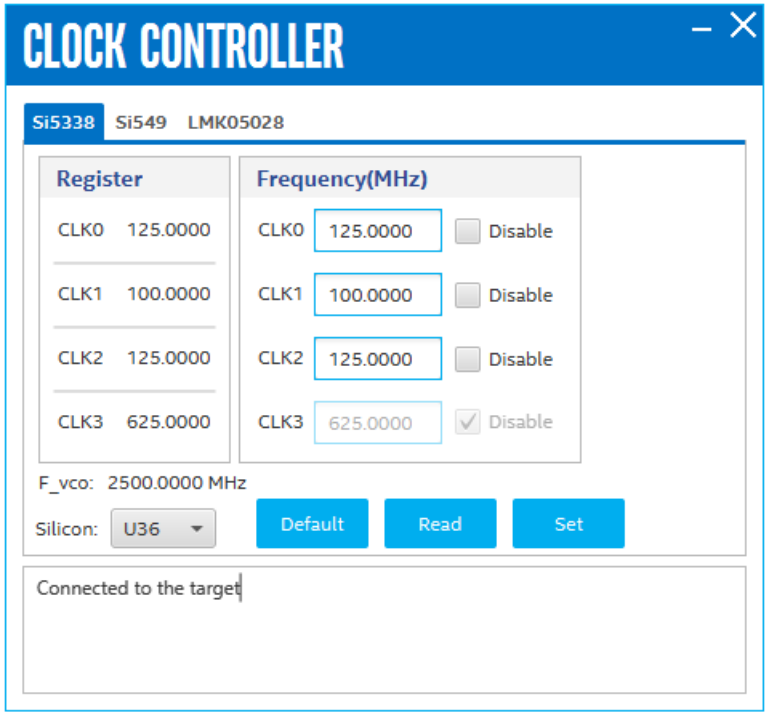
Figure 2. Clock Controller GUI - Si549



Note:

- LSDIV: Low Speed Output Divider
- HSDIV: High Speed Output Divider
- FBDIV: DSPLL™ Feedback Divider used to set Digital VCO Frequency

Figure 3. Clock Controller GUI - Si5338K



The following sections describe the Clock Controller GUI buttons.

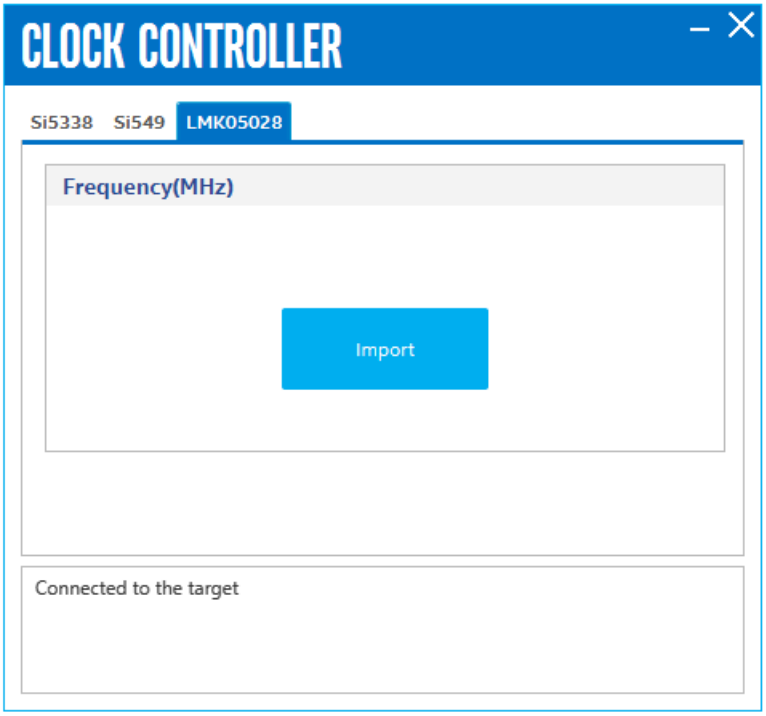
Read: Reads the current frequency setting for the oscillator associated with the active tab.

Default: Sets the frequency for the oscillator associated with the active tab back to its default value. You can also return to the default frequencies by power cycling the board.

Set: Sets the programmable oscillator frequency for the selected clock to the value in the CLKx output controls for the Si5338. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

Import: Import the register file which is generated for new input/output frequency plan into the on-board LMK05028. Register changes are volatile after power recycle.

Figure 4. Clock Controller GUI - LMK05028



3.5. Control on-board power regulator through Power Monitor GUI

The Power Monitor GUI reports most power rails voltage, current, and power information on the board. You can fine-tune some regulators' output voltage by Power Monitor GUI. It also collects temperature from FPGA SDM, FPGA core, E-Tile, P-tile, power modules and diode assembled on PCB.

The Power Monitor GUI communicates with system Intel MAX 10 through either USB port **CN1** or **J19**. System Intel MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire serial bus.

The Power Monitor GUI applications (`PowerMonitor.exe`) runs as a stand-alone application and resides in the `<package dir>\examples\board_test_system` directory.

Attention: You cannot run the stand-alone power application when BTS or Clock Controller GUI is running at the same time.

Power Monitor GUI-1

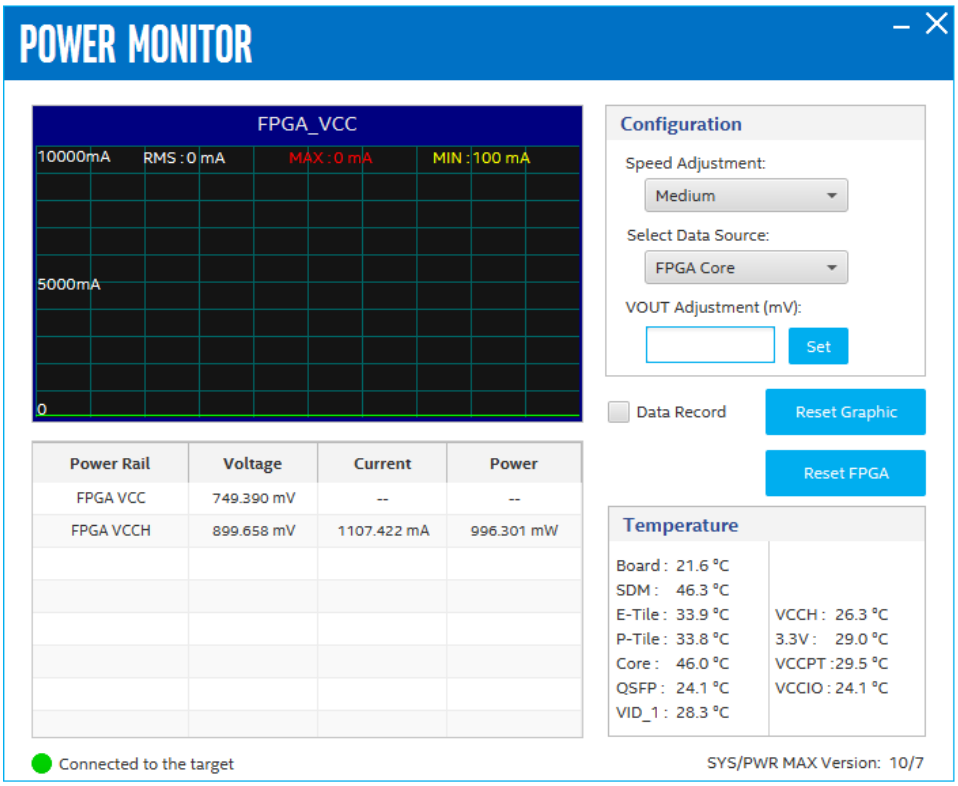


Figure 5. Power Monitor GUI-2

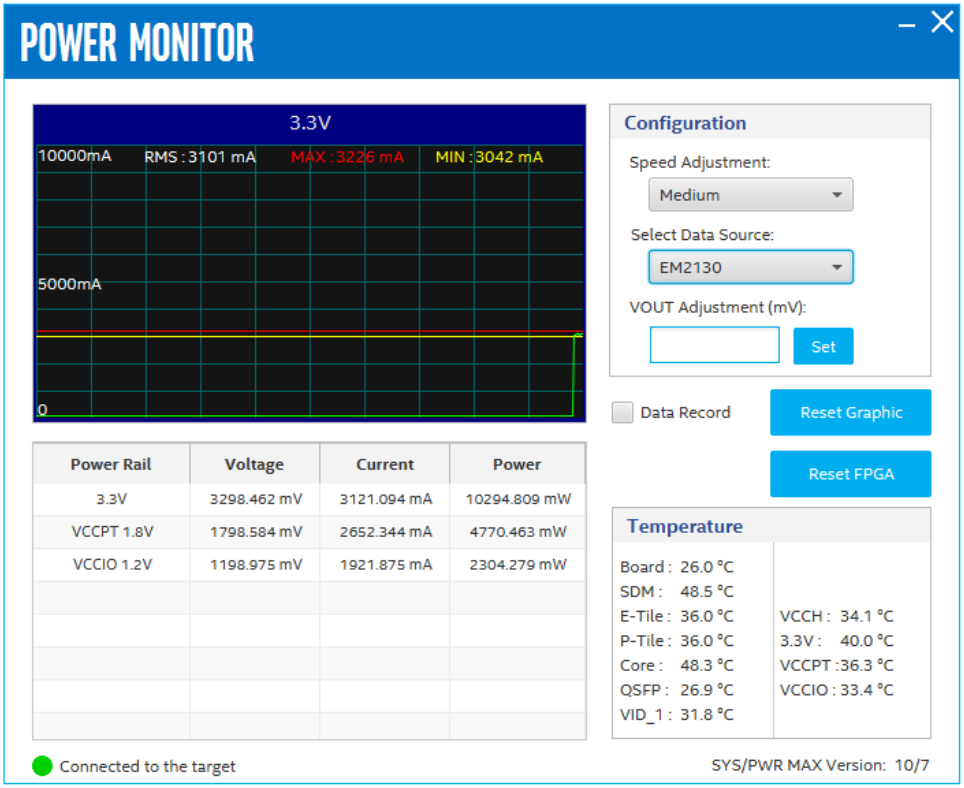


Figure 6. Power Monitor GUI-3

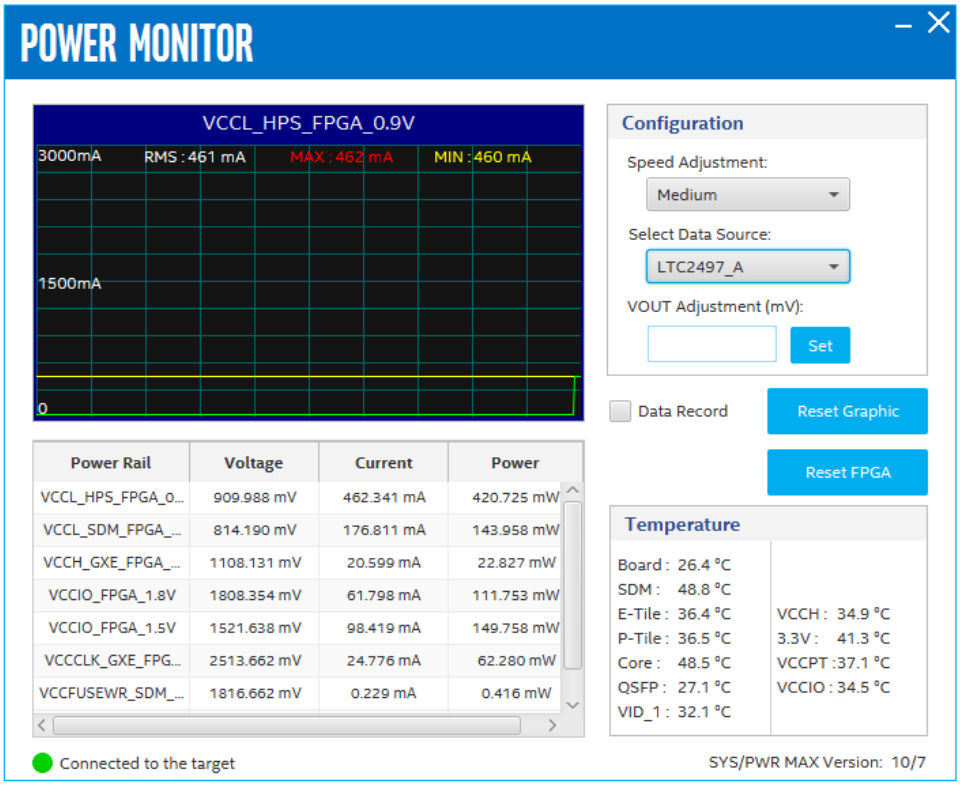
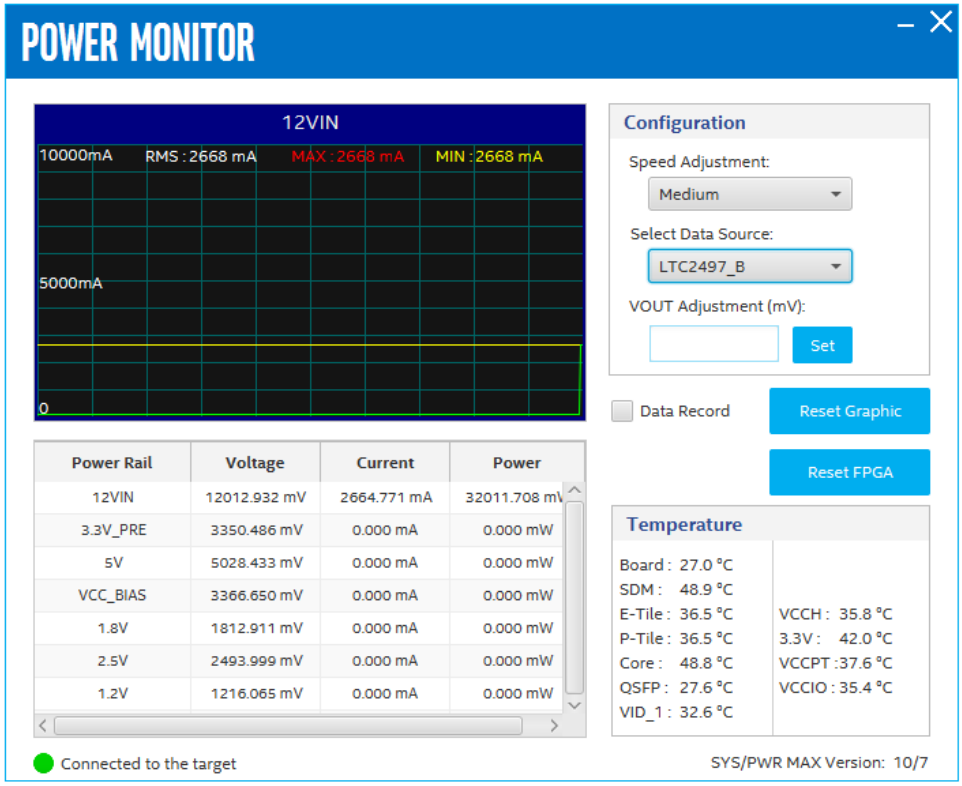


Figure 7. Power Monitor GUI-4



Configuration

Speed Adjustment: Adjust the update rate of current curve

Select Data Source: Switch between different monitor targets

Vout Adjustment (mV): Fine tune each smart regulator module output within +/-7% range.

Temperature

Board: PCB surface temperature near U31

SDM/E-tile/P-tile/Core: FPGA die internal temperature sense diode (TSD)

QSFP: Diode assembled on PCB and close to QSFP/QSFPDD modules

VID_1/VCCH/3.3V/VCCPT/VCCIO: regulator U54/U57/U53/U58/U59 internal TSD. No on-board current measurement circuit for 3.3V_PRE, 5V, VCC_BIAS, 1.8V, 2.5V and 1.2V

4. Board Test System

The Intel Agilex F-Series Transceiver-SoC Development Kit includes several design examples and an application called the Board Test System (BTS) to test the functionality of this board.

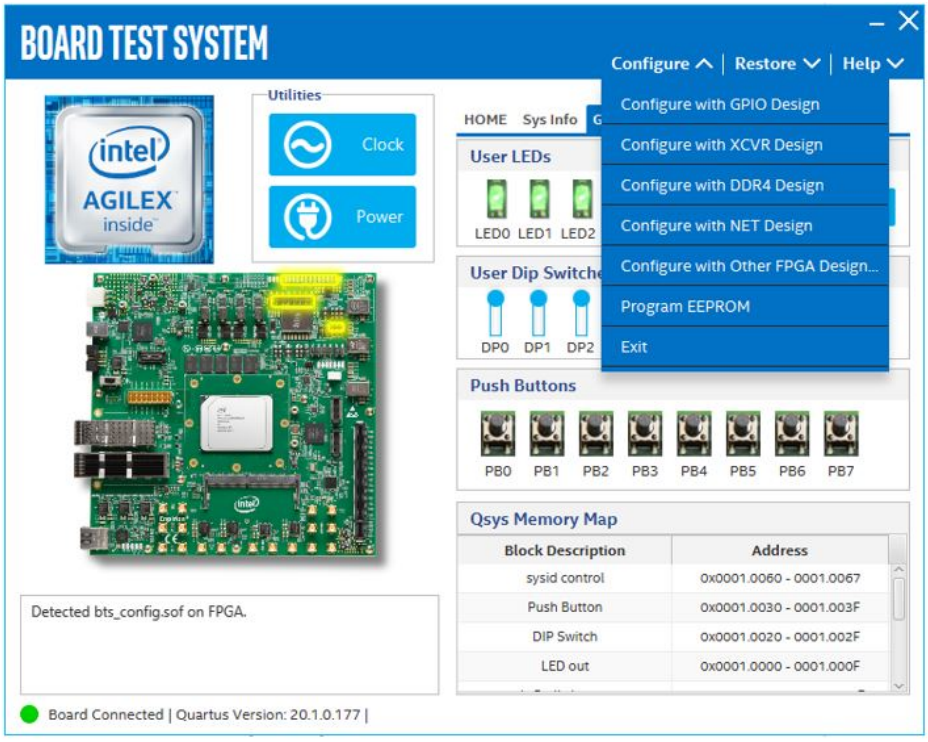
4.1. Test the functionality of the Development Kits

This section describes each control in the Board Test System (BTS).

4.1.1. The Configure Menu

Use the **Configure** Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 8. The Configure Menu



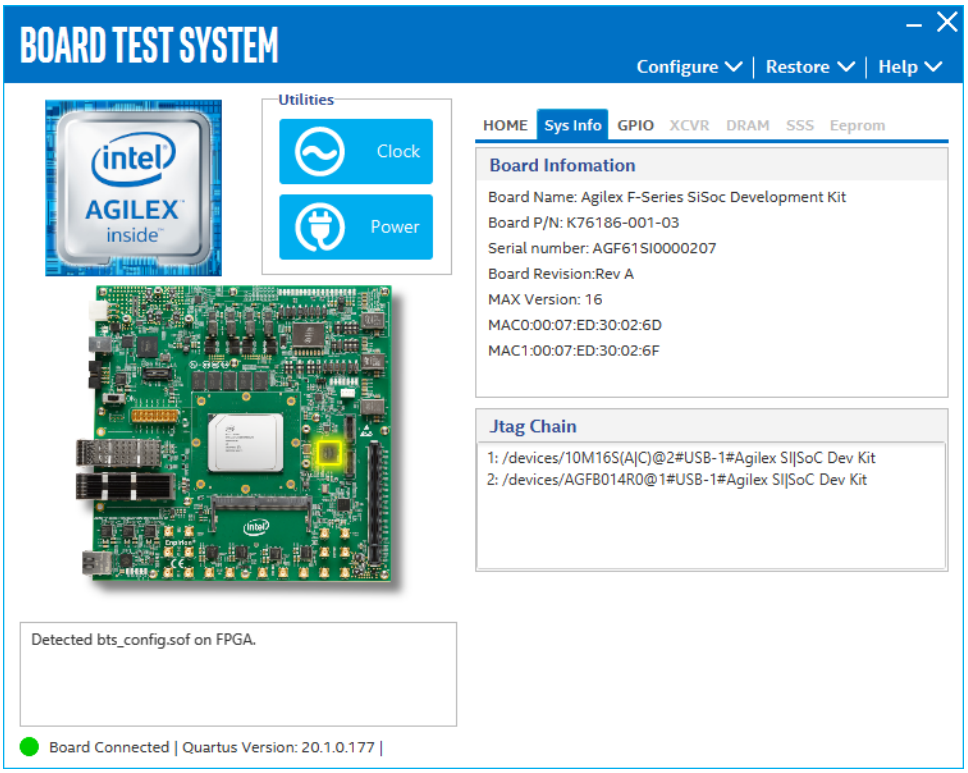
To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure Menu**, click the **Configure** command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the BTS GUI.

4.1.2. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays system Intel MAX 10 control setting, the board's MAC address, and other details stored on the board.

Figure 9. The Sys Info Tab



The following sections describe the controls on the Sys Info tab.

Board Information

The Board Information control displays static information about your board.

- **Board Name:** Indicates the official name of the board given by the BTS.
- **Board P/N:** Indicates the part number of the board.
- **Serial Number:** Indicates the serial number of the board.
- **Board Revision:** Indicates the revision of the board.
- **MAX Version:** Indicates the version of the System Max
- **MAC:** Indicates the MAC address of the board.

JTAG Chain

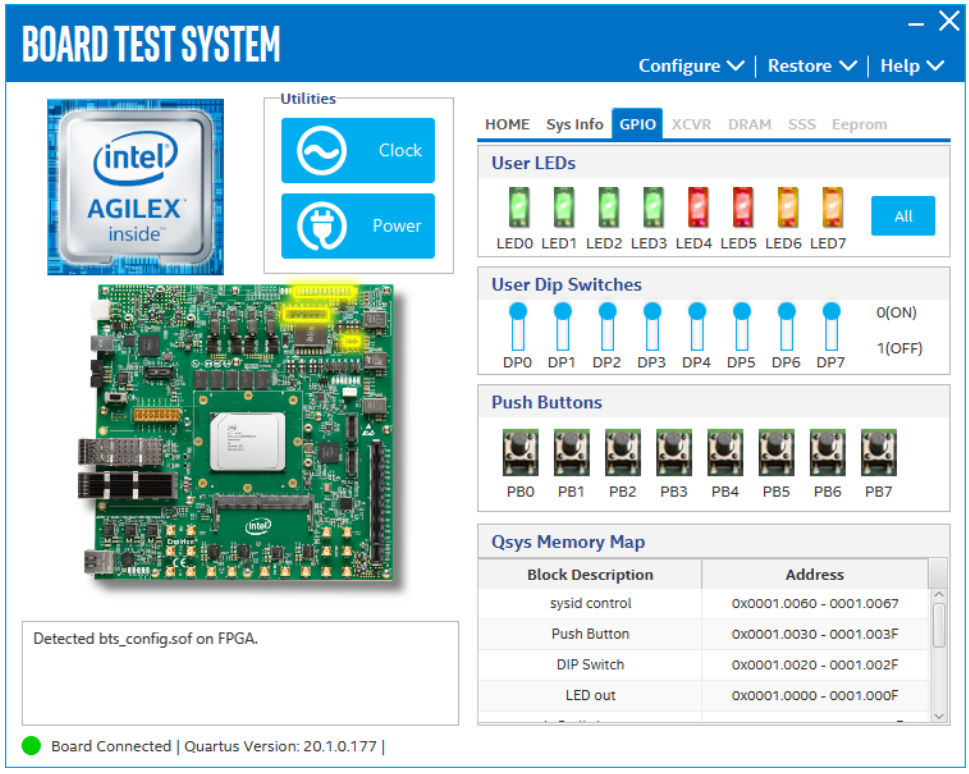
The JTAG chain control shows all the devices currently in the JTAG chain.

Note: When switch **SW3-2 (MAX BYPASS)** is set to **1**, the JTAG chain includes the Intel MAX 10 device. When set to **0**, the Intel MAX 10 device is removed from the JTAG chain. System Intel MAX 10 and FPGA should be placed in the JTAG chain when running the BTS GUI.

4.1.3. The GPIO Tab

The **GPIO** Tab allows you to interact with all the general purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off and detect push button presses.

Figure 10. The GPIO Tab



The following sections describe the controls on the GPIO tab.

User DIP Switches

The read-only User DIP switches control displays the current positions of the switches in the user DIP switch bank **(SW2)**. Change the switches on the board to see the graphical display change.

User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

Push Buttons

The Push Buttons control displays the current state of the push buttons on the board. Toggle the push buttons to turn them on or off.

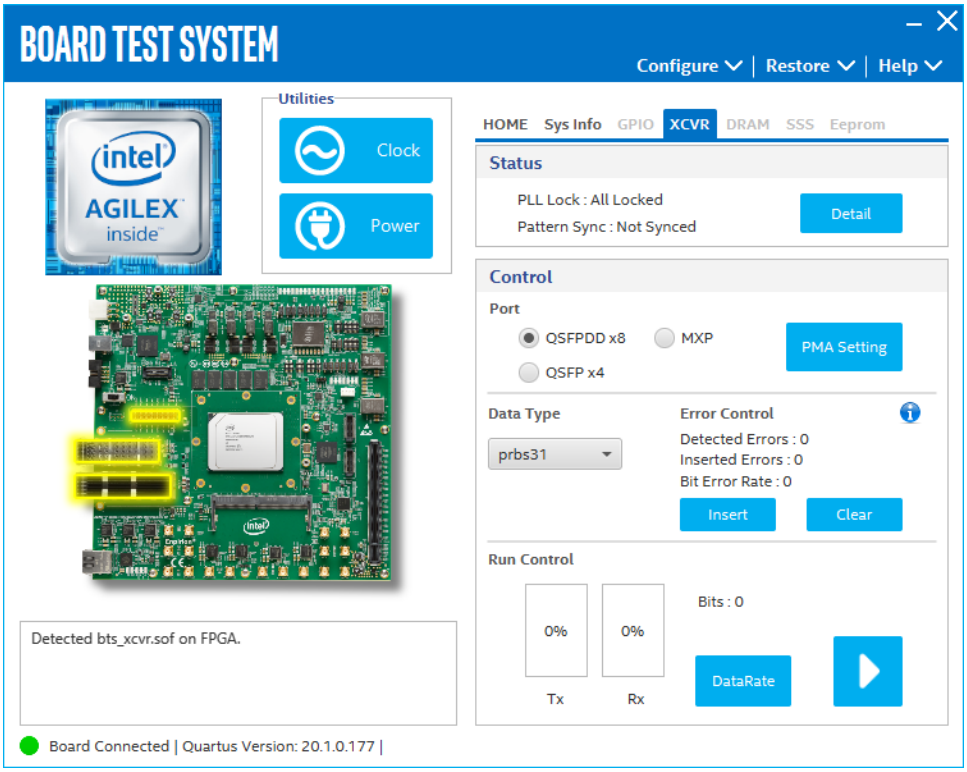
Platform Designer Memory Map

The Platform Designer memory map control shows the memory map of **bts_config.sof** design running on your board. This can be visible when **bts_config.sof** design is running on board.

4.1.4. The XCVR Tab

The **XCVR** Tab allows you to run transceivers QSFPDDx8, QSFPx4 and MXP loopback tests on your board. You can run the test using either electrical loopback modules or optical fiber modules. Plug QSFPDD loopback module in **U12**, plug QSFP loopback module in **J12**, plug MXP loopback cable in **J13** before download transceiver design through BTS GUI. The PRBS traffic is 30 Gbps.

Figure 11. The XCVR Tab



The following sections describe the XCVR tab.

Status

The Status control displays the following status information during the loopback test:

- **PLL lock:** Shows the PLL locked or unlocked state
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status.

Control

Use the following controls to select an interface to apply PMA settings, data type and error control:

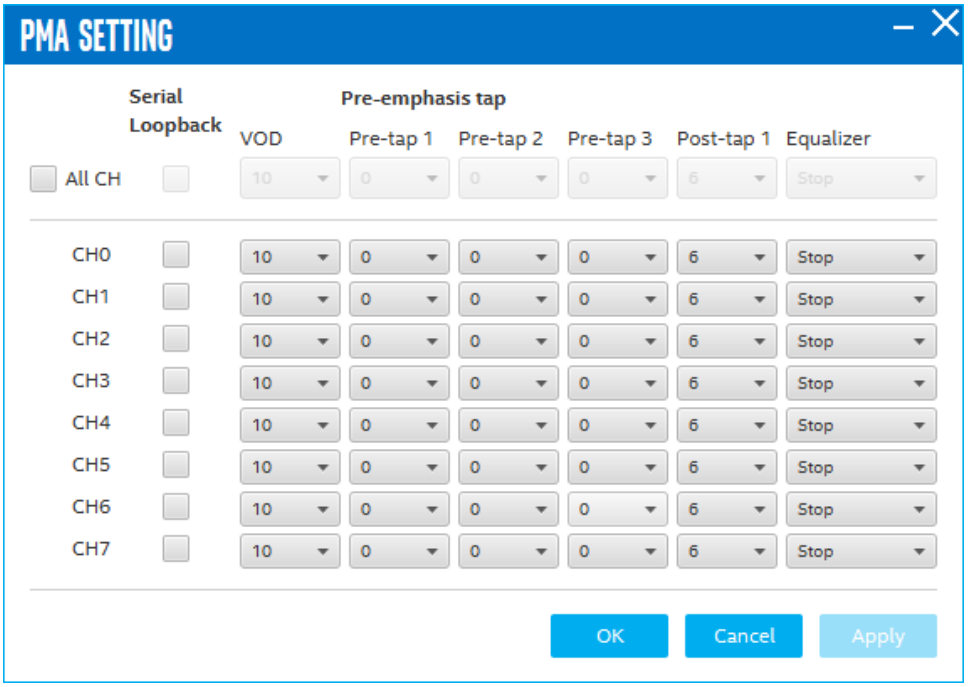
- **QSFPDD x8**
- **QSFP x4**
- **MXP**

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- Equalizer: Specifies the RX tuning mode for receiver equalizer.

Figure 12. XCVR-PMA Setting



Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7:** pseudo-random 7-bit sequences
- **PRBS15:** pseudo-random 15-bit sequences
- **PRBS23:** pseudo-random 23-bit sequences
- **PRBS31:** pseudo-random 31-bit sequences (default)

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the received bit stream.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- **Insert:** Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

Run Control

- **TX and RX performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Start:** This control initiates the loopback tests.
- **Data Rate:** Displays the XCVR type and data rate of each channel.

Figure 13. XCVR- Data Rate

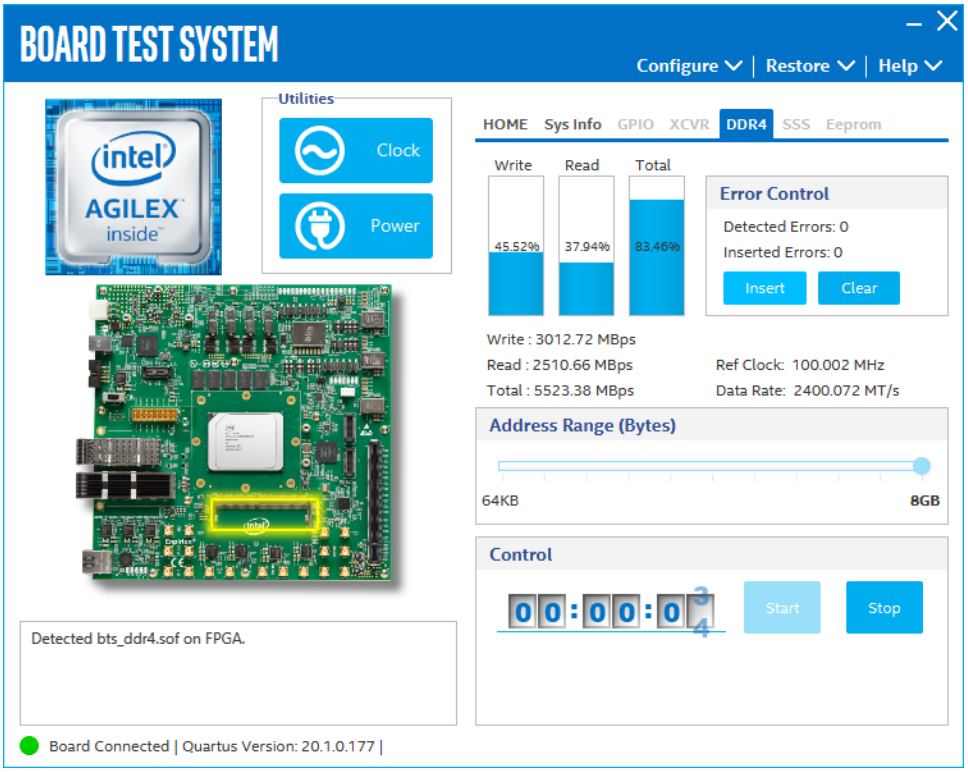
Data Rate

Channel	XCVR Type	Frequency
0	GXE	25000.06 Mbps
1	GXE	25000.06 Mbps
2	GXE	25000.06 Mbps
3	GXE	25000.06 Mbps
4	GXE	25000.06 Mbps
5	GXE	25000.06 Mbps
6	GXE	24999.94 Mbps
7	GXE	25000.06 Mbps

4.1.5. The DDR4 Tab

The **DDR4** tab allows you to read and write DDR4 memory on your board. Plug the DDR4 SODIMM module to single socket **CON1**, then download EMIF designs through BTS.

Figure 14. The DDR4 Tab



The following sections describe the controls on the DDR4 tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits(8 bits ECC) wide, reference clock is 100 MHz and the frequency is 1200 MHz double data rate 2400 MT/s.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zeroes.

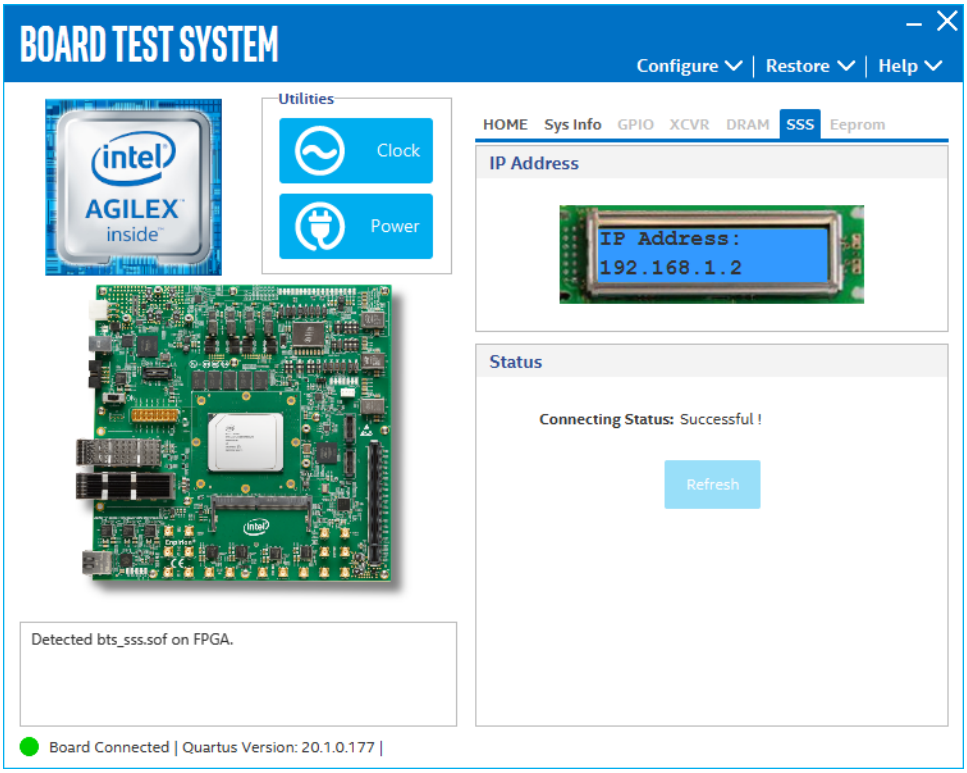
Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

4.1.6. The SSS Tab

The **SSS** tab is for the Simple Socket Server application, shows you the IP address, and allows you to reboot the Nios® II. Connect a router with this development kit's **RJ45** port by the ethernet cable. Make sure DHCP is enabled in router. Download Ethernet SSS design through BTS GUI and check LED status.

Figure 15. The SSS Tab



The following sections describe the controls on the SSS tab.

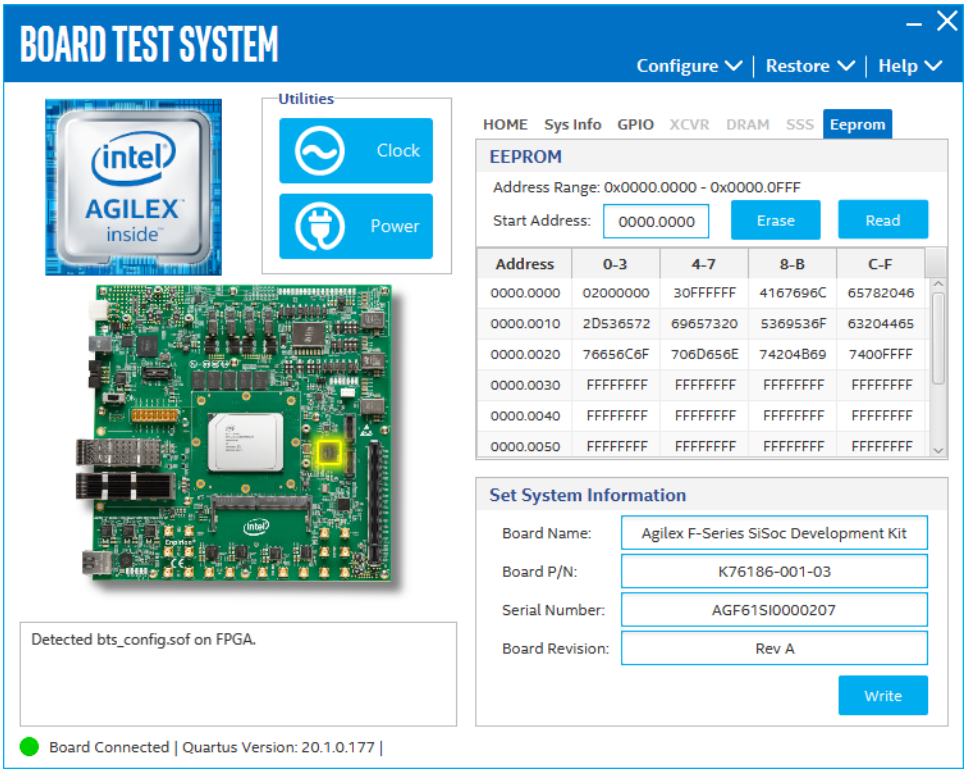
Refresh

Performs a Nios II reboot, accordingly the IP address will be refreshed.

4.1.7. The EEPROM Tab

The EEPROM Tab allows you to read and write EEPROM on your board.

Figure 16. The EEPROM Tab



The following sections describe the controls on the EEPROM tab.

Read

The Read control reads the EEPROM on your board.

To see the EEPROM contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table.

To see flash memory contents, type the address above the base and values starting at this address are displayed. Valid entries are `0x0000.0000` through `0x0000.0FFF`.

Erase

The Erase control erases the EEPROM content, size is `0x18C`.

Write

The Write control writes system information to EEPROM.

5. Development Kit Hardware and Configuration

The Intel Agilex F-Series Transceiver-SoC Development Kit can support multiple application scenarios and configuration modes. You need to change hardware setting and/or re-program system images for these cases.

Table 5. Supported Configuration Modes

SW1 [1:4]	MSEL [2:0]	Configuration Mode
ON/OFF/OFF/X	001	AS – Fast mode (Default setting)
ON/ON/OFF/X	011	AS – Normal mode
ON/ON/ON/X	111	JTAG
OFF/ON/ON/X	110	AvSTx8
ON/OFF/ON/X	101	AvSTx16
OFF/OFF/OFF/X	000	AvSTx32

5.1. Configure FPGA and access HPS Debug Access Port by JTAG

1. JTAG access does not rely on **SW1** settings and system image.
2. Plug the USB cable to **CN1** or Intel FPGA Download Cable to **J19**.
3. Open Intel Quartus Prime Programmer, system console to configuration Intel Agilex FPGA SDM, system Intel MAX 10 and PCIe JTAG nodes.
4. Open Arm Development Studio 5* (DS-5*) Intel SoC FPGA Edition to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

   Note: By default, HPS and FPGA SDM JTAG nodes are chained together internally. **SW3.1** bypasses or enables both nodes at the same time. OOBE's Mictor 38-pin header cannot access HPS DAP function.

5.2. Configure the FPGA device by AS modes (Default Mode)

1. Default **SW1** setting and system Intel MAX 10 image support AS configuration mode.
2. Plug pre-programmed SDM QSPI flash daughter into **J10**.
3. Power on and observe FPGA user LED behavior.

5.3. Configure the FPGA device by AvST modes

1. Set SW1 to AvST x32 mode first.
2. Plug SDM QSPI flash daughter into **J11**.
3. Default system Intel MAX 10 image support AvST x32 mode only. You should build a corresponding .POF image if you select AvST x8 or AvST x16 configuration mode.
4. Detect QSPI flash in Programmer and program QSPI flash with factory provided AvST x32 test image file. Power cycle the board, use push button **S17** to choose page, and **S18** to configure FPGA. LED_D27, LED_28, LED_29 are used to indicate the active page.

Table 6. AvST x32 LED Behavior

LED	Page0 (XCVR)	Page1 (DDR4)	Page2 (SSS)	Page3 (GPIO)
LED_D27	ON	OFF	OFF	OFF
LED_D28	OFF	ON	OFF	ON
LED_D29	OFF	OFF	ON	ON
FPGA_LED_G[0]	Blinking	Blinking	OFF/Blinking	ON
FPGA_LED_G[1]	ON	OFF	OFF/Blinking	ON
FPGA_LED_G[2]	ON	ON	OFF/Blinking	ON
FPGA_LED_G[3]	ON	OFF	Blinking	ON
FPGA_LED_G[4]	OFF	OFF	OFF	ON
FPGA_LED_G[5]	OFF	OFF	OFF	ON
FPGA_LED_G[6]	OFF	OFF	OFF	ON
FPGA_LED_G[7]	OFF	OFF	OFF	ON

5.4. Daughter Cards

The Intel Agilex F-Series Transceiver-SoC Development Kit also supports HPS OOBE/NAND daughter cards. You can demonstrate HPS functions through these daughter cards and cables.

5.4.1. HPS Out of Box Experience (OOBE) Daughter Card

1. Plug HPS OOBE Daughter Card in **J5**
2. To test HPS Ethernet capability, connect OOBE's **RJ45** port **J3** to Internet
3. To test HPS USB2.0 capability, connect OOBE's **J4** port to USB cable
4. To debug HPS from UART terminal applications, use USB cable to connect to OOBE's **J7**
5. OOBE's MicroSD card is pre-programmed with GSRD and OS
6. General I/O access is provided by push buttons and LED indicators

5.4.2. HPS NAND Daughter Card

1. Plug HPS NAND daughter card in **J5**
2. To test HPS Ethernet capability, connect OOBE's **RJ45** port **J3** to Internet
3. To test HPS from UART terminal apps, use USB cable connect to OOBE's **J7**
4. OOBE's NAND flash or eMMC flash are pre-programmed with GSRD and OS
5. Access HPS I^2C bus by **J2** header
6. General I/O access from push buttons and LED indicators

6. Custom Projects for the Development Kit

6.1. Add SmartVID settings in Intel Quartus Prime QSF file

Intel Agilex silicon assembled on this development kit enables SmartVID feature by default. In order to avoid a Intel Quartus Prime from generating an error due to incomplete SmartVID settings, you must put constraints outlined below constraints into Intel Quartus Prime project QSF file. These constraints are designed for Intel Enpirion® ED8401 core circuit.

Open your Intel Quartus Prime project QSF file, copy and paste constraint scripts into the file. Ensure that there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 42
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS 00

set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"

set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-13"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

6.2. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, define I/O standard, direction and general termination. DDR4 pin termination settings are not included. Refer DDR4 example designs for details.

7. Revision History

Table 7. Revision History for the Intel Agilex F-Series Transceiver-SoC Development Kit User Guide

Document Version	Changes
2021.07.27	Corrected Device Part Number for Intel Agilex F-Series Transceiver-SoC Development Kit (Production) in Table: *Ordering Information*.
2021.06.15	• Added Table: *Ordering Information*. • Updated Figure: *Power Tree*. • Removed SW9[1:2] switch from Table: *Factory Default Switch Settings*.
2021.03.17	Updated Control on-board clock through Clock Controller GUI on page 11
2020.07.09	Board Test System (BTS) information added
2020.05.01	Engineering Silicon (ES) Release
2019.09.30	Initial Release

A. Development Kit Components

A.1. System Management

Two Intel MAX 10 FPGAs (10M16SCU324C8G) are used for system management. System Intel MAX 10 acts as system controller. It handles FPGA AvST configuration, I^2C bus access, fan speed control and system reset functions. The UB2/PWR Intel MAX 10 acts as Power manager and on-board JTAG controller. Refer to below description for each function:

- **Power management:** control systems and FPGA power up and optional down sequence, supervise power regulators/switches status and manage power faults, supervise temperature ADC interrupt signals and manage temperature faults.
- **JTAG controller:** Manage JTAG chain topology, JTAG master source and JTAG slaves by SW3

Table 8. JTAG Master Sources

Schematic Signal Name	Description
EXT_JTAG_TCK/TDO/TMS/TDI	JTAG header J19 for Intel download cable
FX2_Dp/n	input port CN1 for on-board Intel download circuit
HPS_GPIO[32:35]	Mictor 38pin header on OOBE daughter card

Intel Agilex HPS JTAG slave can be accessed from either SDM dedicated JTAG pins or HPS dedicated I/Os. When it is accessed from SDM JTAG pins (FPGA_JTAG_TCK/TDO/TMS/TDI), SDM is chained with HPS inside FPGA part. When it is accessed from HPS dedicated I/Os (HPS_GPIO[32:35]), HPS is chained externally by PCB traces.

Table 9. JTAG Chain Topology Settings

Mode	SW3 [8:6]	SW3 [5] [2] [1] ON: Bypass from chain OFF: Enable in chain	Function
000	ON/ON/ON (Default)	SW3.1 (SDM+HPS) SW3.2 (SysMAX) SW3.5 (PCIe)	Mode 1: On-board Intel download circuit act as the only JTAG Master Chained HPS with SDM nodes **internally** Mode 3: External Intel download cable act as the only JTAG Master

continued...

Mode	SW3 [8:6]	SW3 [5] [2] [1] ON: Bypass from chain OFF: Enable in chain	Function
			Chained HPS with SDM nodes **internally**
001	ON/ON/OFF	SDM is always enabled in the JTAG chain SW3.1 (HPS) SW3.2 (SysMAX) SW3.5 (PCIe)	Mode 2: On-board Intel download circuit act as the only JTAG Master Chained HPS with SDM nodes **externally** Mode 4: External Intel download cable act as the only JTAG Master Chained HPS with SDM node **externally**
100	OFF/ON/ON	SW3.1 (SDM) SW3.2 (SysMAX) SW3.5 (PCIe)	Mode 7: Both On-board Intel download circuit and OOBE act as JTAG Masters Separated HPS and SDM JTAG **chains, OOBE only drive HPS** Mode 8: Both External Intel download cable & OOBE JTAG act as JTAG Masters Separated HPS and SDM JTAG **chains, OOBE only drive HPS**
110	OFF/OFF/ON	N/A	Mode 11: Both On-board Intel download circuit and OOBE act as JTAG Masters **On-board** Intel download circuit **only drive SDM, OOBE only drive HPS**
Others	N/A	N/A	Reserved

Note: UB2/PWR Intel MAX 10 has dedicated JTAG header J18 on board bottom side. When customer plugs in the Intel FPGA Download Cable dongle cable into J18, power Intel MAX 10 enters debug mode 0 or 1 by detecting PWRMAX_DEBUGMDn signals. You should not overwrite UB2/Intel MAX 10 image through J18, otherwise board will not function properly.

A.2. Power

Figure 17. Power Tree

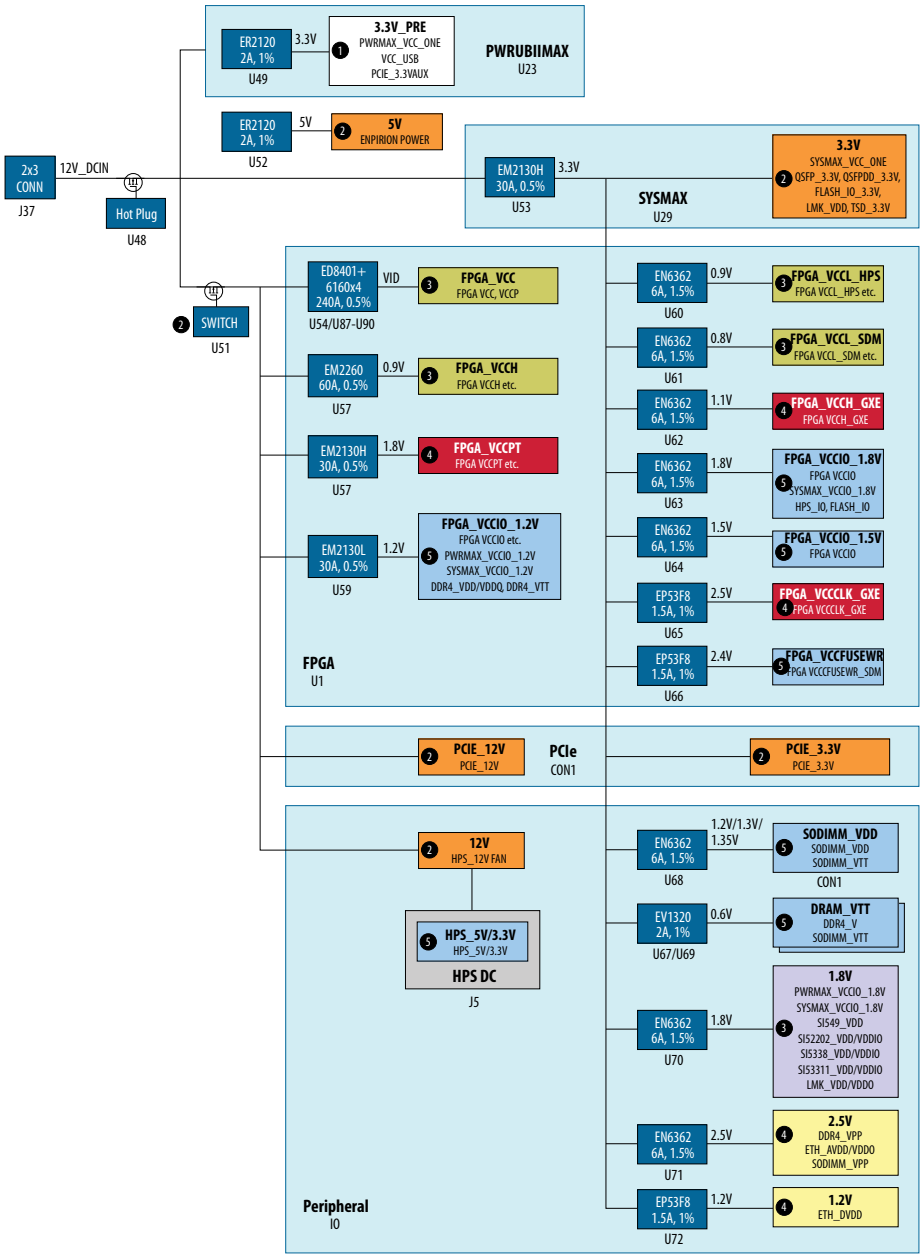
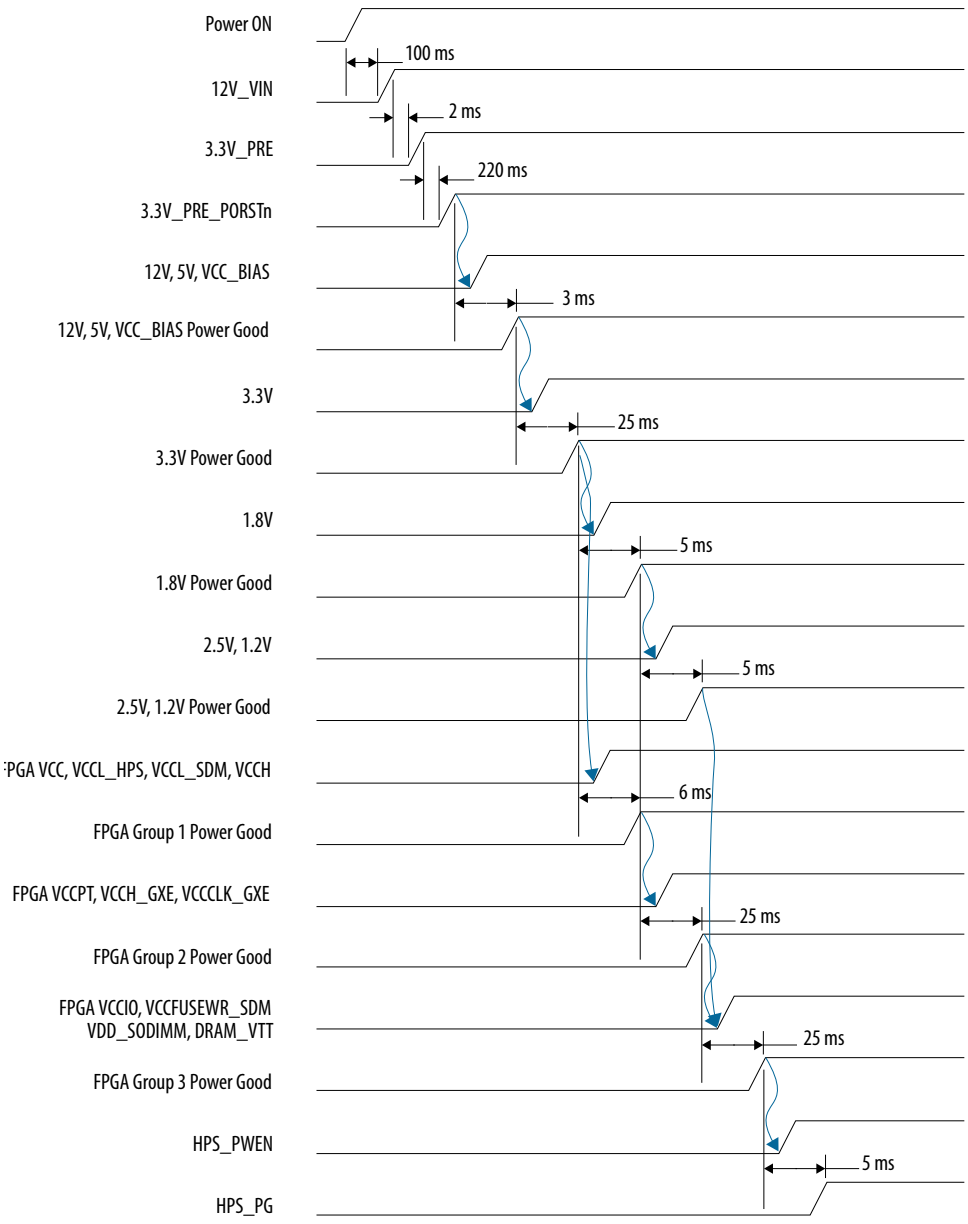


Figure 18. Power Sequence



Onboard hot-plug circuit shuts down all power rails when total power over 360 W (30 A).

UB2/PWR MAX 10 shuts down significant power rails when one or more power good indicators below low due to a power fault.

UB2/PWR MAX10 also shuts down significant power rails when temperature cross the acceptable range.

A.3. Clocks

Table 10. Default Clock Frequency

Schematic Signal Name	Default Frequency
FPGA_GPIO_REFCLKp/n0	156.25M
REFCLK_GXEp/n0	156.25M
SI53311_CLKOUT1p/n	156.25M
REFCLK_GXPp/n0	100M
REFCLK_GXPp/n2	100M
PCIE_RC_REFCLKp/n	100M
FPGA_GPIO_REFCLKp/n1	125M
SODIMM_REFCLKp/n	100M
FPGA_OSC_CLK_1	125M
FPGA_GPIO_REFCLK	100M
DDR4_COMP_REFCLKp/n	100M
FPGA_SYSTEM_CLK	100M
REFCLK_GXEp/n2	153.6M
REFCLK_GXEp/n3	184.32M
Cleaner_SYSTEM_P/N	184.32M
referenceclk_2	184.32M
referenceclk_3	153.6M

The LMK05028 device is a high-performance clock generator, jitter cleaner and clock synchronizer with advanced reference clock selection and hitless switching to meet the stringent requirements of communications infrastructure applications. This clock device has two independent PLL cores that can each synchronize or lock to one of four reference clock inputs, and it can generate up to eight output clocks with up to six different frequencies.

Two E-tile transceiver recovery clocks (`Cleaner_RECOVERY_p/n [0:1]`) feed two of four reference clock inputs, single-end and differential SMA clocks feed other two inputs. LMK05028's output clocks feed back to E-tile transceiver bank, general I/O banks and SMA connectors. LMK05028 can be set to power down mode by SW4.4.

Intel Agilex F-Series FPGA manages LMK05028 through general purpose I/Os (`Cleaner_GPIO[0:6]`, `Cleaner_INSEL`, `Cleaner SCL/SDA`, `Cleaner_status[0:1]`). The connection between these general purpose IOs and FPGA can be shut down by SW10.2.

Figure 19. FPGA Clocks

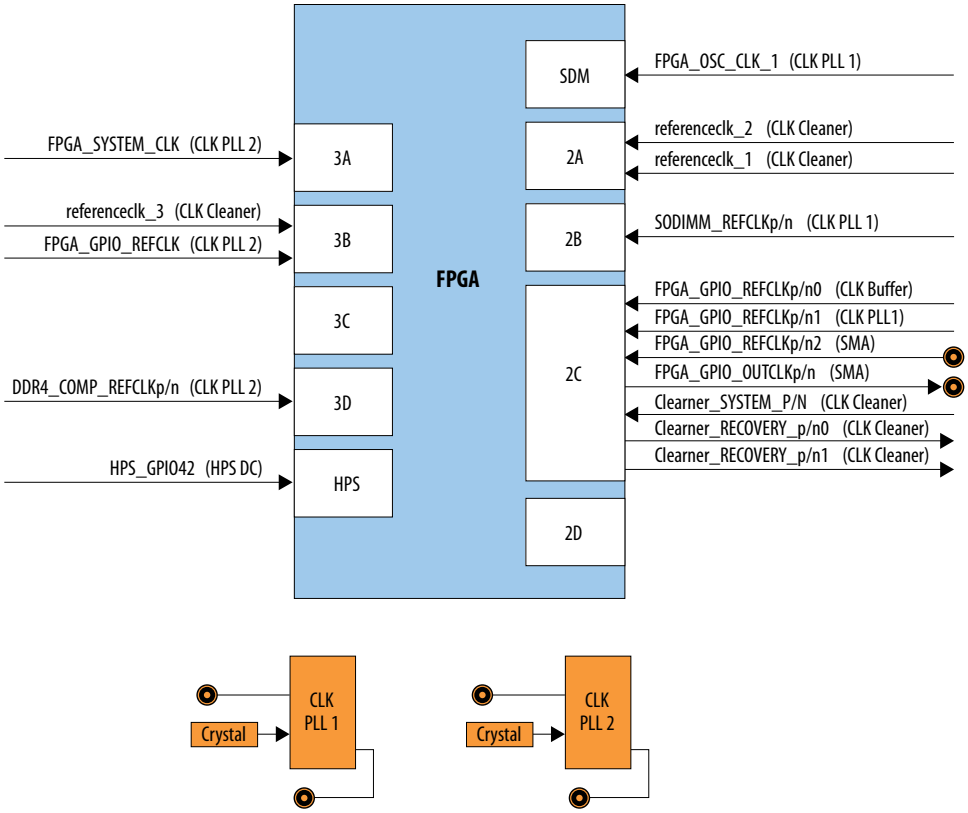
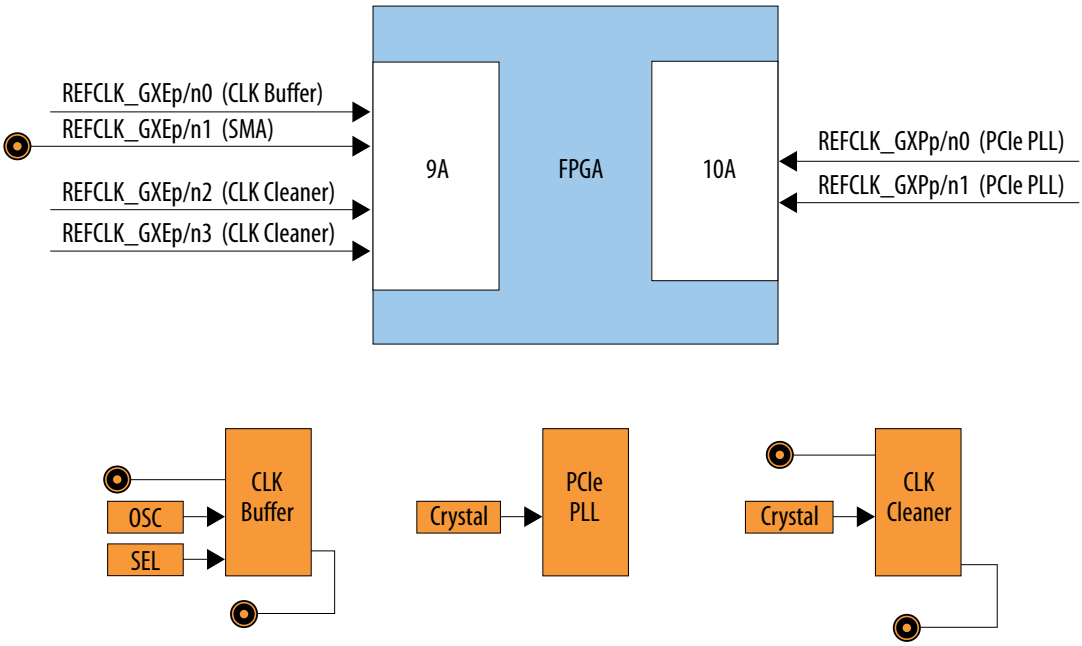


Figure 20. Transceiver Clocks



A.4. General Input/Output

Table 11. Intel Agilex FPGA

Schematic Signal Name	Description
FPGA_LED_G [0:7]	USER_LED[0:7]
FPGA_PB [0:7]	USER_PB[0:7]
FPGA_SW [0:7]	USER_DPSW[0:7]
FPGA_TESTIO [0:9]	USER_IO[0:9]
FPGA_TEST_SCL/SDA/ALERTn	USER_SMBUS

Table 12. System Intel MAX 10

Schematic Signal Name	Description
SYSMAX_LED_G0	PGM_LED0 for AvST configuration
SYSMAX_LED_G1	PGM_LED1 for AvST configuration
SYSMAX_LED_G2	PGM_LED2 for AvST configuration
SYSMAX_LED_G3	MAX_LOAD for AvST configuration
SYSMAX_LED_G4	MAX_CONF_DONE for AvST configuration
SYSMAX_LED_Y0	MAX_ERROR for AvST configuration
SYSMAX_LED_Y1	OVERTEMP
SYSMAX_PB0	MAX_RESETn
SYSMAX_PB1	CPU_RESETn
SYSMAX_PB2	HPS_COLD_RESETn
SYSMAX_PB3	RESERVED
SYSMAX_PB4	PGM_SEL for AvST configuration
SYSMAX_PB5	PGM_CFG for AvST configuration
SYSMAX_SW0	FACTORY_LOADn
SYSMAX_SW1	CLKSEL_156M ON: SI53311_CLKSEL = 0 OFF: SI53311_CLKSEL = 1
SYSMAX_SW[2:3]	USER_DIPSW
SYSMAX_SW4	I2C_3.3V_BUS_DEBUG_MODEn ON: i2c_3.3v_en = 0 OFF: i2c_3.3v_en = 1
SYSMAX_SW5	CLKCleaner_IO_DEBUG_MODEn ON: clkcleaner_io_tsn = 0 OFF: clkcleaner_io_tsn = 1

Table 13. UB2/PWR Intel MAX 10

Schematic Signal Name	Description
PWRMAX_LED_G0	FPGA Power Good
PWRMAX_LED_G1	System MAX10 Power Good
PWRMAX_LED_R0	Power Error
PWRMAX_LED_R1	Over Temperature
PWRMAX_PB0	RESERVED
PWRMAX_SW0	RESERVED
PWRMAX_SW1	VCCFUSEWR_SDM_FPGA_2.4V_SETn ON: 2.4V, OFF: 1.8V
PWRMAX_SW2	VCCLHPS_FPGA_0.9V_BYPASSn ON: From VCC core, OFF: From U60
PWRMAX_SW3	LMK05028_PDn ON: Power Down, OFF: Power ON
PWRMAX_SW4	STBY_MODE0n ON: Power Debug Mode 0, OFF: Normal
PWRMAX_SW5	STBY_MODE1n ON: Power Debug Mode 1, OFF: Normal

A.5. Memory Interfaces

FPGA dedicated external memory interface (SO-DIMM)

Intel is designing and verifying a customized QDRIV SODIMM module which fits with the 260-pin DDR4 SODIMM socket. Both DDR4 and QDRIV protocols can be tested on one single socket CON1. A long guide pin assembled on the customized QDRIV module slides in the guide hole which is reserved on Intel Agilex F-Series Transceiver-SoC Development Kit. This mechanical design avoids a wrong plug between customized QDRIV SODIMM and unsupported mother board. Only Intel Agilex FPGA fabric can access this external memory interface.

FPGA and HPS shared external memory interface (DDR4)

DDR4 component interface is a 72 bit, single rank configuration based on x16 component. It runs at 2400 Mbps. Footprint supports both MT40A1G16RC-062E and MT40A1G16KNR-062E component. By default, the component is: MT40A1G16RC-062E. Both Intel Agilex FPGA fabric and HPS can access this external memory interface, however they cannot be accessed at the same time.

A.6. Communication Interfaces

PCIe Slot

The PCIe root port is a PCIe Gen4 x16 port which fans out from Intel Agilex F-Series FPGA P-tile. This port is designed to meet PCIe Gen4 mother board requirement. System Intel MAX 10 acts as the board management controller (BMC) of the

development kit. It manages power up reset for both PCIe root port (PCIE_RC_PERSTn) and PCIe end point (PCIE_EP_PERSTn). In FPGA user mode, PCIe root complex design can initiate PCIe link reset through FPGA_GPIO[0] signals.

Table 14. PCIe Slot

Schematic Signal Name	Description
PCIE_EP_PERSTn	PCIe endpoint reset
PCIE_RC_WAKEn	PCIe wake up
PCIE_RC_REFCLKp/n	PCIe reference clock
PCIE_RC_PRSNTn	PCIe present
I2C_PCIE_SCL/SDA	PCIe I2C bus
PCIE_RC_JTAG_TCK/TMS/TDO/TDI/TRSTn	PCIe JTAG bus
PCIE_RC_TXP/N[0:15]	Transceiver TX
PCIE_RC_RXP/N[0:15]	Transceiver RX

QSFP28

QSFP28 port fans out from Intel Agilex F-Series FPGA E-tile. All four channels can run up to 30G NRZ and 30G PAM4. Two of them can run up to 58G PAM4. This port supports 2x56G, 4x10G and 4x25G application cases.

Table 15. QSFP28

Schematic Signal Names	Description
QSFP_MODPRSn	Module present
QSFP_RESETn	Module reset
QSFP_MODSELn	Mode select
QSFP_INITMODE	Initial mode
QSFP_INTn	Interrupt
QSFP_I2C_SCL	I^2C clock
QSFP_I2C_SDA	I^2C data
ZQSFP_TXP/N[0:3]	Transceiver TX
ZQSFP_RXP/N[0:3]	Transceiver RX

QSFPDD

QSFPDD port fans out from Intel Agilex F-Series E-tile. All eight channels can run up to 30G NRZ and 30G PAM4. Four of them can run up to 58G PAM4. This port is suitable for 2x56G, 4x10G, 4x25G and 8x25G application cases.

Table 16. QSFPDD

Schematic Signal Names	Description
QSFPDD_MODPRSn	Module present
QSFPDD_RESETn	Module reset
QSFPDD_MODSELn	Mode select
QSFPDD_INITMODE	Initial mode
QSFPDD_INTn	Interrupt
QSFPDD_I2C_SCL	I^2C clock
QSFPDD_I2C_SDA	I^2C data
QSFPDD_TXP/N[0:7]	Transceiver TX
QSFDDP_RXP/N[0:7]	Transceiver RX

MXP

MXP port fan out from Intel Agilex F-Series FPGA E-tile. All four channels can run up to 30G NRZ and 30G PAM4. Two of them can run up to 58G PAM4. This port supports SMA to equipment, backplane, different host compliance boards for 1x10G/1x25G/1x56G/2x56G/4x10G/4x25G cases.

Table 17. MXP

Schematic Signal Names	Description
MXP_TXP/N[0:3]	Transceiver TX
MXP_RXP/N[0:3]	Transceiver RX

10/100/1000M Triple speed ethernet (TSE)

TSE port is using SGMII between 80E1111 PHY and Intel Agilex F-Series FPGA LVDS I/Os.

Table 18. 10/100/1000M Triple speed ethernet (TSE)

Schematic Signal Names	Description
ETH_RSTn	PHY reset
ETH_INTn	Interrupt
ETH_MDC	MDIO clock
ETH_MDIO	MDIO data
ETH_SGMII_TXp/n	SGMII TX
ETH_SGMII_RXp/n	SGMII RX

Serial Buses

SDM I/Os (SDM_IO0/12) and Intel MAX 10 I/Os (SDM_I2C_SCL/SDA) share the same I^2C bus which talks with Intel Agilex FPGA core regulators. By default, SDM acts as SmartVID master and system Intel MAX 10 act as Power GUI master in this chain.

System Intel MAX 10 I/Os (SYSMAX_I2C_SCL/SDA) manages the second I^2C bus which access all I^2C slaves except Intel Agilex FPGA core regulators. The slaves include power regulators, temperature monitor, voltage monitor, EEPROM, RTC,oscillator and PLLs.

HPS I/Os (HPS_GPIO30/31) can access these two I^2C chains by rework optional resistors.

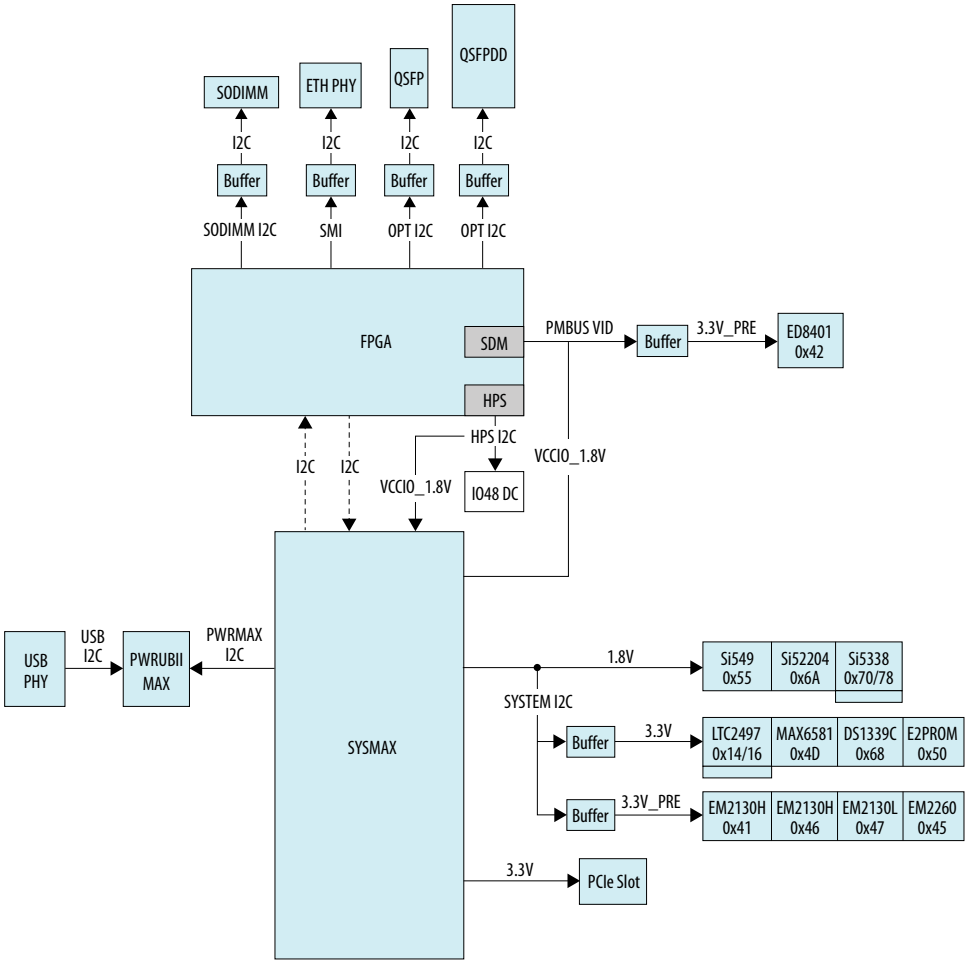
Intel Agilex FPGA general I/Os (F2M_I2C_SCL/SDA) talks with system Intel MAX 10 and it cannot direct access these two I^2C chains.

Intel Agilex FPGA also manages Ethernet PHY, QSFP28, QSFPDD, SODIMM I^2C buses and LMK05028 SPI bus by GPIOs.

Table 19. I^2C Debug Headers

Schematic Signal Name	Description
ENPIRION_I2C_SCL/SDA	Enpirion I^2C header J35
SYSMAX_I2C_SCL/SDA	System Intel MAX 10 I^2C bus header J51
Cleaner_SCL/SDA	Debug header for clock cleaner J26

Figure 21. I²C Serial Bus



A.7. Daughter Cards

HPS IO48 OOBE daughter card

- One RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45
- One UART port: Standard USB Mini-B Receptacle
- One Micro SD Card Connector: Standard Micro SD Card Socket
- One USB 2.0 port: Standard USB Micro-AB Receptacle
- One Mictor 38-pin connector (JTAG only without Trace signals)
- HPS dedicated JTAG pins are connected with both mother board JTAG chain and Mictor 38pin header

- I^2C: HPS I^2C port
- GPIO
  - 2 Push buttons
  - 3 LEDs
  - 1 Ethernet Interrupt from Ethernet PHY
  - 1 USB over-current indicator
- HPS Clock: 25 MHz oscillator

HPS IO48 NAND daughter card

- One RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45
- One UART port: Standard USB Mini-B Receptacle
- NAND Flash (x16): 8 Gb
- eMMC (x8): 8 GB 5.0 compliant eMMC
- I^2C: HPS I^2C port
- GPIO
  - 2 Push Buttons
  - 3 LEDs
  - 1 Ethernet Interrupt from Ethernet PHY
- HPS Clock: 25 MHz oscillator

256MB QSPI flash daughter card

This daughter card is pre-programmed with GHRD for AS configuration. It can be re-programmed by customer image or factory provided AvST test image for AvST configuration mode. The part number is MT25QU02GCBB8E12-0SIT.

B. Additional Information

B.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

B.1.1. Safety Warnings

Power Supply Hazardous Voltage

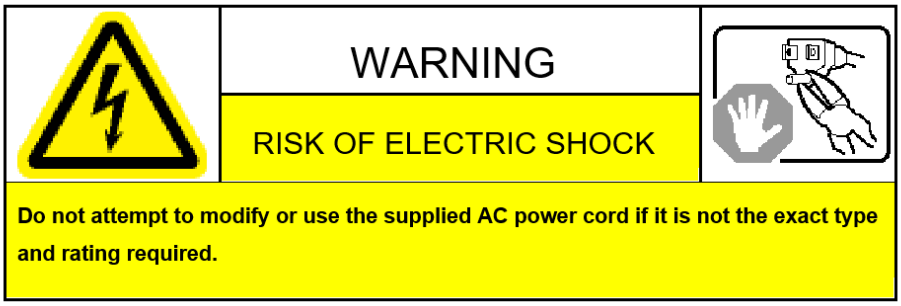
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.

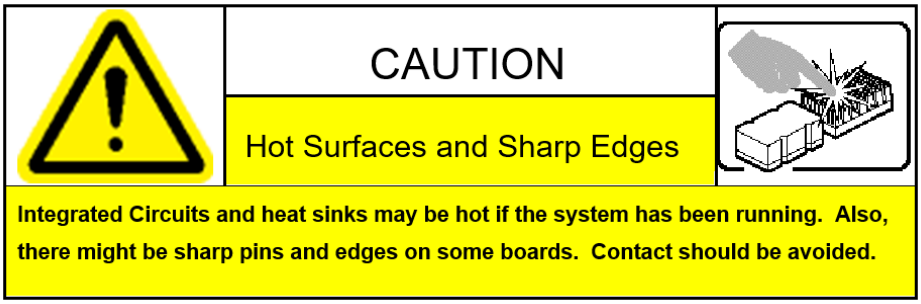
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

B.1.2. Safety Cautions



Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

B.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

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