

# Arria V GX Transceiver Starter Kit

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- [Ordering Information](#)
- [Transceiver Starter Kit Contents](#)
- [Starter Board Photo](#)
- [Related Links](#)

The Altera® Arria® V GX Transceiver Starter Kit provides a complete design environment that includes all the hardware and software you need to develop cost-sensitive FPGA applications immediately. The development kit is RoHS compliant. The development kit features the following:

- Arria V GX FPGA—360KLE, F1517 package, 24X6.6G XCVRs, C4 speed grade
- One I/O expansion slots—one high-speed mezzanine card (HSMC)
- 16 MB of SDRAM memory
- High-definition multimedia interface (HDMI) and serial digital interface (SDI) connections
- SMAs

## Ordering Information

Table 1. Arria V GX Transceiver Starter Kit Ordering Code and Pricing Information		
Ordering Code	Price	Ordering Information
DK-START-5AGXB3NES		<p>The <b>Arria V GX Transceiver Starter Kit</b> features a 5AGXB3 Engineering Sample (ES) device and a 1-year license for the Quartus® II design software.</p> <p>Contact your <a href="#">local Altera distributor</a> to place your order.</p>

[↑TOP](#)

## Transceiver Starter Kit Contents

- The Arria V GX Transceiver Starter Kit features the following:
  - Arria V GX FPGA development board (see Figure 1)
  - FPGA: Arria V GX 5AGXFB3H4F35C4NES
  - System controller: MAX® V 5M2210ZF256C4N
    - Power monitor GUI
    - Single analog-to-digital converter (ADC), eight channels
    - Non-isolated power rail
    - Fast passive parallel (FPP) x16 mode through parallel flash loader (PFL)
    - Control and status registers
  - Embedded USB-Blaster™ II: MAX II EPM570GM100C4N
  - HDMI 1.3 TX
    - x4 XCVR, 3.4 Gbps (max by spec) and 340 MHz TX clock (by spec)
    - HDMI TX connector
    - TI HDMI level shifter SN75DP130
    - Level shift XCVR PCML 1.5V <-> TMDS level
    - DDC and HPD <-> HDMI compliant level
    - Data channel up to 5.4 Gbps; HDMI 1.3 only needs a maximum of 3.4 Gbps
    - Clock channel up to 340 MHz; enough to support 3.4 Gbps data rate
    - HDMI specification: clock period = 10x of UI
    - Requires 100 MHz clock input at CLKIN to generate the TX clk and core logic
  - SDI 3G
    - x1 XCVR TX/RX loopback
    - x2 SMB connectors and cable (cable not included in kit)

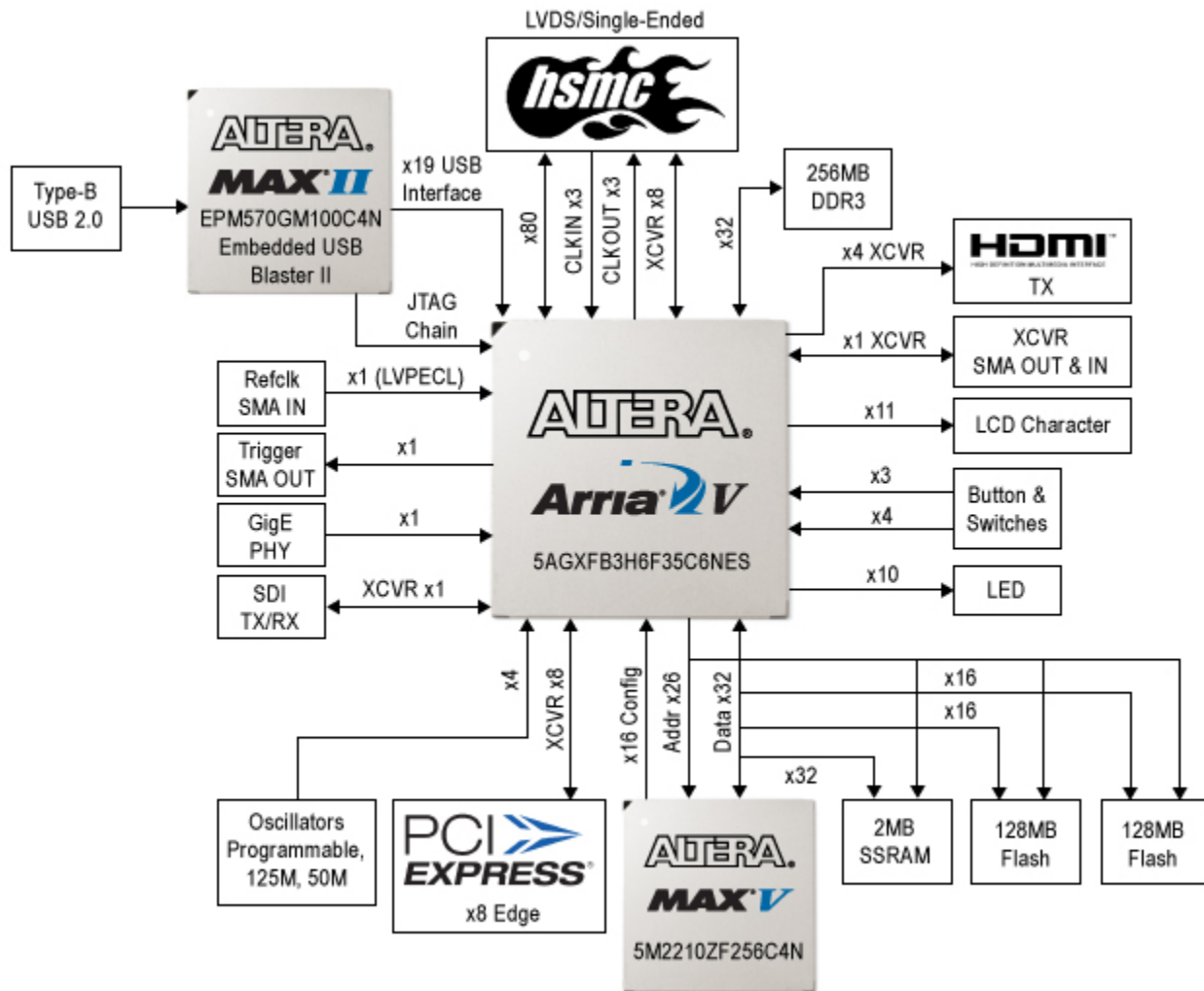
- Up to 2.97 Gbps
- Uses National Semiconductor driver/receiver LMH0384SQ/LMH0303SQx
- Requires 148.5 MHz and 148.35 MHz at XCVR refclk to support US and EU standard respectively
- Use VCXO to fine tune and lock to the recovered CDR frequency
- Requires 125 MHz CLKIN for core logic
- HSMC
  - x8 XCVR up to 6.375 Gbps
  - Not complied to PCI Express® (PCIe®) HIP pin assignment
  - x4 CMOS
  - x17 differential using dedicated TX/RX channel
  - x2 low-voltage differential signalling (LVDS) clock in
  - x2 differential clock out
  - I2C
  - JTAG
  - Minimum current support
    - 2A @ 3.3V
    - 1A @ 12V
  - Dedicated clock domain from Si 5338 clock generator for xcvr refclk
  - HSMC loopback with BTS GUI
- SMA
  - 7x XCVR TX/RX channel
  - 1x LVDS clock input
- Dedicated clock domain from Si 5338 clock generator for xcvr refclk
- DDR3 SDRAM x32
  - Micron MT41J64M16JT-15E DDR3 SDRAM 8MX16X8
  - Two devices: 2 x16 width = x32
  - BTS DDR3 SDRAM GUI using Uniphy and high performance (HP) controller II
- SSRAM
  - 1024k x18, 18 Mb ISSI IS61VPS102418A
  - Shared address or data with flash
- User IO
  - LCD character
  - x4 DIP switch
  - x3 PB
  - x4 LED
- Configuration
  - FPP x16 mode
  - Dual flash 512Mbit Numonyx PC28F512P30BF (52 MHz F<sub>MAX</sub>)
- JTAG header
- Embedded USB Blaster II
  - Cypress Microcontroller CY7C68013A as USB PHY 2.0
  - MAX II
  - Ethernet
    - 10/100/1000 Base-T
    - RJ-45 connector, on-board LED for link status
    - Marvell Ethernet PHY 88E1111
    - Requires 100 MHz and 125 MHz clock from CLKIN

[↑TOP](#)

**Figure 1: Arria V GX Starter Board with a 5AGXB3ES FPGA Device**



Figure 2: Arria V GX Starter Board Block Diagram



[↑TOP](#)

**Related Links**

- [Arria V FPGA documentation page](#)
- [Errata Sheet and Guidelines for Arria V ES Devices \(PDF\)](#)
- [Altera and partner daughter cards](#)
- [Other Arria V FPGA-based development kits](#)
- [Jungo PCI Express WinDriver \(30-day evaluation\)](#)

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