Intel® Enpirion® Power Solutions

ED8401 Digital Multi-Phase Controller

Multi Phase, Single Output, Fully Digital Step-down Controller with PMBus™ v1.2 Compliant Interface

Description

The ED8401 is a true digital multi-phase step-down controller for non-isolated, high current DC/DC applications. A PMBus version 1.2 compliant interface provides setup, control, and telemetry.

Differential remote sensing and ±0.5% set-point accuracy provides precise regulation over line, load and temperature variation to provide excellent static regulation for today's FPGAs, ASICs, processors, and DDR memory devices.

The ED8401 can be configured and controlled in any application by two methods, either in pin-strap mode using onboard resistors, or using the PMBUS interface. The customer can also configure the device during engineering evaluation using the PMBUS interface, which offers a high degree of flexibility and programmability, and then use the pin strap mode when devices are deployed in production. The Intel Enpirion Digital Power Configurator provides a user-friendly and easy-to-use interface for communicating with and configuring the device.

The ED8401 offers a scalable solution by operating in 4, 3, or 2 phase mode. Combined with the Intel Enpirion ET6160LI power stage, this enables an optimized load current range to greater than 200A.

Features

- Programmable digital control loops
- All Phases actively current balanced
- Tracking pin for complex power sequencing
- Vin Feed-forward
- Individual Tmon input for each Phase
- Meets all high-performance FPGA requirements
  - Digital loop for excellent transient response
  - 0.5% set-point over line, load, temperature
  - Differential remote sensing
  - Monotonic startup into pre-bias output
  - Optimized FPGA configs stored in NVM
- Programmable through PMBus
  - V_{OUT} margining, startup and shutdown delays
  - Programmable warnings, faults and response
- Operational without PMBus
  - RVSET resistor for setting V_{OUT}
  - RTUNE resistor for single resistor-based compensation
- Programmable Overcurrent Response
  - Latch Off (default)
  - Hiccup
- Protection features
  - Over-Current Protection
  - Over Voltage protection VIN VOUT
  - Under Voltage protection VIN VOUT
  - Over Temperature
  - Restart and delay times
- Fuse-Based NVM for improved reliability
- RoHS compliant, MSL level 3, 260°C reflow
- Small 5mmx5mmx0.9mm QFN Package

Applications

- High performance FPGA Core Supply
- ASIC and processor supply rails

Ordering Information

Part Number	Configuration*	Package Markings	Package Description
ED8401P01QI	4-Phase 500kHz	84011	5 mm x 5 mm x 0.9mm QFN40
ED8401P03QI	3-Phase 500kHz	84013	5 mm x 5 mm x 0.9mm QFN40
ED8401P05QI	2-Phase 500kHz	84015	5 mm x 5 mm x 0.9mm QFN40
EVB-ED8401P01		Evaluation board; 4-Phase, 500kHz	
EVB-ED8401P03		Evaluation board; 3-Phase, 500kHz	
EVB-ED8401P05		Evaluation board; 2-Phase, 500kHz	
EVI-EM2COMIF	GUI interface dongle		

* For alternative configurations contact Sales

Packing and Marking Information: www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

Pin Assignments

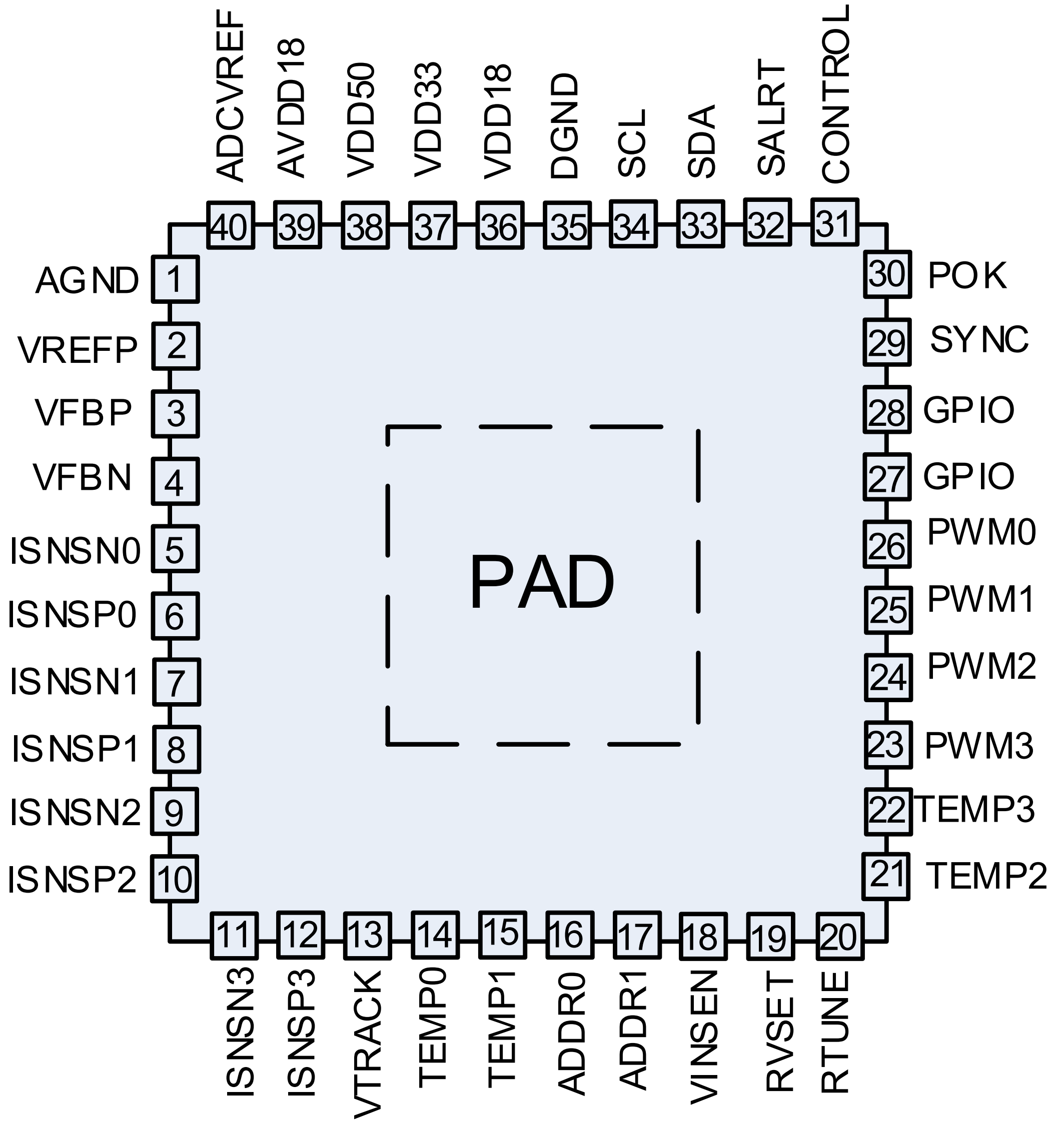


Figure 1: Pin Out Diagram (Top side)

For 2 & 3 Phase derivatives the now unrequired ISNSxx, Tempx and PWMx pins maybe left floating

Pin Description

PIN	NAME	I/O	FUNCTION
1	AGND	Input	Analog ground. Connect to system ground plane.
2	VREFP	Output	Reference terminal
3	VFBP	Input	Differential output voltage sense input (positive).
4	VFBN	Input	Differential output voltage sense input (negative).
5	ISNSN0	Input	Negative input of differential current sensing Phase 0
6	ISNSP0	Input	Positive input of differential current sensing Phase 0

PIN	NAME	I/O	FUNCTION
7	ISNSN1	Input	Negative input of differential current sensing Phase 1
8	ISNSP1	Input	Positive input of differential current sensing Phase 1
9	ISNSN2	Input	Negative input of differential current sensing Phase 2
10	ISNSP2	Input	Positive input of differential current sensing Phase 2
11	ISNSN3	Input	Negative input of differential current sensing Phase 3
12	ISNSP3	Input	Positive input of differential current sensing Phase 3
13	VTRACK	Input	External voltage tracking input
14	TEMP0	Input	Temp0 Channel (with PTOK & Fault Detection)
15	TEMP1	Input	Temp1 Channel (with PTOK & Fault Detection)
16	ADDR0	Input	PMBus address selection 0
17	ADDR1	Input	PMBus address selection 1
18	VINSEN	Input	PVIN supply input voltage sensing
19	RVSET	Input	A resistor from RVSET to AGND; can be used to set the Output Voltage
20	RTUNE	Input	A resistor from RTUNE to AGND; can be used to scale the compensator coefficients
21	TEMP2	Input	Temp2 Channel (with PTOK & Fault Detection)
22	TEMP3	Input	Temp3 Channel (with PTOK & Fault Detection)
23	PWM3	Output	PWM control signal phase 3
24	PWM2	Output	PWM control signal phase 2
25	PWM1	Output	PWM control signal phase 1
26	PWM0	Output	PWM control signal phase 0
27	GPIO	Input/Output	General Purpose Input/Output
28	GPIO	Input/Output	General Purpose Input/Output
29	SYNC	Input/Output	PWM synchronization signal
30	POK	Output	Output status flag (open drain)
31	CONTROL	Input	Control input (configurable – default high = Enable output))
32	SALRT	Output	PMBus alert output
33	SDA	Input/Output	PMBus shift data I/O
34	SCL	Input	PMBus shift clock input (slave-only)
35	DGND	Ground	Digital ground. Connect to system ground plane.
36	VDD18	Output	Internal 1.8V digital supply terminal
37	VDD33	Input/Output	3.3 V supply voltage terminal
38	VDD50	Input	5.0V supply voltage terminal
39	AVDD18	Output	Internal 1.8V analog supply terminal
40	ADCVREF	Input	Analog-to-digital converter (ADC) reference terminal
	PAD	Input	Exposed pad, digital ground. (Connect to Pins 1 & 35)

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Voltage measurements are referenced to PGND.

Absolute Maximum Pin Ratings

Table 1

PARAMETER	SYMBOL	MIN	MAX	UNITS
5V supply voltage	VDD50	-0.3	5.5	V
Maximum slew rate	VDD50		0.15	V/µs
3.3V supply voltage	VDD33	-0.3	3.9	
Maximum slew rate	VDD33 = VDD50		0.15	V/µs
1.8V supply voltage	VDD18 AVDD18	-0.3	2.0	V
Digital I/O pins	SCL, SDA, CTRL, SALRT, POK SYNC, PWMx	-0.3	3.9	V
Analog/Digital I/O pins	TEMPx	-0.3	3.9	V
Analog pins	ADCREF, VREFP, VINSEN, ADDRx, RVSET, RTUNE, VTRACK	-0.3	3.9	V
Voltage feedback, positive	VFBP	-0.3	2.0	V
Voltage feedback, negative	VFBN	-0.3	0.3	V
Current sensing	ISNSPx ISNSNx	-0.3	5.0	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Operating junction temperature			+125	°C
Storage temperature range		-65	+150	°C
Reflow peak body temperature	(10 Sec) MSL3		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM	All pins;	1000		V
CDM	All pins;	500		V

Recommended Operating Conditions

Table 2

PARAMETER	PINS	MIN	MAX	UNITS
Supply voltage VDD50	VDD50	4.75	5.25	V
Supply voltage VDD33 (VDD50 tied to VDD33)	VDD33 = VDD50	3.00	3.6	V
Operation junction temperature		-40	125	°C
Non-Volatile Memory programming		0	50	°C

Thermal Characteristics

Table 3

PARAMETER	PINS	TYPICAL	UNITS
Thermal shutdown default [programmable]	T_{SD}	120	°C
Thermal shutdown Hysteresis [programmable]	T_{SDH}	18	°C
Thermal resistance: junction to case bottom (0 LFM)	θ_{JC}	1.5	°C/W

Electrical Characteristics

PV_{IN} = 12V and VDD50 = 5.0V. The minimum and maximum values are over the ambient temperature range (-40°C to 85°C) unless otherwise noted. Typical values are at T_A = 25°C.

Table 4

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY CHARACTERISTICS						
Input supply voltage range	VDD50		4.75	5.0	5.25	V
	VDD33	Supply for both the VDD33 and VDD50 pins if the internal 3.3V regulator is not used.	3.0	3.3	3.6	V
Input supply current		Normal operation; switching f_{sw} = 500kHz		70	125(2)	mA
		Idle; communication and telemetry but not switching		45		mA
Disabled (V_{CC} ≤ 2.8V) (2)		Disabled (V_{CC} ≤ 2.8V)		1.25		mA
INTERNALLY GENERATED SUPPLY VOLTAGES						
3.3V voltage range	VDD33	VDD50=5.0V	3.0	3.3	3.6	V
3.3V output current(2)		VDD50=5.0V			2	mA
Minimum Capacitance		-40°C to +125°C 3.0V to 3.6V	0.7			µF
1.8V voltage range	VDD18 AVDD18	VDD50=5.0V	1.72	1.8	1.98	V
1.8V output current(2)	AVDD18				1	mA
Minimum Capacitance		-40°C to +125°C 1.72V to 1.98V	0.7			µF
Internal References	VREF ADCREF	VDD50=5.0V		1.44		
Minimum Capacitance		-40°C to +125°C	0.1			µF
Power On Reset (POR) threshold for VDD33 pin – High				2.8		V
Power On Reset (POR) threshold for VDD33 pin – Low				2.6		V
Output voltage startup delay upon exceeding POR(2)		From VDD33 valid, to start of output voltage ramp, if configured to regulate from power on reset, and TON_DELAY is set to 0.		6		ms

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O PIN (SYNC)						
Input high voltage		Configured for input Clk	2.0		3.6	V
Input low voltage		Configured for input Clk	-0.3		0.8	V
Output high voltage		Configured as Output Clk	2.4		VDD 33	V
Output low voltage		Configured as Output Clk			0.4	V
Input leakage current					±1	µA
Output current - source					2.0	mA
Output current - sink					2.0	mA
SYNC frequency range (1)		Percent of nominal switching frequency			±12.5	%
SYNC pulse width(1)			25			ns
Open Drain PIN (POK)						
Low voltage			0		0.8	V
Input leakage current					±1	µA
Output current - sink					2.0	mA
POK Delay(2)		Normal mode & VTRACK mode. Propagation delay from detection of stable output until PG asserts.		42		µs
POK De-Assertion Delay(2)		Normal mode & VTRACK mode. Propagation delay from detection of out-of-band, or major fault, until PG de-asserts.		31		µs
DIGITAL I/O PIN (CTRL)						
Input high voltage			2.0		3.6	V
Input low voltage			-0.3		0.8	V
CTRL response delay (stop) (2)		Configurable polarity; extra turn-off delay configurable (assumes 0 s turn-off delay)		120		µs
CTRL response delay (start) (2)		Configurable polarity; extra turn-on delay configurable (assumes 0 s turn-on delay)		160		µs
DIGITAL I/O PINs (GPIO0 & GPIO1)						
Input high voltage		VDD33=3.3V	2.0		3.6	V
Input low voltage		VDD33=3.3V	-0.3		0.8	V
Output Sink Current		Configured for open drain			2	mA
Output high voltage		VDD33=3.3V	2.4		3.6	V
Output low voltage		VDD33=3.3V	-0.3		0.4	V
Output Drive Current					2	mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Output pins						
PWM output voltage - high		VDD33=3.3V	2.4			V
PWM output voltage - low		VDD33=3.3V			0.4	V
PWM tristate leakage					±1	µA
Frequency accuracy				2.0		%
PWM pulse width(2)			25			ns
Resolution(2)				163		ps
Current Measurement						
Common mode voltage(2)	ISNSP ISNSN		0		5.25	V
Differential voltage range(2)	ISNSP - ISNSN	ET6160 = 1µA/A x 2700Ω x 66.67A			180	mV
Accuracy		Controller reporting		3		%
OUTPUT VOLTAGE SENSE, REPORTING, AND MANAGEMENT						
Output voltage adjustment range			0.5		1.3	V
Output voltage set-point accuracy		0˚C < T_A < 85˚C	-0.5		+0.5	%
		-40˚C < T_A < 85˚C	-1		+1	%
Output set-point resolution				1.4		mV
Output voltage startup delay upon exceeding POR(2)		From VDD33 valid, to start of output voltage ramp, if configured to regulate from power on reset, and TON_DELAY is set to 0.		6		ms
Output voltage ramp delay (TON_DELAY & TOFF_DELAY) (2)		Configurable, no V_{OUT} pre-bias condition.	0		500	ms
VTRACK						
VTRACK ramp rate(2)					2.0	V/ms
VTRACK range			0		1.4	V
VTRACK offset voltage				±100		mV
TEMPERATURE SENSE, REPORTING, AND MANAGEMENT						
Temperature reporting accuracy				5		°C
Resolution				0.22		°C
Offset @ 25^{0}C (Reprogrammable)		Assuming 8mV/^{0}C		800		mV
FAULT MANAGEMENT PROTECTION FEATURES						

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Protection & Under-Voltage Protection						
Set-point voltage		Reference DAC	0		1.58	V
Resolution		Reference DAC		12.5		mV
Response Delay				<1		µs
ANALOG INPUT PINS (RVSET, RTUNE, ADDR0 AND ADDR1) - HKADC						
Input voltage—TEMPx, VINSEN, VCCSEN, ADDR0, ADDR1, RTUNE & RVSET pins			0		1.44	V
Source impedance VINSEN sensing					3	kΩ
ADC resolution				704		µV
SERIAL COMMUNICATION PMBUS DC CHARACTERISTICS						
Input voltage – high (VIH) [1]		SCL and SDA	1.11			V
Input voltage – low (VIL) [1]		SCL and SDA			0.8	V
Input leakage current[1]		SCL, SDA, SALRT, and CTRL.	-10		10	µA
Input leakage current		SCL, SDA, SALRT, and CTRL.		65		µA
Output voltage – low (VOL) [1]		SDA and SALRT at rated pull-up current of 20mA.			0.4	V
Maximum bus voltage		SCL and SDA termination voltage.			3.6	V
Maximum bus voltage		SALRT termination voltage.		3.3	3.6	V

(1) Parameter guaranteed by design or characterization

(2) These values are provided for information only.

Default Protection Values – 25°C - Programmable (unless otherwise stated)

PARAMETER	Note	Typical Value	UNITS
VOUT Over Voltage Protection Values (Programmable)			
Warning	Percentage of VOUT set by RVSET	107	%
Fault	Percentage of VOUT set by RVSET	120	%
Delay before Fault		0	ms
Delay before Retry		0	ms
# of retries		0	
VOUT Under Voltage Protection Values (Programmable)			
Warning	Percentage of VOUT set by RVSET	93	%
Fault	Percentage of VOUT set by RVSET	85	%
Delay before Fault		0	ms
Delay before Retry		0	ms
# of retries		0	
VIN Over Voltage Protection Values (Programmable)			
Warning		16.6	V
Fault		17	V
Delay before Fault		0	ms
Delay before Retry		0	ms
# of retries		0	
VIN Under Voltage Protection Values (Programmable)			
Warning		4.2	V
Fault		3.96	V
Delay before Fault		0	ms
Delay before Retry		0	ms
# of retries		Infinite	
Over Current Protection Values (Programmable)			
Warning Threshold	(Total - All 4 Phases) ED8401 - P01	200	A
Fault Threshold	(Total - All 4 Phases) ED8401 - P01	212	A
Warning Threshold	(Total - All 3 Phases) ED8401 - P03	150	A
Fault Threshold	(Total - All 3 Phases) ED8401 - P03	159	A
Warning Threshold	(Total - All 2 Phases) ED8401 - P05	100	A
Fault Threshold	(Total - All 2 Phases) ED8401 - P05	106	A
Delay before Fault		0	ms
Delay before Retry		0	ms
# of retries		0	

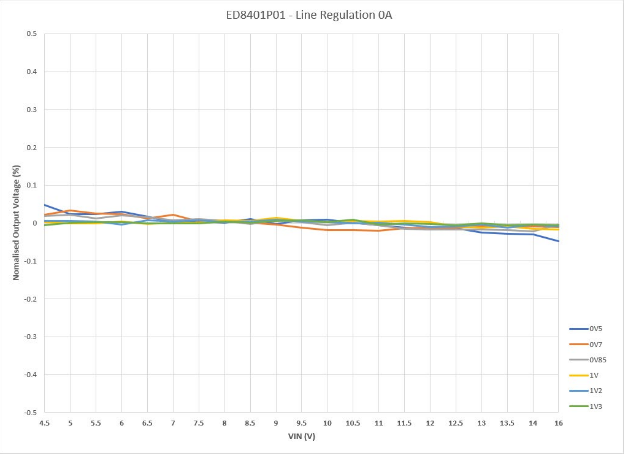
PARAMETER	Note	Typical Value	UNITS
Power Train Over Temperature Protection Values (Programmable)			
Warning Threshold		120	ºC
Fault Threshold		125	ºC
Delay before Fault		0	ms
Delay before Retry		0	ms
Temp On Level	Temperature must drop below before VOUT re-enabled	100	ºC
# of retries		Infinite	
Power Train Fault – through Temperature (TEMP0, TEMP1, TEMP2, TEMP3) Values (Programmable)			
Power Train Fault	Voltage level on TEMPx pins at which Power Train Fault is deemed to have occurred	2.25	V
Controller Over Temperature Protection Values (Programmable)			
Warning Threshold		110	ºC
Fault Threshold		120	ºC
Delay before Fault		0	ms
Delay before Retry		0	ms
Temp On Level	Same Value as used for Power Trains	100	ºC
# of retries		Infinite	
Duty Cycle Limits Values (Programmable)			
Minimum Duty Cycle Saturation	(Minimum PWM pulse width = 25ns)	0	%
Maximum Duty Cycle Saturation		50	%
VIN On/Off Thresholds Values (Programmable)			
On Level		4.4	V
Off Level		4.2	V
POK Thresholds Values (Programmable)			
On Level		95	%
Off Level		90	%

Typical Performance Characteristics

All the performance curves are measured with ED8401Pxx evaluation board at 25°C ambient temperature unless otherwise noted. The configuration of the evaluation board consists of an output inductor of 120µH with output capacitors of 16 x 470 µF (3 mΩ ESR) + 16 x 100 µF (Ceramic).

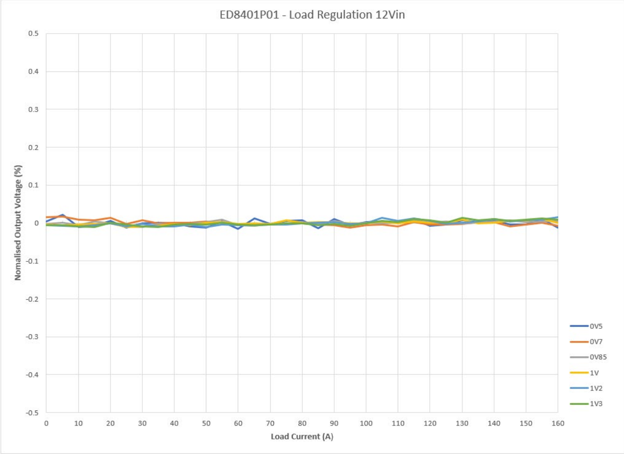
ED8401P01, Line Regulation, IOUT = 0A

Nomalised Output Voltage (%) vs PVIN



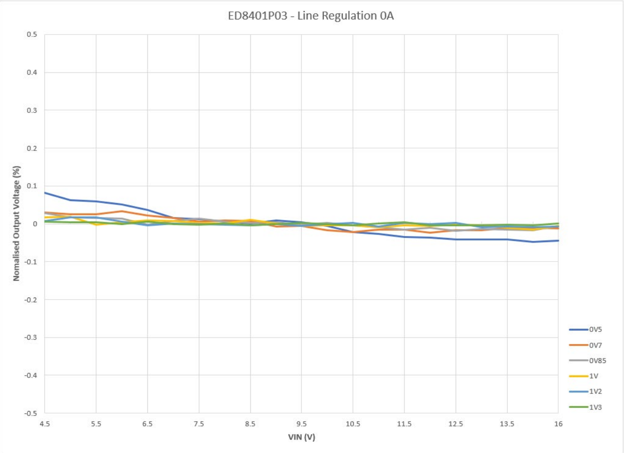
ED8401P01, Load Regulation, Vin = 12V

Nomalised Output Voltage (%) vs IOUT



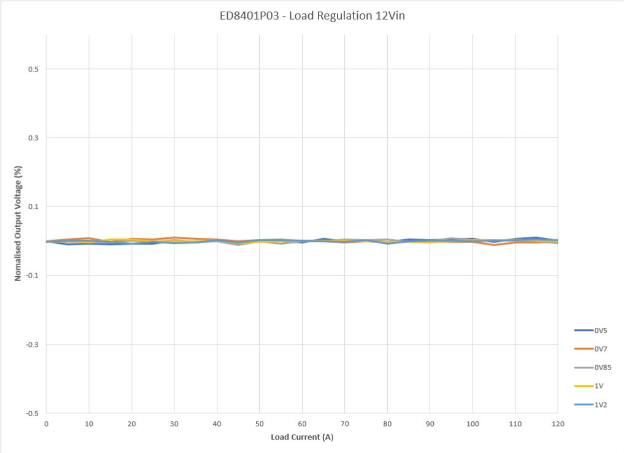
ED8401P03, Line Regulation, IOUT = 0A

Nomalised Output Voltage (%) vs PVIN



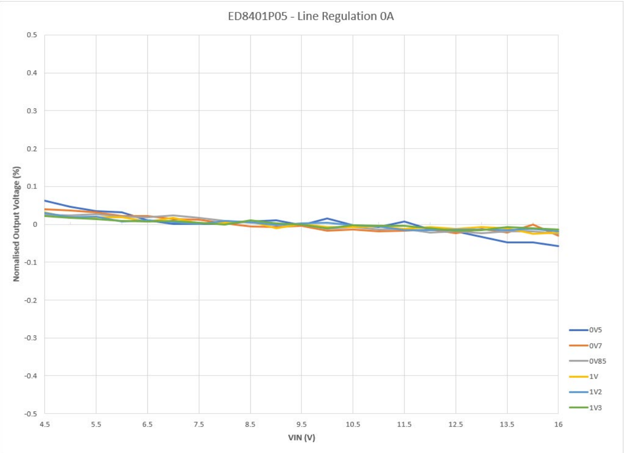
ED8401P03, Load Regulation, Vin = 12V

Nomalised Output Voltage (%) vs IOUT



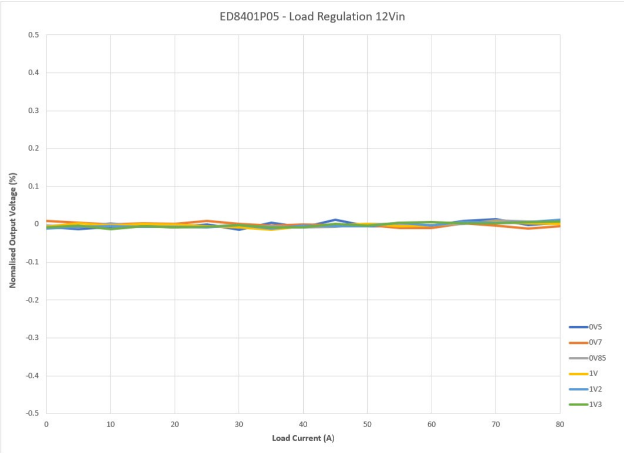
ED8401P05, Line Regulation, IOUT = 0A

Nomalised Output Voltage (%) vs PVIN

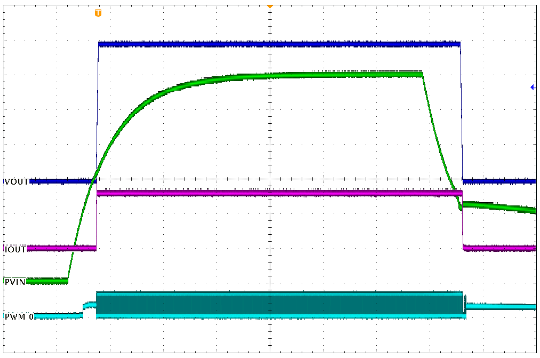


ED8401P05, Load Regulation, Vin = 12V

Nomalised Output Voltage (%) vs IOUT

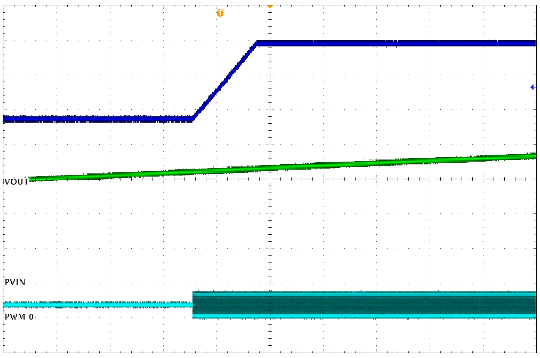


Start-up/Shutdown, PVIN, 1 ms/div



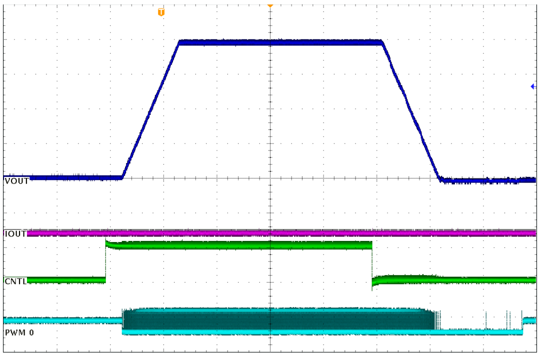
PV$_{IN}$ and PWM: 3 V/div,
V$_{OUT}$: 300 mV/div, I$_{OUT}$: 10 A/div

Start-up/Shutdown, PVIN – PreBias, 1 ms/div



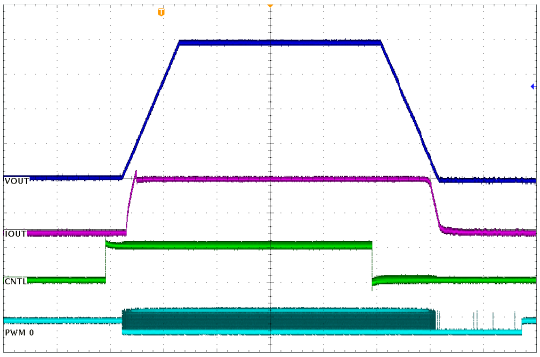
PV$_{IN}$ and PWM: 3 V/div,
V$_{OUT}$: 300 mV/div, I$_{OUT}$: 10 A/div

Start-up/Shutdown, CTRL At No Load, 1 ms/div



CTRL: 2V/div, PWM0: 5V/div,
V$_{OUT}$: 200 mV/div, I$_{OUT}$: 40 A/div

Start-up/Shutdown, CTRL At 160A Load, 800µs/div

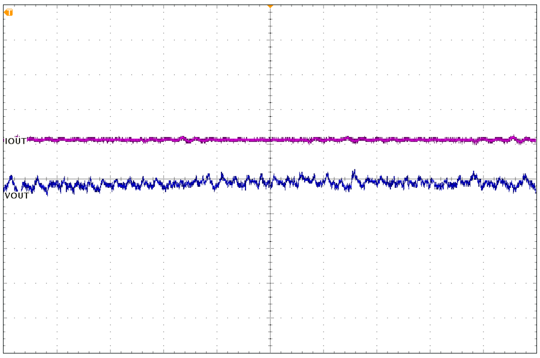


CTRL: 2V/div, PWM0: 5V/div,
V$_{OUT}$: 200 mV/div, I$_{OUT}$: 100 A/div

Typical Performance Characteristics (Continued)

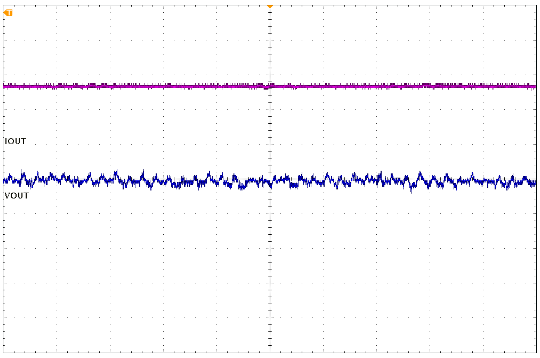
All the performance curves are measured with ED8401P01 evaluation board at 25°C ambient temperature unless otherwise noted. The configuration of the evaluation board consists of an output inductor of 120µH with output capacitors of 16 x 470 µF (3 mΩ ESR) + 16 x 100 µF (Ceramic).

Output Voltage Ripple, No Load



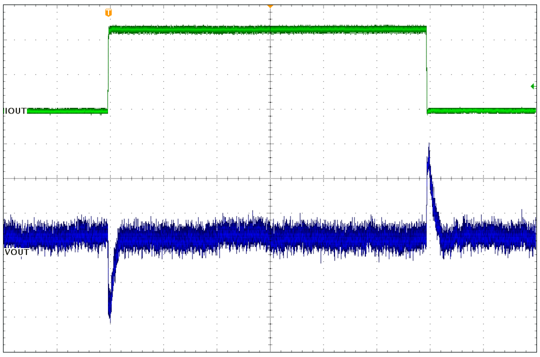
V_{IN} = 12V, V_{OUT} = 0.8V
2 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Ripple, 160A Load



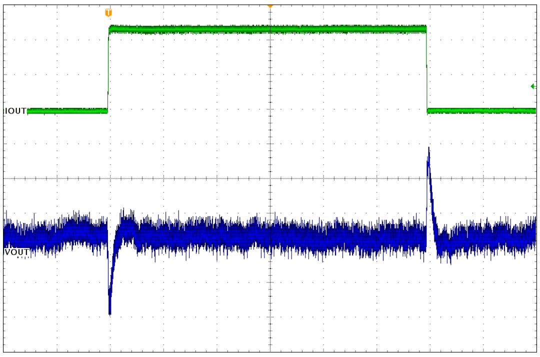
V_{IN} = 12V, V_{OUT} = 0.8V
2 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Transient Response, Load Step From 0A To 80A



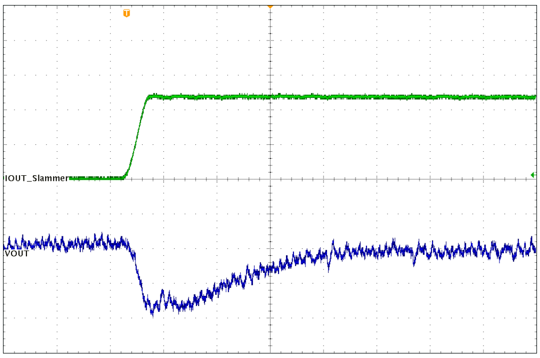
V_{IN} = 12V, V_{OUT} = 0.8V, 100µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 66A/div, 50A/µs

Output Voltage Transient Response, Load Step From 80A To 160A



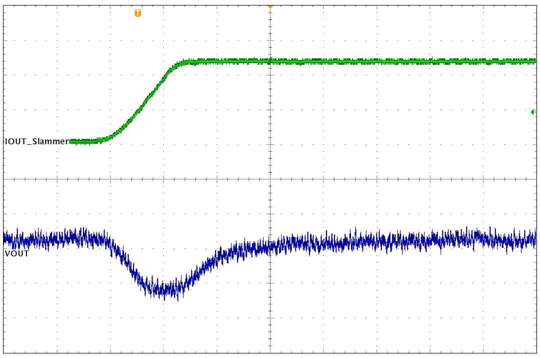
V_{IN} = 12V, V_{OUT} = 0.8V, 100µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 33A/div, 10A/µs

Output Voltage Transient Response, Load Step From 0A To 80A



V_{IN} = 12V, V_{OUT} = 0.8V, 4µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 33.3 A/div, 50A/µs

Output Voltage Transient Response, Load Step From 0A To 80A



V_{IN} = 12V, V_{OUT} = 0.8V, 10µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 33 A/div, 5A/µs

Functional Block Diagram

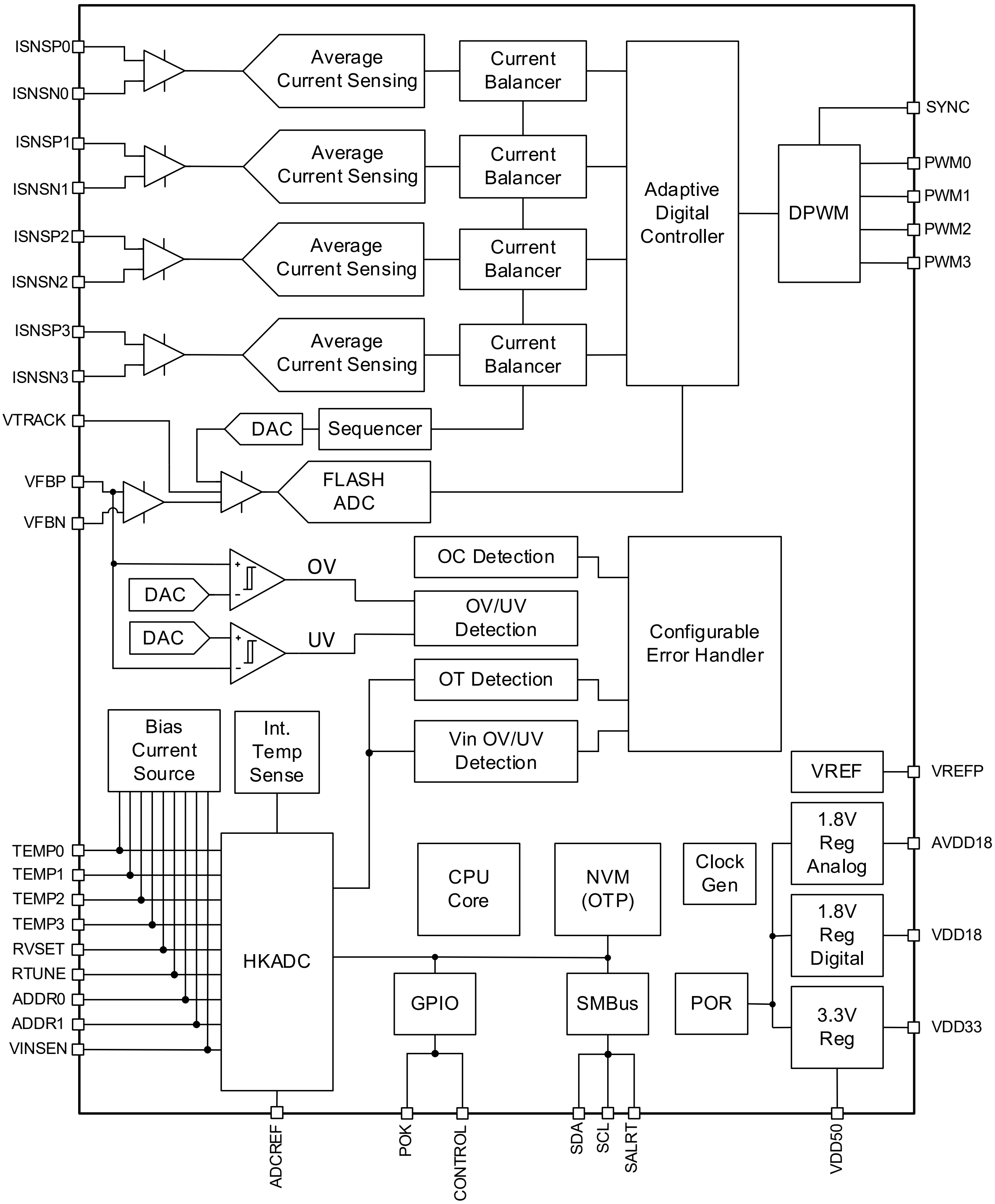


Figure 2: Functional Block Diagram

Functional Description

Overview

The ED8401 is a configurable true-digital scalable 4/3/2 phase single output PWM controller for high-current, non-isolated step down DC/DC supplies supporting switching frequencies up to 1MHz. It offers a PMBus™ configurable digital power control loop incorporating output voltage sensing and average inductor current sensing, bundled with extensive fault monitoring and handling options.

Several different functional units are incorporated in the device. This includes output voltage sensing, average inductor current sensing of all phases, current balancing of all phases, a digital control loop, and a digital pulse-width modulator (DPWM). In parallel, a dedicated, configurable error handler allows fast and flexible detection of error signals and their appropriate handling. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals, such as input voltage and temperature. An application-specific, low-energy microcontroller is used to control the overall system. It manages configuration of the various logic units and handles the PMBus™ communication protocol. A PMBus™/SMBus/I²C™ interface is incorporated to connect with the outside world; supported by control and power-good signals.

A high-reliability, high-temperature, One-Time-Programmable memory (OTP) is used to store configuration parameters. The flexibility for a partial OTP write is also available thus allowing a greater number of configurations to be written to the device. All required bias and reference voltages are internally derived from the external supply voltage.

The ED8401 also has two pin-strapping options giving the user the ability to set the output voltage and use a preconfigured compensator through connecting a predefined resistor to the RVSET and RTUNE pins. The controller also has a SYNC pin to allow synchronization of several controllers either through an externally applied signal or through a master-generated clock signal if in a master/slave configuration. The controller also has a VTRACK pin, allowing sequencing of the output voltage.

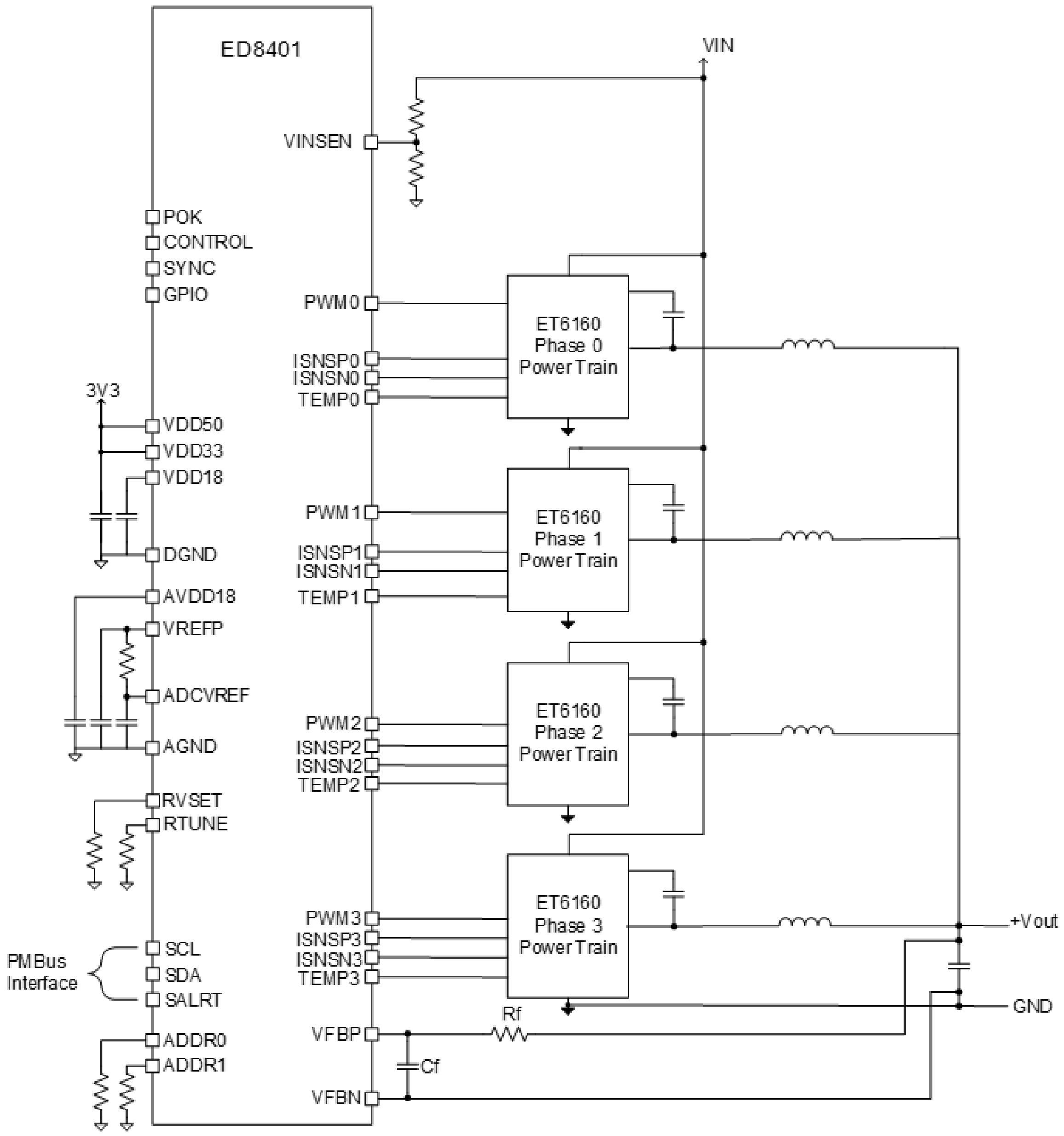


Figure 3: Typical Simplified Application Circuit with ET6160 Power Train utilizing ET6160 Internal Reference (with 3.3Vcc option for controller)

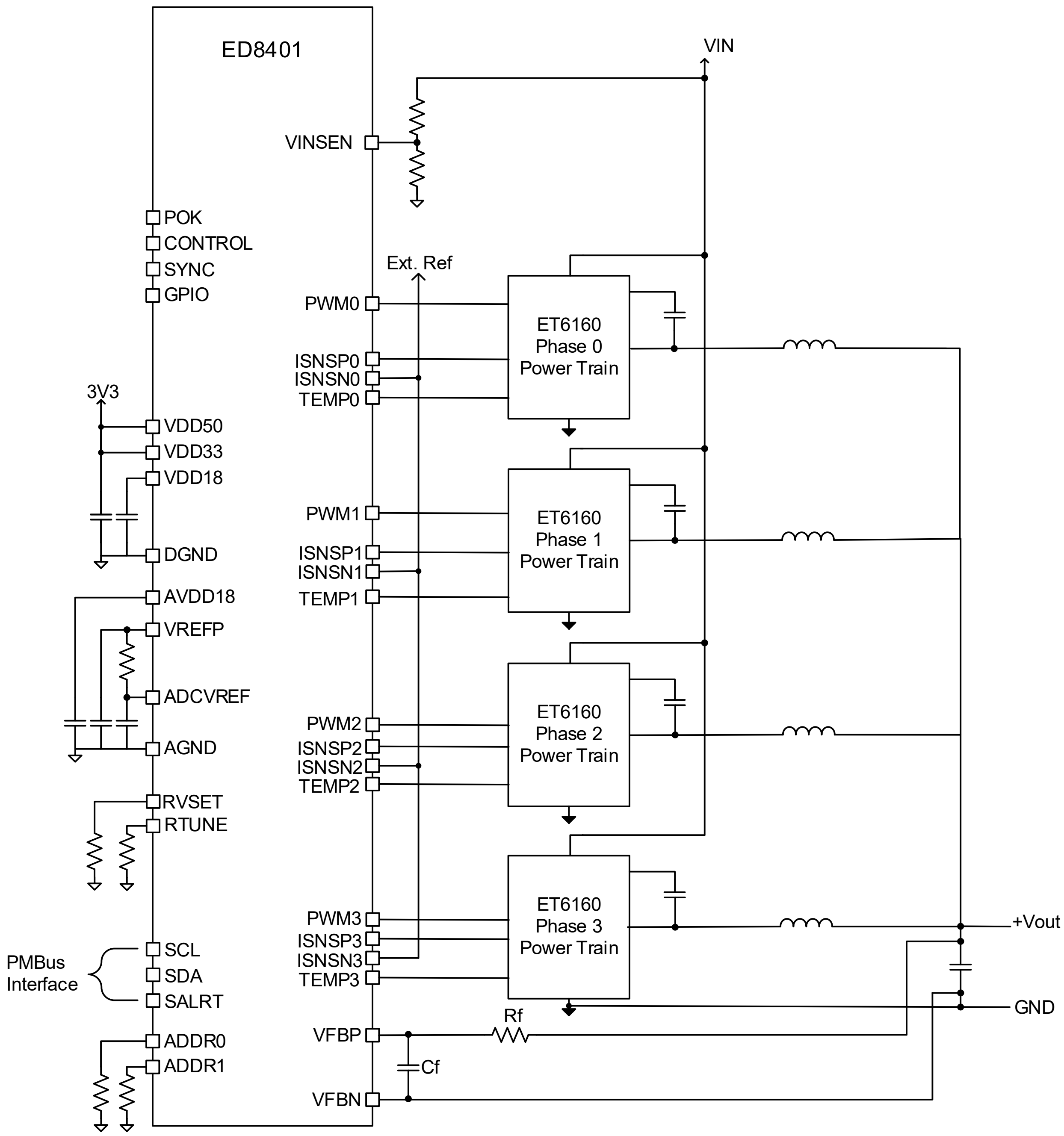


Figure 4: Typical Simplified Application Circuit with ET6160 Power Train utilizing an External Reference (with 3.3Vcc option for controller)

Digital Compensator

The sampled output voltage is processed by a digital control loop in order to modulate the DPWM output signals controlling the power stage. The advanced digital control loop works as a voltage-mode controller using a PID-type compensator. The basic structure of the controller is shown in Figure 5. The ED8401 controller features two parallel compensators for steady-state operation and fast transient operation. Fast, reliable switching between the different compensation modes ensures good transient performance and quiet steady state performance.

The ED8401 uses over-sampling techniques to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any changes in output voltage.

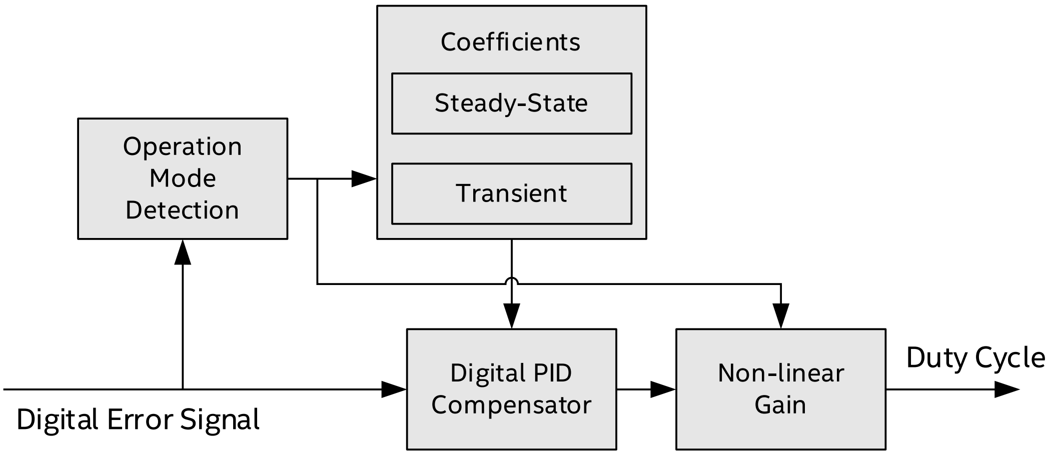


Figure 5: Simplified Block Diagram Of The Digital Compensation

Power Supply Circuitry, Reference Decoupling, and Grounding

The ED8401 incorporates several internal voltage regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5V or 3.3V depending on whether the internal 3.3V regulator is used. If the internal 3.3V regulator is not used, 3.3V must be supplied to VDD33 and VDD50 pins respectively. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0µF minimum; 4.7µF recommended). If the 5.0V supply voltage is used, i.e. the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example. The specified minimum capacitance must take into account temperature and voltage therefore a high-quality dielectric like X7R is recommend.

Table 5: Decoupling Capacitors

Pin #	Pin Name	Value	Note
2	VREFP	100nF	Required
36	VDD18	1µF (minimum)	Required
37	VDD33	1µF (minimum)	Required
38	VDD50	1µF(minimum)	Required
39	AVDD18	1µF (minimum)	Required
40	ADCVREF	100nF	Required
2,40	VREFP to ADCVREF	51Ω	Required

Three different ground connections are available on the outside of the package. These should be connected together to a single ground. A differentiation between analog and digital ground is not required.

The reference voltages required for the analog-to-digital converters are generated within the ED8401. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 100nF capacitor is required at the VREFP pin and a 100nF capacitor at ADCVREF pin. The two pins should be connected with approximately 50Ω resistance in order to provide sufficient decoupling between the pins.

POWER ON RESET

The ED8401 employs an internal power-on-reset (POR) circuit to ensure proper start-up and shut down with a changing supply voltage. Once the VDD33 supply voltage rises above the POR threshold voltage, the ED8401 begins the internal start-up process. Upon its completion, the device is ready for operation.

The power rail PVIN is monitored by VINSEN against programmable threshold to ensure proper power-up and to protect the power MOSFETs under various input power fault conditions.

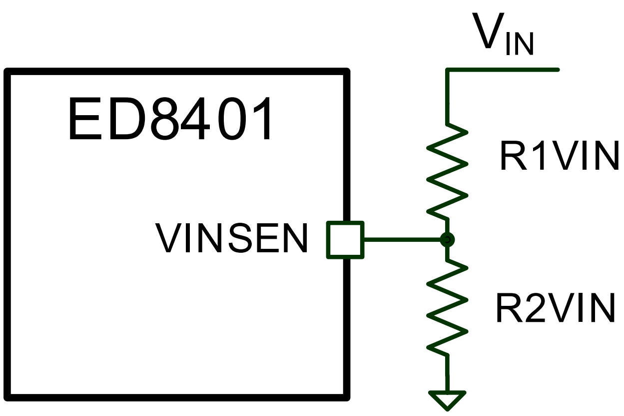


Figure 6: VIN Voltage sense components

The ED8401 also uses the VINSEN monitor for input voltage feed-forward, which eliminates variations in the output voltage due to sudden changes in the input voltage supply. It does this by immediately changing the duty cycle to compensate for the input supply variation by normalizing the DC gain of the loop. In a noisy application, a decoupling capacitor may be placed between VINSEN and GND to act as a filter to unwanted external noise.

Table 6: Input Voltage Sense Components

Nominal Input Voltage	Maximum Input Voltage	R1VIN	R2VIN
12V	17.25V	11kΩ	1kΩ
5	8.2V	4.7kΩ	1kΩ

PWM Output and CLOCK SYNCHRONIZATION

The ED8401 digital pulse width modulator (DPWM) has a resolution of 163ps and supports for tri-state capability.

The ED8401 PWM synchronization feature allows the user to synchronize the switching frequency of multiple devices.

The ED8401 SYNC functionality maybe configured as an input or an output using Intel's GUI software or via the manufacturer-specific PMBus command, MFR_PIN_CONFIG. The default configuration for synchronization control is OFF.

SETTING THE OUTPUT VOLTAGE

The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

The ED8401 supports direct output voltage feedback without external components up to an output voltage of 1.3V. However, adding a high-frequency low-pass filter into the sense path is highly recommended for removing high-frequency disturbances from the sense signals. Placing these components as close as possible to the controller is recommended.

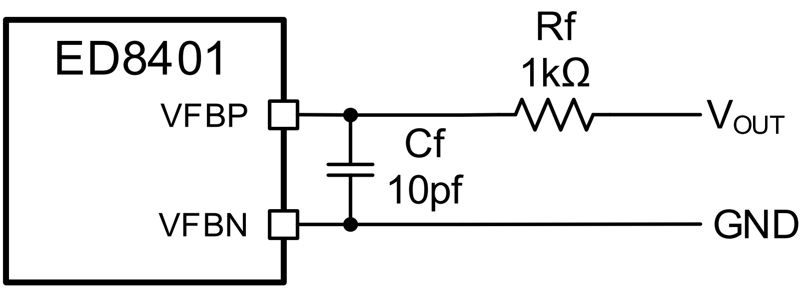


Figure 7: Vfb filter components

Although the reference DAC generates a voltage ≤1.44V, keeping the voltage on the feedback pin (VFBP) at approximately 1.3V max. is recommended to guarantee sufficient headroom.

Differential remote sensing provides for precise regulation at the point of load.

One of thirty output voltages may be selected in the default configuration, based on a resistor connected between the RVSET pin and GND. At power-up, an internal current source biases the resistor and the voltage is measured by an ADC to decode the Vout selection, through which VOUT is defined. Use Table 7 for the details of V_{OUT} selection and RVSET values.

Note: For 1MHz operation at output voltage <0.7V, high PVin values and light loads, pulse skipping will occur which may result in an increase in output ripple. This is due to the very narrow PWM outputs resulting from these conditions and the minimum pulse width accepted by the relevant Power Trian to ensure no cross conduction between the Top and Bottom MOSFET's.

Table 7: Supported Configuration Voltage Values for ED8401 Output Voltage

RVSET Resistor	V_{OUT}
0kΩ	Reserved
0.392kΩ	Reserved
0.576kΩ	1.3V
0.787kΩ	1.25V
1.000kΩ	1.2V
1.240kΩ	1.175V
1.500kΩ	1.15V
1.780kΩ	1.12V
2.100kΩ	1.1V
2.430kΩ	1.05V
2.800kΩ	1.03V
3.240kΩ	1.0V
3.740kΩ	0.975V
4.220kΩ	0.95V
4.750kΩ	0.92V
5.360kΩ	0.9V
6.040kΩ	0.89V
6.810kΩ	0.875V
7.680kΩ	0.85V
8.660kΩ	0.825V
9.530kΩ	0.8V
10.500kΩ	0.775V
11.800kΩ	0.75V
13.000kΩ	0.72V
14.300kΩ	0.7V
15.800kΩ	0.65V
17.400kΩ	0.6V
19.100kΩ	0.55V
21.000kΩ	0.52V
23.200kΩ	0.5V

ALTERNATIVE OUTPUT VOLTAGE CONTROL METHODS

In the default configuration, output voltage selection is determined at power-up by the pin-strapped resistor RVSET. This functionality can be disabled using the PMBus command MFR_PIN_CONFIG. When RVSET is disabled, the output voltage will be determined at start-up by the nominal output voltage setting in the user configuration.

The ED8401 supports a subset of the output voltage commands outlined in the PMBus specification. For example, the output voltage can be dynamically changed using the PMBus command VOUT_COMMAND. When the output is being changed by the PMBus command, POK remains at a high impedance.

POWER OK

The ED8401 has a Power OK indicator at its output pin POK, which is Open Drain and therefore requires a pull-up resistor. A 3.3kΩ Pull-Up resistor may be connected to the VDD33 pin. When de-asserted, POK indicates that the output voltage is below the threshold value, 90% of the programmed output voltage in the default configuration. When asserted, POK indicates that the output is in regulation, and no major faults are present. As a result, POK de-asserts during any serious fault condition where power conversion stops and re-asserts when the output voltage recovers.

In a noisy application, it is strongly recommended that a 100nf decoupling capacitor be placed between the POK pin and GND to act as a filter to unwanted external noise.

Control Pin

In the default configuration, the CTRL pin must be pulled high to enable operation and the PMBus command OPERATION is ignored. Through using the standard PMBus ON_OFF_CONFIG command, this behavior maybe be changed to active low, to using only the PMBus OPERATION command or a combination of both the PMBus operation command and the Control pin.

RTUNE - COMPENSATING THE DIGITAL CONTROL LOOP

To improve the transient performance for a typical point-of-load design, it is common to add output capacitance to the converter. This moves the output LC resonant frequency lower as capacitance increases which results in lower bandwidth, lower phase margin, and longer settling times unless the control loop is compensated for added capacitance.

However with the default configuration of the ED8401 the user can select from preconfigured PID control loop settings (known as compensators) using pin-strapping. A single resistor from the RTUNE pin to GND selects a pre-defined compensator for the EM8401 to use on power up.

The selection of the compensator is driven by switching frequency, output inductor and by the type of output capacitors used, as the ESL and ESR of different capacitor types demands different PID coefficients to optimize transient deviation and recovery characteristics. The default compensator is a design with a combination of ceramic and polymer capacitors, i.e. SP-CAP.

The five different compensators can then be subdivided into groups of six each whereby the initial base capacitance value in the appropriate compensator can be scaled by a factor M to align the actual output capacitance with the base value.

A user can design their own compensator, which may then be programed into the part in an available blank RTUNE compensator using either the GUI or over PMBus.

Table 8: RTUNE configuration table for ED8401P01 – 4-Phase – 500kHz – 120nH

Compensator Description	RTUNE Resistor (Using 1% tolerance or better resistor)	Multiplication factor (M) **COUT = BASE x M**	Typical Deviation with 80A Load Step	Typical Deviation with 60A Load Step	Typical Deviation with 40A Load Step
Polymer Aluminum (SP-CAP) and Ceramic MLCC Output Capacitors **Base capacitance** = 16 x 470µF (Polymer) + 16 x 100µF (Ceramic)	0kΩ	1	± 25mV	± 18mV	± 12mV
	0.392kΩ	0.25	--	--	± 45mV
	0.576kΩ	0.5	± 45mV	± 36mV	± 25mV
	0.787kΩ	0.75	± 32mV	± 25mV	± 18mV
	1.000kΩ	1.5	± 18mV	± 14mV	--
	1.240kΩ	2	± 15mV	± 12mV	--
Reserved for User Programmed Compensation Values	1.500kΩ				
	1.780kΩ				
	2.100kΩ				
	2.430kΩ				
	2.800kΩ				
	3.240kΩ				
	3.740kΩ				
	4.220kΩ				
	4.750kΩ				
	5.360kΩ				
	6.040kΩ				
	6.810kΩ				
	7.680kΩ				
	8.660kΩ				
	9.530kΩ				
	10.500kΩ				
	11.800kΩ				
	13.000kΩ				
	14.300kΩ				
	15.800kΩ				
	17.400kΩ				
	19.100kΩ				
	21.000kΩ				
	23.200kΩ				

Table 9: RTUNE configuration table for ED8401P03 – 3-Phase - 500kHz – 120nH

Compensator Description	RTUNE Resistor (Using 1% tolerance or better resistor)	Multiplication factor (M) **COUT = BASE x M**	Typical Deviation with 80A Load Step	Typical Deviation with 60A Load Step	Typical Deviation with 40A Load Step
Polymer Aluminum (SP-CAP) and Ceramic MLCC Output Capacitors **Base capacitance** = 6 x 470µF (Polymer) + 6 x 100µF (Ceramic)	0kΩ	1	± 45mV	± 34mV	± 25mV
	0.392kΩ	1.5	± 35mV	± 25mV	± 18mV
	0.576kΩ	2	± 27mV	± 19mV	± 12mV
	0.787kΩ	2.5	± 25mV	± 18mV	--
	1.000kΩ	3	± 22mV	± 17mV	--
	1.240kΩ	4	± 15mV	± 12mV	--
Reserved for User Programmed Compensation Values	1.500kΩ				
	1.780kΩ				
	2.100kΩ				
	2.430kΩ				
	2.800kΩ				
	3.240kΩ				
	3.740kΩ				
	4.220kΩ				
	4.750kΩ				
	5.360kΩ				
	6.040kΩ				
	6.810kΩ				
	7.680kΩ				
	8.660kΩ				
	9.530kΩ				
	10.500kΩ				
	11.800kΩ				
	13.000kΩ				
	14.300kΩ				
	15.800kΩ				
	17.400kΩ				
	19.100kΩ				
	21.000kΩ				
	23.200kΩ				

Table: RTUNE configuration table for ED8401P05 – 2-Phase - 500kHz – 120nH

Compensator Description	RTUNE Resistor (Using 1% tolerance or better resistor)	Multiplication factor (M) **COUT = BASE x M**	Typical Deviation with 40A Load Step	Typical Deviation with 30A Load Step	Typical Deviation with 20A Load Step
Polymer Aluminum (SP-CAP) and Ceramic MLCC Output Capacitors **Base capacitance** = 4 x 470µF (Polymer) + 4 x 100µF (Ceramic)	0kΩ	1	± 45mV	± 36mV	± 25mV
	0.392kΩ	1.5	± 37mV	± 27mV	± 21mV
	0.576kΩ	2	± 28mV	± 22mV	± 15mV
	0.787kΩ	2.5	± 25mV	± 20mV	--
	1.000kΩ	3	± 21mV	± 18mV	--
	1.240kΩ	4	± 15mV	± 13mV	--
Reserved for User Programmed Compensation Values	1.500kΩ				
	1.780kΩ				
	2.100kΩ				
	2.430kΩ				
	2.800kΩ				
	3.240kΩ				
	3.740kΩ				
	4.220kΩ				
	4.750kΩ				
	5.360kΩ				
	6.040kΩ				
	6.810kΩ				
	7.680kΩ				
	8.660kΩ				
	9.530kΩ				
	10.500kΩ				
	11.800kΩ				
	13.000kΩ				
	14.300kΩ				
	15.800kΩ				
	17.400kΩ				
	19.100kΩ				
	21.000kΩ				
	23.200kΩ				

Note: In the case of 3 phase and 2 phase scenarios, the base capacitance suggestions (6x470uF + 6x100uF for 3 phase and 4x470uF + 4x100uF for 2 phase) may result in higher steady state ripple because of lower ceramic capacitor count. In order to keep the steady state output ripple within acceptable typical level (of ≤ 10mV), it is recommended to add additional ceramic capacitors (100uF) as needed (based on layout, component derating etc.).

Power Train Selection

The ED8401 and ET6160 have been designed together to provide an overall optimized system solution allowing for flexibility in terms of performance and layout. With this there are two options to connect the IMON related signals between the Power Train and Controllers (See simplified system diagrams 3 & 4)

> Connect IMON and IMONREF pins of the ET6160 directly to the respective ISNSPx and ISNSNx pins of the ED8401
>
> Connect IMON pin of the ET6160 directly to ISNSPx pins of the ED8401 and connect External reference voltage to all ED8401ISNSNx pins

(Please see respective simplified system diagrams 3 & 4, located on pages 18 & 19)

OUTPUT INDUCTOR RECOMMENDATION

The ED8401P01 comes with a switching frequency default of 500kHz switching frequency

An inductor with a DC resistance (DCR) not greater than 0.35mΩ should be selected

The Output inductor should be sized to ensure it can support the required output current including ripple current under all conditions. In the table below are some recommend options for output current towards the higher end, other components may be used.

Table 10: Output Inductor Options

Description	Manufacturer	P/N
120nH, 0.145mΩ, 78A, 9.6mmx6.4mmx10.1mm	ITG	AH3740A-120K
120nH, 0.18mΩ, 70A, 10mmx7mmx8.3mm	TDK	VLBS1007083T-R12L

OUTPUT CAPACITOR RECOMMENDATION

ED8401 is designed for fast transient response and low output ripple. The output capacitors should be a mix of low ESR polymer and ceramic capacitors. With the RTUNE feature, the user can simply scale up the total output capacitance to meet further stringent transient requirement.

Please consult the documentation for your particular FPGA, ASIC, processor, or memory block for the transient and the bulk decoupling capacitor requirements.

Table 11: Recommended Output Capacitors

Description	Manufacturer	P/N
470µF, 2.5V, ESR 3mΩ SP-CAP	Panasonic	EEFGX0E471R
100µF, 6.3V, X5R, 1206 Ceramic	Kemet	C1206C107M9PACTU

PROTECTION FEATURES AND FAULT RESPONSE

The ED8401 monitors various signals during operation to provide a complete suite of programmable fault warnings and protections. Measured and filtered signals are compared to a configurable set of warnings and fault thresholds. In typical usage, a warning sets a status flag, but does not trigger a response; whereas a fault sets a status flag and generates a response. The assertion of the SMBALERT signal can be configured to individual application requirements.

The ED8401 supports different response types depending on the fault detected. A “Soft-Off” response ramps the output voltage down using the falling-edge sequencer setting (TOFF_FALL). The “low-impedance” response immediately turns off the top MOSFET and enables the low-side MOSFET. The “high-impedance” response immediately turns off both the top MOSFET and low-side MOSFET.

In the default configuration, the ED8401 responds to an over temperature event by ramping down V_{OUT} in a controlled manner at a slew rate defined by the T_{OFF_FALL} value. This response type is termed “Soft-Off”. The final state of the output signals depends on the value selected for V_{OFFnom}.

For all other faults the ED8401 will respond by immediately turning off both the top-side MOSFET and low-side MOSFET. This response type is termed “High-Impedance”.

For each fault response, a delay and a retry setting can be configured. If the delay-to-fault value is set to non-zero, the ED8401 will not respond to a fault immediately. Instead it will delay the response by the configured value and then reassesses the signal. If the fault remains present during the delay time, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded.

If the delay-to-retry value is set to non-zero, the ED8401 will not attempt to restart immediately after fault detection. Instead it will delay the restart by the configured value. If the fault is still present when attempting to restart, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded. If the delay-to-fault is a non-zero value, then the delay-to-retry value will be a factor of 100 times greater than the delay-to-fault value.

The retry setting, i.e. the number of ED8401 restarts after a fault event, can be configured. This number can be between zero and six. A setting of seven represents infinite retry operation. This setting is commonly known as “Hiccup Mode.”

The default fault response is zero delay and latch off for most fault conditions. The CTRL pin may be cycled to clear the latch. Table 12 summarizes the default configurations that have been pre-programmed to the device.

Table 12: Fault Configuration Overview

Signal	Fault Level	Default Response Type	Retries#	Default Delay to Fault	Delay Resolution for Setting for Delay to Fault*	Maximum Delay to Fault*
Output Over-Voltage	Warning				1.5µs or 15µs	0.327ms or 3.27ms
	Fault	High-impedance	None	0		
Output Under-Voltage	Warning				1.5µs or 15µs	0.327ms or 3.27ms
	Fault	High-impedance	None	0		
Input Over-Voltage	Warning				1.5µs or 15µs	0.327ms or 3.27ms
	Fault	High-impedance	None	0		
Input Under-Voltage	Warning				1.5µs or 15µs	0.327ms or 3.27ms
	Fault	High-impedance	Infinite	0		
Over-Current	Warning				1.5µs or 15µs	0.327ms or 3.27ms
	Fault	High-impedance	None	0		
Controller Over-Temperature	Warning				5ms	900ms
	Fault	Soft Off	Infinite	0		
Power Train Over-Temperature	Warning				5ms	900ms
	Fault	Soft Off	Infinite	0		

*For voltage and current signals, the resolution (step size) of 1.5µs applies up to a maximum delay time value of 327µs. For a delay time exceeding 327µs, the step size increases to 15µs and the maximum delay time increases to 3.27ms

for retires the delay to retry time can be programed also as per the delay to faults however the retry times are scaled to be 100 greater than Delay to Fault times

Fault Response Types

The controller supports several fault Response types

High Impedance: Places the PWM outputs into tristate condition immediately

Low: Places the PWM outputs into a low state immediately. This allow VOUT to be pull low through the low Side MOSFET very rapidly

Soft Off: This ramps VOUT down as programmed by the sequencer

PVin Protection

Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored.

The ED8401 monitors the input voltage at VINSEN continuously against a number of configurable thresholds. If the input voltage exceeds the over voltage threshold or is below the under-voltage threshold, the default response is generated.

As well as OVP and UVP warning and protection limits, there are also programmable VIN On and OFF Levels. Until the Vin On threshold is exceeded the controller will not allow Vout to be enabled and will report a fault as a Low Input Voltage Fault.

If the VIN Off level is crossed the PWM will disable Vout however in a controlled manner i.e. soft off. In the event of a very fast falling VIN and falling below the UVP threshold thereby a UVP fault occurring this will result in controller disabling Vout immediately by putting the PWM into a high impedance state.

Vout Protection

To prevent damage to the load, the ED8401 utilizes both separate over-voltage and under-voltage protection circuits for VOUT. The voltage at VFBP is continuously compared with a configurable threshold using two high-speed analog comparators. If the voltage falls or rises above the configured thresholds, a fault response is generated and the PWM output is turned off.

Using an ADC, the ED8401 also monitors the output voltage against two thresholds, under voltage warning and over voltage warning. For example, if the output voltage is below the under-voltage warning level and above the under-voltage fault level, an output voltage under-voltage warning is triggered. If the output voltage falls below the fault level, a fault event is generated.

Over Current Protection

A dedicated ADC is used to provide fast and accurate current information during the entire switching period to provide fast Over-Current Protection (OCP) response. If the output current crosses the programmed OCP threshold then the controller will turn off all PWM outputs by placing them into tri-state (high Impedance State. In the default configuration user intervention is required to reenable the output by toggling the control pin (in the controller default configuration)

Over Temperature Protection

Over Temperature Protection (OTP) is supported through direct monitoring of both the controller's internal temperature and the external Power Train temperatures. If the temperature exceeds either OTP thresholds, the device will enter a soft-stop mode slowly ramping the output voltage down until the temperature falls below the default recovery temperature. Once the temperature falls below the temperature on level the controller will automatically restart the output with the default configuration settings. The Temperature on level is set to 100ºC in the default configuration for both controller and Power Trains however they are both independently configurable though the appropriate PMBus commands

Power Train Fault Indicator Detection

Modern Power trains utilize the Temperature monitor output to signal the controller of a fault event having occurred within the Power Train. It does this by pulling the Temperature level to a high voltage typically around 3V.

To support this functionality within the ED8401 each temperature input has an analog comparator which is used to detect when the TMON signal crosses a defined threshold (approx. 2.25V) which is then deemed to be a Power Train Fault. When a Power Train Fault is detected the controller in its default configuration will immediately disable the output and place each PWM output into tri-state The fault status of each Power Train can be checked using the PMBus command MFR_STATUS_EXT

An additional check on the Power Train is upon the application of power to Power Train, a Vcc fault with regards to a Power Train is also communicated to the controller through the Temperature monitoring pin being held low. After initialization and prior to enabling the PWM outputs, the ED8401 monitors each Temperature pin and if the measured voltage is low the controller will not enable the output but will indicate a fault.

This FAULT response maybe changed using the PMBus commands MFR_TEMPx_FAULT_RESPONSE and the MFR_FAULT_RESPONSE command for the PWM.

Individual Power Train Failure

The ED8401 monitors the PWM output of each phase to prevent damage in the event of an unexpected power train failure. If any of the individual PWM outputs, increases above a programmable threshold in a single switching cycle, a Current Balanced Fault event is deemed to have occurred and the controller disables all PWM outputs.

If any of the power trains fail outright and therefore unable to notify the controller via its corresponding Temperature pin or IMON signal, the controller's current balance controller could extend the PWM's of the remaining Power Trains immediately to maintain current balance and this may result in damage to the remaining Power Trains. The protection mechanism prevents this form occurring.

Because the power Train fail detector monitors the duty cycle of each Phase this allows for a very fast response, the controller disables VOUT once the duty cycle exceeds the programmed limit. status of each Power Train can be checked using the PMBus command MFR_STATUS_EXT and the Current Balance controller maximum PWM protection level can be changed using the PMBus Command MFR_CBC_POS_LIMIT.

Production and Test Aids

VFBP & VFBN protection

In-built within ED8401 are protection circuits to ensure that neither voltage sense lines VFBP & VFBN are open at power up. If either or both are detected to be open during initialization (the application of power to VCC), it is detected as a fault, the output will not be enabled. The fault will be signaled through the PMBus command STATUS_MFR_SPECIFIC with B[0] VFBP Open Circuit & B[0] VFBN Open Circuit

RTUNE and RVSET resistor value

Two separate PMBus commands related to RVSET and RTUNE are included in the PMBus list of supported commands within the ED8401 to ensure the correct resistor values are used or that is no manufacturing issues such as a short, open or incorrect value being placed for example.

The PMBus Command MFR_RTUNE when issued return the PMBus value index related to RTUNE. The user can use this to check the value return matches the intended value prior to the initial power up.

The PMBus Command MFR_RVSET when issued return the PMBus value index related to RTUNE. The user can use this t check the value return matches the intended value prior to the initial power up.

Improving Externally Temperature accuracy

The ED8401 supports the calibration of each of the external Temperature Sensors using the PMBus command MFR_EXT_TEMP_CAL_OFFSET (0xE1).

This allows any offset in the TMON of the individual Power Trains to be corrected for once the known temperature is available.

FUNCTIONAL DESCRIPTION: ADVANCED CONFIGURATION

The various ED8401 controllers are delivered with a pre-programmed default configuration, allowing the user to power up without a need to configure the device or even the need for the GUI to be connected. However, a PMBus version 1.2 compliant interface allows access to an extensive suite of digital communication and control commands. This includes configuring the ED8401 for optimum performance, setting various parameters such as output voltage, and monitoring and reporting device behavior including output voltage, output current, and fault responses.

Also the device may be reconfigured multiple times without storing the configuration into the non-volatile memory (NVM). Any configuration changes will be lost upon power-on reset unless specifically stored into NVM using either STORE_DEFAULT_ALL or STORE_DEFAULT_CODE PMBus commands. Please see **Table 17** for more details.

For existing compensation parameter, RVSET and RTUNE table parameters, there is no reprogramming of existing values permitted, only blank locations may be used.

The NVM configuration can be stored seven times in its entirety. However, the consumption of the available NVM is dynamic, based on the configuration parameters that have actually changed. The unused NVM information is given in the GUI or through the manufacture specific command MFR_STORE_PARAMS_REMAINING.

INTEL DIGITAL POWER CONFIGURATOR

The Intel Enpirion Digital Power Configurator is a Graphical User Interface (GUI) software which allows the ED8401 to be controlled via a USB interface to a host computer.

The user can view the power supply's status, I/O voltages, output current and fault conditions detected by the device, program settings to the converter, and issue PMBus commands using the GUI. Most of the parameters (for example, VOUT turn on/off time, protection and fault limits) can be configured and adjusted within the GUI environment. These parameters can also be configured outside of the GUI environment using the relevant PMBus™ commands.

The GUI also allows the user to easily create, modify, test and save a configuration file which may then be used to permanently burn the configuration into NVM within a production test environment.

For greater information on the GUI please refer to the GUI User Guide.

ENABLE, OUTPUT START-UP BEHAVIOR AND POWER SEQUENCING

Three different configuration options are supported to enable the output voltage. The device can be configured to turn on after an OPERATION_ON command, via the assertion of the CTRL pin or a combination of both per the PMBus convention. The ED8401 supports power sequencing features including programmable ramp up/down and delays. The typical sequence of events is shown in Figure 8 and follows the PMBus standard. The individual timing values shown in Figure 8 and Figure 9 can be configured using the appropriate configuration setting in Intel Digital Power Configurator GUI.

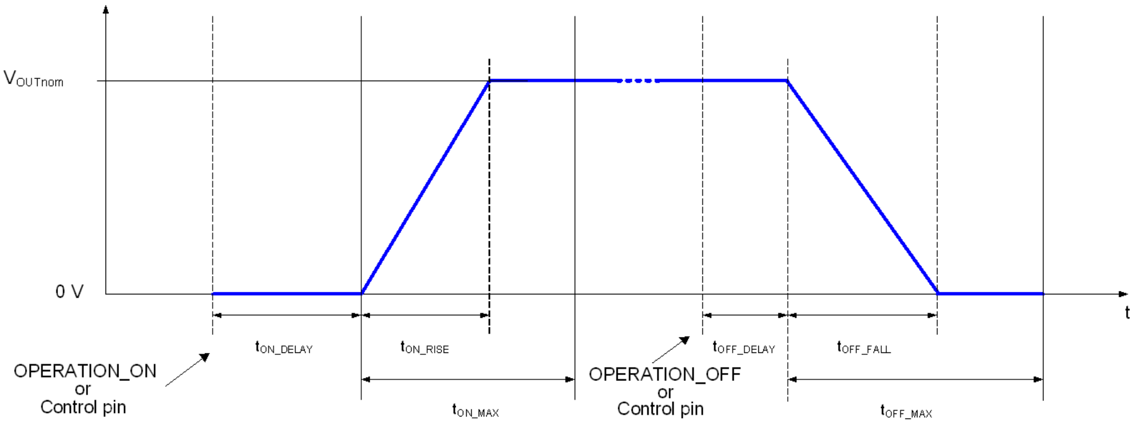


Figure 8: Power Sequencing

Table 13: ED8401 Default Sequencer Values (Programmable)

PARAMETER	Note	Value	UNITS
TON_DELAY		0	ms
TOFF_DELAY		0	ms
TON_RISE		1	V/ms
TOFF_FALL		1	V/ms
TON_MAX		2	ms
TOFF_MAX		2	ms
VOUT OFF	PMBus Command = MFR_VOUT_OFF (0xE0)	0	V

PRE-BIASED START-UP AND SOFT-STOP

In systems with complex power architectures, there may be leakage paths from one supply domain which may charge capacitors in another supply domain, leading to a pre-biased condition on one or more power supplies. This condition is not ideal and can be avoided through careful design, but is generally not harmful. Attempting to discharge the pre-bias is not advised as it may force high current though the leakage path. The ED8401 includes features to enable and disable into pre-biased output capacitors.

If the output capacitors are pre-biased when the ED8401 is enabled, start-up logic in the ED8401 ensures that the output does not pull down the pre-biased voltage and the t_{ON_RISE} timing is preserved. Closed-loop stability is ensured during the entire start-up sequence under all pre-bias conditions.

The ED8401 also supports pre-biased off, in which the output voltage ramp down to a user-defined level (PMBus command : V_{OFF_nom}) rather than to zero. After receiving the disable command, via PMBus command or the CTRL pin, the ED8401 ramps down the output voltage to the predefined value. Once the value is reached, the output driver goes into a tristate mode to avoid excessive currents through the leakage path.

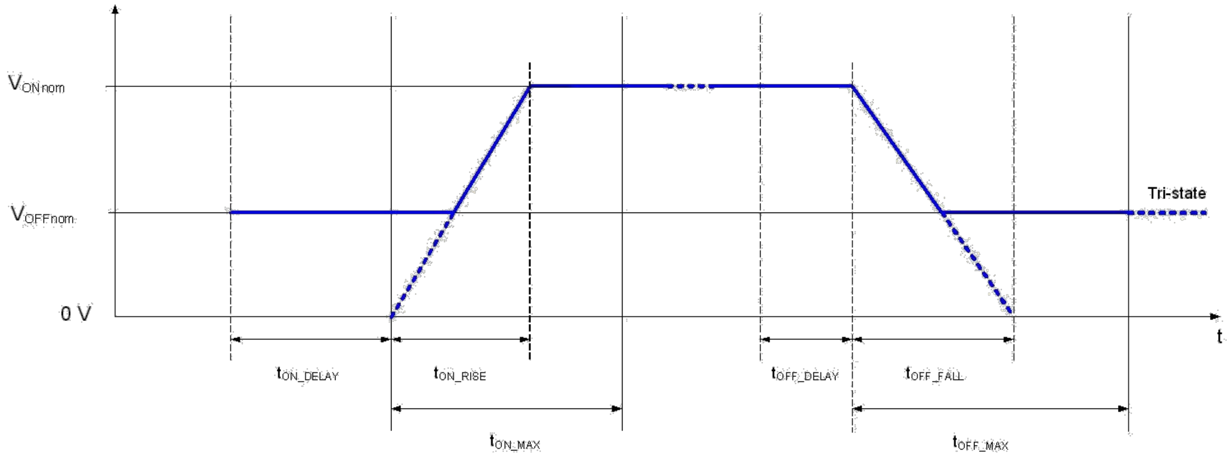


Figure 9: Power Sequencing With Non-Zero Off Voltage

VOLTAGE TRACKING

The ED8401 can control the output voltage based on the external voltage applied to the VTRACK pin, thus allowing sequencing of the output voltage from an external source. Pre-bias situations are also supported. The VTRACK pin voltage is a single-ended input referenced to analog ground. Tracking mode is disabled by default, but it can be enabled using the GUI software or via the manufacturer-specific PMBus command, MFR_FEATURES_CTRL (see **Table 17**).

If VTRACK is not intended to be used, tie the VTRACK pin low or leave it floating.

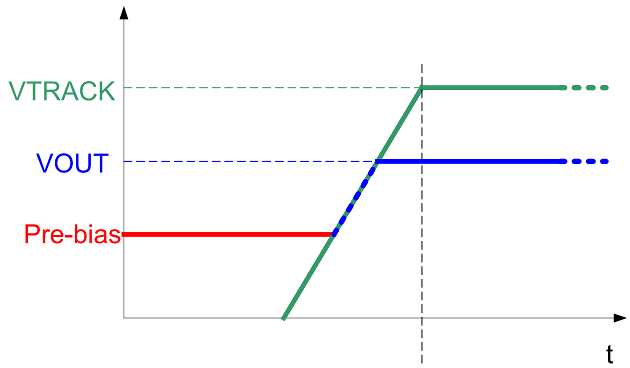


Figure 10: Power Sequencing Using VTRACK With Bias Voltage On VOUT

The set point voltage for the ED8401 is defined by the lower value of the V_{OUT} setting or an external voltage applied to the VTRACK pin. If the VTRACK voltage rises above the V_{OUT} set point voltage, then the final output voltage will be limited by the V_{OUT} setting. If the tracking feature is enabled, but the VTRACK pin is tied low or floating, then the output will never start as the VTRACK pin input is always the lower value and will always be in control. Conversely, if tracking is enabled, but VTRACK is tied high, the output will start but will follow the V_{OUT} set point, not the VTRACK pin.

If tracking is used for sequencing, it is recommended that the VTRACK signal be kept greater than the V_{OUT} voltage. This ensures that the internal V_{OUT} set point is used as the final steady-state output voltage and accuracy is not a function of the externally applied VTRACK voltage. The tracking function will override a programmed pre-bias off level (V_{OFF_nom}).

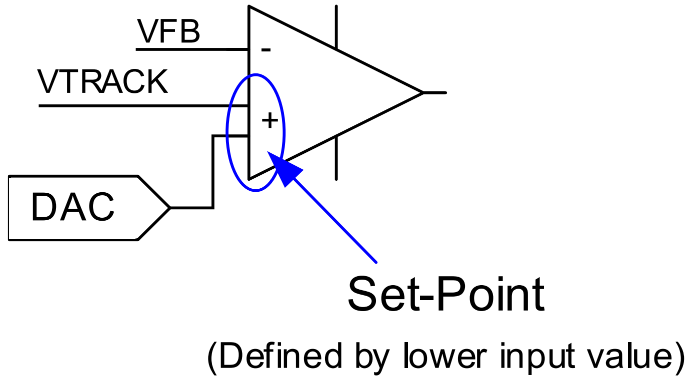


Figure 11: **VTRACK Circuitry**

The following figures demonstrate ratio-metric and simultaneous sequencing of the output voltage, which can be accomplished by applying an appropriate external voltage on the VTRACK pin. When using the VTRACK feature, the sequencing will be ratio-metric as shown in Figure 14, if an external resistor network is used at the VTRACK pin as shown in Figure 12. If no external resistors are used, the output sequence is simultaneous as shown in Figure 15.

In the event that the tracking voltage applied to VTRACK is greater than 1.4V, then a 2kΩ resistor is required in series with the VTRACK pin to minimize leakage current as shown in Figure 13.

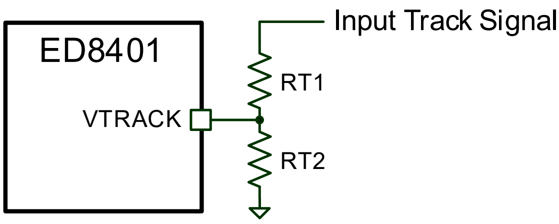


Figure 12: VTRACK Sense Circuitry with Resistor Divider

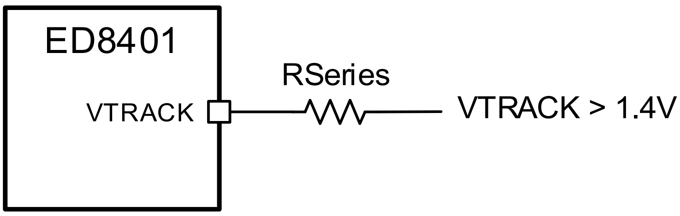


Figure 13: VTRACK Sense Circuitry (Input > 1.4V)

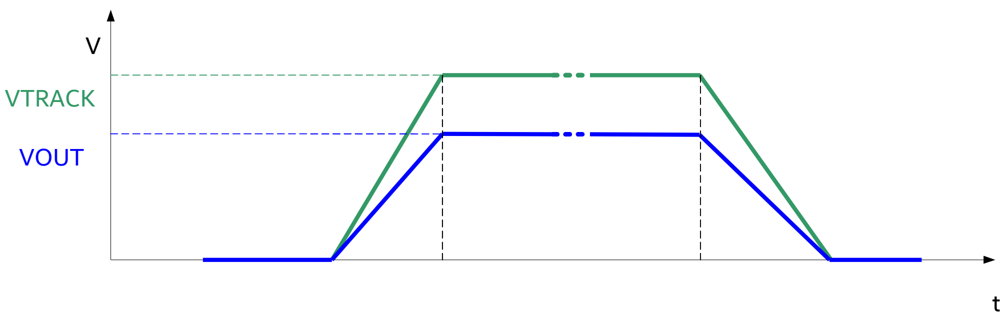


Figure 14: Ratiometric Sequencing Using VTRACK

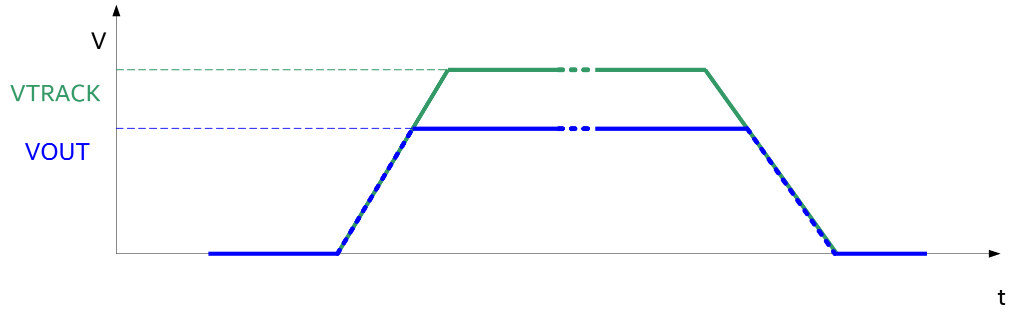


Figure 15: Simultaneous Sequencing Using VTRACK

TEMPERATURE MEASUREMENT

The ED8401 temperature sense block provides the device and the system with precision temperature information over a wide range of temperatures (-40°C to +150°C). The temperature sense block measures both the digital controller's temperature and up to four external Power Train temperatures. The ED8401 supports temperature telemetry and reporting through the standardized PMBus commands, READ_TEMPERATURE_1 is mapped to the Power Trains die temperatures and READ_TEMPERATURE_2 is mapped to the controller die temperature.

SMBAlert Pin

The SMBAlert pin is intended to operate using an external pull-up voltage of 3.3V and contains a weak internal pull-up.

If operating in applications with a lower voltage pull-up voltage, it is recommended that an external low Vf Schottky diode be placed at the input to localise this voltage.

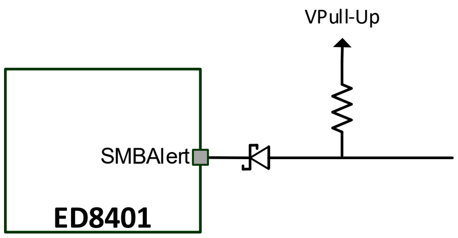


Figure 16: SMBAlert Pin Low Voltage Pull-up Option

Table 14: Schottky Diode Options

Description	Manufacturer	P/N
40V, 300mA, Schottky, SOD523	ST	BAT54KFILM
40V, 250mA, Schottky, SOD523	Diode Inc	BAT64T5Q

PMBus Functionality

INTRODUCTION

The ED8401 supports the PMBus protocol (version 1.2) to enable the use of configuration, monitoring, and fault management features during run-time.

The PMBus host controller is connected to the ED8401 via the PMBus pins (SDA, SCL). A dedicated SMBALERT pin is provided to notify the host that new status information is present.

The ED8401 supports packet error correction (PEC) according to the PMBus™ specification.

The ED8401 supports more than 60 PMBus commands in addition to several manufacturer specific commands related to output voltage, faults, telemetry, and more.

The ED8401 provides a PMBus set of synchronous communication lines, with serial clock input (SCL), serial data I/O (SDA), and serial alarm output (SALRT) pins.

The communication lines provide 1.8V I/O compatibility and open-drain outputs (SDA, SCL and SALRT). The communication lines require external pull-up resistors; typical applications require pull-up resistors on each end of the communication lines (typically values of 10 kΩ each), connected to VDD33 or an alternative termination voltage. Please refer to the PMBus specification (www.pmbus.org) for full details.

The ED8401 provides configurable behavior for the SALRT pin to allow users to determine which fault or warning conditions to communicate over the SALRT line. The default behavior of the controller ensures that any fault or warning results in the ED8401 SALRT pin going low; the alert behavior is enabled for all faults and warnings. You can deselect any of the faults or warnings so when one of these conditions occur, the SALRT pin is not pulled low.

Remote measurement and reporting of telemetry information at the power supply level provides feedback on key parameters such as voltages, current levels, temperature, and energy, and allows reporting of information such as faults and warning flags. With this information, data is collected and analyzed while the power supply is in development, such as in the qualification or verification phases, or in the field, and system level interaction such as power capping is implemented. Several telemetry parameters are supported by standard PMBus commands.

The ED8401 supports the LINEAR data format according to the PMBus specification. Note that in accordance with the PMBus specification, all commands related to the output voltage are subject to the VOUT_MODE settings.

A detailed description of the supported PMBus commands supported by the ED8401 can be found in ED8401 *Application Note – PMBus Commands Guide.*

TIMING AND BUS SPECIFICATION

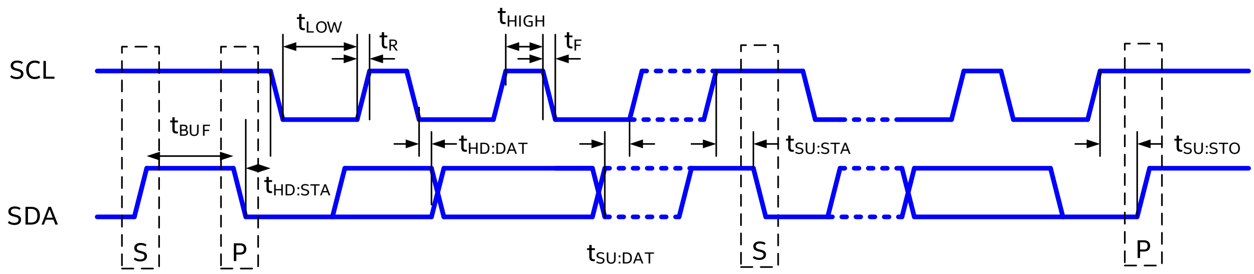


Figure 17: PMBus Timing Diagram

Table 15: ED8401 PMBus Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PMBus operation frequency	f_{SMB}		10	100	400	kHz
Bus free time between start and stop	t_{BUF}		1.3			µs
Hold time after start condition	$t_{HD:STA}$		0.6			µs
Repeat start condition setup time	$t_{SU:STA}$		0.6			µs
Stop condition setup time	$t_{SU:STO}$		0.6			µs
Data hold time	$t_{HD:DAT}$		300			ns
Data setup time	$t_{SU:DAT}$		100			ns
Clock low time-out	$t_{TIMEOUT}$			25	35	ms
Clock low period	t_{LOW}		1.3			µs
Clock high period	t_{HIGH}		0.6			µs
Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
Clock or data fall time	t_F				300	ns
Clock or data rise time	t_R				300	ns

ADDRESS SELECTION VIA EXTERNAL RESISTORS

The PMBus protocol uses a 7-bit device address to identify different devices connected to the bus. This address can be selected via external resistors connected to the ADDRx pins.

The resistor values are sensed using the internal ADC during the initialization phase and the appropriate PMBus address is selected. Note that the respective circuitry is only active during the initialization phase; hence no DC voltage can be measured at the pins. The supported PMBus addresses and the values of the respective required resistors are listed in Table 16.

Table 16: Supported Resistor Values For PMBus Address Selection

Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω
0x40	0	0	0x2B	1.2 k	12 k	0x56	3.9 k	4.7 k
0x01*	0	680	0x2C	1.2 k	15 k	0x57	3.9 k	5.6 k

Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω
0x02*	0	1.2 k	0x2D	1.2 k	18 k	0x58	3.9 k	6.8 k
0x03*	0	1.8 k	0x2E	1.2 k	22 k	0x59	3.9 k	8.2 k
0x04*	0	2.7 k	0x2F	1.2 k	27 k	0x5A	3.9 k	10 k
0x05*	0	3.9 k	0x30	1.8 k	0	0x5B	3.9 k	12 k
0x06*	0	4.7 k	0x31	1.8 k	680	0x5C	3.9 k	15 k
0x07*	0	5.6 k	0x32	1.8 k	1.2 k	0x5D	3.9 k	18 k
0x08*	0	6.8 k	0x33	1.8 k	1.8 k	0x5E	3.9 k	22 k
0x09	0	8.2 k	0x34	1.8 k	2.7 k	0x5F	3.9 k	27 k
0x0A	0	10 k	0x35	1.8 k	3.9 k	0x60	4.7 k	0
0x0B	0	12 k	0x36	1.8 k	4.7 k	0x61*	4.7 k	680
0x0C*	0	15 k	0x37*	1.8 k	5.6 k	0x62	4.7 k	1.2 k
0x0D	0	18 k	0x38	1.8 k	6.8 k	0x63	4.7 k	1.8 k
0x0E	0	22 k	0x39	1.8 k	8.2 k	0x64	4.7 k	2.7 k
0x0F	0	27 k	0x3A	1.8 k	10 k	0x65	4.7 k	3.9 k
0x10	680	0	0x3B	1.8 k	12 k	0x66	4.7 k	4.7 k
0x11	680	680	0x3C	1.8 k	15 k	0x67	4.7 k	5.6 k
0x12	680	1.2 k	0x3D	1.8 k	18 k	0x68	4.7 k	6.8 k
0x13	680	1.8 k	0x3E	1.8 k	22 k	0x69	4.7 k	8.2 k
0x14	680	2.7 k	0x3F	1.8 k	27 k	0x6A	4.7 k	10 k
0x15	680	3.9 k	0x40	2.7 k	0	0x6B	4.7 k	12 k
0x16	680	4.7 k	0x41	2.7 k	680	0x6C	4.7 k	15 k
0x17	680	5.6 k	0x42	2.7 k	1.2 k	0x6D	4.7 k	18 k
0x18	680	6.8 k	0x43	2.7 k	1.8 k	0x6E	4.7 k	22 k
0x19	680	8.2 k	0x44	2.7 k	2.7 k	0x6F	4.7 k	27 k
0x1A	680	10 k	0x45	2.7 k	3.9 k	0x70	5.6 k	0
0x1B	680	12 k	0x46	2.7 k	4.7 k	0x71	5.6 k	680
0x1C	680	15 k	0x47	2.7 k	5.6 k	0x72	5.6 k	1.2 k
0x1D	680	18 k	0x48	2.7 k	6.8 k	0x73	5.6 k	1.8 k
0x1E	680	22 k	0x49	2.7 k	8.2 k	0x74	5.6 k	2.7 k
0x1F	680	27 k	0x4A	2.7 k	10 k	0x75	5.6 k	3.9 k
0x20	1.2 k	0	0x4B	2.7 k	12 k	0x76	5.6 k	4.7 k
0x21	1.2 k	680	0x4C	2.7 k	15 k	0x77	5.6 k	5.6 k
0x22	1.2 k	1.2 k	0x4D	2.7 k	18 k	0x78*	5.6 k	6.8 k
0x23	1.2 k	1.8 k	0x4E	2.7 k	22 k	0x79*	5.6 k	8.2 k
0x24	1.2 k	2.7 k	0x4F	2.7 k	27 k	0x7A*	5.6 k	10 k
0x25	1.2 k	3.9 k	0x50	3.9 k	0	0x7B*	5.6 k	12 k
0x26	1.2 k	4.7 k	0x51	3.9 k	680	0x7C*	5.6 k	15 k

Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω	Address (hex)	ADDR1 Ω	ADDR0 Ω
0x27	1.2 k	5.6 k	0x52	3.9 k	1.2 k	0x7D*	5.6 k	18 k
0x28*	1.2 k	6.8 k	0x53	3.9 k	1.8 k	0x7E*	5.6 k	22 k
0x29	1.2 k	8.2 k	0x54	3.9 k	2.7 k	0x7F*	5.6 k	27 k
0x2A	1.2 k	10 k	0x55	3.9 k	3.9 k			

Note 2: The gray-highlighted addresses with an asterisk are reserved by the SMBus specification.

Clock Stretching

The SMBus specification allows devices to slow down the bus by periodically extending the clock low interval which then allows devices of different speeds to co-exist on the same bus.

The ED8401 family utilizes clock stretching for communications and with this the PMBus master must support clock stretching.

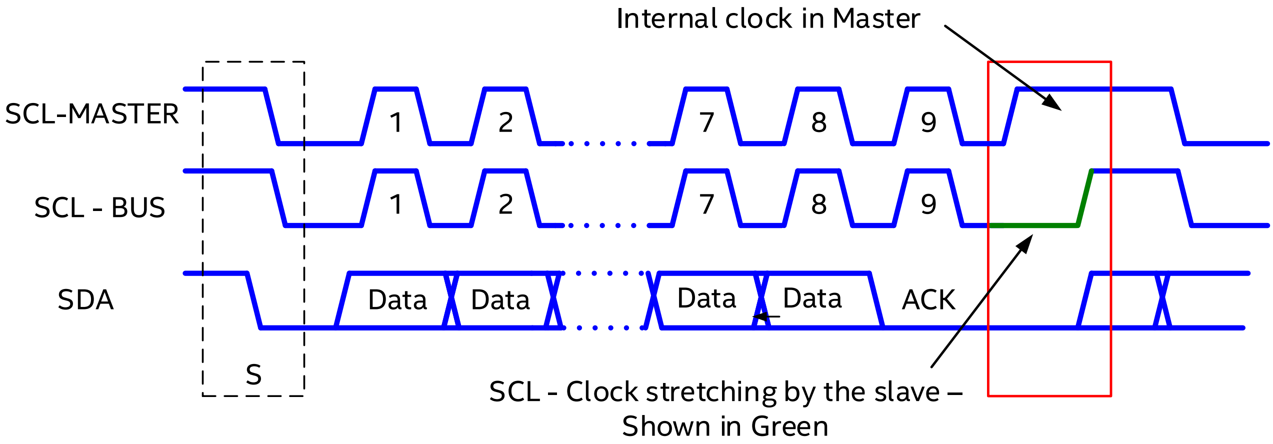


Figure 18: Example of Periodic & Random Clock Stretching

After every byte is received by our module, the module will acknowledge receiving the byte and if required will then hold the SCL line low (Clock stretch) while it processes the received data. Upon completion it will then release the clock signaling to the Master it is ready to receive the next Byte.

Only after issuing the acknowledge bit will our module clock Stretch. The duration of the clock stretch interval will vary in length dependent on the command received and what other activities the controller is performing at that time.

As per the SMBus specification if the SCL is detected to be low for a duration longer than the "Clock low time-out" period then the module will reset its SMBus interface thereby releasing the BUS and be ready for fresh communications. Upon this event occurring the Module will also assert its SMBalert pin to signal the Master an event was occurred. This functionality is not required by the I2C specification, so user should be aware of this difference.

For greater detail on Clock Stretching, please refer to "SMBus Version 2.0" specifications, available at www.smbus.org.

PMBUS COMMANDS

A detailed description of the PMBus commands supported by the ED8401 can be found in a separate document - *ED8401 PMBus Commands Guide.* Below, Table **17** lists of all supported PMBus commands.

Table 17 : List Of Supported PMBus Commands

Command Code	PMBus Parameter	Description
01_{HEX}	**OPERATION**	On/off command
02_{HEX}	**ON_OFF_CONFIG**	On/off configuration
03_{HEX}	**CLEAR_FAULTS**	Clear status information
04_{HEX}	**PHASE**	Configure, control, and monitor phases
10_{HEX}	**WRITE_PROTECT**	Protect against changes
11_{HEX}	**STORE_DEFAULT_ALL**	Copy entire memory into OTP
12_{HEX}	**RESTORE_DEFAULT_ALL**	Copy entire memory from OTP
13_{HEX}	**STORE_DEFAULT_CODE**	Copy single parameter into OTP
14_{HEX}	**RESTORE_DEFAULT_CODE**	Copy single parameter from OTP
19_{HEX}	**CAPABILITY**	PMBus Capabilities
20_{HEX}	**VOUT_MODE** *(Note 3)*	Exponent of the VOUT_COMMAND value
21_{HEX}	**VOUT_COMMAND**	Set output voltage
22_{HEX}	**VOUT_TRIM**	Apply a fixed offset voltage
23_{HEX}	**VOUT_CAL_OFFSET**	Apply a fixed offset voltage
24_{HEX}	**VOUT_MAX**	Sets maximum VOUT
25_{HEX}	**VOUT_MARGIN_HIGH**	Sets maximum value
26_{HEX}	**VOUT_MARGIN_LOW**	Sets minimum value
29_{HEX}	**VOUT_SCALE_LOOP**	Scalar for output voltage divider
$2A_{HEX}$	**VOUT_SCALE_MONITOR**	Scalar for read-back with output voltage divider
$2B_{HEX}$	**VOUT_MAX**	Sets minimum VOUT
35_{HEX}	**VIN_ON**	Input voltage turn on threshold
36_{HEX}	**VIN_OFF**	Input voltage turn off threshold
40_{HEX}	**VOUT_OV_FAULT_LIMIT**	Over-voltage fault limit
41_{HEX}	**VOUT_OV_FAULT_RESPONSE**	Over-voltage fault response
42_{HEX}	**VOUT_OV_WARN_LIMIT**	Over-voltage warning level
43_{HEX}	**VOUT_UV_WARN_LIMIT**	Under-voltage warning level
44_{HEX}	**VOUT_UV_FAULT_LIMIT**	Under-voltage fault level
45_{HEX}	**VOUT_UV_FAULT_RESPONSE**	Under-voltage fault response
46_{HEX}	**IOUT_OC_FAULT_LIMIT**	Over-current fault limit
47_{HEX}	**IOUT_OC_FAULT_RESPONSE**	Over-current fault response

Command Code	PMBus Parameter	Description
$4A_{HEX}$	**IOUT_OC_WARN_LIMIT**	Over-current warning level
$4F_{HEX}$	**OT_FAULT_LIMIT**	Power Train Over-temperature fault level
50_{HEX}	**OT_FAULT_RESPONSE**	Power Train Over-temperature fault response
51_{HEX}	**OT_WARN_LIMIT**	Power Train Over-temperature warning level
55_{HEX}	**VIN_OV_FAULT_LIMIT**	Over-voltage fault limit
56_{HEX}	**VIN_OV_FAULT_RESPONSE**	Over-voltage fault response
57_{HEX}	**VIN_OV_WARN_LIMIT**	Over-voltage warning level
58_{HEX}	**VIN_UV_WARN_LIMIT**	Under-voltage warning level
59_{HEX}	**VIN_UV_FAULT_LIMIT**	Under-voltage fault level
$5A_{HEX}$	**VIN_UV_FAULT_RESPONSE**	Under-voltage fault response
$5E_{HEX}$	**POWER_GOOD_ON**	Power good on threshold
$5F_{HEX}$	**POWER_GOOD_OFF**	Power good off threshold
60_{HEX}	**TON_DELAY**	Turn-on delay
61_{HEX}	**TON_RISE**	Turn-on rise time
62_{HEX}	**TON_MAX_FAULT_LIMIT**	Turn-on maximum fault time
64_{HEX}	**TOFF_DELAY**	Turn-off delay
65_{HEX}	**TOFF_FALL**	Turn-off fall time
66_{HEX}	**TOFF_MAX_WARN_LIMIT**	Turn-off maximum warning time
78_{HEX}	**STATUS_BYTE**	Unit status byte
79_{HEX}	**STATUS_WORD**	Unit status word
$7A_{HEX}$	**STATUS_VOUT**	Output voltage status
$7B_{HEX}$	**STATUS_IOUT**	Output current status
$7C_{HEX}$	**STATUS_INPUT**	Input status
$7D_{HEX}$	**STATUS_TEMPERATURE**	Temperature status
$7E_{HEX}$	**STATUS_CML**	Communication and memory status
80_{HEX}	**STATUS_MFR_SPECIFIC**	Manufacturer specific status
88_{HEX}	**READ_VIN**	Reads input voltage
$8B_{HEX}$	**READ_VOUT**	Reads output voltage
$8C_{HEX}$	**READ_IOUT**	Reads output current
$8D_{HEX}$	**READ_TEMPERATURE_1**	Power Train Temperature read back
$8E_{HEX}$	**READ_TEMPERATURE_2**	Controller Temperature read back
94_{HEX}	**READ_DUTY_CYCLE**	Current Duty Cycle read back
95_{HEX}	**READ_FREQUENCY**	Reads switching frequency

Command Code	PMBus Parameter	Description
96_{HEX}	**READ_POUT**	Reads output power
98_{HEX}	**PMBUS™_REVISION**	PMBus™ revision
99_{HEX}	**MFR_ID**	Manufacturer ID
$9A_{HEX}$	**MFR_MODEL**	Manufacturer model identifier
$9B_{HEX}$	**MFR_REVISION**	Manufacturer product revision
$9E_{HEX}$	**MFR_SERIAL**	Serial number
$A0_{HEX}$	**MFR_VIN_MIN**	Minimum input voltage
$A1_{HEX}$	**MFR_VIN_MAX**	Maximum input voltage
$A4_{HEX}$	**MFR_VOUT_MIN**	Minimum output voltage
$A5_{HEX}$	**MFR_VOUT_MAX**	Maximum output voltage
AD_{HEX}	**IC_DEVICE_ID**	Product Family's model Number
AE_{HEX}	**IC_DEVICE_REV**	Silicon Hardware Revision
$C4_{HEX}$	**MFR_TEMP0_FAULT_RESPONSE**	Phase0 fault response
$C5_{HEX}$	**MFR_TEMP1_FAULT_RESPONSE**	Phase1 fault response
$C6_{HEX}$	**MFR_TEMP2_FAULT_RESPONSE**	Phase2 fault response
$C7_{HEX}$	**MFR_TEMP3_FAULT_RESPONSE**	Phase3 fault response
$C9_{HEX}$	**MFR_CBC_LIM_FAULT_RESPONSE**	CBC LIM fault response
CA_{HEX}	**MFR_CBC_POS_LIMIT**	CBC positive correction limit
$D0_{HEX}$	**MFR_SPECIFIC_00**	Write word (once) / Read word – 2 bytes
$D1_{HEX}$	**MFR_SPECIFIC_01**	Write word / read word – 12 bytes
$D2_{HEX}$	**MFR_READ_VCC**	Reads VCC voltage
$D7_{HEX}$	**MFR_STATUS_EXT1**	External Power Train Fault status Flags 1
$D8_{HEX}$	**MFR_STATUS_EXT2**	External Power Train Fault status Flags 2
$D9_{HEX}$	**MFR_FAULT_RESPONSE_EXT_READ**	Returns additional Fault response settings
DA_{HEX}	**MFR_FAULT_RESPONSE_EXT_WRITE**	Sets additional Fault response settings
DB_{HEX}	**MFR_RTUNE_CONFIG**	Gets/sets RTUNE settings
DD_{HEX}	**MFR_RTUNE_INDEX**	Returns index derived from resistor detected on RTUNE pin
DE_{HEX}	**MFR_RVSET_INDEX**	Returns index derived from resistor detected on RVSET pin
$E0_{HEX}$	**MFR_VOUT_OFF**	Sets the target turn-off voltage
$E1_{HEX}$	**MFR_EXT_TEMP_CAL_OFFSET**	Calibrate with external Temp Sensors
$E2_{HEX}$	**MFR_IOT_FAULT_LIMIT**	Controller Over-temperature fault level
$E3_{HEX}$	**MFR_IOT_WARN_LIMIT**	Controller Over-temperature warning level
$E5_{HEX}$	**MFR_IOT_FAULT_RESPONSE**	Controller Over-temperature fault response

Command Code	PMBus Parameter	Description
$E6_{HEX}$	**MFR_TEMP_ON**	Over-temperature on level
$E7_{HEX}$	**MFR_PIN_CONFIG**	Enable/disable – RTUNE, RVSET, VTRACK and SYNC
$E9_{HEX}$	**MFR_STORE_CONFIG_ADDR_READ**	Reads a configuration value
EA_{HEX}	**MFR_STORE_PARAMS_REMAINING**	Number of STORE_DEFAULT_ALL commands remaining
EB_{HEX}	**MFR_STORE_CONFIGS_REMAINING**	Number of full configurations remaining
EC_{HEX}	**MFR_STORE_CONFIG_BEGIN**	Commence programming of OTP
ED_{HEX}	**MFR_STORE_CONFIG_ADDR_DATA**	Program a configuration value
EE_{HEX}	**MFR_STORE_CONFIG_END**	Completed programming of OTP
EFh	**MFR_OTP_STATUS**	NVM Status

Note 3: VOUT_ MODE is read only for the ED8401

Package Dimensions

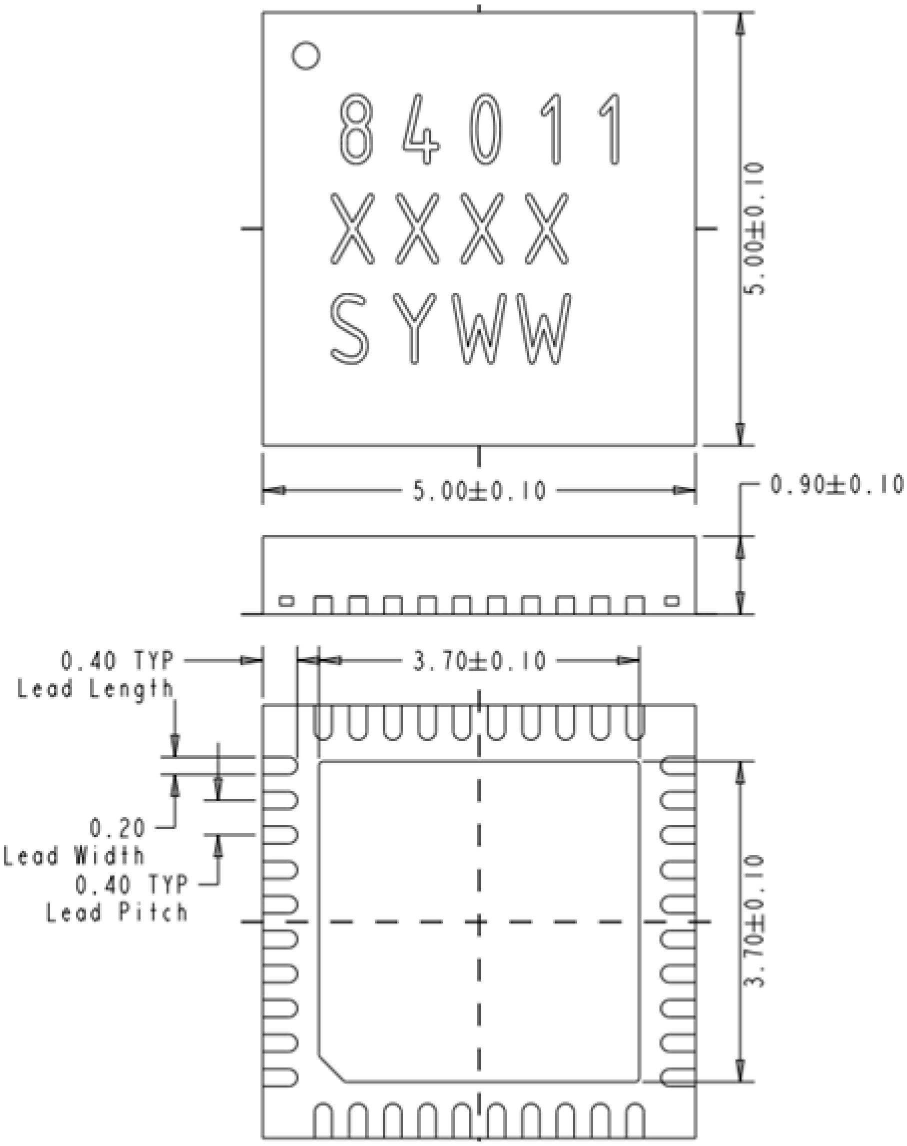


Figure 19: Package Dimensions (ED8401P01 Shown)

Revision History

Rev	Date	Change(s)
A	29th Apr 19	First Release
A1	31st Oct 19	Minor updates
B	6th Apr 20	Release Update

Where to Get More Information

For more information about Intel and Intel Enpirion PowerSoCs, visit **https://www.altera.com/enpirion**