MAX 10 FPGA 10M50 Evaluation Kit User Guide

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MAX 10 FPGA 10M50 Evaluation Kit Overview

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The MAX® 10 Evaluation Kit (P/N : EK-10M50F484) provides an easy-to-use platform for evaluating the MAX 10 FPGA technology and Enpirion® PowerSoC regulators. You can use this kit to do the following:

- Develop designs for the 10M50, F484 package FPGA
- Validate MIPI CSI-2 passive solution for both MIPI transmitter and receiver
- Demonstrate video applications together with HDMI
- Interface MAX 10 FPGAs to LPDDR2 memory at 200 MHz performance
- Interface to daughter cards and peripherals using Digilent Pmod™ Compatible connectors
- Bridge to external devices through single-ended and LVDS through-hole vias
- Measure FPGA power (VCC_CORE)
- Reuse the kit's PCB board and schematic as a model for your design

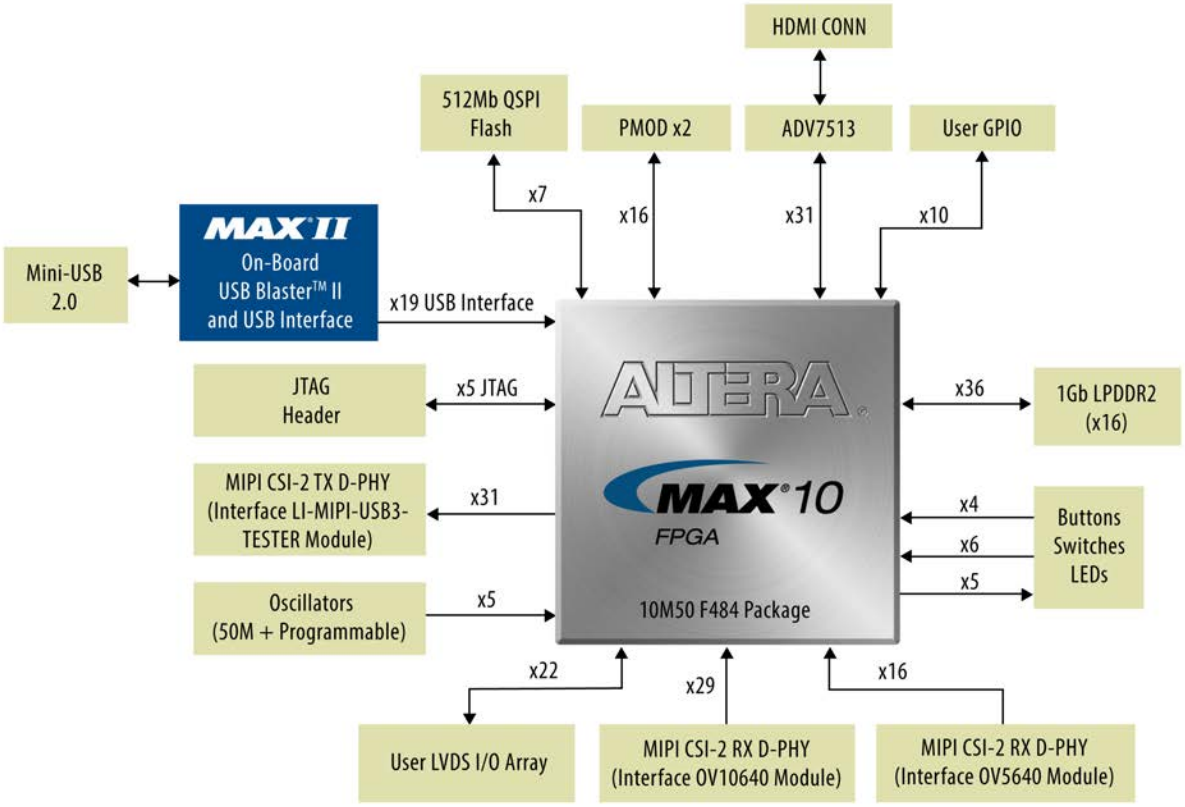
Board Component Blocks

The MAX 10 FPGA 10M50 Evaluation Kit features the following major component blocks. For a detailed description of the board components, see "Board Components" section on Page 3-1.

- Featured Devices
  - MAX 10 FPGA - 10M50D, dual supply, F484 package (P/N: 10M50DAF484C6GES)
  - MAX II CPLD - EPM1270M256C4N (On-board USB Blaster II)
  - Enpirion EP5348UI - 400mA PowerSoC Synchronous Buck Regulator with Integrated Inductor
  - Enpirion EP5358xUI - 600mA PowerSoC DC-DC Step-Down Converters with Integrated Inductor
  - Enpirion EN5329QI/EN5339QI - 2A/3A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor
- FPGA configuration
  - Embedded USB-Blaster II (JTAG)
  - Optional JTAG direct via 10-pin header
- On Board clocking circuitry
  - 25 MHz single-ended, external oscillator clock source
  - Silicon Labs Si510 crystal oscillator
  - Silicon Labs Si5338 clock generator with programmable frequency GUI
- Memory devices
  - 64M x 16 1Gbits LPDDR2 with soft memory controller
  - 512Mbits Quad Serial Peripheral Interface (Quad SPI) Flash

- Communication Ports
  - One HDMI video output
  - Two 12-pin Pmod connectors
  - Two 36-pin MIPI FFC connectors and one 16-pin MIPI FFC connector
- General User I/O
  - General-purpose single-ended through-hole vias (2x5)
  - General-purpose LVDS through-hole vias (2 x 9 LVDS pairs, plus two clock pairs)
  - 5 Green User-defined LEDs
  - 4 User-defined push buttons
  - User DIP Switches (SW1, SW2.1, SW2.2)
- Power
  - Yellow Power-ON LEDs (D9, D10, D11)
  - USB Y cable (USB Type-A to mini Type-B) for both on-board USB-Blaster II and 5V/1A power capability
  - Support DC power adapter option, but 5V power supply and cord are not included in the kit
- Software
  - Free Quartus® Prime Lite Edition design software (download software and license from **http://www.altera.com/download**)
- Complete documentation
  - User Guide, bill of material, schematic and board files

Figure 1-1: MAX 10 10M50 FPGA Evaluation Kit Block Diagram



Related Information

Board Components on page 3-1

Supported Items Not Included with the Kit

The following items are not included in the kit but were designed to be used in conjunction with this kit. All of these items are sold separately.

Table 1-1: Additional Components Not Included with the Kit

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J1, J2	Cable Flat Flex Top / Top 36 POS 0.5 MM pitch	Parlex	050R36-76B	www.parlex.com
		Molex	0210200385	www.molex.com
		Leopard Imaging	LI-FLEX03	www.leopardimaging.com

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J3	Cable Flat Flex Top/ Bottom 16 POS 0.5 MM 6inches	Wurth Electronics Molex	687716152002 02010200171	www.we-online.com www.molex.com
J12, J13	2x10 0.1-inch headers (for LVDS GPIO)	Wurth Electronics	61302021121	www.we-online.com
J14	2x7 0.1-inch headers (for GPIO)	Wurth Electronics	61301421121	www.we-online.com
J5	USB-Blaster Download Cable	Altera	PL-USB-BLASTER-RCN	https://www.altera.com/products/boards_and_kits/download-cables.html
J5	USB-Blaster II Download Cable	Altera	PL-USB2-BLASTER	https://www.altera.com/products/boards_and_kits/download-cables.html
J10	Standard 5V, 2.0A Switching Power Adapter	LI Tone Electronics	LTE12E-S1-316	www.lte.com.tw
J10	Standard 5V, 3.0A Switching Power Adapter	Huntkey	HKA08105030-8B	http://dealer.huntkey.com/en/
J1	LI-MIPI-USB-Tester Daughter Card	Leopard Imaging	LI-USB30-MIPI-TESTER	http://shop.leopardimaging.com
J2	LI-CAM-OV10640-MIPI Daughter Card	Leopard Imaging	LI_CAM-OV10640-MIPI	http://shop.leopardimaging.com
J3	MIPI 5MP AF Camera Daughter Card	UDOO	MIPI 5MP IR AF Camera	http://shop.udoo.org

Getting Started 2

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Powering the Kit

You can apply power to the MAX 10 FPGA Evaluation Kit by plugging in either the 5V DC power adapter to wall jack, or the USB cable to your PC. For low-power design, USB cable connection is suggested, and it can easily provide both power and on-board USB Blaster connection. For high-power design, 5V DC adapter solution is preferred to ensure device performance.

The board includes one Jumper (J11) for power option selection. When use DC power adapter, J11 needs to be placed at Position 1 and 2; while for using USB power, J11 needs to be placed at Position 2 and 3.

Resistors (R292 and R293) can be populated and used in place of the jumper if you want to hard wire the power option.

When powered correctly, D9, D10 and D11 will light.

Caution: Resistors R292 and R293 are designed for hard wiring the power selection. J11 must not be used when either R292 or R293 is populated.

Installing the USB-Blaster Driver

The development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

Installation instructions for the On-Board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Handling the Kit

When handling the board, it is important to observe the following static discharge precaution:

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

The MAX 10 Evaluation Kit must be stored between –40° C and 100° C. The recommended operating temperature is between 0° C and 85° C.

Factory Default Switch and Jumper Settings

Figure 2-1: Switch Locations and Default Settings (Board Top)

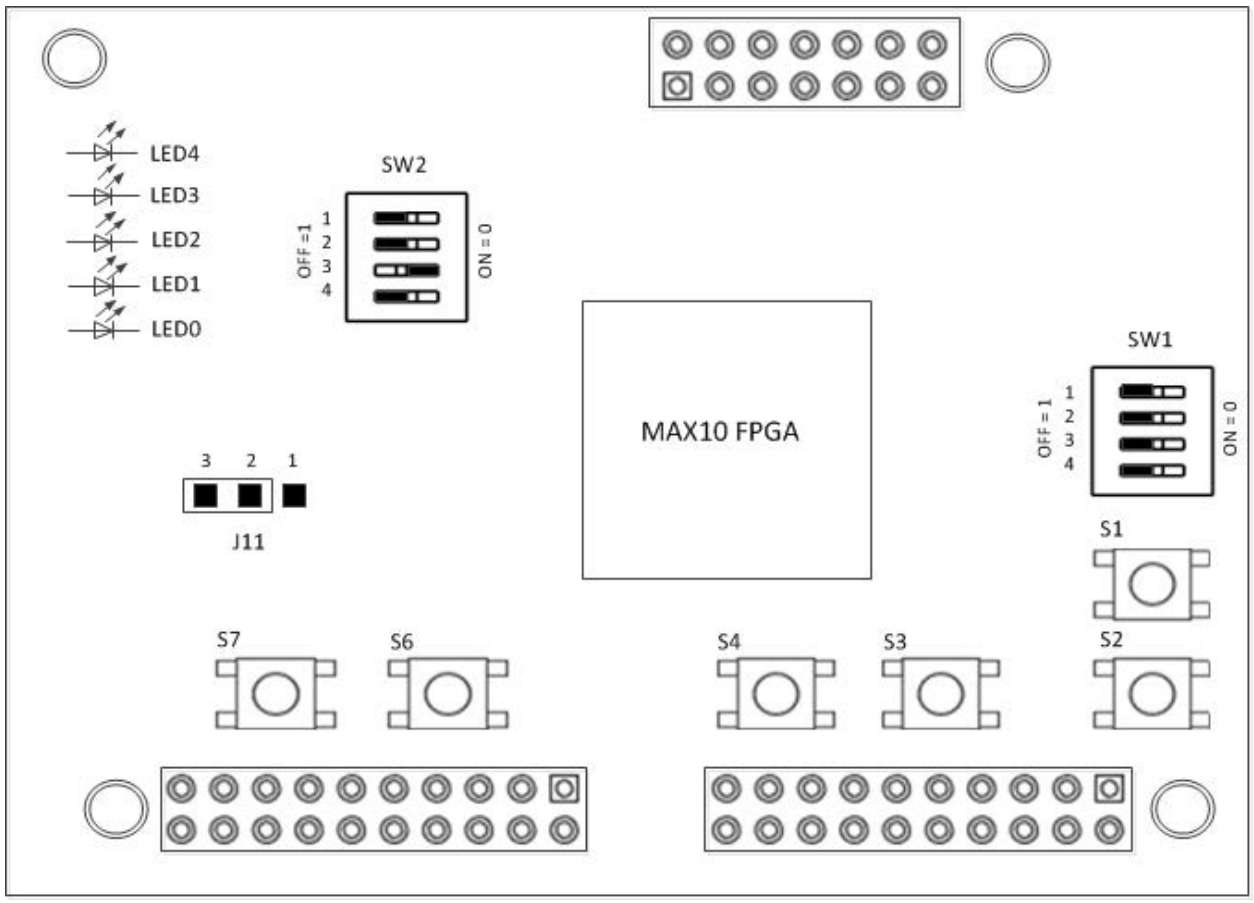

Table 2-1: Default SW1 DIP Switch Settings

Board Reference	Signal Name	Function	Default Position
SW1.1	USER_DIPSW0	User-Defined	HIGH (OFF =1)
SW1.2	USER_DIPSW1	User-Defined	HIGH (OFF =1)
SW1.3	USER_DIPSW2	User-Defined	HIGH (OFF =1)
SW1.4	USER_DIPSW3	User-Defined	HIGH (OFF =1)

Table 2-2: Default SW2 DIP Switch Settings

Board Reference	Signal Name	Function	Default Position
SW2.1	USER_DIPSW4	User-Defined	HIGH (OFF =1)

Board Reference	Signal Name	Function	Default Position
SW2.2	USER_DIPSW5	User-Defined	HIGH (OFF =1)
SW2.3	CONFIG_SEL	CONFIG_SEL: Use this pin to choose CFM0, CFM1 or CFM2 image as the first boot image in dual-image configuration. If the CONFIG_SEL is set to low, the first boot image is CFM0 image. If CONFIG_SEL is set o high, the first boot image is CFM1 or CFM2 image. This pin is read before user mode and before the nSTATUS pin is asserted.	LOW (ON =0)
SW2.4	VTAP_BYPASSn	A virtual JTAG device is provided within the On-board USB-Blaster II, it provides access to diagnostic hardware and board identification information. The device shows up as an extra device on the JTAG chain with ID: 020D10DD. This switch removes the virtual JTAG device from the JTAG chain.	HIGH (OFF =1)

Table 2-3: Default J11 Jumper Settings

Jumper	Function	Setting
J11[1-2]	Jumper for board DC adapter power option when R292 and R293 not installed	Pins 1 and 2
J11[2-3]	Jumper for board USB power option when R292 and R293 not installed. This is the default power jumper position.	Pins 2 and 3

Board Components 3

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This chapter introduces all the important components on the evaluation kit. The *Overview of the MAX 10 FPGA Evaluation Kit Features* figure illustrates major component locations and *MAX 10M50 FPGA (10M50, 484-FPGA) Evaluation Kit Components* table in this chapter provides a brief description of all features of the board.

Related Information

Board Component Blocks on page 1-1

Board Overview

This section provides an overview of the evaluation kit, including an annotated board image and component descriptions.

Figure 3-1: Overview of the MAX 10 10M50 FPGA Evaluation Kit Features - Board Image (Front View)

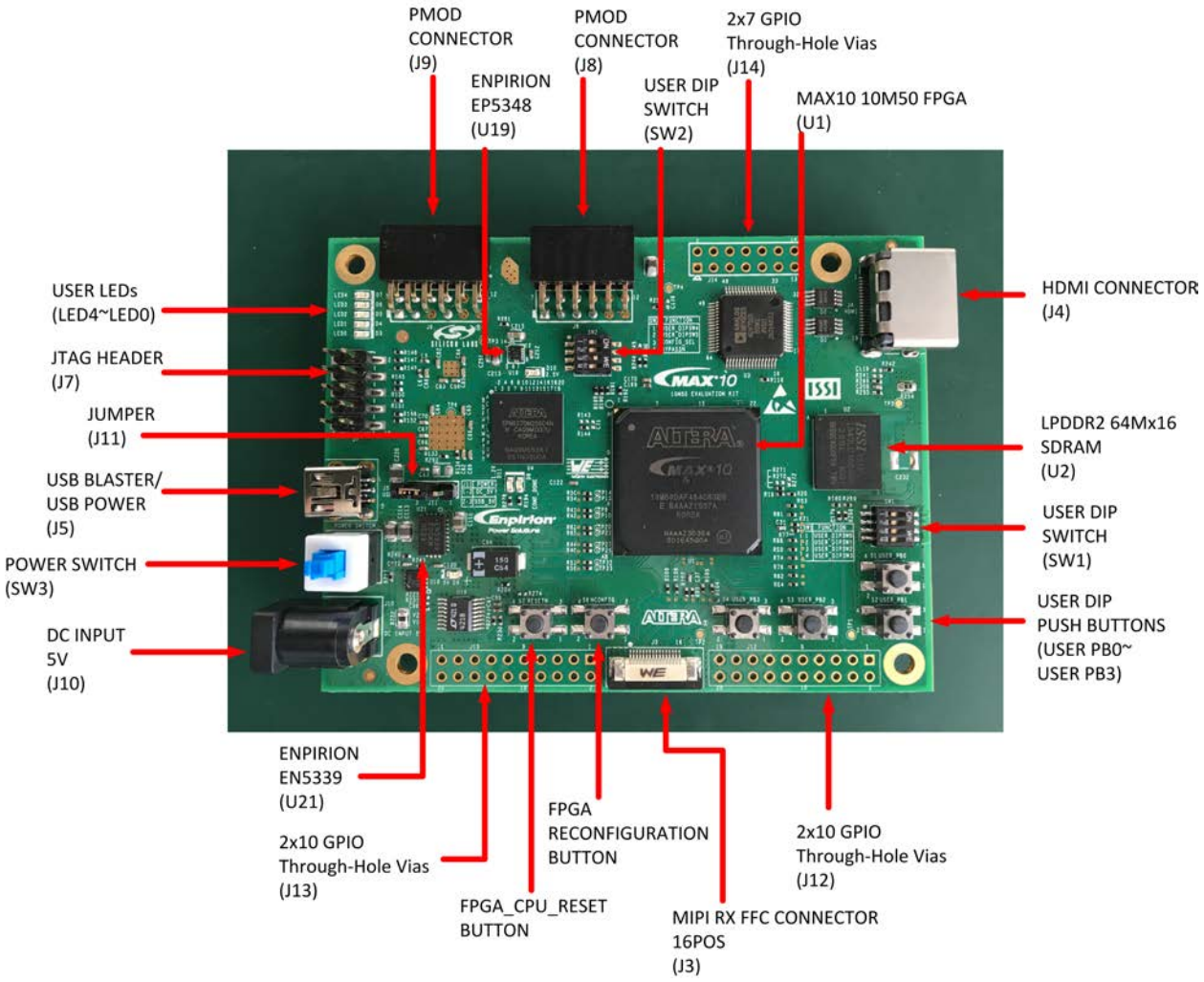


Figure 3-2: Overview of the MAX 10 10M50 FPGA Evaluation Kit Features - Board Image (Rear View)

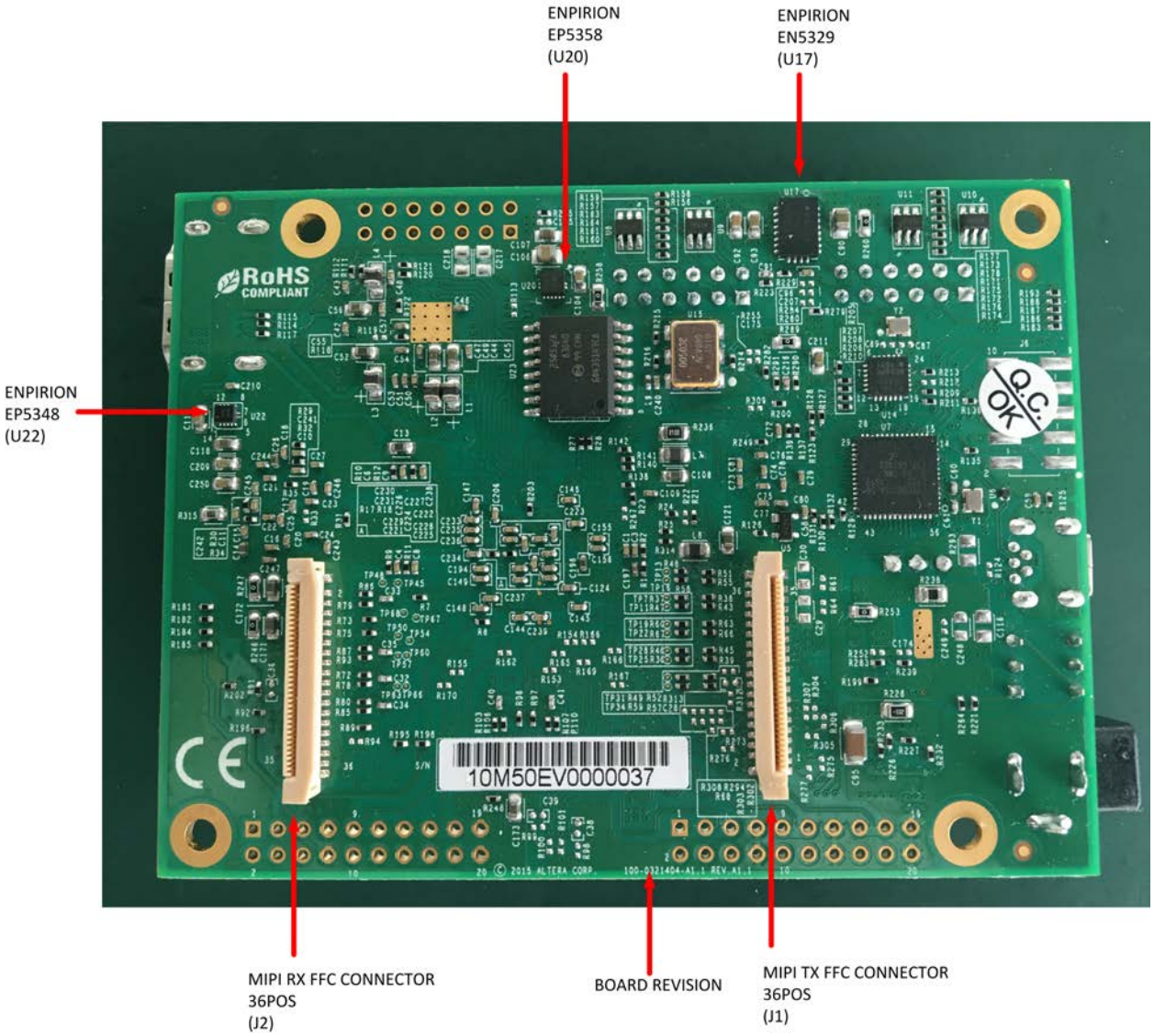


Table 3-1: MAX 10 FPGA (10M50, 484-FPGA) Evaluation Kit Components

Board Reference	Type	Description
Featured Device		
U1	FPGA	MAX 10 FPGA 10M50DAF484C6GES, 50K LEs, F484 package, -6ES speed grade.
U13	CPLD	MAX II EPM1270 256-MBGA, 2.5V/3.3V, VCCINT for On-Board USB-Blaster II.
U17	Power Regulator	Enpirion EN5329QI 2A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor.

Board Reference	Type	Description
U19, U22	Power Regulator	Enpirion EP5348UI 400mA PowerSoC Synchronous Buck Regulator with Integrated Inductor.
U20	Power Regulator	Enpirion EP5358HUI 600mA PowerSoC Synchronous Buck Regulator with Integrated Inductor.
U21	Power Regulator	Enpirion EN5339QI 3A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor.
Configuration and Setup Elements		
J5	On-Board (Embedded) USB-Blaster II	Mini Type-B USB connector for programming and debugging the FPGA.
J7	10-pin header	Optional JTAG direct via 10-pin header for external download cables.
SW2	DIP configuration and user switch	SW2 includes switches to control boot images and JTAG bypass.
S6	MAX10 nCONFIG push button	Toggling this button causes the FPGA to reconfigure from on-die Configuration Flash Memory (CFM).
S7	FPGA register push button	Toggling this button resets all registers in the FPGA.
J11	Jumper for board power option	Default connection is Pins 2 and 3 position, which uses USB power supply. If needed, change jumper position to Pins 1 and 2 for DC adapter power supply solution.
Status Elements		
D8	Configuration done LED, green	Illuminates when the FPGA is configured.
D9	Power LED, yellow	Indicates that 5V is powered up successfully.
D10	Power LED, yellow	Indicates that 2.5V is powered up successfully.
D11	Power LED, yellow	Indicates that 1.2V is powered up successfully.
Clock Circuitry		
U14	Programmable Clock	Four channel programmable oscillator with default frequencies of 24, 24, 125,100 MHz.
U15	50-MHz oscillator	50-MHz crystal oscillator for general purpose logic of MAX 10 and MAX II devices.
General User Input and Output		

Board Reference	Type	Description
S1, S2, S3, S4	User push buttons	Four user push buttons. Driven low when pressed.
D3, D4, D5, D6, D7	User LEDs, green	Five user LEDs. Illuminate when driven low.
SW1, SW2.1, SW2.2	User DIP switches	Quad user DIP switches.
Memory Devices		
U2	LPDDR2 SDRAM memory	64 M x16
U23	Quad serial peripheral interface (quad SPI) flash	512 Mb
Video and Display Ports		
J1	MIPI CSI-2 transmitter output	MIPI CSI-2 transmitter output to Leopard Imaging LI-MIPI-USB3-Tester module.
J2	MIPI CSI-2 receiver	MIPI CSI-2 receiver input from Leopard Imaging LI-CAM-OV10640-MIPI module.
J3	MIPI CSI-2 receiver	MIPI CSI-2 receiver input from UDOO Camera Module OV5640.
J4	HDMI video output	19-pin HDMI connector which provides a HDMIv1.4 video output of up to 1080p through an ADI (Analog Devices, Inc) HDMI transmitter (ADV7513).
I/O and Expansion Ports		
J8, J9	Two Diligent Pmod connectors	12-pin interface with 8 I/O signal pins used to connect low frequency, low I/O peripheral modules.
J12, J13	Two 2x10 GPIO connectors, user install	You can use this area to connect or solder additional components for connection of 9 true LVDS pairs with clock input and output, or 22 single-ended I/O signals.
J14	2x7 GPIO connectors, user install	You can use this area to connect or solder additional components for connection of 10 single-ended I/O signals.
Power Supply		
J10	DC input jack	Accepts 5V DC power supply when USB power supply is not in use.
SW3	Power switch	When using DC power adapter, switch to power on or off the board when power is supplied from the DC input jack. DC adapter and USB power don't work at the same time.

Board Reference	Type	Description
J5	USB connector	USB power supply. Use with USB Y cable to provide 1A current. DC adapter power and USB power don't work at the same time.

Featured Device: MAX 10 FPGA

The MAX 10 FPGA development board features the MAX 10 10M50DAF484C6GES device (U1) in a 484-pin FineLine BGA package.

Table 3-2: MAX 10 FPGA 10M50DAF484C6GES Features

Logic Elements (LEs)	Internal Configuration	M9K Memory (Kb)	User Flash Memory (KB)	18-bit X 18-bit Multipliers	PLLs	ADC Blocks / Temperature Sensing Diode	External Memory Interfaces Supported
50,000	Dual	1,638	736 Note 1	144	4	2/1	DDR3, DDR3L, DDR2, LPDDR2

Note: **1.** The maximum possible value including user flash memory and configuration flash memory. For more information, refer to **MAX 10 User Flash Memory User Guide**.

Configuration

The MAX 10 10M50 Evaluation Kit supports two configuration methods:

- Configuration by downloading a **.sof** file to the FPGA. Any subsequent power cycling of the FPGA or reconfiguration will power up the FPGA to a blank state.
- Programming of the on-die FPGA Configuration Flash Memory (CFM) via a **.pof** file. Any power cycling of the FPGA or reconfiguration will power up the FPGA in self-configuration mode, using the files stored in the CFM

You can use two different USB-Blaster hardware components to program the **.sof** or **.pof** files:

- Embedded USB-Blaster II, mini Type-B connector (J5)
- JTAG header (J7). Use an external USB-Blaster, USB-Blaster II, or Ethernet Blaster download cable. The external download cable connects to the board through the JTAG header.

Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a **.sof**.

Before configuring the FPGA:

- Ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer
- The USB cable is connected to the kit
- Power to the board is on, and no other applications that use the JTAG chain are running.

To configure the MAX 10 FPGA:

1. Start the Quartus II Programmer.
2. Click **Add File** and select the path to the desired **.sof**.
3. Turn on the **Program/Configure** option for the added file.
4. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

The Quartus II Convert Programming File (CPF) GUI can be used to generate a **.sof** file that can use for internal configuration. You can directly program the MAX 10 device's flash which includes Configuration Flash Memory (CFM) and User Flash Memory (UFM) by using a download cable with the Quartus II software programmer.

Selecting the Internal Configuration Scheme

For all MAX 10 devices, except 10M02 device, there are total of 5 different modes you can select internal configuration. Please refer to *Figure 2-2: Configuration Flash Memory Sectors Utilization for all MAX 10 Devices Except for 10M02 Device* of **MAX 10 FPGA Configuration User Guide**. You can access the PDF of the MAX 10 FPGA Configuration User guide **here**.

The internal configuration scheme needs to be selected before design compilation. To select the configuration mode:

1. Open the Quartus II software and load a project using MAX 10 device family.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
3. In the Category list, select **Device**. The **Device** page appears.
4. Click **Device and Pin Options**.
5. In the **Device and Pin Options** dialog box, click the **Configuration** tab.
6. In the **Configuration Scheme** list, select **Internal Configuration**.
7. In the **Configuration Mode** list, select 1 out of 5 configuration modes. For the dual-boot feature:
   a. Must have a Dual Boot IP in the design, for example, in a Qsys component.
   b. Choose **Dual Compressed Images (512 Kbits UFM)** for the **Configuration Mode**.
   c. Generate two **.sof** files above and convert them into one **.pof** file for CFM programming.
8. Turn on Generate compressed bit-streams if needed, and click **OK**.

Status Elements

This topic lists the non-user status elements for the MAX 10 10M50 FPGA Evaluation Board.

Table 3-3: Status LED Signal Names

Board Reference	Signal Name	Colour	Device/Pin Number	I/O Standard
D8	MAXII_CONF_DONE	Green	MAX II / Y10	3.3 V
D9	5V_LED_R	Yellow	---	---
D10	2.5V_LED_R	Yellow	---	---
D11	1.2V_LED	Yellow	MAX II / Y9	3.3 V

Setup Elements

Table 3-4: Board Settings DIP Switch and Jumper Schematic Signals

Board Reference	Signal Name	Device / Pin Number	I/O Standard
SW2.3	MAX10_CONFIG_SEL	MAX 10 / H10	3.3V
SW2.4	MAX10_BYPASSn	MAX II / B20	3.3V

Table 3-5: Board Settings Push Button Signal Names

Board Reference	Signal Name	MAX 10 FPGA Pin Number	I/O Standard
S6	MAX10_nCONFIG	H9	3.3V
S7	MAX10_RESETn	D9	3.3V

General User Input/Output

User-defined I/O signal names, FPGA pin numbers, and I/O standards for the MAX 10 FPGA 10M50 Evaluation Board.

Table 3-6: User-Defined Push Button Signal Names

Board Reference	Signal Name	MAX 10 FPGA Pin Number	I/O Standard
S1	USER_PB0	R20	1.2 V
S2	USER_PB1	Y20	1.2 V
S3	USER_PB2	Y21	1.2 V
S4	USER_PB3	U20	1.2 V

Table 3-7: User-Defined DIP Switch Schematic Signal Names

Board Reference	Signal Name	MAX 10 FPGA Pin Number	I/O Standard
SW1.1	USER_DIPSW0	R18	1.2 V
SW1.2	USER_DIPSW1	T19	1.2 V
SW1.3	USER_DIPSW2	T18	1.2 V
SW1.4	USER_DIPSW3	U19	1.2 V
SW2.1	USER_DIPSW4	G4	3.3 V

Board Reference	Signal Name	MAX 10 FPGA Pin Number	I/O Standard
SW2.2	USER_DIPSW5	F5	3.3 V

Table 3-8: User LED Schematic Signal Names

Board Reference	Signal Name	Color	MAX 10 FPGA Pin Number	I/O Standard
D3	USER_LED0	Green	C3	3.3 V
D4	USER_LED1	Green	C4	3.3 V
D5	USER_LED2	Green	C5	3.3 V
D6	USER_LED3	Green	D5	3.3 V
D7	USER_LED4	Green	C7	3.3 V

Table 3-9: User Defined I/O Through-Hole Vias

Board Reference	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard Note 1	Description
J12.1	2.5V Power	----	----	Power Supply Connector for J12
J12.2	2.5V Power	----	----	Power Supply Connector for J12
J12.3	USER_CLKIN_IO_P	K22	DIFFIO_RX_R40P or CLK3P	Dual purpose pin. Either User I/O or Clock input ref. for this group of LVDS channels
J12.4	USER_LVDS_P2	Y17	DIFFIO_TX_RX_B43P, High Speed	LVDS User I/O_2. Note 1
J12.5	USER_CLKIN_IO_N	K21	DIFFIO_RX_R40N or CLK3N	Dual purpose pin. Either User I/O or Clock input ref. for this group of LVDS channels
J12.6	USER_LVDS_N2	AA17	DIFFIO_TX_RX_B43N, High Speed	LVDS User I/O_2. Note 1
J12.7	GND	----	----	Ground Reference for this group of I/Os
J12.8	GND	----	----	Ground Reference for this group of I/Os

Board Reference	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard Note 1	Description
J12.9	USER_LVDS_P0	AA10	DIFFIO_TX_RX_B22P, High Speed	LVDS User I/O_0. Note 1
J12.10	USER_LVDS_P3	Y14	DIFFIO_TX_RX_B37P, High Speed	LVDS User I/O_3. Note 1
J12.11	USER_LVDS_N0	Y10	DIFFIO_TX_RX_B22N, High Speed	LVDS User I/O_0. Note 1
J12.12	USER_LVDS_N3	Y13	DIFFIO_TX_RX_B37N, High Speed	LVDS User I/O_3. Note 1
J12.13	GND	----	----	Ground Reference for this group of I/Os
J12.14	GND	----	----	Ground Reference for this group of I/Os
J12.15	USER_LVDS_P1	W8	DIFFIO_TX_RX_B13p, High Speed	LVDS User I/O_1. Note 1
J12.16	CLKOUT_LVDS_P	V17	DIFFIO_TX_RX_B57P or PLL_B_CLKOUTP	Dual purpose pin. Either User I/O or Clock output ref. for this group of LVDS channels
J12.17	USER_LVDS_N1	W7	DIFFIO_TX_RX_B13n, High Speed	LVDS User I/O_1. Note 1
J12.18	CLKOUT_LVDS_N	W17	DIFFIO_TX_RX_B57N or PLL_B_CLKOUTN	Dual purpose pin. Either User I/O or Clock output ref. for this group of LVDS channels
J12.19	GND	----	----	Ground Reference for this group of I/Os
J12.20	GND	----	----	Ground Reference for this group of I/Os
J13.1	2.5V Power	----	----	Power Supply for Connector J13
J13.2	2.5V Power	----	----	Power Supply for Connector J13
J13.3	USER_LVDS_P5	V8	DIFFIO_TX_RX_B7p, High Speed	LVDS User I/O_5. Note 1

Board Reference	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard [Note 1]	Description
J13.4	USER_LVDS_P8	AA7	DIFFIO_TX_RX_B16p, High Speed	LVDS User I/O_8. Note 1
J13.5	USER_LVDS_N5	V7	DIFFIO_TX_RX_B7n, High Speed	LVDS User I/O_5. Note 1
J13.6	USER_LVDS_N8	AA6	DIFFIO_TX_RX_B16n, High Speed	LVDS User I/O_8. Note 1
J13.7	GND	----	----	Ground Reference for this group of I/Os
J13.8	GND	----	----	Ground Reference for this group of I/Os
J13.9	USER_LVDS_P6	W6	DIFFIO_TX_RX_B1p, High Speed	LVDS User I/O_6. Note 1
J13.10	USER_LVDS_P4	W10	DIFFIO_TX_RX_B11p, High Speed	LVDS User I/O_4. Note 1
J13.11	USER_LVDS_N6	W5	DIFFIO_TX_RX_B1n, High Speed	LVDS User I/O_6. Note 1
J13.12	USER_LVDS_N4	W9	DIFFIO_TX_RX_B11n, High Speed	LVDS User I/O_4. Note 1
J13.13	GND	----	----	Ground Reference for this group of I/Os
J13.14	GND	----	----	Ground Reference for this group of I/Os
J13.15	USER_LVDS_P7	W3	DIFFIO_TX_RX_B5p, High Speed	LVDS User I/O_7. Note 1
J13.16	NC	----	----	Not Connected
J13.17	USER_LVDS_N7	W4	DIFFIO_TX_RX_B5n, High Speed	LVDS User I/O_7. Note 1
J13.18	NC	----	----	Not Connected
J13.19	GND	----	----	Ground Reference for this group of I/Os
J13.20	GND	----	----	Ground Reference for this group of I/Os

Board Reference	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard Note 1	Description
J14.1	USER_IO0	A17	DIFFIO_RX_ T10n, High Speed	User I/O_0
J14.2	USER_IO5	A19	DIFFIO_RX_T8n, High Speed	User I/O_5
J14.3	USER_IO1	B19	DIFFIO_RX_T6n, High Speed	User I/O_1
J14.4	USER_IO6	A20	DIFFIO_RX_T8p, High Speed	User I/O_6
J14.5	3.3V power	----	----	Power Supply for Connector J14
J14.6	3.3V power	----	----	Power Supply for Connector J14
J14.7	USER_IO2	E16	DIFFIO_RX_T1p, High Speed	User I/O_2
J14.8	USER_IO7	C18	DIFFIO_RX_T7p, High Speed	User I/O_7
J14.9	USER_IO3	C19	DIFFIO_RX_T6n, High Speed	User I/O_3
J14.10	USER_IO8	C17	DIFFIO_RX_T2n, High Speed	User I/O_8
J14.11	GND	----	----	Ground Reference for this group of I/Os
J14.12	GND	----	----	Ground Reference for this group of I/Os
J14.13	USER_IO4	F16	DIFFIO_RX_T5p, High Speed	User I/O_4
J14.14	USER_IO9	D17	DIFFIO_RX_T2p, High Speed	User I/O_9

Note: **1.** Termination resistors are required to be installed by the user for proper high speed LVDS I/O use.

Clock Circuitry

The MAX 10 FPGA 10M50 Evaluation Board includes two oscillators:

- A four channel programmable oscillator with default frequency of 24-MHz, 24-MHz, 125-MHz, 100-MHz.
- A two channel crystal oscillator with default frequency of 50-MHz.

On-Board Oscillators

Figure 3-3: MAX 10 10M50 FPGA Evaluation Kit Clocks

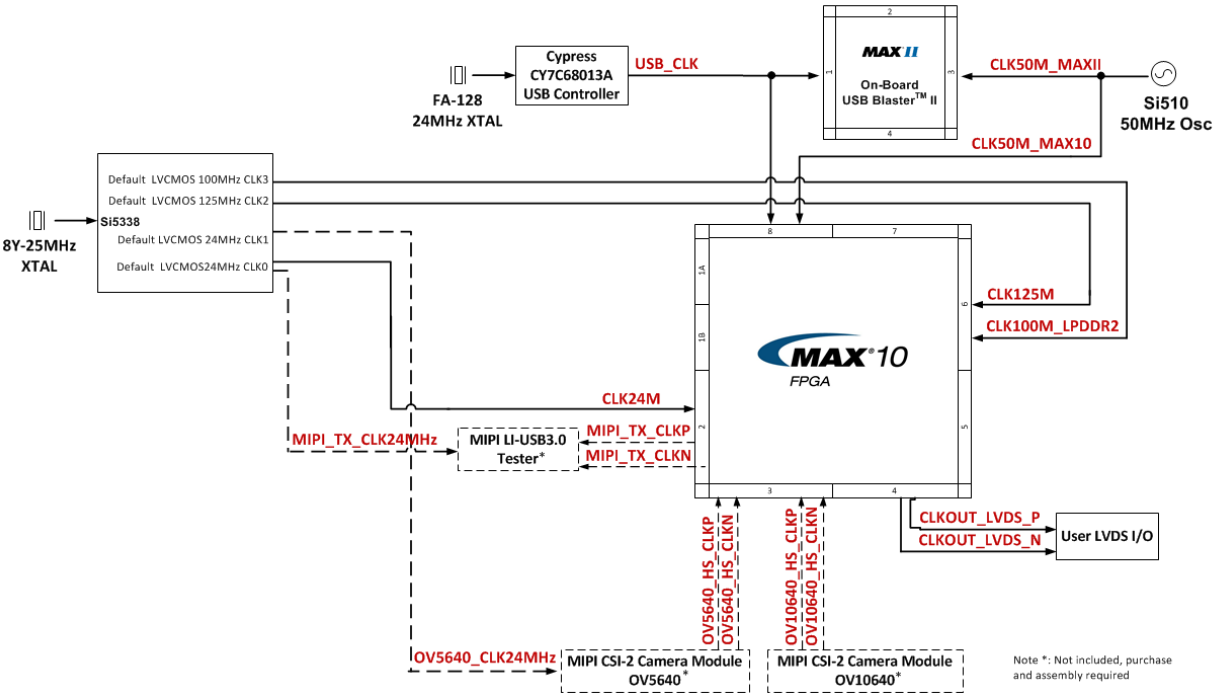


Table 3-10: On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Device / Pin Number	Application
U14	CLK24M	24.000 MHz	1.8 V CMOS	MAX 10/M9	Programmable default 24 MHz clock for MAX 10
U14	OV5640_ CLK24MHz	24.000 MHz	3.3 V CMOS	16 POS FFC connector / J3.12	Clock for MIPI RX OV5640 module

Source	Schematic Signal Name	Frequency	I/O Standard	Device / Pin Number	Application
U14	CLK125M	125.000 MHz	3.3 V CMOS	MAX 10/K22	Programmable default 125 MHz clock for PLL generating required clocks for LVDS GPIO interface
U14	CLK100M_LPDDR2	100.000 MHz	3.3 V CMOS	MAX 10/E10	LPDDR2 clock
U15	CLK50M_MAX10	50.000 MHz	3.3 V CMOS	MAX 10/J10	MAX 10 clock
U15	CLK50M_MAXII	50.000 MHz	3.3 V CMOS	MAX II/L1	MAX II clock

Off-Board Clock Input/Output

The MAX 10 10M50 Evaluation Board has input and output clocks which can be driven onto the board. Resistor reworking might be needed for specific application.

Table 3-11: Off-Board Clock Inputs and Outputs

Source	Schematic Signal Name	I/O Standard	MAX 10 FPGA	Description
J12	USER_CLKIN_P_MAX10	1.2 V	K21	Single-ended clock input, or positive terminal for differential clock inputs from user GPIO
J12	USER_CLKIN_N_MAX10	1.2 V	K22	Single-ended clock input, or negative terminal for differential clock inputs from user GPIO
J12	CLKOUT_LVDS_P	2.5 V	V17	Single-ended clock output, or positive terminal for differential clock output to user GPIO
J12	CLKOUT_LVDS_N	2.5 V	W17	Single-ended clock output, or negative terminal for differential clock output to user GPIO

Clock Control GUI

This kit includes a Clock Control GUI application.

The Clock Control GUI application communicates over the JTAG bus to a test design running in the FPGA. It shares the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II Programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

The Clock Control

The MAX 10 FPGA 10M50 Evaluation Board Clock Control application sets the programmable oscillators to any frequency between 10 MHz and 200 MHz. It communicates with the MAX II device on the board through the JTAG bus. The programmable oscillators are connected to the MAX II device through a 2-wire serial bus.

To run the Clock Control GUI, perform the following steps:

1. Make sure Quartus II 14.1 or later version is installed.
2. Connect the USB cable to the MAX 10M50 FPGA Evaluation Board and power cycle the board.
3. Double click the **Clock Control GUI** application and the interface shows as in the figure below.
4. Perform **Default** to set the default frequencies to the board: CLK0-24MHz, CLK1-24MHz, CLK2-125MHz, CLK3-100MHz
5. Peform **Read** operation to get the current frequency setup.
6. If necessary, input new frequencies to each clock frequency fill-in box and perform **Set New Freq** to set the board to the input clock frequency setup.
7. Select the **Disable** to disable any clock channel if needed.

Figure 3-4: The Si5338 Tab

Table 3-12: The Clock Control Tab

Control	Description
F_vco	Displays the generating signal value of the voltage-controlled oscillator
Registers	Display the current frequencies for each oscillator
Frequency (MHz)	Allows you to specify the frequency of the clock
Disable	Disable each oscillators as required
Read	Reads the current frequency setting for the oscillator associated with the active tab
Default	Sets the frequency for the oscillator associated with the active tab back to its default value. This can be also be accompanied by power cycling the board.
Set New Freq	Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 and CLK3 controls. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies. **Note:** Changing CLK0 of Si5338 will affect the Clock/Power GUI. Once clock from Port CLK0 is used to drive the MAX II device which is working as a 2-wire serial bus interface connected to Si570, Si5338 and power monitor.

Components and Interfaces

This section describes the evaluation board's ports and optional interface cards relative to the MAX 10 FPGA device.

HDMI Video Output

The MAX 10 10M50 evaluation kit supports one HDMI transmitter and one HDMI receptacle. The transmitter incorporates HDMI v1.4 features, and is capable of supporting an input data rate up to 165 MHz (1080p @ 60Hz, UXGA @ 60Hz). The connection between HDMI transmitter and MAX 10 is established in Bank 7, and the communication can be done via I2C interface.

Table 3-13: HDMI Pin Assignments, Signal Names and Functions

Board Reference (U3)	Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
U3.62	HDMI_VIDEO_DIN0	J12	3.3 V	HDMI digital video data bus

Board Reference (U3)	Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
U3.61	HDMI_VIDEO_DIN1	D13	3.3 V	HDMI digital video data bus
U3.60	HDMI_VIDEO_DIN2	E12	3.3 V	HDMI digital video data bus
U3.59	HDMI_VIDEO_DIN3	E13	3.3 V	HDMI digital video data bus
U3.58	HDMI_VIDEO_DIN4	D12	3.3 V	HDMI digital video data bus
U3.57	HDMI_VIDEO_DIN5	B16	3.3 V	HDMI digital video data bus
U3.56	HDMI_VIDEO_DIN6	A16	3.3 V	HDMI digital video data bus
U3.55	HDMI_VIDEO_DIN7	C15	3.3 V	HDMI digital video data bus
U3.54	HDMI_VIDEO_DIN8	B14	3.3 V	HDMI digital video data bus
U3.52	HDMI_VIDEO_DIN9	A14	3.3 V	HDMI digital video data bus
U3.50	HDMI_VIDEO_DIN10	A13	3.3 V	HDMI digital video data bus
U3.49	HDMI_VIDEO_DIN11	B12	3.3 V	HDMI digital video data bus
U3.48	HDMI_VIDEO_DIN12	A12	3.3 V	HDMI digital video data bus
U3.47	HDMI_VIDEO_DIN13	C12	3.3 V	HDMI digital video data bus
U3.46	HDMI_VIDEO_DIN14	A11	3.3 V	HDMI digital video data bus
U3.45	HDMI_VIDEO_DIN15	B11	3.3 V	HDMI digital video data bus
U3.44	HDMI_VIDEO_DIN16	A10	3.3 V	HDMI digital video data bus
U3.43	HDMI_VIDEO_DIN17	C14	3.3 V	HDMI digital video data bus
U3.42	HDMI_VIDEO_DIN18	E14	3.3 V	HDMI digital video data bus
U3.41	HDMI_VIDEO_DIN19	D14	3.3 V	HDMI digital video data bus
U3.40	HDMI_VIDEO_DIN20	C13	3.3 V	HDMI digital video data bus

Board Reference (U3)	Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
U3.39	HDMI_VIDEO_DIN21	E15	3.3 V	HDMI digital video data bus
U3.38	HDMI_VIDEO_DIN22	F15	3.3 V	HDMI digital video data bus
U3.37	HDMI_VIDEO_DIN23	D15	3.3 V	HDMI digital video data bus
U3.53	HDMI_VIDEO_CLK	D6	3.3 V	Video clock
U3.63	HDMI_VIDEO_DATA_EN	J13	3.3 V	Video data enable
U3.64	HDMI_HSYNC	H13	3.3 V	Vertical synchronization
U3.2	HDMI_VSYNC	H14	3.3 V	Horizontal synchroniza-tion
U3.28	HDMI_INTR	A18	3.3 V	Interrupt signal
U3.35	HDMI_SCL	C16	3.3 V	HDMI I2C clock
U3.36	HDMI_SDA	B17	3.3 V	HDMI I2C data

Pmod Connectors

The MAX 10 10M50 Evaluation Kit features two Digilent Pmod™ compatible headers, which are used to connect low frequency, low I/O pin count peripheral modules.

The 12-pin version Pmod connector used in this kit provides 8 I/O signal pins. The peripheral module interface also encompasses a variant using I2C interface, and two or four wire MTE cables. The Pmod signals are connected to Bank 8.

Table 3-14: Pmod A Pin Assignments, Signal Names and Functions

Schematic Signal Name	Schematic Share Bus Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
PMODA_D0	PMODA_IO0	A6	3.3 V	In/Out
PMODA_D1	PMODA_IO1	E8	3.3 V	In/Out
PMODA_D2	PMODA_IO2	B4	3.3 V	In/Out
PMODA_D3	PMODA_IO3	A5	3.3 V	In/Out
PMODA_D4	PMODA_IO4	B7	3.3 V	In/Out
PMODA_D5	PMODA_IO5	E9	3.3 V	In/Out
PMODA_D6	PMODA_IO6	A4	3.3 V	In/Out
PMODA_D7	PMODA_IO7	B5	3.3 V	In/Out
---	VCC	---	3.3 V	Power

Schematic Signal Name	Schematic Share Bus Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
---	GND	---	---	GND

Table 3-15: Pmod B Pin Assignments, Signal Names and Functions

Schematic Signal Name	Schematic Share Bus Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
PMODB_D0	PMODB_IO0	C8	3.3 V	In/Out
PMODB_D1	PMODB_IO1	D8	3.3 V	In/Out
PMODB_D2	PMODB_IO2	A3	3.3 V	In/Out
PMODB_D3	PMODB_IO3	A2	3.3 V	In/Out
PMODB_D4	PMODB_IO4	B3	3.3 V	In/Out
PMODB_D5	PMODB_IO5	C2	3.3 V	In/Out
PMODB_D6	PMODB_IO6	B1	3.3 V	In/Out
PMODB_D7	PMODB_IO7	B2	3.3 V	In/Out
---	VCC	---	3.3 V	Power
---	GND	---	---	GND

Memory

This section describes the evaluation board's memory interface support and also their signal names, types, and connectivity relative to the FPGA. A soft IP memory controller is required as part of the FPGA design. The memory controller can be a user supplied IP or IP available for purchase from Intel PSG (formerly Altera) or a partner.

LPDDR2

The MAX 10 FPGA provides full-speed support to a x16 LPDDR2 200-MHz interface by using a 1Gbit x 16 memory.

Table 3-16: LPDDR2 Pin Assignments, Signal Names, and Functions

Board Reference (U2)	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
U2.P3	LPDDR2_CA0	J22	1.2V HSUL	Command/Address Bus Input
U2.N3	LPDDR2_CA1	J21	1.2V HSUL	Command/Address Bus Input
U2.M3	LPDDR2_CA2	F22	1.2V HSUL	Command/Address Bus Input
U2.M2	LPDDR2_CA3	H21	1.2V HSUL	Command/Address Bus Input

Board Reference (U2)	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
U2.M1	LPDDR2_CA4	H22	1.2V HSUL	Command/Address Bus Input
U2.G2	LPDDR2_CA5	D22	1.2V HSUL	Command/Address Bus Input
U2.F2	LPDDR2_CA6	C22	1.2V HSUL	Command/Address Bus Input
U2.F3	LPDDR2_CA7	E22	1.2V HSUL	Command/Address Bus Input
U2.E3	LPDDR2_CA8	A21	1.2V HSUL	Command/Address Bus Input
U2.E2	LPDDR2_CA9	B22	1.2V HSUL	Command/Address Bus Input
U2.K1	LPDDR2_CKE	E21	1.2V HSUL	Clock Enable
U2.L1	LPDDR2_CSn	G22	1.2V HSUL	Chip Select
U2.J3	LPDDR2_CK	D18	Differential 1.2V HSUL	Differential Input Clock
U2.H3	LPDDR2_CKn	E18	Differential 1.2V HSUL	Differential Input Clock
U2.N8	LPDDR2_DQ0	N18	1.2V HSUL	Data Bus Byte Lane 0
U2.M8	LPDDR2_DQ1	N20	1.2V HSUL	Data Bus Byte Lane 0
U2.M7	LPDDR2_DQ2	M20	1.2V HSUL	Data Bus Byte Lane 0
U2.M9	LPDDR2_DQ3	M14	1.2V HSUL	Data Bus Byte Lane 0
U2.M6	LPDDR2_DQ4	M18	1.2V HSUL	Data Bus Byte Lane 0
U2.L7	LPDDR2_DQ5	M15	1.2V HSUL	Data Bus Byte Lane 0
U2.L8	LPDDR2_DQ6	L20	1.2V HSUL	Data Bus Byte Lane 0
U2.L9	LPDDR2_DQ7	L18	1.2V HSUL	Data Bus Byte Lane 0
U2.G9	LPDDR2_DQ8	K20	1.2V HSUL	Data Bus Byte Lane 1
U2.G8	LPDDR2_DQ9	K19	1.2V HSUL	Data Bus Byte Lane 1
U2.G7	LPDDR2_DQ10	K18	1.2V HSUL	Data Bus Byte Lane 1
U2.F6	LPDDR2_DQ11	H19	1.2V HSUL	Data Bus Byte Lane 1
U2.F9	LPDDR2_DQ12	H20	1.2V HSUL	Data Bus Byte Lane 1
U2.F7	LPDDR2_DQ13	H18	1.2V HSUL	Data Bus Byte Lane 1
U2.F8	LPDDR2_DQ14	J14	1.2V HSUL	Data Bus Byte Lane 1
U2.E8	LPDDR2_DQ15	J18	1.2V HSUL	Data Bus Byte Lane 1
U2.L6	LPDDR2_DQS0	L14	Differential 1.2V HSUL	Data Strobe P Byte Lane 0

Board Reference (U2)	Schematic Signal Name	MAX 10 FPGA Pin Number	I/O Standard	Description
U2.L5	LPDDR2_DQS0n	L15	Differential 1.2V HSUL	Data Strobe N Byte Lane 0
U2.G6	LPDDR2_DQS1	K14	Differential 1.2V HSUL	Data Strobe Byte P Lane 1
U2.G5	LPDDR2_DQS1n	K15	Differential 1.2V HSUL	Data Strobe Byte N Lane 1
U2.K5	LPDDR2_DM0	N19	1.2V HSUL	Input Data Mask Byte Lane 0
U2.H5	LPDDR2_DM1	J15	1.2V HSUL	Input Data Mask Byte Lane 1
U2.D3	LPDDR2_ZQ	/	1.2V HSUL	Output Drive Strength Calibration

Caution: When customers start their own design (with unique PCB layout) and still wish to use the LPDDR2 interface, they should target the 10M50DCF484I6G or 10M50DAF484I6G. For other MAX 10 parts that support LPDDR2 interfaces (include any 10M16 or higher density MAX 10 device, with dual supply, F256 or higher pin-count, and –i6 speed grade), Quartus access to these parts requires contacting the local Altera sales person to provide the designer with a special .INI variable.

Flash

The MAX 10 10M50 Evaluation Kit provides a 512-Mb (megabit) quad SPI flash memory. Altera Generic QUAD SPI controller core is used by default to erase, read, and write quad SPI flash in reference designs of the Board Test System (BTS) installer.

If you use the parallel flash loader (PFL) IP to program the quad SPI flash, you need to generate a **.pof** (Programmer Object File) to configure the device.

Perform the following steps to generate a **.pof** file:

1. Create a byte-order **Quartus.ini** file with the setting:

   ```
   PGMIO_SWAP_HEX_BYTE_DATA=ON
   ```
2. Copy the **.ini** file to the project root directory and open the project with Quartus
3. Open **Convert Programming Files** tool to generate the **.pof** file

Table 3-17: Default Memory Map of the 512-Mb Quad SPI Flash

Block Description	Size (KB)	Address Range
Board Test System Scratch	512	0x03F8.0000 - 0x03FF.FFFF
User Software	56640	0x0083.0000 - 0x03F7.FFFF
Factory Software	4096	0x0043.0000 - 0x0082.FFFF
Board Information	64	0x0002.0000 - 0x0002.FFFF

Block Description	Size (KB)	Address Range
User Design Reset Vector	64	0x0000.0000 - 0x0000.FFFF

Table 3-18: Flash Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U23)	Signal Name	Device/Pin Number	I/O standard	Description
U23.7	FLASH_CSn	MAX 10/A8	3.3 V	Chip select
U23.16	FLASH_CLK	MAX 10/A9	3.3 V	Clock
U23.3	FLASH_RESETn	MAX 10/B8 MAX II/U14	3.3 V	Reset
U23.15	FLASH_D0	MAX 10/C9	3.3 V	Address Bus
U23.8	FLASH_D1	MAX 10/C10	3.3 V	Address Bus
U23.9	FLASH_D2	MAX 10/C11	3.3 V	Address Bus
U23.1	FLASH_D3	MAX 10/A7	3.3 V	Address Bus

MIPI CSI-2 Transmitter

The MAX 10 FPGA 10M50 evaluation kit supports one MIPI CSI-2 transmitter D-PHY to Leopard LI-MIPI-USB3-Tester module. This module includes one MIPI clock channel and four MIPI data channels. To interface the CSI-2 D-PHY compliant I/Os, the MAX 10 FPGA 10M50 Evaluation Kit uses one 1.8V HSTL signal pair and one 2.5V LVCMOS signal pair to support both high-speed and low-power nodes of one MIPI clock or data lane. The control signals (RST, SCLK, and SDATA) for LI-MIPI-USB3-Tester are implemented with both 1.8V and 3.3V options.

Caution: The implemented D-PHY resistor values need to be adjusted based on user design. Simulation and signal quality measurement is required for optimal resistor values. Consult Application Note **AN-754** for technical details on implementing the D-PHY passive circuits. The user must also install control signal path resistors (SCLK, SDATA, RST_IO) depending upon the I/O level desired.

Table 3-19: MIPI CSI-2 Transmitter Pin Assignments, Signal Names and Functions

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J1 (Cable needed to interface LI-MIPI-USB3-Tester module)		P/N: Molex 52559-3652		
J1.26	MIPI_TX_CLK_HS_P	MAX 10/ R2	1.8V HSTL	Differential output clock (high-speed, positive terminal)

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J1.25	MIPI_TX_CLK_HS_N	MAX 10/ R1	1.8V HSTL	Differential output clock (high-speed, negative terminal)
J1.26	MIPI_TX_CLK_LP_P	MAX 10/ Y2	2.5V LVCMOS	Differential output clock (low power, positive terminal)
J1.25	MIPI_TX_CLK_LP_N	MAX 10/ Y1	2.5V LVCMOS	Differential output clock (low power, negative terminal)
J1.29	MIPI_TX_DATA_HS_P1	MAX 10/ N1	1.8V HSTL	Differential output data Lane1 (high speed, positive terminal)
J1.28	MIPI_TX_DATA_HS_N1	MAX 10/ P1	1.8V HSTL	Differential output data Lane1 (high speed, negative terminal)
J1.29	MIPI_TX_DATA_LP_P1	MAX 10/ V5	2.5V LVCMOS	Differential output data Lane1 (high speed, positive terminal)
J1.28	MIPI_TX_DATA_LP_N1	MAX 10/ V4	2.5V LVCMOS	Differential output data Lane1 (high speed, negative terminal)
J1.23	MIPI_TX_DATA_HS_P2	MAX 10/ T2	1.8V HSTL	Differential output data Lane2 (high speed, positive terminal)
J1.22	MIPI_TX_DATA_HS_N2	MAX 10/ T1	1.8V HSTL	Differential output data Lane2 (high speed, negative terminal)
J1.23	MIPI_TX_DATA_LP_P2	MAX 10/ AB3	2.5V LVCMOS	Differential output data Lane2 (high speed, positive terminal)
J1.22	MIPI_TX_DATA_LP_N2	MAX 10/ AB2	2.5V LVCMOS	Differential output data Lane2 (low power, negative terminal)
J1.20	MAX_TX_DATA_HS_P3	MAX 10/ V1	1.8V HSTL	Differential output data Lane3 (low power, positive terminal)
J1.19	MAX_TX_DATA_HS_N3	MAX 10/ U1	1.8V HSTL	Differential output data Lane3 (high speed, negative terminal)
J1.20	MAX_TX_DATA_LP_P3	MAX 10/ AB5	2.5V LVCMOS	Differential output data Lane3 (low power, positive terminal)

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J1.19	MAX_TX_DATA_LP_N3	MAX 10/ AA5	2.5V LVCMOS	Differential output data Lane3 (low power, negative terminal)
J1.17	MIPI_TX_DATA_HS_P4	MAX 10/ W2	1.8V HSTL	Differential output data Lane4 (high speed, positive terminal)
J1.16	MIPI_TX_DATA_HS_N4	MAX 10/ W1	1.8V HSTL	Differential output data Lane3 (high speed, negative terminal)
J1.17	MIPI_TX_DATA_HS_P4	MAX 10/ AB7	2.5V LVCMOS	Differential output data Lane4 (low power, positive terminal)
J1.16	MIPI_TX_DATA_HS_N4	MAX 10/ AB6	2.5V LVCMOS	Differential output data Lane4 (low power, negative terminal)
J1.14	MIPI_TX_CMOS_RST_1V8	MAX 10/ T3	1.8V LVCMOS	Reset/Power Down (1.8V)
J1.14	MIPI_TX_CMOS_RST_3V3	MAX 10/ B10	3.3V LVCMOS	Reset/Power Down (3.3V)
J1.13	MIPI_TX_CMOS_SDATA_1V8	MAX 10/ N2	1.8V LVCMOS	Control Bus Data (1.8V)
J1.13	MIPI_TX_CMOS_SDATA_3V3	MAX 10/ H12	3.3V LVCMOS	Control Bus Data (3.3V)
J1.12	MIPI_TX_CMOS_SCLK_1V8	MAX 10/ N3	1.8V LVCMOS	Control Bus Clock (1.8V)
J1.12	MIPI_TX_CMOS_SCLK_3V3	MAX 10/ J11	3.3V LVCMOS	Control Bus Clock (3.3V)
J1.11	MIPI_TX_CLK24MHz	Clock Generator / U14.21	1.8V LVCMOS	24 MHz Reference Clock Output
J1.10	MIPI_TX_GPIO1	MAX 10/ U3	1.8V LVCMOS	GPIO1
J1.9	MIPI_TX_GPIO2	MAX 10/ U2	1.8V LVCMOS	GPIO2
J1.7	MIPI_TX_GPIO3	MAX 10/ U4	1.8V LVCMOS	GPIO3
J1.6	MIPI_TX_GPIO4	MAX 10/ U5	1.8V LVCMOS	GPIO4
J1.5	MIPI_TX_GPIO5	MAX 10/ V3	1.8V LVCMOS	GPIO5
J1.33, J1.32	1.8V_MIPITX	----	1.8V	1.8V
J1.36, J1.35, J1.34	3.3V_MIPITX	----	3.3V	3.3V

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J1.3, J1.4, J1.8, J1.15, J1.18, J1.21, J1.24, J1.27, J1.30, J1.31	GND		GND	GND

To download MIPI reference designs for this Evaluation Kit, please contact your local Intel PSG (formerly Altera) sales team for assistance or check the **DesignStore**.

MIPI CSI-2 Receiver

The MAX 10 FPGA 10M50 Evaluation Kit supports MIPI CSI-2 receiver D-PHY to both Leopard Imaging OV10640 and UDOO OV5640 modules. The OV10640 module includes one MIPI clock channel and four MIPI data channels, while the OV5640 module has one MIPI clock channel and two MIPI data channels.

To interface MIPI CSI-2 D-PHY compliant I/O, the MAX 10 10M50 evaluation kit uses one 2.5V LVDS signal pair to support high-speed mode and one 1.2V HSTL signal pair to support low-power mode for each MIPI clock or data lane.

Caution: The implemented D-PHY resistor values need to be adjusted based on user design. Simulation and signal quality measurement is required for optimal resistor values. Consult Application Note **AN-754** for technical details on implementing the D-PHY passive circuits.

Table 3-20: MIPI CSI-2 Receiver (for OV10640 module) Pin Assignments, Signal Names and Functions

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J2 (Cable needed to interface OV10640 module)		P/N: 52559-3652		
J2.11	OV10640_CLK_HS_P	MAX 10/P11	2.5V LVDS	Differential input clock (high speed, positive terminal)
J2.12	OV10640_CLK_HS_N	MAX 10/R11	2.5V LVDS	Differential input clock (high speed, negative terminal)
J2.11	OV10640_CLK_LP_P	MAX 10/T21	1.2V HSTL	Differential input clock (low power, positive terminal

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J2.12	OV10640_CLK_LP_N	MAX 10/T22	1.2V HSTL	Differential input clock (low power, negative terminal
J2.8	OV10640_DATA_HS_P1	MAX 10/AA20	2.5V LVDS	Differential input data Lane1 (high speed, positive terminal)
J2.9	OV10640_DATA_HS_N1	MAX 10/AB21	2.5V LVDS	Differential input data Lane1 (high speed,negative terminal)
J2.8	OV10640_DATA_LP_P1	MAX 10/P21	1.2V HSTL	Differential input data Lane1 (low power,positive terminal)
J2.9	OV10640_DATA_LP_N1	MAX 10/N22	1.2V HSTL	Differential input data Lane1 (low power, negative terminal)
J2.14	OV10640_DATA_HS_P2	MAX 10/AB20	2.5V LVDS	Differential input data Lane2 (high speed, positive terminal)
J2.15	OV10640_DATA_HS_N2	MAX 10/AB19	2.5V LVDS	Differential input data Lane2 (high speed, negative terminal
J2.14	OV10640_DATA_LP_P2	MAX 10/V21	1.2V HSTL	Differential input data Lane2 (low power,positive terminal)
J2.15	OV10640_DATA_LP_N2	MAX 10/V22	1.2V HSTL	Differential input data Lane2 (low power, negative terminal
J2.17	OV10640_DATA_HS_P3	MAX 10/AB18	2.5V LVDS	Differential input data Lane3 (high speed, positive terminal)
J2.18	OV10640_DATA_HS_N3	MAX 10/AB17	2.5V LVDS	Differential input data Lane3 (high speed, negative terminal)
J2.17	OV10640_DATA_LP_P3	MAX 10/Y22	1.2V HSTL	Differential input data Lane3 (low power, positive terminal)
J2.18	OV0640_DATA_LP_N3	MAX 10/W22	1.2V HSTL	Differential input data Lane3 (low power, negative terminal)
J2.20	OV10640_DATA_HS_P4	MAX 10/AA16	2.5V LVDS	Differential input data Lane4 (high speed, positive terminal)

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J2.21	OV10640_DATA_HS_N4	MAX 10/AB16	2.5V LVDS	Differential input data Lane4 (high speed, negative terminal)
J2.20	OV10640_DATA_LP_P4	MAX 10/AA21	1.2V HSTL	Differential input data Lane4 (low power, positive terminal)
J2.21	OV10640_DATA_LP_N4	MAX 10/AA22	1.2V HSTL	Differential input data Lane4 (low power, negative terminal)
J2.23	OV10640_CMOS_RST	MAX 10/P4	1.8V LVCMOS	Reset/Power down
J2.24	OV10640_CMOS_SDATA	MAX 10/N8	1.8V LVCMOS	Control Bus Data
J2.25	OV10640_CMOS_SCLK	MAX 10/P5	1.8V LVCMOS	Control Bus Clock
J2.26	OV10640_24MHz	MAX 10/N5	1.8V LVCMOS	24 MHz Reference Clock Output
J2.27	OV10640_GYRO_INT	MAX 10/N9	1.8V LVCMOS	Gyroscope Programmable Interrupt
J2.28	OV10640_G_RDY	MAX 10/R4	1.8V LVCMOS	Gyroscope Data Ready
J2.31	OV10640_XM_INT1	MAX 10/R7	1.8V LVCMOS	Accelerometer and magnetic sensor interrupt 1
J2.30	OV10640_XM_INT2	MAX 10/R5	1.8V LVCMOS	Accelerometer and magnetic sensor interrupt 2
J2.32	OV10640_FSIN	MAX 10/P8	1.8V LVCMOS	Frame sync input
J2.4, J2.5	1.8V	----	1.8V	1.8V
J2.1, J2.2, J2.3	3.3V	----	3.3V	3.3V
J2.6, J2.7, J2.10, J2.13, J2.16, J2.19, J2.22, J2.29, J2.33, J2.34	GND	----	GND	GND

Table 3-21: MIPI CSI-2 Receiver (for OV5640 module) Pin Assignments, Signal Names and Functions

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J3 (Cable needed to interface OV5640 module)		Wurth Electronics 68711614522		
J3.6	OV5640_CLK_HS_P	MAX 10/V10	2.5V LVDS	Differential input clock (high speed, positive terminal)
J3.5	OV5640_CLK_HS_N	MAX 10/V9	2.5V LVDS	Differential input clock (high speed, negative terminal)
J3.6	OV5640_CLK_LP_P	MAX 10/R15	1.2V HSTL	Differential input clock (low power, positive terminal)
J3.5	OV5640_CLK_LP_N	MAX 10/R14	1.2V HSTL	Differential input clock (high speed, positive terminal)
J3.9	OV5640_DATA_HS_P1	MAX 10/AB13	2.5V LVDS	Differential input data Lane1 (high speed,positive terminal)
J3.8	OV5640_DATA_HS_N1	MAX 10/AB12	2.5V LVDS	Differential input data Lane1 (high speed,negative terminal)
J3.9	OV5640_DATA_LP_P1	MAX 10/W19	1.2V HSTL	Differential input data Lane1 (low power,positive terminal)
J3.8	OV5640_DATA_LP_N1	MAX 10/W20	1.2V HSTL	Differential input data Lane1 (low power,negative terminal)
J3.2	OV5640_DATA_HS_P2	MAX 10/AB11	2.5V LVDS	Differential input data Lane2 (high speed,positive terminal)
J3.1	OV5640_DATA_HS_N2	MAX 10/AB10	2.5V LVDS	Differential input data Lane2 (high speed,negative terminal)
J3.2	OV5640_DATA_LP_P2	MAX 10/P15	1.2V HSTL	Differential input data Lane2 (low power,positive terminal)
J3.1	OV5640_DATA_LP_N2	MAX 10/P14	1.2V HSTL	Differential input data Lane2 (low power,negative terminal)
J3.13	OV5640_SDC	MAX 10/M3	3.3V LVCMOS	Control Bus Clock

Source	Schematic Signal Name	Device/Pin Number	I/O Standard	Description
J3.14	OV5640_SDA	MAX 10/L1	3.3V LVCMOS	Control Bus Data
J3.12	OV5640_ CLK24MHz	Clock Generator / U14.18	3.3V LVCMOS	System Input Clock
J3.15	OV5640_CAM_ RESETB	MAX 10/M4	3.3V LVCMOS	Reset
J3.11	OV5640_PWRON	MAX 10/L2	3.3V LVCMOS	Power Down
J3.16	3.3V	----	3.3V	3.3V
J3.3, J3.4, J3.7, J3.10	GND	----	GND	GND

To download MIPI reference designs for this Evaluation Kit, please contact your local Intel PSG (formerly Altera) sales team for assistance or check the **DesignStore**.

Power Supply

The evaluation kit is powered up through a DC power adapter or USB cable. The yellow LEDs D9, D10 and D11 illuminate when the board is powered up.

Power Options

You can apply power to the MAX 10 FPGA Evaluation Kit by plugging in either 5V DC power adapter to wall jack, or USB cable to your PC. For low-power design, USB cable connection is suggested, and it can easily provide both power and on-board USB Blaster connection. For high-power design, DC adapter solution is preferred to ensure device performance.

The board includes one Jumper (J11) for power option selection. When use DC power adapter, J11 needs to be placed at Position 1 and 2; while for using USB power, J11 needs to be placed at Position 2 and 3. The USB power is default power setup.

Resistors (R292 and R293) can be populated and used in place of the jumper if you want to hard wire the power option.

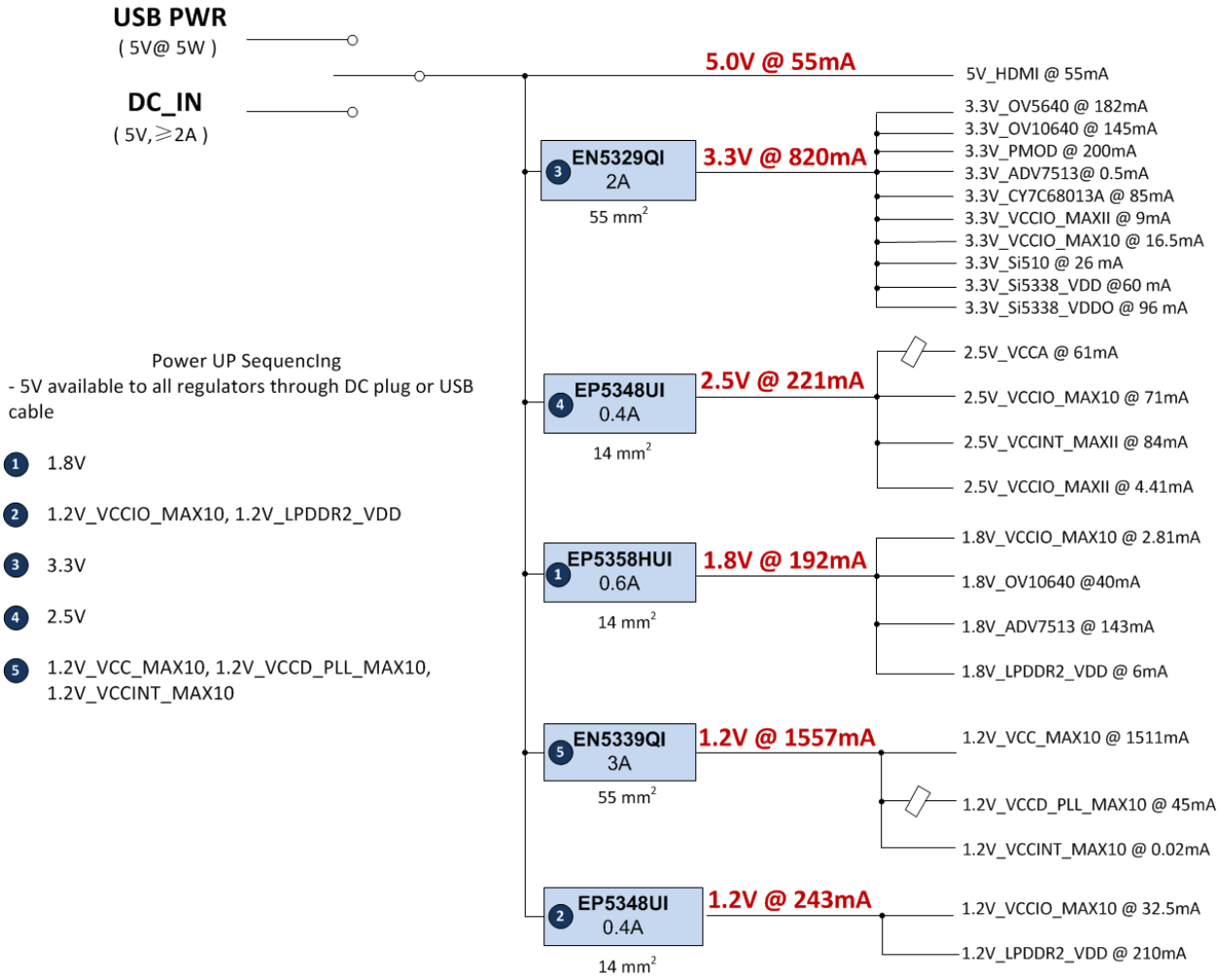
When powered correctly, D9, D10 and D11 will light.

Caution: Resistors R292 and R293 are designed for hard wiring the power selection. J11 must not be used when either R292 or R293 is populated.

Power Up Sequence

The figure below shows the power distribution system on the MAX 10 FPGA 10M50 Evaluation Board.

Figure 3-5: Power Tree



The power up sequence of the MAX 10 FPGA 10M50 Evaluation Board is shown in the table below:

Table 3-22: Power Up Sequence Table

Power Up Sequence	Device	Output Voltage
1	EP5358HUI	1.8V
2	EP5348UI	1.2V
3	EM5329QI	3.3V
4	EP5384UI	2.5V
5	EN5339QI	1.2V

Additional Information A

2016.02.29

UG-20006

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This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Table A-1: MAX 10 10M50 FPGA Evaluation Kit History

Version	Release Date	Description
Production Kit	February 2016	Initial Release for Rev. A board

Compliance & Conformity Statements

CE EMI Conformity Caution

This evaluation kit is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the responsibility of the user.

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