EN6310QI 1A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN6310QI is an Intel® Enpirion® Power System on a Chip (PowerSoC) DC-DC converter. It integrates the inductor, MOSFET switches, small-signal circuits and compensation in an advanced 4mm x 5mm x 1.85mm 30-pin QFN package.

The EN6310QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architectures. The device's advanced circuit techniques, high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- Integrated inductor, MOSFET and Controller
- Small 4mm x 5mm x 1.85mm QFN
- High Efficiency up to 96%
- Solution Footprint Less than 65mm^2
- 1A Continuous Output Current
- VIN Range of 2.7V to 5.5V
- VOUT Range from 0.6V to 3.3V
- Programmable Soft Start and Power OK Flag
- Fast Transient Response and Recovery Time
- Low Noise and Low Output Ripple; 4mV Typical
- 2.2MHz Switching Frequency
- Under Voltage Lock-out (UVLO), Short Circuit, Over Current and Thermal Protection

APPLICATIONS

- Altera FPGAs (MAX, ARRIA, CYCLONE, STRATIX)
- Low Power FPGA Applications
- All SERDES and IO Supplies Requiring Low Noise
- Applications Requiring High Efficiency
- Enterprise Grade Solid State Drive (SSD)
- Noise Sensitive Wireless and RF Application

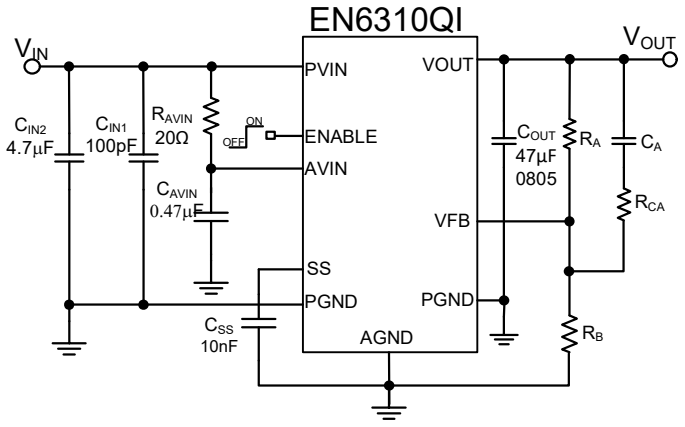


Figure 1: Simplified Applications Circuit

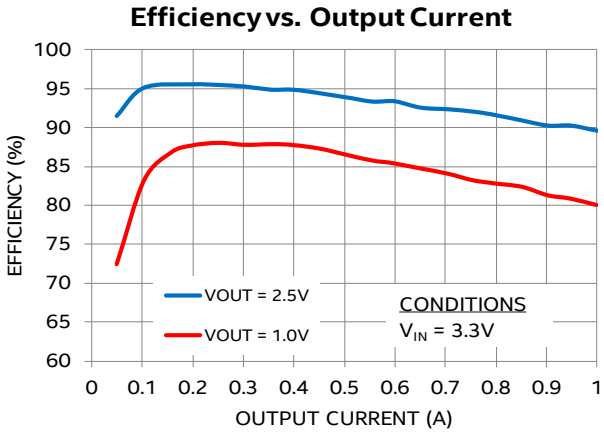


Figure 2: Efficiency at V_{IN} = 5V

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN6310QI	N6310QI	-40°C to +125°C	30-pin (4mm x 5mm x 1.85mm) QFN
EVB-EN6310QI	N6310QI	QFN Evaluation Board	

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

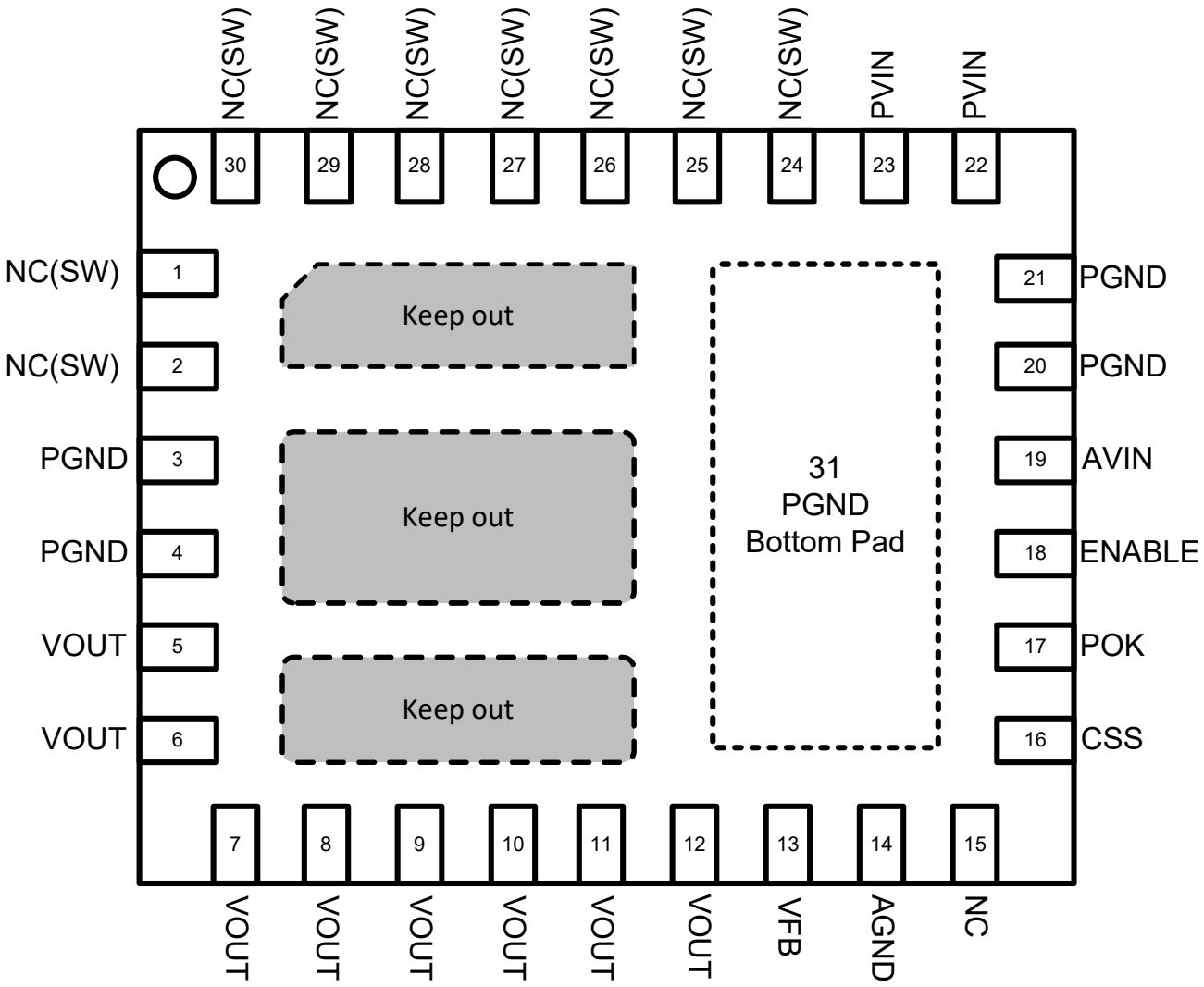


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

NOTE C: Keep-Out are No Connect pads that should not to be electrically connected to each other or to any external signal, ground or voltage. They do not need to be soldered to the PCB.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 2, 24-30	NC(SW)	-	No Connect. These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
3, 4, 20, 21	PGND	Ground	Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
5-12	VOUT	Power	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins. Refer to the Layout Recommendation section.
13	VFB	Analog	External feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) and resistor (R_C) are required in parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage being equal to 0.6V.
14	AGND	Power	Ground for internal control circuits. Connect to the power ground plane with a via right next to the pin.
15	NC	-	No Connect. These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
16	SS	Analog	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval. Refer to Soft-Start Operation in the Functional Description section for more details.
17	POK	Digital	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is above 90% of VOUT nominal. Leave this pin floating if not used.
18	ENABLE	Analog	Input Enable. Applying logic high will enable the device and initiate a soft-start. Applying logic low disables the output and switching stops.
19	AVIN	Power	Input power supply for the controller. Connect to input voltage at a quiet point. Refer to the Layout Recommendation section.
22, 23	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pin. Refer to the Layout Recommendation section.
31	PGND	Ground	Power ground thermal pad. Not a perimeter pin. Connect thermal pad to the system GND plane for heat-sinking purposes. Refer to the Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	6.6	V
ENABLE, POK		-0.3	V_{IN}+0.3	V
VFB, SS		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.7	5.5	V
Output Voltage Range	V_{OUT}	0.6	3.3	V
Output Current Range	I_{OUT}		1	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	140	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	20	°C
Thermal Resistance: Junction to Ambient (0 LFM) (1)	θ_{JA}	60	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	3	°C/W

(1) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = PVIN = AVIN = 5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	PVIN = AVIN	2.7		5.5	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted		2.3		V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted		1.9		V
Output Voltage Range	V_{OUT}		0.6		3.3	V
Maximum Duty Cycle	D_{MAX}			85		%
Feedback Pin Voltage Intial Accuracy (2)	V_{FB}	T_A = 25°C, V_{IN} = 5.0V, I_{LOAD} = 100mA	0.591	0.6	0.609	V
Output Voltage DC Accuracy		VIN = 3.3V; 0A ≤ I_{OUT} ≤ 1.0A; -40°C ≤ T_A ≤ +85°C	-2.0		+2.25	%
		VIN = 5.0V; 0A ≤ I_{OUT} ≤ 1.0A; -20°C ≤ T_A ≤ +85°C	-2.0		+2.0	%
		VIN = 5.0V; 0A ≤ I_{OUT} ≤ 1.0A; -40°C ≤ T_A ≤ +85°C	-3.0		+2.0	%
Feedback pin Input Leakage Current (3)	I_{FB}	VFB pin input leakage current		100		nA
Continuous Output Current	I_{OUT}				1	A
Over Current Trip Level	I_{OCP}		1.2	1.8		A
OCP Threshold	I_{OCP}	2.7 ≤ VIN ≤ 5.5V	1.2			A
AVIN Shut-Down Current	I_{SD}	ENABLE = Low		175		µA
PVIN Shut-Down Current	I_{SD}	ENABLE = Low		175		µA
ENABLE Pin Logic Threshold	EN_{LOW}	Pin = Low	0.0		0.4	V
	EN_{HIGH}	Pin = High	1.8		VIN	V
ENABLE Pin Input Current	I_{ENABLE}	ENABLE = High		5		µA

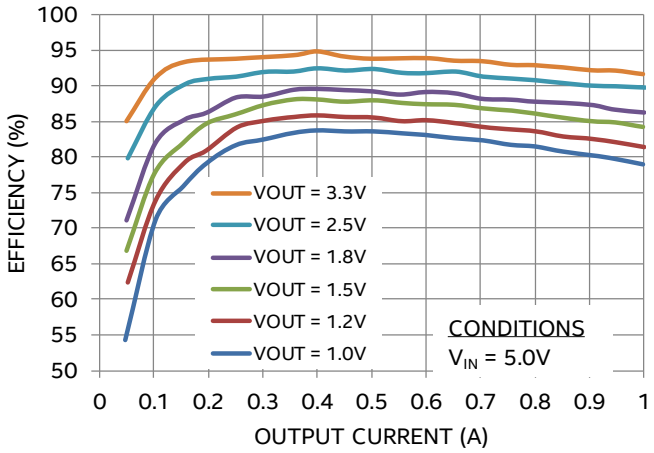
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE Lock-out	ENLO	Time before enable will re-assert internally after being pulled low		12.5		ms
Switching Frequency	f_{SW}			2.2		MHz
Soft Start Time[(2) (3)]	T_{SS}	CSS = 10nF (Note 2 and 3)	5.2	6.5	7.8	ms
Allowable Soft Start Capacitor Range[(3)]	C_{SS}	(Note 3)	0.47		10	nF

(2) Parameter not production tested but is guaranteed by design.

(3) Soft Start Time range does not include capacitor tolerances.

TYPICAL PERFORMANCE CURVES

Efficiency vs. Output Current



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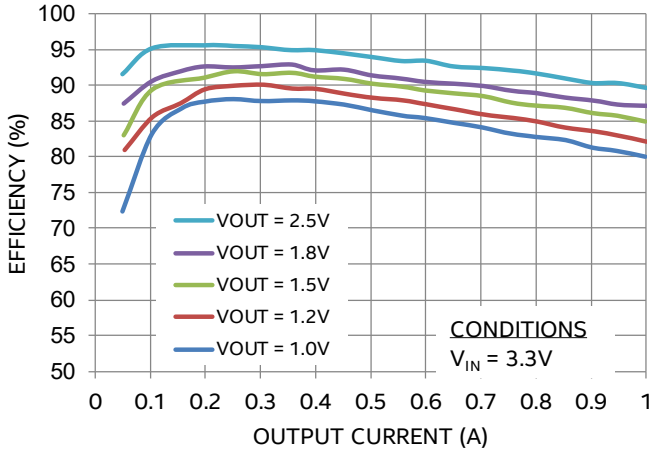
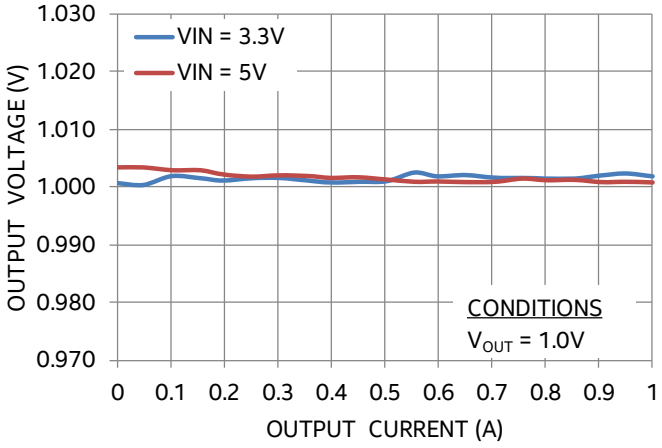


Output Voltage vs. Output Current



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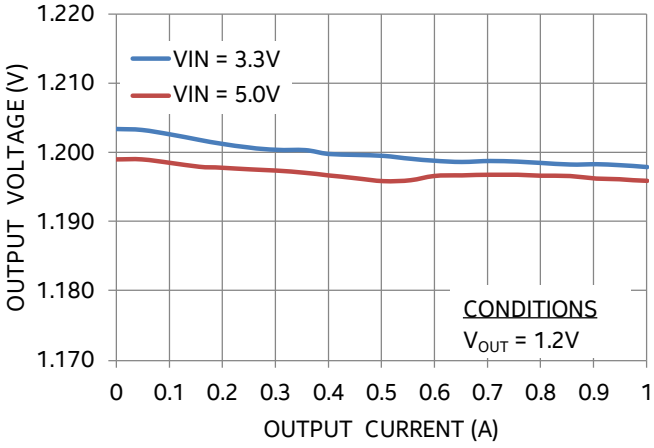

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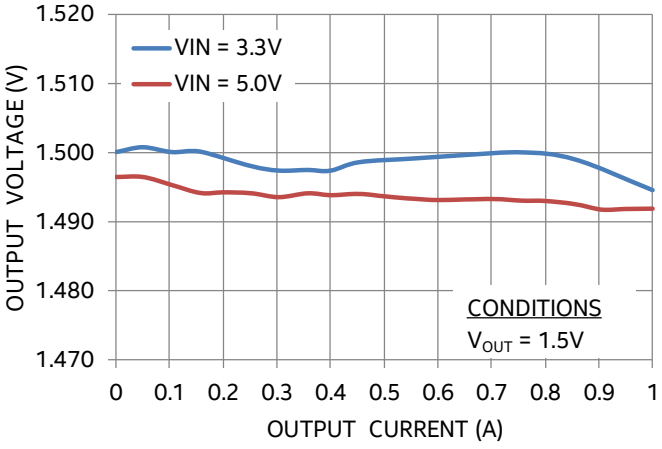

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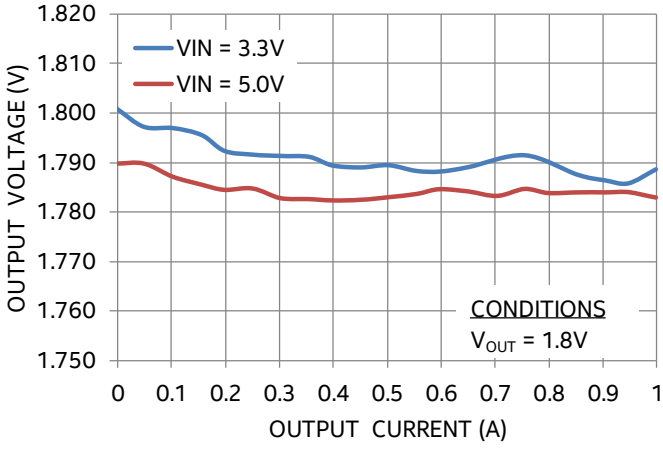
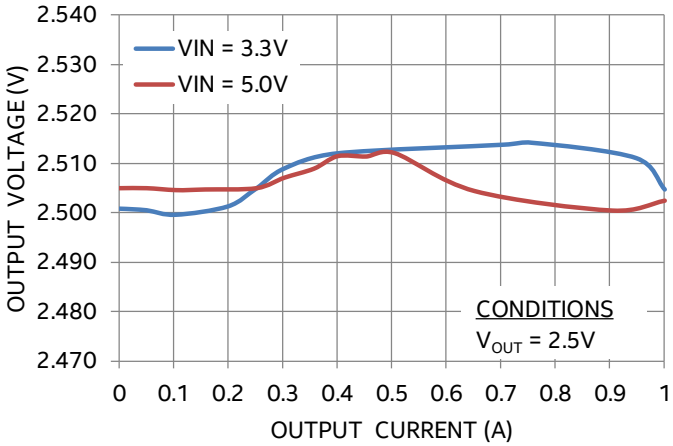
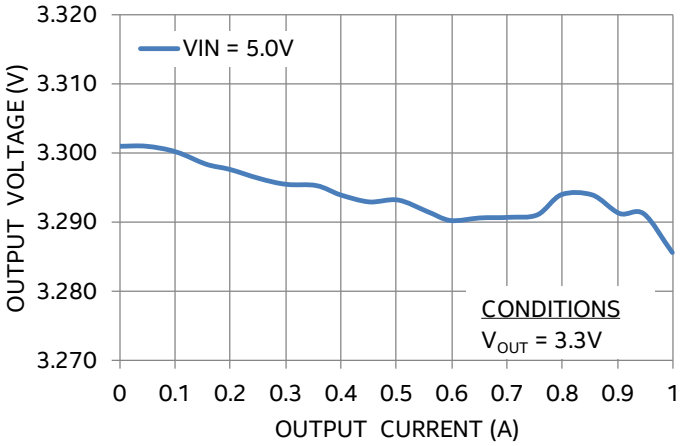


TYPICAL PERFORMANCE CURVES (CONTINUED)

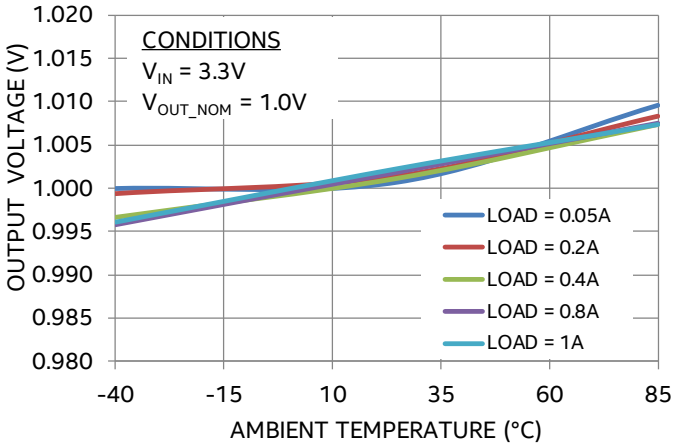
Output Voltage vs. Output Current



Output Voltage vs. Output Current



Output Voltage vs. Temperature



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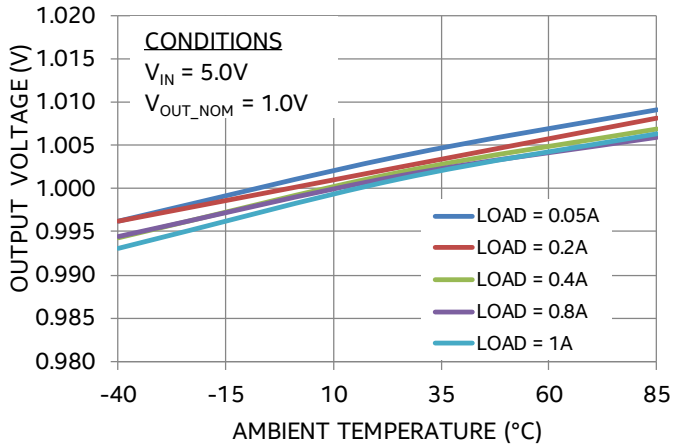

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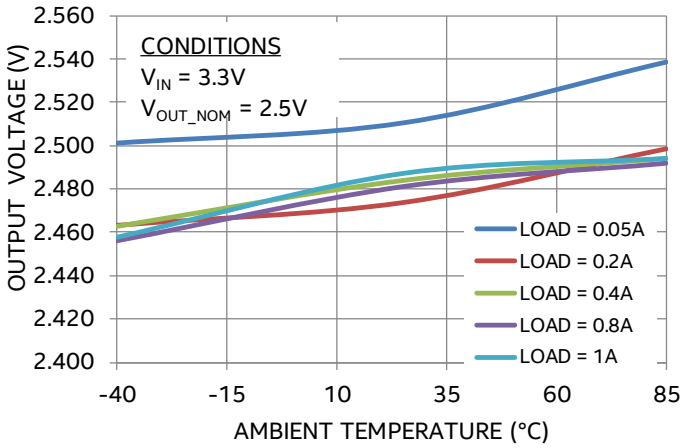
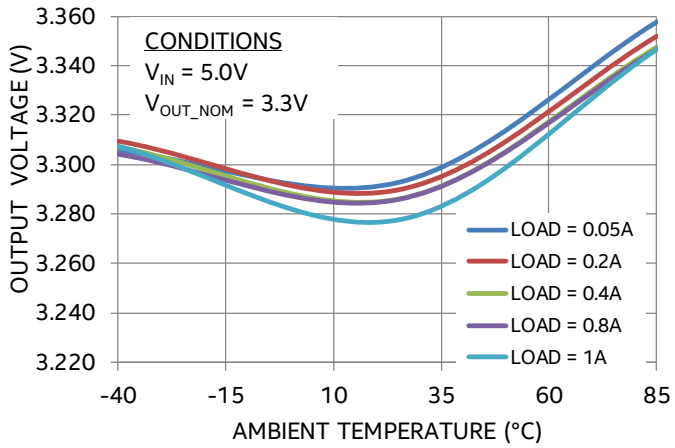
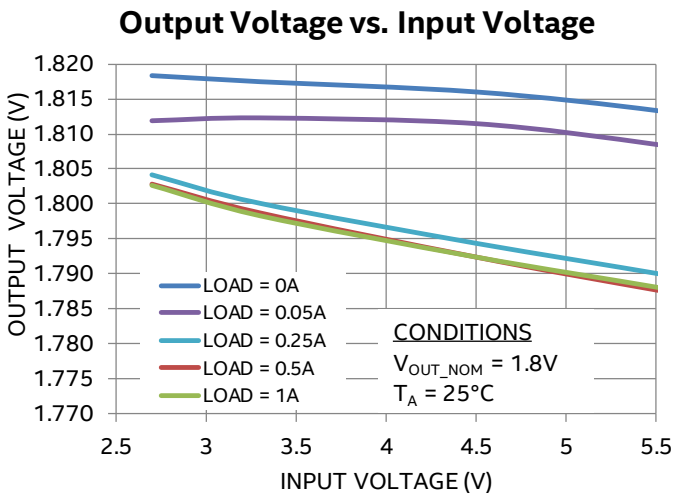
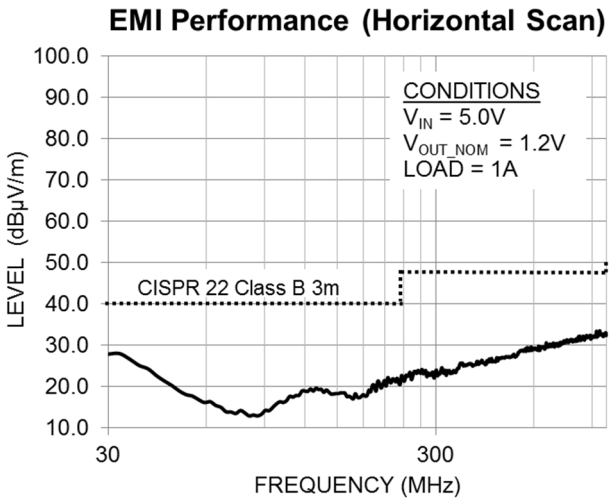


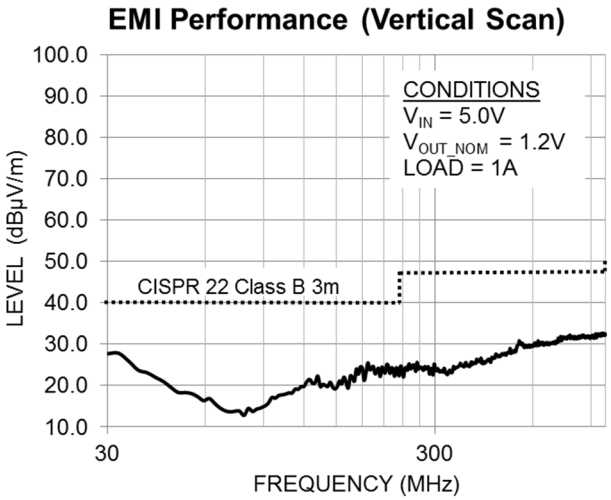
Output Voltage vs. Temperature



TYPICAL PERFORMANCE CURVES (CONTINUED)

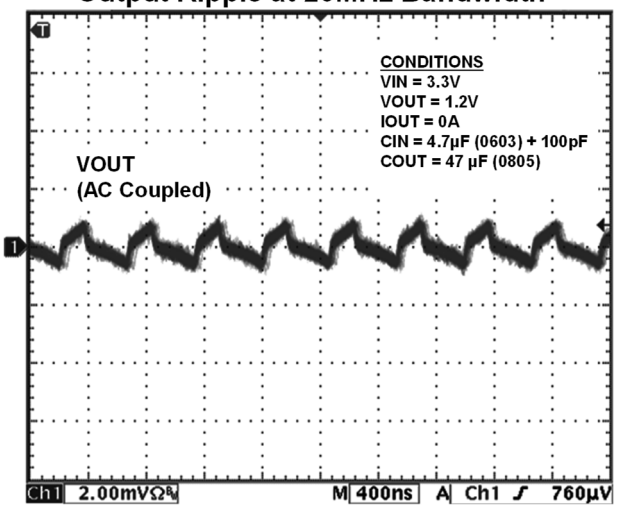




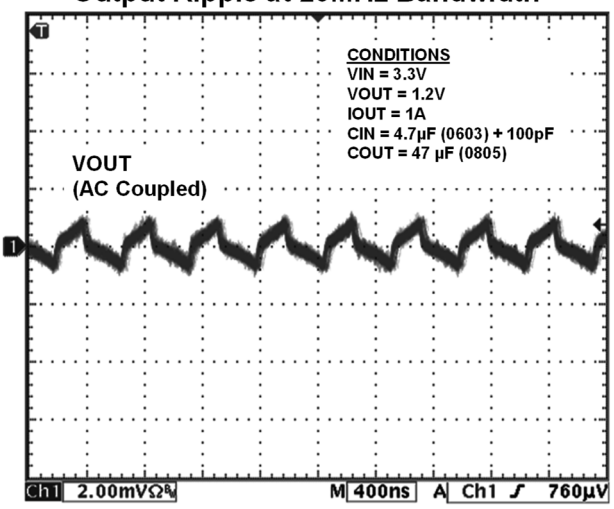


TYPICAL PERFORMANCE CHARACTERISTICS

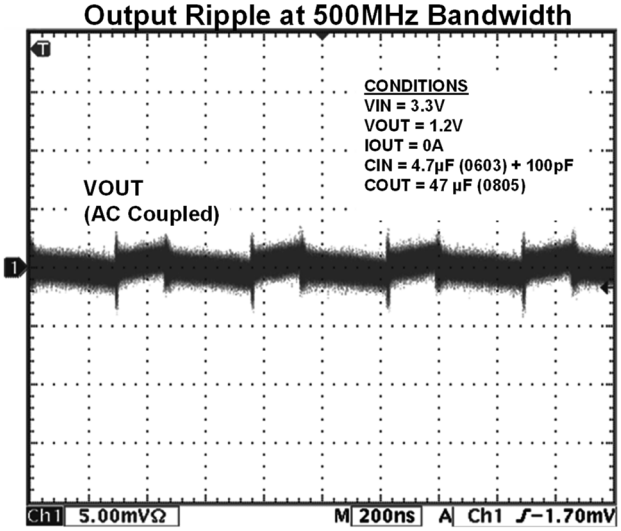
Output Ripple at 20MHz Bandwidth



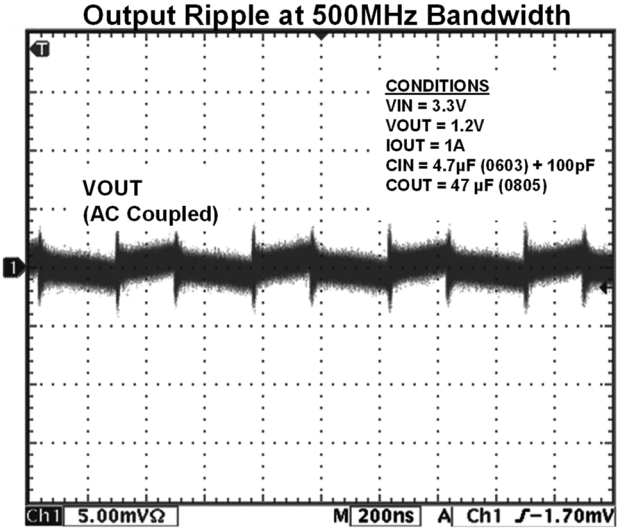
Output Ripple at 20MHz Bandwidth



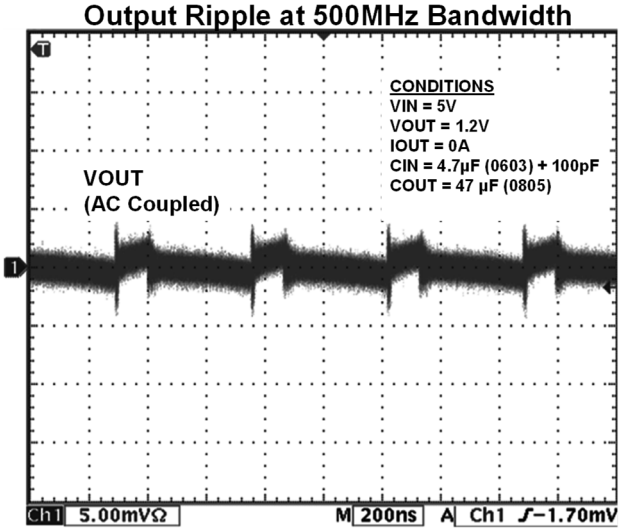
Output Ripple at 500MHz Bandwidth



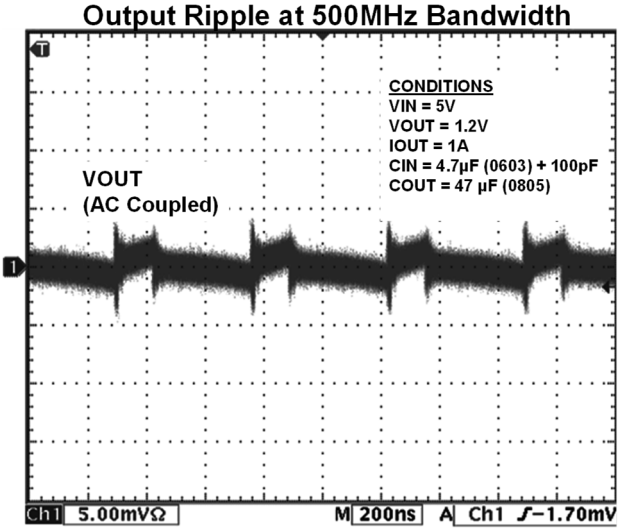
Output Ripple at 500MHz Bandwidth



Output Ripple at 500MHz Bandwidth

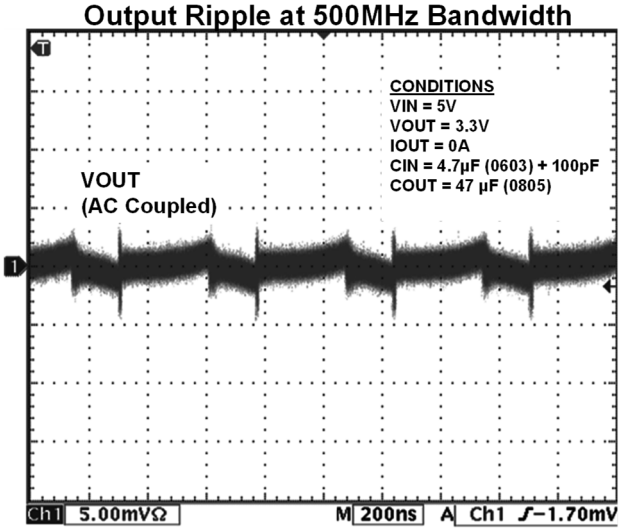


Output Ripple at 500MHz Bandwidth

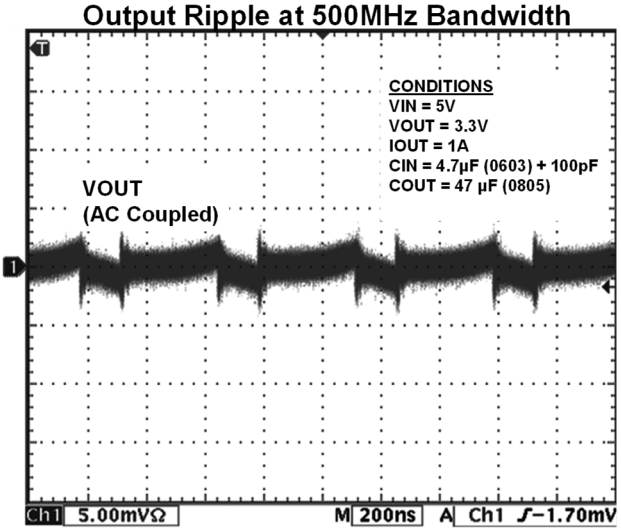


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

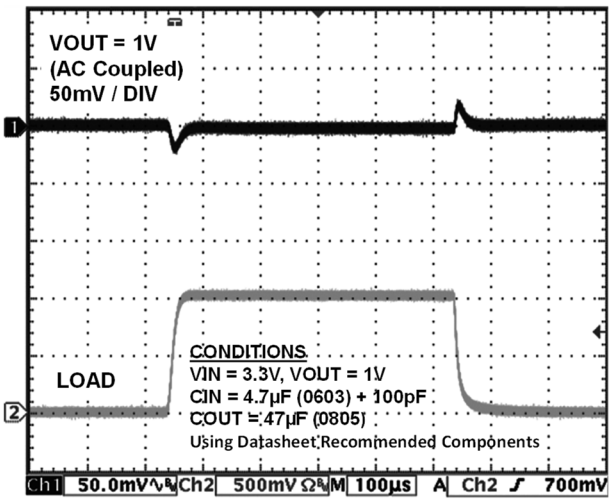
Output Ripple at 500MHz Bandwidth



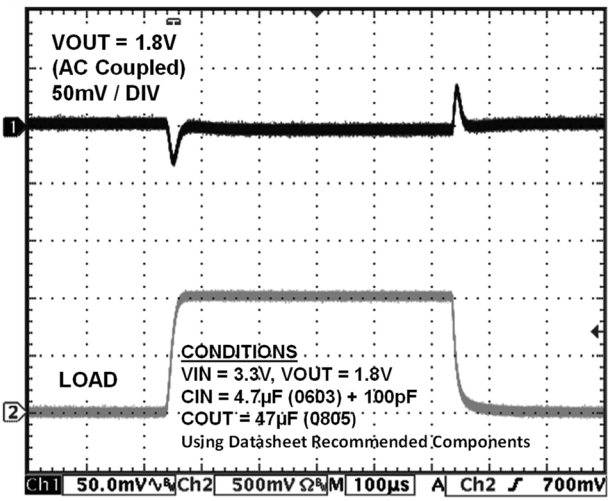
Output Ripple at 500MHz Bandwidth



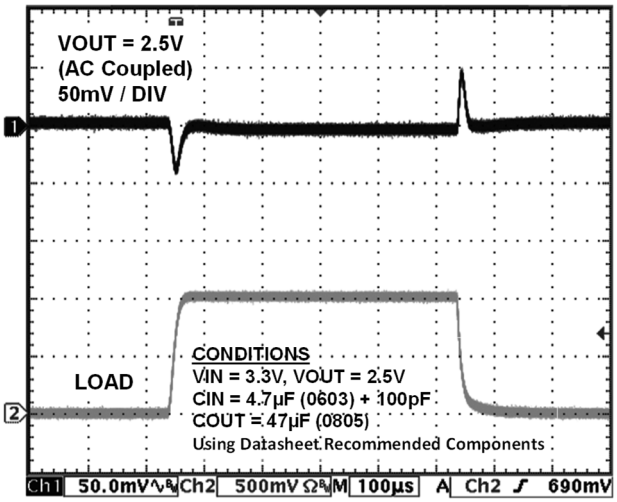
Load Transient from 0A to 1A



Load Transient from 0A to 1A



Load Transient from 0A to 1A



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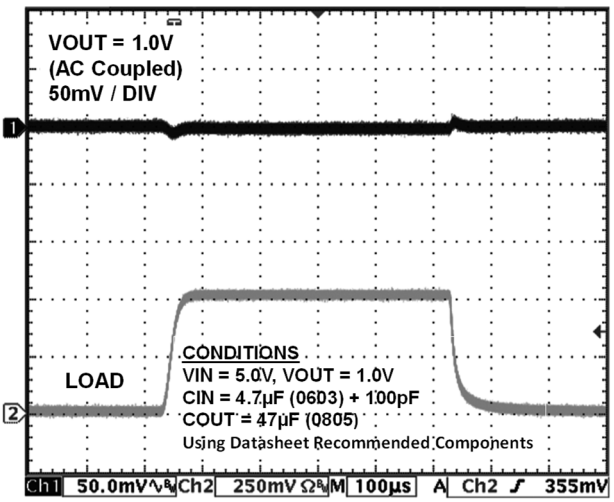
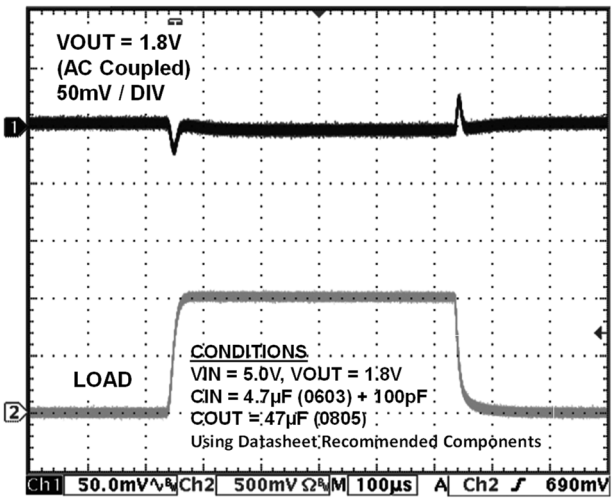


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Load Transient from 0A to 1A



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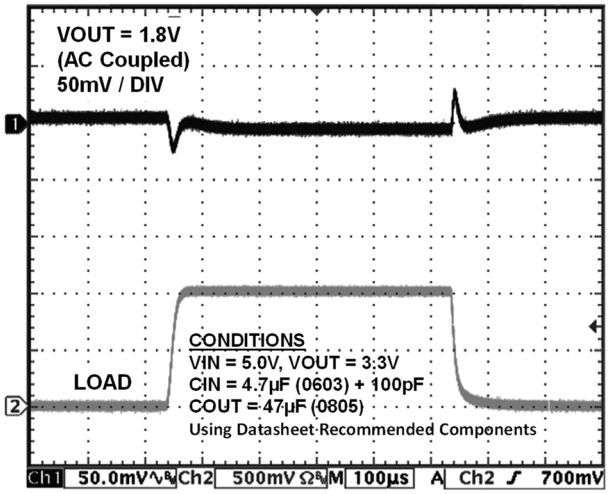
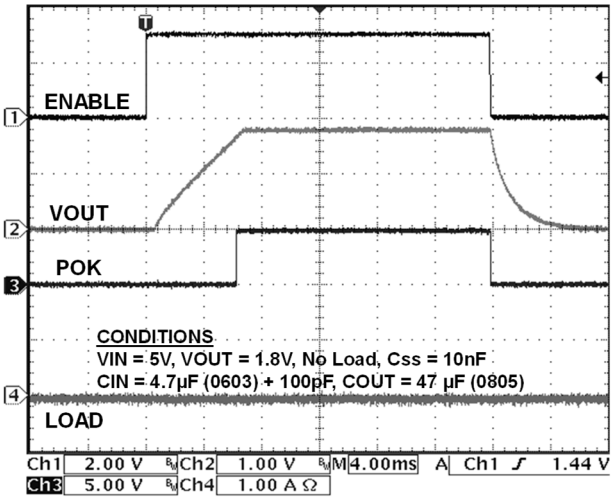
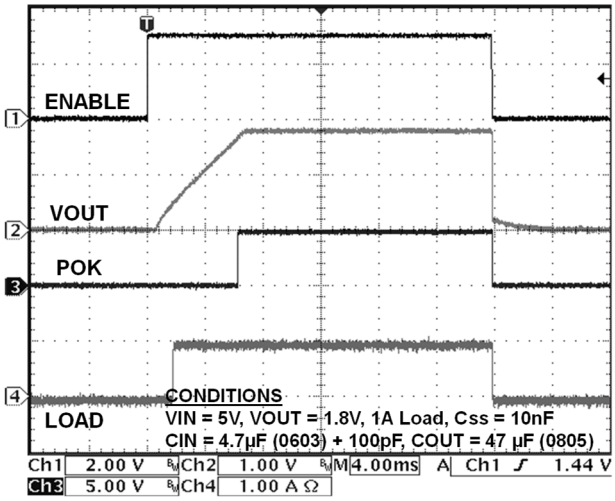


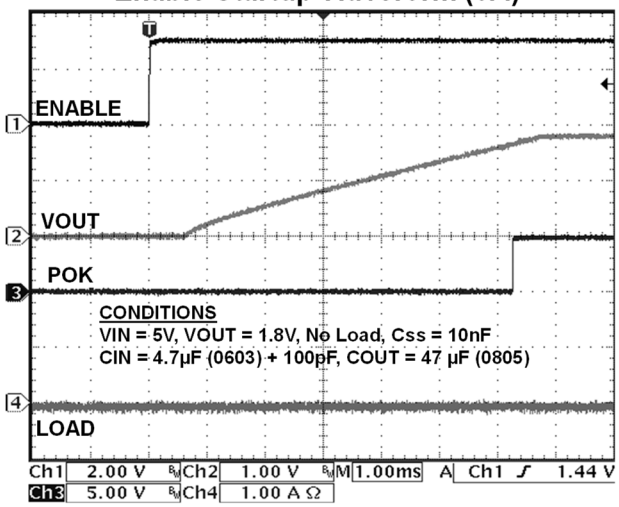
Enable Startup/Shutdown Waveform (0A)



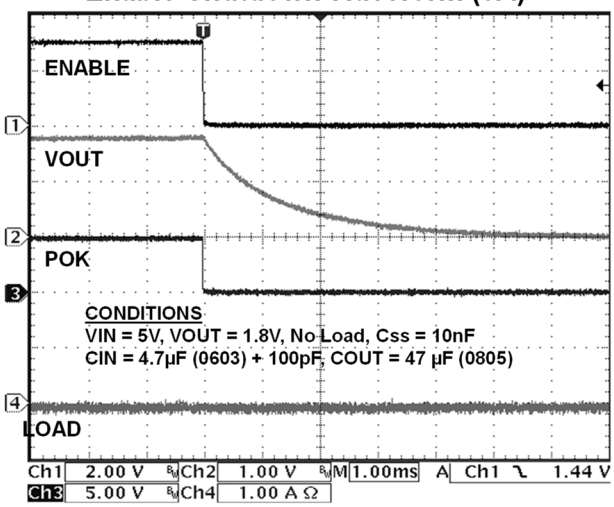
Enable Startup/Shutdown Waveform (1A)



Enable Startup Waveform (0A)



Enable Shutdown Waveform (0A)



FUNCTIONAL BLOCK DIAGRAM

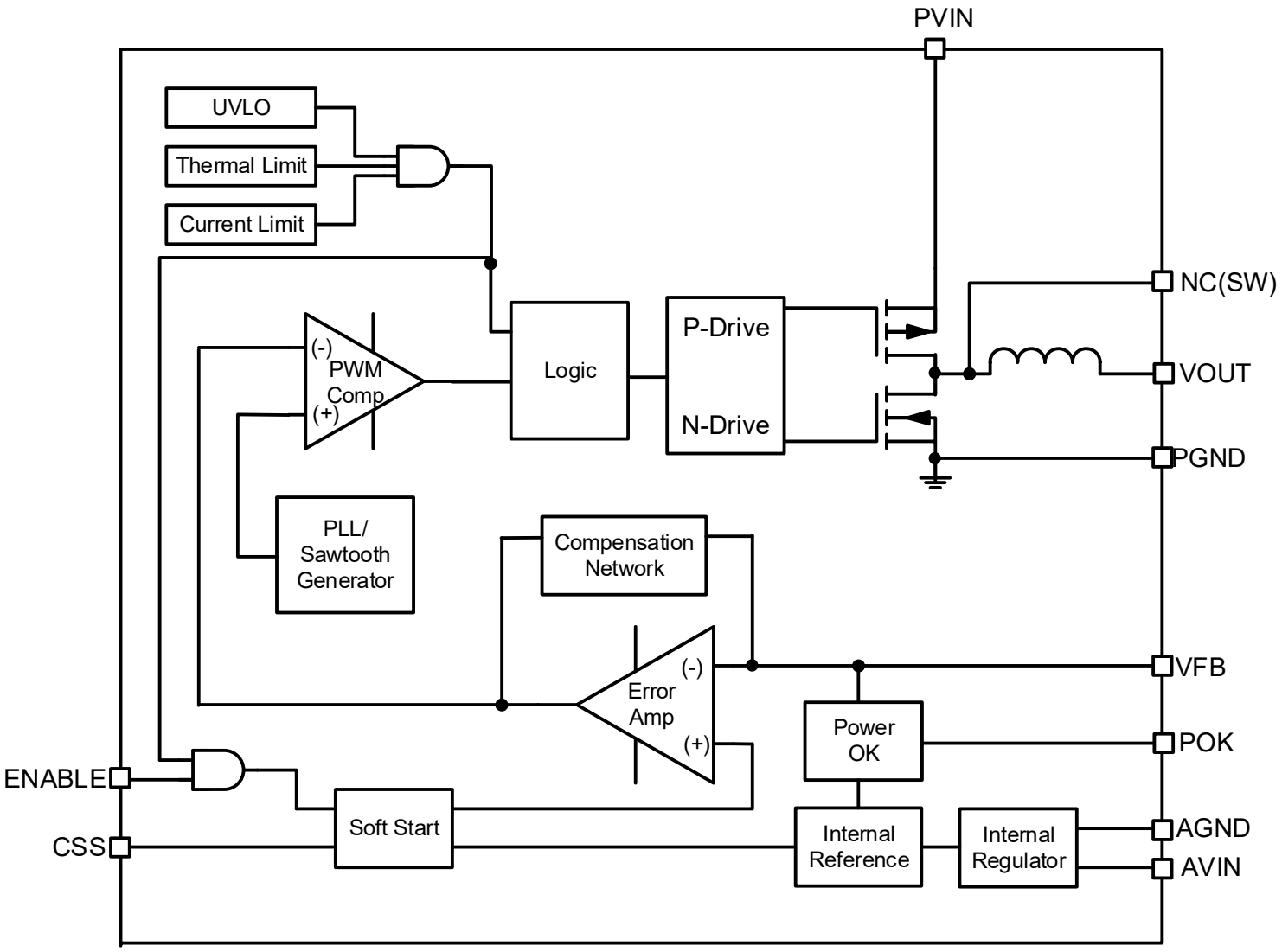


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN6310QI is a synchronous buck converter with integrated MOSFET switches and Inductor. The device can deliver up to 1A of continuous load current. The EN6310QI has a programmable soft start rise time and a power OK (POK) signal. The device operates in a fixed 2.2MHz PWM mode to eliminate noise associated with pulse frequency modulation schemes. The control topology is a low complexity type IV voltage mode providing high noise immunity and stability over the entire operating range. Output voltage is set with a simple resistor divider. The high switching frequency enables the use of small MLCC input and output filter capacitors. Figure 4 shows the EN6310QI block diagram.

Operational Features:

The EN6310QI has the following protection features.

- Over-current protection (to protect the IC from excessive load current)
- Short-Circuit protection
- Thermal shutdown with hysteresis
- Under-voltage lockout circuit to disable the converter output when the input voltage is below a pre-defined level

Protection Features:

- Soft-start circuit, limiting the in-rush current when the converter is initially powered up. The soft start time is programmable with appropriate choice of soft start capacitor value.

High Efficiency Technology

The key enabler of this revolutionary integration is Enpirion's proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seamless integration of all switching, control, and compensation circuitry.

The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Integration for Low-Noise Low-EMI

The EN6310QI utilizes a proprietary low loss integrated inductor. The integration of the inductor greatly simplifies the power supply design process. The inherent shielding and compact construction of the integrated inductor reduces the conducted and radiated noise that can couple into the traces of the printed circuit board. Furthermore, the package layout is optimized to reduce the electrical path length for the high di/dt input AC ripple currents that are a major source of radiated emissions from DC-DC converters. Careful package and IC design minimize common mode noise that can be difficult to mitigate otherwise. The integrated inductor provides the optimal solution to the complexity, output ripple, and noise that plague low power DCDC converter design.

Control Topology

The EN6310QI utilizes an internal type IV voltage mode compensation scheme. Voltage mode control provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance. The EN6310QI is optimized for fast transient recovery for applications with demanding transient performance. Voltage mode control enables a high degree of stability over the entire operating range.

Enable

The EN6310QI ENABLE pin enables and disables operation of the device. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter and initiate a normal soft start operation. When ENABLE is pulled low, the Power MOSFETs stop switching and the output is discharged in a controlled manner with a soft pull down MOSFET. Once the enable pin is pulled low, there is a lockout period before the device can be re-enabled. The lock out period can be found in the Electrical Characteristics Table. Do not leave ENABLE pin floating or it will be in an unknown random state.

The EN6310QI supports startup into a pre-biased output of up to 1.5V. The output of the EN6310QI can be pre-biased with a voltage up to 1.5V when it is first enabled.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. The POK will also be a logic low if the input voltage is in UVLO or if the ENABLE is pulled low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Programmable Soft Start Operation

Soft start is externally programmable by adjusting the value of the C_{SS} capacitor, which is placed between the respective C_{SS} pin and AGND pin. When the enable pin is pulled high, the output will ramp up monotonically at a rate determined by the CSS capacitor.

Soft start ramp time is programmable over a range of 0.5ms to 10ms. The longer ramp times allow startup into very large bulk capacitors that may be present in applications such as wireless broadband or solid state storage, without triggering an Over Current condition. The rise time is given as:

T_{RISE} [ms] = C_{SS} [nF] x 0.65 ± 25%

NOTE: Rise time does not include capacitor tolerances.

If a 10nF soft-start capacitor is used, then the output voltage rise time will be around 6.5ms. The rise time is measured from when $V_{IN} \geq V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value.

Over Current/Short Circuit Protection

The current limit and short-circuit protection is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off and the output is discharged. After 1.6ms the device will be re-enabled and will then go through a normal soft-start cycle. If the over current condition persists, the device will enter a hiccup mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold, the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Thermal Shutdown

When excess power is dissipated in the EN6310QI the junction temperature will rise. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases to a safe operating level, the part will go through the normal startup process. The thermal shutdown temperature and hysteresis values can be found in The electrical characteristics table.

APPLICATION INFORMATION

Output Voltage Setting

The EN6310QI output voltage is programmed using a simple resistor divider network (R_A and R_B). The feedback voltage at VFB is nominally 0.6V. R_A is fixed at 200kΩ and R_B can be calculated based on Figure 5. The values recommended for C_{OUT}, C_A, and R_{CA} make up the external compensation of the EN6310QI. It will vary with each VIN and VOUT combination to optimize on performance. Please see Table 1 for a list of recommended R_A, C_A, R_{CA}, and C_{OUT} values for each solution. Since VFB is a sensitive node, do not touch the VFB node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur.

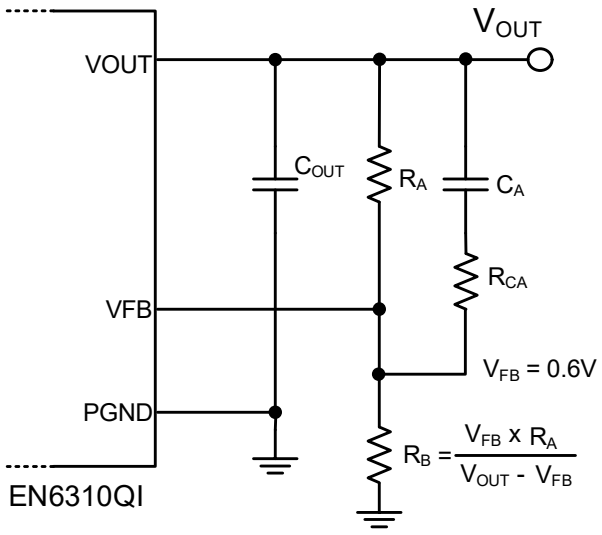


Figure 5: V_{OUT} Resistor Divider & Compensation Capacitor

The output voltage is set by the following formula:

$$VOUT = VREF * \left(1 + \frac{R_A}{R_B}\right)$$

Rearranging to solve for R_B:

$$R_B = R_A * \frac{VREF}{VOUT - VREF}\ k\Omega$$

Where:

R_A = 200kΩ, VREF = 0.60V

Then R_B is given as:

$$R_B = \frac{120}{VOUT - 0.6}\ k\Omega$$

R_A is chosen as 200kΩ to provide constant loop gain. The output voltage can be programmed over the range of 0.6V to 3.3V.

Table 1: Compensation values. For output voltages in between, use the values from the higher output voltage

CIN = 4.7µF/0603 + 100pF					
CAVIN = 20Ω + 0.47µF					
COUT = 47µF/0805 or 2x22µF/0603					
R_A = 200kΩ, R_{CA} = 1kΩ, $R_B = 0.6R_A/(V_{OUT} - 0.6)$					
V_{IN}	V_{OUT}	C_A	V_{IN}	V_{OUT}	C_A
5.5V	3.3V	15pF	5.5V	1.2V	27pF
5.0V			5.0V		
4.5V			4.5V		33pF
5.5V	2.5V	15pF	3.3V		
5.0V			2.7V		39pF
4.5V			5.5V	1.0V	39pF
3.3V			5.0V		
5.5V	1.8V	15pF	4.5V		
5.0V			3.3V		47pF
4.5V			2.7V		
3.3V		22pF	5.5V	0.6V	39pF
2.7V			5.0V		
5.5V	1.5V	22pF	4.5V		47F
5.0V			3.3V		56pF
4.5V			2.7V		
3.3V		27pF			
2.7V		33pF			

Input Filter Capacitor

The EN6310QI requires at least a 4.7µF/0603 and a 100pF input capacitor near the PVIN pins. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Table 2 contains a list of recommended input capacitors.

Table 2: Recommended Input Capacitors

DESCRIPTION	MFG	P/N
4.7µF, 10V, X5R, 10%, 0603	Murata	GRM185R61A475KE11#
4.7µF, 10V, X5R, 10%, 0603	Taiyo Yuden	LMK107BJ475KA-T

Output Capacitor Selection

The EN6310QI requires at least a 47µF/0805 or two 22µF/0603 output filter capacitors. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Table 3 contains a list of recommended output capacitors.

Table 3: Recommended Output Capacitors

DESCRIPTION	MFG	P/N
47µF, 6.3V, X5R, 20%, 0805	Murata	GRM21BR60J476ME15#
47µF, 6.3V, X5R, 20%, 0805	Taiyo Yuden	JMK212BBJ476MG-T
22µF, 10V, X5R, 20%, 0603	Murata	GRM188R60J226MEA0#
22µF, 10V, X5R, 20%, 0603	Taiyo Yuden	JMK107BBJ226MA-T

THERMAL CONSIDERATIONS

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EN6310QI DC-DC converter is packaged in a 4x5x1.85mm 30-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 140°C.

The following example and calculations illustrate the thermal performance of the EN6310QI.

Example:

V_{IN} = 5V

V_{OUT} = 3.3V

I_{OUT} = 1A

First calculate the output power.

P_{OUT} = 3.3V x 1A = 3.3W

Next, determine the input power based on the efficiency (η) shown in Figure 6.

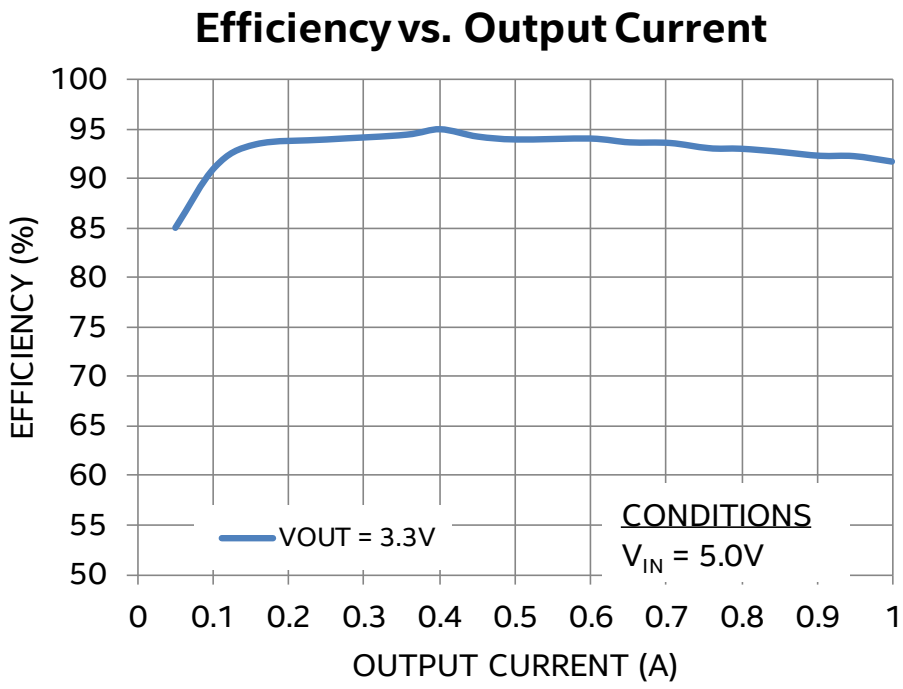


Figure 6: Efficiency vs. Output Current

For V_{IN} = 5V, V_{OUT} = 3.3V at 1A, η ≈ 91%

η = P_{OUT} / P_{IN} = 91% = 0.91

P_{IN} = P_{OUT} / η

P_{IN} ≈ 3.3W / 0.91 ≈ 3.63W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 3.63W – 3.3W ≈ 0.33W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN6310QI has a θ_{JA} value of 60 °C/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 0.33W x 60°C/W ≈ 19.8°C ≈ 20°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 20°C ≈ 45°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 20°C ≈ 105°C

The maximum ambient temperature the device can reach is 105°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION CIRCUITS

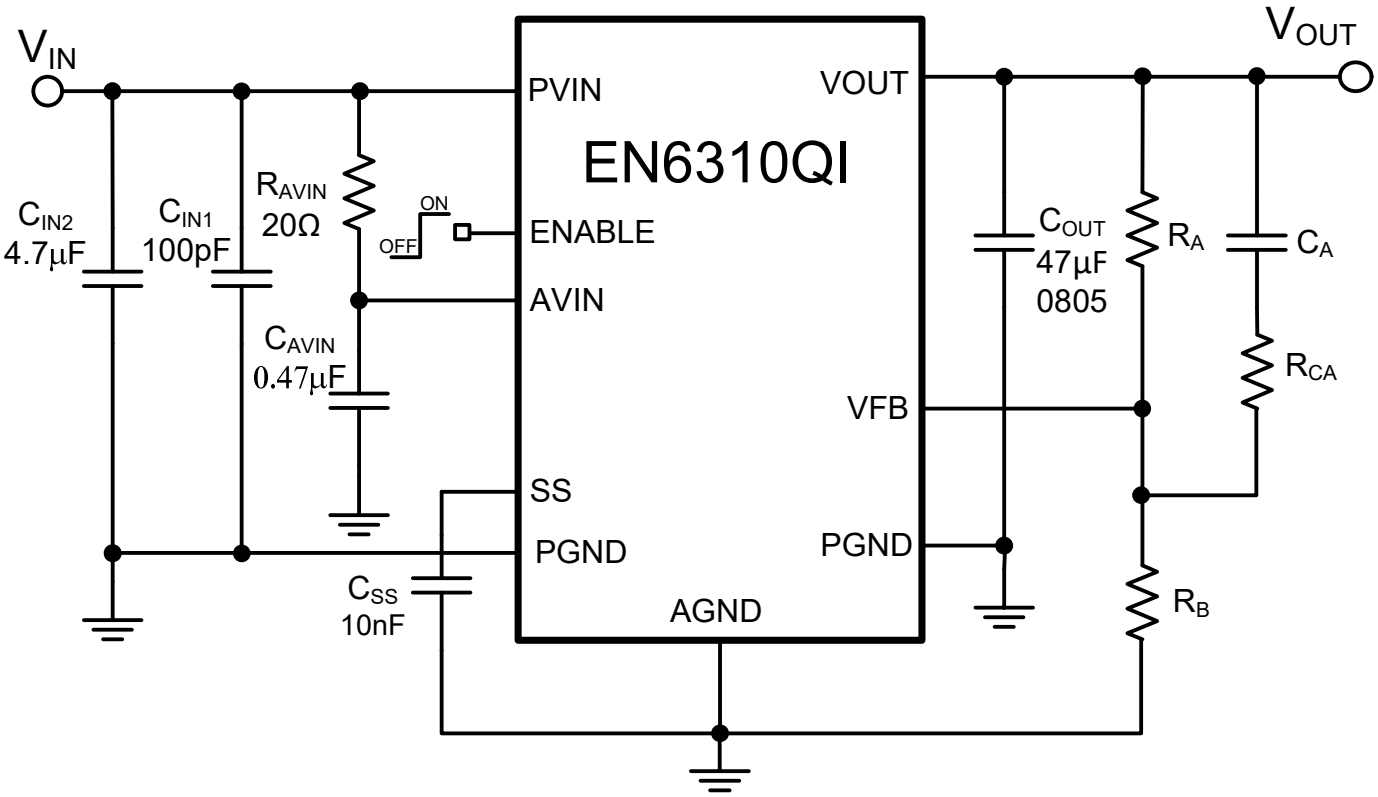


Figure 7: Typical Engineering Schematic

LAYOUT RECOMMENDATIONS

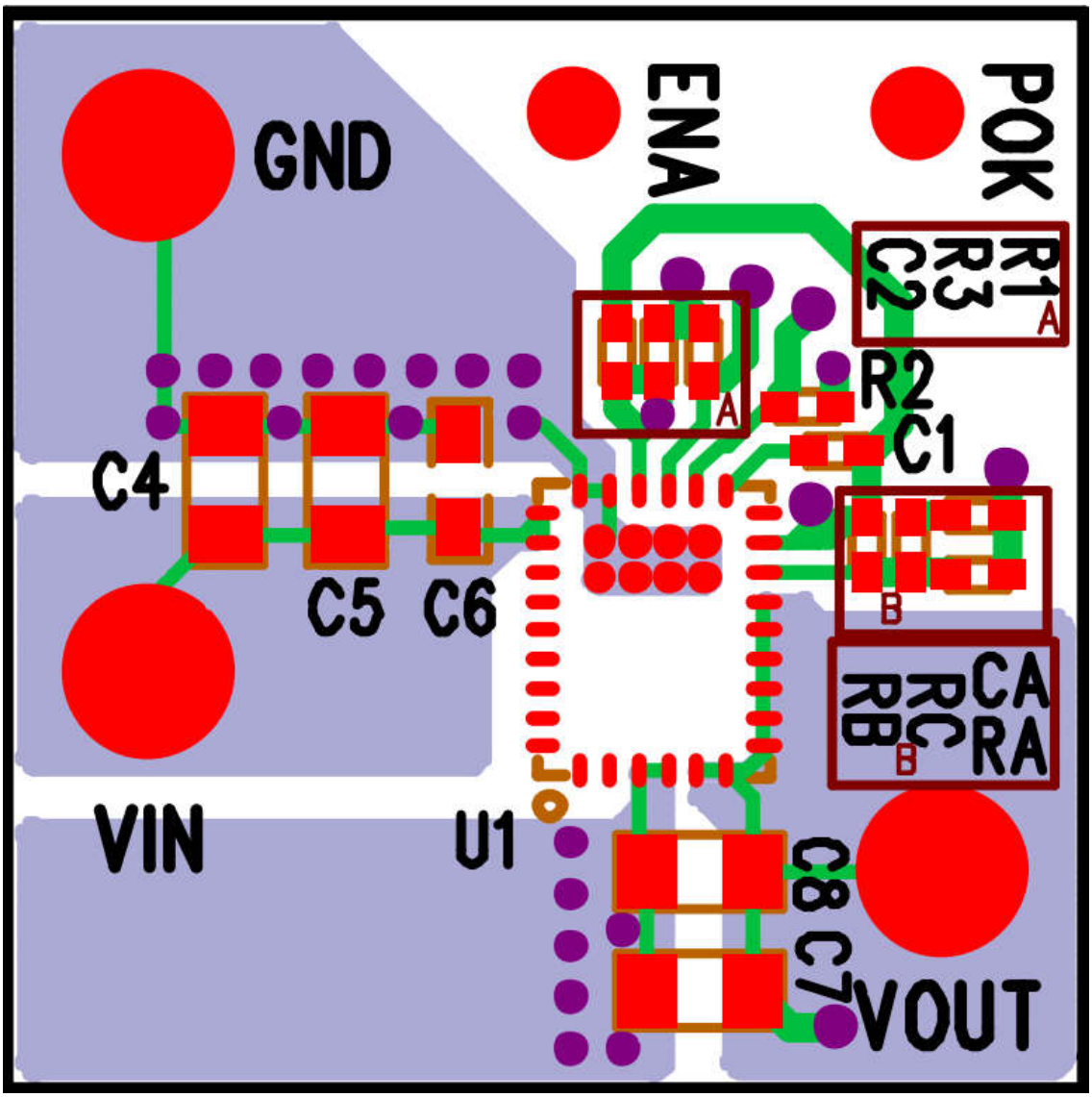


Figure 8: Drop-In Board Layout Recommendations

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN6310QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Voltage and GND traces between the capacitors and the EN6310QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on EN6310QI's product page at www.altera.com/enpirion.

Recommendation 3: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. See Figure 8.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 3 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 8. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane. AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. A good location is to place the AVIN connection on the source side of the input capacitor, away from the PVIN pins.

Recommendation 6: The layer 1 metal under the device must not be more than shown in Figure 8. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 7: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 8: Keep R_A, C_A, and R_B close to the VFB pin (see Figures 6 and 7). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

RECOMMENDED PCB FOOTPRINT

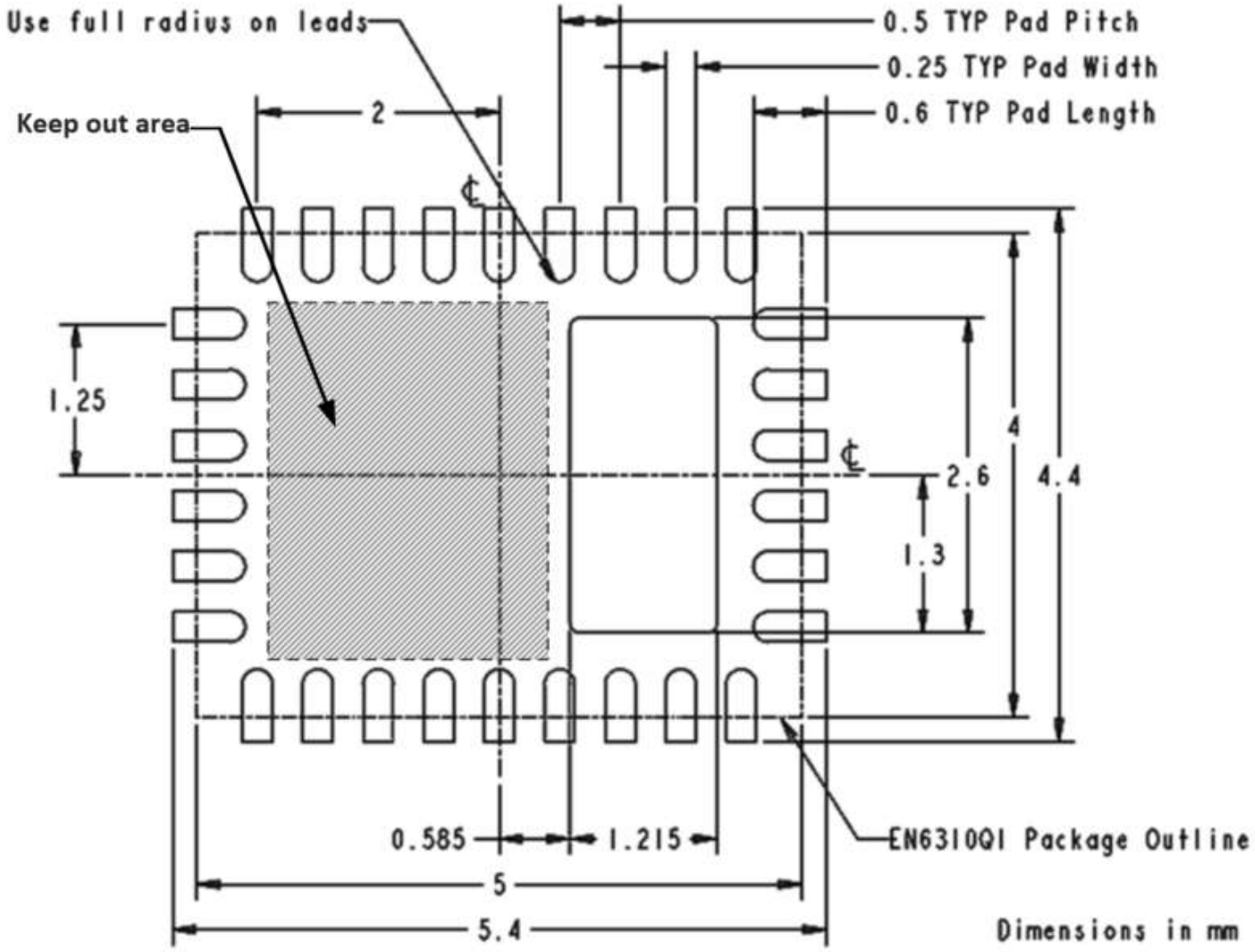


Figure 9: EN6310QI PCB Footprint (Top View)

Note: Don't use the layer underneath the device keep out area as it contains the exposed metal below the package that is not to be mechanically or electrically connected to the PCB.

PACKAGE AND MECHANICAL

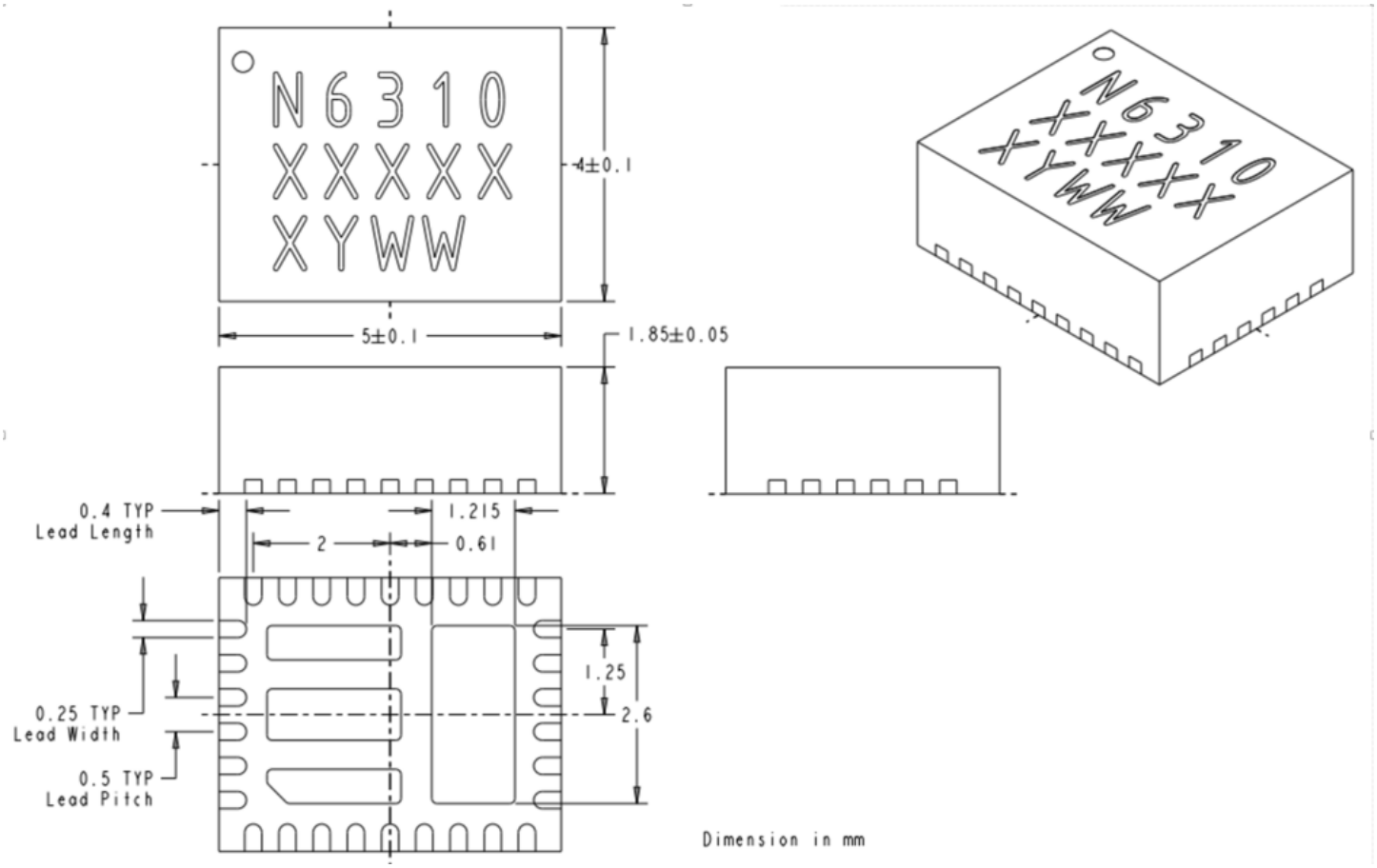


Figure 10: EN6310QI Package Dimensions

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
A	March 2014	Introductory production datasheet.
B	March 2015	Pin 12 changed to VOUT instead of NC.
C	June 2015	Updated the pre-bias section adding the capability of pre-biasing to voltage up to 1.5V.
D	Feb 2016	Changed Feedback Pin Voltage Initial Accuracy on Electrical Characteristics Table. Corrected thermal hysteresis value in thermal shutdown section. Added section on "Design considerations for lead-frame based modules" i.e. keepout area. Modified PCB Footprint and package drawings. Formatting changes.
E	June 2016	Added EMI scan data. Clarified location of Gerber files in layout recommendation section.
F	Feb 2017	Updating the device package drawings with the keep-out area drawing. Drawing the Keep-out Pins in figure 3.
G	April 2018	Changed datasheet into Intel format.

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.altera.com/enpirion

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