ER6230QI 3A Buck Regulator

Step-Down DC-DC Switching Converter with Integrated MOSFET

DESCRIPTION

The ER6230QI is an Intel® Enpirion® DC-DC step-down buck converter. It integrates MOSFET switches, small-signal circuits and compensation in an advanced 4mm x 4mm x 0.85mm 24-pin QFN package.

The ER6230QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architectures. The device's advanced circuit techniques and high switching frequency deliver high-quality, ultra compact, non-isolated DC-DC conversion.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- High Efficiency (Up to 95%)
- Up to 3A Continuous Operating Current
- 2.7V to 6.6V Input Voltage Range
- Programmable Light Load Mode (LLM)
- Total Solution Size (85mm^2)
- 1% V_{FB} Initial Accuracy
- 2% V_{OUT} Accuracy (Line, Load, Temp)
- 1.9MHz Switching Frequency
- Frequency Synchronization with External Clock
- Programmable Soft-Start
- Power OK Indicator
- Thermal, Over-Current, Short Circuit, Under-Voltage
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- Point of Load Regulation for FPGAs, Distributed Power Architectures, Low-Power ASICs, Multi-Core, Communication Processors and DSPs
- Applications Needing High Power Density
- 5V/3.3V Bus Architectures Needing High Efficiency

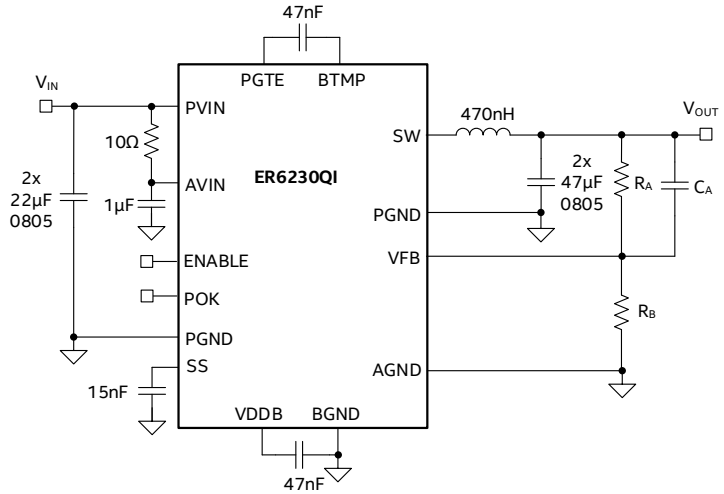


Figure 1: Simplified Applications Circuit

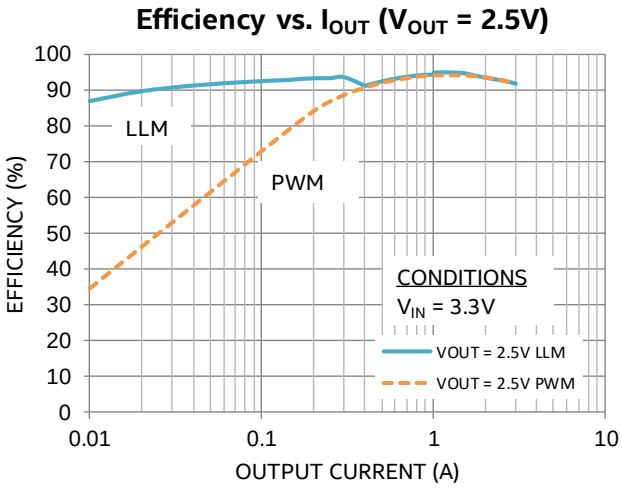


Figure 2: Efficiency at V_{IN} = 3.3V

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
ER6230QI	ER6230QI	-40°C to +125°C	24-pin (4mm x 4mm x 0.85mm) QFN
EVB-ER6230QI	ER6230QI	QFN Evaluation Board	

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

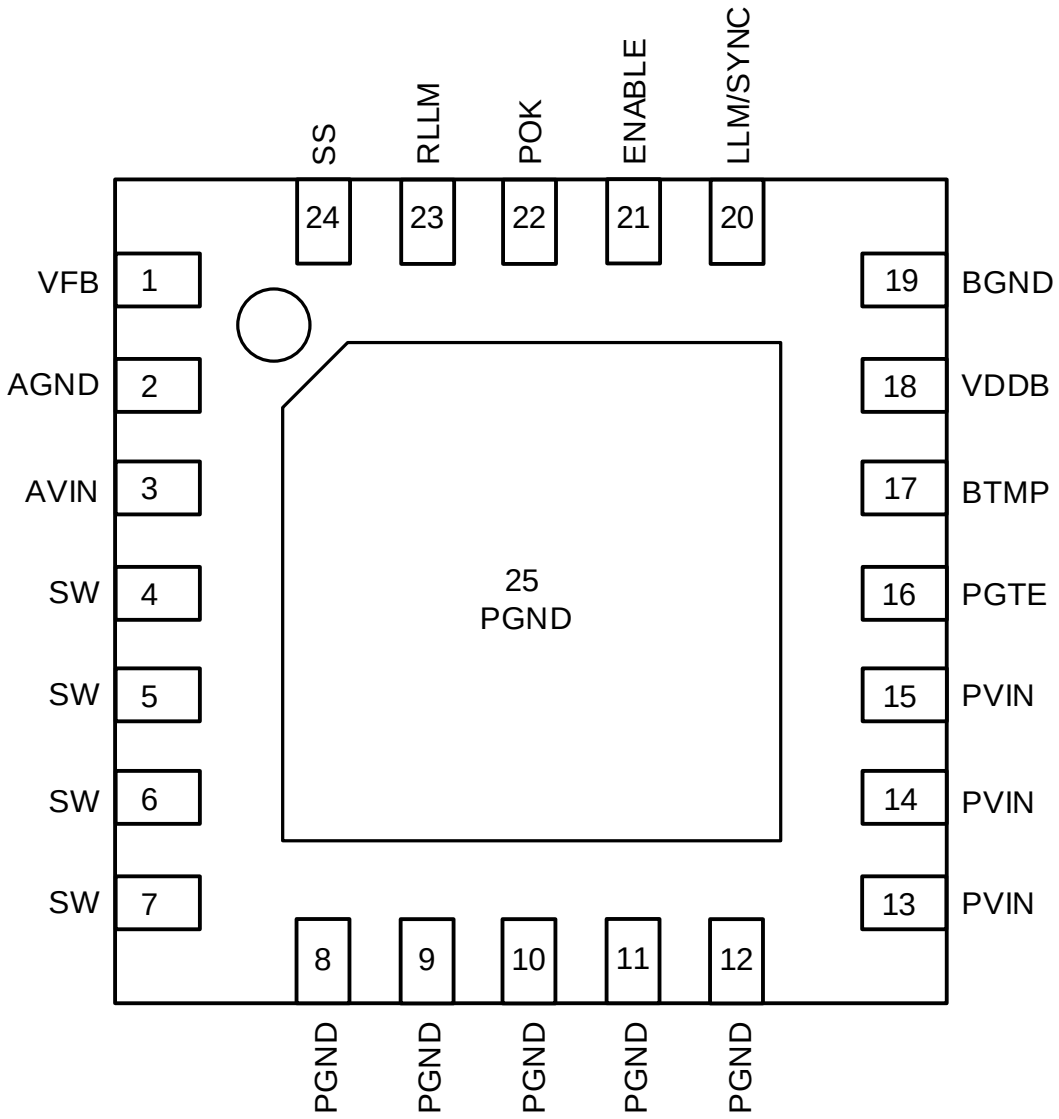


Figure 3: Pin Diagram (Top View)

NOTE A: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1	VFB	Analog	External feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) is required in parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage being equal to 0.75V.
2	AGND	Ground	Ground for internal control circuits. Connect to the power ground plane with a via right next to the pin.
3	AVIN	Power	Input power supply for the controller. Connect to input voltage at a quiet point and decoupling with a 1µF capacitor. Refer to the Layout Recommendation section.
4-7	SW	Output	Switching Node. These pins are internally connected to the common switching node of the internal MOSFETs.
8-12	PGND	Ground	Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors.
13, 14, 15	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pin. Refer to the Layout Recommendation section.
16	PGTE	Analog	PMOS Gate. Connect a 47nF capacitor from PGTE to BTMP. A 560Ω from PVIN to PGTE may be used to assist in filtering the input rail in noisy systems.
17	BTMP	Analog	Bottom Plate connection for internal PGTE. See PGTE description.
18	VDDB	Power	Internal regulated voltage used for the internal control circuitry. Connect a 47nF capacitor from VDDB to BGND.
19	BGND	Ground	Internal LDO Ground. See VDDB description. Connect BGND to PGND.
20	LLM/SYNC	Digital	Dual function pin providing LLM Enable and External Clock Synchronization (see Application Section). At static Logic HIGH, device will allow automatic engagement of light load mode. At static logic LOW, the device is forced into PWM only. A clocked input to this pin will synchronize the internal switching frequency to the external signal. Do not leave this pin floating.
21	ENABLE	Digital	Input Enable. Applying logic high on the ENABLE pin will enable the device and initiate a soft-start. Applying logic low disables the output and switching stops. ENABLE is internally pulled low by a non-passive resistance equivalent to 250kΩ.

PIN	NAME	TYPE	FUNCTION
22	POK	Digital	Power OK is an open drain transistor used for power system state indication. POK is logic high when V_{OUT} is within ±10% of V_{OUT} nominal.
23	RLLM	Analog	Programmable LLM engage resistor. Connect a resistor from RLLM to AGND for adjustment of load current at which Light-Load Mode engages. RLLM can be left open for PWM only operation.
24	SS	Analog	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval. Refer to Soft-Start Operation in the Functional Description section for more details.
25	PGND	Ground	Power ground thermal pad. Not a perimeter pin. Connect thermal pad to the system GND plane for heat-sinking purposes. Refer to the Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	7.0	V
ENABLE, POK		-0.3	V_{IN}+0.3	V
VFB, SS, PGTE, VDDB,		-0.3	2.5	V
SW Voltage DC	V_{SW}		7.0	V
SW Voltage Peak < 5ns	V_{SW_PEAK}	-2.0	10.5	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V

PARAMETER	CONDITION	MIN	MAX	UNITS
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.7	6.6	V
Output Voltage Range	V_{OUT}	0.75	$V_{IN} - V_{DO}$ (1)	V
Output Current Range	I_{OUT}		3	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	25	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	30	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	3	°C/W

(1) V_{DO} (dropout voltage) is defined as (I_{LOAD} x Droput Resistance). Please refer to Electrical Characteristics Table.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = PVIN = AVIN = 5.0V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	PVIN = AVIN	2.7		6.6	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted	2	2.3	2.45	V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted	1.7	2.1	2.3	V
Under Voltage Lock-Out Hysteresis	V_{UVLO_HYS}			200		mV
Shut-Down Supply Current	I_S	ENABLE = 0V		40	60	µA
AVIN Quiescent Current	I_{AVINQ}	LLM/SYNC = High V_{OUT} = 0.75V		650	900	µA
No Load Quiescent Current	I_{VINQ}	PVIN and AVIN V_{OUT} = 1.2V		40		mA
Feedback Pin Voltage [3]	V_{FB}	V_{OUT} = 0.75V I_{LOAD} = 0, T_A =25°C	0.7425	0.75	0.7575	V
Feedback Pin Voltage (Load, Temp.)	V_{FB}	0A ≤ I_{LOAD} ≤ 3A -40°C ≤ T_A ≤ 85°C	0.739	0.75	0.761	V
Feedback Pin Voltage (Line, Load, Temp.)	V_{FB}	2.7V ≤ V_{IN} ≤ 6.6V 0A ≤ I_{LOAD} ≤ 3A -40°C ≤ T_A ≤ 85°C	0.735	0.75	0.765	V
Feedback pin Input Leakage Current [4]	I_{FB}	VFB pin input leakage current	-10		10	nA
V_{OUT} Rise Time Range [4]	t_{RISE}	Capacitor programmable	0.8		8	ms
Soft Start Capacitance Range [4]	C_{SS_RANGE}	Recommended C_{SS} range	10		100	nF
Soft-Start Charging Current	I_{SS}		3.5	10	15	µA
Drop-Out Resistance [4]	R_{DO}	Input to output resistance; L = 470nH 25mΩ DCR		60	90	mΩ

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PMOS On-Resistance	R_{DSON_P}			35	50	mΩ
Continuous Output Current	I_{OUT}		0		3	A
Over Current Trip Level	I_{OCP}	V_{IN} = 5V, V_{OUT} = 1.2V	4	6.5		A
Disable Threshold	$V_{DISABLE}$	ENABLE pin logic going low	1.2	1.34	1.48	V
Enable Threshold	V_{EN}	ENABLE pin logic going high	1.22	1.36	1.5	V
ENABLE Pin Input Current	I_{EN}	V_{EN} = 5V; ENABLE pin has ~250kΩ pull down		20	35	µA
ENABLE Pull-Down Resistance	R_{EN_DOWN}	V_{EN} = 5V; Not a passive resistance		250		kΩ
Switching Frequency	F_{SW}	Free running clock frequency	1.5	1.9	2.4	MHz
SYNC Input Threshold – Low	V_{SYNC_LO}	SYNC Clock Logic Level			0.8	V
SYNC Input Threshold – High (5)	V_{SYNC_HI}	SYNC Clock Logic Level	1.8		2.5	V
POK High Threshold	$POK_{\_HI}$	Percentage of V_{OUT} nominal when POK is asserted high		90		%
POK Low Voltage	V_{POKL}	4mA sink into POK			0.4	V
POK High Voltage	V_{POKH}	2.7V ≤ V_{IN} ≤ 6.6V			V_{IN}	V
POK Pin Leakage Current (4)	I_{POKH}	POK is high			1	µA
LLM Headroom (4)		Minimum VIN - VOUT		800		mV
LLM Logic Low (LLM/SYNC PIN)	V_{LLM_LO}	LLM Static Logic Level			0.3	V
LLM Logic High (LLM/SYNC PIN)	V_{LLM_HI}	LLM Static Logic Level	1.5			V
LLM/SYNC Pin Current		LLM/SYNC Pin is <2.5V		<100		nA

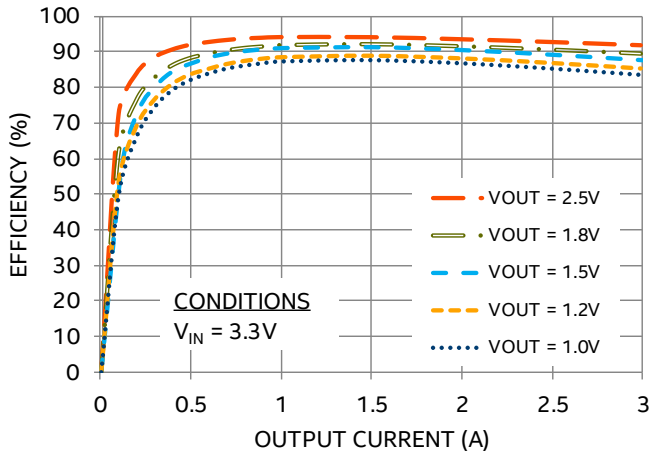
(3) The VFB pin is a sensitive node. Do not touch VFB while the device is in regulation.

(4) Parameter not production tested but is guaranteed by design.

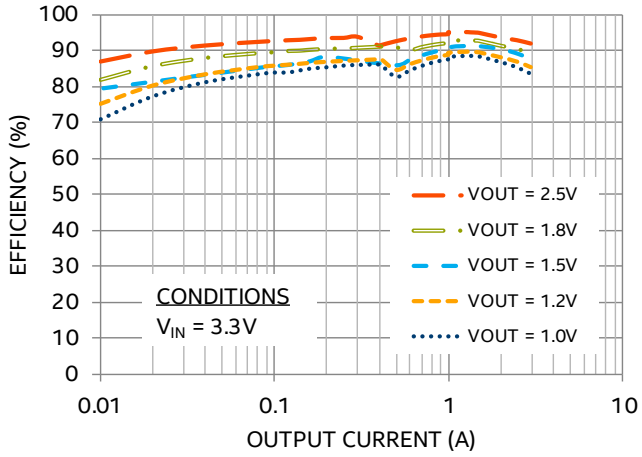
(5) High logic for frequency synchronization with LLM/SYNC pin must be below 2.5V.

TYPICAL PERFORMANCE CURVES

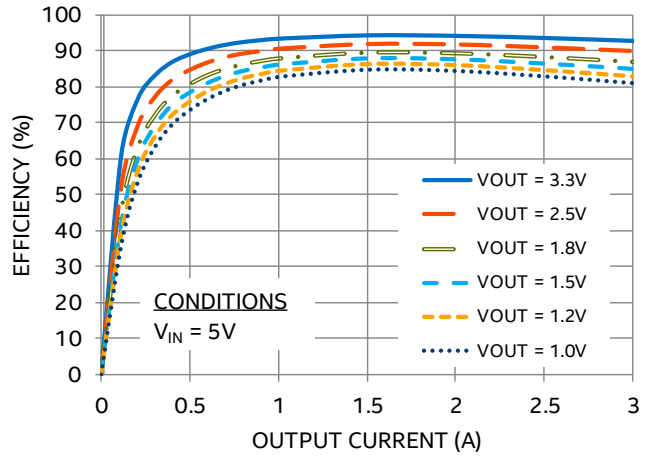
PWM Efficiency vs. I_{OUT} (V_{IN} = 3.3V)



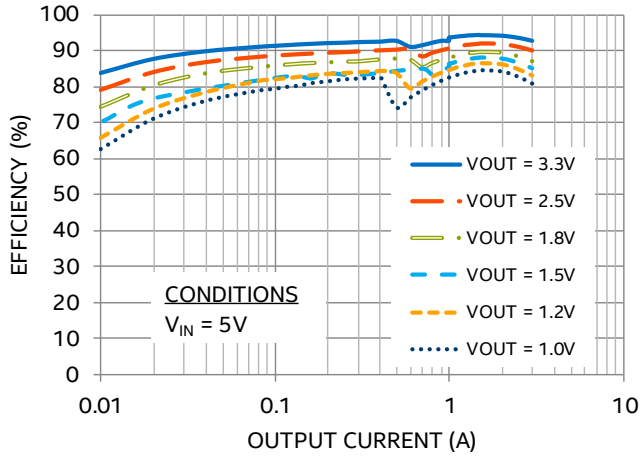
LLM Efficiency vs. I_{OUT} (V_{IN} = 3.3V)



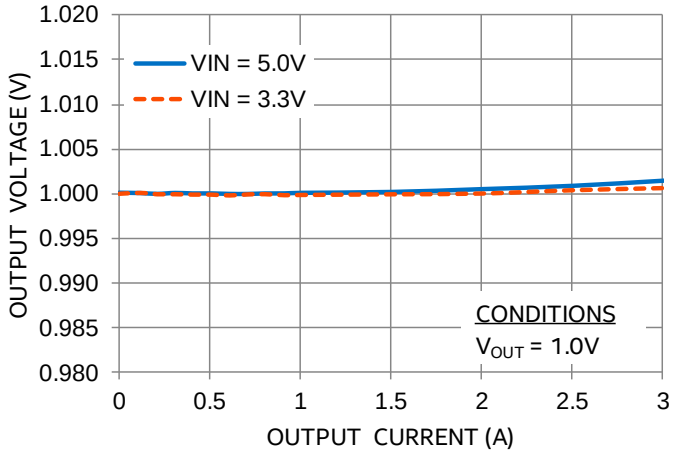
PWM Efficiency vs. I_{OUT} (V_{IN} = 5.0V)



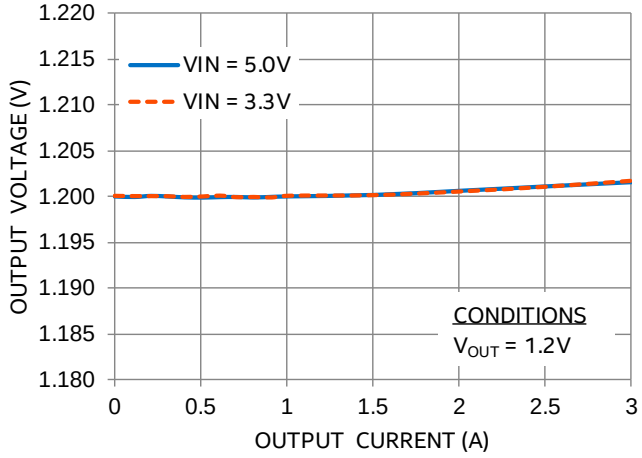
LLM Efficiency vs. I_{OUT} (V_{IN} = 5.0V)



Output Voltage vs. Output Current

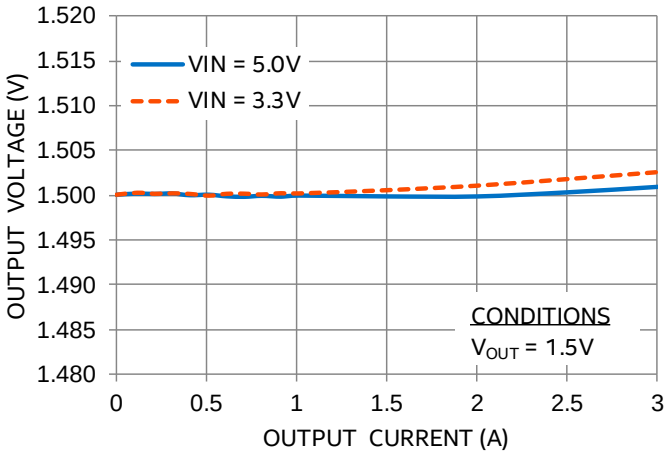


Output Voltage vs. Output Current

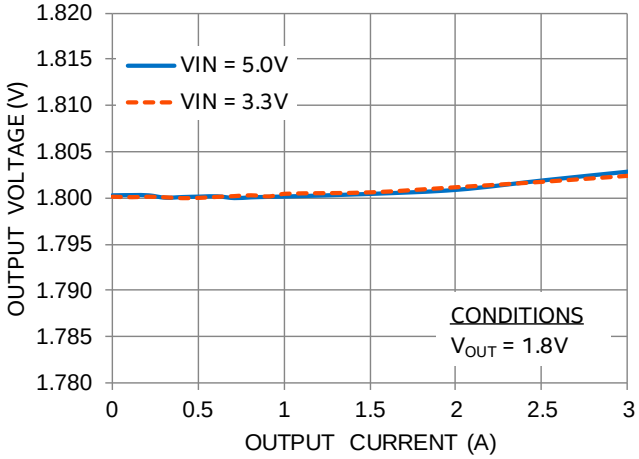


TYPICAL PERFORMANCE CURVES (CONTINUED)

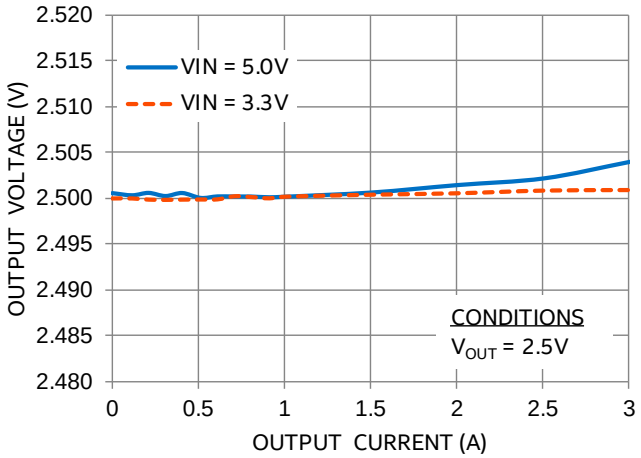
Output Voltage vs. Output Current



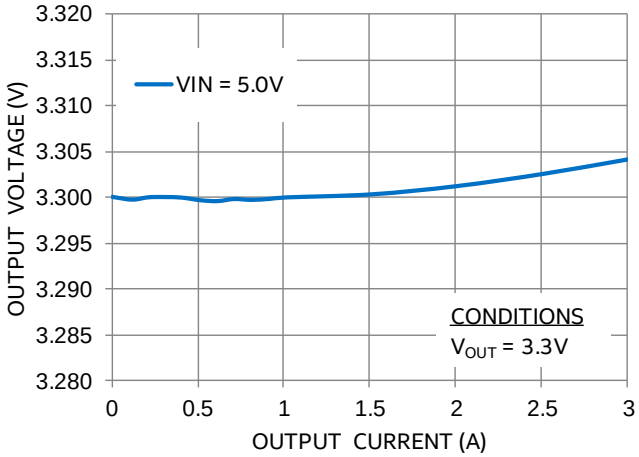
Output Voltage vs. Output Current



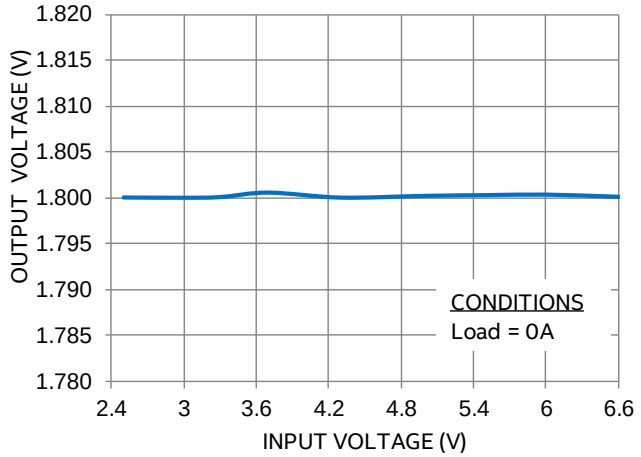
Output Voltage vs. Output Current



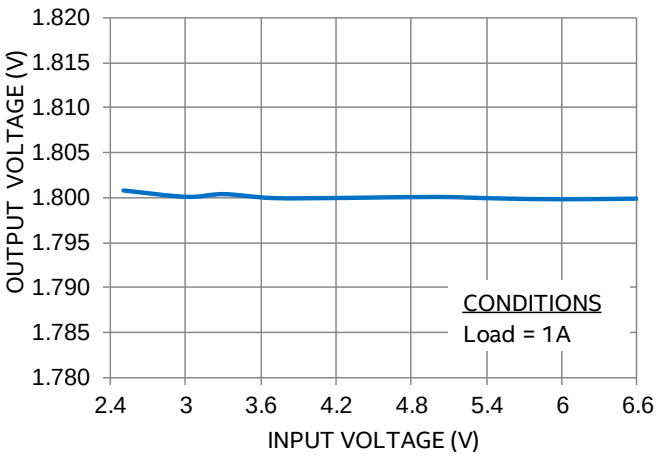
Output Voltage vs. Output Current



Output Voltage vs. Input Voltage

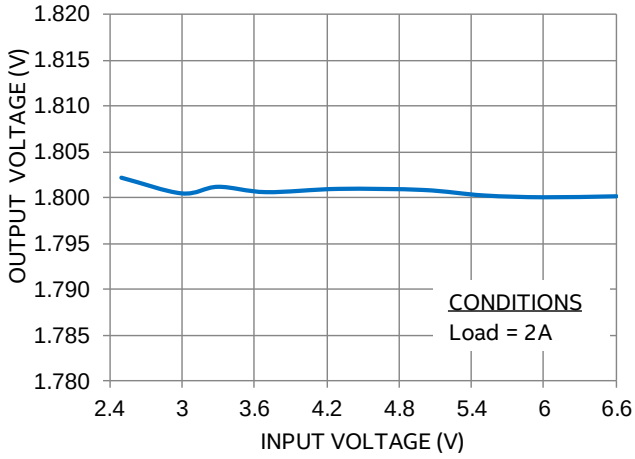


Output Voltage vs. Input Voltage

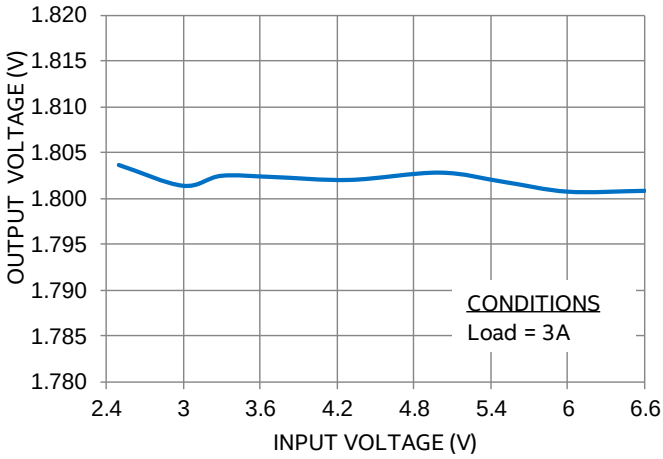


TYPICAL PERFORMANCE CURVES (CONTINUED)

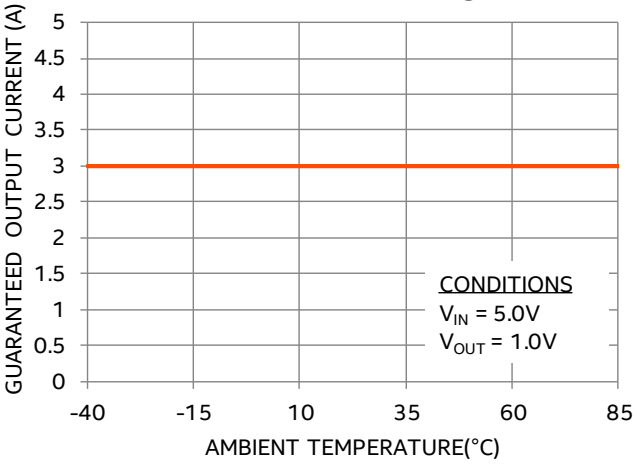
Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage



No Thermal Derating



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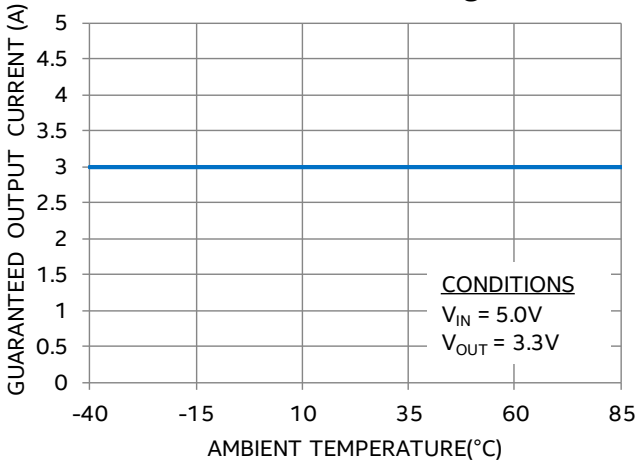
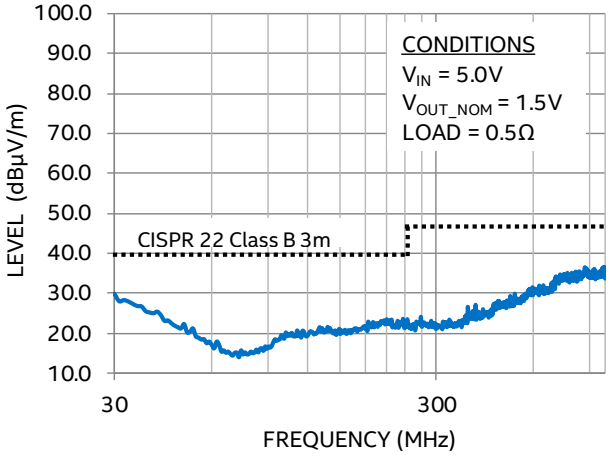
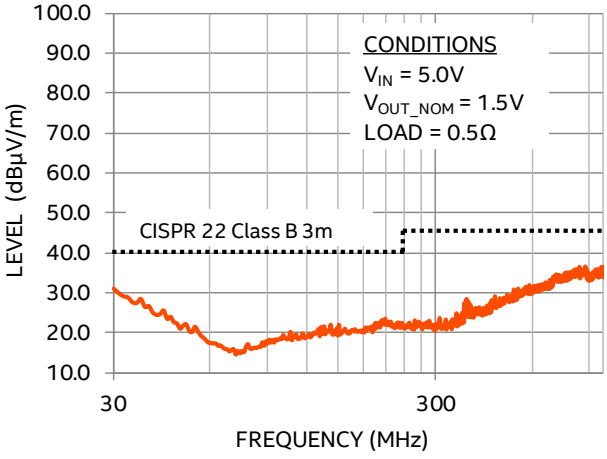


EMI Performance (Horizontal Scan)

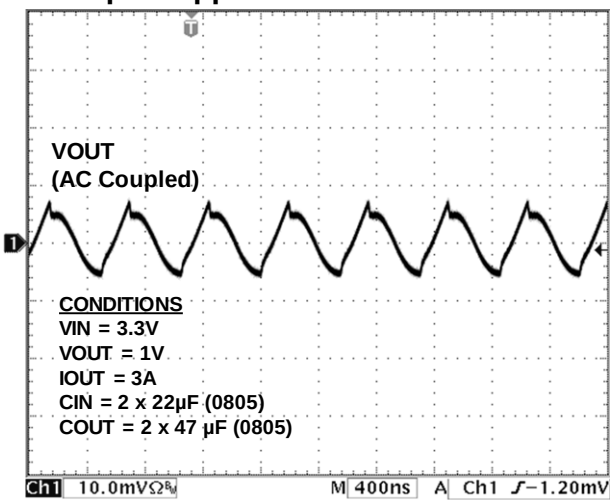


EMI Performance (Vertical Scan)

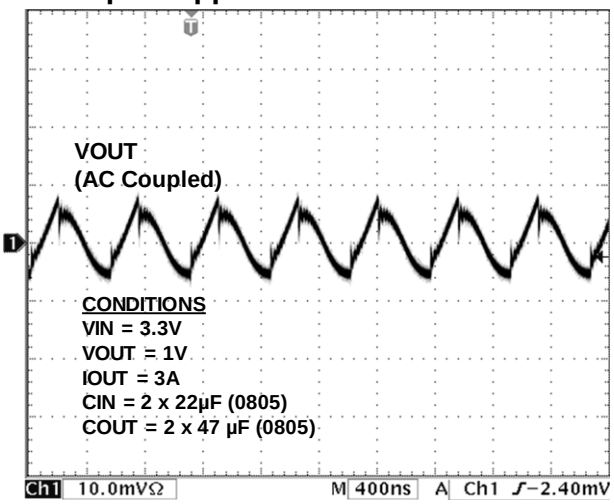


TYPICAL PERFORMANCE CHARACTERISTICS

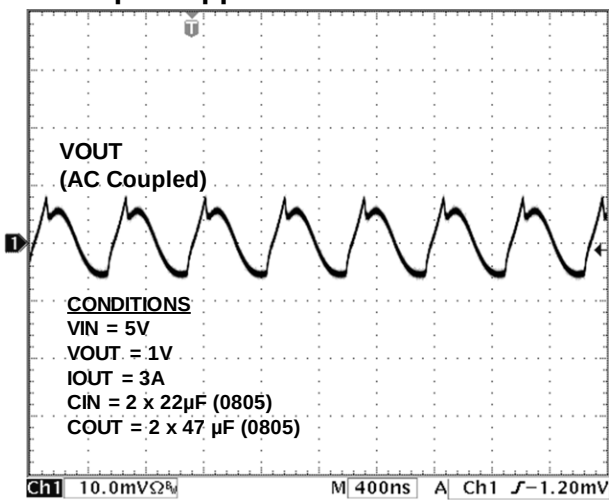
Output Ripple at 20MHz Bandwidth



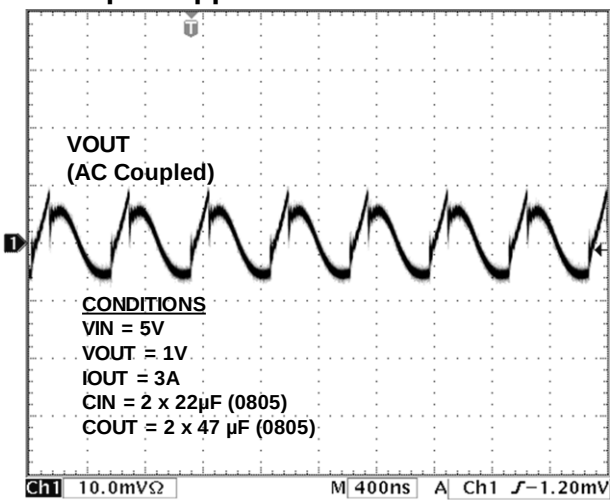
Output Ripple at 500MHz Bandwidth



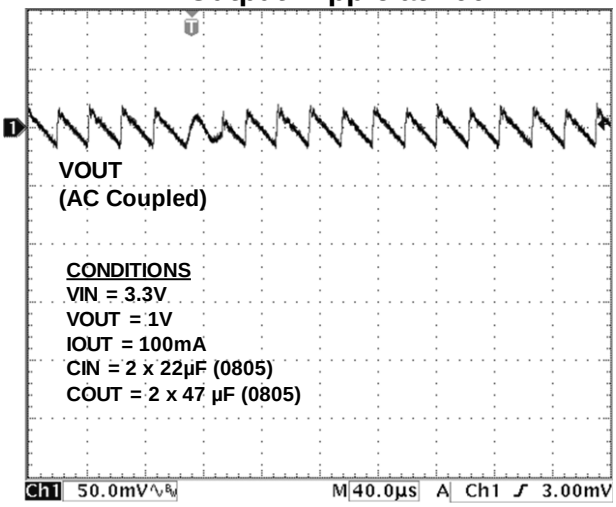
Output Ripple at 20MHz Bandwidth



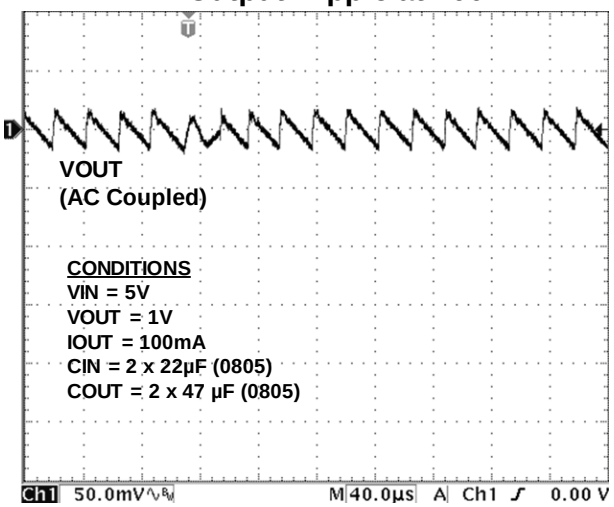
Output Ripple at 500MHz Bandwidth



LLM Output Ripple at 100mA

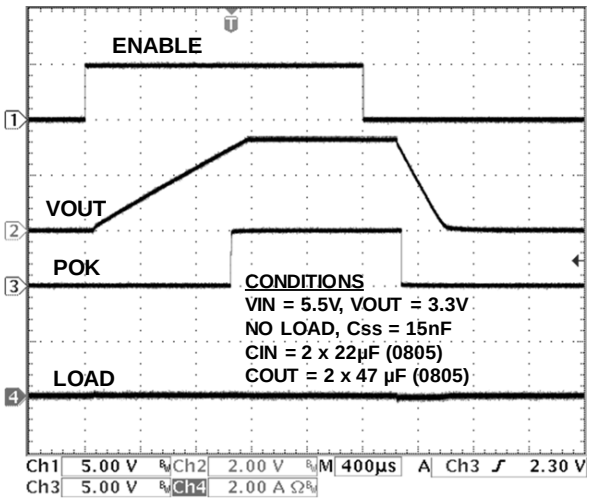


LLM Output Ripple at 100mA

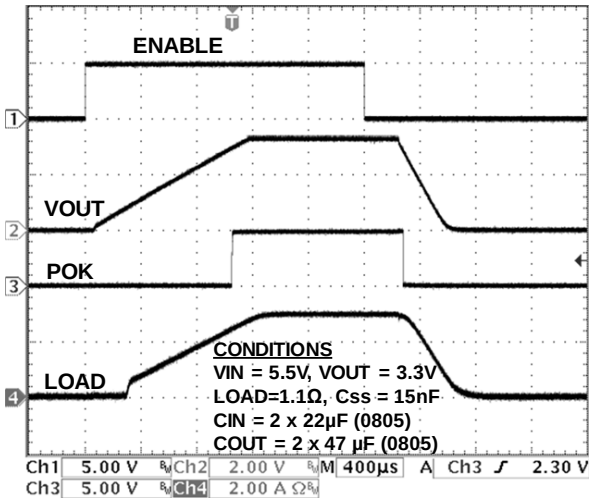


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

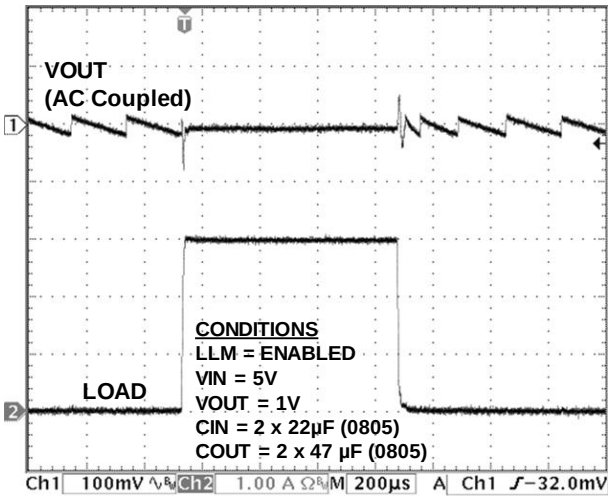
Enable Power Up/Down



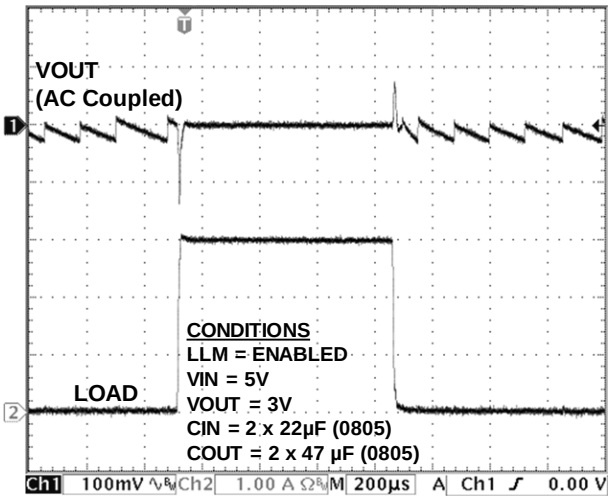
Enable Power Up/Down



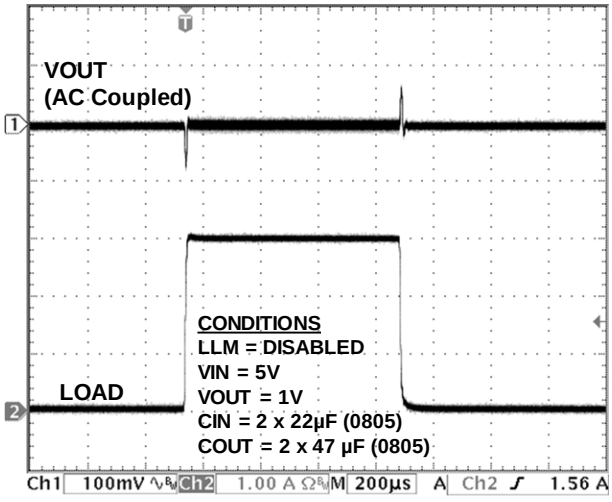
LLM Load Transient from 0.01 to 3A



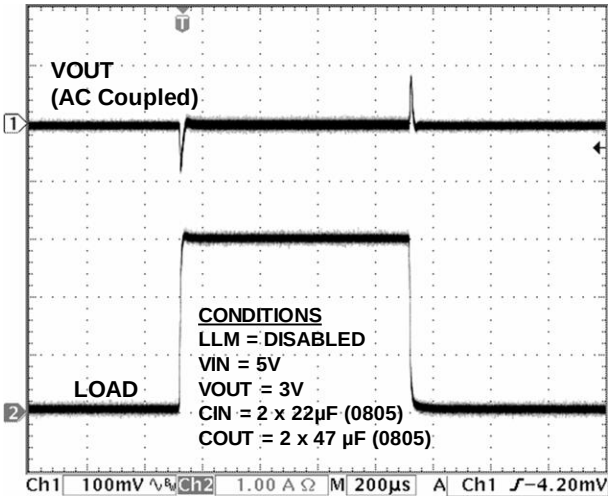
LLM Load Transient from 0.01 to 3A



PWM Load Transient from 0 to 3A



PWM Load Transient from 0 to 3A



FUNCTIONAL BLOCK DIAGRAM

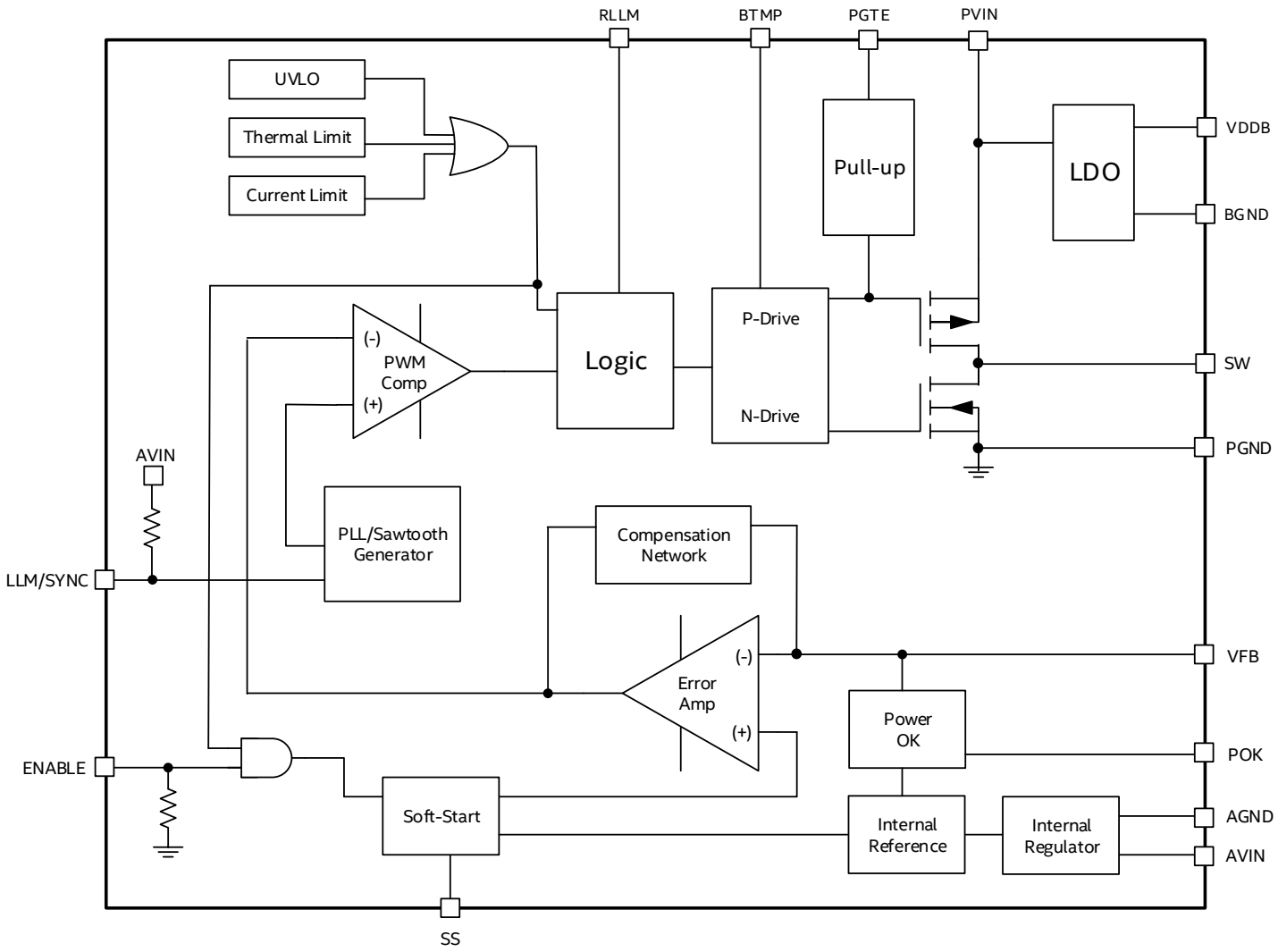


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The ER6230QI is a synchronous DC-DC buck regulator with integrated internal MOSFETs. The nominal input voltage range is 2.7V to 6.6V. The output voltage is programmed using an external resistor divider network. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is internal to the device, but a phase-lead capacitor and resistor are required to complete the compensation network. The type III voltage mode architecture with integrated compensation maximizes loop bandwidth without increasing complexity. This architecture is designed to maintain stability with excellent gain and phase margin and improve transient response. The enhanced voltage mode architecture also provides high noise immunity at light load and maintains excellent line and load regulation. Up to 3A of continuous output current

can be drawn from this converter. The 1.9MHz switching frequency allows the use of smaller case size input and output capacitors within a small footprint.

The ER6230QI architecture includes the following features.

Operational Features:

- Automatic Light Load Mode (LLM) or Forced PWM mode selection
- Soft-start circuit allowing controlled startup and shutdown
- Power OK circuit indicating the output voltage is greater than 90% of programmed value

Protection Features:

- Over-current protection from short circuit or excessive load current
- Thermal shutdown with hysteresis to prevent over temperature stress
- Under-voltage lockout protection to prevent under-voltage operation

Light Load Mode (LLM) Operation

The ER6230QI uses a proprietary Light Load Mode (LLM) to provide high efficiency at low output currents. When the LLM/SYNC pin is asserted high, the device is in automatic LLM "Detection" mode. When the LLM/SYNC pin is low, the device is forced into PWM mode. In automatic LLM "Detection" mode, when a low output current condition is detected, the device will:

(1) Step V_{OUT} up by approximately 1.0% above the nominal operating output voltage setting, V_{NOM} and as low as -0.5% below V_{NOM}, and then

(2) Shut down unnecessary circuitry, and then

(3) Monitor V_{OUT}

When V_{OUT} falls below V_{NOM}, the device will repeat (1), (2), and (3). The voltage step-up, or pre-positioning, improves transient droop when a load transient causes a transition from LLM mode to PWM mode. If a load transient occurs, causing V_{OUT} to fall below the threshold V_{MIN}, the device will exit LLM operation and begin normal PWM operation. Figure 5 demonstrates V_{OUT} behavior during the transition into and out of LLM operation.

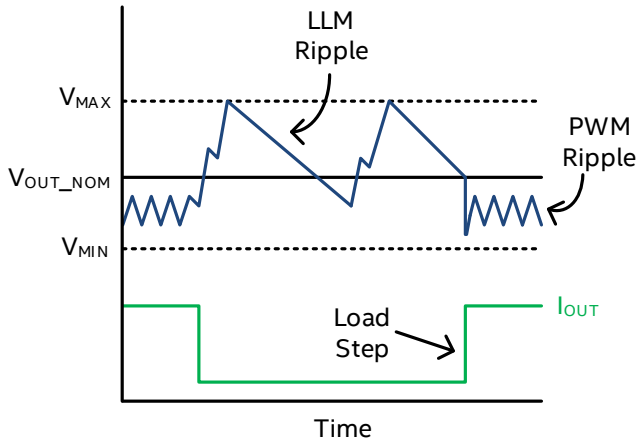


Figure 5: Light Load Mode Operation Illustration

Many multi-mode DCDC converters suffer from a condition that occurs when the load current increases only slowly so that there is no load transient driving V_{OUT} below the V_{MIN} threshold. In this condition, the device would never exit LLM operation. This could adversely affect efficiency and cause unwanted ripple. To prevent this from occurring, the ER6230QI periodically exits LLM mode into PWM mode and measures the load current. If the load current is above the LLM threshold current, the device will remain in PWM mode. If the load current is below the LLM threshold, the device will re-enter LLM operation. There may be a small overshoot or undershoot in V_{OUT} when the device exits and re-enters LLM. The load current at which the device will enter LLM mode is a function of input and output voltage, and the RLLM pin resistor. For PWM only operation, the RLLM pin can be left open. There is a minimum headroom between input and output of 800mV in order to engage into LLM mode.

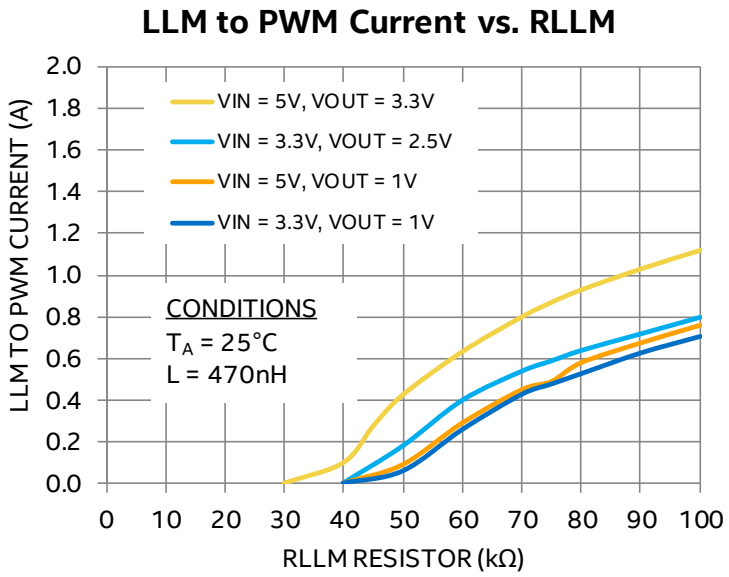


Figure 6: LLM to PWM Transition Point with Various RLLM Values

Enable Operation

The enable (ENABLE) pin provides a mean to startup or to shutdown the device. When the ENABLE pin is asserted high, the device will undergo a normal soft-start where the output will rise monotonically into regulation. Asserting a logic low on this pin will deactivate the device by initiating a soft-shutdown. The soft-shutdown time is approximately 5 times faster than the soft-start time. The ENABLE pin is internally pulled low by a non-passive ressitance of 250kΩ.

Soft-Start Operation

The soft-start circuitry will reduce inrush current during startup as the regulator charges the output voltage up to nominal level gradually. The output rise time is controlled by the soft-start capacitor, which is placed between the SS pin and the AGND pin. When the part is enabled, the soft-start (SS) current generator charges the SS capacitor in a linear manner. Once the voltage on the SS capacitor reaches 0.75V, the controller selects the intenral bandgap voltage as the reference. The voltage across the SS capacitor will continue ramping up until it reaches around 1.36V. The rise time is defined as the time needed by the output voltage to go from zero to the programmed value. The rise time (t_{RISE}) is given by the following equation:

$$t_{RISE}\ [ms] = C_{ss}\ [nF] \times 0.08$$

With a 15nF soft-start capacitance on the SS pin, the soft-start rise time will be set to 1.2ms. The recommended range for the value of the SS capacitor is between 10nF and 100nF. Note that excessive bulk capacitance on the output can cause an over current event on startup if the soft-start time is too low. Refer to the Compensation and Transient Response section for details on proper bulk capacitance usage.

POK Operation

The Power OK (POK) is an open drain signal to indicate if the output voltage is within the specified range. POK is asserted high when the rising output voltage exceeds 90% of the programmed output voltage. An external resistor (10k) should be connected to the intput in order to pull POK high. If the nominal output voltage falls below 90%, the POK signal will be asserted low by an internal 4mA pull-down transistor.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the peak current flowing through the topside power PFET. When the sensed current exceeds the over current trip point (see Electrical Characteristics Table), both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed, the over-current protection circuit will enable normal PWM operation. If the over-current condition persists, the soft start capacitor will gradually discharge causing the output voltage to fall. When the OCP fault is removed, the output voltage will ramp back up to the desired voltage. This cycle can continue indefinitely as long as the over current condition persists. The OCP circuit will disable operation and protect the device from excessive current during operation without compromising the full load capability of the device.

Thermal Protection

The thermal shutdown circuit disables the device operation (switching stops) when the junction temperature exceeds 160°C. When the junction temperature drops by approximately 25°C, the converter will re-start with a normal soft-start. By preventing operation at excessive temperatures, the thermal shutdown circuit will protect the device from overstress.

Input Under-Voltage Lock-Out (UVLO)

When the device input voltage falls below UVLO, switching is disabled to prevent operation at insufficient voltage levels. During startup, the UVLO circuit ensures that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis and input de-glitch circuits are incorporated in order to ensure high noise immunity and prevent a false trigger in the UVLO voltage region.

APPLICATION INFORMATION

Output Voltage Setting

The ER6230QI output voltage is programmed using a simple resistor divider network (R_A and R_B). Figure 7 shows the resistor divider configuration.

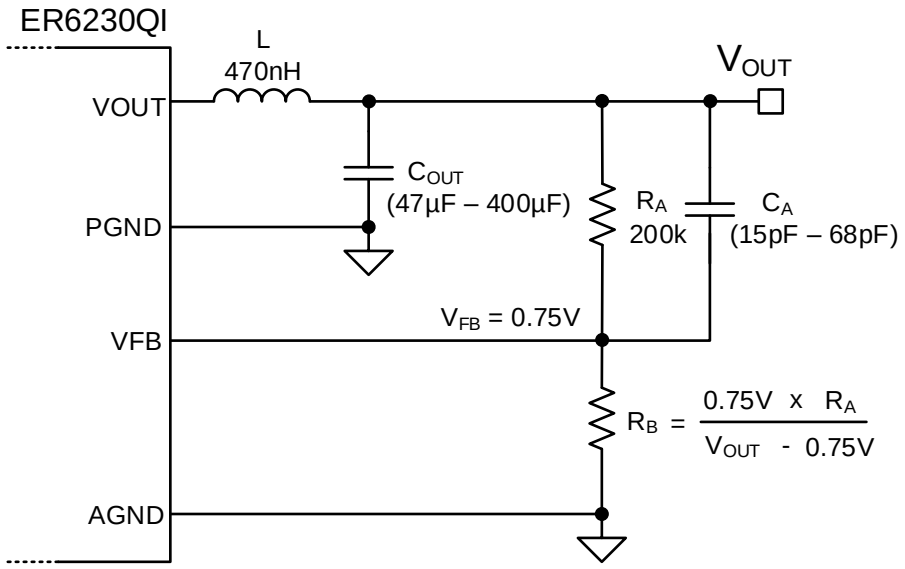


Figure 7: V_{OUT} Resistor Divider & Compensation Capacitor

The recommended R_A resistor value is 200kΩ and the feedback voltage is typically 0.75V. Depending on the output voltage (V_{OUT}), the R_B resistor value may be calculated as shown in Figure 7. Since the accuracy of the output voltage setting is dependent upon the feedback voltage and the external ressitors, 1% or better resistors are recommended. The external compensation capacitor (C_A) is also required in parallel with R_A. Depending on input and output voltage, the recommended external compensation values are shown in Table 1.

Table 1: External Compensation Recommendations

V_{IN}	V_{OUT}	R_B	C_A	R_A	C_{OUT} (0805)
2.7V – 6.6V	0.75V	OPEN	33pF	200kΩ	2 x 47µF
	0.9V	1MΩ	33pF		
	1.0V	604kΩ	27pF		
	1.2V	332kΩ	27pF		
	1.5V	200kΩ	22pF		
	1.8V	143kΩ	22pF		
	2.5V	84.5kΩ	18pF		
	3.3V	59kΩ	15pF		

Compensation and Transient Response

The ER6230QI uses an enhanced type III voltage mode control architecture. Most of the compensation is internal, which simplifies the design. In some applications, improved transient performance may be desired with additional output capacitors (C_{OUT}). In such an instance, the phase-lead capacitor (C_A) can be adjusted depending on the total output capacitance. Using Table 1 as the reference for C_A, if C_{OUT} is increased, then the C_A should also be increased. The relationship is linearly shown below:

$$\Delta C_{OUT} \approx +100\mu F \rightarrow \Delta C_A \approx +10pF$$

As C_{OUT} increases and the C_A value is adjusted, the device bandwidth will reach its optimization level (at around 1/10th of the switching frequency). As shown in Table 1, the recommended C_A value is lower for the 5V input than 3.3V input. This is to ensure that the loop bandwidth is not over extended due to the increased gain at the higher input voltage range. The C_A value may be extrapolated for other input voltages. The limitation for adjusting the compensation is based on diminished return. Further adjustments by increasing C_{OUT} and increasing C_A may not yield better transient response or in some situations cause lower gain and phase margin. Over compensating with excessive output capacitance may also cause the device to trigger current limit on startup due to the energy required to charge the output up to regulation level. Due to such limitations, the recommended maximum output capacitance (C_{OUT_MAX}) is 400µF and the recommended maximum phase-lead capacitance (C_{A_MAX}) is 68pF. Note that lower output voltages can accommodate a higher Ca value.

Inductor Selection

The inductor is one of the most important passive elements in a buck regulator. The inductor can affect the efficiency, transient response, output ripple and over-all system level noise. In most power applications, choosing an inductor comes down to the size, inductance, DC resistance (DCR) and the cost of the inductor. These parameters need to be taken into consideration when selecting an inductor. Generally, the higher the inductance, the more windings are needed around a magnetic core and the larger the inductor. Higher inductance usually increases solution size. Applications with a space constraint may want to select smaller sized inductors; however, smaller sized inductors at the same inductance usually have higher DCR, which can lower the efficiency, so designing is often a trade-off between size and efficiency. Note that the inductor's peak-to-peak current is inversely proportional to the inductance as shown:

$$\Delta I = \frac{(\mathrm{Vin} - \mathrm{Vout})D}{\mathrm{L\ x\ f}}$$

ΔI = Inductor's Peak-to-Peak Current

Vin = Input Voltage

Vout = Output Voltage

D = Duty Cycle = Vout/Vin

L = Inductance

f = Buck Regulator Switching Frequency

If the inductance is too low it will have a higher peak-to-peak current which may activate the peak detection current limit protection at a low output current level. When inductance is lower than recommended, the buck regulator may not be able to support its full load.

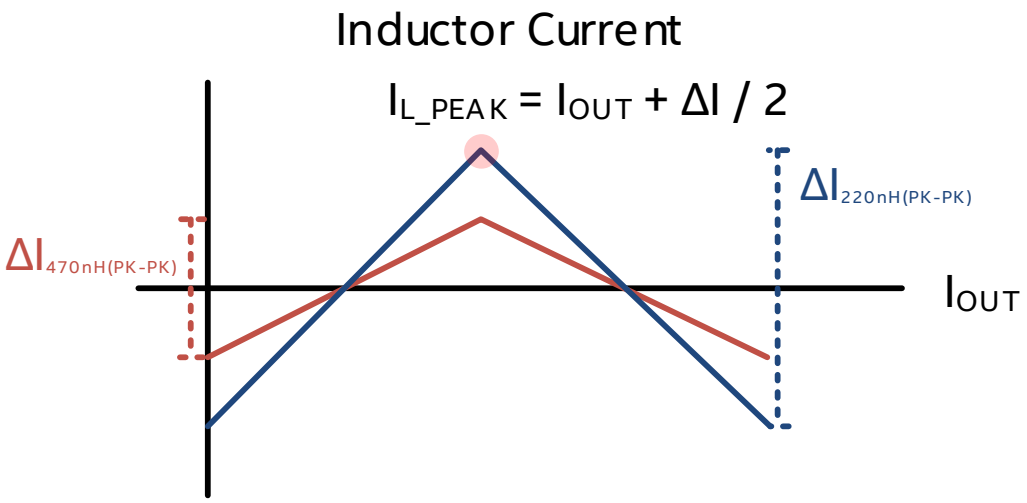


Figure 8: Inductor Peak-to-Peak Current

Since the ER6230QI switches at 1.9MHz, it is designed to accommodate a 470nH inductance with 3A to 4A of saturation. Do not use inductors with lower saturation current than the maximum output current needed in the application. When the inductor saturates, it loses inductance and this will increase its peak-to-peak current. This can sometimes cause false current limit triggers and shutdown the device. Always have sufficient margin. Figure 8 shows the difference in peak-to-peak current depending on the inductance (470nH versus 220nH). A lower than optimum inductance may also introduce peak currents that can increase the system level noise and should be avoided. See Table 2 for a list of recommended inductors.

Table 2: Recommended Inductors

DESCRIPTION	MFG	P/N
L = 470nH I_{SAT} > 3A	FDK	MIPSAZ3225DR47FR
	Murata	DFE252012F-R47M=P2
	Mag Layer	GMPI-322512-R50M-E-RU

Input Capacitor Selection

The input of synchronous buck regulators can be very noisy and should be decoupled properly in order to ensure stable operation. In addition, input parasitic line inductance can attribute to higher input voltage ripple. The ER6230QI requires a minimum of 2 x 22µF 0805 input capacitors. As the distance of the input power source to the input of the ER6230QI is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Low-ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Table 3: Recommended Input Capacitors

DESCRIPTION	MFG	P/N
22µF ±20%, 10V X5R, 0805	Taiyo Yuden	LMK212BBJ226MG-T
	Murata	GRM21BR61A226ME51
	TDK	C2012X5R1A226M125AB

Output Capacitor Selection

The output ripple of a synchronous buck converter can be attributed to its inductance, switching frequency and output decoupling. The ER6230QI requires a minimum of 2 x 47µF 0805 output capacitors. Low ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Table 4: Recommended Output Capacitors

DESCRIPTION	MFG	P/N
47µF ±20%, 10V X5R, 0805	Taiyo Yuden	LMK212BBJ476MG-T
	Murata	GRM21BR61A476ME15L
	TDK	C2012X5R1A476M125AC

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance (ESR) and effective series inductance (ESL):

$$Z = ESR + ESL$$

The resonant frequency of a ceramic capacitor is inversely proportional to the capacitance. Lower capacitance corresponds to higher resonant frequency. When two capacitors are placed in parallel, the benefit of both are combined. It is beneficial to decouple the output with capacitors of various capacitance and size. Placing them all in parallel reduces the impedance and will hence result in lower output ripple.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

THERMAL CONSIDERATIONS

Thermal considerations are important elements of power supply design. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be taken into account. The Intel Enpirion package technology helps alleviate some of those concerns.

The ER6230QI DC-DC converter is packaged in a 4mm x 4mm x 0.85mm 24-pin QFN package. The QFN package is constructed with an exposed thermal pad. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 160°C.

The following example and calculations illustrate the thermal performance of the ER6230QI with the following parameters:

V_{IN} = 5V

V_{OUT} = 3.3V

I_{OUT} = 3A

First, calculate the output power.

$P_{OUT} = V_{OUT} \times I_{OUT} = 3.3V \times 3A = 9.9W$

Next, determine the input power based on the efficiency (η) shown in Figure 9.

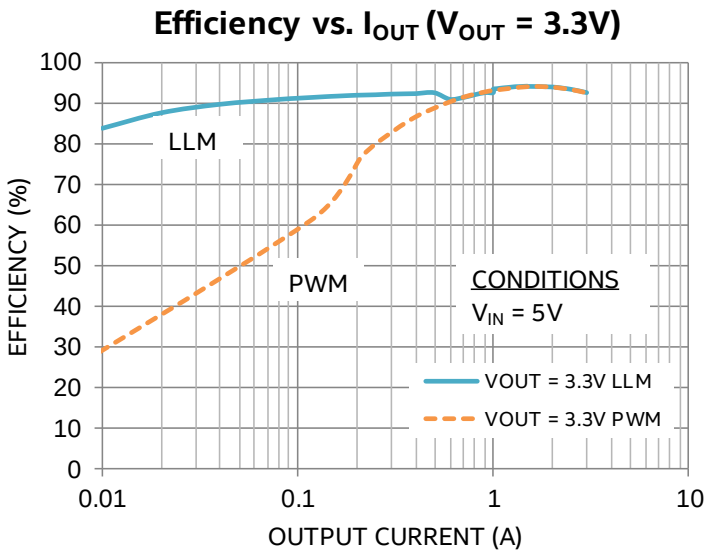


Figure 9: Efficiency vs. Output Current

For V_{IN} = 5V, V_{OUT} = 3.3V at 3A, η ≈ 92.5%

$\eta = P_{OUT} / P_{IN} = 92.5\% = 0.925$

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 9.9W / 0.925 \approx 10.7W$

The total power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_{TOTAL} = P_{IN} - P_{OUT}$

= 10.7W – 9.9W ≈ 0.8W

The total power dissipation includes the loss in the ER6230QI plus the loss in the inductor, but since we are not interested in the inductor's temperature change, we will subtract that to get the ER6230QI's power loss.

$P_{INDUCTOR} = I_{OUT}^2 \times DCR = 3^2 \times 0.020$ (20mΩ is the DCR of the inductor used in this example)

$P_{INDUCTOR} = 3^2 \times 0.020 = 0.18W$

The power dissipation into the ER6230QI package is equal to the total power dissipation minus the inductor's power loss.

$P_{ER6230} = P_{TOTAL} - P_{INDUCTOR} = 0.8W – 0.18W = 0.62W$

With the power dissipation of the ER6230QI known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The ER6230QI has a θ_{JA} value of 30°C/W without airflow.

Determine the change in temperature (ΔT) based on P_{ER6230} and θ_{JA}.

$\Delta T = P_{ER6230} \times \theta_{JA}$

$\Delta T \approx 0.62W \times 30°C/W \approx 18.6°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 18.6°C \approx 43.6°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} – P_{ER6230} \times \theta_{JA}$

$\approx 125°C – 18.6°C \approx 106.4°C$

The maximum ambient temperature the device can reach is 106.4°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION CIRCUIT

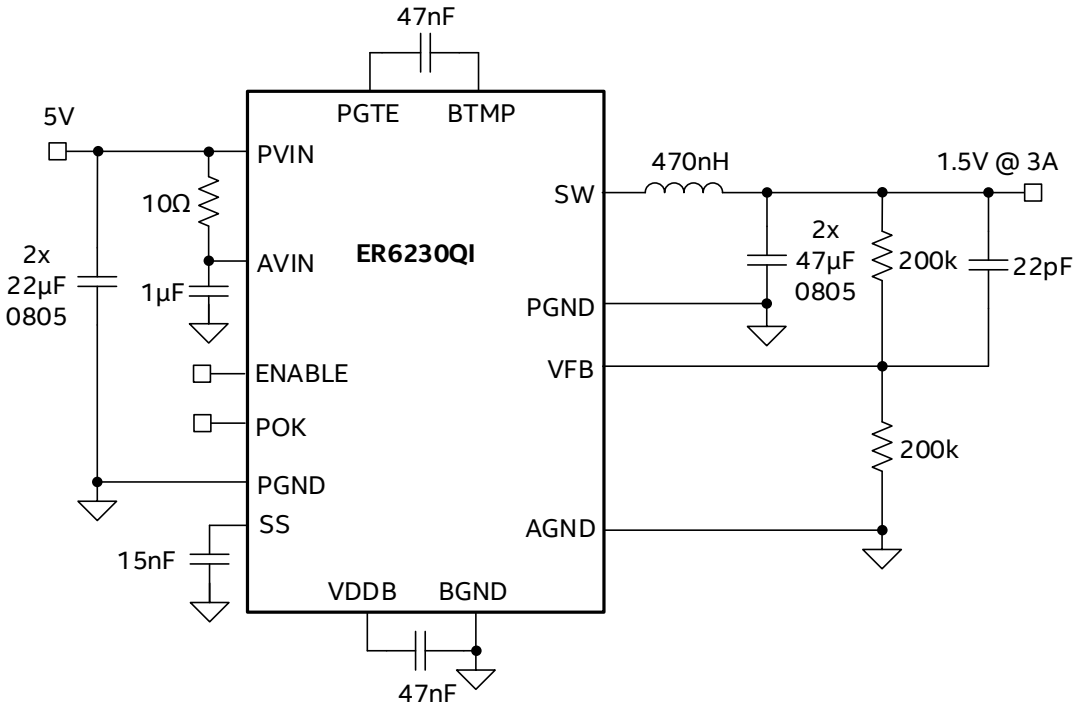


Figure 10: Typical Application Circuit for V_{OUT} = 1.5V

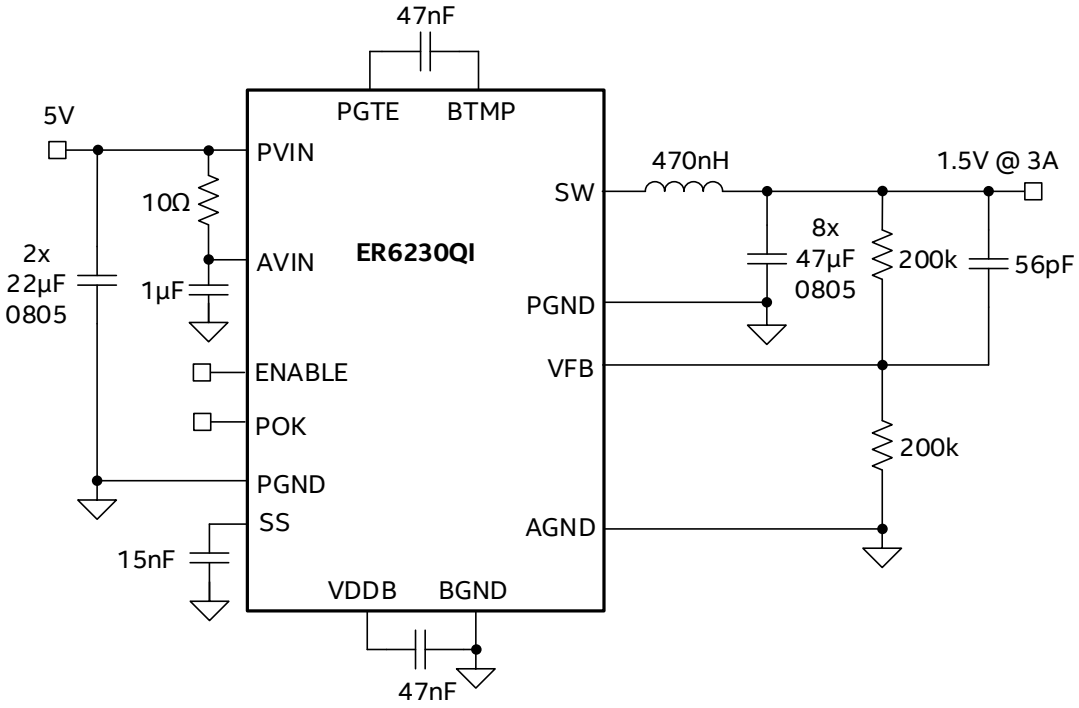


Figure 11: Improved Transient Response Application Circuit for V_{OUT} = 1.5V

LAYOUT RECOMMENDATIONS

Figure 12 shows critical components and layer 1 traces of a recommended minimum footprint ER6230QI layout. ENABLE and other small signal pins need to be connected and routed according to specific customer application. Visit the Enpirion Power Solutions website at www.altera.com/powersoc for more information regarding layout. Please refer to this Figure 12 while reading the layout recommendations in this section.

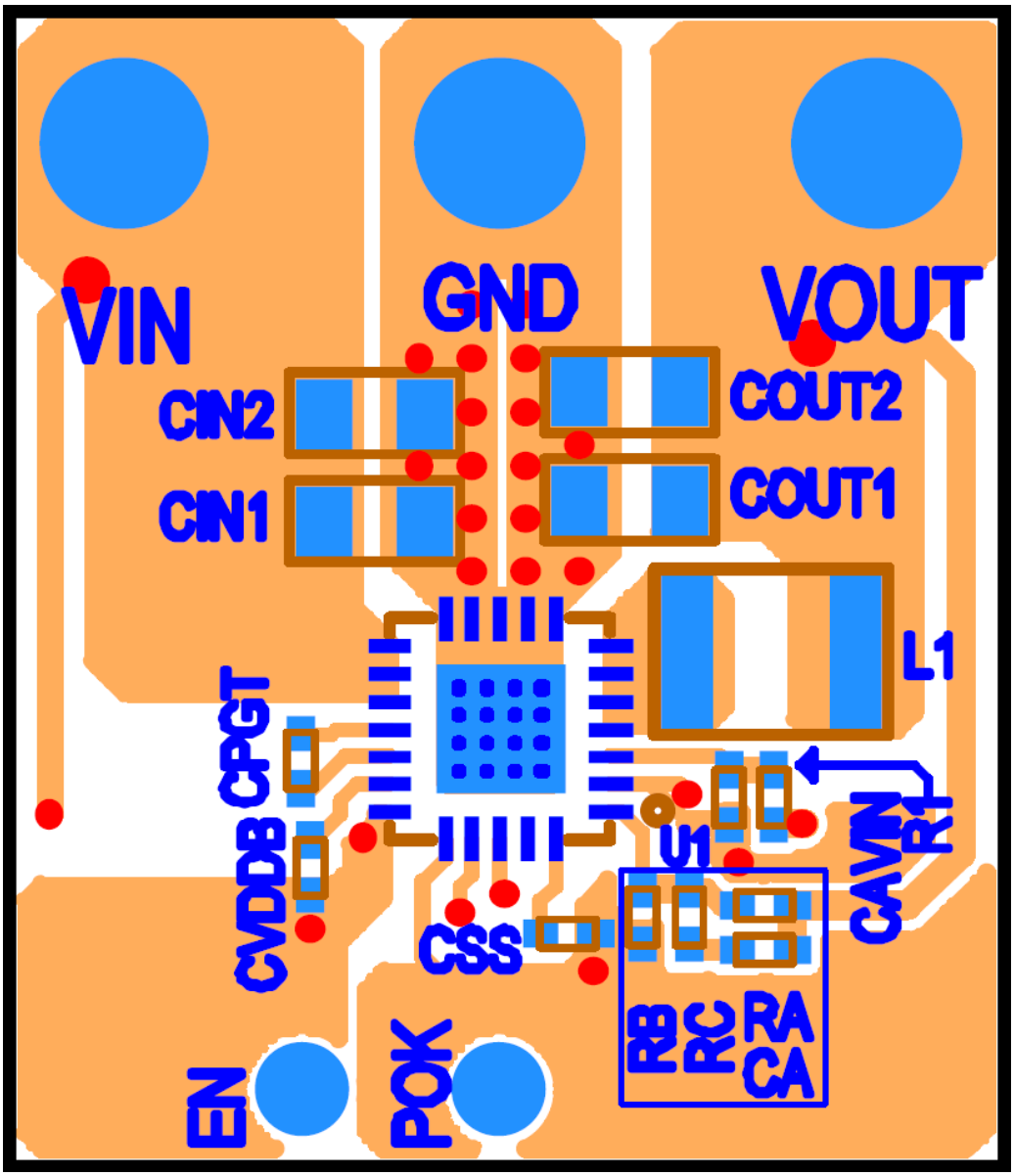


Figure 12: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Rotate the inductor in such a way that the input and output filter capacitors are placed on the same side of the PCB, and as close to the ER6230QI package as possible. The filter capacitors should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Voltage and GND traces between the capacitors and the ER6230QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Half of the PGND pins are dedicated to the input circuit and the other half to the output circuit. The slit shown in Figure 12 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be on the 2nd layer (below the surface layer). This ground plane should be continuous and un-interrupted.

Recommendation 4: The large thermal pad underneath the device must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1-oz. copper plating on the inside wall, making the finished hole size around 0.2mm to 0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figure 12.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. Put the vias under the capacitors along the edge of the GND copper closest to the Voltage copper. Please see Figure 12. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 12 this connection is made at the input capacitor furthest from the PVIN pin and on the input source side. Avoid connecting AVIN near the PVIN pin even though it is the same node as the input ripple is higher there.

Recommendation 7: The V_{OUT} sense point should be connected at the last output filter capacitor furthest from the VOUT pins (near C6). Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 8: Keep R_A, C_A, R_C and R_B close to the VFB pin (see Figure 12). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane. The AGND should connect to the PGND at a single point from the AGND pin to the PGND plane on the 2nd layer.

Recommendation 9: The layer 1 metal under the device must not be more than shown in Figure 12. See the following section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

DESIGN CONSIDERATIONS

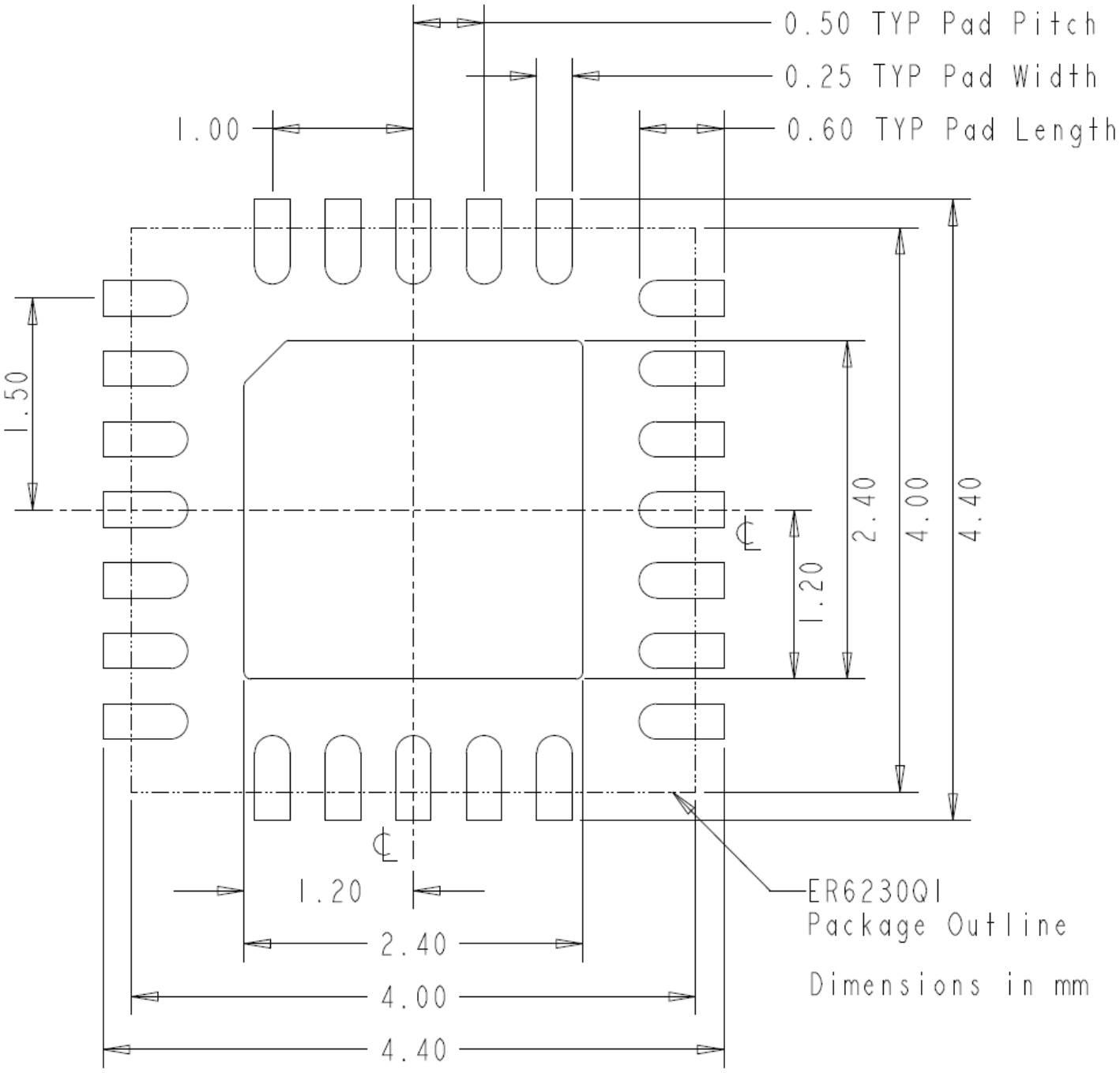


Figure 13: Landing Pattern with Solder Stencil (Top View)

The solder stencil aperture for the thermal PGND pad is shown in Figure 13 and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

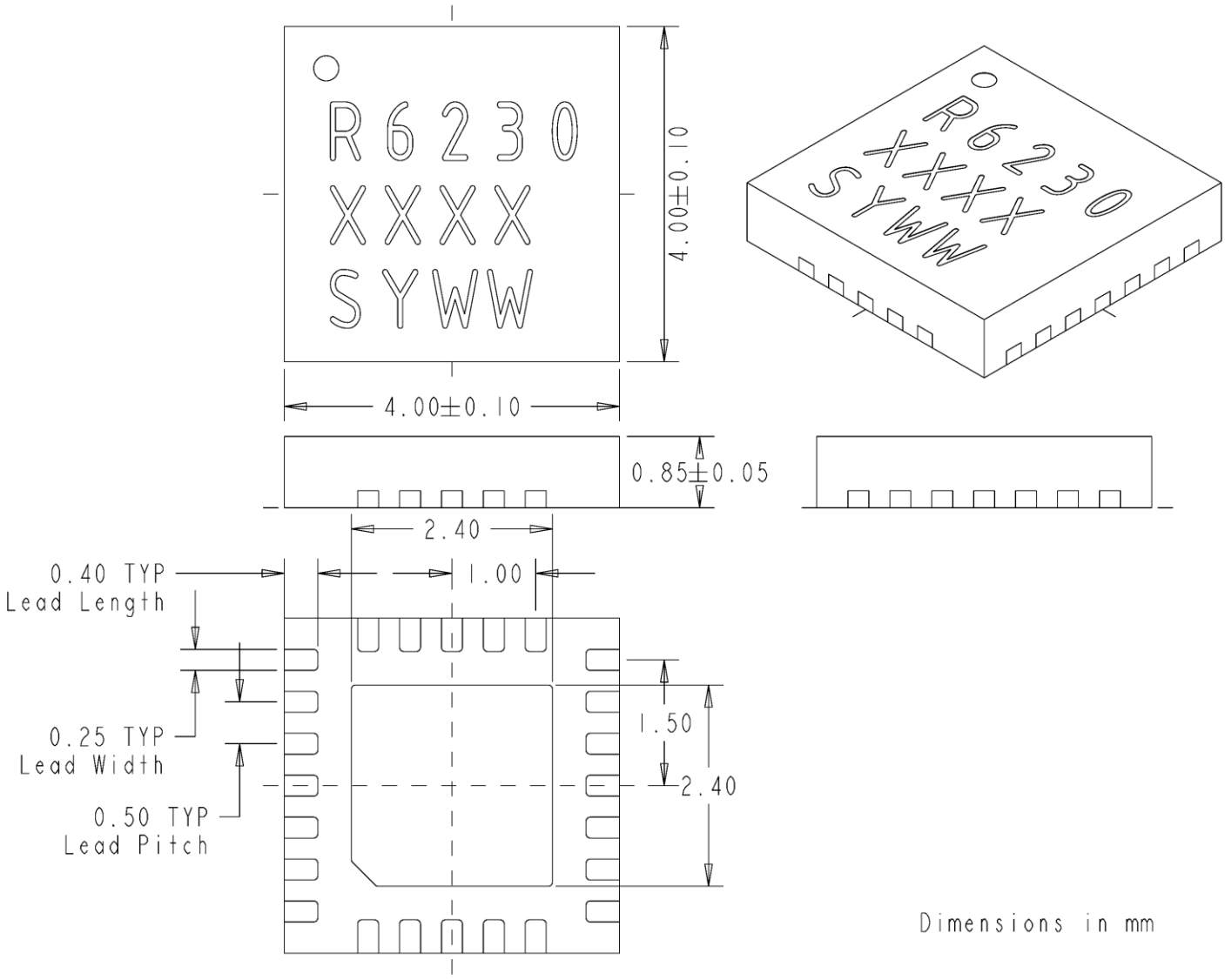


Figure 14: ER6230QI Package Dimensions (Lower Image is Bottom View)

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
A	March, 2018	Datasheet Initial Release
B	August, 2018	Updated ENABLE description by removing text on float turning on device.
C	November, 2018	Updated Switching Frequency specification on Electrical Characteristics Table, 1.5MHz (min) and 2.4MHz (max)

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.altera.com/enpirion

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