ET6160LI 70A Power Stage

Power Stage with Integrated Current and Temperature Sense

DESCRIPTION

The Intel® Enpirion® ET6160LI is a monolithic Smart Power Stage with integrated current and temperature monitors. The power stage is optimized to operate with the ED8401 scalable multi-phase controller.

The ET6160LI monolithic output stage offers high system efficiency while offering high switching frequencies from 500kHz to 1MHz. Monolithic construction provides excellent thermal impedance for HS, LS, and Driver sections and does not require complex internal copper clip technology.

The integration of the drivers and the MOSFETs allows for very accurate current reconstruction (IMON) protecting against large transient events at the load. Integrated thermal information from the ET6160LI also helps the controller monitor the system health and react to temperature driven events.

The 5x6mm package is designed specifically for high thermal stress environments. The pad layout is designed to reduce internal and solder joint stress from temperature cycling thereby increasing long term reliability of the package and solder joints.

FEATURES

- Up to 70A of Current Capability
- High Efficiency for FPGA and ASIC Core Supplies
- Wide Input Range 4.5V – 16V
- Integrated High Accuracy Current Monitor (IMON)
- True Junction Temperature Monitor (TMON)
- Catastrophic Fault Protection
  - Over Temperature Protection (OTP)
  - High/Low-Side Current Protection (OCP)
  - Under Voltage Lock-Out (UVLO)
  - Over Voltage Lock-Out (OVLO)
- Optimized for Operation with ED840X Controllers
- Compact 5.0mm x 6.0mm x 0.7mm LGA Package
- High Reliability Universal Footprint
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- FPGA and ASIC Core Power Rails
- 5G Wireless Base Station and Remote Radio
- High Reliability Communications Infrastructure
- Data Analytics and Acceleration Applications

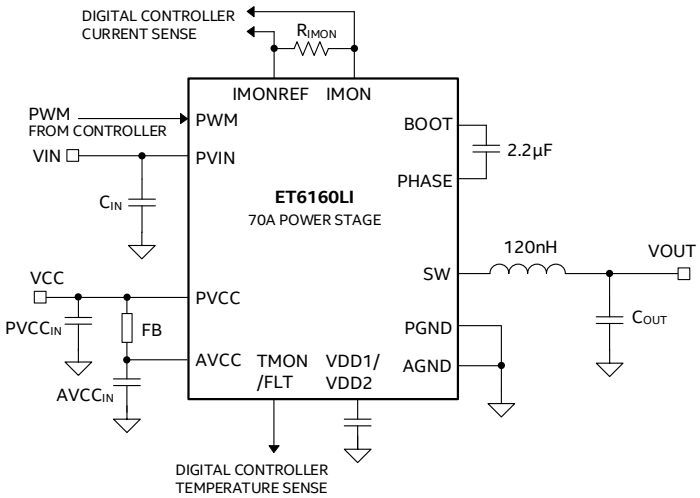


Figure 1: Simplified Applications Circuit

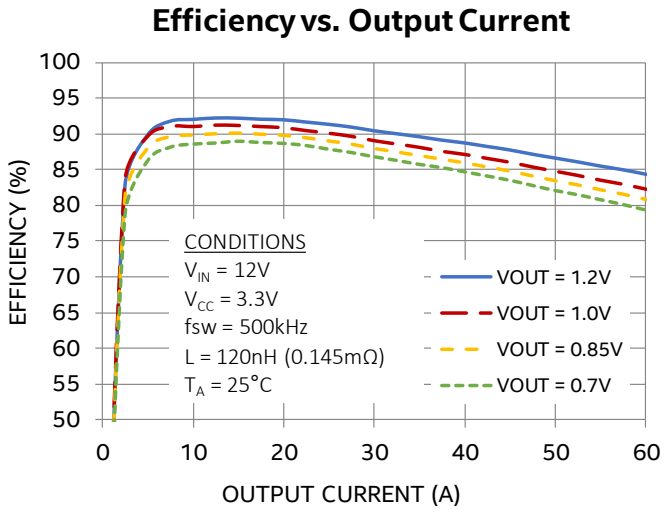


Figure 2: Efficiency at V_{IN} = 12V

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
ET6160LI	T6160	-40°C to +125°C	39-pin 5.0mm x 6.0mm x 0.7mm) LGA

Packing and Marking Information:

www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

PIN FUNCTIONS

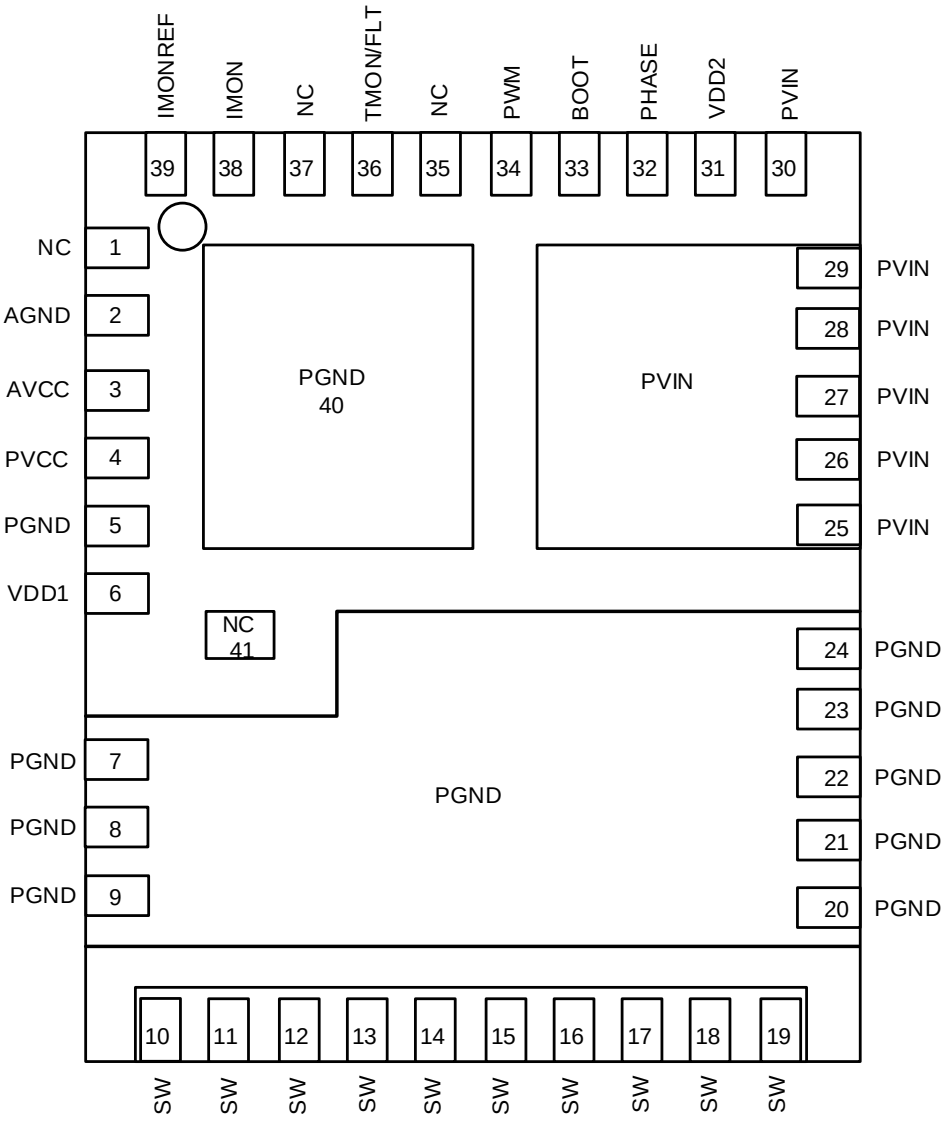


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

NOTE C: Actual bottom of the device package has stress relief lines not shown in the Pin Diagram. Follow Landing Pattern and Solder Stencil Recommendations for PCB layout.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 35, 37, 41	NC	-	No Connect. This pin must be soldered to PCB but not electrically connected to anything. Failure to follow this guideline may result in device damage.
2	AGND	Ground	Analog ground. Supply return for AVCC. Connect to the low impedance power-ground plane.
3	AVCC	Input	Analog supply voltage terminal. Connect to PVCC through ferrite bead. A 3.3V supply voltage on AVCC is required for operation. Decouple with a 2.2µF and a 1µF capacitor to AGND.
4	PVCC	Input	Power supply voltage terminal. Connect to AVCC through ferrite bead. A 3.3V supply voltage on PVCC is required for operation. Decouple with a 10µF and a 2.2µF capacitor to PGND.
5, 7, 8, 9, 20, 21, 22, 23, 24	PGND	Ground	Input/Output power ground. Connect to the low impedance ground electrode of the input and output filter capacitors.
6	VDD1	Output	Internal 1.8V LDO supply terminal. Decouple with a 22µF and 2.2µF capacitor to PGND.
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	SW	Output	Switch Node. Connect with external power inductor.
25, 26, 27, 28, 29, 30	PVIN	Input	Input power supply. Connect to input power supply and decouple with capacitors to PGND pins. Refer to the Layout Recommendation section.
31	VDD2	Output	Internal 1.8V LDO supply terminal. Decouple with a 1nF capacitor to PGND.
32	PHASE	Input/Output	Switch node connection for the floating high-side supply.
33	BOOT	Input/Output	Floating high-side gate-drive supply. Connect to PHASE with the CBOOT capacitor (2.2µF recommended).
34	PWM	Output	PWM Input Signal from a compatible controller. ED8401 controller is recommended for multi-phase buck converter optimization.
36	TMON/FLT	Input/Output	Temperature monitor and fault flag. Follows internal junction temperature at 8mV/°C from 0 to 1.8V. During a fault, TMON will be pulled high to AVCC. Refer to the TMON/FLT description for details.
38	IMON	Output	Current monitor. Provides a high-bandwidth current signal proportional to inductor current with a gain of 1µA/A. Connect IMON to the IMON reference of the Digital Controller through the R_{IMON} resistor. Refer to the IMON description for further details.

PIN	NAME	TYPE	FUNCTION
39	IMONREF	Output	IMON reference voltage. Internally generated 1.25V used for the Digital Controller's current sense reference. This voltage may be used in place of an external IMON reference voltage for current sensing. Refer to the IMON description for further details.
40	PGND PAD	Ground	Power ground thermal pad. Not a perimeter pin. Connect thermal pad to the system GND plane for heat-sinking purposes. Refer to the Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Voltages are referenced to ground unless otherwise noted.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power FET Input	PVIN	-0.3	20	V
Power Stage Control Input	AVCC, PVCC	-0.3	5.5	V
Gate-Drive Supply	VDD1, VDD2	-0.3	2.1	V
Current Monitor	IMON	-0.3	AV_{CC} + 0.3	V
Current Monitor Reference	IMONREF	-0.3	AV_{CC} + 0.3	V
Temperature Monitor	TMON	-0.3	AV_{CC} + 0.3	V
PWM Logic	PWM	-0.3	AV_{CC} + 0.3	V
SW Voltage DC	V_{SW}		PVIN + 0.3	V
SW Voltage Peak < 10ns	V_{SW_PEAK}		25	V
BOOT	V_{BOOT}		V_{SW} + 2.1	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±1000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	PVIN	4.5	16	V
Power Stage Controller Input Range	AVCC, PVCC	3.0	3.6	V
Output Current Range (2)	I_{OUT}	0	70	A
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	145	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	25	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	10	°C/W
Thermal Resistance: Junction to Substrate (0 LFM)	$\theta_{J\text{-}SUB}$	2.2	°C/W
Thermal Resistance: Junction to Top (0 LFM)	$\theta_{J\text{-}TOP}$	1.5	°C/W

(1) These values are provided for information only.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{PVIN} = 12V, AVCC = PVCC = 3.3V, Minimum and Maximum values are over operating ambient temperature range (-40°C to 85°C) unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY CHARACTERISTICS						
PVIN Tri-state Current	I_{TRI_PVIN}	PWM tri-state		1	2	mA
PVIN Quiescent Current	I_{Q_PVIN}	V_{PVIN} = 12V, V_{OUT} = 1.2V, Load = 0A, f_{SW} = 500kHz		30		mA
PVIN Under-Voltage Lockout - Rising	$V_{UVR,PV}$		3.9	4.2	4.4	V
PVIN Under-Voltage Lockout Hysteresis	$V_{HYS,PV}$			400		mV
PVIN Over-Voltage Lockout - Rising	$V_{OVR,PV}$		16.5	17.5	18.5	V
PVIN Over-Voltage Lockout Hysteresis	$V_{OVRHYS,PV}$			0.6		V
PVCC Quiescent Current	$I_{Q,PVCC}$	PWM tri-state		0.1	2	µA
PVCC Run Mode	I_{PVCC}	Switching (500kHz)		40		mA
PVCC Run Mode	I_{PVCC}	Switching (1MHz)		80		mA
AVCC Under-Voltage Lockout Rising	$V_{UVR,CTRL}$		2.7	2.8	2.95	V
AVCC Under-Voltage Lockout Hysteresis	$V_{UVF,CTRL}$			150		mV
AVCC Quiescent Current	$I_{Q,AVCC}$	PWM tri-state		7.5	10	mA
AVCC Run Mode	I_{AVCC}	Switching (500kHz)		7.5	10	mA
AVCC Run Mode	I_{AVCC}	Switching (1MHz)		7.5	10	mA
INTERNAL SUPPLY VOLTAGE CHARACTERISTICS						
1.8V Under-Voltage Lockout – Rising[3]	VDD_{UVLO}	PVCC=3.3V	1.65	1.73	1.78	V
1.8V UVLO Hysteresis[3]	VDD_{HYS}			100		mV
PWM SIGNAL CHARACTERISTICS						
Input Current	I_{PWM}	Sinking, V_{PWM} = 3.3V		330		µA
		Sourcing, V_{PWM} = 0V		-275		µA
PWM Logic Low level	V_{IL_PWM}	PVCC = 3.3V	0.60	0.8	0.98	V
PWM Logic High level	V_{IH_PWM}	PVCC = 3.3V	2.25	2.40	2.60	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Tri-State Upper Threshold	V_{TRI_HI}		2.055	2.2	2.45	V
Tri-State Lower Threshold	V_{TRI_LO}		0.7	0.96	1.2	V
Pull Up Resistance	R_{PWM_UP}	PWM pull-up to AVCC		12		kΩ
Pull Down Resistance	R_{PWM_DN}	PWM pull-down to ground		10		kΩ
Tri-State Open Voltage	V_{HIZ_PWM}		1.3	1.5	1.7	V
High-to-Low Propagation Delay	$t_{D,OFF}$			45		ns
Low-to-High Propagation Delay	$t_{D,ON}$			50		ns
Minimum PWM On-Time	t_{MIN_ON}			45		ns
Minimum PWM Off-Time	t_{MIN_OFF}			100		ns
Operating Switching Frequency Range	f_{SW}	Nominal switching frequency range	0.4	0.5	1.1	MHz
Maximum Duty Cycle	D_{MAX}			90		%
PWM Tri-State to SW Hi-Z	$t_{3HT}+t_{3SD}$			60		ns
	t_{3Rd}			60		ns
	t_{3RD}			60		ns
	$t_{3HT}+t_{3SD}$			60		ns
IMON CHARACTERISTICS						
IMON Current Gain[4]	h_{IMON}	ILOAD > 5A	0.95	1	1.05	µA/A
IMON Voltage Gain[4]	b_{IMON}	ILOAD > 5A, RIMON = 2.7kΩ	2.565	2.7	2.835	mV/A
IMON DC Accuracy		ILOAD = -30A (sinking)	-5	0	+5	%
IMON DC Accuracy		ILOAD = 30A (sourcing)	-5	0	+5	%
IMON DC Accuracy		ILOAD = 70A (sourcing)	-7	0	+7	%
IMON Voltage Range	IMON	Reference to ground	0.65		2.25	V
OCP Sourcing Fault Threshold	I_{OCP}	Peak Sourcing Current Limit		90		A
OCP Sinking Fault Threshold		Peak Sinking Current Limit		-60		A
TMON / FLT PIN CHARACTERISTICS						
Thermal Gain 25°C	ΔTMON			8		mV/°C
V_{TMON} at 0°C[2]	$TMON_{0°C}$			0.6		V
V_{TMON} at 25°C[2]	$TMON_{25°C}$			0.8		V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TMON} at 100°C[2]	$TMON_{100°C}$			1.4		V
V_{TMON} at 145°C[2]	$TMON_{145°C}$	OTP TMON voltage threshold		1.76		V
OTP Fault Temperature	T_{OTP}	Thermal shutdown protection		145		°C
OTP Recovery Temperature		Temperature must drop below before re-enabling PWM input		120		°C
OTP Hysteresis				25		°C
TMON Source Current	$TMON_{SRC}$			5		mA
$V_{TMON/FLT}$ [1]		If AVCC, PVCC or PVIN invalid at power up		0		V
$V_{TMON/FLT}$ [1]		Fault	3.0	V_{AVCC}	3.6	V
FAULT MODE – ALL FAULTS						
Delay Before Fault[1]				0.1		µs
Delay Before Retry[1]		Fixed Value		1		ms
Number of Retries		Hiccup Mode - 1ms intervals		Infinite		
Inductor Current Threshold Before Tri-stating (Sourcing)		During Active Brake Fault Mode	7	10		A
Inductor Current Threshold Before Tri-stating (Sinking)		During Active Brake Fault Mode		-10	-7	A

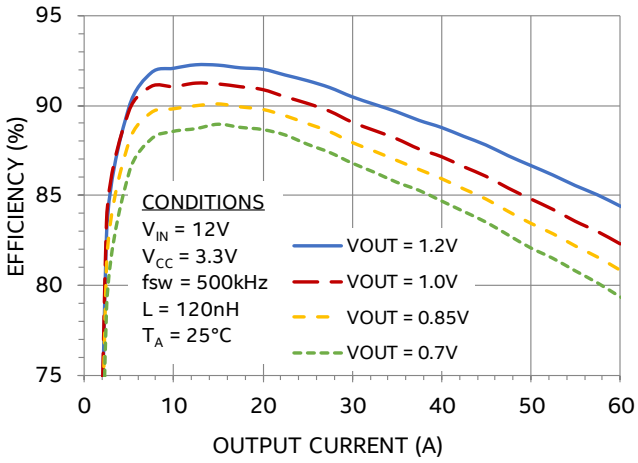
(3) Parameter not production tested but is guaranteed by design.

(4) IMON gain accuracy is guaranteed by ATE testing of high-side and low-side individually with offset adjustment.

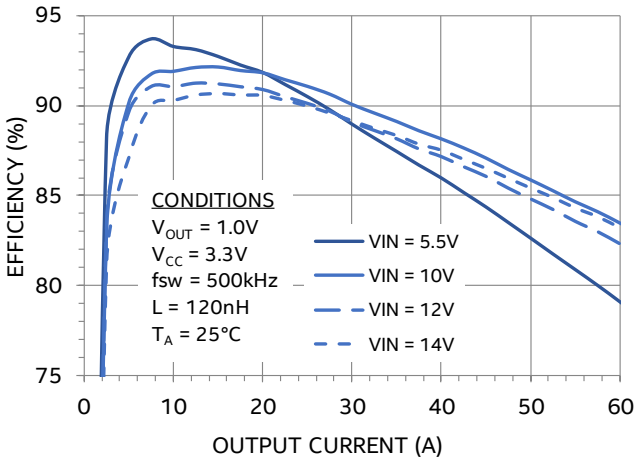
(5) Junction temperature is be kept below 125°C for high current measurements by external cooling.

TYPICAL PERFORMANCE CURVES

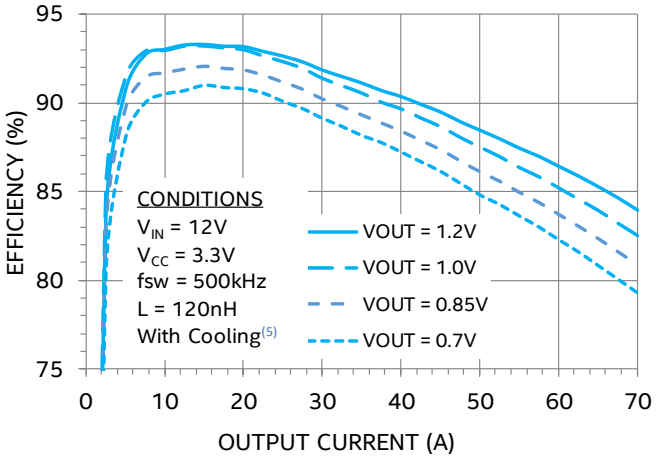
Efficiency vs. Output Current



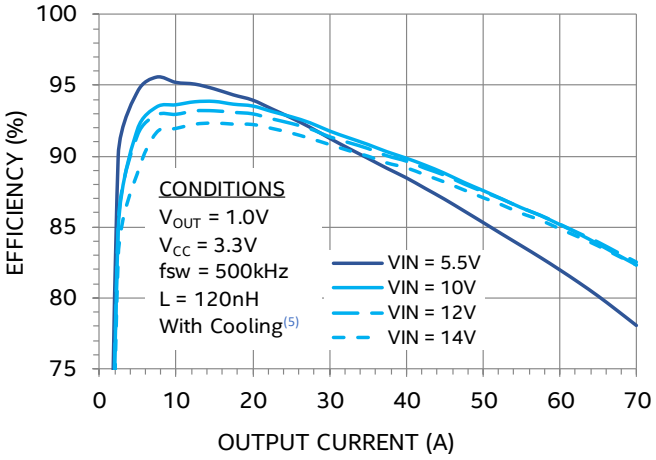
Efficiency vs. Output Current



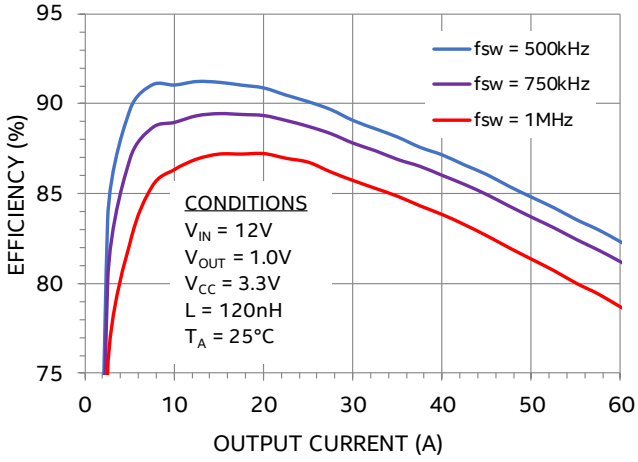
Efficiency vs. Output Current



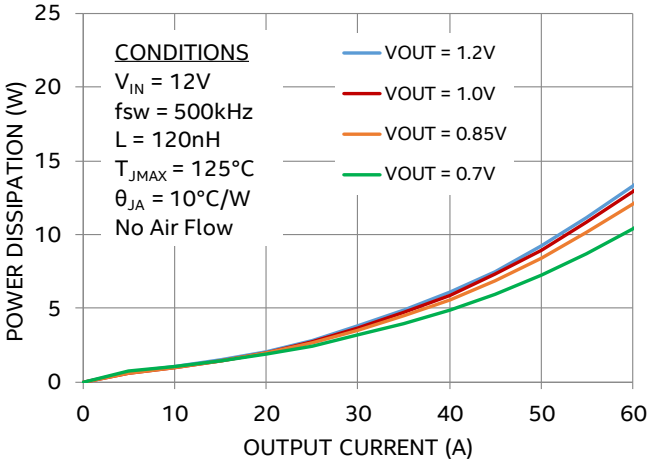
Efficiency vs. Output Current



Efficiency vs. Output Current

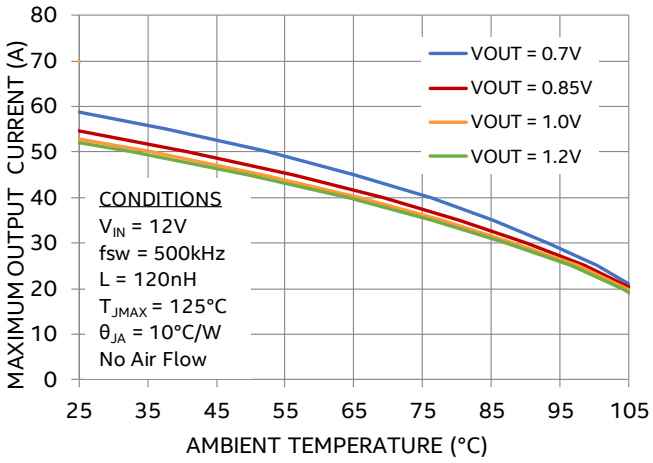


Power Dissipation

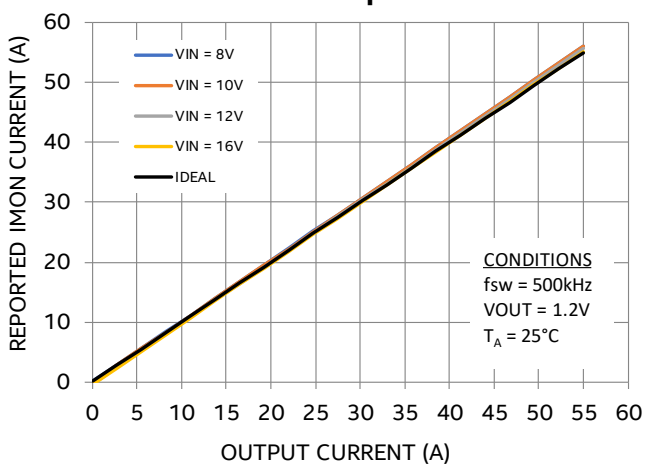


TYPICAL PERFORMANCE CURVES (CONTINUED)

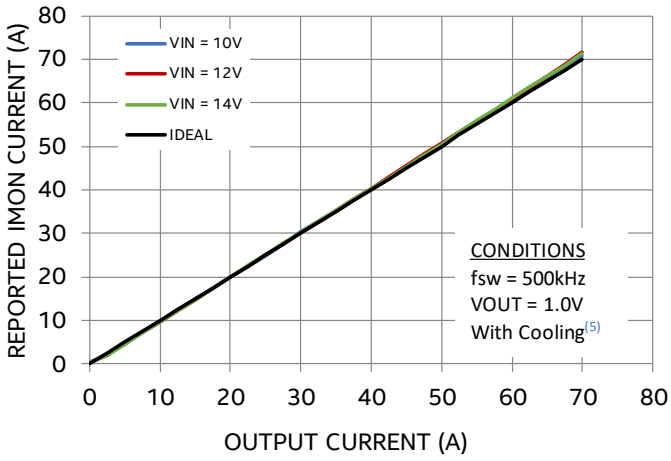
Output Current De-rating



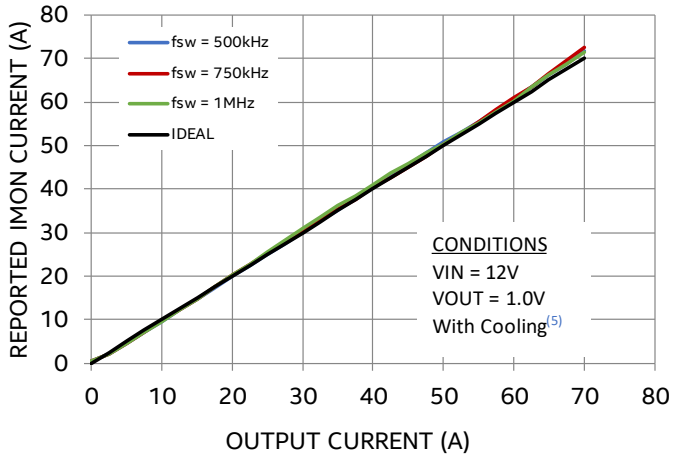
IMON vs. Output Current



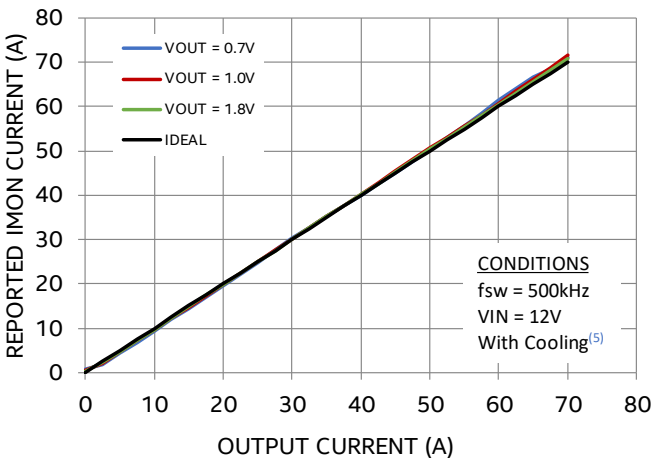
IMON vs. Output Current



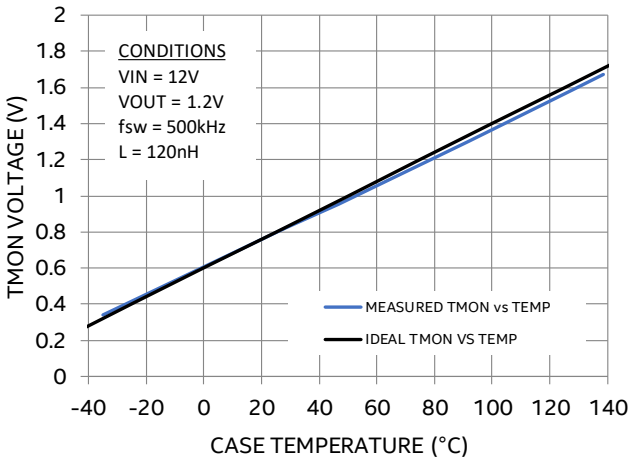
IMON vs. Output Current



IMON vs. Output Current

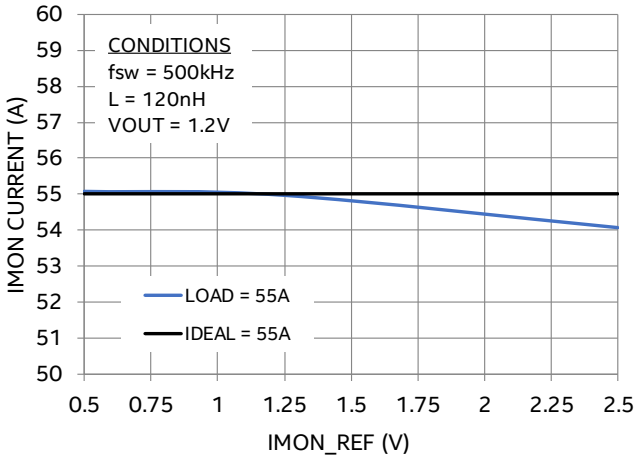


TMON vs. Temperature

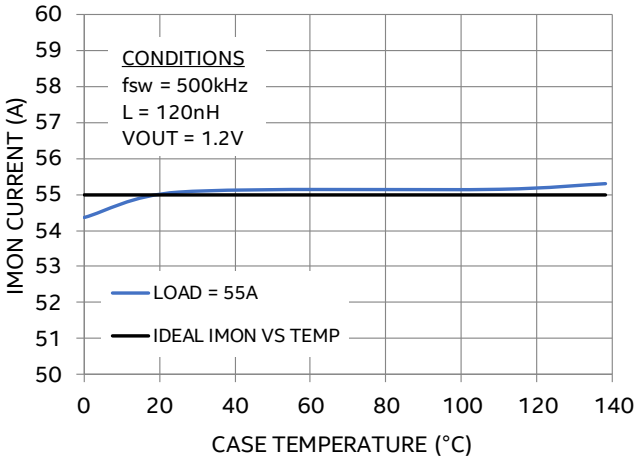


TYPICAL PERFORMANCE CURVES (CONTINUED)

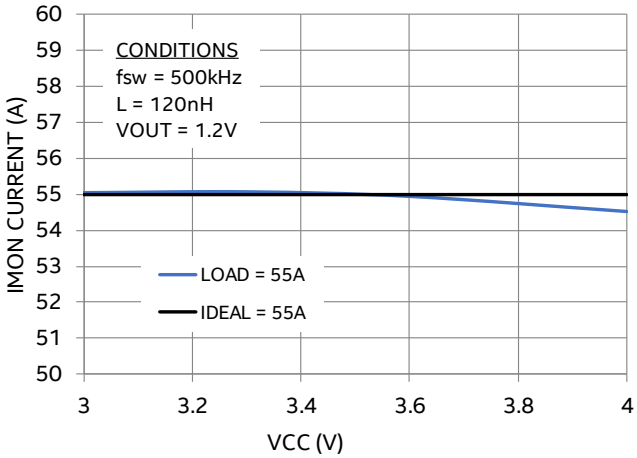
IMON vs. IMON_REF



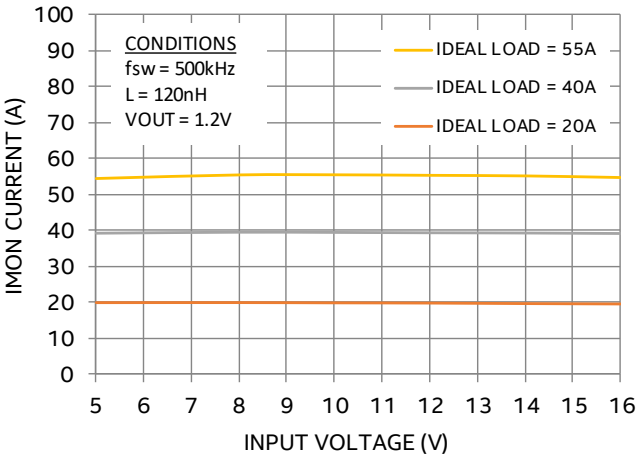
IMON vs. Temperature



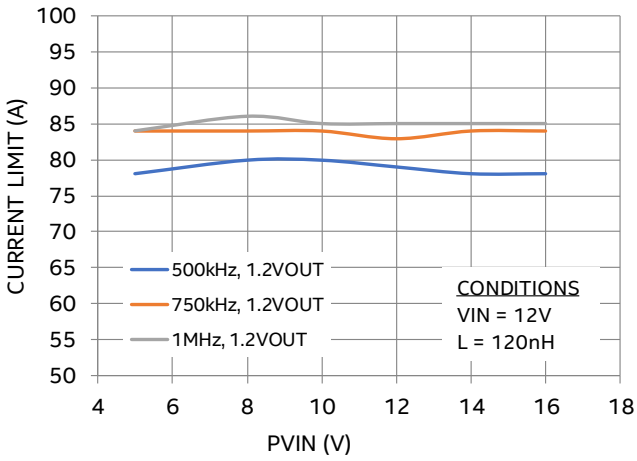
IMON vs. VCC



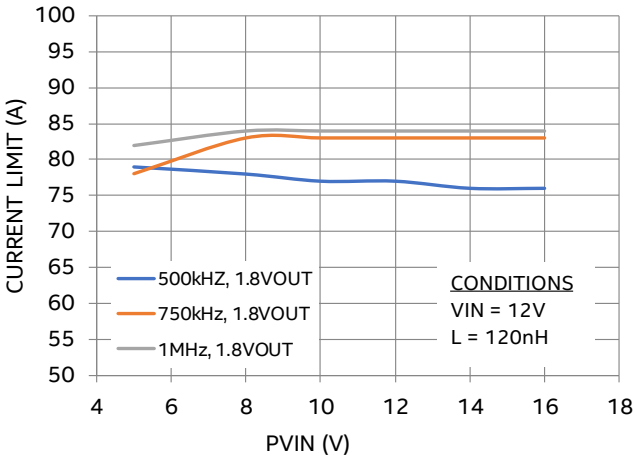
IMON vs PVIN



DC Current Limit vs. Input Voltage

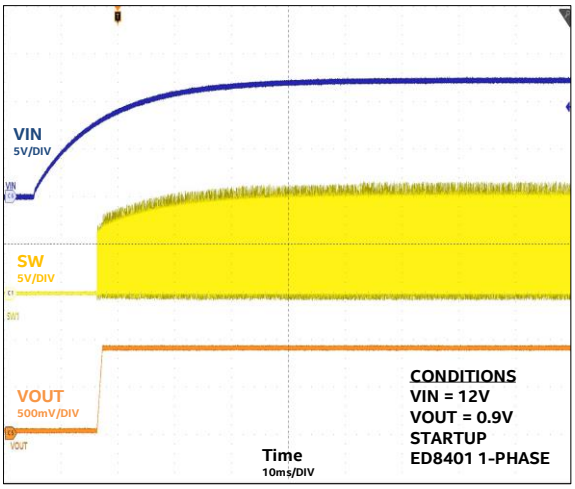


DC Current Limit vs. Input Voltage

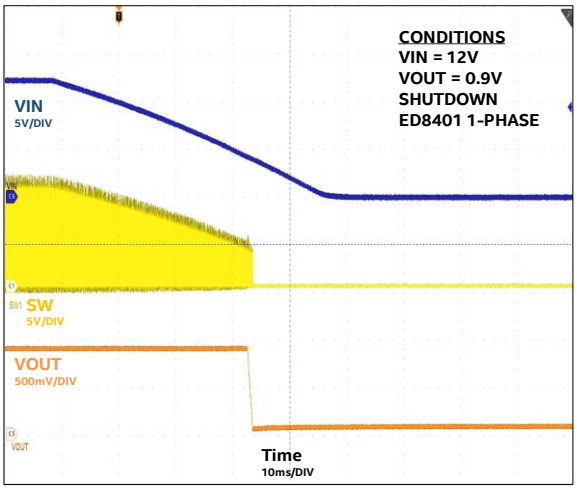


TYPICAL PERFORMANCE CHARACTERISTICS

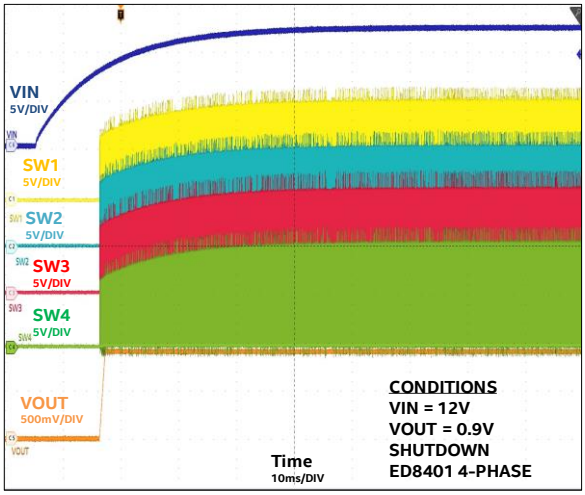
Startup with VIN at No Load (1-Phase)



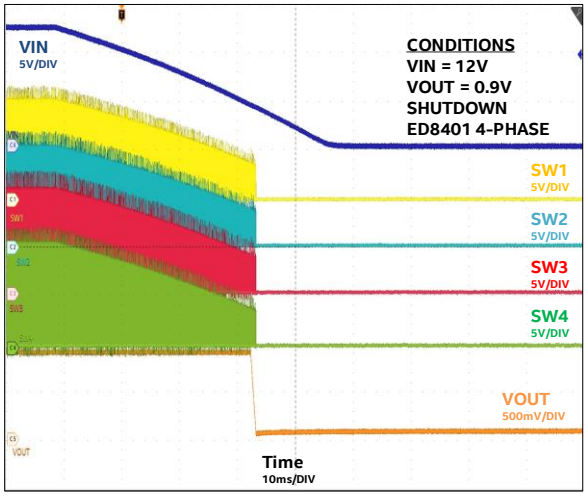
Shutdown with VIN at No Load (1-Phase)



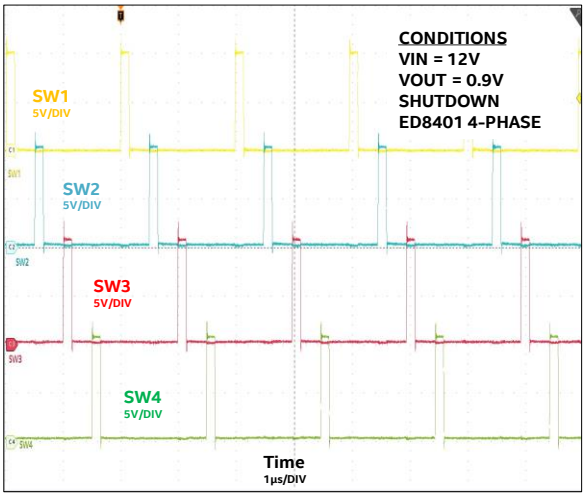
Startup with VIN at No Load (4-Phase)



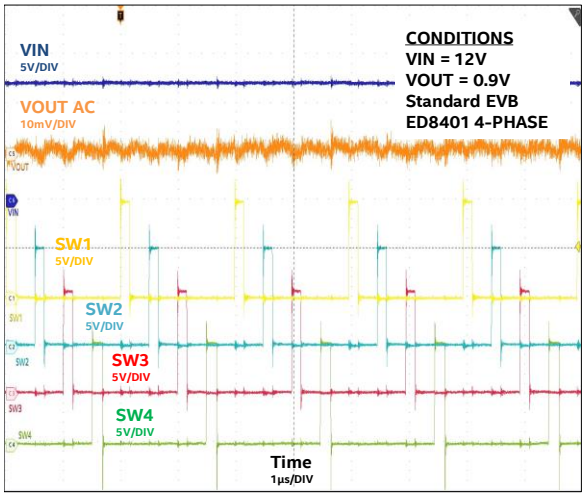
Shutdown with VIN at No Load (4-Phase)



Switching Waveform at No Load (4-Phase)

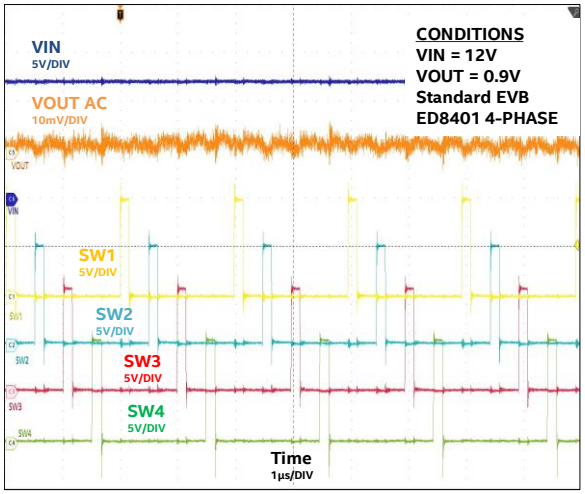


Output Ripple at No Load (4-Phase)

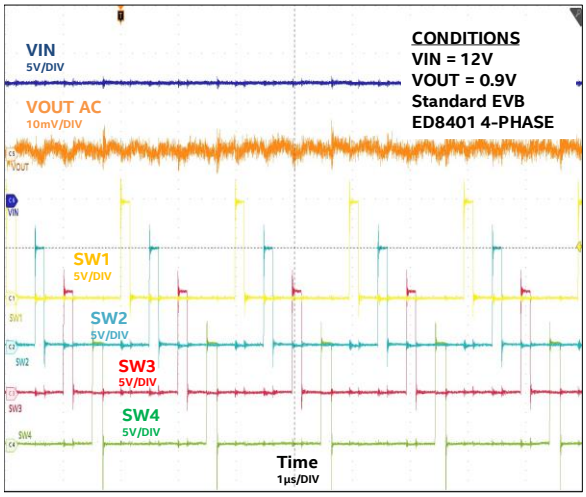


TYPICAL PERFORMANCE CHARACTERISTICS

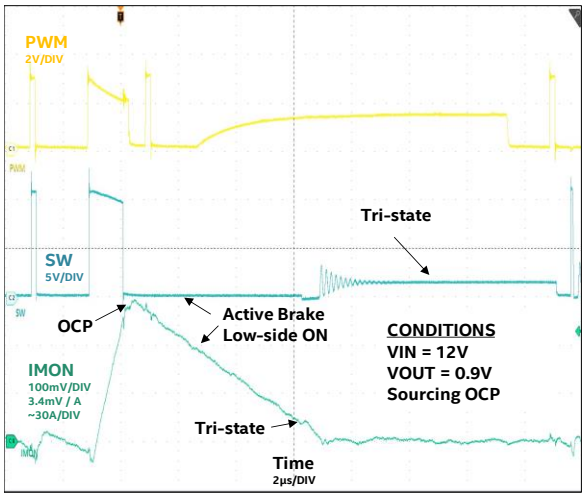
Output Ripple at 100A (4-Phase)



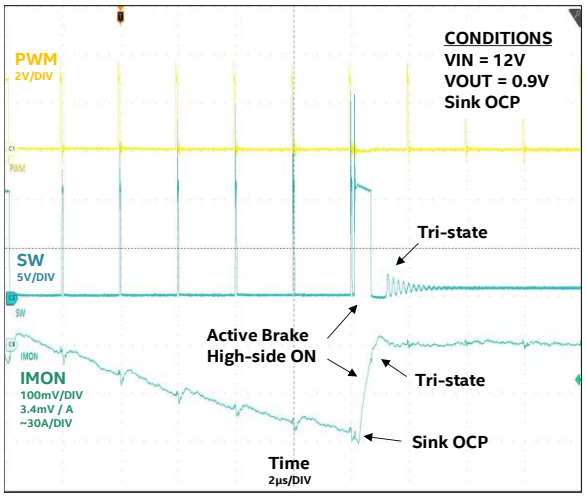
Output Ripple at 160A (4-Phase)



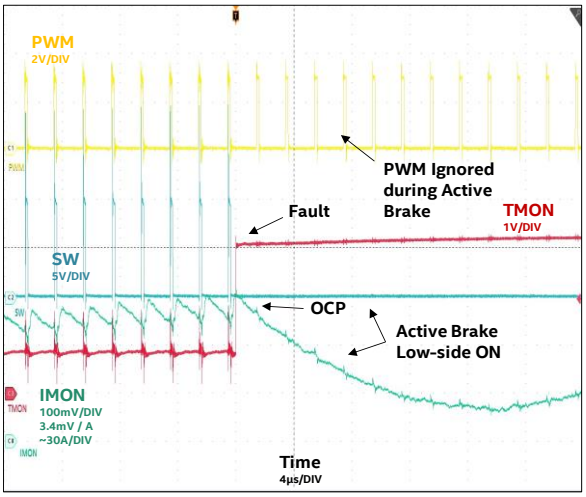
Sourcing OCP with Active Brake



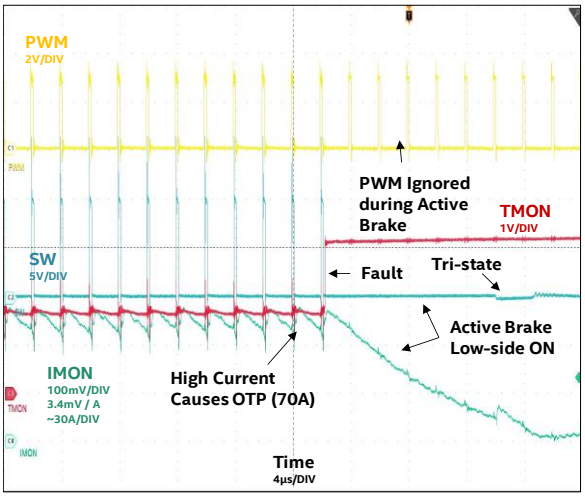
Sinking OCP with Active Brake



TMON/FLT on OCP and Active Brake



OTP Protection with Active Brake (70A)



FUNCTIONAL BLOCK DIAGRAM

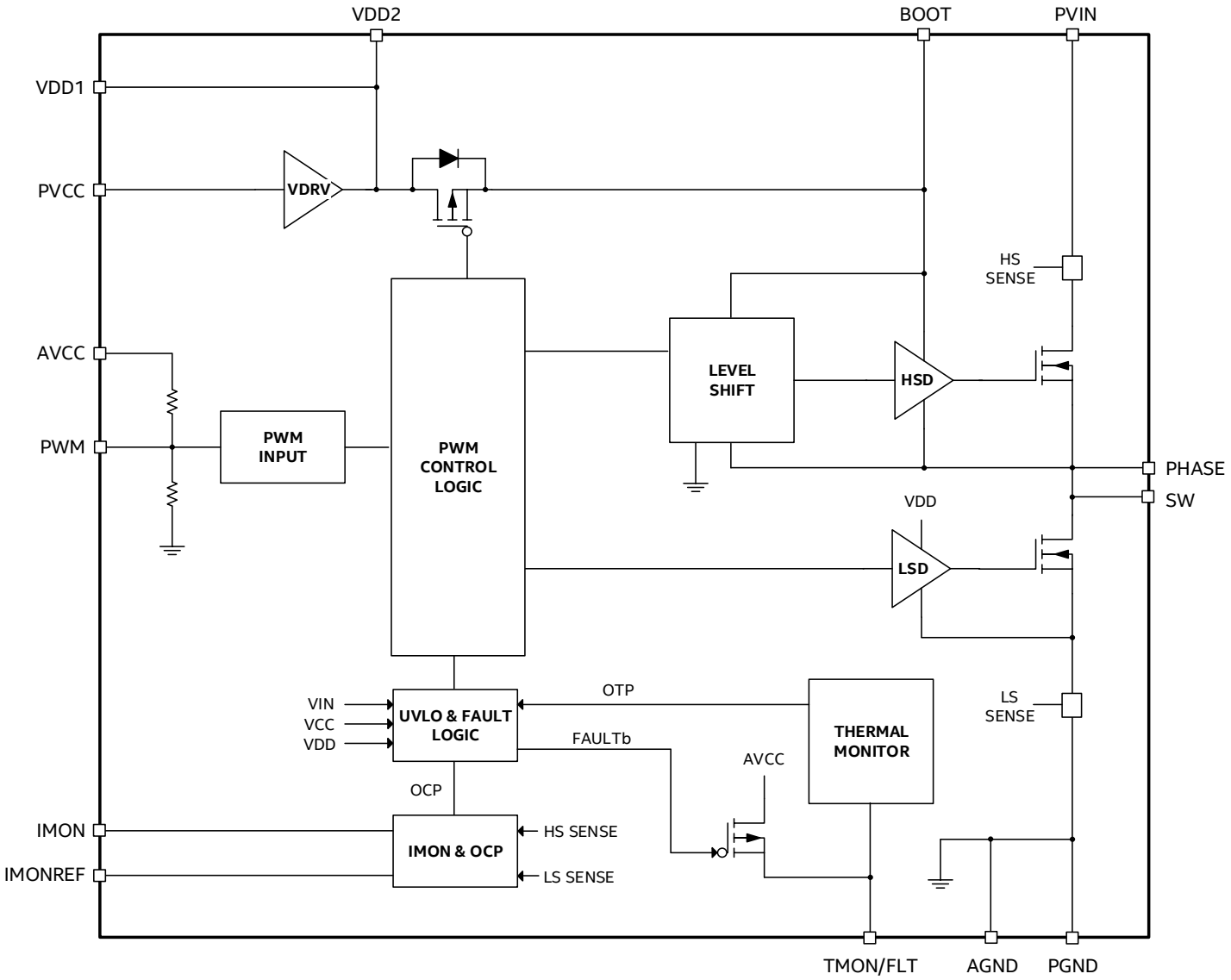


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Power Stage Overview

The ET6160LI is a 70A capable power stage intended to be used with a Digital Controller in a single-phase or multi-phase buck converter configuration. It requires two input voltages (PVIN and PVCC/AVCC). The operating input voltage range is 4.5V to 16V for PVIN and 3.0V to 3.6V for the VCC pins. The ET6160LI consists of driver circuitry, control interface, protection circuitry, and n-channel lateral DMOS power switches. By combining all circuit blocks into a single die, the ET6160LI is optimized for switching frequencies up to 1MHz and can offer accurate telemetry while also providing high burst current capability. The ET6160LI has its own internal protection and features that are independent of a Digital Controller.

Protection and Features

The ET6160LI comes with its own protection and features that is independent of the external Digital Controller to ensure protection from catastrophic system events while providing accurate telemetry. The internal protection thresholds are set higher than the digital controller thresholds to prevent conflict and will become active in the event that the digital multi-phase controller suddenly loses power.

Operational Features:

- IMON inductor current monitor and reporting
- TMON/FLT temperature monitor and reporting
- TMON/FLT power stage not ready indicator

Protection Features:

- Over-current and short protection (OCP) with Active Brake soft turn-off
- Over-temperature (OTP) with hysteresis to prevent over temperature stress
- PVIN/AVCC Under-voltage lockout (UVLO) protection with hysteresis
- PVIN Over-voltage lockout protection (OVLO) to prevent over-voltage stress
- MOSFET driver voltage (VDD) UVLO to prevent insufficient gate drive

Current Monitor (IMON)

The ET6160LI drives a current proportional to the output current on the IMON pin at a ratio equal to 1µA/A. This proportional current consists of the sum of both the high-side and low-side MOSFET current. A resistor between IMON and the IMON reference bias voltage sets the voltage gain at the controller's current sense input. A filter between IMON and IMON reference can be used to reject unwanted signal components.

For example, if the output current is 1A, then the output of IMON is 1µA and if the R_{IMON} resistor value is 2.7kΩ, then the voltage across IMON and IMONREF can be calculated as:

V_{IMON} = 1µA * 2.7kΩ = 2.7mV

The voltage gain for R_{IMON} = 2.7kΩ is 1mV/A. At 50A output current, the expected voltage between IMON and IMONREF is 135mV. Since the IMON current is bi-directional, the voltage can be positive or negative depending if the buck is sourcing or sinking current, respectively. Note that R_{IMON} and the IMON voltage gain ratio on the Digital Controller should be adjusted to accurately represent the output current and this preference is defined by the user. Most Digital Controllers have a voltage limit on the current sense input, so be sure to choose a R_{IMON} value that does not cause over-voltage and saturate the sensing input.

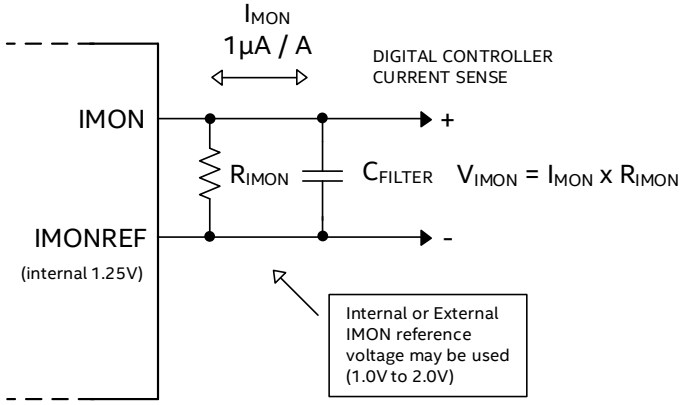


Figure 5: IMON Circuit Diagram

Temperature Monitor (TMON/FLT)

The TMON/FLT tracks the internal junction temperature as a voltage. This offers temperature sense telemetry to the Digital Controller. Under normal operation when VCC is powered, the internal thermal circuitry outputs a voltage relative to ground on TMON/FLT with a gain ratio of 8mV/°C. The ET6160LI provides temperature information over a wide range for accurate reporting in any system environment. Multiple TMON/FLT signals from other ET6160LI power stages can be combined together and the highest voltage has priority. Note that the ED8401 Digital Controller has independent temperature sense inputs for each of the 4 phases and thus the TMON/FLT signals do not need to be combined. Figure 6 shows the curve of the TMON/FLT voltage versus junction temperature. The TMON/FLT voltage can be calculated based on junction temperature, as shown.

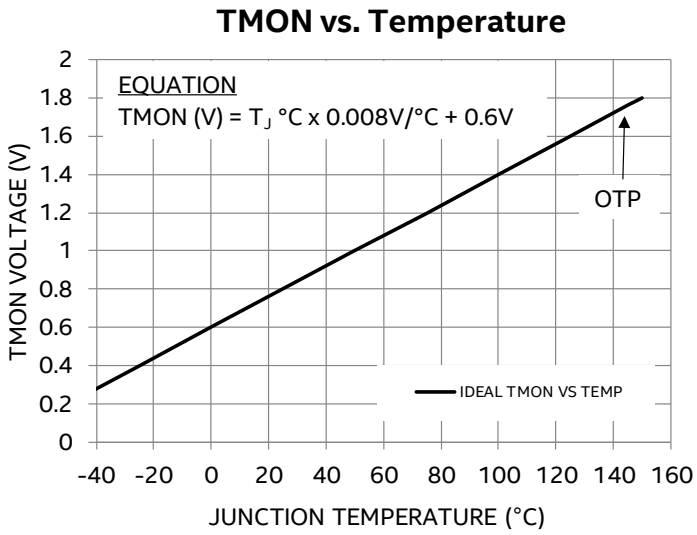


Figure 6: Ideal TMON vs. Temperature Graph

Power Stage Not Ready

The TMON/FLT also acts as a fault indicator. When a protection circuit is triggered (OCP, TSD, UVLO, OVLO), the TMON/FLT pin will be pulled high to VCC internally for the duration of 1ms. If the fault continues to be present after 1ms, then this duration is repeated. Once the 1ms timer is over and the fault is removed, the device will resume normal operation. When multiple TMON/FLT pins are connected together for multi-phase operation, the fault mechanism is OR'ed and any of the power stages can trigger a fault for the Digital Controller. The ET6160LI has a built-in mechanism called Active Brake to protect itself during a fault. The table below summarizes the protection behavior of the ET6160LI.

Table 1: TMON/FLT Fault Mechanism Table

Condition	Fault Response
PWM Active –> Tri-state	Active Brake then Tri-state
OCP	Active Brake then Tri-state
OTP	Active Brake then Tri-state
PVIN UVLO	Active Brake then Tri-state
PVIN OVLO	Active Brake then Tri-state
AVCC UVLO	Tri-state Immediately
VDD1/2 UVLO	Tri-state Immediately

Over Current Protection with Active Brake (OCP)

The ET6160LI also has an internal OCP circuit with Active Brake to safely handle faults and is independent of the Digital Controller to provide further protection. The Active Brake mechanism will ramp the inductor current down to around 10A before tri-staing. For example, if the output current is detected to be greater than the internal OCP (sourcing or sinking) threshold, a fault is triggered and the TMON/FLT is pulled to VCC. Due to the destructive nature of operating at high current, the ET6160LI's Active Brake mechanism is designed to ramp the inductor current magnitude down to 10A whether it is sourcing or sinking. When the ET6160LI is in fault mode, it will ignore the PWM signal from the controller to protect itself. If the power stage is sourcing current and faults, the top-side MOSFET is immediately turned off and the low-side MOSFET turns on until the inductor current ramps down to 10A. Once the inductor current magnitude is below 10A, the SW pin tri-states and both top and bottom MOSFETs are off. If the power stage is sinking current and faults, then the top-side MOSFET will turn on until the inductor current ramps down to 10A. Once the inductor current magnitude is below 10A, the SW pin tri-states. This Active Brake mechanism protects the power stage from uncontrolled current and voltage spikes in a catastrophic event and provides extra protection behind the Digital Controller's own protection settings.

Over Temperature Protection (OTP)

The ET6160LI has an internal OTP that is independent of the Digital Controller. As die temperature increases during operation, the TMON/FLT voltage rises. Once the junction temperature of the ET6160LI exceeds 145°C (TMON/FLT ≈ 1.76V), the device will enter a fault. In fault, TMON/FLT voltage will be pulled high to VCC and the device will begin Active Brake to ramp the inductor current down to a magnitude of 10A before tri-stating and turning off both top-side and bottom-side MOSFETs. When the ET6160LI is in its internal fault mode, it will ignore the PWM signal from the controller to protect itself. The device will remain in tri-state until the junction temperature falls by 25°C. Once the temperature fall below 120°C, the device will resume normal operation and accept PWM signals.

Input Protection (UVLO/OVLO)

The ET6160LI monitors the input voltage on the PVIN and AVCC pins continuously to ensure voltage levels are within operating limits. If the PVIN input voltage is below the UVLO threshold, then the device will be in fault mode and the TMON/FLT will be pulled high to VCC. The device will fault and Active Brake until the inductor currents magnitude is below 10A and then tri-state (ignoring the PWM signal). If the VCC input voltage is below the UVLO threshold, the device will immediately tri-state and turn off both top-side and bottom-side MOSFETs. There is an Over-Voltage Lock-out (OVLO) on the PVIN pin to prevent switching at high input voltage levels. If the PVIN input voltage exceeds the over-voltage protection threshold a fault will occur and the TMON/FLT will be pulled high to VCC. In this fault, the device will tri-state and turn off both top-side and bottom-side MOSFETs. See specification table for PVIN UVLO Fault, PVIN OVLO Fault and related hysteresis values.

MOSFET Gate-Drive Protection (UVLO)

The ET6160LI monitors its own internal gate-drive voltage (VDD1 and VDD2). Under normal operation, the VDD voltages should be at 1.8V. This voltage is internally regulated and should not be tampered with externally. In the event that the VDD voltage drops below its UVLO threshold, the device will tri-state, turning off both the top-side and bottom-side MOSFETs. The UVLO protection circuit is designed with anti-glitch filtering and will ignore noise spikes that do not degrade the drive capability. This ensures the ET6160LI gate drive is always sufficient during normal operation.

APPLICATION INFORMATION

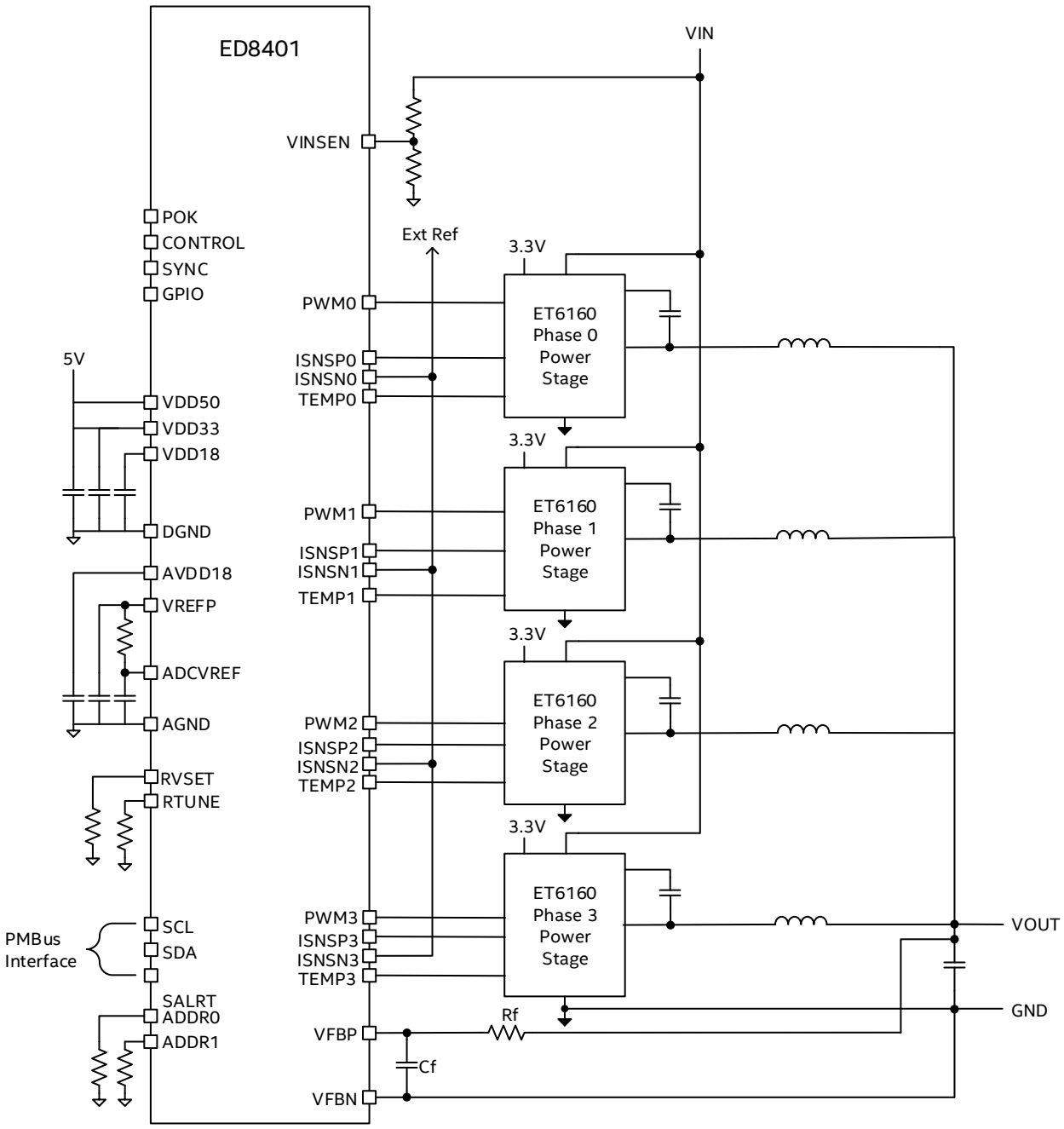


Figure 7: 4-Phase Buck Converter Topology

Multi-Phase Converter Overview

The ET6160LI is a 70A capable power stage intended to be used with a Digital Controller in a single-phase or multi-phase buck converter configuration. It is designed and optimized to interface with Intel® Enpirion® Digital Controllers such as the 4-Phase ED8401. Figure 7 shows a typical 4-phase buck topology capable of delivering peak currents up to 280A. The ED8401 Digital Controller can be configured for 1 to 4 phases and controls the ET6160LI through its PWM0 to PWM3 signals. It has individual input current sense using the IMON of the ET6160LI power stages. It also has independent temperature monitor and can utilize the TMON to report each

of the power stage's temperatures invidually. In order to operate, the ED8401 needs a 5V input voltage while the ET6160LI needs a 3.3V, 12V and a PWM signal. Combining the ET6160LI with the ED8401 controller allows the user to customize and design a multi-phase power solution for cores voltages with ease.

PWM Input

ET6160LI accepts PWM input from a Digital Controller such as the ED8401. When the PWM input goes high, the lower MOSFET switches off followed by the upper MOSFET turning on. This upper MOSFET remains on until PWM goes low or tri-state. When PWM goes low, the upper MOSFET turns off followed by the lower MOSFET turning on. The lower MOSFET remains on until PWM goes high or tri-state. When PWM goes tri-state the on-state MOSFET turns off after a detection period. In the event the PWM entering tri-state (such as during a fault) while the high side MOSFET is on, the high side will turn off and the low side remain on until the inductor current has fallen to within the Inductor current tri-state threshold (Active Brake). After this both MOSFETs remain off until PWM goes high or low. The detection period is the time required to be certain that PWM is dwelling in tri-state instead of passing through and in essence protects the device from switching intermittently due to noise.

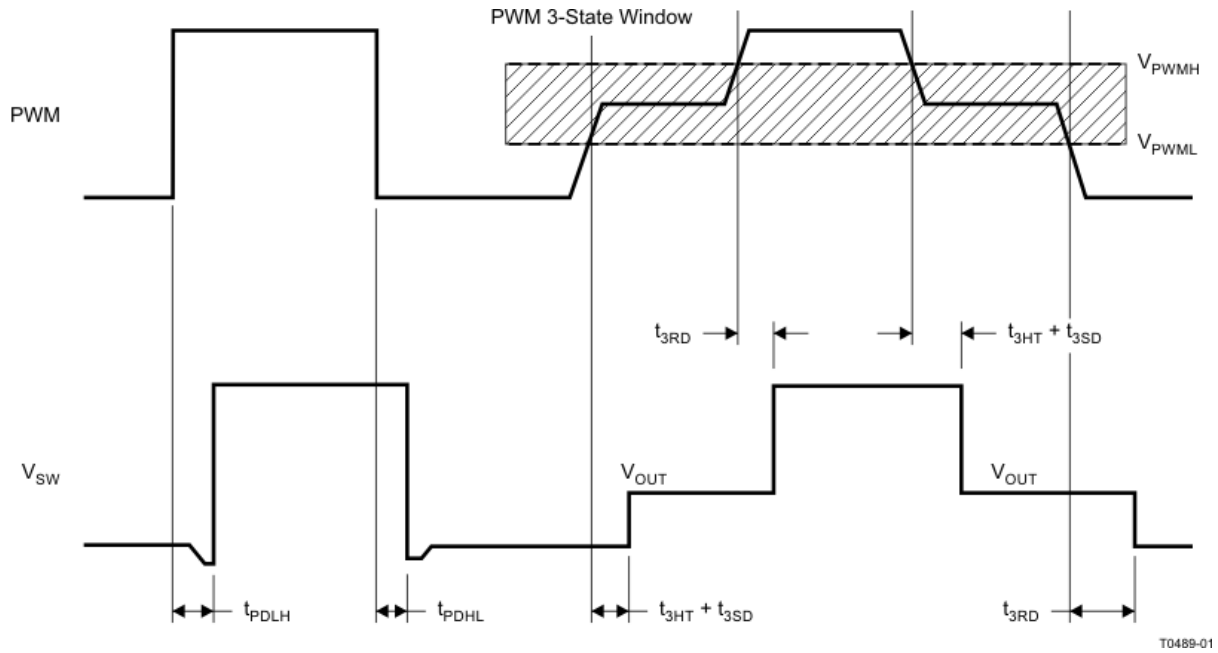


Figure 8: PWM Timing Diagram

Inductor Selection

The inductor is one of the most important passive elements in a buck regulator. The inductor can affect the efficiency, transient response, output ripple and over-all system level noise. In most power applications, choosing an inductor comes down to the size, inductance, DC resistance (DCR) and the cost of the inductor. These parameters need to be taken into consideration when selecting an inductor. Generally, the higher the inductance, the more windings are needed around a magnetic core and the larger the inductor. Higher inductance usually increases solution size. Applications with a space constraint may want to select smaller sized inductors; however, smaller sized inductors at the same inductance usually have higher DCR, which can lower the efficiency, so designing is often a trade-off between size and efficiency. Note that the inductor's peak-to-peak current is inversely proportional to the inductance as shown:

$$\Delta I = \frac{(Vin - Vout)D}{L \times f}$$

ΔI = Inductor's Peak-to-Peak Current

Vin = Input Voltage

Vout = Output Voltage

D = Duty Cycle = Vout/Vin

L = Inductance

f = Buck Regulator Switching Frequency

If the inductance is too low it will have a higher peak-to-peak current which may activate the peak detection current limit protection at a low output current level. When inductance is lower than recommended, the buck regulator may not be able to support its full load.

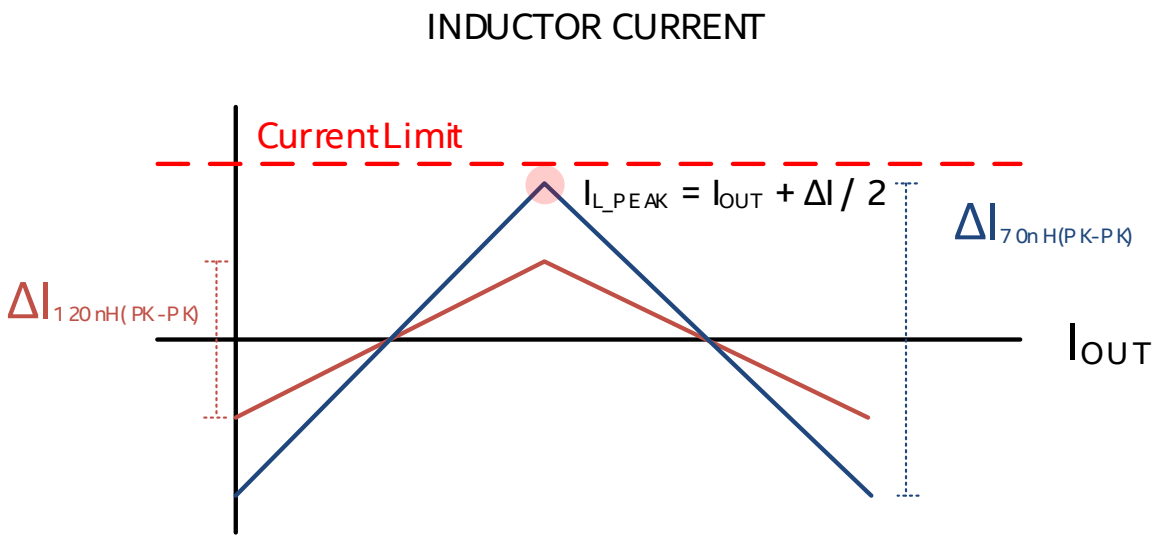


Figure 9: Inductor Peak-to-Peak Current

Since the ET6160LI is optimized for switching frequencies from 500kHz to 1MHz, it is designed to accommodate a inductance range from 70nH to 150nH. Do not use inductors with lower saturation current than the maximum output current needed in the application. When the inductor saturates, it loses inductance and this will increase its peak-to-peak current. This can sometimes cause false current limit triggers and shutdown the device. Always have sufficient margin. Figure 9 shows the difference in peak-to-peak current depending on the inductance (120nH versus 70nH). A lower than optimum inductance may also introduce peak currents that can increase the system level noise and should be avoided. See Table 2 for a list of recommended inductors.

Table 2: Recommended

DESCRIPTION	MFG	P/N
120nH, 0.145mΩ, 78A, 9.6mmx6.4mmx10.1mm	ITG	AH3740A-120K
120nH, 0.18mΩ, 70A, 10mmx7mmx8.3mm	TDK	VLBS1007083T-R12L
70nH, 0.145mΩ, 78A, 9.6mmx6.4mmx10.4mm	ITG	AH3740A-70K
70nH, 0.228mΩ, 60A, 11mmx7.65mmx7.2mm	Coilcraft	SLC1175-700ME

Power Stage Decoupling

The ET6160LI incorporates several internal voltage regulators to derive all required supply and bias voltages from the AVCC and PVCC supply voltages. Decoupling capacitors are required on the AVCC, PVCC, and both VDD1 and VDD2 pins. The specified minimum capacitance must consider temperature and voltage therefore a high-quality dielectric like X7S or X7R is recommended.

Table 3: Power Stage Decoupling Capacitors

Pin #	Pin Name	Value	Note
2	AVCC	2.2µF & 1µF	Required
3	PVCC	10µF & 2.2µF	Required
6	VDD1	22µF & 2.2µF	Required
31	VDD2	1nF	Required
32 & 33	PHASE to BOOT	2.2µF	Required

All decoupling capacitors from the power stage should be connected through a low impedance path to PGND. See Layout Recommendations for details.

Input Capacitor Selection

The input of synchronous buck regulators can be very noisy and should be decoupled properly in order to ensure stable operation. In addition, input parasitic line inductance can attribute to higher input voltage ripple. The ET6160LI input capacitance recommendation is 4 x 100µF/20V, 4x 10µF/20V and a 1µF/20V as close to the PVIN pins as possible. Note that in a multi-phase application, the Digital Controller will switch each ET6160LI out of phase and input capacitance is shared; therefore, the amount of input capacitance needed per phase is reduced. As the distance of the input power source to the input of the ET6160LI is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Low-ESR ceramic capacitors should be used. The dielectric must be X5R/X7R or equivalent and the size should be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling.

Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Table 4: Recommended Input Capacitors

DESCRIPTION	MFG	P/N
1µF Ceramic, X5R, 10%, 25V, 0402	Taiyo Yuden	TMK105BJ105KV-F
	Murata	GRM155R61E105KA12
10µF Ceramic, X5R, 10%, 25V, 0805	Taiyo Yuden	TMK212BBJ106KG-T
	Murata	GRM21BR61C106KE15
100µF Poscap, 20V, 20%	Panasonic	20TQC100MYF

Output Capacitor Selection

The output ripple of a synchronous buck converter can be attributed to its inductance, switching frequency and output decoupling. The ET6160LI output capacitance recommendation is 4 x 470µF/4V, 4 x 22µF/4V and a 10µF/4V output capacitor. Low ESR ceramic capacitors should be used. The dielectric must be X5R/X7R or equivalent and the size should be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Tantalum bulk capacitors may be used in conjunction to increase total output capacitance but should not be used solely as a replacement for the ceramic capacitors. Do not use electrolytic capacitors on the output due to their high ESR. Total output capacitance depends on the Digital Controller as it may determine device stability and transient response. It is recommended to follow the Digital Controller's own output decoupling recommendations for stability and loop control.

Table 5: Recommended Output Capacitors

DESCRIPTION	MFG	P/N
22µF Ceramic, X5R, 20%, 10V, 0805	Murata	RM21BR61A226ME51
10µF Ceramic, X5R, 20%, 10V, 0603	Murata	GRM188R61A106KE69
100µF Ceramic, 6.3V, X5R, 1206	Kemet	C1206C107M9PACTU
470µF SP-CAP, 2.5V, ESR 3mΩ	Panasonic	EEFGX0E471R

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance (ESR) and effective series inductance (ESL):

$$Z = ESR + ESL$$

The resonant frequency of a ceramic capacitor is inversely proportional to the capacitance. Lower capacitance corresponds to higher resonant frequency. When two capacitors are placed in parallel, the benefit of both are combined. It is beneficial to decouple the output with capacitors of various capacitance and size. Placing them all in parallel reduces the impedance and will hence result in lower output ripple.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

THERMAL CONSIDERATIONS

Thermal considerations are important elements of power supply design. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be taken into account. The Intel Enpirion packaging technology helps alleviate some of those concerns.

The ET6160LI Smart Power Stage is packaged in a 5mm x 6mm x 0.7mm 39-pin LGA package. The LGA package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 145°C.

The following example and calculations illustrate the thermal performance of the ET6160LI with the following parameters:

V_{IN} = 12V

V_{OUT} = 0.85V

I_{OUT} = 50A

First, calculate the output power.

$P_{OUT} = V_{OUT} \times I_{OUT} = 0.85V \times 50A = 42.5W$

Next, determine the input power based on the efficiency (η) shown in Figure 9.

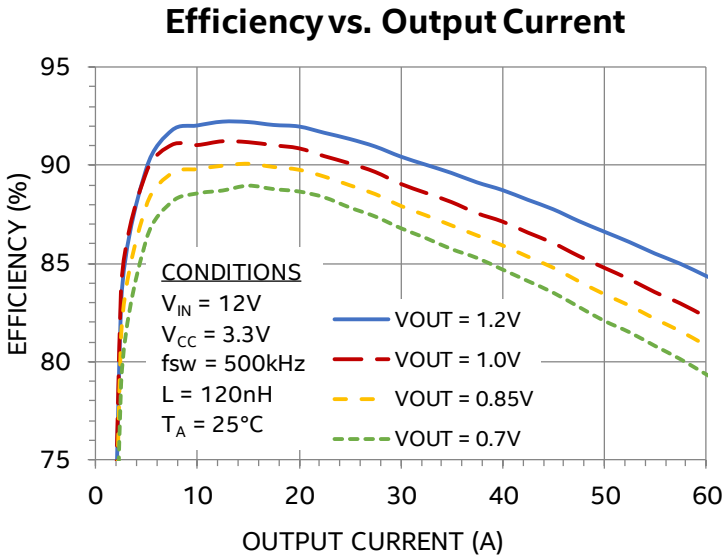


Figure 9: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 0.85V at 50A, η ≈ 83.5%

$\eta = P_{OUT} / P_{IN}$ = 83.5% = 0.835

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 42.5W / 0.835 \approx 50.9W$

The total power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_{TOTAL} = P_{IN} – P_{OUT}$

= 50.9W – 42.5W ≈ 8.4W

The total power dissipation includes the loss in the ET6160LI plus the loss in the inductor, but since we are not interested in the inductor's temperature change, we will subtract that to get the ET6160LI's power loss.

$P_{INDUCTOR} = I_{OUT}^2$ x DCR = 50^2 x 0.000145 (0.145mΩ is the DCR of the inductor used in this example)

$P_{INDUCTOR}$ = 50^2 x 0.000145 = 0.3625W (assume AC losses in the inductor are negligible at 500kHz)

The power dissipation into the ET6160LI package is equal to the total power dissipation minus the inductor's power loss.

$P_{ET6160} = P_{TOTAL} - P_{INDUCTOR}$ = 8.4W – 0.3625W = 8.04W

With the power dissipation of the ET6160LI known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The ET6160LI has a θ_{JA} value of 10°C/W without airflow.

Determine the change in temperature (ΔT) based on P_{ET6160} and θ_{JA}.

$\Delta T = P_{ET6160} \times \theta_{JA}$

$\Delta T \approx 8.04W \times 10°C/W \approx 80.4°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 80.4°C \approx 105.4°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} – P_{ET6160} \times \theta_{JA}$

≈ 125°C – 80.4°C ≈ 44.6°C

The maximum ambient temperature the device can reach is 44.6°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION CIRCUITS

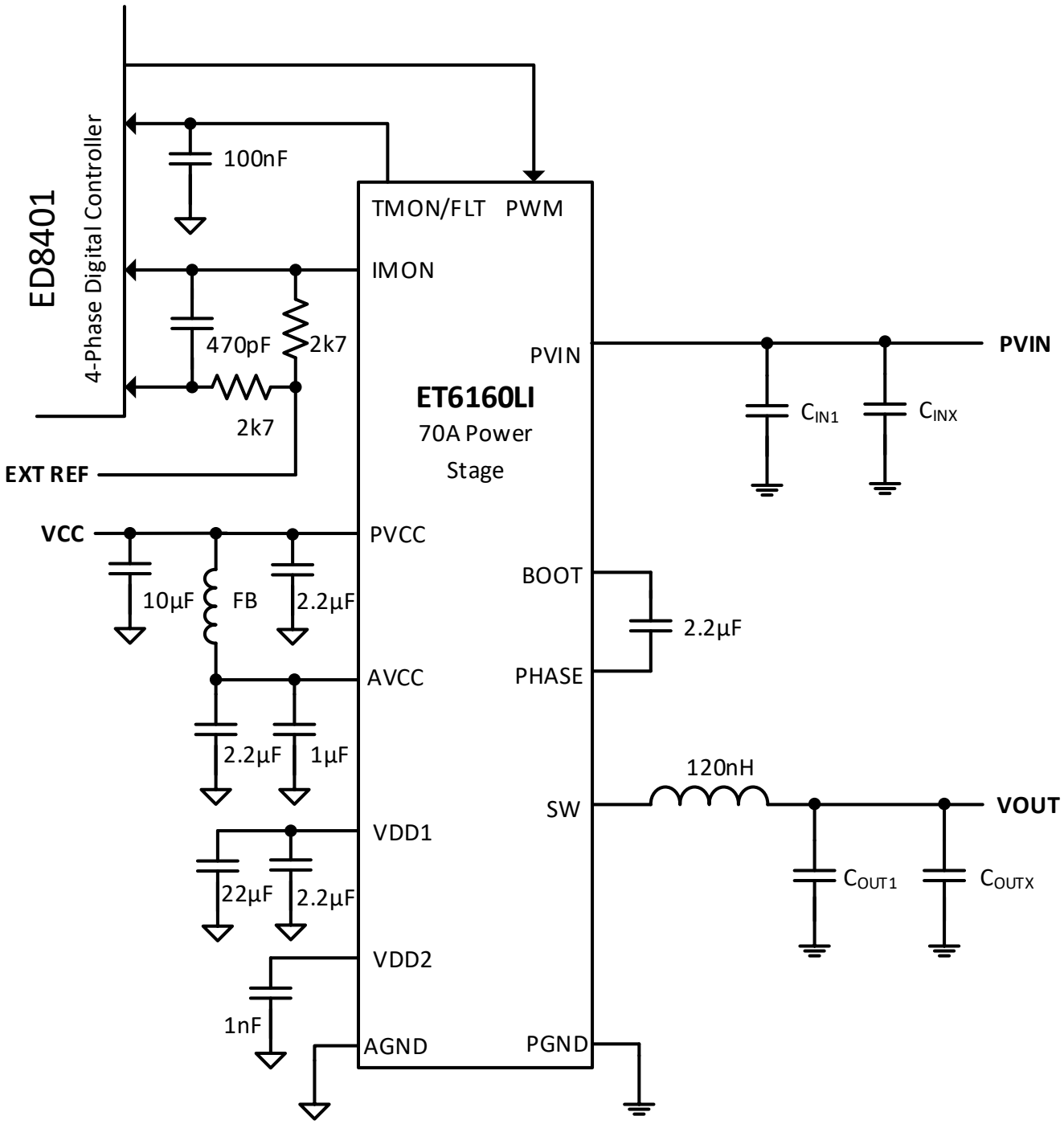


Figure 11: Typical Application Circuit for V_{OUT} = 0.85V

LAYOUT RECOMMENDATIONS

Figure 12 shows critical components and top layer traces of ET6160LI layout. Visit the Enpirion Power Solutions website at www.intel.com/power for more information regarding layout. Please refer to Figure 12 while reading the layout recommendations in this section.

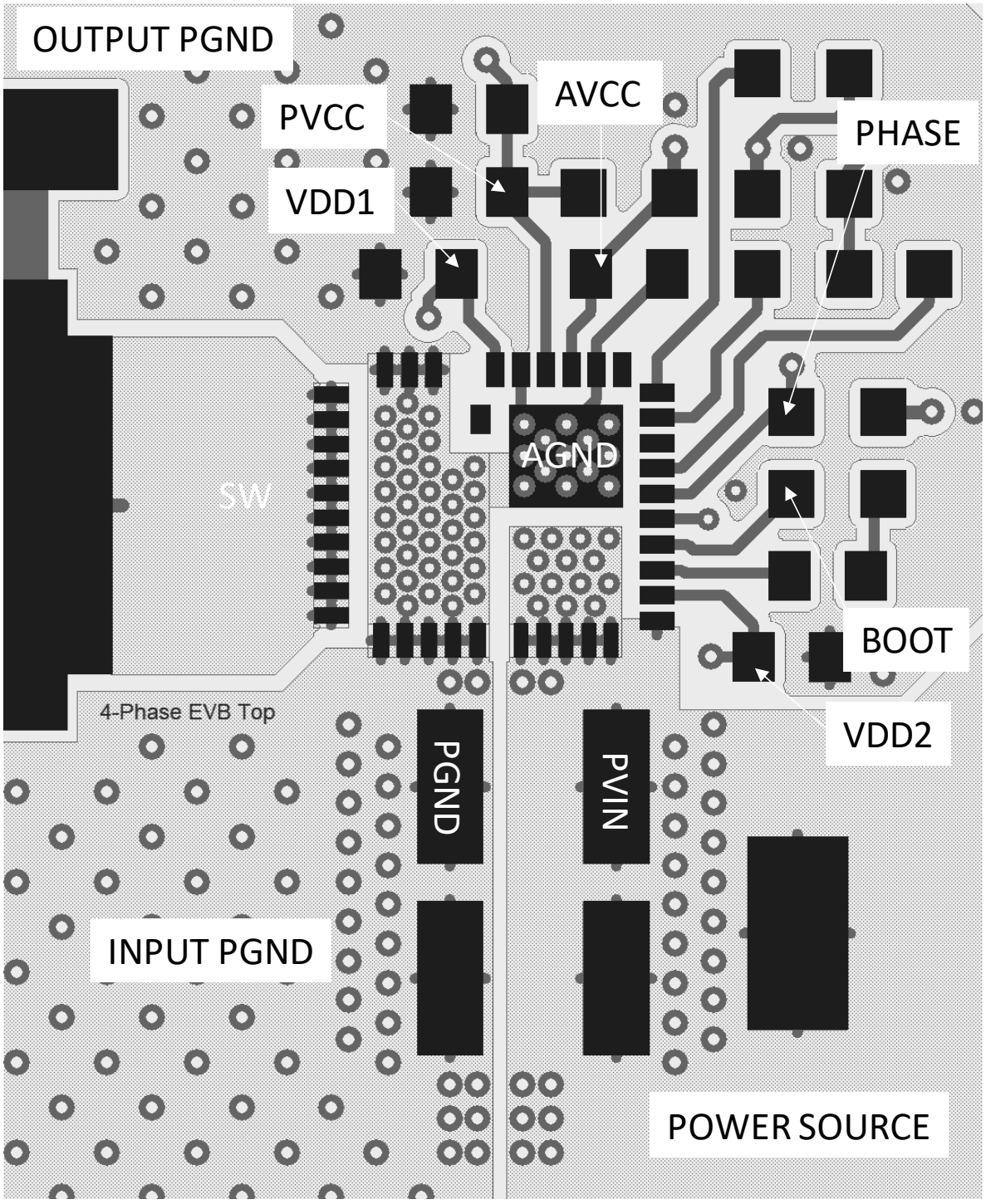


Figure 12: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the ET6160LI package as possible. They should be connected to the device with very short and wide

traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Voltage and GND traces between the capacitors and the ET6160LI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors. It is good practice to separate the input ground from the output ground on the top layer to prevent the input ripple from coupling directly into the output capacitors. Placing capacitors on the bottom side will work, but not as effective at reducing the input or output ripple due to the additional series inductance caused by the vias.

Recommendation 2: The system ground plane should be on the 2nd layer (below the surface layer). This ground plane should be continuous and un-interrupted. During PCB stacking, it is good practice to have ground separation between the planes to reduce the coupling effects of signals from layer to layer. For example, the PCB layers should be stacked with Signal (top), Ground (2nd layer), Power (layer 3), Ground (layer 4), Signal (layer 5) and so on. By inserting a ground plane between each signal or power plane, the effects of signals coupling into each other are reduce significantly.

Recommendation 3: The large PGND and AGND thermal pad underneath the device must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1-oz. copper plating on the inside wall, making the finished hole size around 0.2mm to 0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the ET6160LI to the board. Refer to Figure 12 for illustration.

Recommendation 4: The PVCC input capacitors should be rotated in such a way that its ground is on the output ground section. A ferrite bead is recommended between PVCC and AVCC to reduce high frequency spikes from the PVCC into AVCC. PVCC provides power for the drivers while AVCC provides power for the internal control logic. Follow the layout and decoupling scheme as shown in Figure 12.

Recommendation 5: The VDD1 decoupling capacitors should be rotated so that their ground is on the output ground side, as shown in Figure 12. VDD2 is on the other side of the package and cannot be grounded near the output ground section; however, do not connect the VDD2 decoupling capacitor's ground to the input ground to prevent input noise from coupling into the driver supply of the Power Stage. It is best practice to connect all VDD1/2 grounds in the output ground section.

Recommendation 6: The output inductor should be connected to the SW pins with a thick and wide trace, as shown in Figure 12. All output capacitors following the inductor should have their ground connected on the output ground side. Doing so ensures that the input and output ground of the buck regulator are separated on the top layer and noise coupling is reduced. Output voltage remote sensing done by the Digital Controller should be connected to a capacitor near the load side. Keep the two sense traces impedance matched and as far away from noisy signals as possible.

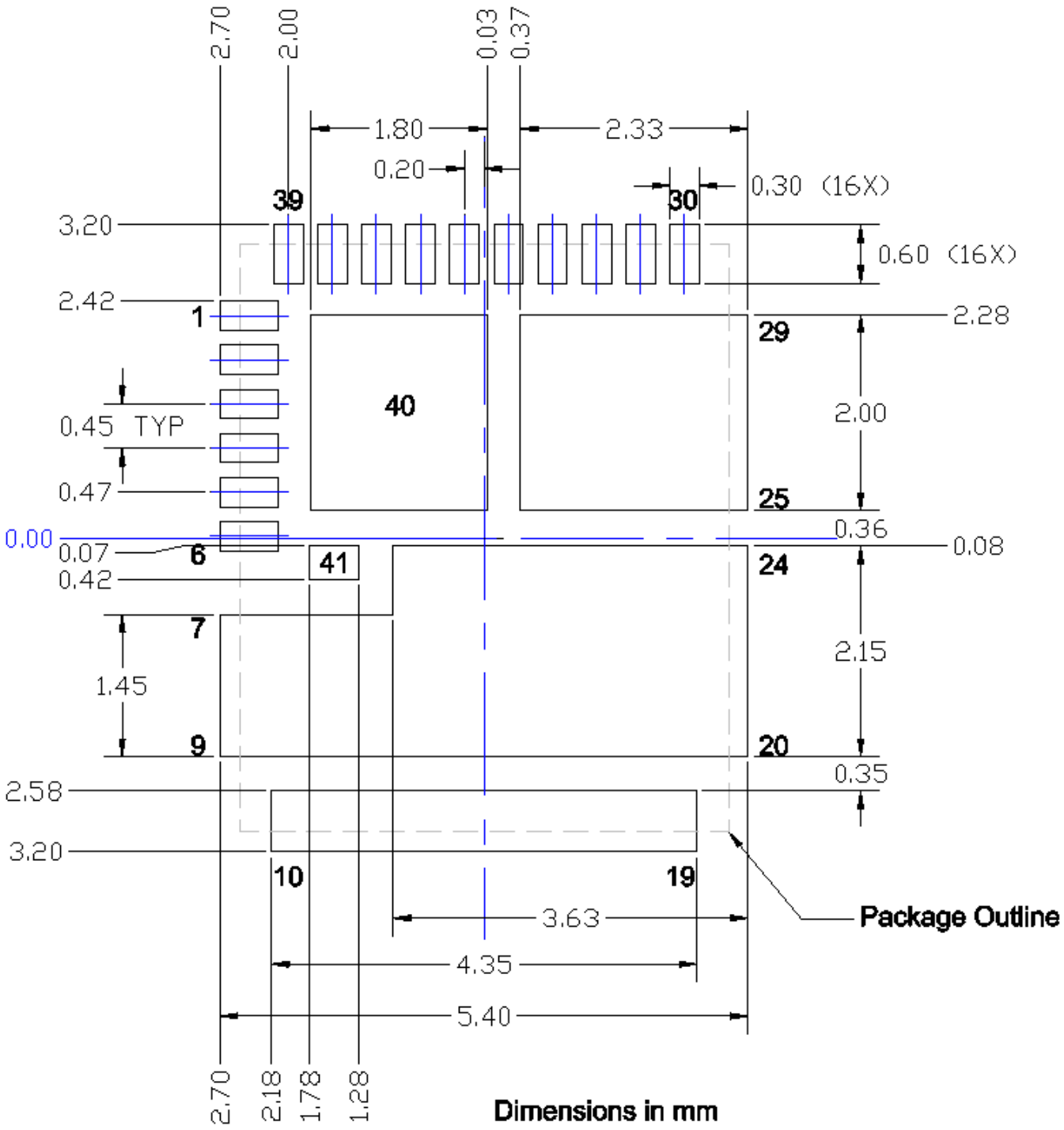


Figure 13: Landing Pattern Recommendation (Top View)

The landed pad dimensions shown in Figure 13 are recommended based on Enpirion power product manufacturing specifications.

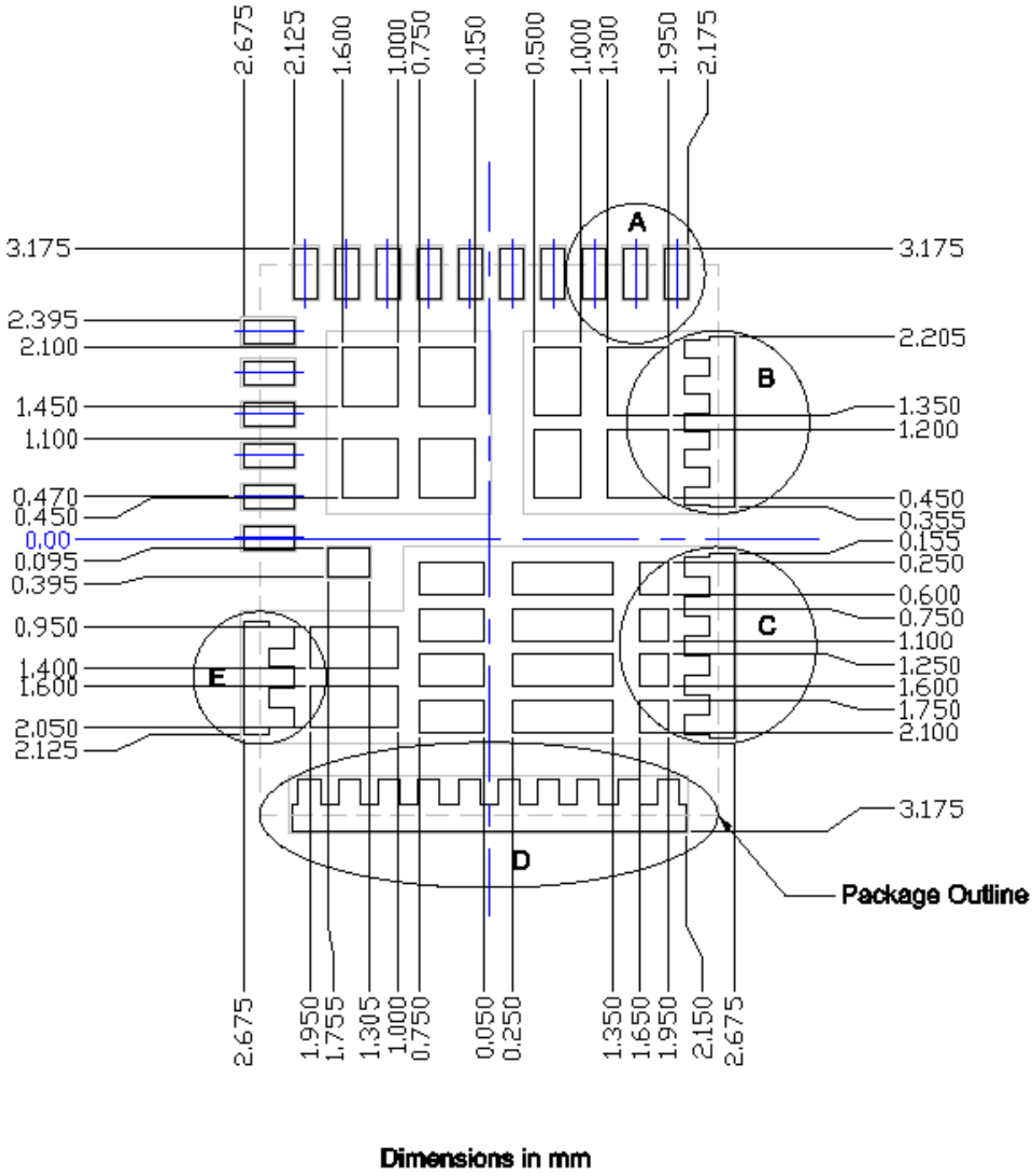


Figure 14: Solder Stencil Recommendation (Top View)

The solder stencil aperture for the pads below the device (shown in Figure 14) is recommended based on Enpirion power product manufacturing specifications.

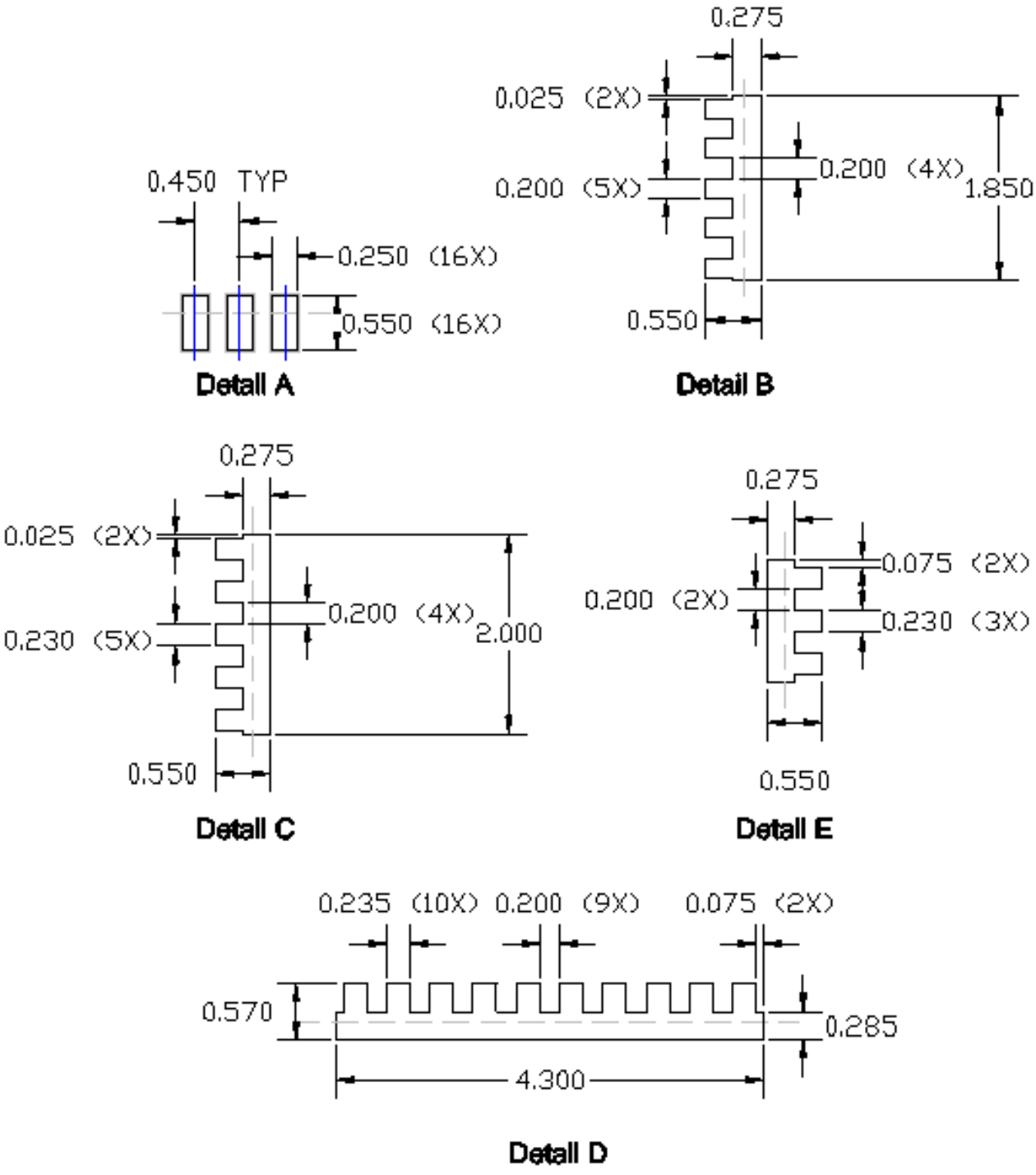


Figure 15: Solder Mask Dimensions (Top View)

PACKAGE DIMENSIONS

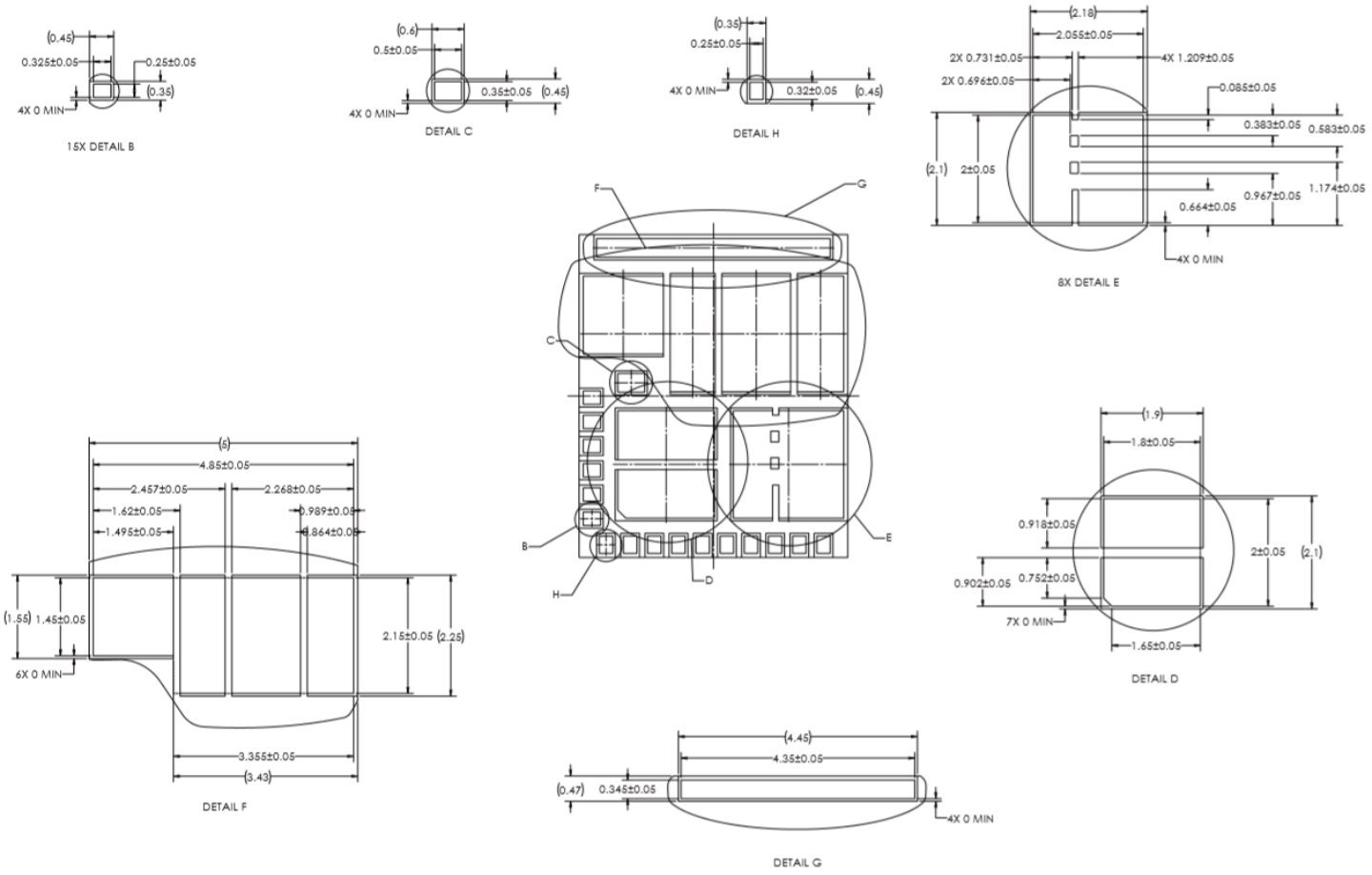


Figure 16: ET6160LI Package Dimensions (Bottom View)

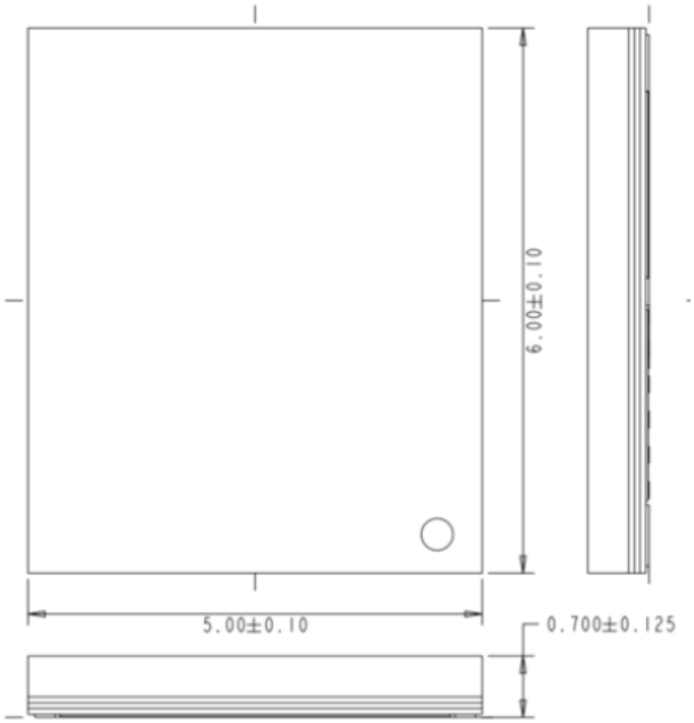


Figure 17: ET6160LI Package Dimensions

Packing and Marking Information:

https://www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
A	April, 2020	Initial Released Datasheet

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