

The Altera® Enpirion® ES1010SI is a fully featured hot-swap power controller that targets +12V applications. The ES1010SI has an integrated charge pump, which can generate a higher (6.5V) gate drive to improve efficiency.

This IC features programmable overcurrent (OC) detection, current regulation (CR) with time delay to latch-off and soft-start.

The current regulation level is set by 2 external resistors; R_{ISET} sets the CR V_{th} and the other is a low ohmic sense resistor across, which the CR V_{th} is developed. The CR duration is set by an external capacitor on the CLTIM pin, which is charged with a 20 μ A current once the CR V_{th} level is reached. The IC then quickly pulls down the GATE output latching off the pass FET.

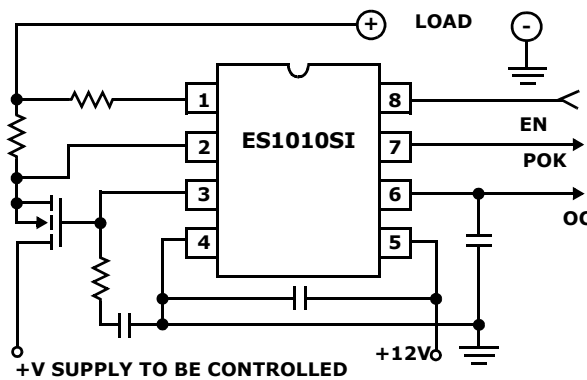
Features

- Hot-swap Single Power Distribution Control for +12V
- Overcurrent Fault Isolation
- Programmable Current Regulation Level
- Programmable Current Regulation Time to Latch-Off
- Rail-to-Rail Common Mode Input Voltage Range
- Enhanced Internal Charge Pump Drives N-Channel MOSFET gate to 6.5V above IC bias.
- Undervoltage and Overcurrent Latch Indicators
- Adjustable Turn-On Ramp
- Protection During Turn-On
- Two Levels of Overcurrent Detection Provide Fast Response to Varying Fault Conditions
- 1 μ s Response Time to Dead Short
- Pb-Free (RoHS Compliant)

Applications

- FPGA, DSP, and ASIC power protection
- Power Distribution Control
- Hot Plug Components and Circuitry

Application Circuits - High Side Controller



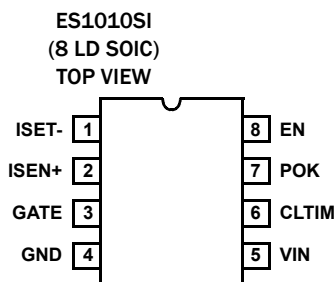
Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ES1010SI	1010	-40 to +85	8 Ld SOIC	M8.15
EVB-ES1010SI	Evaluation Platform			

NOTES:

- These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020..

Pin Configuration



Pin Descriptions

PIN NO.	SYMBOL	FUNCTION	DESCRIPTION
1	ISET-	Current Set	Connect to the low side of the current sense resistor through the current limiting set resistor. This pin functions as the current limit programming pin.
2	ISEN+	Current Sense	Connect to the more positive end of sense resistor to measure the voltage drop across this resistor.
3	GATE	External FET Gate Drive Pin	Connect to the gate of the external N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to $V_{IN} + 6.5V$ by an $14\mu A$ current source.
4	GND	Chip Return	
5	VIN	Chip Supply	12V chip supply. This can be either connected directly to the +12V rail supplying the switched load voltage or to a dedicated GND +12V supply.
6	CLTIM	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor determines the time delay between an overcurrent event and chip output shutdown (current limit time-out). The duration of current limit time-out is equal to $93k\Omega \times CLTIM$.
7	POK	Power Good Indicator	Indicates that the voltage on the ISEN+ pin is satisfactory. POK is driven by an open drain N-Channel MOSFET and is pulled low when the output voltage (V_{ISEN+}) is less than the UV level for the particular IC.
8	EN	Power-ON	EN is used to control and reset the chip. The chip is enabled when EN pin is driven high to a maximum of 5V or is left open. Do not drive this input $>5V$. After a current limit time-out, the chip is reset by a low level signal applied to this pin. This input has $20\mu A$ pull-up capability.

Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

V_{IN}	-0.3V to +16V
GATE	-0.3V to $V_{IN} + 8V$
ISEN+, POK, EN, CLTIM, ISET-	-0.3V to $V_{IN} + 0.3V$

Operating Conditions

V_{IN} Supply Voltage Range	+12V $\pm 15\%$
Temperature Range (T_A)	-40°C to +85°C
ESD	
Human Body Model	2.5kV
Machine Model	250V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
8 Ld SOIC Package	98
Maximum Junction Temperature (Plastic Package)	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile	—

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
- All voltages are relative to GND, unless otherwise specified.

Electrical Specifications $V_{IN} = 12V, T_A = T_J = \text{full temperature range, Unless Otherwise Specified.}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
CURRENT CONTROL						
ISET- Current Source	I_{ISET_ft}		17	20	22	μA
ISET- Current Source	I_{ISET_pt}	$T_J = +15^\circ\text{C to } +55^\circ\text{C}$	19	20	21	μA
Current Limit Amp Offset Voltage	V_{io_ft}	$V_{ISET-} - V_{ISEN+}$	-4.5	0	4.5	mV
Current Limit Amp Offset Voltage	V_{io_pt}	$V_{ISET-} - V_{ISEN+}, T_J = +15^\circ\text{C to } +55^\circ\text{C}$	-2	0	2	mV
GATE DRIVE						
GATE Response Time to Severe OC	pd_woc_amp	V_{GATE} to 10.8V	-	100	-	ns
GATE Response Time to Overcurrent	pd_oc_amp	V_{GATE} to 10.8V	-	600	-	ns
GATE Turn-On Current	I_{GATE}	V_{GATE} to = 6V	10.8	14	16.7	μA
GATE Pull-Down Current	OC_GATE_I_4V	Overcurrent	45	82	124	mA
GATE Pull-Down Current (Note 4)	WOC_GATE_I_4V	Severe Overcurrent	-	0.8	-	A
Undervoltage Threshold	12V _{UV_VTH}		8.9	9.6	10.2	V
GATE High Voltage	12VG	GATE Voltage	$V_{IN} + 5.7V$	$V_{IN} + 6.5V$	-	V
BIAS						
V_{IN} Supply Current	I_{VIN}		-	3	3.9	mA
V_{IN} POR Rising Threshold	$V_{IN_POR_L2H}$	V_{IN} Low to High	7	8.4	9	V
V_{IN} POR Falling Threshold	$V_{IN_POR_H2L}$	V_{IN} High to Low	6.9	8.1	8.7	V
V_{IN} POR Threshold Hysteresis	$V_{IN_POR_HYS}$	$V_{IN_POR_L2H} - V_{IN_POR_H2L}$	0.1	0.3	0.5	V
Maximum EN Pull-Up Voltage	PWRN_PUV	Maximum External Pull-up Voltage	-	5	-	V

that immediately shuts down the MOSFET switch should a rapid load current transient such as with a dead short cause the CR Vth to exceed the programmed level by 150mV. Additionally, it has an UV indicator and an OC latch indicator. The functionality of the POK feature is enabled once the IC is biased, monitoring and reporting any UV condition on the ISEN+ pin.

Upon initial power-up, the IC can either isolate the voltage supply from the load by holding the external N-Channel MOSFET switch off or apply the supply rail voltage directly to the load for true hot swap capability. The EN pin must be pulled low for the device to isolate the power supply from the load by holding the external N-Channel MOSFET off. With the EN pin held high or floating the IC will be in true hot swap mode. In both cases the IC turns on in a soft-start mode protecting the supply rail from sudden inrush current.

At turn-on, the external gate capacitor of the N-Channel MOSFET is charged with a 11µA current source resulting in a programmable ramp (soft-start turn-on). The internal ES1010SI charge pump supplies the gate drive for the 12V supply switch driving that gate to $\sim V_{IN} + 6.5V$. Load current passes through the external current sense resistor. When the voltage across the sense resistor exceeds the user programmed CR voltage threshold value, (see Table 1 for R_{ISET-} programming resistor value and resulting nominal current regulation threshold voltage, V_{CR}) the controller enters its current regulation mode. At this time, the time-out capacitor, on CLTIM pin is charged with a 20µA current source and the controller enters the current limit time to latch-off period. The length of the current limit time to latch-off duration is set by the value of a single external capacitor (see Table 2) for C_{CLTIM} capacitor value and resulting nominal current limited time-out to latch-off duration placed from the CLTIM pin (pin 6) to ground. The programmed current level is held until either the OC event passes or the time-out period expires. If the former is the case then the N-Channel MOSFET is fully enhanced and the C_{CLTIM} capacitor is discharged. Once C_{CLTIM} charges to $\sim 1.8V$ signaling that the time-out period has expired, an internal latch is set whereby the FET gate is quickly pulled to 0V turning off the N-Channel MOSFET switch, isolating the faulty load.

TABLE 1. R_{ISET-} PROGRAMMING RESISTOR VALUE

R _{ISET-} RESISTOR	NOMINAL CR VTH
10kΩ	200mV
4.99kΩ	100mV
2.5kΩ	50mV
1.25kΩ	25mV

NOTE: Nominal Vth = R_{ISET-} x 20µA.

TABLE 2. C_{CLTIM} CAPACITOR VALUE

C _{CLTIM} CAPACITOR	NOMINAL CURRENT LIMITED PERIOD
0.022µF	2ms
0.047µF	4.4ms
0.1µF	9.3ms

NOTE: Nominal time-out period = C_{CLTIM} x 93kΩ.

This IC responds to a severe overcurrent load (defined as a voltage across the sense resistor >150mV over the OC Vth set point) by immediately driving the N-Channel MOSFET gate to 0V in about 10µs. The gate voltage is then slowly ramped up turning on the N-Channel MOSFET to the programmed current regulation level; this is the start of the time-out period.

Upon a UV condition, the POK signal will pull low when connected through a resistor to the logic or VIN supply. This pin is a UV fault indicator. For an OC latch-off indication, monitor CLTIM, pin 6. This pin will rise rapidly from 1.8V to VIN once the time-out period expires.

See Figures 2 through 13 for graphs and waveforms related to text.

The IC is reset after an OC latch-off condition by a low level on the EN pin and is turned on by the EN pin being driven high.

Application Considerations

Design applications where the CR Vth is set extremely low (25mV or less), there is a two-fold risk to consider.

- There is the susceptibility to noise influencing the absolute CR Vth value. This can be addressed with a 100pF capacitor across the R_{SENSE} resistor.
- Due to common mode limitations of the overcurrent comparator, the voltage on the ISET- pin must be 20mV above the IC ground either initially (from I_{SET-}*R_{SET}) or before C_{CLTIM} reaches time-out (from gate charge-up). If this does not happen, the IC may incorrectly report overcurrent fault at start-up when there is no fault. Circuits with high load capacitance and initially low load current are susceptible to this type of unexpected behavior.

Do not signal nor pull-up the EN input to > 5V. Exceeding 6V on this pin will cause the internal charge pump to malfunction.

During the soft-start and the time-out delay duration with the IC in its current limit mode, the V_{GS} of the external N-Channel MOSFET is reduced driving the MOSFET switch into a (linear region) high $r_{DS(ON)}$ state. Strike a balance between the CR limit and the timing requirements to avoid periods when the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the **MOSFET SOA** information in the manufacturer's data sheet.

When driving particularly large capacitive loads a longer soft-start time to prevent current regulation upon charging and a short CR time may offer the best application solution relative to reliability and FET MTF.

Physical layout of R_{SENSE} resistor is critical to avoid the possibility of false overcurrent occurrences. Ideally, trace routing between the R_{SENSE} resistors and the IC is as direct and as short as possible with zero current in the sense lines (see Figure 1).

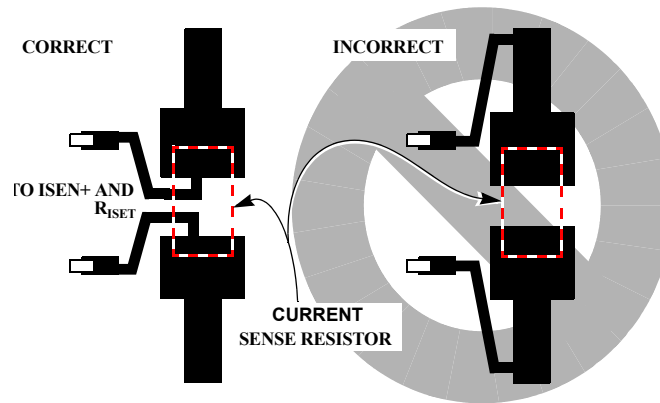


FIGURE 1. SENSE RESISTOR PCB LAYOUT

Typical Performance Curves

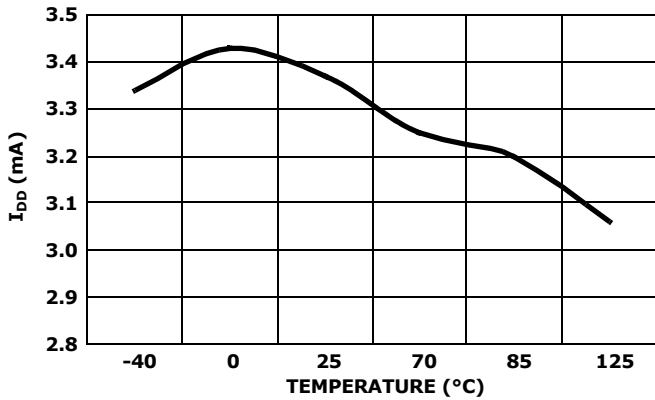


FIGURE 2. V_{IN} BIAS CURRENT

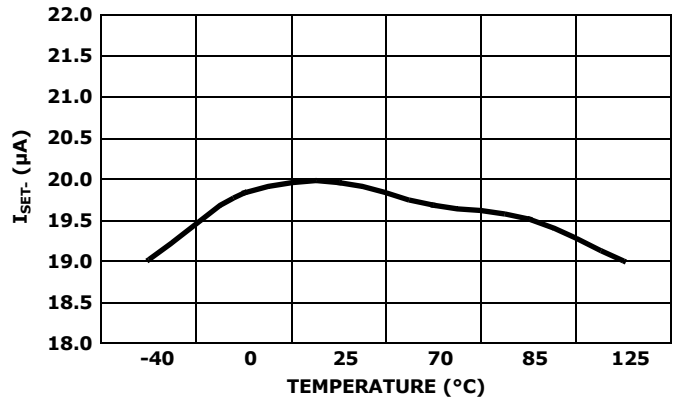


FIGURE 3. I_{SET-} SOURCE CURRENT

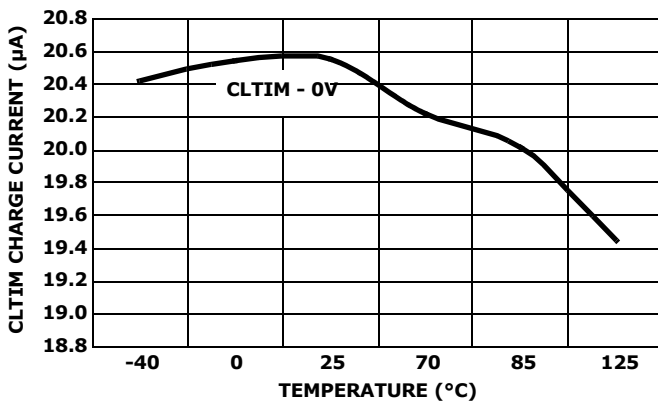


FIGURE 4. C_{CLTIM} CURRENT SOURCE

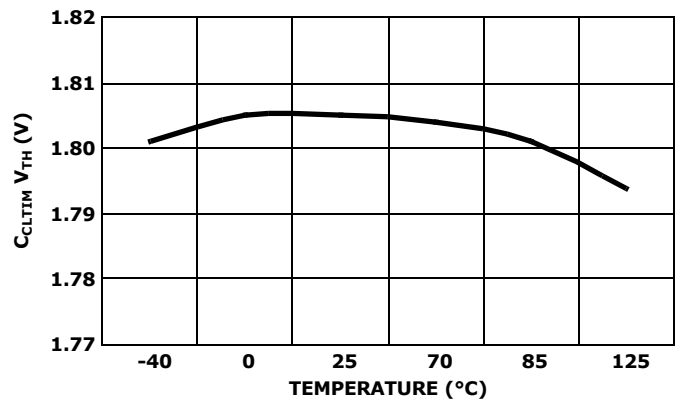


FIGURE 5. C_{CLTIM} OC VOLTAGE THRESHOLD

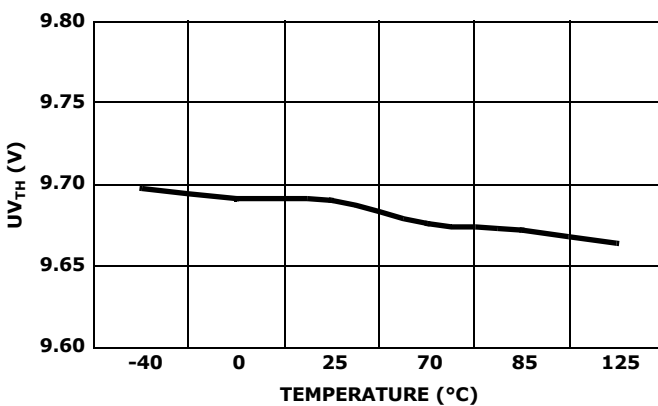


FIGURE 6. UV THRESHOLD

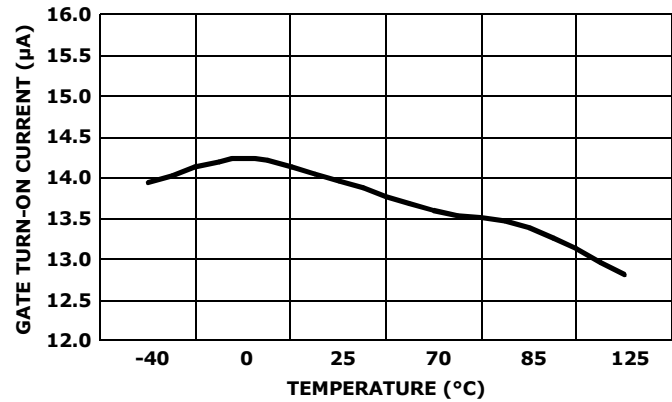


FIGURE 7. GATE CHARGE CURRENT

(EQ. 1)

$$I_{DD1} = \frac{(72 - 12)}{1.58k\Omega}$$

$$I_{DD1} = 38mA [\text{Typical Value} = 12V \text{ rating, } 50mA \text{ reverse current}]$$

Typical Performance Curves (Continued)

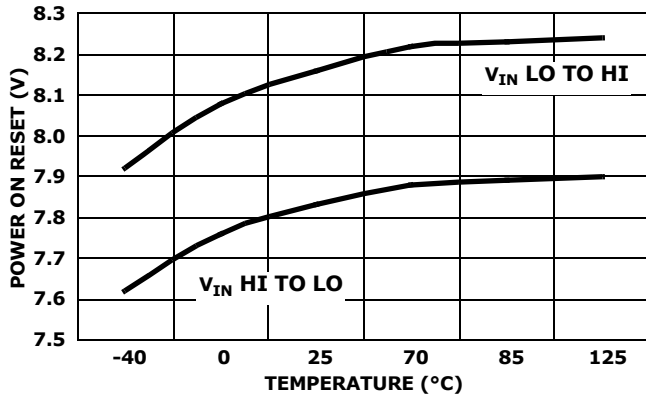


FIGURE 8. POWER-ON RESET VOLTAGE THRESHOLD

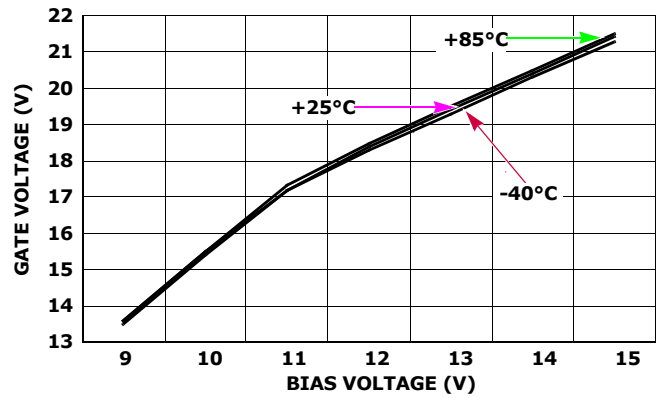


FIGURE 9. GATE VOLTAGE vs BIAS and TEMPERATURE

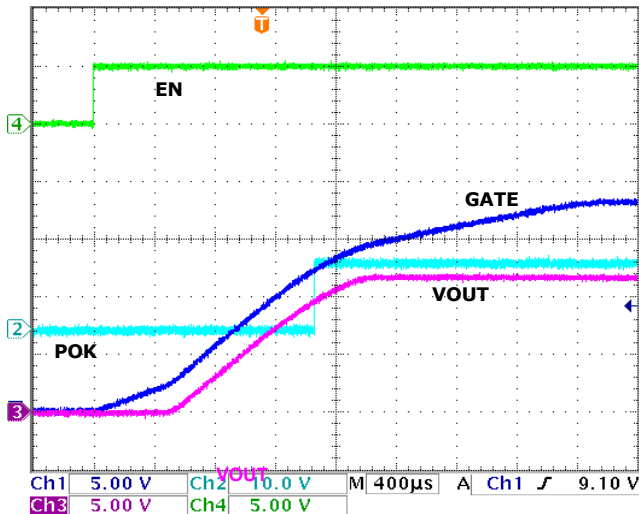


FIGURE 10. ES1010SI TURN-ON

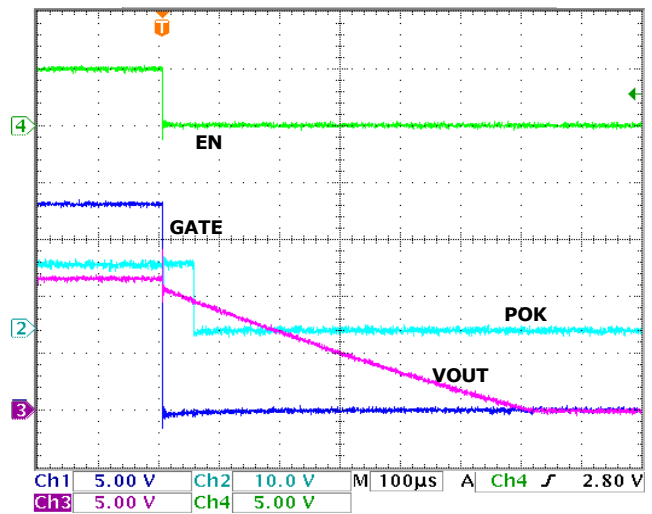


FIGURE 11. ES1010SI TURN-OFF

Typical Performance Curves (Continued)

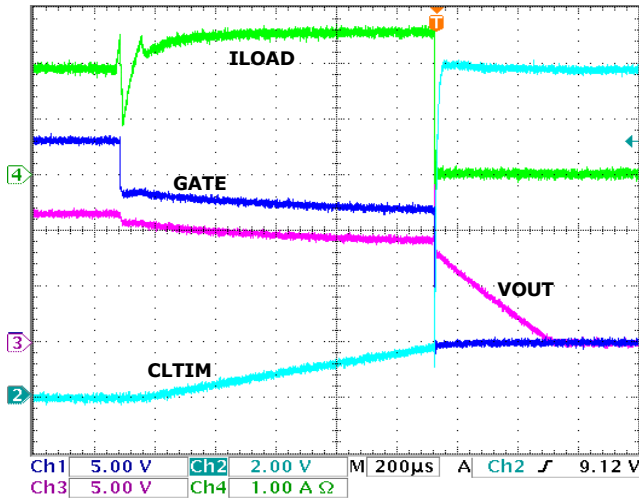


FIGURE 12. IOC REGULATION and TURN-OFF

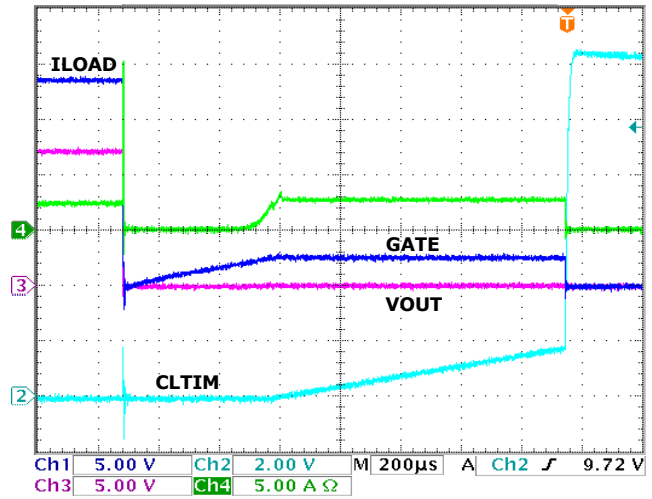


FIGURE 13. WOC TURN-OFF and RESTART

EVB-ES1010SI Board

The EVB-ES1010SI is default provided as a +12V high side switch controller with the CR level set at ~2.5A. See Figure 11 for EVB-ES1010SI schematic and Table 3 for BOM. Bias and load connection points are provided along with test points for each IC pin.

With J1 installed the ES1010SI will be biased from the +12V supply (V_{IN}) being switched. Connect the load to VLOAD+. EN pin pulls high internally enabling the ES1010SI if not driven low via EN test point or J2.

With $R_3 = 1.24k\Omega$ the CR V_{th} is set to 24.8mV and with the 10m Ω sense resistor (R_1) the EVB-ES1010SI has a nominal CR level of 2.5~A. The 0.01 μ F delay time to latch-off capacitor results in a nominal 1ms before latch-off of output after an OC event.

Reconfiguring the EVB-ES1010SI board for a higher CR level can be done by changing the R_{SENSE} and/or R_{ISET} resistor values as the provided FET is rated for a much higher current.

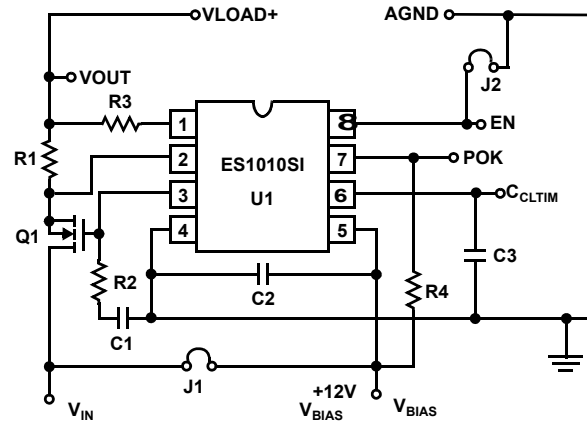


FIGURE 14. EVB-ES1010SI HIGH SIDE SWITCH APPLICATION

TABLE 3. BILL OF MATERIALS, EVB-ES1010SI

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
U1	ES1010SI	Altera Enpirion
Q1	N-FET	11.5m Ω , 30V, 11.5A Logic Level N-Channel Power MOSFET or equivalent
R1	Load Current Sense Resistor	WSL-2512 10m Ω 1W Metal Strip Resistor
R2	Gate Stability Resistor	20 Ω 0603 Chip Resistor
R3	Overcurrent Voltage Threshold Set Resistor	1.24k Ω 0603 Chip Resistor ($V_{th} = 24.8mV$)
R4	POK Pull up Resistor	10k Ω 0603 Chip Resistor
C1	Gate Timing Capacitor	0.001 μF 0402 Chip Capacitor (<2ms)
C2	IC Decoupling Capacitor	0.1 μF 0402 Chip Capacitor
C3	Time Delay Set Capacitor	0.01 μF 0402 Chip Capacitor (1ms)
J1	Bias Voltage Selection Jumper	Install if switched rail voltage is = +12V.
J2	EN Disable	Install J2 to disable U2. Connects EN to GND.

Document Revision History

The table lists the revision history for this document.

Date	Version	Changes
March 2014	1.0	Initial release.

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