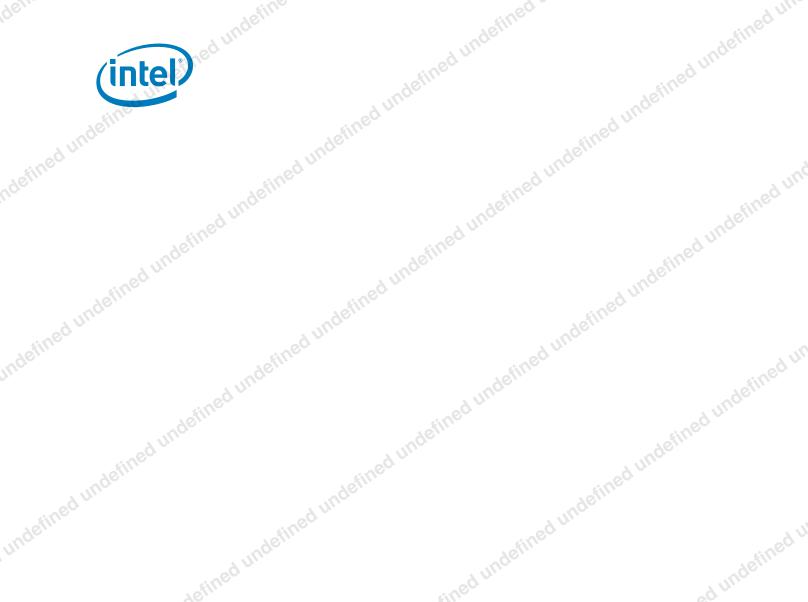


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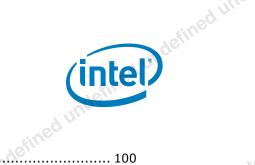
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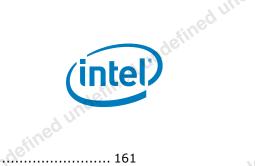


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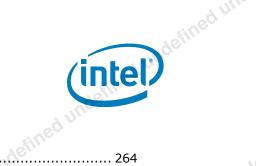
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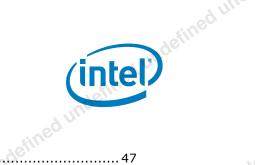
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Revision History

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	Document Number	Revision Number	Description	Revision Date	JUL
	332065	001	Initial release	March 2015	
tined unde	332065	002	 Added Type3 SoC features and specifications included Updated Section 2.24, "Hardware Straps" strap pins updated. Max. Imaging video resolution updated for T4 to 1080p30. Table 124 VID values for all SKU's to match PRQ values. Section 12.1, "SoC Storage Overview" 	June 2015	undefine
		003	 Added Intel[®] Atom[™] processor X5-Z8350, Z8550, and Z8750. Updated Table 3, updated Table 124 	March 2016	undein
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Introduction ndefined undefined



Introduction

The **Intel[®] Atom™ Z8000 Processor Series Datasheet** is the Intel Architecture (IA) SoC that integrates the next generation Intel[®] processor core, Graphics, Memory Controller, and I/O interfaces into a single system or still

The figures below shows the system level block diagram of the SoC. Refer the subsequent chapters for detailed information on the functionality of the different interface blocks.

Note:

Throughout this document Intel[®] Atom[™] Z8000 Processor Series is referred as SoC.

Section 1.3 lists the different features supported by the SoC packages.

References 1.1 undefined undefined

Refer the following documents, which may be beneficial when reading this document or for additional information:

Document	Document Number	
Intel [®] 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/ products/processor/ manuals/index.htm	undefined
Intel [®] Atom [™] Z8000 Processor Series Datasheet (Volume 2 of 2)	332066	
Intel [®] Atom [™] Z8000 Processor Series Specification Update	332067	
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Terminology

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3 un	Term	Description	definec
	ACPI	Advanced Configuration and Power Interface	uno
20	Cold Reset	Full reset is when PWROK is de-asserted and all system rails except VCCRTC are powered down	
	DP	Display Port	
	DTS	Digital Thermal Sensor	
du.	EMI	Electro Magnetic Interference	-
undefined undefined u	eDP	embedded Display Port	
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terined under		ined undefine	

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hed unde	under	define
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	under.	
Aine	ed U.	
inde	define	
Term	Description	
НДМІ	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-	, Ú
timed und	definition video, plus multi-channel digital audio on a single cable. HDMI transmits all Advanced Television Systems Committee (ATSC) HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available at http://www.hdmi.org/).	Indefineo
Intel [®] TXE	Intel [®] Trusted Execution Engine	
LPDDR	Low Power Dual Data Rate memory technology.	
LPE	Low Power Engine	
MIPI CSI	MIPI Camera Interface Specification	
MIPI DSI	MIPI Display Interface Specification	
MP	Mega Pixel	6
MPEG	Moving Picture Experts Group	atine
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.	unoc
sined undefined the MSR	Model Specific Register, as the name implies, is model-specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64 bits of the MSR in the EDX: EAX register pair. The WRMSR writes the contents of the EDX: EAX register pair into the MSR.	
PWM	Pulse Width Modulation	
POSM	Power on state machine	stine
Rank SCI SDRAM SERR SMC	A unit of DRAM corresponding to the set of SDRAM devices that are accessed in parallel for a given transaction. For a 64-bit wide data bus using 8-bit (x8) wide SDRAM devices, a rank would be eight devices. Multiple ranks can be added to increase capacity without widening the data bus, at the cost of additional electrical loading.	Junde
SCI	System Control Interrupt. SCI is used in the ACPI protocol.	
SDRAM	Synchronous Dynamic Random Access Memory	
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.	
SMC	System Management Controller or External Controller refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks.	indefine
SMI	System Management Interrupt is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).	<i>,</i> d <i>,</i>
SIO	Serial I/O	
SIO TMDS Warm Reset	Transition-Minimized Differential Signaling. TMDS is a serial signaling interface used in DVI and HDMI to send visual data to a display. TMDS is based on low-voltage differential signaling with 8/10b encoding for DC balancing.	
Warm Reset	Warm reset is when both PMC_PLTRST# and PMC_CORE_PWROK are asserted.	
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Table 1.

1.3	SoC Packages Interface		a undefined unc	tined un
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Table 1.	SoC Packages	(Sheet 1 of 2)	a undefined unc	Ained L.
Table 1.	SoC Packages	(Sheet 1 of 2)	a undefined unc	ξη.
Table 1.	SoC Packages	(Sheet 1 of 2)	d unor	
_	Interface			
unde		2A	→ ^C T 4	T3 2 U
-	CDU	No. of Cores	4	4 4
F	CPU	Burst Speed	2.4 GHz	1.84 GHz ^[4]
	GPU	Speed	Gen8-LP 12/16EU up to 600 MHz	Gen8-LP 12EU up to 500 MHz
		Туре	17x17mm Type 4	17x17mm Type 3
	nin safin	IO count	628	378
	Package Mechanical	Ball count	1380	592
		ball pitch	0.4mm	0.65mm
, de	11.	Z-height	0.937mm	1.002mm
06	Memory	Interface, Max transfer data rate	Dual Channel 2x64 bit, LPDDR3 - 1600MT/S	Single Channel 1x32/64 DDR3L-RS - 1600MT/s
	mentor y	Туре	BGA	BGA
		Capacity	2 - 8GB	1 - 2GB
F		Number of ports	2	1
	PCIe	Port Configuration	1x2, 2x1	×1
		Number of lanes	6	6
	Imaging	Lane configuration	4+2, 3+2, 2+2+2	4+2, 3+2, 2+2
n0e		Speed	1.5 GHz	1.5 GHz
		Still & Video	13MP ZSL, 1080p30	8MP, 1080p30
nd	Media	Media decode rate	H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG	H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG
		Media encode rate	H.264, H.263, VP8, MVC, JPEG	H.264, H.263, VP8, MVC, JPEG
F	Audio	LPE (Low Power Engine)	3 I2S ports	3 I2S ports
	edu	USB 3.0	3	Not Supported
		USB 3.0 OTG	510 ⁰⁰ 1	1 20
n ^p	USB devices	USB 2.0	-	3 stine
uno		USB SSIC	2	Not Supported
		USB HSIC	2 defined undefined u	2

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intel	ined undefin	ed undef	ined undefined	Introduction
Idefined undefinition Table 1.	SoC Packages		uni	
	Interface	Category	T4 CO	Т3
	, uno	LPC	YES	Not supported
	tined -	I2C	d U1 7	6
	ethi	I2C Max Speed	1.7 MHz	1.7 MHz
d un		I2C NFC	1	1
	SIO	I2C ISH	1	UI CO
nder		SPI	3	Not supported ^[1]
Idefined undefined und		SPI Speed	Master Only up to 25 MHz	Master Only up to 25 MHz
	101	Fast SPI	Quad mode	Dual mode
	, una	SD Card	x1 SDR104	x1 SDR104 ^[2]
	Storage	SDIO	x1 SDR104	x1 SDR104
	detti	eMMC	4.51	4.51
d un		DDI ports	x3	x2
adefinec		Max MIPI DSI Resolution	2560x1600 @60fps	1900x1200 @60fps
dull		MIPI-DSI ports	2x 4 Lanes @ 1Gbps	1x 4 Lanes @ 1Gbps
ndefined undefined un	Display	Max eDP Resolution	2560x1600 @ 24bbp	1920x1080 @60fps
	ed uno	eDP ports	2 (2x4 @2.7Gbps)	2 (2x4 @2.7Gbps)
d undefined u	ndefine	Max DP 1.1a Resolution	2560x1600 @60fps	2560x1600 @60fps
offined b		Max HDMI 1.4b Resolution	3840x2160 @30fps	1920x1080 @60fps
d under	NOTES:	ndefini	1	retined

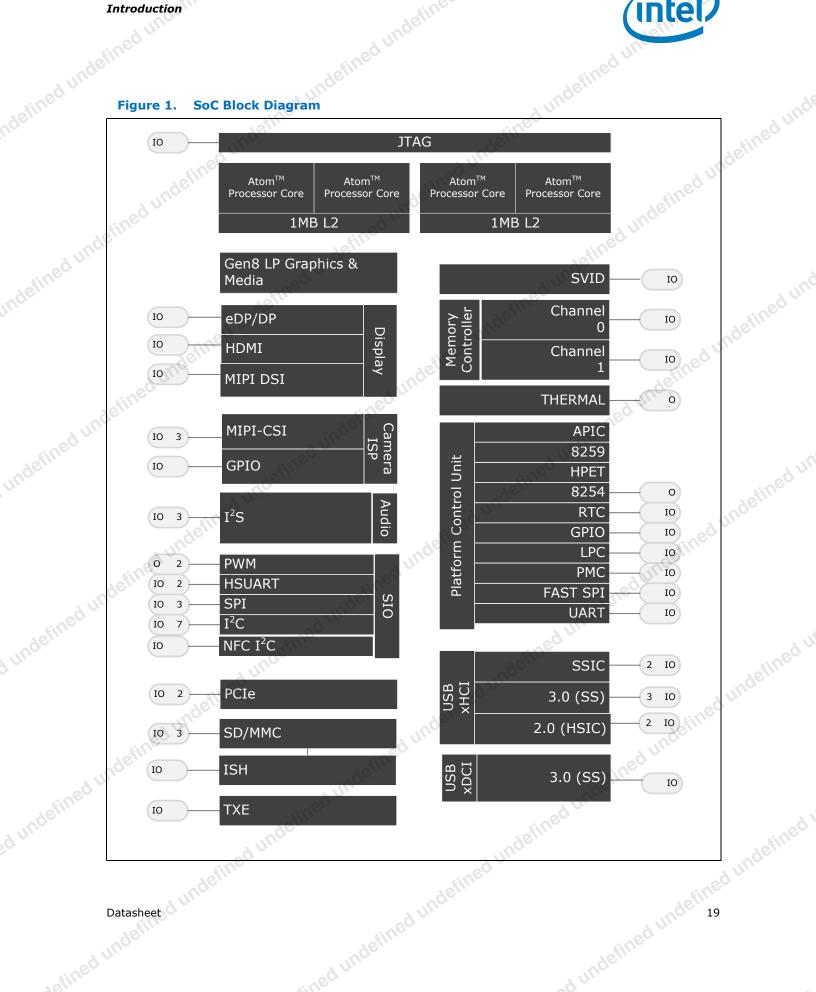
NOTES:

- undefined undefined un 1. One SPI port is multiplexed with reference clock signal which is GPIO signal, and the usage will be dependent on the GPIO configurations on the platform.
 - 2. Is limited to DDR50 due to PMIC power delivery limitation.
 - 3. MPO available on Display Pipe B only.
 - 4. The Burst Speed mentioned is for 2 Cores. This is PRE-SMT package height. undefined undefined undefined undefined undefined undefined undefit



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Idefined undefined undefined SoC Block Diagram Figure 1.



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Introduction



Feature Overview 1.4

1.4.1 **Processor Core**

- Up to four IA-compatible low power Intel[®] processor cores
 - One thread per core
- Two-wide instruction decode, out of order execution.
- On-die, 32 KB 8-way L1 instruction cache and 24 KB 6-way L1 data cache per core.
- On-die, 1 MB, 16-way L2 cache, shared per two cores.
- 36-bit physical address, 48-bit linear address size support.
- Supported C-states: C0, C1, C6C, C6, C7.
- Supports Intel[®] Virtualization Technology (Intel[®] VT-x2).

1.4.2 System Memory Controller Indefined undefined

- Memory Controller supports dual-channel DDR3L-RS/LPDDR3.
- Up to two ranks per channel (4 ranks in total).
- 32 Bit or 64 Bit data bus.
- Supports DDR3L-RS/LPDDR3 with 1600 MT/s data rate.
- Supports x32 LPDDR3 DRAM device data widths.
- Supports x16 DDR3L-RS DRAM device data widths.
- Total memory bandwidth supported is 12.8GB/s (for 1600 MT/s single-channel) to 25.6GB/s (for 1600 MT/s dual-channel).
- Supports different physical mappings of bank addresses to optimize performance.
- Supports Dynamic Voltage and Frequency Scaling.
- Out-of-order request processing to increase performance.
- Aggressive power management to reduce power consumption.
- Proactive page closing policies to close unused pages.

1.4.3 **Display Controller**

- Supports up to 3 Display pipes.
- Supports 2 MIPI DSI ports.
- Supports 3 DDI ports to configure eDP 1.3/DP 1.1a/DVI/HDMI 1.4b.
- Supports 2 panel power sequence for 2 eDP ports.
- Supports Audio on DP/HDMI.
- Supports Intel[®] Display Power Saving Technology (DPST) 6.0, Panel Self Refresh (PSR) and Display Refresh Rate Switching Technology (DRRS). indefined undefin

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1.4.4 **Graphics and Media Engine**

- fined undefined und • Intel's 8th generation (Gen 8) LP graphics and media encode/decode engine.
- Supports 3D rendering, media compositing and video encoding.
- Graphics Burst enabled through energy counters.
- Supports DX*11.1, OpenGL 4.3, OGL ES 3.0, OpenCL 1.2.
- 4x anti-aliasing.
- Full HW acceleration for decode of H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG.
- Full HW acceleration for encode of H.264, H.263, VP8, MVC, JPEG.
- defined undefined undefined Supports Content protection using PAVP2.0, HDCP 1.4 (wired)/2.2 (wireless) and Media Vault DRM.

1.4.5 Image Signal Processor

- Supports up to three MIPI CSI ports.
- Supports up to 13MP sensors.

indefined undefined **Power Management**

- Supports ACPI 5.0.
- Processor Core states: C0, C1, C1E, C6C, C6 and C7.
- Display and Graphics device states: D0, D3.
- System sleep states: S0, S0ix, S4, S5.
- Support CPU and GFx Burst for selected SKUs.
- Dynamic I/O power reductions (disabling sense amps on input buffers, tristating output buffers).
- Dynamic memory self-refresh.

1.4.7 **PCI Express***

- Supports x2 PCIe 2.0 compliant controller.
- Supports both Gen1 and Gen2 data rates.
- The controller provides a max data payload of 128B with the capability of splitting the request at 64B granularity.
- Supports autonomous up-configuration and autonomous down-configuration as in a materined undefined undefined target. A undefined undefined undefined Datasheet o undefined undefined





1.4.8 **USB** Controller

1.4.8.1 **USB xHCI Controller**

USB Host Controller supports:

- Two (2) Super Speed Inter-Chip (SSIC) port.
- Three (3) Super Speed (SS) ports [Backward Compatible of USB 2.0 HS/FS/LS]
- Two (2) High Speed Inter-Chip (HSIC) ports.
- SoC can support the 4th SS port when OTG port is in Host mode.

1.4.8.2 **USB xDCI Controller**

The SoC implements OTG block for device-mode functionality:

- Supports one USB 3.0 Super Speed port with backward compatibility of USB 2.0 High Speed and Low/Full Speed.
- Supports SuperSpeed OTG v3.0 device.
- Supports USB3 Debug Device Class Specification [USB3-debug].

1.4.9

1.4.10

Note:

Low Power Engine (LPE) Audio Controller

- Support 3 I2S ports.
- I2S and DDI with dedicated DMA.
- Supports MP3, AAC, AC3/DD+, WMA9, PCM (WAV).
- ned undefined undefined Provides HW acceleration for common audio and voice functions such as codecs, acoustic echo cancellation, noise cancellation.

Storage

Storage Control Cluster (eMMC, SDIO, SD) 1.4.10.1

- Supports one eMMC 4.51 controller 200 MB/s Data rate
- Supports one SDIO 3.0 interface 800 Mb/s Data rate
- Supports one SDXC controller
- 800 Mb/s Data rate

1.4.11

Intel[®] Trusted Execution Engine (Intel[®] TXE)

Intel TXE is responsible for supporting and handling security related features.

- Supports MediaVault with OMA-DRM and One Time Password.
- Isolated execution environment for crypto operations.
- Supports secure boot with customer programmable keys to secure code.

(intel)

Introduction

1.4.14

Serial I/O (SIO) 1.4.12

- Controller for external devices via SPI, UART, I²C or PWM.
- Each port is multiplexed with general purpose I/O for configurations flexibility.
- Supports up to 7 I²C, NFC I²C, ISH I²C, 2 HSUART, 2 PWM, 3 SPI interface.

Platform Control Unit (PCU) 1.4.13

Platform controller unit is a collection of HW blocks, including UART, debug/boot SPI and Intel legacy block (iLB), that are critical to implement a Windows* compatible platform. Some of its key features are:

- Universal Asynchronous Receiver/Transmitter (UART) with COM1 interface.
- j undefined A Fast Serial Peripheral Interface (SPI) for Flash only - stores boot FW and system configuration data.
- Intel Legacy Block (iLB) supports legacy PC platform features
 - RTC, Interrupts, Timers and Peripheral interface (LPC for TPM) blocks.

Intel[®]Sensor Hub

Intel[®] Sensor Hub Supports:

- Acquisition / sampling of sensor data.
- The ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS.
- Low power operation through clock gating and power gating of parts of the ISH together with the ability to turn sensors off.
- The ability to operate independently when the host platform is in low power state.

.4.15 Package

	Category	, T4 [©]	Т3	C SkUs.
	Туре	17x17mm Type 4	17x17mm Type 3	unoc
ackage	IO count	628	378	20
uckuge	Ball count	1380	592	
	ball pitch	0.4mm	0.65mm	
	Z-height	0.937mm	1.002mm	_
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Table 2. **Package Attributes**

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	inte				defined	undef	Ined	~		2	Introdu	1 V.	
defined und	1.4.16	SKU	List	ined un	defill				ned und	Jefined			d und
	Processor	sine	KU List Package	SDP(W)	Core LFM (MHz)/	Core max	Tjmax	TDP/ SDP	GFx Normal	No. of		Memory	afinet.
	Number	Stepping	Туре	SUP(W)	(MHZ)/ HFM (GHZ)	Burst (GHz)	(°C)	Tj(°C)	/Burst (MHz)	Graphics EU	Channel	(MT/s)	
	Z8750	D-1	T4	2.0	480/1.6	2.56	90	70	400/600	16	2x64	LPDDR3- 1600	_
med un	Z8550	D-1	T4	2.0	480/1.44	2.4	90	70	400/600	12	2x64	LPDDR3- 1600	_
defil	Z8350	D-1	T3	2.0	480/1.44	1.92	90	70	400/500	12	1x64	DDR3L/ LPDDR3- 1600	ined un
	Z8700	C-0	T 4	2.0	480/1.6	2.4	90	70	400/600	16	2x64	LPDDR3- 1600	detti
	Z8500	C-0	T4	2.0	480/1.44	2.24	90	70	400/600	12	2x64	LPDDR3- 1600	
	Z8300	C-0	Т3	2.0	480/1.44	1.84	90	70	400/500	12	1x32/64	DDR3L- 1600	
	nder.				ndefin		· · ·			Jetine	0		
lefineu		Issue		i heni	21		Ax/Bx, A		in reset di	uring warm	n reboot cy	ycles	
Indefined un		Stepp	around	SIL		BIOS bit2	6 should	program		t Controlle g and clea) 2 :her	ndefined ut
		Impa	ct of Wor	r <mark>karound</mark>			Jetine					fined	
		Notes				USB					Ó	<u> </u>	

6	inet and the second s	
Issue	XHCI controller stuck in reset during warm reboo	ot cycles
Stepping	BXT Ax/Bx, APL Ax	
Workaround	BIOS should program USB Host Controller Misc bit2 =1, set Bit5 for A0 stepping and clear for al steppings	
Impact of Workaround	defili	All
Notes	USB	196

	sino		stepp	ings	June
	Impact of Workaround		5.	efti.	ner
undefined undefined ut	Notes	0	USB	under	
ndell		- serine		and the second s	
ed un	Pad Name	o ^{oo} GPI	O #	Net Name	
defille	GP187_DDI0_DDC_SDA	GPIO_18	7	HDMI_DDC_SDA	
UNC	GP188_DDI0_DDC_SCL	GPIO_18	8	HDMI_DDC_SCL	sineo
	GP193_PNL0_VDDEN	GPIO_19	3	DISP0_VDDEN	den
24 undefined undefined u	undefined undefined	undefine		Net Name HDMI_DDC_SDA HDMI_DDC_SCL DISP0_VDDEN § Datash	tined undefined
24 24 Lindefined	- ine	d undefin	led ut	Datash	leet

Physical Interfaces

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2.1



Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, Some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

Pin States

This section describes the states of each signal before, during and directly after reset. Additionally, Some signals have internal pull-up/pull-down termination resistors, and their values are also provided. All signals with the "" symbol are muxed and may not be available without configuration. defined

Platform Power Well Definitions Table 4.

defined undefined	Power Type	Voltage Range (V)	Power Well Description	
ed u	VCC0/1	Refer Table 118	Variable voltage rail for core	
etine	VGG	Refer Table 118	Variable voltage rail for Graphics Core	
	VNN	Refer Table 118	Variable voltage rail for SoC.	
	V1P15	1.15	Fixed voltage rail for SoC, Graphics, camera	defill
	V1P05A	1.05	Fixed voltage rail for P-unit, LPE, TXE,I/O's, PLL's and ISH	,no.
	V1P2A	1.24	Fixed voltage rail for I/O's and PLL's.	
edu	VDDQ	1.24/1.35	Fixed voltage rail for DDR PHY	
	VDDQG	1.24/1.35	Fixed voltage rail for DDR PHY	
unoc	V1P8A	1.8	Fixed voltage rail for I/O's.	
adefined undefills	V3P3A	3.3	Fixed voltage rail for I/O's.	
defin	V3P3A_V1P8A	1.8/3.3	Fixed voltage rail for SDIO.	
	V3P3RTC	3.3	Voltage rai For RTC clock.	
Table 5.	Buffer Type I	Definitions (She	eet 1 of 2) ned une	Inder

Table 5.

Buffer Type Definitions (Sheet 1 of 2)

Buffer Type	Buffer Description	
MIPI-DPHY	1.24 V tolerant MIPI DPHY buffer type	
USB3 PHY	1.0 V tolerant USB3 PHY buffer type	
USB2 PHY	1.8 V tolerant USB3 PHY buffer type	
SSIC PHY	1.2 V tolerant SSIC PHY buffer type	
HSIC PHY	1.2 V tolerant HSIC PHY buffer type	
GPIO	GPIO buffer type. This can be of the following types: 1.8/3.3 V.	dein
Indefine	ed undefined undefined undefined undefined undefined	, UII.

Datasheet Indefil undefil

Physical Interfaces



defined undefined undefined **Buffer Type Definitions (Sheet 2 of 2)** Table 5.

Buffer Type	Buffer Description
MODPHY	1.0 V tolerant MODPHY buffer type
DDR3	1.5 V tolerant DDR3 buffer type
Analog	Analog pins that do not have specific digital requirements. Often used for circuit calibration or monitoring.
GPIOMV, HS	GPIO Buffer type, Medium Voltage(1.8V), High Speed (FMAX~208Mhz)
GPIOMV, MS	GPIO Buffer type, Medium Voltage(1.8V), Medium Speed (FMAX~60Mhz)
GPIOMV, MS, CLK	GPIO Buffer type, Medium Voltage(1.8V), Medium Speed (FMAX~60Mhz), Clock
GPIOMV, HS, CLK	GPIO Buffer type, Medium Voltage(1.8V), High Speed (FMAX~208Mhz), Clock
GPIOMV, HS, RCOMP	GPIO Buffer type, Medium Voltage(1.8V), High Speed (FMAX~208Mhz), RCOMP
GPIOMV, MS, I2C	GPIO Buffer type, Medium Voltage(1.8V), Medium Speed (FMAX~60Mhz), I2C
GPIOHV, HS	GPIO Buffer type, High Voltage(1.8V/3.3V), High Speed (FMAX~208Mhz)
GPIOHV, HS, RCOMP	GPIO Buffer type, High Voltage(1.8V/3.3V), High Speed (FMAX~208Mhz), RCOMP

Default Buffer State Definitions (Sheet 1 of 2) Table 6.

	Delidate Burre	a State Demittons (Sheet 1 012)	
11	Buffer State	Description	>
atined L.	Z	The SoC places this output in a high-impedance state. For inputs, external drivers are not expected.	
indefined undefined	Do Not Care	The state of the input (driven or tristated) does not affect the processor. For outputs, it is assumed that the output buffer is in a high-impedance state.	
rines	V _{OH}	The SoC drives this signal high with a termination of 50 Ω .	
inde	V _{OL}	The SoC drives this signal low with a termination of 50 Ω .	du
70.	Unknown	The processor drives or expects an indeterminate value.	efine
	VIH	The SoC expects/requires the signal to be driven high.	Inde
	VIL	The SoC expects/requires the signal to be driven low.	ġ.
A U	"P" 1.1V	USB low speed Single ended 1.	
definec	Pull-up	This signal is pulled high by a pull-up resistor (internal or external — internal value specified in "Term" column).	
thed une	Pull-down	This signal is pulled low by a pull-down resistor (internal or external — internal value specified in "Term" column).	
defin	Running	The clock is toggling, or the signal is transitioning.	21
ed une	Off	The power plane for this signal is powered down. The processor does not drive outputs, and inputs should not be driven to the processor. (VSS on output)	defined
	undefines	odefined	led une
26		Datasheet	
od undefin		undefined t	
18fine		cined t	

undefined un



Physical Interfaces

ndefined undefin Table 6.

Default Buffer State Definitions (Sheet 2 of 2)

	d une	
	affined us	
Default Buffe	er State Definitions (Sheet 2 of 2)	
Buffer State	Description	duno
1 unos	Buffer drives V _{OH}	stinet
0.0	Buffer drives V _{OL}	NOE.
н	Buffer Hi Z, weak PU, default to 20K, unless explicitly specified otherwis	se
L	Buffer Hi Z, weak PD, default to 20K, unless explicitly specified otherwise	se
Input H	Input enable, weak PU	
Output L	Output enable, weak PU	
Pgm	Programmable	
Retain	retain configuration/data prior to standby	ind
System	Memory Controller Interface Signals	undefined t
DDR3L-RS	s and undefine	
DDR3L-RS Sy	ystem Memory Signals (Sheet 1 of 2)	
	Default Buffer State	77.

undefined undefined undef System Memory Controller Interface Signals 2.2

2.2.1 un⁰ **DDR3L-RS**

undefined undef Table 7. DDR3L-RS System Memory Signals (Sheet 1 of 2)

atineo	tined un				Def	fault Buffer St	ate	
undefined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	undefined un
	DDR3_M0_MA[15:0]	0	V1P35	DDR	Z	Z	Z	UNC
	DDR3_M0_CK[1,0]_P	0	V1P35	DDR	Z	Z	ZINC	
bec	DDR3_M0_CK[1,0]_N	0	V1P35	DDR	Z	Z	οŻ	
defille	DDR3_M0_CKE[3:0]	0	V1P35	DDR	Weak 0	0 0	0	
a undefined undefined	DDR3_M0_CS[1,0]_N	0	V1P35	DDR	Z	Z	Z	
sine ⁰	DDR3_M0_CAS_N	0	V1P35	DDR	Z	INOZ	Z	
dein	DDR3_M0_RAS_N	0	V1P35	DDR	Z	Z	Z	undefined
Un	DDR3_M0_WE_N	0	V1P35	DDR	Z	Z	Z	sinec
	DDR3_M0_BS[2:0]	0	V1P35	DDR	Unz	Z	Z	nder
	DDR3_M0_DRAMRST_N	0	V1P35	DDR	Weak 0	0	1	Un
	DDR3_M0_ODT[1,0]	0	V1P35	DDR	Z	Z	Z	
cin ^{ec}	DDR3_M0_DQ[63:0]	I/O	V1P35	DDR	Z	Z	, n°z	
den	DDR3_M0_DM[7:0]	0	V1P35	DDR	Z	Z	Z	
dune	DDR3_M0_DQSP[7:0]	I/O	V1P35	DDR	Z	Z	Z	
stines	DDR3_M0_DQSN[7:0]	I/O	V1P35	DDR	Z	JUCZ	Z	
nder	DDR3_M0_OCAVREF	0	V1P35	DDR	Ze	Z	Z	6
ed undefined undefined	DDR3_M0_ODQVREF	0	V1P35	DDR	Z	Z	Z	etine
	d undefined s			define	d un		eine	d unoc
Datasheet			60	JUUN			undel 27	7
Datasheet		und	efine	DDR		undefine		d undefined



Physical Interfaces

defined undefined undefined DDR3L-RS System Memory Signals (Sheet 2 of 2) Table 7.

ad undefine Table 7.	DDR3L-RS System M	emory	ed und y Signals	s (Sheet		ÎU.	Indefines	
	Jefine				Defa	ault Buffer Si	tate	
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	ndefine
	DR3_M0_RCOMPPD	Ι	V1P35	DDR	Z	Z	Z	
DI	DR3_M1_MA[15:0]	0	V1P35	DDR	Z	Z	Z	
DI	DR3_M1_CK[1,0]_P	0	V1P35	DDR	Z	Z	un z	
	DR3_M1_CK[1,0]_N	0	V1P35	DDR	Z	ZIVer	Z	
DI	DR3_M1_CKE[3:0]	0	V1P35	DDR	Weak 0	00	0	
DI	DR3_M1_CS[1,0]_N	0	V1P35	DDR	Z	Z	Z	undefin
DI	DR3_M1_CAS_N	0	V1P35	DDR	Z	Z	Z	
DI	DR3_M1_RAS_N	0	V1P35	DDR	Z	Z	Z	defin
DI	DR3_M1_WE_N	0	V1P35	DDR	Z	Z	Z	JULE
DI	DR3_M1_BS[2:0]	0	V1P35	DDR	Z	Z	Zine	
DI	DR3_M1_DRAMRST_N	0	V1P35	DDR	Weak 0	0	10	
DI	DR3_M1_ODT[1,0]	0	V1P35	DDR	Z	Z	Z	
UNO DI	DR3_M1_DQ[63:0]	I/O	V1P35	DDR	Z	Z	Z	
ned undefined Di Di Di Di Di	DR3_M1_DM[7:0]	0	V1P35	DDR	Z	, n°z	Z	
DI	DR3_M1_DQS[7:0]_P	I/O	V1P35	DDR	Z	Z	Z	
DI	DR3_M1_DQS[7:0]_N	I/O	V1P35	DDR	Z	Z	Z	
DI	DR3_M1_OCAVREF	0	V1P35	DDR	UNZ	Z	Z	undefi
DI	DR3_M1_ODQVREF	0	V1P35	DDR	Z	Z	Z	U
DI	DR3_M1_RCOMPPD	Ι	V1P35	DDR	Z	Z	Z	
C DI	DR3_DRAM_PWROK	Ι	V1P35	DDR	Input	Input	Input	
deill Di	DR3_CORE_PWROK	Ι	V1P35	DDR	Input	Input	Input	
tined une	ined	uno	9.			d undern.	,	

d undefined undefined

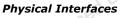
LPDDR3 System Memory Signals (Sheet 1 of 2) Table 8.

	dune		unde		Defa	ult Buffer S	State	
od undefine	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
adefined un	LPDDR3_M0_CA[9:0]	0	V1P24	DDR	Z	UN Z	Z	
inde	LPDDR3_M0_CK_P_A/B	0	V1P24	DDR	Z	Z	Z	ed l
39 r.	LPDDR3_M0_CK_N_A/B	0	V1P24	DDR	de z	Z	Z	10fine
	undefinet		6	stined				ned und
28			dune				Datashee	t
stined undefin	ed un	Jefin				undefine		



d un	andefine	nı.					entre	
atinec						tined un		
unde.	defile							
Table 8	LPDDR3 System Memory S	ignal	s (Sheet	2 of 2)				
etined undefined unit	stineo				Defa	ault Buffer S	State	ال م
~	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	ndefined ur
	LPDDR3_M0_CKE[1:0]_A/B	0	V1P24	DDR	Weak 0		0	-
defined undefined ut		0	.0-			0		_
einec	LPDDR3_M0_CS[1:0]_N	0	V1P24	DDR	Z	Z	Z	_
der	LPDDR3_M0_ODT_A/B	0	V1P24	DDR	Z	Z	Z	_
dui	LPDDR3_M0_DQ[31:0]_A/B	I/O	V1P24	DDR	Z	Z	Z	_
since	LPDDR3_M0_DM[3:0]_A/B	0	V1P24	DDR	Z	Z	Z	-
9e.	LPDDR3_M0_DQS[3:0]_P_A/B	I/O	V1P24	DDR	C ^O Z	Z	Z	- d'
	LPDDR3_M0_DQS[3:0]_N_A/B	I/O	V1P24	DDR	Z	Z	Z	- Stine
	LPDDR3_M0_OCAVREF	0	V1P24	DDR	Z	Z	Z	Inde
	LPDDR3_M0_ODQVREF	0	V1P24	DDR	Z	Z	Z	¥*
24	LPDDR3_M0_RCOMPPD	Ι	V1P24	DDR	Z	Z	Z	
sineu	LPDDR3_M1_CA[9:0]	0	V1P24	DDR	Z	Z	Z	
dell	LPDDR3_M1_CK_P_A/B	0	V1P24	DDR	Z	ZO	Z	
ndefined undefined u	LPDDR3_M1_CK_N_A/B	0	V1P24	DDR	Z	e Z	Z	
sine	LPDDR3_M1_CKE[1:0]_A/B	0	V1P24	DDR	Weak 0	0	0	1
nde.	LPDDR3_M0_CS[1:0]_N	0	V1P24	DDR	Z	Z	Z	6
»	LPDDR3_M0_ODT_A/B	0	V1P24	DDR	Z	Z	Z	fine
	LPDDR3_M1_DQ[31:0]_A/B	I/O	V1P24	DDR	Z	Z	Z	inde
	LPDDR3_M1_DM[3:0]_A/B	0	V1P24	DDR	Z	Z	Z	
2	LPDDR3_M1_DQS[3:0]_P_A/B	I/O	V1P24	DDR	Z	Z	Z	-
sineu	LPDDR3_M1_DQS[3:0]_N_A/B	I/O	V1P24	DDR	Z	Z	Z	-
d undefine		0	V1P24	DDR	Z	Z	Z	-
dun.	LPDDR3_M1_ODQVREF	0	V1P24	DDR	Z	Z	Z	_
sines	LPDDR3_M1_RCOMPPD	I	V1P24	DDR	Z	z	Z	-
Indefined une	LPDDR3_DRAM_PWROK	T	V1P24	DDR	Input	Input	Input	5
р.»	LPDDR3_CORE_PWROK	T	V1P24	DDR	Input	Input	Input	- stine
l		-	VIIZŦ	DDK	Input	Input	Input	Inde.
undefined undefined	LPDDR3_M1_OCAVILI LPDDR3_M1_ODQVREF LPDDR3_DRAM_PWROK LPDDR3_CORE_PWROK	ined	undefil	10		defined	undefine	
undefinee	thed undefined b			d un	defined			Indefine
Datasheet	J unden.		d undef	IUG-			undefin ²	9
ed une	inde					define		
	ed u.				. 1	unu		

defined undefined undefined ndefined undefined LPDDR3 System Memory Signals (Sheet 2 of 2) Table 8.





defined undefined ut **USB Controller Interface Signals** 2.3

USB2.0 Interface Signals 2.3.1

Table 9. USB2.0 Interface Signals undefined undefined

USB2.0 Interfact	Dir I/O	Plat. Power V1P8	Type	Def Pwrgood Assert State	ault Buffer St Resetout Deassert State	tate S0ix	TUR
B_DN[3:0] B_DP[3:0]	I/O	Power		Pwrgood Assert	Resetout Deassert	UNO.	
B_DN[3:0] B_DP[3:0]	I/O	Power		Assert	Deassert	S0ix	
B_DP[3:0]	·	V1P8				1	
	I/O		0502 111	"P" 1.1V	"P" 1.1V	S0i3 ¹	
D OTO ID		V1P8	USB2 PHY	"P" 1.1V	"P" 1.1V	S0i3 ¹	ed
B_OTG_ID	I/O	V1P8	USB2 PHY	Input, weak pull up	Input, weak pull up	Input	indefine
B_VBUSSNS	I/O	V1P8	USB2 PHY	Input	Input	Input	
B_RCOMP	0	V1P8	USB2 PHY	Output	Output	Output	
B_OC[1:0]_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
NOTES: 1. ¹ Depends on USI 2. USB 2.0 Port 0 is USB HSIC Ir	s the OTO	G port.	nals	undefined	J undefile		adefined
letine			cin ^e				
USB 2.0 HSIC In	nterface	e Signals	den			efine	
		ć		Def	ault Buffer St	tate	
	USB HSIC I	USB HSIC Interfa	Inder	USB HSIC Interface Signals	USB 2.0 HSIC Interface Signals	USB 2.0 HSIC Interface Signals	USB HSIC Interface Signals

NOTES:

USB HSIC Interface Signals 2.3.2

Table 10. USB 2.0 HSIC Interface Signals e undefined undefine

undefined L	NOTES: 1. ¹ Depends on USB2 2. USB 2.0 Port 0 is th		ort.		sine	d under		ed'
2.3.2	USB HSIC Int		e Signa	als	d undefine		ane	d undefined
Table 1	USB 2.0 HSIC Inte	erface S	ignals	IUUC		fault Buffer S		1
undefined undefine	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
under	USB_HSIC0_DATA	I/O	V1P2	HSIC Buffer	Weak 0	Weak 0	Weak 0	sined
	USB_HSIC0_STROBE	I/O	V1P2	HSIC Buffer	Weak 1	Weak 1	Weak 1	d under.
	USB_HSIC1_DATA	I/O	V1P2	HSIC Buffer	Weak 0	Weak 0	Weak 0	
odefin	USB_HSIC1_STROBE	I/O	V1P2	HSIC Buffer	Weak 1	Weak 1	Weak 1	
sined un.	USB_HSIC_RCOMP	000	V1P2	HSIC Buffer	Z	Zien	Z	
undefined undefin	NOTE: The HSIC shou	ld be rese	et after So(c.	ned undefin	160		ned undefine
30 ed undefit	led un	. u	ndefined	unoe			Datashee	t
18fine						dull		



Physical Interfaces

ndefined undefined **USB3.0 Interface Signals** 2.3.3

2.3.3.1 **USB 3.0 Interface Signals**

Table 11. USB 3.0 Interface Signals undefined undefined ur

USB3.0 Interface	Sign	als		ndefined			ndefined
USB 3.0 Interface S	ignals		stineo		fault Buffer S	0.0	
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	-
SB3_TXN[3:0]	0	V1P05A	USB3	х	n ^{de} z	Output	-
SB3_TXP[3:0]	0	V1P05A	USB3	Xed	Z	Output	eined
SB3_RXN[3:0]	Ι	V1P05A	USB3	X	Z	Input	sineo
SB3_RXP[3:0]	Ι	V1P05A	USB3	X	Z	Input	deir
SB3_RCOMP_N	I	V1P05A	USB3	Х	Output	Off)
SB3_RCOMP_P	Ι	V1P05A	USB3	Х	Output	Off	
NOTE: USB3.0 Port 0 is					adefined	unoc	
USB SSIC Interface	Signa	ls			une		

Jefined " 2.3.3.2 **USB SSIC Interface Signals**

Table 12. **USB SSIC Interface Signals**

undefined C Table 1	.2. USB SSIC Interface	e Sigr	nals		etined	unde		undefined u
	d unu				nd ^{en} De	1efine		
undefined undefined	Under Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	SOix	UNO-
	USB_SSIC_RX_N[0,1]	I/O	V1P24	SSIC PHY	Input	Input	Input	1
nden	USB_SSIC_RX_P[0,1]	I/O	V1P24	SSIC PHY	Input	Input	Input	1
du.	USB_SSIC_TX_N[0,1]	I/O	V1P24	SSIC PHY	Z	Output	Output	1
efine	USB_SSIC_TX_P[0,1]	I/O	V1P24	SSIC PHY	Z	Output	Output	1 .
Inde	USB_SSIC_RCOMP_N	0	V1P24	SSIC PHY	Output	Output	Output	ed '
	USB_SSIC_RCOMP_P	0	V1P24	SSIC PHY	Output	Output	Output	1efine
d undefined undefined	A	d un		U		d undefine	3 unoc	4
	USB_SSIC_RCOMP_P			d undefine	d undefin.		d undefine	d undefined
Datasheet	la se	ed u	nder.			d undefine	9	

undefined und



Integrated Clock Interface Signals 2.4

					Def	ault Buffer Sta	ate
sined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	UND SOIX
d under.	ICLK_OSCIN	I	V1P0	Crystal Oscillator	Input (Crystal)	Input (Crystal)	Input (Crystal)
defined	ICLK_OSCOUT	0	V1P0	Crystal Oscillator	Output (Crystal)	Output (Crystal)	Output (Crystal)
UUC.	ICLK_ICOMP	0	Analog	Analog	Input	Input	Input
	ICLK_RCOMP	0	Analog	Analog	Input	Input	Input

Table 13. Integrated Clock Interface Signals

2.5 ned undefin Display - Digital Display Interface (DDI) Signals

Table 14. Digital Display Interface Signals (Sheet 1 of 2)

efinee					Def	fault Buffer State	e
undefine	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
	DDI0_TXP[3:0]	0	V1P24	DDI	ine z	Output	Output
	DDI0_TXN[3:0]	0	V1P24	DDI	Z	Output	Output
eine	DDI0_AUXP	I/O	V1P24	DDI	Z	Output	Output
dell	DDI0_AUXN	I/O	V1P24	DDI	Z	Output	Output
d un	DDI0_BKLTCTL	I/O	V1P8	GPIOMV, MS	0	0	0
stinee	DDI0_BKLTEN	I/O	V1P8	GPIOMV, MS	0	00	0
a undefined undefine	DDI0_DDC_CLK	I/O	V1P8	GPIOMV, MS, CLK	Input (20k PU)	Input (20k PU)	Input (20k PU)
~	DDI0_DDC_DATA	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)
	DDI0_HPD	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)
nip.	DDI0_VDDEN	I/O	V1P8	GPIOMV, MS	0	0	0 10
inde	DDI0_RCOMP_N	0	V1P24	DDI	Z	Output	Output
edu	DDI0_RCOMP_P	0	V1P24	DDI	Z	Output	Output
ad undefined undefine	DDI1_TXP[3:0]	0	V1P24	DDI	Z	Output	Output
unos	DDI1_TXN[3:0]	0	V1P24	DDI	Z	Output	Output
20	DDI1_AUXP	I/O	V1P24	DDI	Z not	Output	Output
32 Jefined undefin	led undefine		m.	defined un	defined s	d undefin	Datasheet
lefine-						d un	

undefined un



defined unde

idefined und

Indefined un

4. Digital Displ	av In		d unoc	at 2 of 2)	defined un	em			
	neo			Default Buffer State					
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix			
DDI1_AUXN	I/O	V1P24	DDI	Z	Output	Output			
DDI1_BKLTCTL	I/O	V1P8	GPIOMV, MS	0	0	0000			
DDI1_BKLTEN	I/O	V1P8	GPIOMV, MS	0	0 0	0			
DDI1_DDC_CLK	I/O	V1P8	GPIOMV, MS, CLK	Input (20k PU)	Input (20k PU)	Input (20k PU)			
DDI1_DDC_DATA	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)			
DDI1_HPD	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)			
DDI1_VDDEN	I/O	V1P8	GPIOMV, MS	0	0	0			
DDI1_RCOMP_N	0	V1P24	DDI	Z	Output	Output			
DDI1_RCOMP_P	0	V1P24	DDI	Z	Output	Output			
DDI2_DDC_CLK	I/O	V1P8	DDI	Z	Output	Output			
DDI2_DDC_DATA	I/O	V1P8	DDI	Z	Output	Output			
DDI2_TXP[3:0]	0	V1P24	DDI	Z	Output	Output			
DDI2_TXN[3:0]	0	V1P24	DDI	Z ine	Output	Output			
DDI2_AUXP	I/O	V1P24	DDI	Z	Output	Output			
DDI2_AUXN	I/O	V1P24	DDI	d v z	Output	Output			
DDI2_HPD	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)			

ndefined undefined Table 14. Digital Display Interface Signals (Sheet 2 of 2)

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MIPI DSI Interface Signals

Table 15. MIPI DSI Interface Signals (Sheet 1 of 2)

2.6	MIPI DSI I	nte	rface	Signals		lefined .		
Lefineo	.5. MIPI DSI Interfa	sq n,		-	actined	unde	· · ·	offined
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	unde
	MDSI_A_CLKN	0	V1P24	MIPI-DPHY	0	0	0	
nde	MDSI_A_CLKP	0	V1P24	MIPI-DPHY	0	0,000	0	
edu	MDSI_A_DN[3:0]	I/O	V1P24	MIPI-DPHY	0	0 0	0	
undefined undefin	MDSI_A_DP[3:0]	1/0	V1P24	MIPI-DPHY	0	0	0	
, unu-	MDSI_C_CLKN	0	V1P24	MIPI-DPHY	0	0	0	tined.
	MDSI_C_CLKP	0	V1P24	MIPI-DPHY	0 11	0	0	defini
Datasheet	d undefine	ed'	undefine	d undefine	20.	undefined	undefine ³³	d un



Physical Interfaces

MIPI DSI Interface Signals (Sheet 2 of 2) Table 15.

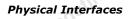
fineo		eet 2 of 2)	Defa	nu.			
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	Indefined
MDSI_C_DN[3:0]	I/O	V1P24	MIPI-DPHY	0	0	0	
MDSI_C_DP[3:0]	I/O	V1P24	MIPI-DPHY	0	0	0 0	
MDSI_RCOMP	I/O	V1P24	MIPI-DPHY	0	0 0	0	

undefined undefined

MIPI Camera Serial Interface (CSI) and ISP Idefined unde **Interface Signals**

Table 16. MIPI CSI Interface Signals

ned un		un ^c				ndefill		
ined un 2.7	MIPI Came Interface S	ra S igna	erial als	Interfac) and IS	P	undefined
Table	16. MIPI CSI Interfac	e Sigi	nals				6	UI.
	unc			ndei	Def	fault Buffer St		
stined undefine	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
fines	MCSI_1_CLKN	οI	V1P24	MIPI-DPHY	Input	Input	Input	
	MCSI_1_CLKP	Ι	V1P24	MIPI-DPHY	Input	Input	Input	
	MCSI_1_DN[0:3]	Ι	V1P24	MIPI-DPHY	Input	Input	Input	undefiner
	MCSI_1_DP[0:3]	Ι	V1P24	MIPI-DPHY	Input	Input	Input	unos
	MCSI_2_CLKN	Ι	V1P24	MIPI-DPHY	Input	Input	Input	
	MCSI_2_CLKP	Ι	V1P24	MIPI-DPHY	Input	Input	Input	
ined undefine	MCSI_2_DN[0:1]	Ι	V1P24	MIPI-DPHY	Input	Input	Input	
inde.	MCSI_2_DP[0:1]	Ι	V1P24	MIPI-DPHY	Input	Input	Input	
red	MCSI_3_CLKN	I	V1P24	MIPI-DPHY	Input	Input	Input	
	MCSI_3_CLKP	Γ	V1P24	MIPI-DPHY	Input	Input	Input	
	MCSI_RCOMP	I/O	V1P24	MIPI-DPHY	Input	Input	Input	
efined undefin	ed underined under	ned		d undefine	0 ₆	ed undefin	ed undefine	du.
34 sined undefi	MCSI_RCOMP	6	undefin	ed undefin	ed under.	undefi	Datasheet	ed undefin





ndefined undef **PCI Express Signals** 2.8

Table 17. PCIe Signals and Clocks

Jetined undefined un 2.8		. ATIN	led und					
Letined U. 2.8	PCI Express	Sig	nals		6	Indefin		inde
Table 17.	PCIe Signals and Cl	ocks			adefine			retined c
				ed l'	D	efault Buffer Sta	ate 🔍 🗸	100
Aefined undefined unde	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
under.	PCIE_RXN[0:1]	Jei I	V1P05	PCIe PHY	x	Weak Pull Down	Input	
defineo	PCIE_RXP[0:1]	I	V1P05	PCIe PHY	×	Weak Pull Down	Input	und
JUC	PCIE_TXN[0:1]	0	V1P05	PCIe PHY	X	Z	Output	sineo
	PCIE_TXP[0:1]	0	V1P05	PCIe PHY	NUC X	Z	Output	dell.
	P_RCOMP_N	IO	Х	PCIe PHY	Х		Off	
Inc	P_RCOMP_P	IO	Х	PCIe PHY	Х		Off	
defined t	PCIE_CLKREQ[0:1]_N	IO	V1P8	GPIOMV, MS	Х	Input (20k PU)	Prg	

undefined undefined unde

Low Power Engine (LPE) for Audio (I²S) Interface Signals

Table 18. LPE Interface Signals

	.nder.				Def	fault Buffer Stat	e sineo
a undefined undefined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	UN SOix
ined un	LPE_I2S[2:0]_CLK	I/O	V1P8	GPIOM V, MS	Input (20k PD)	Input (20k PD)	0
unden	LPE_I2S[2:0]_FRM	I/O	V1P8	GPIOM V, MS	Input (20k PD)	Input (20k PD)	1
0.	LPE_I2S[2:0]_DATAOUT	I/O	V1P8	GPIOM V, MS	0 (20k PD)	0 (20k PD)	0
	LPE_I2S[2:0]_DATAIN	I/O	V1P8	GPIOM V, MS	Input (20k PD)	Input (20k PD)	Input
ed undefined undefine	to undefined undefin	sd ut			d undefit	Input (20k PD)	
Datashee	undefilit				stined		lefiner
Jeffned Undefin	Ę.	.d 1	Indefin	ed un		od undefine	d unde 35



aed



ndefined und **Storage Interface Signals** 2.10

Storage Controller (eMMC, SDIO, SD) 2.10.1

Table 19. Storage Controller (eMMC, SDIO, SD) Interface Signals

SD3_D[3:0] I/O V1P8/ V3P3 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ V3P3 CPIOHV, HS Z (20k PU) Z (20k PU)		
MMC1_RCLK I/O V1P8 GPIOMV, HS Z (20k PD) Z MMC1_RESET_N I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS Z Z SD2_D[2:0] I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_D[3]_CD_N I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CMD I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CLK I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU)	Z (20k PU)	
MMC1_RCLK I/O V1P8 GPIOMV, HS Z (20k PD) Z MMC1_RESET_N I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS Z Z SD2_D[2:0] I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_D[3]_CD_N I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CMD I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CLK I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU)		ind
MMC1_RCLK I/O V1P8 GPIOMV, HS Z (20k PD) Z MMC1_RESET_N I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS Z Z SD2_D[2:0] I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_D[3]_CD_N I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CMD I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CLK I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU)	Z (20k PU)	edu
MMC1_RESET_N I/O V1P8 GPIOMV, HS Z Z MMC1_RCOMP I/O V1P8 GPIOMV, HS, RCOMP Z Z SD2_D[2:0] I/O V1P8 GPIOMV, HS Z Z SD2_D[3]_CD_N I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_D[3]_CD_N I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CMD I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CLK I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8 GPIOMV, HS, CLK O (20k PD) O SD3_D[3:0] I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU)	0 (20k PD)	tined und
MMC1_RCOMP I/O V1P8 GPIOMV, HS, RCOMP Z Z Z SD2_D[2:0] I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) Z (20k PU) SD2_D[3]_CD_N I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CMD I/O V1P8 GPIOMV, HS Z (20k PU) Z (20k PU) SD2_CLK I/O V1P8 GPIOMV, HS, CLK 0 (20k PD) 0 SD3_D[3:0] I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU) SD3_D[3:0] I/O V1P8/ GPIOHV, HS Z (20k PU) Z (20k PU)	Zeò	
SD3_D[3:0] I/O V1P8/ V3P3 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ V3P3 CPIOHV, HS Z (20k PU) Z (20k PU)	Z	
SD3_D[3:0] I/O V1P8/ V3P3 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ V3P3 CPIOHV, HS Z (20k PU) Z (20k PU)	ed un'z	
SD3_D[3:0] I/O V1P8/ V3P3 GPIOHV, HS Z (20k PU) Z (20k PU)	Z (20k PU)	
SD3_D[3:0] I/O V1P8/ V3P3 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ V3P3 CPIOHV, HS Z (20k PU) Z (20k PU)	Z (20k PU)	
SD3_D[3:0] I/O V1P8/ V3P3 GPIOHV, HS Z (20k PU) Z (20k PU) SD3_CMD I/O V1P8/ V3P3 CPIOHV, HS Z (20k PU) Z (20k PU)	Z (20k PU)	dui
	0	efined un
V3P3 V3P3 SD3_PWREN_N I/O V1P8 GPIOMV, HS 1 (20k PD) 1 SD3_CLK I/O V1P8/ GPIOHV, HS, 0 (20k PD) 0	Z (20k PU)	
SD3_PWREN_N I/O V1P8 GPIOMV, HS 1 (20k PD) 1 SD3_CLK I/O V1P8/ GPIOHV, HS, 0 (20k PD) 0 V3P3 CLK CLK 0 0 0	Z (20k PU)	
SD3_CLK I/O V1P8/ GPIOHV, HS, 0 (20k PD) 0 V3P3 CLK CLK 0	in ^{er -}	
	0	
SD3_RCOMP I/O V1P8/ V3P3 GPIOHV, HS, RCOMP Z Z	Z	Jefined u
SD3_1P8_EN I/O V1P8 GPIOMV, HS 0 (20k PD) 0	-	
SD3_CD_N I/O V1P8 GPIOMV, HS Input (20k PU) Input (20k PU	U) Input (20k PU)	
ed undefined under undefined under ode	stined undefit.	
SD3_CD_N I/O V1P8 GPIOMV, HS Input (20k PU) Input (20k PU) 36	Datasheet	lefined
undefined un	sined un	
36 defined w	Datasheet	
tined under under	Alla	



defined undefined undefined ndefined undefined High Speed UART Interface Signals 2.11 defined

Table 20. **High Speed UART Interface Signals**

	fined				ed De	efault Buffer Sta	ate a un	
		Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
unden	UART1_DATAIN	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
ined undefined	UART1_DATAOUT	I/O	V1P8	GPIOMV, MS	1 (20k PU)	d uno1	1	ndefine
	UART1_RTS_N	I/O	V1P8	GPIOMV, MS	1 (20k PU)	1	1	1efiner
	UART1_CTS_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
ed	UART2_DATAIN	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
fined undefined	UART2_DATAOUT	I/O	V1P8	GPIOMV, MS	1 (20k PU)	1 sined	1	
	UART2_RTS_N	I/O	V1P8	GPIOMV, MS	1 (20k PU)	4 Undern	1	
	UART2_CTS_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
efined una		ed '	under			d undefine		
efined und	ad undefil	ned	under		undefi	ned undefine		defin
efined und	undefined undefi	ned	under	6	efined undefi	ned undefine	atined	undefin
lefined und	ed undefined undefi	ned	unden	ned und	efined undefi	ned undefine	ed undefined	undefir
efined undefin	ed undefined undefined	ned	unden	ned und	efined undefi	ned undefine	ed undefined	undefit
defined undefin	ed undefined undefi	ned	unden	ned und	efined undefi	ined undefine	ed undefined	undefil
defined undefind	ed undefined undefi	ned	unden	ned und	efined undefi	ned undefine	ed undefined	undefit
defined undefind	UART2_CTS_N	ned	unden	ned und	efined undefi	med undefine	ed undefined	undefir
Betimed undering	UART2_RTS_N UART2_CTS_N UART2_CTS_N UART2_CTS_N	ned	unden	ned und	efined undefi	ned undefine	ed undefined	undefit



ndefined unde 2.12

Table 21.

	d und	efine			ndefi	ned		ndefined
in	tel red und			und	efined undefi	PI	hysical Interfaces	
ned undefine	-		26			ned undefine	d unt	
Table	e 21. I ² C Interf	Sin		ignalo		ined un		stined
	stineo				ed un D	efault Buffer Sta	ite	IUUG
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	SOix	
define	I2C0_DATA	I/O	V1P8	GPIOMV, MS, I2C	Z (1k PU, OD)	Z (1k PU, OD)	Z (1k PU, OD)	
ned une	I2C0_CLK	I/O	V1P8	GPIOMV, MS, I2C	Z (1k PU, OD)	Z (1k PU, OD)	Z (1k PU, OD)	
tined undefine	I2C1_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	I2C1_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	Indefili
	I2C2_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
efin	I2C2_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
afined undefin	I2C3_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
stine	I2C3_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	I2C4_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	defin
	I2C4_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	Jun -
	I2C5_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
Jeffined undefil	I2C5_CLK	I/O	V1P8	GRIOMV	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
lefiner	I2C6_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	I2C6_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	Aefil
defined undef	I2C6_CLK			undefined	undefinedus	ade	Z (20k PU, OD) Z (20k PU, OD) Z (20k PU, OD) Datasheet	ed unit
define	adefined	und	afineo .		untined ut	ndefined un		ed undefi
38 A unde	tined une			undefined	unde.		Datasheet	
efiner			ined			d uno		

ndefined undefin NFC I²C Interface Signals 2.13

Table 22. NFC I²C Interface Signals

				ed U. D	efault Buffer Sta	te di	
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
NFC_I2C_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
NFC_I2C_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
GPIO_ALERT	I/O	V1P8	GPIOMV, MS	0 (20k PU)	neo o	0	ined un
d un ^o Signa	ls		ed uni	Je _{µ1} ,	erface (SP	I)	nden
le 23. PCU- Fas	t Seria	l Periph	eral Interf	ace (SPI) Signa	als	,0	
		d une			Default Buffer S	tate	

define

PCU- Fast Serial Peripheral Interface (SPI) 2.14

stined un	^O Signals			d undern		face (SPI)	undefined
ed und Table 23	8. PCU- Fast Seria	i Perip مں ر	oheral I	nterface		fault Buffer Stat	
Hefined und Cable 23	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
	FST_SPI_CLK	I/O	V1P8	GPIOMV, HS	0 (20k PU)	Output	Output
edu	FST_SPI_CS[0]_N	I/O	V1P8	GPIOMV, HS	1 (20k PU)	Output	Output
	FST_SPI_CS[1]_N	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Output	Output
ndefined undefined u	FST_SPI_CS[2]_N	I/O	V1P8	GPIOMV, HS	1 (20k PU)	Output	Output
nde.	FST_SPI_D[3:0]	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)
undefined undefined	undefined undef	ined '		led unde	fil.	ned undefine	d undefin

undefined u



PCU - Real Time Clock (RTC) Interface Signals 2.15

					Defa	ault Buffer S	tate
ndefined undefined uni	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	SOix
4 under.	RTC_X1	Ι	V3P3	RTC PHY	Input (Crystal)	Input (Crystal)	Input (Crystal)
defined	RTC_X2	00	V3P3	RTC PHY	Output (Crystal)	Output (Crystal)	Output (Crystal)
	RTC_RST_N	Ι	V3P3	RTC PHY	Input	Input	Input
	RTC_TEST_N	Ι	V3P3	RTC PHY	Input	Input	Input
	RTC_EXTPAD	0	V3P3	RTC PHY	Input	Input	Input
and un	DCII Low			4 under			5n.

Table 24. PCU - Real Time Clock (RTC) Interface Signals

2.16 undefined une

PCU - Low Pin Count (LPC) Bridge Interface Signals atined underin

Table 25. PCU - LPC Bridge Interface Signals

aned t	-		une			d under.		
undefined L Table 2	5. PCU - LPC Brid	lge Iı	nterface	Signals		sined u		d un
	d uno				D	efault Buffer Sta	ate	define
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	d undefined un
define	LPC_AD[3:0]	I/O	V3P3/ V1P8	GPIOHV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
ed unc	LPC_FRAME_N	I/O	V3P3/ V1P8	GPIOHV, HS	1 (20k PU)	1 def	1	
a undefined undefined	LPC_SERIRQ	I/O	V1P8	GPIOHV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)	ed undefined u
9 n.	LPC_CLKRUN_N	I/O	V3P3/ V1P8	GPIOHV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)	ndefine
	LPC_CLKOUT[0]	I/O	V3P3/ V1P8	GPIOHV, HS	0 (20k PU)	Clock	0	ed un
Sine	LPC_CLKOUT[1]	I/O	V3P3/ V1P8	GPIOHV, HS	Input (20k PD)	Input	Input	
d under	LPC_RCOMP	I/O	V3P3/ V1P8	GPIOHV, HS	Z	Z	inec z	
40 40	od un	defin	edu		undefined un	defined uns		ned undefined
	odefinee				lefined t			ned une
40	led un.			, d	INOC		Datashee	et
thed under			dunn	Jefines		mo	etined un	
16111		611	ner			du.		



stined undefined undefined ndefined undefin **PCU - Power Management Controller (PMC)** 2.17 **Interface Signals**

Table 26. PCU - Power Management Controller (PMC) Interface Signals

	udefili			Aefil	De	efault Buffer Sta	ate sined	
tined undefined	Signal Name	Dir	Plat. Power	d Type	Pwrgood Assert State	Resetout Deassert State	under S0ix	
ined un-	PMC_PLTRST_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	Indefille	1	
	PMC_PWRBTN_N	I	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	defined
	PMC_RSTBTN_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	ndefill.
	PMC_SUSPWRDNACK	I/O	V1P8	GPIOMV, MS	0 (20k PD)	0 (20k PD)	0 (20k PD)	
efined	PMC_SUS_STAT_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	1	unden	
tined undefined	PMC_SUSCLK[0]	I/O	V1P8	GPIOMV, MS	0 (20k PD)	32 KHz Clock	32 KHz Clock	
ine	PMC_SLP_S4_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	ed ^{un1}	1	
	PMC_SLP_S0ix_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	1	0 at S0ix2	ndefiner
	PMC_ACPRESENT	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)	711-
	PMC_BATLOW_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
stined undefine	PMC_WAKE_N	I/O	V1P8	GPIOMV,	Input (20k PU)	Input (20k PU)	Input (20k PU)	
	PMC_CORE_PWROK	IO	V3P3	RTC PHY	Input	Input	Input	
	PMC_RSMRST_N	I	V3P3	RTC PHY	Input	Input	Input	
	PMC_RSMRST_N			a und	atined under		Input Input Input	undefine
defined undefin			d undef			wed undefin	ed u.	
	d undefined unde				Jefined undef	<i>'I</i>	teriner	d undefin
Datashee	20			sined un			ed unos 41	
ed unos			unde	<u> </u>		defi	No.	



Serial Peripheral Interface (SPI) Signals 2.18

				Default Buffer State						
Signal Name	Dir	Plat. Power	Type	Pwrgood Assert State	Resetout Deassert State	S0ix				
SPI[1,2,3]_CLK	I/O	V1P8	GPIOMV, HS	0 (20k PU)	0	0				
SPI[1,2,3]_CS[0:1]_N	I/O	V1P8	GPIOMV, HS	1 (20k PU)	, nuger,	1				
SPI[1,2,3]_MOSI	I/O	V1P8	GPIOMV, HS	0 (20k PU)	0	0				
SPI[1,2,3]_MISO	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Input (20k PD)	Input				
	SPI[1,2,3]_CLK SPI[1,2,3]_CS[0:1]_N SPI[1,2,3]_MOSI	SPI[1,2,3]_CLK I/O SPI[1,2,3]_CS[0:1 I/O]_N I/O SPI[1,2,3]_MOSI I/O	Signal Name Dir Power SPI[1,2,3]_CLK I/O V1P8 SPI[1,2,3]_CS[0:1] I/O V1P8 _N SPI[1,2,3]_MOSI I/O V1P8	Signal Name Dir Power Type SPI[1,2,3]_CLK I/O V1P8 GPIOMV, HS SPI[1,2,3]_CS[0:1] I/O V1P8 GPIOMV, HS N SPI[1,2,3]_MOSI I/O V1P8 GPIOMV, HS	Signal Name Dir Plat. Power Type Pwrgood Assert State SPI[1,2,3]_CLK I/O V1P8 GPIOMV, HS 0 (20k PU) SPI[1,2,3]_CS[0:1 I/O V1P8 GPIOMV, HS 1 (20k PU) SPI[1,2,3]_MOSI I/O V1P8 GPIOMV, HS 0 (20k PU)	Signal NameDirPlat. PowerTypePwrgood Assert StateResetout Deassert StateSPI[1,2,3]_CLKI/OV1P8GPIOMV, HS0 (20k PU)0SPI[1,2,3]_CS[0:1]I/OV1P8GPIOMV, HS1 (20k PU)1J_NI/OV1P8GPIOMV, HS0 (20k PU)0SPI[1,2,3]_MOSII/OV1P8GPIOMV, HS0 (20k PU)0				

Table 27. Serial Peripheral Interface (SPI) Signals

JTAG Interface Signals 2.19

Table 28. JTAG Interface Signals

2.19	JTAG Ir	nter	face	Signals	stined		defined		
Table 2	8. JTAG Interf	ace S	Signals	Jefined U.	Default Buffer State				
efined under	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix		
	JTAG_TCK	I/O	V1P8	GPIOMV, MS	Input (5k PD)	Input (5k PD)	Input (5k PD)		
	JTAG_TDI	I/O	V1P8	GPIOMV, MS	Input (5k PU)	Input (5k PU)	Input (5k PU)		
	JTAG_TDO	I/O	V1P8	GPIOMV, MS	e Z	Z	Z sin		
	JTAG_TMS	I/O	V1P8	GPIOMV, MS	Input (5k PU)	Input (5k PU)	Input (5k PU)		
define	JTAG_TRST_N	I/O	V1P8	GPIOMV, MS	Input (5k PU)	Input (5k PU)	Input (5k PU)		
Jefined undefine	JTAG_PRDY_N	I/O	V1P8	GPIOMV, MS	Z (5k PU, OD)	Output (5k PU, OD)	Z (5k PU, OD)		
Jefine	JTAG_PREQ_N	I/O	V1P8	GPIOMV, MS	Input (5k PU, OD)	Input (5k PU, OD)	Input (5k PU, OD)		

Integrated Sensor Hub Interface Signals 2.20

Integrated Sensor Hub Interface Signals (Sheet 1 of 2) Table 29.

Inder			6-		De	fault Buffer Sta	ault Buffer State		
ndefined L.	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix		
	ISH_GPIO[7:0]	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Z (20k PU)	Z (20k PU)		
42	led undern.			efined	Indefine		Datashe		
Jefined UI.			ned un			ad unde			



defined undefined undefined ndefined undefined

efined ^{un} Table 2	1efine	<u>}</u> 0			nals (Sheet 2	6		
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	ndefines
du	ISH_GPIO[8]	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
adefinec	ISH_GPIO[9]	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
sined un	ISH_I2C1_SDA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
elli	ISH_I2C1_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	cined
2.21	PWM Inte	erfa	ice Si	ianals	ned unos		24	Indefin
21	Inde			inde			definec	

	ISH_IZCI_SDA	1/0	VIPO	MS, I2C	Input (20k PO)	Z (ZUK PU, UD)	2 (20k P0, 0D)	
Indett.	ISH_I2C1_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	med un
2.21	PWM Inte	erfa	ice Si	ignals	ined unos		sined "	Indefit
Table	e 30. PWM Interface	e Sigı	nal	led uno	D	efault Buffer Sta	d undein	1
undefined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	sined un
	PWM[0]	I/O	V1P8	GPIOMV, MS	0 (20k PD)	0	0	unden
	PWM[1]	I/O	V1P8	GPIOMV, MS	0 (20k PU)	0	0 neo	-
Lefined un2.22	2 SVID Inte	erfa	ice S	ignals		-d undefin	ed und	
d und ^{oo} Table	e 31. SVID Interface	a Sigi	nal			inec	<u> </u>	stined b
				ļ	De	efault Buffer Sta	ate	

undefined un**2.22**

SVID Interface Signals

Table 31. SVID Interface Signal

	ed un.				UNOD	efault Buffer Sta	ate	nden
6	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
ndefine	SVID_DATA	I/O	V1P8	GPIOMV, MS	0	0	1 or Z	
undefined undefine	SVID_CLK	I/O	V1P8	GPIOMV, MS	0	1 or Z	1 or Z	
d under.	SVID_ALERT_N	I/O	V1P8	GPIOMV, MS	Input	Input	Input	sined
	undefined				defined unt		atin	d under.
Datasheet				afined un			d under 43	3
stined unde			ed und	3411.		d undefi	Inec.	

undefinedu



Miscellaneous Signals 2.23

Miscellaneous Signals and Clocks Table 32.

			d undefi	iu.	Phys	sical Interfaces	
Miscellan	eou	is Sig	nals		d undefined		ind
Miscellaneous	Sign	als and	Clocks	ed undefin	efault Buffer Sta	te	indefined L.
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	SOix	
PLT_CLK[0:5]	I/O	V1P8	GPIOMV, MS	0 (20k PD)	Clock (20k PD)	01	
PROCHOT_N	I/O	V1P8	GPIOMV, MS	Z	edurz	Z	ed un
				ined under		6	undefines
	Miscellaneous Signal Name PLT_CLK[0:5] PROCHOT_N NOTE: '0' in S0i2	Miscellaneous Miscellaneous Signa Signal Name Dir PLT_CLK[0:5] I/O PROCHOT_N I/O NOTE: '0' in S0i2 or belo	Miscellaneous Signals and Miscellaneous Signals and Signal Name Dir Plat. Power PLT_CLK[0:5] I/O V1P8	Miscellaneous Signals Miscellaneous Signals and Clocks Signal Name Dir Plat. Type PLT_CLK[0:5] I/O V1P8 GPIOMV, MS PROCHOT_N I/O V1P8 GPIOMV, MS NOTE: '0' in S0i2 or below.	Miscellaneous Signals and Clocks Miscellaneous Signals and Clocks Signal Name Dir Plat. Pwrgood Assert State PLT_CLK[0:5] I/O V1P8 GPIOMV, 0 (20k PD) PROCHOT_N I/O V1P8 GPIOMV, Z MS NOTE: '0' in S0i2 or below. MS MS MS MS	Miscellaneous Signals and Clocks Default Buffer State Signal Name Dir Plat. Pwrgood Resetout Signal Name Dir Plat. Type Pwrgood Resetout Deassert FLT_CLK[0:5] I/O V1P8 GPIOMV, O (20k PD) Clock (20k PD) PROCHOT_N I/O V1P8 GPIOMV, Z Z MS Signal Name Signal Name Signal Name Signal Name Signal Name VIP8 GPIOMV, O (20k PD) Clock (20k PD) Clock (20k PD) NOTE: 'O' in S0i2 or below. MS MS MS	Miscellaneous Signals and Clocks Default Buffer State Signal Name Dir Plat. Pwrgood Resetout Soix Signal Name Dir Plat. Type Pwrgood Resetout Deassert Soix PLT_CLK[0:5] I/O V1P8 GPIOMV, 0 (20k PD) Clock (20k PD) 0 ¹ PROCHOT_N I/O V1P8 GPIOMV, Z Z Z Z NOTE: '0' in S0i2 or below. K K K K K K K K K

2.24 Hardware Straps undefined undefined

All straps are sampled on the rising edge of **PMC_RSMRST_N**.

While PMC_RSMRST_N is low all strap pins are in input mode. Weak pull ups or downs keep straps from floating during this time. Strap values can be changed by driving the strap pins or using stronger pull resistors. Hefined

Table 33. Straps (Sheet 1 of 2)

adefine		stronger pull resistors		be changed by driving the	undefined un
	Signal Name	Purpose	Pull up/Pull Down	Strap Description	Indell
tined un	GPIO_SUS[0] ¹	DDI0 Detect	Weak internal pull down of 20K	DDI0 Detect 0 = DDI0 not enabled 1 = DDI0 enabled	5 [~]
undefined undefined un	GPIO_SUS[1]	DDI1 Detect	Weak internal pull down of 20K	DDI1 Detect 0 = DDI1 not enabled 1 = DDI1 enabled	
d undern.	GPIO_SUS[2]	A16 swap overdrive	Weak internal pull up of 20K	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation	indefined u
edu	GPIO_SUS[3]	DSI Display Detect	Weak internal pull down of 20K	MIPI DSI Detect 0 = DSI not enabled 1 = DSI enabled	3d ""
A undefined undefined u	GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull up of 20K	BIOS Boot Selection 0 = Default 1 = SPI	
d undefine	GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull up of 20K	Security Flash Descriptors 0 = Override 1 = Normal Operation	i afined !
	undefineo		defined un	li).	led unde
44 sined		ed ut		Datasheet	t
Lefined under		ned undefine		d undefineo	



Jeffined undefined undefined ndefined undefined Straps (Sheet 2 of 2) Table 33.

ed un		y unde		define a	
Table 33.	Straps (Sheet 2 of	adefineo		defined un	
Inec. Table 55.	Signal Name	Purpose	Pull up/Pull Down	Strap Description	2
	med under		od undefilt	0 = Supply is 1.25V 1 = Supply is 1.35V	defined
stined undefined undef	GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull up of 20K	This strap also contains PLL LDO 0: supply is 1.25V 1: supply is 1.35V.	
tined	odefined	une	Lefined U	Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI	
		ICLK, USB2, DDI SFR Bypass	Weak internal pull down of 20K	Bypasses LDOs for ICLK 0 = Use LDOs 1 = Bypass LDOs (Supply1.05V on power pins)	ndetti
efined undefined unde	GPIO_SUS[10]	POSM Select	Weak internal pull down of 20K	Selects which POSM (power on state machine) will be observed at time 0 0 = Fuse controller 1 = PMC	
	GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull down of 20K	0 = No Bypass 1 = Bypass	define
6	GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull down of 20K	0 = No Bypass 1 = Bypass	JULY
stined	GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull down of 20K	0 = No Bypass 1 = Bypass	
	NOTE: 1. Ignore this strap at can be used as a G		anism to detect the rel	evant DDI port. This signal	
	ed undefill.		4 undefined		ndefine

NOTE:

.e rek 1. Ignore this strap and use a software mechanism to detect the relevant DDI port. This signal -d as

-she



defined undefined undefined ndefined unde SoC RCOMP List 2.25

Table 34. RCOMP's List (Sheet 1 of 2)

defined		sined un.	ed unde
2.25	SoC RCOMP Lis	st	d undefine
Table 34.	RCOMP's List (Sheet 1	of 2)	adefines
Interface Name	RCOMP Name	Bias	Remarks
DDR3	DDR3_M0_RCOMPPD/ LPDDR3_M0_RCOMPPD	182 Ohm ±1% to Ground	RCOMP pins for DDR3
nder	DDR3_M1_RCOMPPD LPDDR3_M1_RCOMPPD	182 Ohm ±1% to Ground	defineo
MIPI DSI	MDSI_RCOMP	150 Ohm ±1% to Ground	RCOMP pin for MIPI DSI
MIPI CSI	MCSI_RCOMP	150 Ohm ±1% to Ground	RCOMP pin for MIPI CSI
eMMC	MMC1_RCOMP	100 Ohm ±1% to Ground	eMMC, SDIO, FST_SPI RCOMP
SD Card	SD3_RCOMP	80.6 Ohm ±1% to Ground	SD Card contains its own RCOMP as it can be either 1.8V or 3.3V. Special care is needed to perform an RCOMP any time a card is inserted.
LPC	LPC_RCOMP	100 Ohm ±1% to Ground	LPC has its own RCOMP because it can operate at 1.8V or 3.3V.
iCLK	ICLK_ICOMP	2.5k Ohm ±1% to Ground	The calibration will be handled inside the iCLK.
retined r	ICLK_RCOMP	50 Ohm ±1% to Ground	od under
USB2	USB_RCOMP	113 Ohm ±1% to Ground	The calibration will be handled inside USB
USB2 HSIC	USB_HSIC_RCOMP	45 Ohm ±1% to Ground	The calibration is handled inside the USB HSIC.
SSIC	USB_SSIC_RCOMP_P USB_SSIC_RCOMP_N	90 Ohm ±1% Between SSIC RCOMP pads	The calibration is handled inside the USB SSIC.
USB3	USB3_RCOMP_N USB3_RCOMP_P	402 Ohm 1% between RCOMP pads	The calibration is handled inside the USB3.
GPIO	GPIO0_RCOMP	100 Ohm to Ground	Will be shared across all GPIO buffers on the north side of the chip.
PCIE	PCIE_RCOMP_N PCIE_RCOMP_P	402 Ohm 1% between RCOMP pads	The Calibration is handled in PCIE.
46 ndefined	undefilt	defined und	Datasheet

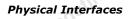




Table 34.	RCOMP's List (Sheet	2 of 2)	ndefinec	
Interface Name	RCOMP Name	Bias	Remarks	ined un
DDI	DDI0_RCOMP_N	402 Ohm 1%	The calibration is handled in DDI	den
ndef	DDI0_RCOMP_P	between RCOMP pads	aned	UI.
ed ui	DDI1_RCOMP_N	402 Ohm 1%	den	
	DDI1_RCOMP_P	between RCOMP pads	ined un	

Table 34. RCOMP's List (Sheet 2 of 2)

undefined unde **GPIO Muxing** 2.26

Not all interfaces can be active at the same time. To provide flexibility, these shared interfaces are muxed with GPIOs.

Note:

All GPIOs default to function as GPIO name at boot. BIOS is responsible for enabling red undefined undefined proper configuration.

	dui	proper co	nfigurat	ion.	un ^c				gein.		
	define	GPIO Nur	nber= G	GPIO pin l	ocation				Un		
Indefined	undefined un Table 35.			ed u.	n which the T4 SoC (S		ntes f 11) « N ^{ed}	undefined			ed un
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	
	ISH_GPIO[8]/ ISH_SPI_CS[0]_N/ I2S5_CLK	BL9	E23		ISH_GPIO[8]	ISH_SPI _CS[0]_ N	I2S5_CLK		Indefin	60	
0	LPC_AD[2]/ ISH_GPIO[14]/ ISH_I2C0_DATA	BP20	SE45	, und	LPC_AD[2]	ISH_GPI O[14]	ISH_I2C0_ DATA	ndefine	0		
y undefin	I2C4_CLK/ DDI0_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	BP34	SW52	160	I2C4_CLK	DDI0_D DC_CLK	DDI2_DDC _CLK	MDSI_DDC _CLK			lined u
	LPC_AD[3]/ ISH_GPIO[15]/ ISH_I2C0_CLK/ SPI2_MOSI	BR21	SE50		LPC_AD[3]	ISH_GPI O[15]	ISH_I2C0_ CLK	SPI2_MOSI	odefi	ned uno	
	PMC_PLT_CLK[4]/ ISH_GPI0[14]/ ISH_I2C0_DATA/ SPI2_MISO	BR7	SE3	dun	PMC_PLT_ CLK[4]	ISH_GPI O[14]	ISH_I2C0_ DATA	SPI2_MISO	ed un		
ed undefin	PMC_PLT_CLK[1]/ ISH_GPIO[11]/ ISH_UART_DATAIN /SPI2_CS[1]_N	BR9	SE2	IUer	PMC_PLT_ CLK[1]	ISH_GPI O[11]	ISH_UART_ DATAIN	SPI2_CS[1]_N		6	etined
	, v	ndefine	L	I		define	0	1		tined un	<u>_</u>
	Datasheet				ed l	71,			d unde	47	
	led undefine				ndefined			ndefil	hed unde		
1641				sineu				dui			

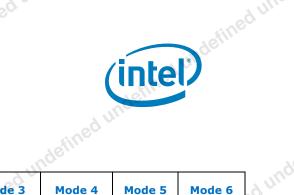
Table 35. Multiplexed Functions - T4 SoC (Sheet 1 of 11)





	ed un	define			undefin	eq .
(intel				undefine		
Table 35.	Multiple	xed Function	ons - T4 S	oC (Sheet	: 2 of 11)	
	-					

	71.	define				defined				10
intel	s) red L			ined und	efinedu		Phy	sical Interi	faces	
defill			-9e				afined	unde		
GPIO Pin Name	Multiplex Package Ball #	ced Fun GPIO #	Mode 0	T4 SoC (S Mode 1	Sheet 2 of Mode 2	f 11) Mode 3	Mode 4	Mode 5	Mode 6]
I2C4_DATA/ DDI2_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	BT32	SW46		I2C4_DAT A	efined	DDI2_DDC _DATA	MDSI_DDC _DATA	1	ed undef	<u>+</u> 0'
PMC_PLT_CLK[5]/ ISH_GPI0[15]/ ISH_I2C0_CLK/ SPI2_MOSI	BT6	SE6		PMC_PLT_ CLK[5]	ISH_GPI O[15]	ISH_I2C0_ CLK	SPI2_MOSI	undein		-
MMC1_RCLK/ MMC1_RESET_N	BU13	SE69	eduit	MMC1_RCL K	MMC1_R ESET_N	-0	unob			
PMC_PLT_CLK[2]/ ISH_GPIO[12]/ ISH_UART_CTS_N/ SPI2_CS[0]_N	BU7	SE7		PMC_PLT_ CLK[2]	ISH_GPI O[12]	ISH_UART_ CTS_N	SPI2_CS[0]_N		d unde	
PMC_PLT_CLK[3]/ ISH_GPIO[13]/ ISH_UART_RTS_N/ SPI2_CLK	BU9	SE4		PMC_PLT_ CLK[3]	ISH_GPI O[13]	ISH_UART_ RTS_N	SPI2_CLK	d undefi	her.	
DDI2_DDC_CLK/ DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/ MDSI_A_TE	E21	N67	ned und	DDI2_DDC _CLK	DDI1_D DC_CLK	UARTO_DA TAOUT	MDSI_DDC _CLK	MDSI_A_ TE		
GPIO_N1/ C0_BPM3_TX/ C1_BPM3_TX	E39	N1			sined	under		CO_BPM3 _TX	C1_BPM3 _TX	6
DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/ MDSI_C_TE	F20	N62		DDI2_DDC _DATA	DDI1_D DC_DAT A	UARTO_DA TAIN	MDSI_DDC _DATA	MDSI_C_ TE	lle.	
DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK	F26	N71	ined ut	DDI0_DDC _CLK	DDI1_D DC_CLK	MDSI_DDC _CLK	ed unot			
GPIO_N2/ C0_BPM2_TX/ C1_BPM2_TX	F38	N2			-0	d under		C0_BPM2 _TX	C1_BPM2 _TX	3.0
GPIO_N4/ C0_BPM0_TX/ C1_BPM0_TX	G39	N4		6	Indefini			CO_BPMO _TX	C1_BPM0 _TX	
DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	H26	N66		DDI0_DDC _DATA	DDI1_D DC_DAT A	MDSI_DDC _DATA	defi	neou		
JTAG2_TMS	J37	N24	stined	JTAG2_TM S		275	ed ut			
48 atmed undefined	undefine	ed uno		e d	undefin	ed undefit		Data	sheet	,0
fined under			ed'	undefine			unde	ineo		



Physical Inter	IALES			-9e	<i>[11</i> .			(inte	
sined				ned undef				Inter	
nder			defi	n-			sineo		
Table 35.	Multiple	xed Fur	ctions -	T4 SoC (S	heet 3 of	F 11)	nder.		<u> </u>
ndefined un Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode
GPIO_N6/ C0_BPM3_TX/ C1_BPM3_TX	J39	N6			tined un	0		CO_BPM3 _TX	C1_BPM _TX
GPIO_N8/ C0_BPM1_TX/ C1_BPM1_TX	К40	N8		ned und			~	C0_BPM1 _TX	C1_BPM _TX
GPIO_N3/ CO_BPM1_TX/ C1_BPM1_TX	B38	N3	d under				Indefine	CO_BPM1 _TX	C1_BPM _TX
ISH_GPIO[13]/ C0_BPM2_TX/ C1_BPM2_TX	C39	N7				ndefineo	ISH_GPIO[13]	C0_BPM2 _TX	C1_BPM _TX
GPIO_N0/ C0_BPM0_TX/ C1_BPM0_TX	D40	N0			efined			CO_BPM0 _TX	C1_BPM _TX
GPIO_CAMERASB0 3	B28	N51		GPIO_CAM ERASB03			2	under	
JTAG_TMS	B34	N34	20	JTAG_TMS	†	+	sine	-	1
PMC_PWRBTN_N	BH10	E8	sq nuor	PMC_PWR		6	unden		
[2]		CE22	 	BTN_N		tine			+
SD3_D[2] PMC_RSTBTN_N	BH18 BH24	SE33 SE76		SD3_D[2] PMC_RSTB	red	Nuge.			d und
UART2_RTS_N	BH26	SW19		TN_N UART2_RT S_N	0e ^{f11} .		<u> </u>	4 undefit	
UART2_DATAIN	BH28	SW17	ed und	UART2_DA			undefine	<u>, , , , , , , , , , , , , , , , , , , </u>	
LPE_I2S0_CLK	BH32	SW31		LPE_I2S0_ CLK		Lefine			
I2C6_CLK/NMI_N	BH34	SW53	<u> </u>	I2C6_CLK	NMI_N	una	+	+	_
I2C2_DATA	BH36	SW62		I2C2_DAT A	ndefined	2 2		Acti	nedun
PMC_BATLOW_N	BH4	E1		PMC_BATL OW_N			i afin	ed une	
LPE_I2S2_FRM	BH40	SW96	nedur	LPE_I2S2_ FRM			d unde		
PMC_SUS_STAT_N	BH6	E2 de		PMC_SUS_ STAT_N		undefin			
	ndefine				Jefine	0.			ined u
Datasheet				ndefined	Julos		ه هر	ned unde	49
ed un				uge.			ndefi		
							- d UI.		

Physical Interfaces Table 35. Multiplexed Functions - T4 SoC (Sheet 3 of 11)





Cincel	Intel				efine		Physical Interfaces				
undefine			nde	tined und		44.)	defined	unoc			
Table 35. GPIO Pin Name	Multiplex Package Ball #	GPIO #	Mode 0	T4 SoC (S Mode 1	Mode 2	f 11) Mode 3	Mode 4	Mode 5	Mode 6		
MMC1_CMD	BJ15	SE23		MMC1_CM D	6	inds.	+	<u> </u>	Indef		
LPC_FRAME_N/ UART0_DATAIN/ SPI2_MISO	BJ19	SE48		LPC_FRAM E_N	UARTO_ DATAIN		SPI2_MISO	ndefin	80.		
GPIO_ALERT/ ISH_GPIO[11]/ ISH_UART_DATAIN	BJ21	SE77	Ind	GPIO_ALE RT	ISH_GPI O[11]	ISH_UART_ DATAIN	define	8.0.			
FST_SPI_D[2]	BJ25	SW0	leo T	FST_SPI_ D[2]			Un				
PMC_SLP_S3_N	BJ3	E0		PMC_SLP_ S3_N	6	undefill			unde		
LPE_I2S1_DATAIN	BJ30	SW37		LPE_I2S1_ DATAIN	defines		<u> </u>	ing in	Ned T		
NFC_I2C_CLK	BJ33	SW54		NFC_I2C_ CLK		<u> </u>		d unde			
UARTO_DATAIN	BJ37	SW77	, uni	Je, j	UART0_ DATAIN	<u> </u>	defin				
PMC_PLTRST_N	BJ5	E5	ned -	PMC_PLTR ST_N		define	0.011				
PMC_WAKE_N	BJ7 BJ7	E10		PMC_WAK E_N	ed	Un	1		4 und		
PMC_SLP_S4_N	BJ9	E9		PMC_SLP_ S4_N	ndefine			Indef	neo		
ISH_GPIO[6]/ I2S4_DATAOUT	BK10	E25		ISH_GPIO[6]		I2S4_DATA OUT	fil	eò			
MMC1_D[3]	BK12	SE26	ned ut	MMC1_D[3]		<u> </u>	d unde	<u> </u>			
MMC1_D[1]	BK14	SE24		MMC1_D[1]		defin		<u>+</u>			
SD3_D[0]	BK16	SE35		SD3_D[0]		dun		<u> </u>	un'		
SPI1_MOSI	BK18	SE64		SPI1_MOS I	defin				tined		
LPC_CLKOUT[0]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	ВК20	SE51		LPC_CLKO UT[0]	ISH_GPI O[10]		ISH_UART _DATAOUT	ned uno			
PMC_SUSPWRDNA CK	BK22	SE83	stined	PMC_SUSP WRDNACK		infile.	red unot				
50 med undefined	Indefine	d un		wrdnack	defin	ed under			efined un		
50 indefined				tefined	une		od undef	Datas	sheet		
ned u.			6	unos			unde	/			

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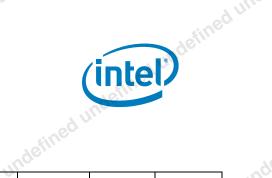
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ndefinec			Acti	ned u.			eined I	The	
Table 35.	Multiple	xed Fur	ictions -	T4 SoC (S	iheet 5 of	F 11)	ndeir		
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode
FST_SPI_D[1]	BK26	SW5		FST_SPI_ D[1]	ed un	0			unde
UART2_DATAOUT	BK28	SW21		UART2_DA TAOUT				define	0
LPE_I2S0_FRM	BK32	SW35		LPE_I2S0_ FRM			ined	<u></u>	
I2C5_CLK	BK34	SW50	unde	I2C5_CLK	+	+	-defin.	+	+
SPI3_MOSI	BK36	SW82	,0		SPI3_MO SI	sined			+
LPE_I2S2_CLK	BK38	SW92	<u> </u>	LPE_I2S2_ CLK	ن بر	ndei			bn.
PMC_ACPRESENT	BK4	E4		PMC_ACPR ESENT	efinec			defin	39
LPE_I2S2_DATAOU T	BK40	SW97		LPE_I2S2_ DATAOUT			e	Un	
ISH_GPIO[9]/ ISH_SPI_MISO/ I2S5_FS	ВК8	E20	ed unde	ISH_GPIO[9]	ISH_SPI _MISO	I2S5_FS	undefille		
SD2_CLK	BL11	SE19	<u> </u>	SD2_CLK	<u> </u>	inet inet	†	1	1
SD3_D[3]	BL15	SE32	†	SD3_D[3]		nde	1	1	1
SD3_CLK	BL17	SE31	<u>+</u> ,	SD3_CLK	ed		1	1	201
SPI1_MISO	BL19	SE60		SPI1_MIS O	detine			defit	e.
LPC_CLKRUN_N/ UART0_DATAOUT/ SPI2_CLK	BL21	SE46	à	LPC_CLKR UN_N	UART0_ DATAOU T		SPI2_CLK	d un	
FST_SPI_D[3]	BL25	SW3	hed un	FST_SPI_ D[3]			y under		
UART2_CTS_N	BL27	SW22		UART2_CT S_N		undefine			
PMC_SLP_SOIX_N	BL3	E3		PMC_SLP_ SOIX_N	ndefined			Acti	nedu
I2C6_DATA/ SD3_WP	BL33	SW49		I2C6_DAT A	SD3_WP		Air a	ed une	
I2C2_CLK	BL35	SW66	dun	I2C2_CLK			Inde		
UART0_DATAOUT/ SPI3_CLK	BL37	SW79	ine		SPI3_CL K	UART0_DA TAOUT	30.		
	Indefined) UN			efine	d unos			ned
Datasheet	<u>}</u> ,			ndefined	JUUGE			ned unde	51
ed un.			ed ut	nac			undefi		

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(inte	shea -			and the	stined u		Phy	sical Interi	Faces		
defin			20	fined un.				unoc			
Table 35.	Multiple	xed Fun	ictions -	T4 SoC (S	heet 6 of	11)	Inder				
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6		
LPE_I2S2_DATAIN	BL39	SW94		LPE_I2S2_ DATAIN	6	inc.			Inde		
MMC1_D[0]	BM12	SE17		MMC1_D[0]	efine			defin	20		
MMC1_D[2]	BM14	SE20		MMC1_D[2]				JUNC			
ISH_GPIO[7]/ I2S4_DATAIN	BM2	E16	d und	ISH_GPIO[7]		I2S4_DATA IN	ndefine				
LPC_CLKOUT[1]/ ISH_GPIO[11]/ ISH_UART_DATAIN	BM20	SE49	60	LPC_CLKO UT[1]	ISH_GPI O[11]	terined	ISH_UART _DATAIN				
LPC_SERIRQ/ SPI2_CS[0]_N	BM24	SE79		LPC_SERIR Q	ed an	unoc	SPI2_CS[0]_N		dunde		
LPE_I2S0_DATAOU T	BM32	SW30		LPE_I2S0_ DATAOUT	deti			of i	Neu		
SPI3_CS[0]_N	BM38	SW76		Sineo	~	SPI3_CS[0]_N		ad unac			
ISH_GPIO[3]/ I2S3_DATAIN	BM4	E15	dun	ISH_GPIO[3]		I2S3_DATA IN	indefin				
PMC_SUSCLK[0]	BM6	E6 Undefi	nee	PMC_SUSC LK[0]		define	b				
ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	BM8	E26		ISH_I2C1_ DATA	ISH_SPI _MOSI	I2S5_DATA OUT			ined und		
SD2_CMD	BN11	SE22		SD2_CMD	00-			nde			
MMC1_CLK	BN15	SE16		MMC1_CLK				edu			
SPI1_CLK FST_SPI_D[0]	BN19 BN25	SE62 SW1	ed uf	SPI1_CLK FST_SPI_ D[0]			4 Undefil				
ISH_I2C1_CLK/ ISH_SPI_CLK/ I2S5_DATAIN	BN3	E17de		ISH_I2C1_ CLK	ISH_SPI _CLK	I2S5_DATA IN	20				
NFC_I2C_DATA	BN33	SW51		NFC_I2C_ DATA	Lefine	¢ ¯			ined un		
SPI3_MISO	BN37	SW81		ed	SPI3_MI SO			a unde			
ISH_GPIO[1]/ I2S3_FS	BN5	E18		ISH_GPIO[1]		I2S3_FS	Jefi	ner			
SD2_D[3]_CD_N	BP12	SE15	fined v	SD2_D[3] _CD_N			ed une				
MMC1_D[6]	BP14	SE63		MMC1_D[6]		indefin					
52 to the second	undefine	,-]	undefin	ed -		Data	sheet		
ined u.			red	uno			d unde				



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Physical Inte	rfaces			ned undef	ined un			inte	e) de
Table 35. GPIO Pin Name							lefined !	Inc	-
Table 35. GPIO Pin Name	Multiple: Package Ball #	xed Fur GPIO #	Mode 0	T4 SoC (S Mode 1	heet 7 of Mode 2	f 11) Mode 3	Mode 4	Mode 5	Mode
SD3_D[1]	BP16	# SE30		SD3_D[1]		dell.			26
USB_OC[0]_N	BP22	SE80		USB_OC[0]_N	tined un				d una
FST_SPI_CLK	BP24	SW2		FST_SPI_C LK				undefill	
LPE_I2S1_DATAOU T	BP28	SW34	nde	LPE_I2S1_ DATAOUT			defineo		
I2C1_CLK	BP36	SW63	9.2	I2C1_CLK		~	10-		<u> </u>
GPIO_SW93 ISH_GPIO[5]/ I2S4_FS	BP38 BP4	SW93 E19		ISH_GPIO[5]		I2S4_FS			10
PMC_PLT_CLK[0]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	BP8	SE0		PMC_PLT_ CLK[0]	ISH_GPI O[10]	ISH_UART_ DATAOUT		defin	ed uno
SD2_D[1]	BR11	SE18		SD2_D[1]				, ville	
MMC1_D[4]	BR13	SE67	4 unde	MMC1_D[4]			ndefine		
SD3_CMD	BR15	SE34	S.C.	SD3_CMD		6	0.1		
SPI1_CS[1]_N	BR17	SE66		SPI1_CS[1]_N		ndefine			
LPC_AD[1]/ ISH_GPIO[13]/ ISH_UART_RTS_N	BR19	SE52		LPC_AD[1]	ISH_GPI O[13]	<i>v</i> .	ISH_UART _RTS_N	611	ed un
FST_SPI_CS[1]_N	BR23	SW4		FST_SPI_C S[1]_N	<u></u>			4 under	
UART1_RTS_N	BR25	SW15	d und	UART1_RT S_N			undefine	3~	
UART1_CTS_N	BR27	SW18	10	UART1_CT S_N		define	0.		
ISH_GPIO[0]/ I2S3_CLK	BR3	E21		ISH_GPIO[0]	sined	I2S3_CLK			ed un
LPE_I2S1_CLK	BR30	SW32		LPE_I2S1_ CLK	Iger.			indef	Nue -
I2C5_DATA	BR33	SW45	.0	I2C5_DAT A			defin	ed T	
I2C1_DATA	BR35	SW60	ined u	I2C1_DAT A		nia	d unu		
	ndefined	unu	1	A	sine	d under.	<u>I</u>	1	tined u
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ed undefinite				ndefine				nea	
			. ed				4 UM		





GPIO Pin Name ISH_GPIO[12]/ ISH_UART_CTS_N	Multiplex Package Ball # BR37			ined und	stineu		Phy	sical Interf	aces
Table 35.IGPIO Pin NameIISH_GPIO[12]/ ISH_UART_CTS_NI	Multiple> Package Ball #	ced Fun		ined und					
GPIO Pin Name I ISH_GPIO[12]/ ISH_UART_CTS_N I	Multiple> Package Ball #	ced Fun		tined				dein	
ISH_GPIO[12]/	Package Ball #	GPIO					6	Un	
ISH_GPIO[12]/	Package Ball #	GPIO	ictions -				define		
ISH_GPIO[12]/			Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
-		SW75			ISH_GPI	ISH_UART_			96
	PP20	<u> </u>			0[12]	CTS_N			JUIL -
N	BR39	SW90		PCIE_CLK REQ[0]_N	le _t ,			ning.	6-
SD2_D[0]	BT10	SE25		SD2_D[0]				unde	
MMC1_D[7]	BT14	SE68	6	MMC1_D[7]			stine		
SPI1_CS[0]_N	BT18	SE61	edun	SPI1_CS[0]_N		~	unde		
ISH_GPIO[2]/ I2S3_DATAOUT	BT2	E24	•	ISH_GPIO[2]		I2S3_DATA OUT	,		
	BT22	SE85		SD3_1P8_ EN	ned	U.L.			d und
UART1_DATAIN/ UART0_DATAIN	BT26	SW16		UART1_DA TAIN	UARTO_ DATAIN			Indefi	1.CV
I2C0_CLK	BT36	SW65		I2C0_CLK				9	
· • •	BT4	E22	ed un	ISH_GPIO[4]		I2S4_CLK	underin		
	BT40	SW95	00	-	SD3_WP	eine			
	BU11	SE21		SD2_D[2]	_	detti			
	BU15	SE65		MMC1_D[5]	the character	U.C.			dun
SD3_CD_N	BU17	SE81		SD3_CD_N	det				Iner I
LPC_AD[0]/ ISH_GPIO[12]/ ISH_UART_CTS_N	BU19	SE47		LPC_AD[0]	ISH_GPI O[12]		ISH_UART _CTS_N	ed unde	
USB_OC[1]_N	BU21	SE75	ed un	USB_OC[1]_N			undeili		
SD3_PWREN_N	BU23	SE78	In	SD3_PWR EN_N		10fine	<u>,0</u>		
FST_SPI_CS[0]_N	BU25	SW6		FST_SPI_C S[0]_N		d unu			Jur
	BU27	SW20		UART1_DA TAOUT	UART0_ DATAOU T			inde	tinec
									+
UART0_DATAOUT	BU30	SW33		LPE_I2S0_ DATAIN				neu	

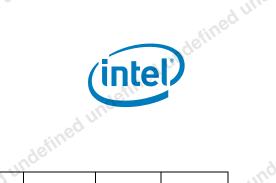


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Table 35.			9e1				lefined !		
Table 35.	Multiple	xed Fun	ctions -	T4 SoC (S	heet 9 of	11)	nde.	T	I
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode
I2C0_DATA	BU35	SW61		I2C0_DAT A	ined un	0			Junde
GPIO_SW78	BU37	SW78		di				1efine	
PCIE_CLKREQ[1]_ N	BU39	SW91	ŝ	PCIE_CLK REQ[1]_N			60	unat	
PWM[1]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	BU5	SE1	d unde	PWM[1]	ISH_GPI O[10]	ISH_UART_ DATAOUT	ndefine		
FST_SPI_CS[2]_N	BV24	SW7		FST_SPI_C S[2]_N		ndefill			
LPE_I2S1_FRM	BV28	SW36		LPE_I2S1_ FRM	stined				dunu
I2C3_CLK	BV34	SW67		I2C3_CLK				detin	
MMC1_RESET_N/ SPI3_CS[1]_N	BV38	SW80	10	tineo	MMC1_R ESET_N	SPI3_CS[1]_N	ti ned	UL	
PWM[0]	BV4	SE5	, uno.	PWM[0]			der		
DDI2_HPD	C21	N68	20.	DDI2_HPD		_>	01.		
GPIO_CAMERASB0 7	C27	N54		GPIO_CAM ERASB07		defines			
GPIO_CAMERASB0 4	C30	N56		GPIO_CAM ERASB04	ed				d und
SVID_ALERT_N	C33	N38		SVID_ALE RT_N	Jet.			defil	6
GPIO_SUS5/ PMC_SUSCLK[1]	C35	N20		PMC_SUSC LK[1]			e a construction de la construcción de la construcc	dun	
GPIO_SUS3/ JTAG2_TDI	C37	N17	od unc	JTAG2_TDI			unden		
GPIO_CAMERASB1 0	D26	N50	10	GPIO_CAM ERASB10		lefiner			
SVID_DATA	D32	N33	SVID_D ATA		60	unoc			nu.
GPIO_SUS6/ PMC_SUSCLK[2]	D36	N25		PMC_SUSC LK[2]	define			10th	neo
DDI1_HPD	E25	N64		DDI1_HPD				uno	
GPIO_CAMERASB0 6	E27	N49		GPIO_CAM ERASB06			1efin	eo	
GPIO_CAMERASB0	E30	N46	nedu	GPIO_CAM ERASB02			d unos	ned unde	
2 JTAG_TDI		N41	· ·	JTAG_TDI	· · · · · · · · · · · · · · · · · · ·				

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	(intel) ed undefine					define			
(intel	3) neu			tined und	efined u		Phy	sical Inter	Faces
undefit			-9e				defined	unde	
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	T4 SoC (S Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
JTAG_TRST_N	E35	N30		JTAG_TRS T_N		inde.			nde
GPIO_SUS0	E37	N15		1_IN	sineu				80 U.
DDI0_VDDEN	F22	N72		DDI0_VDD EN				undefin	
GPIO_CAMERASB1 1	F28	N55	6	GPIO_CAM ERASB11			efine	¢	
SVID_CLK	F32	N40	duin	SVID_CLK			inde		
JTAG_TCK	F34	N31		JTAG_TCK		inec			
GPIO_SUS8	F36	N23		GPIO_SUS 8		undern			be
GPIO_CAMERASB0 5	G27	N45		GPIO_CAM ERASB05	<i>lefineo</i>			4	ned un.
JTAG_PRDY_N	G33	N37		JTAG_PRD Y_N				under	
GPIO_SUS4/ JTAG2_TDO	G37	N22		JTAG2_TD O			1efin	9 ⁰	
DDI1_VDDEN/ MDSI_DDC_DATA	H22	N69	ned u.	DDI1_VDD EN	MDSI_D DC_DAT A		d una		
PROCHOT_N	H32	N32		PROCHOT_ N		undefini			50
JTAG_PREQ_N	H34	N26		JTAG_PRE Q_N	Jefine				ined un
GPIO_DFX4	H38	N5		20	<u> </u>			nde	
DDI1_BKLTEN/ MDSI_DDC_CLK	J21	N70		DDI1_BKL TEN	MDSI_D DC_CLK			ed u	
GPIO_CAMERASB0 9	J27	N52	ned ur	GPIO_CAM ERASB09			d unde.		
GPIO_CAMERASB0 0	J30	N48		GPIO_CAM ERASB00		defin	8°.		
JTAG_TDO	J33	N39		JTAG_TDO		dum			22.
GPIO_SUS9	J35	N27		GPIO_SUS 9	define				tined L
DDI1_BKLTCTL/ MDSI_A_TE/ MDSI_C_TE	K20	N63		DDI1_BKL TCTL	10-	MDSI_A_T E	MDSI_C_T E	sed und	
DDI0_BKLTCTL	K22	N65	~~~	DDI0_BKL TCTL			indef	· · · · · · · · · · · · · · · · · · ·	
DDI0_HPD	K26	N61	finer	DDI0_HPD		a al	ed		
GPIO_CAMERASB0 8	K28	N47		GPIO_CAM ERASB08		undefi	· ·		
56 56	undefin			ERASB08	undefin	60		Data	sheet
ined un			60	unoc			unde	tined ut.	



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ined	Indefined U. Table 35.	Multiple	xed Fun	ctions -	ned unas	heet 11 c	of 11)	defined	men		
ndefine	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	ed und
	GPIO_CAMERASB0 1	К32	N53		GPIO_CAM ERASB01	ed un	0			unden	
	GPIO_SUS10	К34	N16		GPIO_SUS 10	(inc			Jefine	0	
	GPIO_SUS7/ PMC_SUSCLK[3]	K36	N18		PMC_SUSC LK[3]			ood	uno		
red	GPIO_SUS1/ JTAG2_TCK	K38	N19	y nude	JTAG2_TC K			ndefine			
Indefill	DDI0_BKLTEN	L21	N60	5_	DDI0_BKL TEN		sined				ed un
~	Table 36.	Multiple	xed Fun	octions -	T3 SoC (S	heet 1 of	9)		~~~	ed undef	11
	GPIO Pin	Package	GPI	D Mode	0 Mode	1 Mode	2 Mode 3	Mode 4	Mode 5	Mode 6	

Jefined undefined undefined **T4 SoC** (Sheet 11 of 11) Table 35 **Multiplexed Functions**

Table 36. Multiplexed Functions - T3 SoC (Sheet 1 of 9)

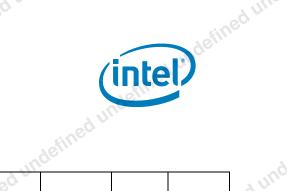
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	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	
defined	DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK	A10	N71	unde	DDI0_DD C_CLK	DDI1_DD C_CLK	MDSI_D DC_CLK	Indefin			, un
uno	GPIO_SE79	AA13	SE79			nu	Jefine			6	efineo
	I2C4_CLK/ DDI1_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	AB17	SW52		I2C4_CLK	DDI1_DD C_CLK	DDI2_D DC_CLK	MDSI_DDC _CLK	ndefil	ned uno	
	I2C4_DATA/ DDI1_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	AB18	SW46	undefi	I2C4_DA TA	DDI1_DD C_DATA	DDI2_D DC_DATA	MDSI_DDC _DATA	0.		
d undefin.	PMC_PLT_CLK[3]/ ISH_GPIO[13]/ ISH_UART_RTS_N/ SPI2_CLK	AB4	SE4		PMC_PLT _CLK[3]	ISH_GPI O[13]	ISH_UAR T_RTS_N	SPI2_CLK			Jefined U
	PMC_PLT_CLK[4]/ ISH_GPIO[14]/ ISH_I2C0_DATA/ SPI2_MISO	AC3	SE3		PMC_PLT _CLK[4]	ISH_GPI O[14]	ISH_I2C 0_DATA	SPI2_MIS O	undef	ined un	
ei (PMC_PLT_CLK[2]/ ISH_GPIO[12]/ ISH_UART_CTS_N/ SPI2_CS[0]_N	AC4	SE7	d undef	PMC_PLT _CLK[2]	ISH_GPI O[12]	ISH_UAR T_CTS_N	SPI2_CS[0]_N	0		
d under	PMC_PLT_CLK[5]/ ISH_GPIO[15]/ ISH_I2C0_CLK/ SPI2_MOSI	AE3	SE6		PMC_PLT _CLK[5]	ISH_GPI O[15]	ISH_I2C 0_CLK	SPI2_MOS I			defined
I		ndefin		1		definer				fined W	<u> </u>
	Datasheet				ned un				d unde	57	
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	define				sq n,			6	unos		
ined	Table 36.	Multiplexe	d Functi	ons - T3	SoC (She	eet 2 of 9))	ndefine			
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	fined u
	MMC1_RCLK/ MMC1_RESET_N	AE8	SE69		MMC1_R CLK	MMC1_R ESET_N				ed uno.	
	PMC_SUSCLK[3]	B12	N18		PMC_SUS CLK[3]				undefi		-
	JTAG2_TDI	B14	N17	indefil	JTAG2_T DI			defined			
'Ue	DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	C10	N66		DDI0_DD C_DATA	DDI1_DD C_DATA	MDSI_D DC_DATA	7100			ined
	PMC_SUSCLK[2]	C14 C14	N25		PMC_SUS CLK[2]	. ned un	0			d und	ern
	JTAG2_TCK	C15	N19		JTAG2_TC K	SUL			ndef	Ner	
	GPIO_N3/ C0_BPM1_TX/ C1_BPM1_TX	C17	N3	Indefi	Nec			define	C0_BPM 1_TX	C1_BPM1 _TX	
	DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/ MDSI_C_TE	C9	N62 ndefine	0	DDI2_DD C_DATA	DDI1_DD C_DATA	UARTO_D ATAIN	MDSI_DDC _DATA	MDSI_C _TE		defined
	JTAG2_TDO	D14	N22		JTAG2_T DO	efineo				ined un	_
-	JTAG2_TMS	D15	N24		JTAG2_T MS				ed unde	20	
	DDI1_BKLTCTL/ MDSI_A_TE/ MDSI_C_TE	D8	N63	ed unde	DDI1_BK LTCTL		MDSI_A_ TE	MDSI_C_T E			-
	DDI2_DDC_CLK/ DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/ MDSI_A_TE	E10	N67		DDI2_DD C_CLK	DDI1_DD C_CLK	UARTO_D ATAOUT	MDSI_DDC _CLK	MDSI_A _TE	ed ut	define
	GPIO_N4/ C0_BPM0_TX/ C1_BPM0_TX	E16	N4		ined un	96.			C0_BPM 0_TX	C1_BPM0 _TX	1
	GPIO_N0/ C0_BPM0_TX/ C1_BPM0_TX	E17	NO	ed und	SU.			undefil	C0_BPM 0_TX	C1_BPM0 _TX	
er.	GPIO_N2/ C0_BPM2_TX/ C1_BPM2_TX	F16	N2 eff				ndefin	30 °	CO_BPM 2_TX	C1_BPM2 _TX	Jefin
L		undefineo				defined				sined "	Ino
	58 58 ined undefined				Jefined W	no			Data	asheet	
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Ndefined undefined undefined Multiplexed Functions - T3 SoC (Sheet 2 of 9) Table 36.



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sined U.				d undefin				neel	
nden.			define						
Table 36.	Multiplexe	ed Funct	ions - T3	SoC (She	et 3 of 9)	22.	del.		
Table 36. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
GPIO_N1/ C0_BPM3_TX/ C1_BPM3_TX	F17	N1		Jefi	nedun			CO_BPM 3_TX	C1_BPM _TX
UART0_DATAIN	V13	SE48	eine	d une	UART0_D ATAIN		6	Jude	
PMC_SLP_S0IX_N	W4	E3	undett	PMC_SLP _S0IX_N			ndefine		
UART0_DATAOUT	Y12	SE46			UART0_D ATAOUT	stined			
GPIO_N6/ C0_BPM3_TX/ C1_BPM3_TX	C16	N6			ined unc			CO_BPM 3_TX	C1_BPM _TX
GPIO_N8/ C0_BPM1_TX/ C1_BPM1_TX	D16	N8		ed unde			0	CO_BPM 1_TX	C1_BPM _TX
ISH_GPIO[13]/ C0_BPM2_TX/ C1_BPM2_TX	D17	N7	undefin				ISH_GPIO[13]	C0_BPM 2_TX	C1_BPM _TX
GPIO_SUS9	A13	N27		GPIO_SU S9		<i>lefined</i>			
GPIO_SUS0	A14	N15			ined un				d un
DDI0_VDDEN	A9	N72		DDI0_VD DEN	3			defi	Ne
SD3_CMD	AA10	SE34	defi	SD3_CM D			stine	3.0.	
FST_SPI_CS[0]_N	AA12 AA14	SW6 SW36	dun	FST_SPI_ CS[0]_N LPE_I2S1	<u> </u>	60	unde	<u> </u>	<u> </u>
	ال م	noc		_FRM		define		<u> </u>	ļ
LPE_I2S0_DATAOU T	AA15	SW30		LPE_I2S0 _DATAOU T	efined .			ć	ined ut
LPE_I2S0_CLK	AA16	SW31	۵. ام	LPE_I2S0 _CLK				d unde	1
I2C2_CLK	AA17	SW66	d unde	I2C2_CLK			undefin		
ISH_I2C1_CLK/ ISH_SPI_CLK/ I2S5_DATAIN	AA3	E17 in		ISH_I2C1 _CLK	ISH_SPI_ CLK	I2S5_DA TAIN	3 ~ .		
	Indefineo			afined un	defined I	<i>)</i> ,	d undefin		eined l
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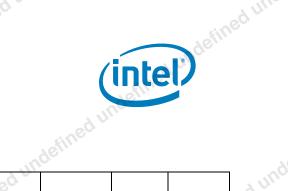
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			d undef		
Multiplexed	l Functi	ons - T3	SoC (She	eet 4 of 9)	
	Multiplexed		odefin	adefined und	Multiplexed Functions - T3 SoC (Sheet 4 of 9)

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intel				ad undef	ned u.		Phys	sical Inter	faces
			ndefin				defined	une	
Table 36. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
ISH_GPIO[9]/ ISH_SPI_MISO/ I2S5_FS	AA4	E20		ISH_GPI O[9]	ISH_SPI_ MISO	I2S5_FS		ci.	ned und
ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	AA5	E26	- fil	ISH_I2C1 _DATA	ISH_SPI_ MOSI	I2S5_DA TAOUT	e	under	2
MMC1_CMD	AA6	SE23	under	MMC1_C MD			define		
MMC1_D[7]	AA7	SE68	<u> </u>	MMC1_D[7]		Lefined	077 .		
MMC1_D[0]	AA8	SE17		MMC1_D[0]	d ur	0.			. nd
SD3_PWREN_N	AA9	SE78		SD3_PWR EN_N	stine			40	med u.
SD3_D[2]	AB10	SE33	e.	SD3_D[2]				dunu	
FST_SPI_D[0]	AB11	SW1	d undet	FST_SPI_ D[0]			undefine		
FST_SPI_CLK	AB12	SW2		FST_SPI_ CLK		sined			
UART2_DATAOUT	AB13	SW21		UART2_D ATAOUT	ed U	nder			nu -
LPE_I2S1_CLK	AB14	SW32		LPE_I2S1 _CLK	efine			10	sined s
LPE_I2S0_DATAIN	AB15	SW33	20	LPE_I2S0 _DATAIN			272	ed unoc	
I2C5_CLK	AB16	SW50	sq nurs	I2C5_CLK			d under		
LPE_I2S2_CLK	AB19	SW92		LPE_I2S2 _CLK		ndefine			
ISH_GPIO[0]/ I2S3_CLK	AB2	E21		ISH_GPI O[0]	afined	I2S3_CL K			uned u
PCIE_CLKREQ[0]_ N	AB20	SW90		PCIE_CLK REQ[0]_ N	0-			d und	er,
ISH_GPIO[2]/ I2S3_DATAOUT	AB3	E24	ind	ISH_GPI O[2]		I2S3_DA TAOUT	defi	no	
SD2_CMD	AB5	SE22	led r	SD2_CM D			ed un		
MMC1_D[2]	AB6	SE20		MMC1_D[2]		indefin			
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ned un			ed un				undet	1.	



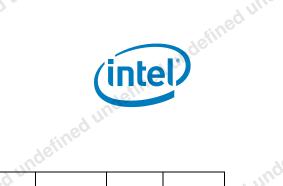
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stined u.				d undefin			2 13	nielli	
Table 36.	Multiplexe	ed Funct					defined		
Table 36. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
MMC1_D[6]	AB7	SE63	<u>+</u>	MMC1_D[6]	ned un	<u> </u>			d unde
SD3_1P8_EN	AB8	SE85		SD3_1P8 _EN				ndefine	
SD3_D[1]	AB9	SE30	define	SD3_D[1]			sined		
ISH_GPIO[7]/ I2S4_DATAIN	AC1	E16	and	ISH_GPI O[7]		I2S4_DA TAIN	nder.		
SD3_D[0]	AC10	SE35		SD3_D[0]	6	efineu			
FST_SPI_D[1]	AC11	SW5		FST_SPI_ D[1]	ined un				d und
UART2_RTS_N	AC12	SW19		UART2_R TS_N	<u> </u>			Indefin	
UART1_CTS_N	AC13	SW18	undefin	UART1_C TS_N			ndefined		
UART1_DATAOUT/ UART0_DATAOUT	AC14	SW20	2	UART1_D ATAOUT	UART0_D ATAOUT	efined			
NFC_I2C_DATA	AC15	SW51	+	NFC_I2C _DATA	ined un			+	dun
NFC_I2C_CLK	AC16	SW54	1	NFC_I2C _CLK				ndefi	le.
I2C2_DATA	AC17	SW62	undefi	I2C2_DA TA			define	0	
GPIO_SW78	AC18	SW78	,D	+		sined	UN	1	
LPE_I2S2_FRM	AC19	SW96	1	LPE_I2S2 _FRM	ad ut	loer.		1	
ISH_GPIO[4]/ I2S4_CLK	AC2	E22	<u> </u>	ISH_GPI O[4]	etime-	I2S4_CL K	<u> </u>	10	ined
GPIO_SW93	AC20	SW93		inedu				d unas	
MMC1_D[3]	AC6	SE26	d unde	MMC1_D[3]	+		Indefin	+	+
MMC1_D[4]	AC7	SE67		MMC1_D[lefine		<u> </u>	
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			ed un.				d unde		

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intel				ed undefi			Physical Interfaces					
undefine Table 36.	Multiplexe	a Functi	ger.)	defined	UI.				
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6			
MMC1_D[5]	AC8	SE65		MMC1_D[5]	ined un				ed unde			
SD3_CLK	AC9	SE31		SD3_CLK		1	†	1611				
SD3_D[3]	AD10	SE32	Ali P	SD3_D[3]			ec	Junos				
UART2_CTS_N	AD12	SW22	under	UART2_C TS_N			undefin					
UART1_DATAIN/ UART0_DATAIN	AD14	SW16		UART1_D ATAIN	UARTO_D ATAIN	defined						
I2C6_DATA/ SD3_WP	AD16	SW49		I2C6_DA TA	SD3_WP			¢.	ned une			
MMC1_RESET_N	AD18	SW80		ed uno	MMC1_R ESET_N	+		undet				
PWM[1]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	AD2	SE1	d under	PWM[1]	ISH_GPI O[10]	ISH_UAR T_DATAO UT	undefine					
SD3_WP	AD20	SW95			SD3_WP	ndefiner						
PWM[0]	AD3	SE5		PWM[0]	e d V	<u> </u>	+	+	_ un			
SD2_D[0]	AD4	SE25		SD2_D[0]	Jetin	+		20	ineo			
SD2_CLK	AD5	SE19		SD2_CLK	1	1		2 Uni				
SD2_D[3]_CD_N	AD6	SE15	unde	SD2_D[3]_CD_N			defin	60				
MMC1_CLK	AD8	SE16	SO _	MMC1_CL K		-0	d un					
UART2_DATAIN	AE12	SW17		UART2_D ATAIN	6	undefine						
UART1_RTS_N	AE13	SW15		UART1_R TS_N	definer			6	stined			
I2C6_CLK/NMI_N	AE16	SW53	6	I2C6_CLK	NMI_N		lije i	ned un				
I2C5_DATA	AE17	SW45	ned une	I2C5_DA TA			ed unde					
UARTO_DATAIN	AE18	SW77			UART0_D ATAIN	Indefin						
62 Ined undefined	undefine			Jefined U	ndefined			Data	sheet			
ed under.			und	Jefine			d undef	ined				
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Physical Inte	14000			ndefin				Inte	
ndefined unor Table 36. GPIO Pin			adefiner	3 UN			defined u	in-	
Table 36. GPIO Pin Name	Multiplexe Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
SD2_D[1]	AE4	SE18		SD2_D[1]	ned un				d unde
SD2_D[2]	AE5	SE21		SD2_D[2]				ndefini	
SD3_CD_N	AE9	SE81	define	SD3_CD_ N			efined		
GPIO_CAMERASB1 0	B10	N50	D/	GPIO_CA MERASB1 0		sined u	NG6.		
DDI0_BKLTCTL	B8 UN	N65	+	DDI0_BK LTCTL	4 und	6		<u> </u>	6
GPIO_CAMERASB1 1	C11	N55		GPIO_CA MERASB1 1	INEO			defin	ed un
JTAG_TDI	C12	N41		JTAG_TDI			2	NUC	
GPIO_SUS8	C13	N23	undefit	GPIO_SU S8			defined		
DDI0_BKLTEN	C8	N60		DDI0_BK LTEN		stined			
GPIO_CAMERASB0 9	D10 Un	N52		GPIO_CA MERASB0 9	ined un	05.			d un
GPIO_CAMERASB0 8	D11	N47		GPIO_CA MERASB0 8				undefi	
DDI0_HPD	D9	N61	Indefi	DDI0_HP D			define		
SVID_ALERT_N	E12	N38	¢	SVID_AL ERT_N		sined	UN	1	
ITAG_TRST_N	E13	N30		JTAG_TR ST_N		19er			1
ITAG_TCK	E14	N31		JTAG_TC K	efinec			¢	nedu
DDI2_HPD	E9	N68		DDI2_HP D				d unde	
SVID_CLK	F11	N40	L unde	SVID_CL K			adefin		
SVID_DATA	F12	N33	SVID_D ATA			sine	Y Ou.		
JTAG_TDO	F13	N39		JTAG_TD O		uger.			
Datasheet	Indefin			atined un	definer			- 66	fined 63
Indefine				stined			d undefin	ed une	05
			d uno				nden		

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intel				ad undefi	ned u.		Phys	sical Inter	faces
			ndefin				defined	unoc	
Table 36. GPIO Pin Name	Multiplexe Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
JTAG_TMS	F14	N34		JTAG_TM S	ned un				d unde
GPIO_DFX4	F18	N5		d unde				undefi	
PROCHOT_N	F9	N32	defi	PROCHOT _N			fine		
LPE_I2S2_DATAIN	U17	SW94	VINC	LPE_I2S2 _DATAIN		ed	unde		
PMC_SUSPWRDNA CK	V12	SE83		PMC_SUS PWRDNA CK	-d un	detin			, ind
LPE_I2S2_DATAOU T	V18	SW97		LPE_I2S2 _DATAOU T	stiner			def	neo
PMC_SUS_STAT_N	V5	E2	i a	PMC_SUS _STAT_N				d ulli	
I2C1_DATA	W15	SW60	d unde	I2C1_DA TA		ed	undefil.		
I2C1_CLK	W16	SW63		I2C1_CLK	sined U	ndefill			ined un
PMC_PWRBTN_N	W3	E8		PMC_PW RBTN_N	CJ1.			a unde	AULO
ISH_GPIO[3]/ I2S3_DATAIN	Y1	E15	inde	ISH_GPI O[3]		I2S3_DA TAIN	Jefin		
LPE_I2S1_DATAIN	Y13	SW37	ed V.	LPE_I2S1 _DATAIN		eine	d une		
LPE_I2S1_DATAOU T	Y14 sined	SW34		LPE_I2S1 _DATAOU T	ed	IUder			du
LPE_I2S0_FRM	Y16	SW35		LPE_I2S0 _FRM	detint			60.	efineo
I2C0_CLK	Y17	SW65	ned und	I2C0_CLK			d undefi	ned us	
neo		, defi	ned t			in	ed un		
64 ined undefined	defined	UI.		Jefined u	stined	unde			rined
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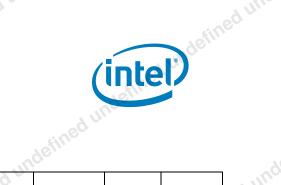


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	Indefinec			defined				afined u	Uc.			
ined)	Table 36.	Multiplexe	ed Functi	ions - T3	SoC (She	et 9 of 9)	<u>n.</u>	9e.			_	
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	ned	
	I2C0_DATA	Y18	SW61		I2C0_DA TA	led a.			Indefine	d uno		
6	ISH_GPIO[1]/ I2S3_FS	Y2	E18	Indefinit	ISH_GPI O[1]		I2S3_FS	definet				
fine	PMC_WAKE_N	Y3	E10		PMC_WA KE_N		sined ut				5	
	PMC_SUSCLK[0]	Y4 uns	E6		PMC_SUS CLK[0]	ed und	3			4 unde	ane	
	PMC_PLTRST_N	Y5	E5		PMC_PLT RST_N				indefin	20 [.]		
2	MMC1_D[1]	Y8	SE24	defin	MMC1_D[1]			etined			1	
etiner	USB_OC[0]_N	Y9	SE80	n.	USB_OC[1]_N		red	moe				
	Table 37.	Multiplexe	ed Funct	ions - T3	SoC (She	et 1 of 9)	Jetu.			a undr	stine	

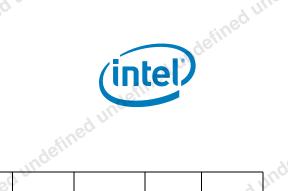
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Table 37. Multiplexed Functions - T3 SoC (Sheet 1 of 9)

					6414						_
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	
undefined un	DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK	A10	N71	Jetti	DDI0_DD C_CLK	DDI1_DD C_CLK	MDSI_D DC_CLK	stines			
Junden	GPIO_SE79	AA13	SE79			defi	neo			Sin	30 1
	I2C4_CLK/ DDI1_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	AB17	SW52		I2C4_CLK	DDI1_DD C_CLK	DDI2_D DC_CLK	MDSI_DDC _CLK	efined	unde	-
والمناجع	I2C4_DATA/ DDI1_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	AB18	SW46	defined	I2C4_DA TA	DDI1_DD C_DATA	DDI2_D DC_DATA	MDSI_DDC _DATA	0		
ed undefinee	PMC_PLT_CLK[3]/ ISH_GPIO[13]/ ISH_UART_RTS_N/ SPI2_CLK	AB4	SE4		PMC_PLT _CLK[3]	ISH_GPI O[13]	ISH_UAR T_RTS_N	SPI2_CLK		1efil	ed '
	undef				defin	ed u.			stined	Juno	
	Datasheet			efine	undefin			utined u	65 G5		
lefined !	71.		cined U	nac			d un	detin			



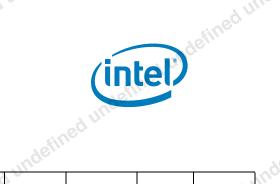
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	(intel)				ndefined	0.		Physical I	Interfaces		
	etti		-96					ined une			
tined und	GPIO Pin	Package Ball #	GPIO #	Mode 0	(Sheet 2 Mode 1	of 9) Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	N.
	Name PMC_PLT_CLK[4]/ ISH_GPIO[14]/ ISH_I2C0_DATA/ SPI2_MISO	AC3	SE3		PMC_PLT _CLK[4]	ISH_GPI O[14]	ISH_I2C 0_DATA	SPI2_MIS O	efined	uden.	
ed un	PMC_PLT_CLK[2]/ ISH_GPIO[12]/ ISH_UART_CTS_N/ SPI2_CS[0]_N	AC4	SE7	efined	PMC_PLT _CLK[2]	ISH_GPI O[12]	ISH_UAR T_CTS_N	SPI2_CS[0]_N	20		
stine	PMC_PLT_CLK[5]/ ISH_GPIO[15]/ ISH_I2C0_CLK/ SPI2_MOSI	AE3	SE6		PMC_PLT _CLK[5]	ISH_GPI O[15]	ISH_I2C 0_CLK	SPI2_MOS I		defined	
	MMC1_RCLK/ MMC1_RESET_N	AE8	SE69		MMC1_R CLK	MMC1_R ESET_N			60	JU.	
	PMC_SUSCLK[3]	B12	N18	6	PMC_SUS CLK[3]			27.	detine		
d ur	JTAG2_TDI	B14	N17	defines	JTAG2_T DI			efined			
efines	DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	C10	N66		DDI0_DD C_DATA	DDI1_DD C_DATA	MDSI_D DC_DATA			- fin	
	PMC_SUSCLK[2]	C14	N25		PMC_SUS CLK[2]	ed une				unde	
	JTAG2_TCK	C15	N19		JTAG2_TC K				ndefine		
ed v	GPIO_N3/ C0_BPM1_TX/ C1_BPM1_TX	C17	N3	ndefine				defined	C0_BPM 1_TX	C1_BPM1 _TX	
define	DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/ MDSI_C_TE	C9	N62		DDI2_DD C_DATA	DDI1_DD C_DATA	UARTO_D ATAIN	MDSI_DDC _DATA	MDSI_C _TE	ndefit	
	JTAG2_TDO	D14	N22		JTAG2_T DO	0~			stine	0	
	JTAG2_TMS	D15	N24	fine	JTAG2_T MS			ed	JUGE		
defined	DDI1_BKLTCTL/ MDSI_A_TE/ MDSI_C_TE	D8	N63	Juge.	DDI1_BK LTCTL		MDSI_A_ TE	MDSI_C_T E			
	66	afined und			ed undefi	ined und	etu.			ed undefi	5
	66 undefined un			defin	ed unos			efined	Datasheet		
lefined			ed	UI				Inde			



ger.		undefine				defined				Jefined un
	Physical Interfaces				Jefined U	(ne		(in	tel	Je.
Idefined undef	ined b.		ik.	ined un				ied uniel		
sined un	Table 37. Mult	iplexed Fu	nctions -	T3 SoC	(Sheet 3	of 9)	indefi			6
nderr.	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	DDI2_DDC_CLK/ DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/ MDSI_A_TE	E10	N67	ed un	DDI2_DD C_CLK	DDI1_DD C_CLK	UART0_D ATAOUT	MDSI_DDC _CLK	MDSI_A _TE	
ed unde	GPIO_N4/ C0_BPM0_TX/ C1_BPM0_TX	E16	N4 unde	ine			ndef	neo	C0_BPM 0_TX	C1_BPM0 _TX
Indefine	GPIO_N0/ C0_BPM0_TX/ C1_BPM0_TX	E17	NO			define	0		CO_BPM 0_TX	C1_BPM0 _TX
	GPIO_N2/ C0_BPM2_TX/ C1_BPM2_TX	F16	N2		sined	UNC			C0_BPM 2_TX	C1_BPM2 _TX
	GPIO_N1/ C0_BPM3_TX/ C1_BPM3_TX	F17	N1	ined u	nder			d und	C0_BPM 3_TX	C1_BPM3 _TX
sined une	UARTO_DATAIN	V13	SE48	2		UARTO_D ATAIN	, unde	Ine		
undell	PMC_SLP_S0IX_N	W4	E3		PMC_SLP _SOIX_N	i efin	80 -			ined ut
	UART0_DATAOUT	Y12	SE46		0	UART0_D ATAOUT				unden
	GPIO_N6/ C0_BPM3_TX/ C1_BPM3_TX	C16	N6	. 6	Indefine			und	CO_BPM 3_TX	C1_BPM3 _TX
ed un	GPIO_N8/ C0_BPM1_TX/ C1_BPM1_TX	D16	N8	Jefines				stined	C0_BPM 1_TX	C1_BPM1 _TX
undefined u	ISH_GPIO[13]/ C0_BPM2_TX/ C1_BPM2_TX	D17	N7			Jefi	ned un	ISH_GPIO[13]	CO_BPM 2_TX	C1_BPM2 _TX
	GPIO_SUS9	A13	N27		GPIO_SU S9	d une			2	under
	GPIO_SUS0	A14	N15		undefill			21.	definee	
	DDI0_VDDEN	A9	N72	define	DDI0_VD DEN			sined		
lefined c	SD3_CMD	AA10	SE34		SD3_CM D		d uni	(C)		
d undefined u	FST_SPI_CS[0]_N	AA12	SW6		FST_SPI_ CS[0]_N	det	Ines			leftined.
	indefi				Aefin	led un.				d under
I	Datasheet				d undefin			defined u	ndell'67	
offined			redu	nder.				define		



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(intel)				ndefined			Physical 1	Interfaces		
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GPIO Name	iplexed Fu Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	ò
LPE_I2S1_FRM	AA14	SW36		LPE_I2S1 _FRM	UNC			ed l	nde.	
LPE_I2S0_DATAOU T	AA15	SW30	ined	LPE_I2S0 _DATAOU T			od und	Set		
LPE_I2S0_CLK	AA16	SW31	C.	LPE_I2S0 _CLK		unde	AINE			
I2C2_CLK	AA17	SW66		I2C2_CLK	defi	160			nie	69
ISH_I2C1_CLK/ ISH_SPI_CLK/ I2S5_DATAIN	AA3	E17		ISH_I2C1 _CLK	ISH_SPI_ CLK	I2S5_DA TAIN		ed	unde.	
ISH_GPIO[9]/ ISH_SPI_MISO/ I2S5_FS	AA4	E20	aned	ISH_GPI O[9]	ISH_SPI_ MISO	I2S5_FS	dun	defit		
ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	AA5	E26	9er.	ISH_I2C1 _DATA	ISH_SPI_ MOSI	I2S5_DA TAOUT	etine			
MMC1_CMD	AA6	SE23		MMC1_C MD	101	ned			e.x	e
MMC1_D[7]	AA7	SE68		MMC1_D[7]	d unoc				undein	
MMC1_D[0]	AA8	SE17		MMC1_D[0]				lefiner		
SD3_PWREN_N	AA9	SE78	sined	SD3_PWR EN_N			du	nde		
SD3_D[2]	AB10	SE33	lo _{ell} .	SD3_D[2			Jetines			
SD3_D[2] FST_SPI_D[0]	AB11	SW1] FST_SPI_ D[0]	20	ined un			c.	
FST_SPI_CLK	AB12	SW2		FST_SPI_ CLK	ed unos				under	
UART2_DATAOUT	AB13	SW21		UART2_D ATAOUT				Aefine	P	
LPE_I2S1_CLK	AB14	SW32	Lefine	LPE_I2S1 _CLK			ed	JULO		
LPE_I2S0_DATAIN	AB15	SW33	Ince	LPE_I2S0 _DATAIN		ال لم	Idet.			
LPE_I2S0_DATAIN	AB16	SW50		I2C5_CLK	60.	etineu			10	și î
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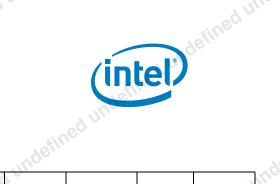
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ger.		Je	ine							
Table 37. Mul	tiplexed Fu	nctions	- T3 SoC	(Sheet 5	of 9)	under.	•	1		
Table 37. Mul GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode	
LPE_I2S2_CLK	AB19	SW92		LPE_I2S2 _CLK				ined un	0.	
ISH_GPIO[0]/ I2S3_CLK	AB2	E21	ed un	ISH_GPI O[0]		I2S3_CL K	unde			
PCIE_CLKREQ[0]_ N	AB20	SW90	stine	PCIE_CLK REQ[0]_ N		ndef	neo			
ISH_GPIO[2]/ I2S3_DATAOUT	AB3	E24		ISH_GPI O[2]	eine	12S3_DA TAOUT				
SD2_CMD	AB5	SE22		SD2_CM D	undell				defin	
MMC1_D[2]	AB6	SE20		MMC1_D[2]				eined u		
MMC1_D[6]	AB7	SE63	ed u	MMC1_D[6]			_ und	0		
SD3_1P8_EN	AB8	SE85	stin	SD3_1P8 _EN		20	ineo			
SD3_IP8_EN SD3_D[1] ISH_GPI0[7]/	AB9	SE30				ed unos				
ISH_GPIO[7]/ I2S4_DATAIN	AC1	E16		ISH_GPI O[7]	indefit	I2S4_DA TAIN			10fil	
SD3_D[0]	AC10	SE35		SD3_D[0]	6. ¹ .			ed	Ino-	
FST_SPI_D[1]	AC11	SW5	6	FST_SPI_ D[1]			un	etine		
UART2_RTS_N	AC12	SW19	define	UART2_R TS_N		b _n .	stined			
UART2_RTS_N UART1_CTS_N	AC13	SW18		UART1_C TS_N	defi	ned u.				
UART1_DATAOUT/ UART0_DATAOUT	AC14	SW20		UART1_D ATAOUT	UART0_D ATAOUT			6	unde	
NFC_I2C_DATA	AC15	SW51	-9	NFC_I2C _DATA			11.	define		
NFC_I2C_CLK	AC16	SW54	defines	NFC_I2C _CLK			efined			
I2C2_DATA	AC17	SW62		I2C2_DA		ined und				
I2C2_DATA	ined unde			I2C2_DA TA	ed unde	Inec			d uni	
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	efit		6	Stille				ined uno		
ned und	Table 37. Mult GPIO Pin Name	tiplexed Fu Package Ball #	GPIO #	- T3 SoC Mode 0	(Sheet 6 Mode 1	of 9) Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	GPIO_SW78	AC18	SW78		tatined	s une			ed	inde.
	LPE_I2S2_FRM	AC19	SW96	ed 1	LPE_I2S2 _FRM			, uni	eth	
d un	ISH_GPIO[4]/ I2S4_CLK	AC2	E22	Jetine	ISH_GPI O[4]		I2S4_CL K	tineo		
inec	GPIO_SW93	AC20	SW93			1	red unit			.0
	MMC1_D[3]	AC6	SE26		MMC1_D[3]	d under.				andefine
	MMC1_D[4]	AC7	SE67		MMC1_D[4]				etined	· · · · · · · · · · · · · · · · · · ·
	MMC1_D[5]	AC8	SE65	ned	MMC1_D[5]			dun	00	
ured ur	SD3_CLK SD3_D[3]	AC9 AD10	SE31 SE32	defin	SD3_CLK SD3_D[3		in ^c	etinec		
3411.	UART2_CTS_N	AD12	SW22] UART2_C TS_N	ndef	ned U.			4efin
	UART1_DATAIN/ UART0_DATAIN	AD14	SW16		UART1_D ATAIN	UARTO_D ATAIN			sined	una
	I2C6_DATA/ SD3_WP	AD16	SW49	eined	I2C6_DA TA	SD3_WP		du	Nge.	
ined "	MMC1_RESET_N	AD18	SW80	ndell		MMC1_R ESET_N	71.	define		
efined	PWM[1]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	AD2	SE1		PWM[1]	ISH_GPI O[10]	ISH_UAR T_DATAO UT			ndefil
	SD3_WP	AD20	SW95		defil	SD3_WP			stine	dun
	PWM[0]	AD3	SE5	.0	PWM[0]				unde.	
-	SD2_D[0]	AD4	SE25	define	SD2_D[0]			sineo		
	SD2_CLK	AD5	SE19	ALT	SD2_CLK			loe,		
defined	SD2_D[3]_CD_N	AD6	SE15		SD2_D[3]_CD_N		efined			<u>.</u>
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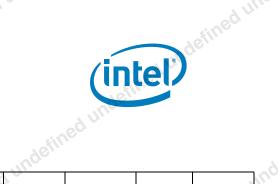


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Table 37. Mul GPIO Pin	tiplexed Fu	nctions	- T3 SoC	(Sheet 7	of 9)	undefin			
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode
MMC1_CLK	AD8	SE16		MMC1_CL K				d un	0.0
UART2_DATAIN	AE12	SW17	ned un	UART2_D ATAIN			d unde	AULE	
UART1_RTS_N	AE13	SW15		UART1_R TS_N		undefi	Ver		
I2C6_CLK/NMI_N	AE16	SW53		I2C6_CLK	NMI_N	0			0.55
I2C5_DATA	AE17	SW45		I2C5_DA TA	uno			du	Ndern.
UARTO_DATAIN	AE18	SW77		ndetil	UART0_D ATAIN		6	etine	
SD2_D[1]	AE4	SE18	efined	SD2_D[1]			ned une		
SD2_D[2]	AE5	SE21		SD2_D[2]		, unde			
SD3_CD_N	AE9	SE81		SD3_CD_ N	defin	60			- All
GPIO_CAMERASB1 0	B10	N50		GPIO_CA MERASB1 0	d un			sined	Inde
DDI0_BKLTCTL	B8	N65	ed'	DDI0_BK LTCTL				ye.	
GPIO_CAMERASB1 1 GPIO_SUS8 DDI0_BKLTEN	C11	N55	define	GPIO_CA MERASB1 1		ind	stineo		
GPIO_SUS8	C13	N23		GPIO_SU S8	in the second	nedu			
DDI0_BKLTEN	C8	N60		DDI0_BK LTEN	ad under			-0	undef
GPIO_CAMERASB0 9	D10	N52	6	GPIO_CA MERASB0 9				definee	
GPIO_CAMERASB0 8	D11	N47	define	GPIO_CA MERASB0 8		~	efined		
DDI0_HPD	D9	N61		DDI0_HP		ined un			
20	ined with	1	1	d undefil	led unde	1			d unde
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defined undefined undefined Table 37. Multiplexed Functions - T3 SoC (Sheet 7 of 9)



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	intel				ndefined			Physical I	nterfaces	
			6					ined uno.		
efined un		Package Ball #	GPIO #	Mode 0	(Sheet 8 Mode 1	of 9) Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	Name SVID_ALERT_N	E12	N38		SVID_AL	unos				Ugell.
	DDI2_HPD	E9	N68		ERT_N DDI2_HP D			50.	etined	
	SVID_CLK	F11	N40	efineo	SVID_CL K			inedur		
ined ut	SVID_DATA	F12	N33	SVID_D ATA	ĸ		d unde			
	GPIO_DFX4	F18	N5			indefil	e ^{c.}			define
	PROCHOT_N	F9	N32		PROCHOT _N	<u>9</u> .			ed	JUO
	LPE_I2S2_DATAIN	U17	SW94	ed	 LPE_I2S2 _DATAIN			a un	define	
ed 1	PMC_SUSPWRDNA CK	V12	SE83	detin	PMC_SUS PWRDNA CK		nd	efined		
•	LPE_I2S2_DATAOU T	V18	SW97		LPE_I2S2 _DATAOU T	def	nedu			ni)
	PMC_SUS_STAT_N	V5	E2		PMC_SUS _STAT_N	ed une			6	under
	I2C1_DATA	W15	SW60	. net	I2C1_DA			ران	adefined	<u></u>
ned	I2C1_CLK	W16	SW63	ndefini	I2C1_CLK		ined un	Jefinec		
ined	PMC_PWRBTN_N	W3 UNO	E8		PMC_PW RBTN_N	unde	ANCC			defin
	ISH_GPIO[3]/ I2S3_DATAIN	Y1	E15		ISH_GPI O[3]	60	I2S3_DA TAIN		sine	3 11.
	LPE_I2S1_DATAIN	Y13	SW37	eine	LPE_I2S1 _DATAIN			ed '	udell	
	LPE_I2S1_DATAOU T	Y14	SW34	Inder	LPE_I2S1 _DATAOU T			define		
afined	LPE_I2S0_FRM	Y16	SW35		LPE_I2S0 _FRM	nd	efineo			105
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	Table 37. Mult	tiplexed Fu	nctions ·	- 13 Soc	(Sheet 9	of 9)	uno			
	Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	I2C0_CLK	Y17	SW65	nu ,	I2C0_CLK			de	ined un	
		2410	01461	ineo	1200 54			ed ull		
	I2C0_DATA	Y18	SW61		I2C0_DA TA		d undefi	nu l		
		defin				stine				ned
	ISH_GPIO[1]/ I2S3_FS	Y2	E18		ISH_GPI O[1]	uno	I2S3_FS		. *	dern
	PMC_WAKE_N	Y3	E10		PMC_WA			A	afined u	
	PMC_SUSCLK[0]	Y4	E6	efined	PMC_SUS CLK[0]			ined une		
	PMC_PLTRST_N	Y5	ES UNO		PMC_PLT RST_N		sq nuqe			
	MMC1_D[1]	Y8	SE24		MMC1_D[ndeft				1efine
	MMC1_D[1] USB_OC[0]_N Datasheet	Y9	SE80		1] USB_OC[1]_N				sined	nau
	USB_OC[0]_N			cined !	§		I	od un	901.	
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Table 37.

Processor Core



Processor Core

fined undefined un Up to four out-of-order execution processor cores are supported, each dual core module supports up to 1 MB of L2 cache.

Features

- 14nm Process technology.
- Quad Out-of-Order Execution (OOE) processor cores.
- Primary 32 KB, 8-way L1 instruction cache and 24 KiB, 6-way L1 write-back data cache.
- Cores are grouped into dual-core modules: modules share a 1 MB, 16-way L2 cache (2 MB total for Quad Core)Intel[®] Streaming SIMD Extensions 4.1 and 4.2 (SSE4.1 and SSE4.2), which include new instructions for media and for fast XML parsing.
- Intel[®] 64 Bit architecture
- Supports IA 32-bit.
- Supports Intel[®] VT-x2.
- Supports Intel[®] Advanced Encryption Standard (AES) New instructions (AES-NI).
- Supports Intel[®] Carry-Less Multiplication Instruction (PCLMULQDQ).
- Supports Digital Random Number Generator (DRNG).
- Supports C0, C1, C1E, C6C, C6 and C7 states.
- Thermal management support via Intel[®] Thermal Monitor (TM1 & TM2).
- Uses Power Aware Interrupt Routing (PAIR).

Intel[®] Hyper-Threading Technology is not supported.

3.1.1

Note:

Intel[®] Virtualization Technology (Intel[®] VT)

Intel[®] Virtualization Technology (Intel[®] VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel[®] VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel[®] Virtualization Technology for IA-32, Intel[®] 64 and Intel[®] Architecture (Intel[®] VT-x2) added hardware support in the processor to improve the virtualization performance and robustness.

Intel[®] VT-x2 specifications and functional descriptions are included in the *Intel[®]* 64 and IA-32 Architectures Software Developer's Manual, Volume 3B and is available at: http:/ /www.intel.com/products/processor/manuals/index.htm. in a sum defined undefined ut

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3.1.1



Other Intel[®] VT-x2 documents can be referenced at: http://www.intel.com/ technology/virtualization/index.htm

Intel[®] VT-x2 Objectives 3.1.1.1

- Robust: VMMs no longer need to use paravirtualization or binary translation. This means that they will be able to run off-the-shelf OSs and applications without any special steps.
- Enhanced: Intel[®] VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system. Intel[®] VT-x2 provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel[®] VT-x2 features to provide improved reliable virtualized platform.

Intel[®] VT-x2 Features

- Extended Page Tables (EPT)
 - EPT is hardware assisted page table physical memory virtualization.
 - Support guest VM execution in unpaged protected mode or in real-address mode.
 - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance.
- Virtual Processor IDs (VPID)
 - A VM Virtual Processor ID is used to tag processor core hardware structures (such as TLBs) to allow a logic processor to cache information (such as TLBs) for multiple linear address spaces.
 - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
 - Mechanism for a VMM to preempt the execution of a guest OS VM after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
 - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees flexibility in guest VM scheduling and building Quality of Service (QoS) schemes.
- Descriptor-Table Exiting
 - undefined undefined undefin Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data

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structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).

- A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.
- VM Functions
 - VM function is an operation provided by the processor that can be invoked using the VMFUNC instruction from quest VM without a VM exit.
 - VM function to perform EPTP switching is supported and allows guest VM to load a new value for the EPT pointer, thereby establishing a different EPT paging structure hierarchy.

Security and Cryptography Technologies 3.1.2

3.1.2.1 Advanced Encryption Standard New Instructions (AES-NI)

The processor supports Advanced Encryption Standard New Instructions (AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). AES-NI are valuable for a wide range of cryptographic applications, for example: applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

AES-NI consists of six Intel[®] SSE instructions. Four instructions, namely AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for support AES, offering security, high performance, and a great deal of flexibility.

3.1.2 **PCLMULQDQ** Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

Digital Random Number Generator

The processor introduces a software visible digital random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the new RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards (ANSI X9.82 and NIST SP 800-90). imed undefined

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Some possible uses of the new RDRAND instruction include cryptographic key generation as used in a variety of applications including communication, digital signatures, secure storage, and so on.

3.1.3 **Power Aware Interrupt Routing**

PAIR is an improvement in H/W routing of "redirectable" interrupts. Each core powerstate is considered in the routing selection to reduce the power or performance impact of interrupts. System BIOS configures the routing algorithm, e.g. fixed-priority, rotating, hash, or PAIR, during setup via non-architectural register. The PAIR algorithm can be biased to optimize for power or performance and the largest gains will be seen in systems with high interrupt rates.

3.2

Platform Identification and CPUID

In addition to verifying the processor signature, the intended processor platform type must be determined to properly target the microcode update. The intended processor platform type is determined by reading bits [52:50] of the IA32_PLATFORM_ID register, (MSR 17h) within the processor. This is a 64-bit register that must be read using the RDMSR instruction. The 3 Platform Id bits, when read as a binary coded decimal (BCD) number, indicate the bit position in the microcode update header's Processor Flags field that is asSoCiated with the installed processor.

undefined undefined undefined Executing the CPUID instruction with EAX=1 will provide the following information.

	EAX	Field Description
	[31:28]	Reserved
Ind	[27:20]	Extended Family value
redt	[19:16]	Extended Model value
defill	[15:13]	Reserved
	[12]	Processor Type Bit
sineo	[11:8]	Family value
den	[7:4]	Model value
J UI.	[3:0]	Stepping ID Value
d undefined un	[7:4]	Model value

References

efined un For further details on Intel[®] 64 and IA-32 architectures refer Intel[®] 64 and IA-32 Architectures Software Developer's Manual Combined Volumes:1, 2A, 2B, 2C, 3A, 3B, and 3C:

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Processor Core

For more details on AES-NI refer:

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Integrated Clock

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Integrated Clock

Idefined und Clocks are integrated, consisting of multiple variable frequency clock domains, across different voltage domains. This architecture achieves a low power clocking solution that supports the various clocking requirements of the SoC's many interfaces.Platform clocking is provided internally by the iClock block and does not require external devices for clocking. All the required platform clocks are provided by only two inputs: a 19.2 MHz primary reference for the integrated clock block and a 32.768 kHz reference for the Real Time Clock (RTC) block. Both of these would likely be implemented as ndefined und crystal references.

Table 38. **SoC Clock Inputs**

Table 38.	. SoC Clock Inputs		d une		nder	
	Clock Domain	Signal Name	Frequency	Usage/Description		
aned un	Main	ICLK_OSCIN ICLK_OSCOUT	19.2 MHz	Reference crystal for the iCLK PLL		
4 undern	RTC	RTC_X1 RTC_X2	32.768 kHz	RTC crystal I/O for RTC block		
etinec	LPC	LPC_CLKOUT	19.2 MHz	Can be configured as an input to compensate for board routing delays through Soft Strap.		

SoC Clock Outputs (Sheet 1 of 2) Table 39.

Table 39.	SoC Clock Outp	outs (Sheet 1 of 2)			UNC
ind	Clock Domain	Signal Name	Frequency	Usage/Description	
undefined undefined une	DDR	LPDDR3_M0_CK_P_A/B LPDDR3_M0_CK_N_A/B LPDDR3_M1_CK_P_A/B LPDDR3_M1_CK_N_A/B	800 MHz	Drives the Memory ranks 0-1. Data rate (MT/s) is 2x the clock rate.	
undefine	SDXC	MMC1_CLK SD2_CLK SD3_CLK	200 MHz	Clock for Storage Devices	-fined u
	SPI	SPI1_CLK FST_SPI_CLK	20 MHz, 33 MHz, 50 MHz	Clock for SPI flash	Junder
eined un	PMIC/COMMS	PMC_SUSCLK[0]	32.768 kHz	Pass through clock from RTC oscillator	
undefined undefined un	LPC	LPC_CLKOUT[0:1]	19.2 MHz	Provided to devices requiring LPC clock	
definet	Display Port	DDI[0]_TXP[3] DDI[0]_TXN[3]	162 or 270 MHz	Differential clock for DP devices	2
ed une	HDMI unde	DDI[2]_TXP[3] DDI[2]_TXN[3]	25-297 MHz	Differential clock for HDMI devices	defined
	ndefine		defined -	an a	ed une
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Integrated Clock



defined undefined undefined Table 39. SoC Clock Outputs (Sheet 2 of 2)

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	define		
able 39. SoC Clock Out	outs (Sheet 2 of 2)		inder
Clock Domain	Signal Name	Frequency	Usage/Description
HDMI DDC	DDI[2:0]_DDCCLK	100 kHz	Clock for HDMI DDC devices
MIPI DSI	MDSI_A_CLKP MDSI_A_CLKN MDSI_C_CLKP MDSI_C_CLKN	1000 MHz	Differential clock for MIPI DSI Devices
MIPI CSI	MCSI1_CLKP MCSI1_CLKN MCSI2_CLKP MCSI2_CLKN MCSI3_CLKP MCSI3_CLKN	200-400 MHz	Clocks for front and rear cameras
SVID	SVID_CLK	20 MHz	Clock used by voltage regulator
I ² S	LPE_I2S[2:0]_CLK	9.6 MHz	Continuous serial clock for I ² S interfaces
Platform Clocks SIO SPI I ² C NFC	PLT_CLK [5:0]	19.2MHz	Platform clocks.
SIO SPI	SPI CLK	15 MHz	SPI clock output
I ² C	I2C[6:0]_CLK	1.7MHz	I ² C clocks
NFC	NFC_I2C_CLK	100 kHz	Clock for NFC device
ned unde		defir.	ndefine
etined undefined unde	afined undefined s		offined undefined un
timed undefined	teffined u	ndefined un	I ² C clocks Clock for NFC device
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5



Power Up and Reset Sequence fined undefined undefined

This chapter provides information on the following topics:

- "Power Up Sequences"
- "Power Down Sequences
- "Reset Behavior"

defined undefine SoC System States

System Sleeping States Control (S-states) 5.1.1

The SoC supports the S0, S0i1, S0i2, S0i3, S4, and S5 sleep states. S4 and S5 states are identical from a hardware and power perspective. The differentiation is software determined (S4 = Suspend to Disk).

The SoC platform architecture assumes the usage of an external power management controller e.g., CPLD or PMIC. Some flows in this section refer the power management controller for support of the S-states transitions.

The SoC sleep states are described in Chapter 7, "Power Management".

5.2 **Power Up Sequences**

5.2.1

RTC Power Well Transition (G5 to G3 States Transition)

When RTC_VCC (Real Time Clock power) is applied via RTC battery, the following occurs (refer Figure 2 for timing):

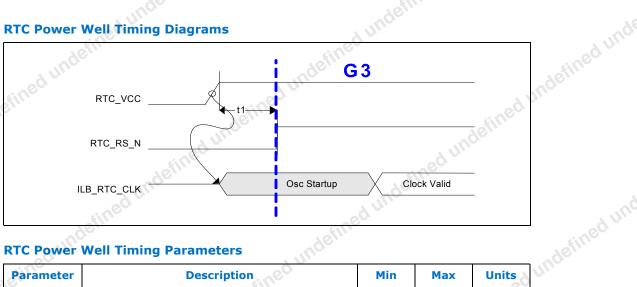
- 1. RTC_VCC ramps. RTC_RST_N should be low.
- 2. The system starts the real time clock oscillator.
- undefined undefined undefined undefined undefined undefined 3. A minimum of t1 units after RTC VCC ramps, the external RTC RC circuit de-asserts RTC_RST_N. The system is now in the G3 state. RTC oscillator is unlikely to be stable at this point.

n. Instimed undefi



ndefined undefine Power Up and Reset Sequence

Figure 2. **RTC Power Well Timing Diagrams**



Indefined undefined unde Table 40. RTC Power Well Timing Parameters

2	Parameter	Description	Min	Мах	Units
1	t1	RTC_VCC to RTC_RST_N de-assertion	9	-	ms

NOTES:

- 1. This delay is typically created from an RC circuit.
- 2. The oscillator startup times are component and design specific. A crystal oscillator can take several second to reach a large enough voltage swing. A silicon oscillator can have startups times <10 ms.
- 3. All VCC measurements points are at 90% nominal VCC voltage.

5.2.2 G3 to S4/S5

The timings shown in Figure 3 occurs when a board event such as AC power or power button is pressed. The following occurs:

- 1. Suspend well ramp in the order given.
- 2. The external power management controller de-asserts PMC_RSMRST_N after the suspend rails become stable.
- 3. PMC_SUSCLK will begin toggling after the de-assertion of PMC_RSMRST_N.
- undefined undefi 4. The system is now in S4/S5 state. Depending on policy bits, the system either wa undefined undefined undefined waits for a wake event, or continues to S0 states. S undefined unde



5.2.3 S4/S5 to S0

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- VCC, VNN and other S0 core voltage power rails may be enabled after the initiation of the S4/S5 to S0 event. The VCC and VNN voltage rails must be driven to the default values.
 After the PST.
- 3. After the DRAM power rail ramp, the external power management controller drives DRAM PWROK high.
- 4. After all of the S0 core voltage power rails are stable, external power management controller drives PMC_CORE_PWROK and VCCA_PWROK to HIGH.
- 5. The processor de-asserts PMC_PLTRST_N after PMC_CORE_PWROK is stable. The PMC_PLTRST_N is the main platform reset to other components.
- 6. The processor will begin fetching code from either the PCU-located SPI interface or defined u the LPC interface.

Figure 3. S4/S5 to S0 (Power Up) Sequence

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Cold Boot Sequencing	efine		efined une	
VSVS	mas		efin	
PWRBNTIN#	ed u.	, un		
PW RBTN#	ALL CONTRACTOR	cineo.		
Inoc		-deil.		
VSPOA		un	Jefined undefined	
VNN		inou		
V1P05A V1P8A	24		sineu	
VDDQ	100-		4611.	
V1P2A	du.			
V3P 3A				
PSMRST#	AG11.		sine	
SUSPWRDNACK	und		9 _{61.}	
DRAMPWROK-	cine ⁰	d th	~	
SLP_SOIX#	e	etino		
		nac	ed undefined	2
V1P15		-0 4		
VCC0		ci Det	6	
V0C1		elli	eine -	
V1P25X		P	- 9e.,	
V1P85X			, unc	
VDD0_VTT [*] VCCAPWROK			ed -	
	<u> </u>		1917	
COREP WROK			90.	
MODEM OFF	<u></u> 0			
SD WN#	- AIN ^O			
* V5P0A does not exist on a liappioned PMICs		a fine		
* In some configurations the SX rais are off by default				
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d undefine			6-	
		16th		
A UN	undefined un		tetined undefined	
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NOTES:

- defined undefined und 1. RTC and SUS power rails may come up at the same time if no RTC battery is used.
- 2. RTC clock should be oscillating, but may not be at 32.768 KHz yet.
- 3. Wake events show in figure are optional and depending on platform configuration.

5.3 **Power Down Sequences**

5.3.1^C

S0 to S4/S5 Sequence

Entry to Sleep states (S4, S5) is initiated by any of the following methods:

- Setting the desired sleep type in PM1_CNT.SLP_TYP and setting PM1_CNT.SLP_EN.
- Detection of an external catastrophic temperature event may cause a transition to G3, if the system is designed to do so.

The following sequence applies to S0-S4/S5 transitions.

- 1. The Operating System Power Management (OSPM) will handle the enabling or disabling of interrupt generation after S4 resume. The Operating System Power Management (OSPM) will need to read and clear Wake status information and the processing of the clearing wake status which will include enabling interrupts (both at the core level and platform level).
- 2. All interrupts in the processor need to be disabled before the S4 sequence is started (and re-enabled on exit). The CPU APIC must be disabled.
- ndefined undefined 3. When the desired sleep state is set in the PM1_CNT.TYP and PM1_CNT.SLP_EN registers, a sleep state request is sent to the PMC.
- 4. The PMC flushes all the internal buffers to main memory.

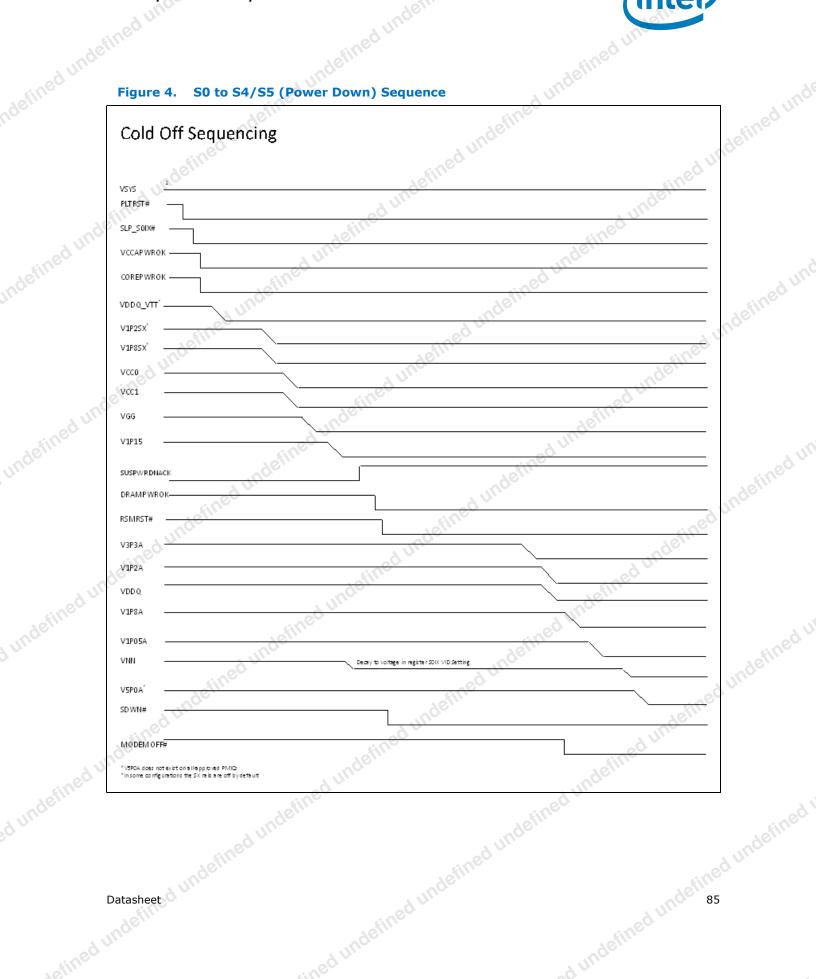
The Power Down Sequence is shown in Figure 4 below.

Other Assumptions:

- Entry to a Cx state is mutually exclusive with software-initiated entry to a Sleep state. This is because the processor(s) can only perform one register access at a time. This requirement is enforced by the CPU as well as the OS. The system may hang if it attempts to do a C-state and S-state at the same time.
- The G3 system state cannot be entered via any software mechanism. The G3 state indicates a complete loss of power. In this state, the RTC well may or may not be powered by an external coin cell battery.
- An external Power Management Controller (PMIC/EC) can be used to put the processor in G3 when the S4/S5 state is requested by the SoC. This is done to save power in S4/S5 state. This G3 like state is enabled by removing SUS rails via the SUSPWRDNACK pin. Doing so prevents the use of any of SUS wake events including USB, RTC, and GPIOs including the power button. The external Power Management Controller (or re-application of power) is required to return to S0. tundefined undefined undefined



S0 to S4/S5 (Power Down) Sequence Figure 4.





S4/S5 to S0 (Exit Sleep States) 5.3.2

Sleep states (S5) are exited based on Wake events. The Wake events will force the system to a full on state (S0), although some non-critical subsystems might still be powered down and have to be brought back manually. For example, the hard disk may be powered down during a sleep state, and have to be enabled via an I/O pin before it can be used. Upon exit from software-entered Sleep states (i.e., those initiated via the PM1 CNT.SLP EN bit), the PM1 STS EN.WAK STS bit will be set.

To enable Wake Events, the possible causes of wake events (and their restrictions) are shown in Table 41.

S4/S5 to S0 Cause of Wake Events Table 41.

	Cause	Туре	How Enabled	ed
	RTC Alarm	Internal	Set PM1_STS_EN.RTC_EN register bit	defini
	PMC_PWRBTN_N (Power Button)	External	Default enabled as Wake event	une
ed undefined un	GPIO_NORTH And GPIO_SOUTHWEST	External	GPE0a_EN register (after having gone to S5 via PM1_CNT.SLP_EN, but not after a power failure.) Note: GPIOs that are in the core well are not capable of waking the system from sleep states where the core well is not powered.	
define	GPIO_SOUTHEAST	External	Southeast GPIO can (optionally) be used as Wake sources based on GPIO register programming.	
	Primary PME_N	Internal	GPEOa_EN.PME_B0_EN register bit. This wake status bit includes multiple internal agents: EHCI (USB2)	undefine
adefined un	PMC - Initiated	Internal	No enable bits. The PMC can wake the host independent of other wake events listed, if desired. A bit is provided in PRSTS for reporting this wake event to BIOS. Note that this wake event may be used as a wake trigger on behalf of some other wake source.	

ndefined undefined un

Enter S0ix

The SOIX state is entered when the SoC is in a shallow sleep state. This state is entered when the SoC asserts the PMC_SLP_SOIX_N (LOW) pin to the PMIC. VDDQ_VTT and SX rails are turned off. The VCC rail is turned off by SVID commands (not by PMC_SLP_SOIX_N signal). The VNN rail is set to a voltage set in SVID address 39h. The rest of the VRs remain on but enters into PFM/power save mode.

5.3.4

Exit S0ix

The SOIX state is exited when the SoC de-asserts the PMC_SLP_SOIX_Npin (HIGH). VDDQ_VTT and SX rails are turned on. The VCC rail will be turned on by SVID commands (not by PMC_SLP_SOIX_N). The rest of the rails will come out of PFM/power save mode. All SMI/SCI events wake SoC from the S0ix states. The following table lists the addition events that wake the SoC from S0ix states.

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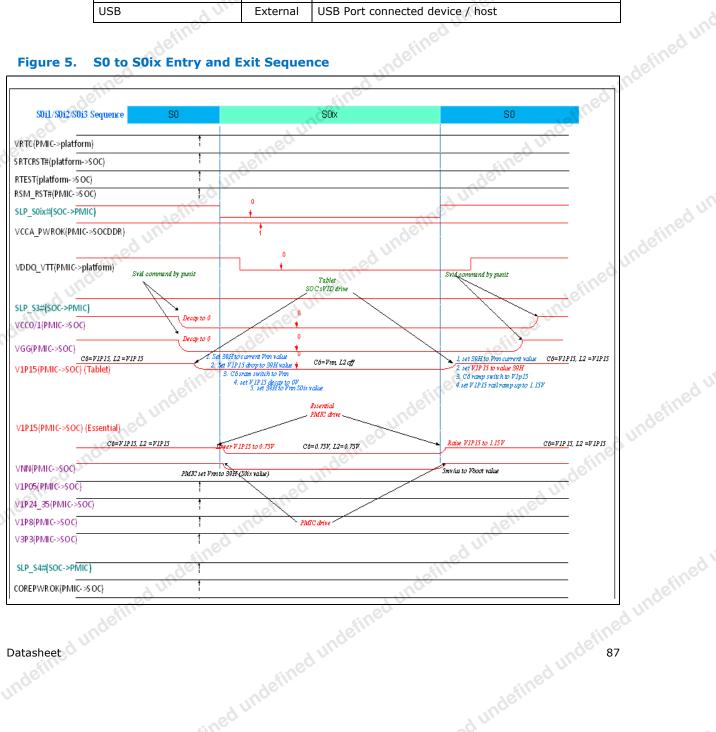
red undening Power Up and Reset Sequence



undefined undefined underined ndefined undefined Table 42. S0ix Cause of Wake Events

S0ix Cause of Wake E	sfine ^o	d undefined un	71.
Cause	Туре	How Enabled	sined u
Any GPIO	External	IO-APIC forwards the interrupt, resulting in S0 (as configured by BIOS). Alternatively use S0ix Wake Register (S0IX_WAKE_EN and S0IX_WAKE_STS) in PMC	dell
LPC CLKRUN	External	Wake from S0i2/3 only when the signal is asserted, moves the SoC to S0i1.	
ISH	External	From External Sensors	
USB	External	USB Port connected device / host	
50 to S0ix Entry and I	Exit Soquor	defined	sined u

undefined undefined undef Figure 5. S0 to S0ix Entry and Exit Sequence



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ndefined undefined Power Up and Reset Sequence



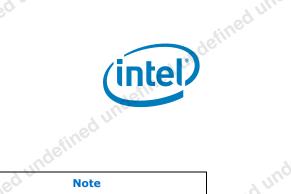
5.3.5 **Handling Power Failures**

undefined unde ndefined undefined undefined undefined The power failures can occur if the AC power or battery is removed. In this case, when the system was originally in a S0 state, power failure bit (GEN_PMCON1.PWR_FLR) is set after a power failure. Software can clear the bit.

Reset Behavior

	I ways to reset the processor.	
Table 43. Types of Resets	s (Sheet 1 of 2) Description	Note
Write of 0Eh to CF9 Register	Write of 0Eh to the CF9 register	TYPE 2: Host Reset with Power Cycle: Cold
PMC_RSTBTN_N & CF9h bit 3= 1	User presses the reset button, causing the PMC_RSTBTN_N signal to go active (after the debounce logic)	reset. PMC will lose all the information. All the functionality in SoC gets reset. The host system automatically is powered back up and brought out of reset to S0 state. SoC must not drop this type of reset
under.	ined un.	request if received while the system is in a software-entered S4/5 state.However, SoC is allowed to perform the reset without executing the RESET_WARN protocol in these states. If the system is in S5 due to a reset type #8 event, SoC is allowed to drop this type of reset request.
PMC_RSTBTN_N & CF9h bit 3= 0	User presses the reset button, causing the PMC_RSTBTN_N signal to go active (after the debounce logic)	TYPE 1:Host Reset with Power Cycle: Warm Reset 1. Host-Only functionality in SoC gets reset
Write of 06h to CF9 Register	Write of 06h to the CF9 register	2. Any functionality that needs to remain operational during a host reset must not
TCO watchdog timer	TCO timer reaches zero two times	 get reset. 3. PMC does not get reset. 4. RTC remain information. 5. Suspend well remain information 6. S4/S5 drop the warm reset request.
S4/S5	The processor is reset when going to S4 or S5 state	 TYPE 4: Sx Entry (host stays there) 1. All the Vnn reset by external power Good. Except: 1. PMC remain information. 2. RTC remain information. 3. Suspend well remain information
88 88 undefined undefined undefined	efilin aned undefined undefin	 2. RTC remain information. 3. Suspend well remain information Datasheet
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Table 43. Types of Resets (Sheet 1 of 2)



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Power Up and Reset Sequence	Jefine -	(Intel)
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Table 43. Types of Reset	s (Sheet 2 of 2)	ndetti
Trigger	Description	Note
Power Failure	PMC_CORE_PWROK signal goes inactive in S0/S1	TYPE 7: Global, Power Cycle Reset: S0->S4/S5->S0
Write of 06h or 0Eh to CF9 Register	CF9h global Reset bit = 1b	1. All the Vnn reset by external power
Host Partition Reset Entry Timeout	Host partition reset entry sequence took longer than the allowed timeout value (presumably due to a failure to receive one of the internal or external handshakes)	 Good. 2. All power wells that are controlled by the PMC_SLP_SOIX_N pins are turned off. 3. PMC get reset. 4. External Dram-unchanged Except: 1. RTC retain information. 2. Suspend well retain information.
Processor Thermal Trip	The internal thermal sensor signals a catastrophic temperature condition – transition to S5 and reset asserts	SOC_G3: Straight-to-S5 (thermal trip->SOC_G3) SOC power cycle: S0->SOC_G3 SOC lost all the info Except: RTC retain info
PMC_PWRBTN_N PMC_PWRBTN_N Power Button Override	10-second press causes transition to S5 (and reset asserts)	TYPE 8: Straight-to-S5 (Host stays there) SOC power cycle: S0->S4->S5 1. All the Vnn reset by external power
S4/S5 Entry Timeout	S4, or S5 entry sequence took longer than the allowed timeout value (presumably due to a failure to receive one of the internal or external handshakes)	 Good. 2. All power wells that are controlled by the PMC_SLP_SOiX_N pins are turned off. 3. External Dram-unchanged Except:
PMC Watchdog Timer	Firmware hang and Watchdog Timeout detected in the PMC platform	 PMC retain information. RTC retain information. Suspend well retain information
CPU Shutdown with Policy to assert PMC_PLTRST_N	Shutdown special cycle from CPU can cause either INIT or Reset Control-style PMC_PLTRST_N	Type 7:Global, Power Cycle Reset (if CF9h Global Reset bit = 1b) Type 2:Host Reset with Power Cycle (if CF9h Register bit 3 = 1b) Type 1:Host Reset without Power Cycle (others setting)
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Thermal Management

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6

6

Thermal Management

The SoC's thermal management system helps in managing the overall thermal profile of the system to prevent overheating and system breakdown. The architecture implements various proven methods of maintaining maximum performance while remaining within the thermal spec. Throttling mechanisms are used to reduce power consumption when thermal limits of the device are exceeded and the system is notified of critical conditions via interrupts or thermal signalling pins. SoC thermal management differs from legacy implementations primarily by replacing dedicated thermal management hardware with firmware.

The thermal management features are:

- Eight digital thermal sensors (DTS).
- Supports hardware trip point and four programmable trip points based on the temperature indicated by thermal sensors.
- Supports different thermal throttling mechanisms.

Thermal Sensors

SoC Sensors are based on DTS (Digital Thermal Sensor) to provide more accurate measure of system thermals.

The SoC has 8 DTS's. DTS provides as wires the current temperature around the real estate it occupies on SoC. These are driven to PM unit, which in turn monitor the temperature from DTS on the SoC.

DTS output are adjusted for silicon variations. For a given temperature the output from DTS is always the same irrespective of silicon.

Temperature Reading Based on DTS (Sheet 1 of 2)

Jefine	DTS Counter Value [8:0]	Temperature Reading (If T _{J-MAX} =90°C)	Temperature Reading (If T _{J-MAX} =100°C)	Temperature Reading (If T _{J-MAX} =110°C)	Temperature Reading (If T _{J-MAX} =100°C) Thermal Read Register [7:0]
20	127	90°C	100°C	110°C	100°C
	137	80°C	90°C	100°C	90°C
Idefined undefined u	147	70°C	80°C	90°C	80°C
d un.	157	60°C	70°C	80°C	70°C
atine	167	50°C	60°C	70°C	60°C
	177	40°C	50°C	60°C	50°C
	187	30°C	40°C	50°C	40°C
90 90 undefined	undefine	adef	ined undefined		Datashee
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ed undefined

DTS Counter Value [8:0]	Temperature Reading (If T _{J-MAX} =90°C)	Temperature Reading (If T _{J-MAX} =100°C)	Temperature Reading (If T _{J-MAX} =110°C)	Temperature Reading (If T _{J-MAX} =100°C) Thermal Read Register [7:0]	ndefined ut
197	20°C	30°C	40°C	30°C	
207	10°C	20°C	30°C	20°C	
217	0°C	10°C	20°C	10°C	
227	-10°C	0°C	10°C	0°C	
237	-20°C	-10°C	0°C	-10°C	
247	-30°C	-20°C	-10°C	-20°C	ineo '
257	-40°C	-30°C	-20°C	-28°C [255]	detin
247	-50°C	-40°C	-30°C	-28°C [255] 🔬	JUL

fined undefined undefine ndefined undefin Temperature Reading Based on DTS (Sheet 2 of 2) Table 44.

Note: 🕔 undefined undefin

DTS encoding of 127 always represents Tjmax. If Tjmax is at 100°C instead of 90°C then the encoding 127 from DTS indicates 100°C, 137 indicates 90°C and so forth.

Thermal trip points are of two types:

- Hard Trip: The Catastrophic trip points generated by DTS's based on predefined temperature setting defined in fuses.
- undefined • Programmable Trips: SoC provides four programmable trip settings (Hot, Aux2, Aux1, Aux0) that can be set by firmware/software. Default value for Hot Trip is from Fuses.

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DTS Timing

	2.0	7 N.		
undefined undefine	DTS should be enabled only counts from DTS to trigger t The figure below shows the	hermal events. P-Unit dete	ermines when DTS is enabled.	
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Figure 6.	DTS Operation Mode	de		
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Thermal Management



Hardware Trips 6.2

Catastrophic Trip (THERMTRIP) 6.2.1

Catastrophic trip is generated by DTS whenever the ambient temperature around it reaches (or extends) beyond the max value (indicated by a fuse). Catastrophic trip will not trip unless enabled (DTS are enabled only after HFPLL is locked). Within each DTS Catastrophic trips are flopped to prevent any glitches on Catastrophic signals from affecting the SoC behavior. Catastrophic trips are reset, once set, during power cycles.

Catastrophic trip signals from all DTS in the SoC are combined to generate THERMTRIP function which will in turn shut off all the PLL's and power rails to prevent SoC breakdown. To prevent glitches from triggering shutdown events, Catastrophic trip's from DTS's are registered before being sent out.

6.3

6.3.1

SoC Programmable Trips

Programmable trips can be programmed to cause different actions when triggered to reduce temperature of the die.

Aux3 Trip

By default, the Aux 3 (Hot Trip) point is set by software/firmware has an option to set these to a different value.

This trip point is enabled by firmware to monitor and control the system temperature while the rest of the system is being set up.

Aux2, Aux1, Aux0 Trip

These are fully programmable trip points for general hardware protection mechanisms. The programmable trips are only active after software/firmware enables the trip.

Note:

Unlike Aux3, the Aux[2:0] trip registers are defaulted to zero. To prevent spurious results, software/firmware should program the trip values prior to enabling the trip point.

Platform Trips 6.4

6.41

PROCHOT#

The platform components use the signal PROCHOT# to indicate thermal events to SoC. Assertion of the PROCHOT# input will trigger Thermal Monitor 1 or Thermal Monitor 2 throttling mechanisms if they are enabled. undefined undefined ur

Datasheet

Thermal Management



6.4.2 EXTTS

d undefined undefined undefine ndefined undefined und SoC does not support external thermal sensors and the corresponding bits in the P-Unit registers will be reserved for future use if needed.

For SoC, PROCHOT is the only mechanism for a platform component to indicate Thermal events to P-Unit.

sVID

When the Voltage Regulator (VR) reaches it's threshold (VR Icc Max, VR Hot), status bits in sVID are set. sVID sends SVID Status message to PUnit.

6.5

6.4.3

Dynamic Platform Thermal Framework (DPTF)

SoC is required to support interface for OS level thermal drivers and Intel's DPTF (Dynamic Platform and Thermal Framework) drivers to control thermal management. This interface provides high-level system drivers a mechanism to manage thermal events within the SoC with respect to events outside SoC. These events could potentially be triggered before PM Unit firmware performs active management as DPTF/OS level drivers respond to events on platform outside of SoC.In addition, these interfaces also respond to interrupts from within the SoC.

Platform level thermal management layout is shown in the figure below.

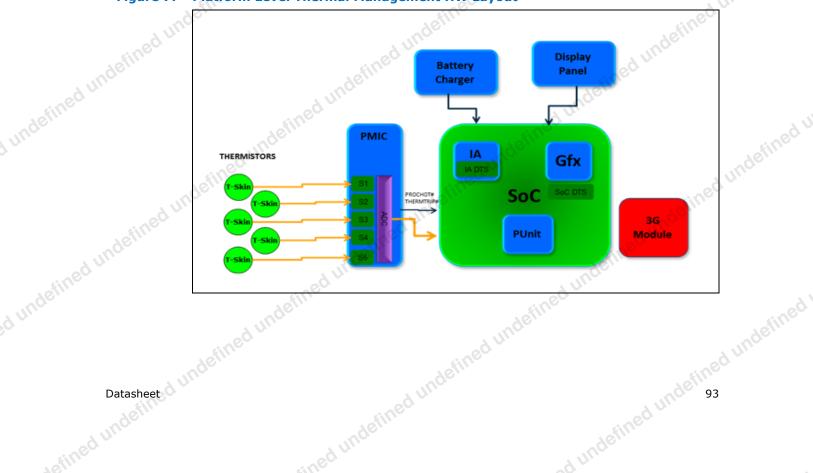


Figure 7. **Platform Level Thermal Management HW Layout**

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defined undefined undefined undefined unde The thermal events happen outside of SoC on platform level are reported as interrupts from PMIC. PMIC monitors a number of catastrophic and critical thermal events, such as PMIC over-temperature, system over-temperature (reported by skin sensors), and

Thermal Status The firmware capture to trigger them action The firmware captures Thermal Trip events (other than THERMTRIP) in status registers , of pr. a underned to trigger thermal actions. Associated with each event is a set of programmable

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7.1



Power Management

fined undefined und This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- Integrated Graphics Controller

Features

- ACPI System States support (S0, S0i1, S0i2, S0i3, S4, S5).
- Processor Core/Package States support (C0 C7).
- SoC Graphics Adapter States support D0 D3.
- Supports CPU and GFx Burst.
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers).
- Active power down of display links.

7.2 **States Supported**

The Power Management states supported by the processor are described in this defined undefined section.

7.2.1

System States

Table 45. General Power States for System (Sheet 1 of 2)

			-
indefinec	States/Sub- states	Legacy Name / Description	ed
	G0/S0/C0	FULL ON: CPU operating. Individual devices may be shut down to save power. The different CPU operating levels are defined by Cx states.	ndefine
	G0/S0/Cx	Cx State: CPU manages C-state itself.	
stined un	G0/S0i1	S0i1 State: Low power platform active state. All DRAM and IOSF traffic are halted. PLL are configured to be off. This state allows MP3 playing using ISH/LPE engine	
nde	G0/S0i2	S0i2 State: The SoC clocks and oscillators are parked	
ed u.	G0/S0i3	S0i3 State: All SoC clocks and oscillators are turned off	
Datasheet	defined undefin	need undefined undefined c	ad undefined
Jefined under		ned undefine	



States/Sub- states	Legacy Name / Description	ined ut
G1/S4	Suspend-To-Disk (STD): The context of the system is maintained on the disk. All of the power is shut down except power for the logic to resume. The S4 and S5 states are treated the same.	Indefit
G2/S5	 Soft-Off: System context is not maintained. All of the power is shut down except power for the logic to restart. A full boot is required to restart. A full boot is required when waking. The S4 and S5 states are treated the same. 	
G3	Mechanical OFF. System content is not maintained. All power shutdown except for the RTC. No "Wake" events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3.	defined "

Table 45. General Power States for System (Sheet 2 of 2)

Table 48 shows the transitions rules among the various states.

Note:

Transitions among the various states may appear to temporarily transition through intermediate states. These intermediate transitions and states are not listed in the table.

Table 46. **Cause of Sx Wake Events**

table.	Inder	lefine
Cause of Sx Wake E	vents sined un	d ur
Cause	How Enabled	define
RTC Alarm	Set RTC_EN bit in PM1_EN Register	4 UNC
Power Button	Always enabled as Wake event from Sx	sineo
PMC_SLP_S4_N	None	dell
PMC_BATLOW_N	None	od un
PMC_SUS_STAT_N	None	atine
PMC_SLP_S0IX_N	None	9.0
PMC_ACPRESENT	None	2 A A
PMC_PLTRST_N	None	sinec
PMC_SUSCLK[0]	None	ndell

The following shows the differences in the sleep states with regards to the processor's output signals.

Table 47. SoC Sx-States to SLP_S*# (Sheet 1 of 2)

ined un.	State	SOUN	S4	S 5	Reset w/o Power Cycle	Reset w/ Power Cycle
N*	CPU Executing	In C0	OFF	OFF	No	OFF
	PMC_SLP_S4_N	HIGH	LOW	LOW	HIGH	LOW
96	undefin			d undef	Iner	

Datasheet -4 undefined



ndefined undefined SoC Sx-States to SLP S*# (Sheet 2 of 2) Table 47.

SoC Sx-States to SLP_S*# (Sheet 2 of 2)			ind	affined un			
	State	S0	S4	S 5	Reset w/o Power Cycle	Reset w/ Power Cycle	ined und
	S0 Power Rails	ON	OFF	OFF	ON	OFF	delli
11	PMC_PLTRST_N	0	1	120	1	1	-d ulli-
	PMC_SUS_STAT_N	HIGH	LOW	LOW	HIGH	LOW	^C

NOTE: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S4_N. PMC_SUS_STAT_N is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT_N also warns of upcoming reset. unde

undefined undefined undef **ACPI PM State Transition Rules**

Table 48.	ACPI PM Sta	ite Transition Rules	d undern	
Inde.	Present State	Transition Trigger	Next State	lefined u.
	G0/S0/C0	IA Code MWAIT or LVL Rd	C0/S0/Cx	noc
und	S// .	PM1_CNT.SLP_EN bit set	G1/Sx or G2/S5 state (specified by PM1_CNT.SLP_TYP)	
sineo		Power Button Override	G2/S5	
dell		Mechanical Off/Power Failure	G3	
defined un	G0/S0/Cx	Cx break events which include: CPU snoop, MSI, Legacy Interrupt, AONT timer	G0/S0/C0	nu .
uno		Power Button Override	G2/S5	red
	d un.	Resume Well Power Failure	G3	defin
	G1/S4	Any Enabled Wake Event	G0/S0/C0	JUG
- inf		Power button Override	G2/S5	
ed u		Resume Well Power Failure	G3	
defille	G2/S5	Any Enabled Wake Event	G0/S0/C0	
, una		Resume Well Power Failure	G3	
d undefined undefinec	G3	Power Returns	Option to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other enabled wake event) or G1/S4 (if system state was S4 prior to the power failure). Some wake events are preserved through a power failure.	undefined

	tines.			6	preserved through a	power failure.	- unc.
7.2.2 Table 49.			e Combin mbinations	ations (Sheet 1 of 2))	tined undefin	
undefined L	Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description	ed
	G0	S0	C0	Full On	On	Full On	16111
	undefine			ndefined	D.	ing i	ned und
Datasheet			undefine	d un		efined unoe	97
Jefine -		in P	20		d une	*	



G, S and	C State Co	mbinations (Sheet 2 of 2)	undein	led under.	1
Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description	adefined u
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt	uno
G0	S0	C6	Deep Power Down	On	Deep Power Down	
G0	S0ix	C7	Deep Power Down	On	Deep Power Down	
G1	S4	Power off		Off except RTC & internal ring OSC	Suspend to Disk	
G2	S5	Power off		Off except RTC & internal ring OSC	Soft Off	ed
G3	NA	Power Off	a ¹	Power off	Hard Off	1efine
• –		aphics Dis ter State Con	play State	25	aed undefine	d undefined
	State	under.	Description	. 68	ine	
D0		Full on, Di	splay active	4 Miller		
D3	811.	Power off	diamlay			

Table 49. G, S and C State Combinations (Sheet 2 of 2)

7.2.3 Integrated Graphics Display States

Table 50. SoC Graphics Adapter State Control

	State	Description	
D0	ed t	Full on, Display active	24
D3	4efin	Power off display	sineu
		•	Yer

Integrated Memory Controller States 7.2.4

Table 51. Main Memory States

otato		
DO	Full on, Display active	
D3	Power off display	ed u
Integrated Memo	ory Controller States	indefine
defile	Leftmer ine	d u.
Main Memory States	unoc detti	
States	Description	
Powerup	CKE asserted. Active mode.	
Precharge Powerdown	CKE de-asserted (not self-refresh) with all banks closed.	
Active Powerdown	CKE de-asserted (not self-refresh) with at least one bank active.	
Self-Refresh	CKE de-asserted using device self-refresh	sine

Table 52. D, S and C State Combinations (Sheet 1 of 2) ed undefined undefined

÷			A /2. V		
defined undefined u	Graphics Adapter (D) State	Sleep (S) State	(C) State	Description	
nder	D0	SO	C0	Full On, Displaying	
od un	D0	S0	C1	Auto-Halt, Displaying	
efine	D0	S0 S0	C6	Deep Sleep, Display Off	
98	undefined und		undefined un	Datasheet	led undefine
so undefined		ned undefined		a undefined u	



D, S and C State Combinations (Sheet 2 of 2) Table 52.

D, S and C State (Combinations (Sh	eet 2 of 2)	under.	
Graphics Adapter (D) State	Sleep (S) State	(C) State	Description	sined un
D0	S0ix	C7	Deep Sleep, Display Off	9eur
D3	S0/S0ix	Any	Not Displaying	
D3	S4 🔪		Not Displaying	
	med une		Suspend to disk Core power off	

fined undefined undef

Processor Core Power Management

While executing code, Enhanced Intel SpeedStep[®] Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

7.3.1

Enhanced Intel SpeedStep[®] Technology

The following are the key features of Enhanced Intel SpeedStep[®] Technology:

- Applicable to Processor Core Voltage and Graphic Core Voltage
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency:
 - If the target frequency is higher than the current frequency, Core_VCC is ramped up slowly to an optimized voltage. This voltage is signaled by the SVID signals to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
 - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the SVID signals.
- The processor controls voltage ramp rates by requesting appropriate ramp rates from an external SVID controller.
- Because there is low transition latency between P-states, a significant number of indefined undefined undefined undefined undefined transitions per second are possible.
- Thermal Monitor mode.
 - Refer Chapter 6, "Thermal Management"



7.3.3

7.3.2 **Dynamic Cache Sizing***

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following condition:

- The C0 timer that tracks continuous residency in the Normal state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The predefined L2 shrink threshold is triggered.

Low-Power Idle States

When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-state. However, ned undefit higher C-states have longer exit and entry latencies. Resolution of C-state occur at the thread, processor core, and processor core level.

Clock Control and Low-Power States* 7.3.3.1

The processor core supports low power states at core level. The central power management logic ensures the entire processor core enters the new common processor core power state. For processor core power states higher than C1, this would be done by initiating a P LVLx (P LVL4 & P LVL6) I/O read to all of the cores. States that require external intervention and typically map back to processor core power states. States for processor core include Normal (C0, C1), and Stop Grant.

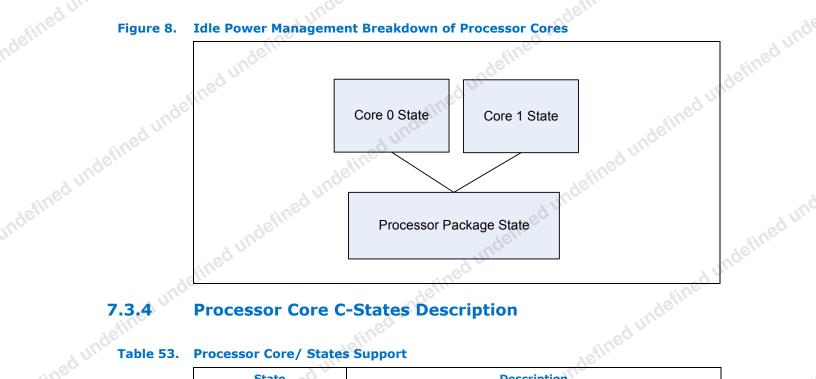
The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state specifies and P LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P LVLx I/O read interface. The sub-state specifications used for each P LVLx read can be configured in a software programmable MSR by BIOS.

undefined undefined undefined undefined undefined undefined The Cx state ends due to a break event. Based on the break event, the processor returns the system to C0. The following are examples of such break events:

- Any unmasked interrupt goes active
- Any internal event that will cause an NMI or SMI_B
- CPU Pending Break Event (PBE_B) st



Figure 8. **Idle Power Management Breakdown of Processor Cores**



7.3.4 **Processor Core C-States Description**

Table 53. **Processor Core/ States Support**

State	Description	
CO	Active mode, processor executing code	edu
C1	AutoHALT state	defille
C1E	AutoHALT State with lowest frequency and voltage operating point.	unos
C6	Deep Power Down. Prior to entering the Deep Power Down Technology (code named C6) State, The core process will flush its cache and save its core context to a special on die SRAM on a different power plane. Once Deep Power Down Technology (code named C6) sequence has completed. The core processor's voltage is completely shut off.	
C7 med C	Execution cores in this state behave similarly to the C6 state. Voltage is removed from the system agent domain	
The following state descr state.	riptions assume that both threads are in common low power	undefined
Core C0 State	indefine	
5	C0 C1 C1E C6 C7 The following state descr state.	C0Active mode, processor executing codeC1AutoHALT stateC1EAutoHALT State with lowest frequency and voltage operating point.C6Deep Power Down. Prior to entering the Deep Power Down Technology (code named C6) State, The core process will flush its cache and save its core context to a special on die SRAM on a different power plane. Once Deep Power Down Technology (code named C6) sequence has completed. The core processor's voltage is completely shut off.C7Execution cores in this state behave similarly to the C6 state. Voltage is removed from the system agent domainThe following state descriptions assume that both threads are in common low power state.

Core C0 State 7.3.4.1

The normal operating state of a core where code is being executed.

7.3.4.2 **Core C1/C1E State**

A undefined undefined undefined C1/C1E is a low power state entered when a core execute a HLT or MWAIT(C1/C1E) instruction.

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A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. Refer Intel[®] 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, refer Section 7.3.8.2, "Package C1/C1E".

Core C6 State

Individual core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM.Once complete, a core will have its voltage reduced. During exit, the core is powered on and its architectural state is restored.

7.3.4.4 Core C7 State

7.3.4.5

Individual core can enter the C7 state by initiating a P_LVL7 I/O read or an MWAIT(C7) instruction. The core C7 state exhibits the same behavior as core C6 state, but in addition gives permission to the internal Power Management logic to enter a package S0ix state if possible.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore incorrect or inefficient usage of deeper C-states has a negative impact on battery life. In order to increase residency and improve battery life in deeper C-states, the processor supports C-state auto-demotion.

This is the C-State auto-demotion option:

• C7/C6 to C1

The decision to demote a core from C7/C6 to C1 is based on each core's immediate residency history. Upon each core C7/C6 request, the core C-state is demoted to C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C6 or C7.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.



7.3.5 Module C-states

Table 54. **Module C-states**

Module C- Module C-stat		defined undefined un	defined unde
C-states	Core Status	Cache status	dunc
C0	At least one core in CO	Normal Operation	6°
C1	Both cores HALTed. Most clocks OFF	No Cache flushed; Snoops wake up cores	•
C6	Both cores in C6 (powered off) CPLL bypassed (powered off) CPU Refclk OFF BIU domain powered off	Core DL1s flushed L2 flushed L2 domain powered off C2 popup NOT required	od und

Module C6 7.3.6

There are two module C-states the Punit can put a CPU module into depending on the type of C-state entry sub-state hint and remaining size of L2. In this module C-state, both cores are power gated and all ways of L2 cache can be flushed. In this state, the Punit can power gate the BIU/L2 Vcc domain as well as the VCCSRAM_GT domain.

7.3.7 **S0i1**

Once the core has entered package C6 or C7, the SoC can transition to S0i1. S0i1 transitions from a PC6 means that L2 state will be preserved through S0i1. Transitions from C7 no longer have state retention. These two paths are quite different due to the requirements on the L2 power rails and the need to snoop the core.

7.3.8ò

Package C-States*

The processor supports C0, C1/C1E,C6 and C7 power states. The following is a summary of the general rules for package C-state entry. These apply to all package Cstates unless specified otherwise:

- Package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
- Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
- The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected.



7.3.8.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E via MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E via the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E.

7.3.8.3 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C7 state but has allowed a package C6 state.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts.

.4 Package C7 State

A processor enters the package C7 low power state when all cores are in the C7 state. In package C7, the processor will take action to remove power from portions of the system agent.

Core break events are handled the same way as in package C6.

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7.3.9 Graphics, Video and Display Power Management

7.3.9.1 Graphics and video decoder C-State

GFX C-State (GC6) are designed to optimize the average power to the graphics and video decoder engines during times of idleness. GFX C-state is entered when the graphics engine, has no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the processor will power gate the Graphics and video decoder engines.

7.3.9.2 Intel[®] Display Power Saving Technology (Intel[®] DPST)

The Intel DPST technique achieves backlight power savings while maintaining visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user image quality at a decreased backlight power level.

- The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel[®] DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
- 2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
- 3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image. Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

7.3.9.3

Intel[®] Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the back light setting.

7.3.9.4

Intel[®] Seamless Display Refresh Rate Switching Technology (Intel[®] SDRRS Technology)

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel[®] Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when on plugged in power or when the end user has not selected/



enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the design application is on battery power and when the user has selected/enabled this feature.

There are two distinct implementations of Intel SDRRS—static and seamless. The static Intel SDRRS method uses a mode change to assign the new refresh rate. The seamless Intel SDRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.

Memory Power Management

The main memory is power managed during normal operation and in low-power states.

7.4.1

1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as unpopulated, or single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

7.4.2

DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

7.4.2.1 Initialization Role of CKE*

During power-up, CKE is the only input to the SDRAM that is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power- up.

CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

Datasheet



Conditional Self-Refresh 7.4.2.2

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package low-power states. RMPM functionality depends on graphics/ display state (relevant only when internal graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then places all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package low-power states as long as there are no memory requests to service.

7.4.2.3 **Dynamic Power Down Operation**

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power down state. The processor core controller can be configured to put the devices in active power down (CKE deassertion with open pages) or precharge power down (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

DRAM I/O Power Management 7.4.2.4

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to undefined undefine prevent spurious results due to noise on the unused signals (typically handled J). Sector Datasheet undermed under med under me automatically when input receiver is disabled).

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System Memory Controller

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. 8.1

System Memory Controller

The system memory controller supports DDR3L-RS/LPDDR3 protocol with up to two 64bit wide dual rank channels at data rates up to 1600 MT/s with ECC is also available on a single DDR3L-RS channel.

Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- , undefined " • **Description**: A brief explanation of the signal's function.

DDR3L-RS Interface Signals 8.1.1

Table 55. Memory Channel 0 DDR3L-RS Signals (Sheet 1 of 2)

Indefined Table 55.	Memory Channel 0 DDR		edunt	d un
Table 55.	Signal Name	Direction Type	Description	4 undefines
ad ut	DDR3_M0_CK[1,0]_P DDR3_M0_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.	⁶ 0
ndefine	DDR3_M0_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.	
undefined undefines	DDR3_M0_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.	
d unde.	DDR3_M0_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.	ofined u
	DDR3_M0_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.	od unde.
ined	DDR3_M0_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands	le.
sined undefit.	DDR3_M0_CAS_N	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands	
o undefinec	DDR3_M0_WE_N	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.	Lefined !
	ndefined		Jefined un	med unoc
108 Latined			Datashe	eet
Jeffined unde	cined	undefin	od undefinec	

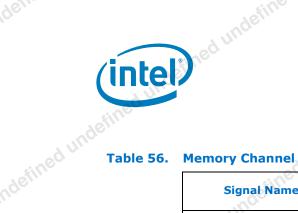


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			ad une
System Memor	y Controller	ined unde	sined un
Table 55.	Memory Channel 0 DDR	Direction	nals (Sheet 2 of 2)
c.	DDR3_M0_DQ[63:0]	I/O DDR3	Data Lines: Bidirectional signals between DRAM/ PHY
ined under	DDR3_M0_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
	DDR3_M0_DQS[7:0]_P DDR3_M0_DQS[7:0]_N	I/O DDR3	Data Strobes: The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
AG	DDR3_M0_ODT[1,0]	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
tined unc	DDR3_M0_RCOMPD	I DDR	Resistor Compensation: This signal needs to be terminated to VSS on board. This signal is driven from external clock source.
	DDR3_M0_OCAVREF	O DDR	Reference Voltage: DDR3 CA interface Reference Voltage
-	DDR3_M0_ODQVREF	O DDR	Reference Voltage: DDR3 DQ interface Reference Voltage
2	DDR3_CORE_PWROK	I DDR	Core Power OK: This signal indicates the status of the DRAM Core power supply (power on in S0).Active high signal indicates that DDR PHY voltage(1.5v) is good.
ined une	DDR3_VDD_S4_PWROK	I DDR	VDD Power OK: Asserted once the VRM is settled.
efined und Table 56.	DDR3_M0_DRAMRST_N	etino	DRAM Reset: This signal is used to reset DRAM devices.
Table 56.	Memory Channel 1 DDR	3L-RS Sig	nals (Sheet 1 of 2)
	Signal Name	Direction Type	Description
	DDR3_M1_CK[1,0]_P DDR3_M1_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.
JUN	DDR3_M1_CS[1,0]_N	0	Chip Select: (1 per Rank). Driven by PHY to

a undefined undefined und Table 56. Memory Channel 1 DDR3L-RS Signals (Sheet 1 of 2)

AU				
June	Signal Name	Direction Type	Description	defined
	DDR3_M1_CK[1,0]_P DDR3_M1_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.	ed unos
eined un	DDR3_M1_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.	
d under.	DDR3_M1_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.	
adefinec	DDR3_M1_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.	
ed un	DDR3_M1_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.	odefined
	ndefine	·	defineo	red un
Datasheet		ined '	une dunden	.09
ed unot	<u>_ 1</u>	Indefin	adefines	
1 efint	cine0		d ^u	-



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intel	med c	defined une	
afined D.		stined unc	
Table 56.	Memory Channel 1 DDF	© R3L-RS Signals (Sheet 2 of	2)

	0.00	Direction	nals (Sheet 2 of 2)	ן
	Signal Name	Туре	Description	eine
	DDR3_M1_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands	nudell
ined un	DDR3_M1_CAS_N	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands	
ned undefined u.	DDR3_M1_WE_N	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.	
	DDR3_M1_DQ[63:0]	I/O DDR3	Data Lines: Bidirectional signals between DRAM/ PHY	nia
	DDR3_M1_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.	J under
ined undefined un	DDR3_M1_DQS[7:0]_P DDR3_M1_DQS[7:0]_N	I/O DDR3	Data Strobes: The data is captured at the crossing point of DDR3_M1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.	
	DDR3_M1_ODT[1,0]	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.	1611
	DDR3_M1_DRAMRST_N	0	Reset DRAM: This signal can be used to reset DRAM devices.	d unor

	denn-	-	DRAM devices.	ed V
8.1.2 ^{cd ut}	DDR3L-RS Interfa	ice Sign	als dundefin	-
Table 57.	Memory Channel 0 DDR	3L-RS Sig	nals (Sheet 1 of 2)	
defined	Signal Name	Direction Type	Description	
d une	DDR3_M0_CK[1,0]_P DDR3_M0_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.	defineo
	DDR3_M0_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.	ed un
tined u	DDR3_M0_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.	
d under	DDR3_M0_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.	
ndefine	DDR3_M0_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.	· / /
ed un	DDR3_M0_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands	indefine
110	unden		Datashe	ned to
ed undefine		undefined	a codefined unasic	
retim	eineo		d ^u .	



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	Memory Channel 0 DDR	ned ^W	nals (Shoet 2 of 2) defined un	
_	in ^{eo}	JL-KJ JIU		
	Signal Name	Direction Type	Description]
A 1778 V	DDR3_M0_CAS_N	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands	Indef
undefined unde	DDR3_M0_WE_N	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.	
TUR	DDR3_M0_DQ[63:0]	I/O DDR3	Data Lines: Bidirectional signals between DRAM/ PHY	1
	DDR3_M0_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.	nde
	DDR3_M0_DQS[7:0]_P DDR3_M0_DQS[7:0]_N	I/O DDR3	Data Strobes: The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.	01.
· ·	DDR3_M0_ODT[1,0]	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.	1
	DDR3_M0_RCOMPD	I DDR	Resistor Compensation: This signal needs to be terminated to VSS on board.This signal is driven from external clock source.	
6.	DDR3_M0_OCAVREF	O DDR	Reference Voltage: DDR3 CA interface Reference Voltage	d un
fined un-	DDR3_M0_ODQVREF	O DDR	Reference Voltage: DDR3 DQ interface Reference Voltage	1
under	DDR3_CORE_PWROK	I DDR	Core Power OK: This signal indicates the status of the DRAM Core power supply (power on in S0).Active high signal indicates that DDR PHY voltage(1.5v) is good.	
F	DDR3_VDD_S4_PWROK	I DDR	VDD Power OK: Asserted once the VRM is settled.	dun
	DDR3_M0_DRAMRST_N		DRAM Reset: This signal is used to reset DRAM devices.	Jun



defined undefined underimed Table 58. Memory Channel 1 DDR3L-RS Signals

able 58. Memory Channel 1 DDR3 Signal Name DDR3_M1_CK[1,0]_P DDR3_M1_CK[1,0]_N DDR3_M1_CS[1,0]_N	Direction Type O	nals Description
Signal Name DDR3_M1_CK[1,0]_P DDR3_M1_CK[1,0]_N	Direction Type O	$a_{0} \psi_{N}$
DDR3_M1_CK[1,0]_N		
	DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.
-0 ⁻¹	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.
DDR3_M1_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.
DDR3_M1_CS[1,0]_N DDR3_M1_CKE[3,0] DDR3_M1_MA[15:0] DDR3_M1_BS[2:0]	O DDR3	Memory Address: Driven by PHY to DRAM.
DDR3_M1_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.
DDR3_M1_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands
DDR3_M1_CAS_N	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands
DDR3_M1_CAS_N DDR3_M1_WE_N DDR3_M1_DQ[63:0]	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
DDR3_M1_DQ[63:0]	I/O DDR3	Data Lines: Bidirectional signals between DRAM/ PHY
DDR3_M1_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DDR3_M1_DQS[7:0]_P DDR3_M1_DQS[7:0]_N	I/O DDR3	Data Strobes: The data is captured at the crossing point of DDR3_M1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DDR3_M1_ODT[1,0]	O DDR3	 whereas in the Write command, the strobe crossing is in the centre of the data window. On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write. Reset DRAM: This signal can be used to reset DRAM devices.
DDR3_M1_DRAMRST_N	0	Reset DRAM: This signal can be used to reset DRAM devices.



defined undefined undermed ndefined undefined LPDDR3 Interface Signals 8.1.3

Table 59. Memory Channel 0 LPDDR3 Signals

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	8.1.3	LPDDR3 Interface	Signals	s and unoc	
	Table 59.	Memory Channel 0 LPDI	OR3 Signal	ls adefine	lefineo
		Signal Name	Direction Type	Description	unoc
dun	defined une	LPDDR3_M0_CK_P_A/B LPDDR3_M0_CK_N_A/B	O DDR3	SDRAM and inverted Differential Clock: (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.	
efinec		LPDDR3_M0_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Used to qualify the command on the command bus for a particular rank.	. ned
	ined und	LPDDR3_M0_CKE[1,0]_ A/B	O DDR3	Clock Enable: (power management) It is used during DRAM power up/power down and Self refresh. NOTE: LPDDR3 uses only LPDDR3_M0_CKE[2,0]. LPDDR3_M0_CKE[1,3] are not being used for LPDDR3.	d undefin
defined ut	ndefined und	LPDDR3_M0_CA[9:0]	O DDR3	Memory Address: Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol w.r.t. LPDDR3_M0_CKN, LPDDR3_M0_CKP pairs	
		LPDDR3_M0_DQ[31:0]_ A/B	I/O DDR3	Data Lines: Data signal interface to the DRAM data bus	define
	atined un	LPDDR3_M0_DM[3:0]_A /B	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.	ed un
idefined l	Indefined un	LPDDR3_M0_DQS[3:0]_ P_A/B LPDDR3_M0_DQS[3:0]_ N_A/B	I/O DDR3	Data Strobes: The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.	sine
		LPDDR3_M0_ODT_A/B	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.	d undefine
	undefinedur	LPDDR3_M0_RCOMPD	I DDR	Resistor Compensation: This signal needs to be terminated to VSS on board. This signal is driven from external clock source.	-20
	under	LPDDR3_M0_OCAVREF	O DDR	Reference Voltage: LPLPDDR3 CA interface Reference Voltage	1
odefineo		LPDDR3_M0_ODQVREF	O DDR	Reference Voltage: LPLPDDR3 DQ interface Reference Voltage	-
<i>.</i> ,		Indefined unde	1	Jefined under	ined undefin
	Datasheet	<i>b</i> .		uno-	113
ed		ال ۲	ndefine	under undefined undef	
1efins		cineo		d ^u	



undefined undefined undefined Table 60. Memory Channel 1 LPDDR3 Signals

Table 60.	Memory Channel 1 LP	_	als ed un	I
	Signal Name	Direction Type	Description	defi
	LPDDR3_M1_CK_P_A/B LPDDR3_M1_CK_N_A/B	O DDR3	SDRAM and inverted Differential Clock: (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.	JUL
de	LPDDR3_M1_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Used to qualify the command on the command bus for a particular rank.	
F	LPDDR3_M1_CKE[1,0]_ A/B	O DDR3	Clock Enable: (power management) It is used during DRAM power up/power down and Self refresh. NOTE: LPDDR3 uses only LPDDR3_M1_CKE[0,2]. LPDDR3_M1_CKE[1,3] are not being used for LPDDR3.	unde
defined un	LPDDR3_M1_CA[9:0]	O DDR3	Memory Address: Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol relative to LPDDR3_M1_CKN, LPDDR3_M1_CKP pairs	
	LPDDR3_M1_DQ[31:0] A/B	I/O DDR3	Data Lines: Data signal interface to the DRAM data bus.	
	LPDDR3_M1_DM[3:0]_A /B	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.	nd
	LPDDR3_M1_DQS[3:0]_ P_A/B LPDDR3_M1_DQS[3:0]_ N_A/B	I/O DDR3	Data Strobes: The data is captured at the crossing point of LPDDR3_M1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.	9 01
	LPDDR3_M1_ODT_A/B	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.	
	LPDDR3_M1_OCAVREF	O DDR	Reference Voltage: LPDDR3 CA interface Reference Voltage	
	LPDDR3_M1_ODQVREF	O DDR	Reference Voltage: LPDDR3 DQ interface Reference Voltage	Jun

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ECC Support

The system memory controller supports ECC. When ECC is enabled, only Memory Channel 0 will be active. Memory Channel 1 will be disabled and used for the ECC data pins. The table below shows the details on the muxing relationship between the ECC med undefined Signals and the Memory Channel 1 signals.

Note:

ECC SO-DIMMs are not backwards compatible with non-ECC SO-DIMMs.



Table 62. ECC Signals

i.	ined und	ined united	
ECC Signals		od underti	und
Signal Name	Direction Type	Description	defined
DDR3_M0_ECC_DQ[7:0]	I/O DDR3	ECC Check Data Bits These are muxed with channel 1.	IUC
DDR3_M0_ECC_DM	O DDR3	ECC Data Mask: DM is an optional output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of ECC_DQS. This signal is muxed with channel 1 and may not be needed.	4 und
DDR3_M0_ECC_DQSP DDR3_M0_ECC_DQSN	I/O DDR3	ECC Data Strobes: The data is captured at the crossing point the 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window. These are muxed with channel 1.	undefineo

Features

undefined undefined unde System Memory Technology Supported

The system memory controller supports the following DDR3L-RS/LPDDR3 Data Transfer Rates, DRAM Device Technologies:

- DDR3L-RS/LPDDR3 Data Transfer Rates: 1600MT/s (12.8 GB/s per channel).
- LPDDR3 (1.2V DRAM VDDQ)
- DDR3L-RS (1.35V DRAM interface I/Os)
- DDR3L-RS DRAM Device Technology
 - Standard 2 Gb technologies and addressing
 - Read latency 5, 6, 7, 8, 9, 10, 11, 12, 13
 - Write latency 3, 4, 5, 6, 7, 8
- LPDDR3 DRAM Device Technology
 - x64, 253 ball LPDDR3 DRAM package
 - 8 GB (2 rank per channel) package density
- idefined undefined undefined u Standard 2 Gb, 4 Gb and 8 Gb DRAM technologies and addressing
 - Read latency 5, 6, 7, 8, 9, 10, 11, 12, 13
 - Write latency 3, 4, 5, 6, 7, 8
- Supports Trunk Clock Gating
- ECC supports 64-bit data bus on DDR3L-RS single channel
- Supports early SR exit
- Supports slow power down
- Supports CA tri-state when not driving a valid command imadefined undefin



Table 63. Supported LPDDR3 DRAM Devices

apported LPDDR3 DRAM DevicesDRAM DensityData WidthBanksBank AddressRow AddressColumn AddressPage Size2Gbx328BA[2:0]A[13:0]A[8:0]2KB4Gbx328BA[2:0]A[13:0]A[9:0]4KB		und	Jefined uno			ndefined		
DensityWidthBanksAddressAddressAddressAddressPage Size2Gbx328BA[2:0]A[13:0]A[8:0]2KB4Gbx328BA[2:0]A[13:0]A[9:0]4KB	upported I	LPDDR3 DR	AM Devices	ł.	sined ut			ed u
4Gb x32 8 BA[2:0] A[13:0] A[9:0] 4KB			Banks				Page Size	ndefine
	2Gb	x32	8	BA[2:0]	A[13:0]	A[8:0]	2KB	D. *
	4Gb	x32	8	BA[2:0]	A[13:0]	A[9:0]	4KB	
SGD X3Z S BA[Z:U] A[I4:U] A[9:U] 4KD	8Gb	x32	8	BA[2:0]	A[14:0]	A[9:0]	4KB	

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Table 64. Supported DDR3L-RS DRAM Devices

Supported	DDR3L-RS	DRAM De	evices		ndein		
DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size	ned un
2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB	defin
Supported	DDR3L-RS	DRAM De	evices	ò		afined	une
DRAM	Data	Banks	Bank	Row	Column	Page Size	

Table 65. Supported DDR3L-RS DRAM Devices

DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size
2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB
Supported I		emory Si	ze Per Rani	k _{sin} n	ed und	
	DDAM			NG.	-	-

undefined undefit Table 66. Supported LPDDR3 Memory Size Per Rank

Supported L	PDDR3 Me	mory Size Pe	r Rank	sined	du
Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus	d undefine
512MB	2	2Gb	x32	4KB = 2KB * 2 chips	-
1GB	2	4Gb	x32	8KB = 4KB * 2 chips	
2GB	2	8Gb	x32	8KB = 4KB * 2 chips	

undefined undefined Table 67.

Supported DDR3L-RS Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
1GB	4	2Gb	x16	8KB = 2KB * 4 chips

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Register Map

For more information on System Memory Controller registers, refer Intel[®] Atom™ .J66 undefined undefined undefined Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066. undefined undefined undefined undefine

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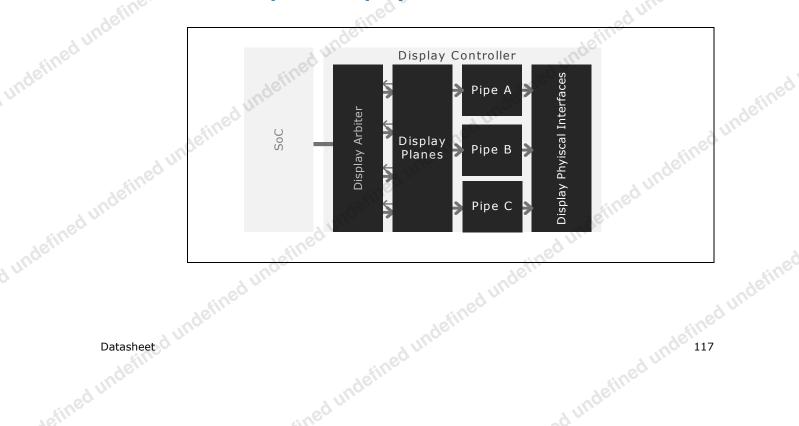
Graphics, Video and Display

This chapter provides an overview of Graphics, Video and Display features of the SoC.

Features

The key features of the individual blocks are as follows:

- Refreshed eight generation Intel graphics core with sixteen Execution Units (EUs)
 - 3D graphics hardware acceleration including support for DirectX*11.1, OpenGL 4.3, OGL ES 3.0, OpenCL 1.2.
 - Video decode hardware acceleration including support for H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG.
 - Video encode hardware acceleration including support for H.264, H.263, VP8, MVC, JPEG.
 - Display controller, incorporating the display planes, pipes and physical interfaces.
 - Four planes available per pipe 1x Primary, 2x Video Sprite & 1x Cursor.
 - Three multi-purpose Digital Display Interface (DDI) PHYs implementing HDMI, DVI, DisplayPort (DP) or Embedded DisplayPort (eDP) support.
 - Two dedicated digital Display Serial Interface PHYs implementing MIPI-DSI support.



SoC Graphics Display

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The Processor Graphics controller display pipe can be broken down into three components:

Display Planes

(intel) red und

- Display Pipes
- Display Physical Interfaces

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display hardware logic that defines the format and location of a rectangular region of memory that can be displayed on a display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

9.2.1 Primary Planes A, B and C

Planes A, B and C are the main display planes and are associated with Pipes A, B and C respectively. Each plane supports per-pixel alpha blending.

9.2.2

Video Sprite Planes A, B, C, D, E and F

Video Sprite Planes A, B, C, D, E and F are planes optimized for video decode.

- Pipe A Primary planeA, VSpriteA, VSpriteB, CusrorA
- Pipe B Primary planeB, VSpriteC, VSpriteD, CursorB
- Pipe C Primary planeC, VSpriteE, VSpriteF, CursorC

9.2.3 Cursors A, B and C

Cursors A, B and C are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A, B and C respectively.

9.3

Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed.

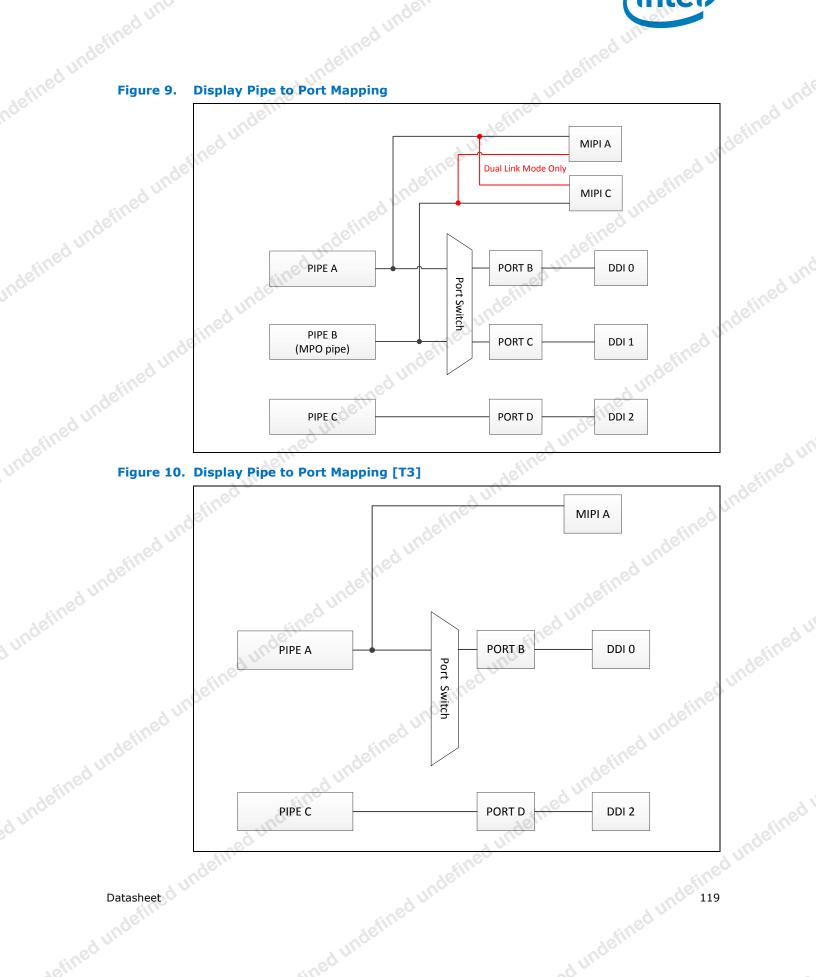
The display pipes A, B and C operate independently of each other at the rate of one pixel per clock. They can attach to any of the display interfaces.

Display Physical Interfaces

The display physical interfaces consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device. These interfaces are digital (MIPI-DSI, DisplayPort*, Embedded DisplayPort*, DVI and HDMI*) interfaces.

Datasheet



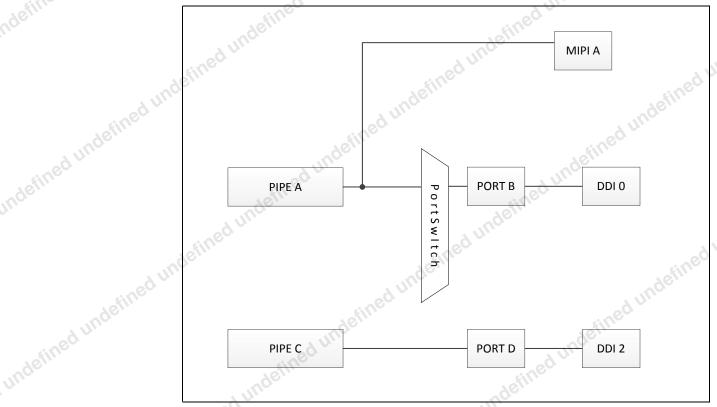




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Figure 11. Display Pipe to Port Mapping [T3]



Digital Display Interfaces 9.4.1

SoC Display Configuration (Sheet 1 of 2)

Table 68.	SoC Display Conf	iguration (Shee	et 1 of 2)		red undefine
ed un	Feature	MIPI DSI	eDP	DP	HDMI/DVI
ndefined under co.	Number of Ports	2 (x4 @ 1Gbps)	2 (x4 @2.7Gbps)	2 (x4 @2.7GHz)	2 (x4 @2.97GHz)
	Max Resolution	2560x1600 24bpp @60Hz	2560x1600 24bpp @60Hz	2560x1600 24bpp @60Hz	1920x1080 24bpp @120Hz/ 3840x2160 24bpp @ 30Hz
fined !	Standard	DSI1.01/ DPHY1.00	eDP1.3	DP1.1a	HDMI1.4b
Indefined undefined	Power gated during S0ix w/display off	Yes	Yes	Yes	Yes
definer	DRRS (Refresh reduction)	Yes (M/N pair)	Yes (Panel command)	N/A un	N/A
Jue	Self-Refresh with Frame buffer in Panel	Yes (Command Mode)	Yes (PSR)	Noeth	No
120 sined	unden		d undefine		Datashee
fined undefined		etine			Datashee

(intel) defined un

Graphics, Video and Display

ndefined undefined Table 68.

SoC Display Configuration (Sheet 2 of 2)

Table 68.		defined un.			hed une	
Table 68.	SoC Display Con	figuration (She	et 2 of 2)	unde.		
	Feature	MIPI DSI	eDP	CO DP	HDMI/DVI	- 20
	Content-Based backlight control	DPST6.0/CABC	DPST6/CABC	N/A	N/A	definee
	HDCP wired display	N/A	N/A(ASSR support)	1.4	1.4 sined	
efined undefined un	HDCP wireless display	N/A	N/A(ASSR support)	2.2	2.2	
nder	PAVP	AES-encrypted but	uffer, plane control	, panic attack 🔬	neu	
dui	SEC	All display registe	ers can be accesse	d by CEC	×.	
	LPE Audio	N/A	N/A	Yes	Yes	
	Compressed Audio	N/A	N/A	Yes	Yes	ed
	sined uns		d unde			undefine
Table 69.	SoC Display supp	orted Resolutio	onstine		ned	
d un		1 Display	10	isplays	3 Displays	

undefined undefined

	Compressed A			N/A	ies	fes
Table 69.	SoC Display	support	ed Resolutio	nstined	nde.	ined
ed un.		1	Display	102	2 Displays	3 Displays
undefined undefined und		1 Intern	al 1 Extern	al 1 Inter +1 Exte		1 Internal +2 External
	ed und	eDP* 2560x16 @ 60Hz	2	eDP * 2560x16 @ 60H	500 Iz	eDP* 2560x1600 @ 60Hz
sined un	Internal #1	or MIPI DS 2560x16 @60Hz	00	or MIPI D 2560x16 @60H	500	or MIPI DSI* 2560x1600 @60Hz
a undefined undefined un	External #1	N/A	HDMI/D 3840x21 @ 30Hz 2560x16 @ 60Hz	60 3840×22 z @ 30H 00 2560×16	160 Iz N/A	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz
	ineo.	N/A	N/A	underi N/A	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz
ed undefined undefined u	NOTES: 1. SoC is supp extended m 2. Experience	odes. 🔥			lays. External displa lution, and work loa	

NOTES:

- 1. SoC is supported maximum of 3 simultaneous displays. External display in both clone and A materined undefined undefined ! extended modes.
- , and 2. Experience may differ based on configuration, resolution, and work loads.

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9.4.1.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

stined undefined Table 71. **Display Physical Interfaces Signal Names (2 of 2)**

Inder	Signal names	Direction Type	Description	stined un
	MDSI_A_CLKP	0	MIPI Clock output for port A	nde.
	MDSI_A_CLKN	0	MIPI Clock complement output for port A	0.0.
	MDSI_A_DP[3:0]	I/O	MIPI Data Lane 3:0 for port A	
cin ^{e0}	MDSI_A_DN[3:0]	I/O	MIPI Data Lane 3:0 complement for port A	
defined undefine	MDSI_C_CLKP	0	MIPI Clock output for port C	
dull	MDSI_C_CLKN	0,0	MIPI Clock complement output for port C	
stines	MDSI_C_DP[3:0]	I/O	MIPI Data Lane 3:0 for port C	0.
inde	MDSI_C_DN[3:0]	I/O	MIPI Data Lane 3:0 complement for port C	ed ui
	MDSI_A_TE	I/O	Tearing Effect Signal from x4 port A display	lefine
	MDSI_C_TE	I	Tearing Effect Signal from x4 port C display	unac
	MDSI_DDC_DATA	I/O	DDC Data	9
- d ^N	MDSI_DDC_CLK	I/O	DDC Clock	
ed undefines	MDSI_RCOMP	I/O	MDSI_RCOMP: This is for pre-driver slew rate compensation for the MIPI DSI Interface. An external precision resistor of 150 Ω ±1% should be connected from this pin to ground.	

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9.4.1.2.1

Dual Link interface supports display resolution up to 2560 x 1600p @ 60 Hz with 24b per pixel. Interface supports maximum of 1Gbps per land rz with

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Full Frame Buffer Panel

The display controller supports full frame buffer display (also called command-mode display) with optimizations for both SoC power consumption and system power consumption. Full frame buffer panel does not need to be refreshed regularly by a frame buffer in system memory so the path between panel and system memory can be power-managed as much as possible until a new request occurs to update one or more planes that are active in the display pipe.

Sub-Display Support

The display controller supports a sub-display panel that uses a different virtual channel and shares the same interface with the main panel. The pixel data for this sub-display can come from a direct system memory read or it can come from the output at the pipe as described. Sub-display allows, for example, the pixel stream to be updated more frequently or presented in a format and/or resolution that would require software to convert or scale the panel resolution.

One example usage of sub-display is as a view finder for camera. The camera interface unit may output images in a format and resolution that are not read by the sub-display itself or must be blended with camera application graphics.

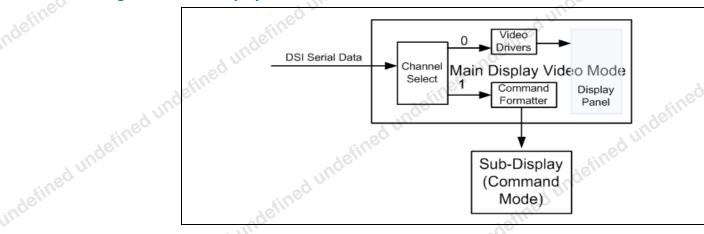


Figure 12. Sub-Display Connection

Partial Display Mode Support

The display controller supports a partial display mode that utilizes the MIPI command set to transition the panel from normal mode to partial display mode, so a small part of the display panel can be kept active for pixel data. The same panel can switch from full screen mode to a sub-display mode with a handful of scan lines to show time, date, signal strength indicator, etc., to save power for the host processor and display panel.

There are two scenarios:

 Type 1 display panel—both full display and partial display operates in command mode.

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Type 2 display panel—full display (normal mode) operate in video mode; partial display operates in command mode. This requires the host processor and display panel to be in sync in transition from normal mode to partial mode after 2 frames from the enter_partial_mode command.

The software driver must implement most of the protocols of transition and send the correct commands to the display panel to start the transition. The software driver must program the display controller to select the buffer for partial display (display pipe output or system memory) and follow the protocol to be in sync with the display panel.

When the display transitions from partial mode to normal mode, it is recommended to turn the display off to avoid tearing effect as in a flow chart in DCS specification.

MIPI DSI Dual-link Mode

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The SoC supports MIPI DSI dual-link mode, so that a single display can transmit a single stream of video data across two independent MIPI DSI interfaces. The packetization and timing of each link follows MIPI DSI 1.00 and DPHY 1.00 precisely, but the receiving device, which is a panel or a bridge, can combine the streaming data from two interfaces and display it in a single panel.

There are two types of dual-link panels that the SoC can support:

- Front-back type of panel, the first half of columns of pixels is always transmitted by port A and the second half of columns of pixels is always transmitted by port B.
- Pixel alternative type of panel, odd columns of pixels are always transmitted by port A and even columns of pixels are always transmitted by port B. So the 1st, 3rd, 5th, 7th, etc., pixels are separated at the source and sent in the first interface; the 2nd, 4th, 6th, 8th, etc., pixels are sent in the second interface.When the platform requires a dual-link interface for a large MIPI DSI panel or bridge (usually with resolution larger than 1920x1080 in which a 4-lane interface does not have enough bandwidth), the driver treats dual-link a special port configuration, with special handling of DSI controller but the operation of dual-link mode is consistent with single-link mode for planes and pipe operations. The system interface with upper level of SW does not need to change, like flip mechanism, interrupt, and so on.

LVDS Panel Support

An external MIPI DSI-to-LVDS bridge device is required to connect the display controller to a LVDS panel. A bridge device is used for larger panels.

High Definition Multimedia Interface

The High-Definition Multimedia Interface (HDMI) is provided for transmitting digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multichannel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the SoC and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable. immed undefined undefin

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HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) (not supported by the SoC). As shown in Figure 13, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the SoC are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

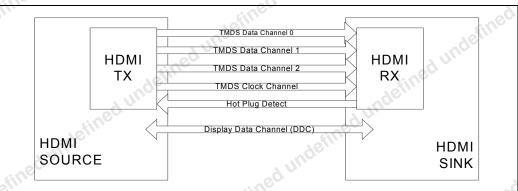
The SoC HDMI interface is designed as per the High-Definition Multimedia Interface Specification 1.4. The SoC supports High-Definition Multimedia Interface Compliance Test Specification 1.4.

Stereoscopic Support on HDMI 9.4.1.3.1

SoC display supports HDMI 1.4 3D video formats. If the HDMI panel is detected to support 3D video format then the SW driver will program Pipe2dB for the correct pipe timing parameters.

The left and right frames can be loaded from independent frame buffers in the main memory. Depending on the input S3D format, the display controller can be enabled do perform frame repositioning, image scaling, line interleaving.

Figure 13. HDMI Overview



Display Port

Display Port is a digital communication interface that utilizes differential signalling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. Display Port is also suitable for display connections between consumer electronics devices such as high definition optical disc red undefined in the stined undefined undefined undef players, set top boxes, and TV displays.

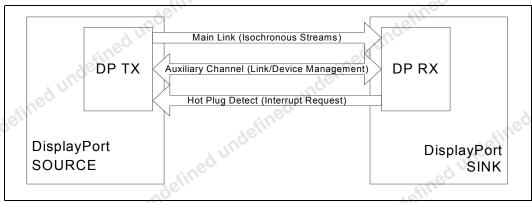




A Display Port consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a uni-directional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The SoC supports DisplayPort Standard Version 1.2.

Figure 14. DisplayPort* Overview



9.4.1.5 Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP) is a embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. eDP is supported only on Digital Display Interfaces 0 and/or 1. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

Each eDP port can be configured for up-to 4 lanes.

The SoC supports Embedded DisplayPort Standard Version 1.3.

9.4.1.5.1 DisplayPort Auxiliary Channel

A bidirectional AC coupled AUX channel interface replaces the I^2C for EDID read, link management and device control. I^2C -to-Aux bridges are required to connect legacy display devices.

9.4.1.5.2 Hot-Plug Detect (HPD)

SoC supports HPD for Hot-Plug sink events on the HDMI and DisplayPort interfaces.

9.4.1.5.3 Integrated Audio over HDMI and DisplayPort

SoC can support two audio streams on DP/HDMI ports. Each stream can be programmable to either DDI port. HDMI/DP audio streams can be sent with video streams as follows.

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LPE mode: In this mode the uncompressed or compressed audio sample buffers are generated either by OS the audio stack or by audio Lower Power Engine (LPE) and stored in system memory. The display controller fetches audio samples from these buffers, forms an SPDIF frame with VUCP and preamble (if needed), then sends out with video packets.

High-Bandwidth Digital Content Protection (HDCP) 9.4.1.5.4

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TV). The SoC supports HDCP 1.4(wired)/2.2(wireless) for content protection over wired displays (HDMI, DisplayPort and Embedded DisplayPort). Idefined undefined ur

9.5 References

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- High-Definition Multimedia Interface Specification, Version 1.4b
- High-bandwidth Digital Content Protection System, Revision 1.4
- VESA DisplayPort Standard, Version 1.2
- VESA Embedded DisplayPort Standard, Version 1.3

9.6 **3D Graphics and Video**

The SoC implements a derivative of the Generation 8 LP graphics engine which consists of rendering engine and bit stream encoder/decoder engine. The rendering engine is used for 3D rendering, media compositing and video encoding. The Graphics engine is built around sixteen execution units (EUs).

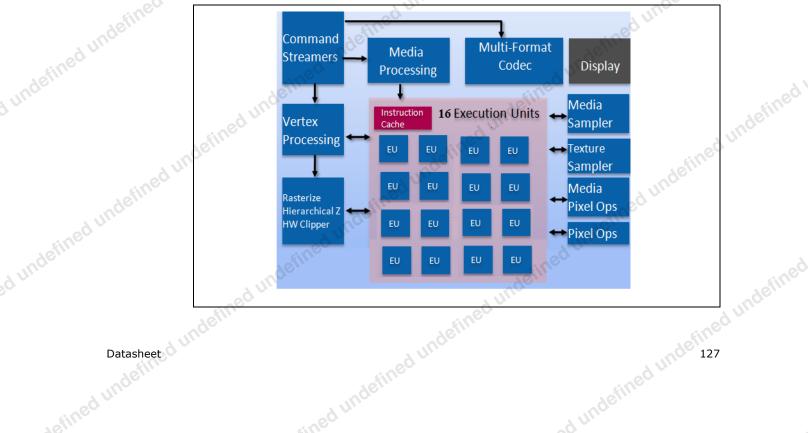


Figure 15. 3D Graphics Block Diagram



9.7 Features

The 3D graphics pipeline architecture simultaneously operates on different primitives or undefine on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 8.0 LP 3D engine provides the following performance and power-management enhancements:

- Hierarchal-Z
- Video quality enhancements

9.7.1

3D Engine Execution Units

- The EUs perform 128-bit wide execution per clock
- defined undefined Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing

9.7.2 **3D Pipeline**

9.7.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

9.7.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

Clip Stage 9.7.2.4

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

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9.7.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

Video Engine

The video engine is part of the Intel Processor Graphics for image processing, playback and transcode of Video applications. Processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content. This engine supports Full HW acceleration for decode of AVC/H.264, VC-1 and MPEG -2 contents along with encode of MPEG-2 and AVC/H.264 apart from various video processing features. The new Processor Graphics Video engine adds support for processing features such as frame rate conversion, image stabilization and gamut conversion.

9.8

VED (Video Encode/Decode)

The video engine is part of the Intel Processor Graphics for image processing, playback and transcode of Video applications. Processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content.

9.8.1 Features

The features for the Video decode hardware accelerator in SoC are:

- VED core can be configured on a time division multiplex basis to handle single, dual and multi-stream HD decoding/encoding.
- VED provides full hardware acceleration Decode/Encode support below Media formats.

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Table 72.

MVC

					0	
	Encode Format	Profile	Level	Resolution	Bitrate (Mbps)	Frame Rate
	H.263			6 ⁰ 480p		30
nd	H.264	HP/BP/CBP	L5.1	4kx2k	100-130	30
			, unc	1080p		120
	VP8		~e0	4kx2k		30

L4.2

Hardware Accelerated Video Decode/Encode Codec Support

HP/BP/CBP

	-						
defined u	JPEG	-d un	1067Mpps (42	20), 800Mpps (4	22) @400Mhz		
Indefin	inde	stine		defin	ed		odefined un
	Decode Format	Profile	Level	Resolution	Bitrate (Mbps)	Frame Rate	under
, un	H.263		der	480p		30	
odefined undefined un	MPEG4	SP	-d un	480p		30	
detti	H.264	HP,MP,CBP	L5.2	4Kx2K	200-250	60	
d une		nde		1080P	16/11	240	
	H.265(HEVC)	MP	L5	4Kx2K	unos	30	
dell	VP8	etine		4kx2k	100	30	adefined un
UI.	VP9			1080p	Þ	30	sines
	MVC			4Kx2K		30	nde
	MPEG2	MP	HL	1080p		60	d ^U
	VC1	AP	L4	1080P		60	<i>v</i>
	JPEG		1067Mpps (42	20), 800Mpps (4	22) @400Mhz	unos	

1080p

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Register Map

For more information on Graphics, Video and Display registers refer Intel[®] Atom™ Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID: 332066. ed undefined undefined undefined

PCI Express 2.0



Idefined undefined PCI Express 2.0 10

undefined und There are up to two PCI Express root ports, each supporting the PCI Express* Base Specification, Rev. 2.0 at a maximum 5 GT/s signaling rate. The root ports can be configured to support a diverse set of lane assignments.

10.1

Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

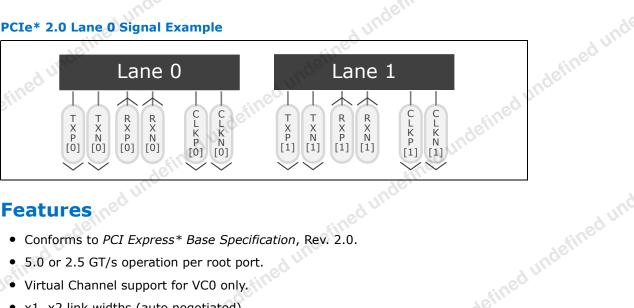
- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 73. Signals

und Table 73.	Signals	defined	Chapter 19, "Electrical Specifications". n of the signal's function.	т
leftined.	Signal Name	Direction /Type	Description	
100	PCIE_TXP[1:0] PCIE_TXN[1:0]	O PCIe	PCI Express* Transmit PCI Express* Ports 1:0 transmit pair (P and N) signals. Each pair makes up the transmit half of a lane.	ndefin
od und	PCIE_RXP[1:0] PCIE_RXN[1:0]	I PCIe	PCI Express* Receive: PCI Express* Ports 1:0 receive pair (P and N) signals. Each pair makes up the receive half of lane.	
Indefined undefined und	PCIE_CLKREQ[1:0]_N	IO	PCI Express* Clock Request Used for devices that need to request one of the output clocks. Each clock request maps to the matching PCIe Root Port (e.g. PCIE_CLKREQ#[0] maps to PCIE Root Port [0] and so on) NOTE: These signals are muxed and may be used by other functions.	112
	P_RCOMP_P P_RCOMP_N	I/O	These pins connected with 402 Ohm 1% between RCOMP pads.	under.
undefined undefined un	Idefined undefined i	Indefined	These pins connected with 402 Ohm 1% between RCOMP pads.	undef
Datasheet	den		undefiner undefin	
Datasheet	6	undefine	indefineo	



Figure 16. PCIe* 2.0 Lane 0 Signal Example



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Features

- Conforms to PCI Express* Base Specification, Rev. 2.0.
- 5.0 or 2.5 GT/s operation per root port.
- Virtual Channel support for VC0 only.
- x1, x2 link widths (auto negotiated).
- Spread Spectrum Clocking (SSC) is supported for PCIe Gen1 components.
- Flexible Root Port configuration options
 - (1) x2's
 - (2) x1
- Interrupts and Events
 - Legacy (INTx) and MSI Interrupts
 - General Purpose Events
 - Express Card Hot Plug Events
 - System Error Events
- Power Management
 - Link State support for ASPM(L0s, L1), L1 sub states (L1.SNOOZ,L1.OFF), L23_RDY,L2 and L3.
 - Powered down in ACPI S3 state L3.

Note:

Intel recommends disabling Spread Spectrum Clocking (SSC), if PCIe Gen2 based component is used.

10.2.1 **Root Port Configurations**

Depending on SKU, there are up to two possible lane assignments for root ports 1-2.

Root port configurations are set by SoftStraps stored in SPI flash, and the default option is " $(2) \times 1''$. Links for each root port will train automatically to the maximum in a undefined undefined possible for each port.

PCI Express 2.0



x2 link widths are not common. Most devices will only train to x1 Note:

Note:

PCI functions in PCI configuration space are disabled for root ports not available.

Interrupts and Events 10.2.2

A root port is capable of handling interrupts and events from an end point device. A root port can also generate its own interrupts for some events, including power management and hot plug events, but also including error events.

There are two interrupt types a root port will receive from an end point device: INTx (legacy), and MSI. MSI's are automatically passed upstream by the root port, just as other memory writes would be. INTx messages are delivered to the Legacy block's interrupt router/controller by the root port.

Hefined undefined Events and interrupts that are handled by the root port are shown with the possible interrupts they can deliver to the interrupt decoder/router.

Packet/Event	Туре	INTx	MSI	SERR	SCI	SMI	GPE	1
INTx	Packet	x	X	·'	223	eo	l	
PM_PME	Packet	X	X	· · · · · · · · · · · · · · · · · · ·	nder.	łł		
Power Management (PM)	Event	Х	Х	ed.	х	Х	i	
Hot Plug (HP)	Event	Х	X	SUL	Х	Х	i	odefined
ERR_CORR	Packet	(,	, uno	Х			i	den
ERR_NONFATAL	Packet	0	<u> 0</u>	Х				Un
ERR_FATAL	Packet	-9er		Х			Sine	
Internal Error	Event			Х		21	be.	
VDM	Packet	[<u>_</u>	Х	

Table 74. **Possible Interrupts Generated From Events/Packets**

NOTE: Above table lists the possible interrupts and events generated based on Packets received, or events generated in the root port. Configuration needed by software to enable the different interrupts as applicable.

ed undefined undefined When INTx interrupts are received by an end point, they are mapped to the following interrupts and sent to the interrupt decoder/router in the iLB.

Interrupt Generated for INT[A-D] Interrupts Table 75.

	INTA	INTB	INTC	INTD
Root Port 1	INTA#	INTB#	INTC#	INTD#
Root Port 2	INTD#	INTA#	INTB#	INTC#

NOTE: Interrupts generated from events within the root port are not swizzled. in a undefined undefined undef



PCI Express 2.0

10.2.2.1 **Express Card Hot Plug Events**

Express Card Hot Plug is available based on Presence Detection for each root port.

Note:

A full Hot Plug Controller is not implemented.

Presence detection occurs when a PCI Express* device is plugged in and power is supplied. The physical layer will detect the presence of the device, and the root port will set the SLSTS.PDS and SLSTS.PDC bits.

When a device is removed and detected by the physical layer, the root port will clear the SLSTS.PDS bit, and set the SLSTS.PDC bit.

Interrupts can be generated by the root port when a hot plug event occurs. A hot plug event is defined as the transition of the SLSTS.PDC bit from 0 to 1. Software can set the SLCTL.PDE and SLTCTL.HPE bits to allow hot plug events to generate an interrupt.

If SLCTL.PDE and SLTCTL.HPE are both set, and STSTS.PDC transitions from 0 to 1, an interrupt will be generated.

10.2.2.2 System Error (SERR)

System Error events are support by both internal and external sources. Refer the PCI Express* Base Specification, Rev. 2.0 for details.

10.2.3 **Power Management**

Each root port's link supports LOs, L1, and L2/3 link states per PCI Express* Base Specification, Rev. 2.0. L2/3 is entered on entry to S3.

10.3

References

PCI Express* Base Specification, Rev. 2.0

10.4 **Register Map**

indefined undefined undefined undefined undefined undefined For more information on PCI Express* 2.0 registers refer Intel[®] Atom™ Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID: 332066.



11

MIPI-Camera Serial Interface (CSI) and ISP

MIPI CSI and controller front end interfaces with three sensors and is capable of simultaneously acquiring three streams, one from each sensor. These three streams are presented to the ISP.

11.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Indefined undef **CSI Signals** Table 76.

CSI Signals	underpland	ation of the signal's function.	
Signal Name	Direction	Description	6
MCSI1_CLKP/N	I	Clock Lane: MIPI CSI input clock lane 0 for port 1.	afine
MCSI1_DP/N[3:0]	I	Data Lanes: Four MIPI CSI Data Lanes (0-3) for port 1. Lanes 2 and 3 can optionally used as data lanes for port 3.	unoc
MCSI2_CLKP/N	Ι	Clock Lane: MIPI CSI input clock lane 0 for port 2.	
MCSI2_DP/N[1:0]	I	Data Lane: Two MIPI CSI Data Lanes for port 2.	
MCSI3_CLKP/N	I	Clock Lane: MIPI CSI input clock lane 0 for port 3.	
MCSI_RCOMP	I/O	Resistor Compensation: This is for pre-driver slew rate compensation for the MIPI CSI Interface.	

Indefined undefined und Table 77. GPIO Signals (Sheet 1 of 2)

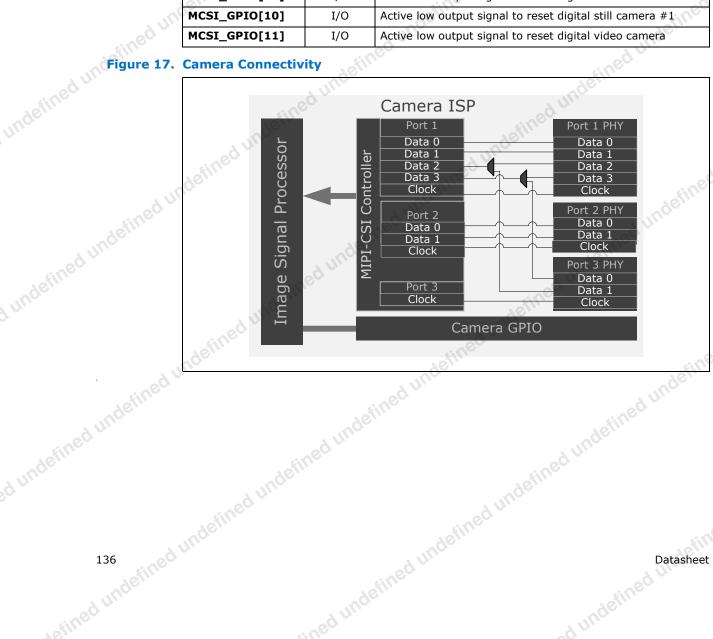
since		0	compensation for the MIFI CSI Interface.	
Junden Table 77.	GPIO Signals (Sh	eet 1 of 2)		red u
	Signal Name	Direction /Type	2d Und Description	undefille
roed un	MCSI_GPIO[00]	I/O	Output from shutter switch when its pressed halfway. This switch state is used to trigger the Auto focus LED for Xenon Flash or Torch mode for LED Flash	
undefil.	MCSI_GPIO[01]	I/O	Output from shutter switch when its pressed full way. This switch state is used to trigger Xenon flash or LED Flash	
affined t	MCSI_GPIO[02]	J/O	Active high control signal to Xenon Flash to start charging the Capacitor	
d unde	MCSI_GPIO[03]	I/O	Active low output from Xenon Flash to indicate that the capacitor is fully charged and is ready to be triggered	afined
Datasheet	ndefined		dundefined un	ad under
undefined undefin.		ned undef	ne. dundefined h.	



defined undefine GPIO Signals (Sheet 2 of 2) Table 77.

d undefine		adefine	d under under	
Idefine ⁰ Table 77.	GPIO Signals (Sh Signal Name	Direction /Type	Description	ined und
	MCSI_GPIO[04]	I/O	Active high Xenon Flash trigger / Enables Torch Mode on LED Flash IC	Indern
d un	MCSI_GPIO[05]	I/O	Enables Red Eye Reduction LED for Xenon / Triggers STROBE on LED Flash IC /	
Indefined	MCSI_GPIO[06]	I/O	Camera Sensor 0 Strobe Output to SoC to indicate beginning of capture / Active high signal to still camera to power down the device.	
ndefined L.	MCSI_GPIO[07]	J/O	Camera Sensor 1 Strobe Output to SoC to indicate beginning of capture / Active high signal to still camera to power down the device.	d ur
	MCSI_GPIO[08]	I/O	Active high signal to video camera to power down the device.	definec
	MCSI_GPIO[09]	I/O	Active low output signal to reset digital still camera #0.	UNC
	MCSI_GPIO[10]	I/O	Active low output signal to reset digital still camera #1	
-00	MCSI_GPIO[11]	I/O	Active low output signal to reset digital video camera	

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ndefined undefined undefine MIPI-Camera Serial Interface (CSI) and ISP



11.2 **Features**

- Integrated MIPI-CSI 2.0 interface.
- Image Signal Processor (ISP) with DMA and local SRAM.
- Imaging data is received by the MIPI-CSI interface and is relayed to the ISP for processing.
- Up to six MIPI-CSI 2.0 data lanes.
 - Each lane can operate at up to 1.5Gbp/s. resulting in roughly 1.2 Gbp/s of actual pixels.
- The MIPI-CSI interface supports lossless compressed image streams to increases the effective bandwidth without losing data.
- Up to 13MP sensors supported, and full HD 1080p30 Can also support Stereo HD 1080p30.

Imaging Capabilities 11.2.1

undefined undefined undefined **Imaging Capabilities**

undefined uns 11.2.1	 The MIPI-CSI interface supports lossless compressed image streams to increases the effective bandwidth without losing data. Up to 13MP sensors supported, and full HD 1080p30. Can also support Stereo HD 1080p30. 				
and und		summarizes imaging capabilities.	~		
Table 78.	Imaging Capabili Feature	Capabilities]		
undefined L.	Sensor interface	Configurable MIPI-CSI2 interfaces. 3 sensors: x2, x2, x2 or x1 x2, x3 2 sensors: x4, x2	uned un		
ь — — — — — — — — — — — — — — — — — — —	Simultaneous sensors	Up to 3 simultaneous sensors	Indefin		
	2D Image capture	13MP ZSL @ 18fps	·		
dul	2D video capture	Up to 1080p30			
stines	Input formats	RAW 8, 10, 12, 14, RGB444, 565, 888, YUV420, 422, JPEG.			
inde.	Output formats)	YUV422, YUV420, RAW]		
d undefined L	Special Features	Image and video stabilization Low light noise reduction Burst mode capture Memory to memory processing 3A (Auto Exposure (AE), Auto White Balance (AWB) and Auto Focus (AF)) High Dynamic Range (HDR)	undefined u		
ad u	nde.	Multi-focus Zero shutter lag			

11.2.2 Simultaneous Acquisition

SoC will support on-the-fly processing for only one image at a time. While this image is being processed on-the-fly, images from the other two cameras are saved to DRAM for ined undefined in a undefined undefined undefined later processing.

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11.2.3 **Primary Camera Still Image Resolution**

Maximum still image resolution for the primary camera in post-processing mode is limited by the resolution of the sensors. Currently 13Mpixel sensors are supported.

Higher resolution, or higher frame rates are supported as long as the product of resolution and frame rate does not exceed 235 Mpixels/s (= 13 Mpixels * 18 fps).

Maximum primary camera on-the-fly stereoscopic still image resolution for primary camera is 8 Mpixel for each of the left and right images at 18 fps. The number of Mpixels can be increased by decreasing the frame rate.

11.2.4 **Burst Mode Support**

The SoC supports capturing multiple images back to back at maximum sensor resolution. At least 5 images must be captured in burst mode. The maximum number of images that can be so captured is limited only by available system memory. These images need not be processed on-the-fly.

11.2.5 **Continuous Mode Capture**

SoC supports capturing images and saving them to DRAM in a ring of frame buffers continuously at maximum sensor resolution. This adds a round trip to memory for every frame and increases the bandwidth requirements.

11.2.6 Secondary Camera Still Image Resolution

Maximum secondary camera still image resolution is 4 Mpixel at 15 fps.

11.2.7 **Primary Camera Video Resolution**

Maximum primary camera video resolution is 1080p60. Maximum primary camera dual video resolution is 1080p30

11.2.8 **Secondary Camera Video Resolution**

Maximum secondary camera video resolution is 1080p30.

11.2.9

Bit Depth

Capable of processing 14-bit images at the stated performance levels.

Capable of processing 18-bit images at half the performance levels, i.e. process onthe-fly 13 Mpixel 18-bit images at 7 fps instead of 15 fps.

Capable of processing up to 18-bit precision.

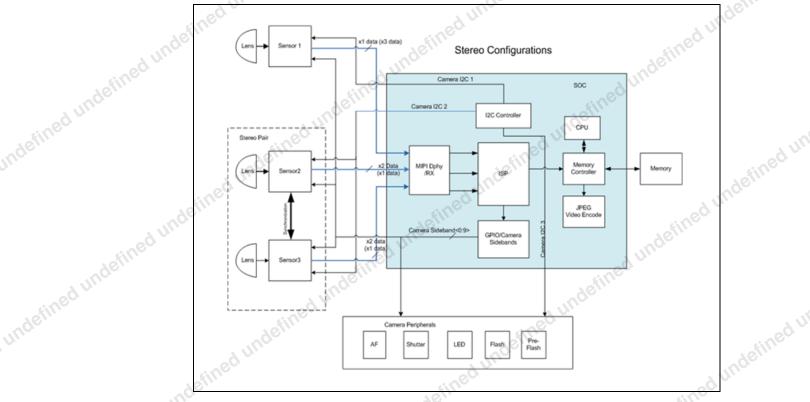
The higher precision processing will be employed mainly for high dynamic range imaging (HDR). -gi efined undefined unde



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Imaging Subsystem Integration 11.3

Figure 18. Image Processing Components



11.3.1 **CPU Core**

The CPU core augments the signal processing capabilities of the hardware to perform post-processing on images such as auto focus, auto white balance, and auto exposure. The CPU also runs the drivers that control the GPIOs and I²C for sensor control.

11.3.2 **Imaging Signal Processor (ISP)**

The ISP (Imaging Signal Processor) includes a 64-way vector processor enabling high quality camera functionality. Key features include support of three camera sensors.

MIPI-CSI-2 Ports 11.3.2.1

The SoC has three MIPI clock lanes and six MIPI data lanes. The Analog Front End (AFE) and Digital Physical Layer (DPHY) take these lanes and connects them to three virtual ports. Two data lanes are dedicated to each of the rear facing cameras and the A undefined undefined undefined remaining data lane is connected to the front facing camera. The MIPI interfaces follow the MIPI-CSI-2 specifications as defined by the MIPI Alliance. They support YUV420, YUV422, RGB444, RGB555, RGB565, and RAW 8b/10b/12b. Both MIPI ports support

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compression settings specified in MIPI-CSI-2 draft specification 1.01.00 Annex E. The compression is implemented in Hardware with support for Predictor 1 and Predictor 2. ined undefined Supported compression schemes:

- 12-8-12
- 12-7-12
- 12-6-12
- 10-8-10
- 10-7-10
- 10-6-10

The data compression schemes above use an X-Y-Z naming convention where X is the number of bits per pixel in the original image, Y is the encoded (compressed) bits per pixel and Z is the decoded (uncompressed) bits per pixel.

11.3.2.2 I²C for Camera Interface

The platform supports three (3) I^2C ports for the camera interface. These ports are used to control the camera sensors and the camera peripherals such as flash LED and lens motor.

11.3.2.3 **Camera Sideband for Camera Interface**

Twelve (12) GPIO signals are allocated for camera functions, refer Table 77 for signal names. These GPIOs are multiplexed and are available for other usages without powering on the ISP. The ISP provides a timing control block through which the GPIOs can be controlled to support assertion, de-assertion, pulse widths and delay. The configuration below of camera GPIOs is just an example of how the GPIOs can be used. Several of these functions could be implemented using I^2C , depending on the sensor implementation for the platform.

Sensor Reset signals

Force hardware reset on one or more of the sensors.

- Sensor Single Shot Trigger signal
 - -Indicate that the target sensor needs to send a full frame in a single shot mode, or to capture the full frame for flash synchronization.
- PreLight Trigger signal
 - -Light up a pilot lamp prior to firing the flash for preventing red-eye.
- Flash Trigger signal
 - -Indicate that a full frame is about to be captured. The Flash fires when it detects an assertion of the signal.
- Sensor Strobe Trigger signal
 - -Asserted by the target sensor to indicate the start of a full frame, when it is configured in the single shot mode, or to indicate a flash exposed frame for flash synchronization.



11.4 Functional Description

At a high level, the Camera Subsystem supports the following modes:

- Preview
- Image capture
- Video capture

Preview

11.4.1

Once the ISP and the camera subsystem is enabled, the ISP goes into the preview mode where very low resolution frames, such as VGA/480p (programmable), are being processed.

11.4.2 Image Capture

During the image capture mode, the camera subsystem can acquire at a peak throughput of 13 Mpixels @ 18fps. While doing this, it continues to output preview frames simultaneously.

- The ISP can output RAW, RGB or YUV formats. The ISP can capture one full frame at a time or perform burst mode capture, where up to five full back-to-back frames are recorded.
- The ISP will not limit the number of back-to-back full frames captured, but the number is programmable and determined on how much memory can be allocated dynamically.
- The ISP can process all the frames on the fly and writes to memory only after fully
 processing the frames, without requiring download of any part of the frame for
 further processing.
 - The exceptions to this approach are image stabilization and some other advanced functions requiring temporal information over multiple frames.

The ISP can support image stabilization in image capture model.

- The ISP initially outputs preview frames.
- When the user decides to capture the picture, image stabilization is enabled. The ISP checks the previous frame for motion and compensates for it appropriately.

Auto Exposure (AE), Auto Focus (AF), and Auto White Balance (AWB), together known as 3A, are implemented in the CPU to provide flexibility.

11.4.3 Video Capture

During video recording, the ISP can capture video up to 1080p @ 60 fps and output preview frames concurrently. The ISP output video frames to memory in YUV420 or YUV422 format.

11.4.4 ISP

The Camera subsystem consists of 2 parts, the hardware subsystem and a software stack that implements the ISP functionality on top of this hardware.

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The core of the ISP is a vector processor. The vector processor is supported by the following components:

- Interfaces for data and control
- A small input formatter that parallelizes the data
- A scalar (RISC) processor, for system control and low-rate processing
- An accelerator for scaling, digital zoom, and lens distortion correction
- A DMA engine transfers large amounts of data such as input and output image data or large parameter sets between LPDDR2 and the ISP block.

11.4.5 Memory Management Unit (MMU)

The camera subsystem has capabilities to deal with a virtual address space, since a contiguous memory range in the order of 16–32MB cannot be guaranteed by the OS.

11.4.5.1 Interface

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The MMU performs the lookup required for address translation from a 32-bit virtual address to 36-bit physical address. The lookup tables are stored external to the system. The MMU performs the lookup through a master interface without burst support that is connected to the Open Core Protocol (OCP) master of the subsystem. The MMU configuration registers can be accessed through a 32-bit Core I/O (CIO) slave interface. Additionally there is a 32-bit CIO slave interface connected to the address translator.

11.5

MIPI-CSI-2 Receiver

MIPI-CSI-2 devices are camera serial interface devices. They are categorized into two types, a CSI transmitter device with Camera Control Interface (CCI) slave and CSI receiver device with CCI master.

Data transfer by means of MIPI-CSI is unidirectional that is, from transmitter to receiver. CCI data transfer is bidirectional between the CCI slave and master.

Camera Serial Interface Bus (CSI) is a type of serial bus that enables transfer of data between a Transmitter device and a receiver device. The CSI device has a point-topoint connections with another CSI device by means of D-PHYs and as shown in Figure 19.

Similarly, CCI (Camera Control Interface bus) is a type of serial bus that enables transfer back and forth between the master CCI and a Slave CCI Unit. undefined undefined undefined undefined undefined i



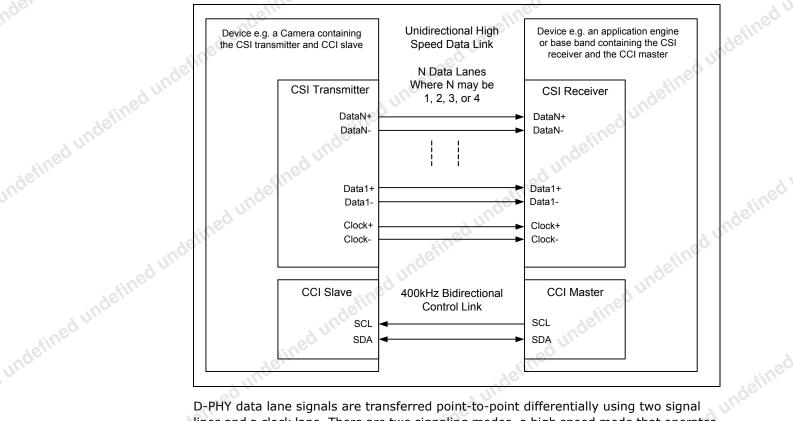


Figure 19. MIPI-CSI Bus Block Diagram

D-PHY data lane signals are transferred point-to-point differentially using two signal lines and a clock lane. There are two signaling modes, a high speed mode that operates up-to 1500Mbs and a low power mode that works at 10Mbs. The mode is set to low power mode and a stop state at start up/power up. Depending on the desired data transfer type, the lanes switch between high and low power modes.

The CCI interface consists of an I²C bus which has a clock line and a bidirectional data line.

The MIPI-CSI-2 devices operate in a layered fashion. There are 5 layers identified at the receiver and transmitter ends.

MIPI-CSI-2 Functional Layers:

• PHY Layer

- An embedded electrical layer sends and detects start of packet signalling and end of packet signalling on the data lanes. It contains a serializer and deserializer unit to interface with the PPI / lane management unit. There is also a clock divider unit to source and receive the clock during different modes of operation.

PPI/Lane Management Unit

 This layer does the lane buffering and distributes the data in the lanes as programmed in a round robin manner and also merges them for the PLI/Low Level Protocol unit. in a undefined undefin

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PLI/Low Level Protocol Unit

 This layer packetizes as well as de-packetizes the data with respect to channels, frames, colors and line formats. There is also a CRC checker or CRC generator unit to pack the payload data with CRC checksum bits for payload data protection.

Pixel/Byte to Byte/Pixel Packing Formats

 Conversion of pixel formats to data bytes in the payload data is done depending on the type of image data supported by the application. It also re-converts the raw data bytes to pixel format understandable to the application layer.

• Application

 Depending on the type of formats, camera types, capability of the camera used by the transmitter, the application layer recovers the image formats and reproduces the image in the display unit. It also works on de-framing the data into pixel-to-packing formats. High level encoding and decoding of image data is handled in the application unit.

11.5.1 MIPI-CSI-2 Receiver Features

CSI Features:

- Compliant to CSI-2 MIPI specification for Camera Serial Interface (Version 1.00).
- Supports standard D-PHY receiver compliant to the MIPI Specification.
- Supports PHY data programmability up to four lanes.
- Supports PHY data time-out programming.
- Has controls to start and re-start the CSI-2 data transmission for synchronization failures and to support recovery.
- The ISP may not support all the data formats that the CSI-2 receiver can handle.
- Refer Table 78 for formats supported by the ISP
- Supports all generic short packet data types
- Single Image Signal Processor interface for pixel transfers to support multiple image streams for all virtual channel numbers

D-PHY Features:

- Supports synchronous transfer in high speed mode with a bit rate of 80-1500Mb/s.
- Supports asynchronous transfer in low power mode with a bit rate of 10Mb/s.
- Differential signalling for HS data.
- Spaced one-hot encoding for Low Power [LP] data.
- Data lanes support transfer of data in high speed as well as low power modes.
- Supports ultra low power mode, escape mode, and high speed mode.
- Hasa clock divider unit to generate clock for parallel data reception and transmission from and to the PPI unit.
- Activates and disconnects high speed terminators for reception and control mode.
- Activates and disconnects low power terminators for reception and transmission.

11.6 Register Map

For more information on MIPI- Camera Serial Interface (CSI) and ISP registers refer Intel[®] Atom[™] Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.

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SoC Storage Overview 12.1

12.1.1 Storage Control Cluster (eMMC, SDIO, SD)

The SCC consists of SDIO, SD and eMMC controllers to support mass storage and IO devices.

- One eMMC 4.51 interface
- One SD 3.0 interface
- One SDIO 3.0 interface

Signal Descriptions 12.2 undefined undefined

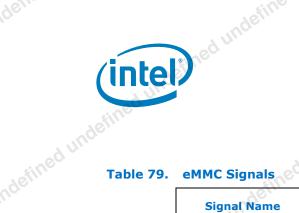
Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

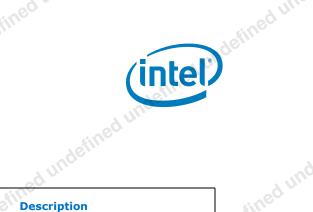
- Signal Name: The name of the signal/pin.
- A underfined underfined underfined underfined underfined underfined underfined underfined underfined underfined

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afine	ed	un.	
d unde	ndefine	stineu	
Table 79. eMMC Signals	UT-	AUNDE	
Signal Name	Direction /Type	Description	defined
MMC1_CLK	I/O/GPIO	eMMC Clock The frequency may vary between 25 and 200MHz.	un
MMC1_D[7:0]	I/O/GPIO	eMMC Port Data bits 0 to 7 Bidirectional port used to transfer data to and from eMMC device.	
d unor	d undern.	By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines D[1]-D[7].	d undefined
undefined W MMC1_CMD	I/O/GPIO	eMMC Port Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.	
MMC1_RCOMP	I/O/GPIO	eMMC RCOMP	
MMC1_RST_N	I/O/GPIO	This signal is used for pre-driver slew rate compensation. eMMC Reset Signals Active low to recet	Aine
MMC1 RCLK	I/GPIO	Active low to reset. eMMC Return Clock Signals	inder
ned undefined undefined undefin	ned undefil	defined undefined undefined undefined un.	ied undefine
MMC1_RCLK	ined undef	eMMC Reset Signals Active low to reset. eMMC Return Clock Signals	ned undefin
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ger.	dundefine		indefined	defined un-
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ed undefine	, U	ndefined	odefined un	
Table 80.	SDIO Signals		ed un	- und
.00	Signal Name	Direction /Type	Description	defineo
000	SD2_CLK	I/O/GPIO	SDIO Clock The frequency may vary between 25 and 200MHz.	unu
sined undefined une	SD2_D[2:0]	I/O/GPIO	 SDIO Port Data bits 0 to 2 Bidirectional port used to transfer data to and from SDIO device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3]. 	
Inder.	SD2_D[3]_CD_N	I/O/GPIO	SDIO Port Data bit 3 Bidirectional port used to transfer data to and from the SDIO device. Also, Card Detect. Active low when device is present.	undefined un
undefined un	SD2_CMD	I/O/GPIO	SDIO Port Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.	
Jefined Table 81.	SD Signals (Sheet	1 of 2)	ed unde	
UN	Signal Name	Direction	Description	sineo

undefined undefined und Table 81. SD Signals (Sheet 1 of 2)

		96.	initialization, and push-pull for fast command transier.	
defined Table 81.	SD Signals (Sheet	: 1 of 2)	red under	dun
UII	Signal Name	Direction /Type	Description	odefinec
71.	SD3_CLK	I/O/GPIO	SD Card Clock The frequency may vary between 25 and 200 MHz.	
undefined undefined un	SD3_D[3:0]	I/O/GPIO	SD Card Data bits 0 to 3 Bidirectional port used to transfer data to and from SD/ MMC card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].	
J unde.	SD3_CD_N	I/O/GPIO	SD Card Detect Active low when a card is present. Floating (pulled high with internal PU) when a card is not present.	defined u
inedu	SD3_CMD	I/O/GPIO	SD Card Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.	3d un
d undefined undefined un	SD3_1P8EN	I/O/GPIO	SD Card 1.8V Enable Controls the voltage of the SD Card, the default is low (3.3V). The voltage is 1.8V when this signal is high.	
ed under.	ndefined undefin		terined underined	red undefined
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Jefined undefine		ned undefi	d undefined	



Table 81. SD Signals (Sheet 2 of 2)

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SD Signals (Shee	t 2 of 2) Direction	- ed undefiner	und
Signal Name	/Туре	Description	sineo
SD3_RCOMP	I/O/GPIO	SD Card RCOMP This signal is used for pre-driver slew rate compensation.	undell
SD3_PWREN_N	I/O/GPIO	SD Card Power Enable This signal is used to enable power on a SD device.	>
SD3_WP	I/O/GPIO	SD Card Write Protect Active high to protect from write.	

stined undefined une **Features**

12.3.1 Memory Capacity

- Standard Capacity SD Memory Card (SDSC): Up to and including 2 GB.
- High Capacity SD Memory Card (SDHC): More than 2GB and up to and including 32GB.
- Extended Capacity SD Memory Card (SDXC): More than 32GB and up to and including 2TB.

12.3.2 **SDIO/SD Interface Features**

- Host clock rate variable between 0 and 200 MHz.
- Up to 800 Mbits per second data rate using 4 parallel data lines (SDR104 mode).
- Transfers the data in 1 bit and 4 bit SD modes.
- Transfers the data in following UHS-I modes (SDR12/25/50/104 and DDR50).
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Designed to work with I/O cards, Read-only cards and Read/Write cards.
- Supports Read wait Control, Suspend/Resume operation.

12.3.3 eMMC Interface Features

- Supports eMMC v4.51.
- Host clock rate variable between 0 and 200 MHz.
- Supports HS400 mode.
- Up to 1600 Mbits per second data rate using 8 bit parallel data lines (High Speed DDR mode).
- Up to 3200 Mbits per second data rate using 8 bit parallel data lines (HS400 mode).
- Transfers the data in 1 bit, 4 bit and 8 bit modes.
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Supports MMC Plus and MMC mobile. inen undefined undefine



12.3.4 Storage Interfaces

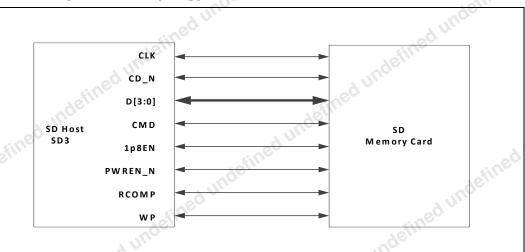
This section provides a very high level overview of the SD, SDIO, eMMC 4.51 specification.

SD 3.0 Bus Interface 12.3.4.1

The SD Card bus has a single master, single slaves (card), synchronous topology (refer Figure 20). During initialization process commands are sent to the card, allowing the application to detect the card and assign logical addresses to the physical slot. All data communication in the Card Identification Mode uses the command line (CMD) only.

SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Card will use only SD3_D[0] for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between hardware cost and system performance. Note that while DAT1-SD3 D[3:1] are not in use, the SoC will tri-state those signals.





12.3.4.2 SDIO 3.0 Interface

Je undefined undefined undefined undefined undefined undefined The SDIO interface is the very much like the SD card interface. The SoC supports one Datasheet dumaalimed undermed undermed undermed undermed undermed undermed undermed under the second s SDIO device.

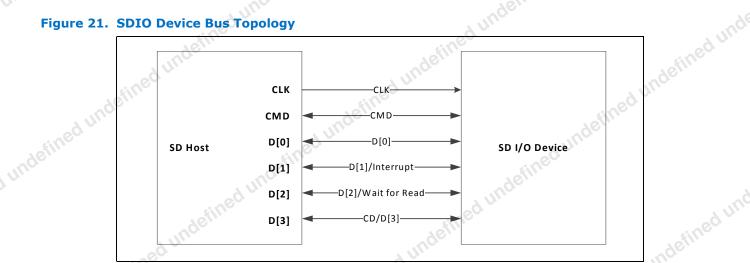
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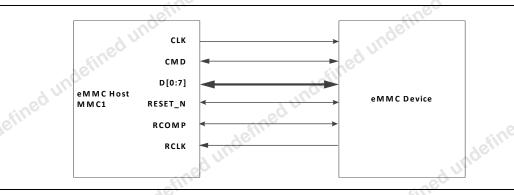


Figure 21. SDIO Device Bus Topology



12.3.4.3 eMMC 4.51 Interface

Figure 22. eMMC Interface



The standard offers performance enhancement features, including HS400 support and has an interface bandwidth of 400 MByte/sec.

The command protocol is significantly improved with Packed Commands (the ability to group a series of commands in a single data transaction), Context ID (grouping different memory transactions under a single ID so the device can understand that they are related), and Data Tag (tagging specific write transactions so they can be prioritized and targeted to a memory region with higher performance and better reliability).

The v4.51 standard also adds provision for volatile data cache, which can greatly reduce the latency between data transactions to improve performance. e

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12.4 References

The controller is configured to comply with:

- SD Specification Part 01 Physical Layer Specification version 3.00, April 16, 2009.
- SD Specification Part E1 SDIO Specification version 3.00, December 16, 2010.
- SD Specification Part A2 SD Host Controller Standard Specification version 3.00, February 18, 2010.
- SD Specification Part 03 security Specification version 1.01, April 15, 2001.
- Embedded MultiMedia Card (eMMC) Product Standard v4.51, JESD84-A5.

Register Map 12.5

Jundefined undefined undefined undefined undefined For more information on SoC Storage registers refer Intel[®] Atom[™] Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID: 332066.

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USB Controller Interfaces 13

USB Controller contains xHCI host controller that supports xHCI framework and USB1/ 2/3 specifications. And it has xDCI controller block for device only mode functionality. These 2 controllers will use an integrated mux to select between the 2 modes. All of this functionality is located in xDCI Controller.

SoC Supports

- Two (2) Super Speed Inter-Chip (SSIC) ports
- Three (3) Super Speed (SS) ports [Backward Compatible of USB 2.0 HS/FS/LS]
- One (1) Super Speed (SS) OTG port
- Two (2) High Speed Inter-Chip (HSIC) ports

SoC can support the 4th SS port when OTG port is in Host mode.

Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 82. **USB SSIC Signals**

	Signal Name	Direction /Type	Description
	USB_SSIC_RX_P/ N[0,1]	I/O/ SSIC PHY	Receiver serial data inputs: High-speed serialized data inputs.
	USB_SSIC_TX_P/ N[0,1]	I/O/ SSIC PHY	Transmitter serial data outputs: High-Speed Serialized data outputs.
sined	USB_SSIC_RCOMP _P/N	I / SSIC PHY	Resistor Compensation: An external resistor of 90 Ohm $\pm 1\%$ must be connected between the RCOMP pads.
ed undefined	undefined unde	ined .	Betined underined underined Datas
	ndefine		defined



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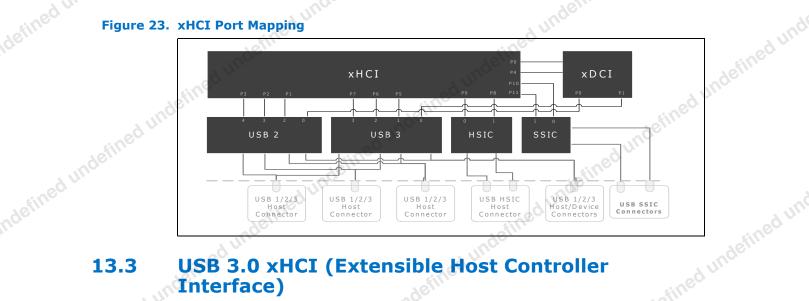
	ined under.			ed undefine	defined c
USB Controlle USB Controlle Undefined Table 83.	er Interfaces	Indefine	d undef	med to intel	
Table 83.	USB Signals	Direction		sined unc	ed u
	Signal Name	/Туре		Description	retine
	USB3_TXP/ N[0:3]	O USB3 PHY		itter serial data outputs: High-Speed Serialized puts.	Nor
stined un.	USB3_RXP/ N[0:3]	I USB3 PHY		r serial data inputs: High-speed serialized data	
d under.	USB3_RCOMP_P /N	I USB3 PHY		r Compensation: An external resistor of 402 Ohm ist be connected between the RCOMP pads.	
stine	USB_DP/N[0:3]	I/O USB2 PHY		ata: High speed serialized data I/O.	6-
	USB_RCOMP	O USB2 PHY		r Compensation: An external resistor of 113 Ohm ist be connected between pin and GND.	definec
ind	USB_OTG_ID	I/O USB2 PHY		Pin out to detect the OTG ID.	0
terined t	USB_PLL_MON	O USB2 PHY		n Speed Observation	
ed unot	USB_VBUSSNS	I/O USB2 PHY		erface: VBUS_Sense	
Table 84.	HSIC Signals			estined u.	ned
	Signal Nam	e C	irection	Description	defin

Table 84. HSIC Signals

ned un	USB2 F		adeilie	
undefined ^{ull} . Table 84.	HSIC Signals		tetined u.	undefined un
	Signal Name	Direction /Type	Description	undeit
sined unc	USB_HSIC[0:1]_DATA	I/O HSIC Buffer	HSIC Data.	
d undefined undefined und	USB_HSIC[0:1]_STROBE	I/O HSIC Buffer	HSIC Strobe	
Jundetti	USB_HSIC_RCOMP	I/O HSIC Buffer	Resistor Compensation: RCOMP for HSIC buffer. Resistor: 450hm +/-1% connected between USB_HSIC_RCOMP and ground.	defined
ad undefined undefined un	defined undefined un	defined	Resistor Compensation: RCOMP for HSIC buffer. Resistor: 450hm +/-1% connected between USB_HSIC_RCOMP and ground.	2 U.
	ndefined undefine		defined undefined t	ed undefined i
Datasheet			unde 153	3
Letined underine	ined	nder	d undefine	



Figure 23. xHCI Port Mapping



USB 3.0 xHCI (Extensible Host Controller 13.3 **Interface**)

The xHCI compliant host controller can control up to 2 SSIC, 3 USB3.0 ports. USB3.0 being backward compatible to support USB2.0. It supports devices conforming to USB 1.x to 3.0 at bit rates up to 5 Gbps.

undefined undefin 13.3.1 **USB 3.0 Host Features**

The USB 3.0 Super Speed data interface is a four wire differential (TX and RX pairs) interface that supports simultaneous bi-directional data transmission. The interface supports a bit rate of 5 Gbps with a maximum theoretical data throughput over 3.2 Gbps due to 8b/10b symbol encoding scheme and protocol overhead (link flow control, packet framing and protocol overhead).

Low Frequency Periodic signaling (LFPS) is used to communicate initialization, training and power management information across a link that is in low power link state without using Super Speed signaling. This reduces power consumption.

13.3.1.1 **USB SSIC**

- Supports the SuperSpeed protocol only as defined in [USB 3.0].
- Optimized for Power, Area, Cost and EMI robustness.
- Supports 2 ports of 1 lane each.

USB 3.0

- Supported by xHCI software host controller interface.
- USB3 port disable.
- Supports local dynamic clock gating and trunk clock gating.
- Supports USB 3.0 LPM (U0, U1, U2, and U3) and also a SS Disabled low power .ate state. \lambda

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13.3.1.2



- Supports USB3 Debug Device.
- Supports IVCAM(USB PC Camera).

13.3.2 USB HSIC Features

HSIC is a 2-signal (strobe and data) source synchronous serial interface for on board inter-chip USB communication. The interface uses 240 MHz DDR signaling to provide High-Speed 480 Mb/s USB transfers which are 100% host driver compatible with traditional USB cable connected topologies. Full Speed (FS) and Low Speed (LS) USB transfers are not directly supported by the HSIC interface.

Major feature and performance highlights are as follows:

- Supported by xHCI software host controller interface
- High-Speed 480 Mb/s data rate only.
- Source-synchronous serial interface.
- Power is only consumed when a transfer is in progress.
- No Plug and Play support.
- No hot plug removal/attach.
- Signals driven at 1.2V standard LVCMOS levels.
- Designed for low power applications.
- Support for two host ports compliant to High Speed Inter-Chip Supplement (HSIC) to the USB 2.0 Specification. (USB 2.0).
- Clock request/ack mechanism.

13.4 USB 3.0 xDCI (Extensible Device Controller Interface)

The xDCI compliant Device controller can control up to 1 USB3.0 OTG port. USB3 being backward compatible to support USB2.0. It supports devices conforming to USB 1.x to 3.0 at bit rates up to 5 Gbps.

13.5 References

USB 3.0 Specification

USB 2.0 Specification (Includes High-Speed Inter-Chip USB Electrical Specification)

13.5.1 Host Controller Specifications

Extensible Host Controller Interface (xHCI) Specification for USB 3.0 version 1.0.



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Low Power Engine (LPE) for Audio (I²S)



Low Power Engine (LPE) for Audio (I²S) 14

Low Power Engine for Audio provides acceleration for common audio and voice functions. The voice and audio engine provides a mechanism for rendering audio and voice streams and tones from the operating system, applications to an audio or voice codec, and ultimately to the speaker, headphones, or Bluetooth* headsets.

Audio streams in the SoC can be encoded and decoded by the Low Power Engine (LPE) in the Audio subsystem.

LPE Audio provides three external I²S audio interfaces.

Signal Descriptions 14.1

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional). ined undefined
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 85. LPE Signals

Signal Name	Direction /Type	Description
LPE_I2S[2:0]_CLK	I/O	Clock signal for I ² S
LPE_I2S[2:0]_FRM	I/O	Frame select signal for I ² S
LPE_I2S[2:0]_DATAIN	I/O	RX data for I ² S
LPE_I2S[2:0]_DATAOUT	I/O	TX data for I ² S

NOTE: All LPE signals are muxed and may be used by other functions.

Features

The LPE Audio Subsystem consists of the following:

- Integrated, power-efficient 32-bit architecture core with 24-bit audio processing instructions.
- in a undefined undefined undefined • Core processing speeds up to 343 MHz.
- Closely Coupled Memories (CCMs)
 - 80 KB Instruction RAM

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Low Power Engine (LPE) for Audio (I²S)



- 160 KB Data RAM
- 48 KB Instruction Cache
- 96 KB Data Cache
- Very low-power consumption coupled with high-fidelity 24-bit audio.
- Dual-issue, static, super-scalar VLIW processing engine.
- Mode-less switching between 16-, 24-, and 64-bit dual-issue instructions.
- Dual MACs which can operate with 32 x 16-bit and/or 24 x 24-bit operands.
- Inter-Process Communication (IPC) mechanism to communicate with the SoC Processor Core including 4 KB mailbox memory.
- Flexible audio interfaces include three SSPs with I²S port functionality for BI-directional audio transfers.
 - I²S mode supports PCM payloads
 - Frame counters for all I²S ports
- High Performance DMA
 - DMA IP to support multiple outstanding transactions
 - Interleaved scatter-gather support for Audio DMA transfers
- Clock switching logic including new frequency increments.
- External timer function with an always running clock.

The LPE core runs at a peak clock frequency of 343 MHz and has dedicated on-chip program and data memories and caches. The LPE core can access shared SRAM blocks, and external DRAM through OCP fabric. It communicates with audio peripherals using the audio sub-fabric, and employs Inter-Processor Communication (IPC) mechanism to communicate with the SoC Processor Core.

The Audio subsystem includes two OCP-based DMA engines. These DMA engines support single and multi-block transfers. They can be configured to transfer data between DRAM and audio CCMs or transfer data between CCMs and the audio peripheral interfaces.

All these interfaces are peripherals in the Audio subsystem. LPE, LPE DMA, or the SoC processor core may access the peripherals during normal operation. The PMC may access all peripherals during specific tasks such as at boot time or during power state changes. A complete audio solution based on an internal audio processing engine which includes several I²S-based output ports.

The audio core used is a dedicated audio DSP core designed specifically for audio processing (decoding, post-processing, mixing, etc.)

Note:

LPE requires systems with more than 512 MB memory. This is required since the LPE firmware must reside at a stolen memory location on 512 MB boundaries below 3 GiB. The LPE firmware itself is \sim 1 MB, and is reserved by BIOS for LPE use.

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Low Power Engine (LPE) for Audio (I²S)



Audio Capabilities 14.2.1

14.2.1.1 **Audio Decode**

undefined undefined undefined undefined undefined Audio core supports decoding of the following formats:

- MP3
- AAC-LC
- HE-AAC v1/2
- WMA9,10, PRO, Lossless, Voice
- MPEG layer 2
- RealAudio
- OggVorbis
- FLAC
- DD/DD+

14.2.1.2

Audio Encode

ndefined undefined undefined undefined undefined undefined Audio core supports encoding of the following formats:

- MP3
- AAC-LC
- WMA
- DD-2channel

14.3

Clocks

14.3.1 **Clock Frequencies**

Table 86. **Clock Frequencies**

der	Table 86 shows the cloc Clock Frequencies	ck frequency options for the a	Audio functional blocks.	sined "
	Clock	Frequency	Notes	Inden
red un	Audio core	343/250/200 MHz/100/ 50 MHz/2x Osc/Osc 50(RO)/100(RO)	Audio input clock trunk. CCU drives one of several frequencies as noted.	5
defille	DMA 0	50/OSC	DMA clock	1
y unc	DMA1	50/OSC	DMA clock	1
undefined undefines	Audio fabric clock	50/OSC	Fabric clock derived from audio core clock	1
,d ^u	ndefined under	ndefined	ndefin	d undefined
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undefined undef Low Power Engine (LPE) for Audio (I²S)

Table 86. **Clock Frequencies**

Clock Frequencies	TUC	inder	
Clock	Frequency	Notes	dune
SSP0 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP0 clock domains	ndefinec
SSP1 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP1 clock domains	
SSP2 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP2 clock domains	

undefined und 14.3.2 38.4 MHz Clock for LPE

38.4 MHz, the 2X OSC clock, is added to increase MIPS for low power MP3 mode. This frequency will be supplied by the clock doubler internal to the SoC's Clock Control Unit.

Calibrated Ring Osc (50/100 MHz) Clock for LPE 14.3.3

A calibrated Ring Oscillator in the CCU SUS provides a 50Mhz or an 100Mhz clock as another option for higher MIPS for low power MP3 mode. It is expected that this will be required to support decode of HE-AAC streams in the low power mode.

14.3.4 Cache and CCM Clocking

Data CCM, Data cache, Instruction CCM, and Instruction Cache run off of the LPE clock. These memories are in a single clock domain.

Note:

All Data CCM and Instruction CCM run in the same clock domain.

SSP (I²S)

The SoC audio subsystem consists of the LPE Audio Engine and three Synchronous Serial Protocol (SSP) ports. These ports are used in PCM mode and enable simultaneous support of voice and audio streams over I²S. The SoC audio subsystem also includes two DMA controllers dedicated to the LPE. The LPE DMA controllers are used for transferring data between external memory and CCMs, between CCMs and the SSP ports, and between CCMs. All peripheral ports can operate simultaneously.

The Enhanced SSP Serial Ports are full-duplex synchronous serial interfaces. They can connect to a variety of external analog-to-digital (A/D) converters, audio, and telecommunication codecs, and many other devices which use serial protocols for transferring data. Formats supported include National* Microwire, Texas Instruments* Synchronous Serial Protocol (SSP), Motorola* Serial Peripheral Interface (SPI) protocol and a flexible Programmable Serial Port protocol (PSP). undefined undefined undefine

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The Enhanced SSPs operate in master mode (the attached peripheral functions as a slave) or slave mode (the attached peripheral functions as a master), and support serial bit rates from 0 to 6.5 Mbps, dependent on the input clock. Serial data formats range from 4 to 32-bits in length. Two on-chip register blocks function as independent FIFOs for transmit and receive data.

FIFOs may be loaded or emptied by the system processor using single transfers or DMA burst transfers of up to the FIFO depth. Each 32-bit word from the bus fills one entry in a FIFO using the lower significant bits of a 32-bit word.

14.4.1 **Features**

The SSP port features are:

- Inter-IC Sound (I²S) protocols, are supported by programming the Programmable Serial Protocol (PSP).
- One FIFO for transmit data (TXFIFO) and a second, independent, FIFO for receive data (RXFIFO), where each FIFO is 16 samples deep x 32 bits wide.
- Data sample sizes from 8, 16, 18, or 32 bits.
- 6.5 Mbps maximum serial bit-rate in both modes: master and slave.
- Clock master or slave mode operations.
- Receive-without-transmit operation.
- Network mode with up to eight time slots for PSP formats, and independent transmit/receive in any/all/none of the time slots.
- After updating SSP configuration, for example active slot count, the SSP will need to be disabled and enabled again. In other words, a SSP will not function correctly if a user changes the configuration setting on the fly.

14

Register Map

indefined undefined undefined undefined undefined undefined For more information on Low Power Engine (LPE) for Audio (I2S) registers refer Intel® Atom[™] Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066. - 0i

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Intel[®] Trusted Execution Engine (Intel[®] TXE)



15 Intel[®] Trusted Execution Engine (Intel[®] TXE)

This chapter describes the security components and capabilities. The security system contains an $Intel^{\textcircled{R}}$ TXE and additional hardware security feature that enable a secure and robust platform.

15.1 Features

15.1.1 Security Features

Intel[®] TXE in the SoC is responsible for supporting and handling security related features.

- 32-bit RISC processor.
- 256KB Data/Code RAM accessible only to the Intel[®] TXE.
- 128KB On Chip Mask ROM for storage of Intel[®] TXE code.
- Inter-Processor Communication for message passing between the Host CPU and Intel® TXE.
- 64 byte input and output command buffers.
- 256 byte shared payload (enables 2048-bit keys to be exchanged as part of the command).
- Multiple context DMA engine to transfer data between Host CPU address domain (System memory) and the Intel[®] TXE; programmable by the Intel[®] TXE CPU only.
- Secure I²C interface to NFC using master I²C block integrated into the Intel TXE -IP. Secure GPIOs to support input alert and two GP Outputs.

15.1.1.1 HW Accelerators

- DES/3DES (ECB, CBC) 128b ABA key for 3DES Key Ladder Operations.
- Three AES engines Two fast -128 and one slow- 128/256.
- Exponentiation Acceleration Unit (EAU) for modular exponentiation, modular reduction, large number addition, subtraction, and multiplication.
- SHA1, SHA256/384/512, MD5.

15.1.1.2 FW Utilities and Ciphers

- RSA (with EAU acceleration).
- Flash Write Enable/Disable.
- Comprehensive IPC Command Set.
- Chip Unique Key encryption key wrapping of other platform keys (Flash).

undefined unde Intel[®] Trusted Execution Engine (Intel[®] TXE)



Downloadable FW Utilities and Ciphers 15.1.1.3

- defined undefined un Integrated Theft Deterrence Technology - Intel[®] Anti-Theft Technology (Intel[®] AT).
- One Time Programmable (OTP).
- Firmware TPM (fTPM) measured boot.

15.1

TXE Interaction with NFC

- The NFC device requests attention from the TXE from GPIO_ALERT pin to a SoC input interrupt pin (GPIO_SUS[8] pin).
- The GPIO block sends the pin value to TXE over a dedicated wire.
- The wire is connected to the TXE clock request mechanism in order to get a clock for sampling the wire. The TXE bridge includes a configuration register which includes an enable bit to qualify the clock request (which allows masking the clock request, in case the GPIO_SUS[8] is not used by NFC), and a polarity bit (which allows selecting whether the a clock request would be set on a high or low value in the wire).)
- The same qualified & polarity configured clock request input is also sent to PMU. In S0ix PMU uses it as a wake request.
- When a clock is available, the wire value is updated to an ICR (SICR31) in TXE bridge.
- TXE Bridge configuration register also includes two bits that allow detection of falling and/or rising edge on the alert pin. They cause an ISR (SISR[31]) to be set. When both ISR and IER bits for the alert are set an interrupt is generated.
- When the TXE is interrupted it parses the interrupt status registers in the TXE Bridge and figures the cause is the NFC device.
- TXE clears the Bridge ISR and sets configuration to detect the next edge on the alert pin.
- In order to use the I2C master, the TXE sets an I2C clock request register in the Bridge.
- The firmware then uses the I2C master to communicate with the NFC device. The firmware configures the I2C master to read up to 33Bytes of data (up to 36 bytes are supported by HW for read/write).
- When the I2C read is completed, the firmware is interrupted. The TXE may then read the data/status and clear the interrupt.
- The firmware repeats read/write sequence's as many times as it needs.
- When firmware is done with the I2C master, it must poll the controller to check that the I2C bus is idle before writing to the register to remove the I2C clock request, and before any reset of the I2C controller or power gating sequence. Shutting off clock or I2C master before the completion all activity on the bus will hang the I2C A undefined undefined undefined in a sundefined undefined undefi device.

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Intel[®] Sensor Hub

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16.1 V

Intel[®] Sensor Hub 16

This chapter describes Intel[®] Sensor Hub.

Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- adefined undefined • Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 87. ISH Signals

Signal Name	Direction	Description
ISH_I2C1_CLK	I/O	Clock Lane: ISH input clock
ISH_I2C1_SDA	I/O	Data Lane: ISH Data Lane
ISH_GPIO	I/O	ISH GPIO

16.2 **Features**

- Acquisition / sampling of sensor data.
- The ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS.
- Low power operation through clock gating of the ISH together with the ability to turn sensors off under control of host SW.
- The ability to operate independently when the host platform is in a low power state(S0-S0i3).
- Power saving features.
- Clock gating and power gating of functional blocks depending on current workloads.

Hardware

- Minute IA microprocessor.
- 384KB on chip Data/Code SRAM accessible only to the ISH.
- 8KB on chip ROM for ISH boot code. in a sum defined undefined un

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16.2.1

Intel[®] Sensor Hub



- Inter-Processor Communication for message passing between the Host CPU and Intel[®] ISH.
 - Single Command/Doorbell DWORD register and 32 DWORD data registers each direction.
- Inter-Processor Communication for message passing between the Intel[®] ISH and Intel[®] TXE for ISH FW load.
 - Single Command/Doorbell DWORD register and 32 DWORD data registers each direction.
- Inter-Processor Communication for message passing between the Intel[®] ISH and •
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SIO - Serial Peripheral Interface (SPI) 17.1

The Serial I/O implements three SPI controllers that supports master mode.

17.1.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 88. SPI Interface Signals undefined undefined ur

• Description: A	·	nation of the signal's function.	Indefineo
Signal Name	Direction /Type	Description	
SPI[1,2,3]_CLK	O GPIO	SPI Clock: When the bus is idle, the owner will drive the clock signal low.	
SPI[1,2,3]_CS[0]_N	O GPIO	SPI Chip Select 0: Used as the SPI Chip select 0.	
SPI[1,2,3]_CS[1]_N	O GPIO	SPI Chip Select 1: Used as the SPI Chip select 1.	lefined
SPI[1,2,3]_MISO	I GPIO	SPI Master IN Slave OUT: Data input pin for the SoC.	unos
SPI[1,2,3]_MOSI	O GPIO	SPI Master OUT Slave IN: Data output pin for the SoC. Operates as a second data input pin for the SoC when in Single Input, Dual Output Fast Read mode.	

defined undefined uni Features

The following is list of SPI features:

- Single interrupt line.
 - Could be assigned to interrupt PCI INT [A] or ACPISIO INT[1].
- Configurable frame format, clock polarity and clock phase.
- Supports three SPI peripherals only.
- Two Chip selects are supported for each of the 3 SPI controllers.
- Supports master mode only.
- Receive and transit buffers are both 256x32 Bits.
 - The receive buffer has only 1 water mark.
 - The transmit buffer has 2 water marks.

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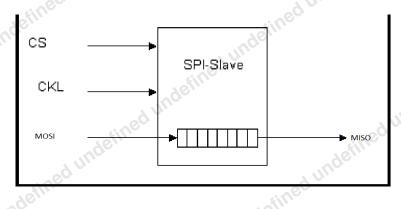
• Supports up to 20 Mbps.

17.1.2.1 General

The Serial Peripheral Interface is used primarily for a synchronous serial communication of host processor and peripherals.

In the standard configuration for a slave device, two control and two data lines are used. The data output MISO serves on the one hand the reading back of data, offers however also the possibility to cascade several devices. The data output of the preceding device then forms the data input for the next IC.

Figure 24. SPI Slave



There is a MASTER and a SLAVE mode. The MASTER device provides the clock signal and determines the state of the chip select lines, i.e. it activates the SLAVE it wants to communicate with. CS and CKL are therefore outputs. The SLAVE device receives the clock and chip select from the MASTER, CS and CKL are therefore inputs. This means there is one master, while the number of slaves is only limited by the number of chip selects.

A SPI device can be a simple shift register up to an independent subsystem. The basic principle of a shift register is always present. Command codes as well as data values are serially transferred, pumped into a shift register and are then internally available for parallel processing.

The SPI requires two control lines (CS and CLK) and two data lines MOSI (Master-Out-Slave-In) and MISO (Master-In-Slave-Out).

17.1.2.2

2 Data and Control lines for SPI

With CS (Chip-Select) the corresponding peripheral device is selected. This pin is mostly active-low. In the un-selected state the MISO lines are hi-Z and therefore inactive. The master decides with which peripheral device it wants to communicate. The clock line CLK is brought to the device whether it is selected or not. The clock serves as synchronization of the data communication. The majority of SPI devices provide these four lines. Sometimes it happens that MOSI and MISO are multiplexed.

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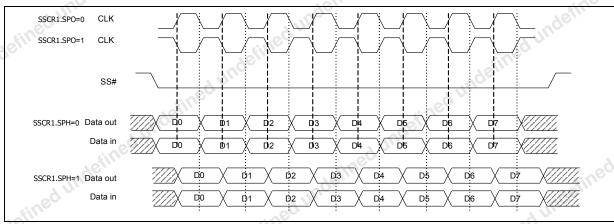
ndefined undefined SPI Configuration: Clock Phase and Polarity 17.1.2.3

SPI clock phase and clock polarity overview.

- undefined unde The SSCR1.SPO polarity setting bit determines whether the serial transfer occurs on the rising edge of the clock or the falling edge of the clock.
 - When SSCR1.SPO = 0, the inactive or idle state of SPI1 CLK is low.
 - When SSCR1.SPO = 1, the inactive or idle state of SPI1_CLK is high.
- The SSCR1.SPH phase setting bit selects the relationship of the serial clock with the • slave select signal.
 - When SSCR1.SPH = 0, SPI1 CLK is inactive until one cycle after the start of a frame and active until 1/2 cycle after the end of a frame.
 - undefined un — When SSCR1.SPH = 1, SPI1_CLK is inactive until 1/2 cycle after the start of a frame and active until one cycle after the end of a frame.

Below figure shows an 8-bit data transfer with different phase and polarity settings.

Figure 25. Clock Phase and Polarity



In a single frame transfer, the SPI controller supports all four possible combinations for the serial clock phase and polarity.

The combinations of polarity and phases are referred to as modes which are commonly numbered according to the following convention, with SSCR1.SPO as the high order bit and SSCR1.SPH as the low order bit.

Table 89. **SPI Modes** ed undefined undefined

undefined un	Mode	SSCR1.SPO	SSCR1.SPH
	0	0	0 0
	1	0	1
	2	1	100 0
	3	1 0	1
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SIO - I²C Interface 17.2

ed undefined und The SoC supports 7 instances of I^2C controller. Both 7-bit and 10-bit addressing modes are supported. These controllers operate in master mode only.

Signal Descriptions 17.2.1

I²C is a two-wire bus for inter-IC communication. Data and clock signals carry information between the connected devices. The following is the I^2C Interface. The SoC supports 7 I²C interfaces for general purpose to control external devices. The I²C signals are muxed over GPIOs.

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 90. I²C[6:0] Signals

² C[6:0] Signals	und	nder	_
Signal Name	Direction /Type	Description	based
I2C[6:0]_DATA	I/O/	I ² C Serial Data	1efill
lefinec	GPIOMV, MS, I2C	These signals are muxed and may be used by other functions.	ed unos
12C[6:0]_CLK	I/O/	I ² C Serial Clock	
	GPIOMV, MS, I2C	These signals are muxed and may be used by other functions.	
NFC I ² C Interf	ace Sign	als undefine	_
IFC I ² C Interface S			

NFC I²C Interface Signals 17.2.2

Table 91. NFC I²C Interface Signals

ofine 17.2.2	NFC I ² C Interf	ace Signa	als dunde	
Table 91.	NFC I ² C Interface S	Signals	definer	-fined u
e -	Signal Name	Direction/ Type	Description	d under.
offined	NFC_I2C_DATA	I/O/ GPIOMV, MS, I2C	NFC I²C Serial Data These signals are muxed and may be used by other functions.	Nec
sined unde.	NFC_I2C_CLK	I/O/ GPIOMV, MS, I2C	NFC I²C Serial Clock These signals are muxed and may be used by other functions.	
ed under.	GPIO_ALERT	I/O/ GPIOMV, MS	ALERT pin for NFC These signals are muxed and may be used by other functions.	defined
	ndefine		defined	ined unc
170 mdefined			Datash	eet
settned b.		ned unc	d under.	



17.2.3 **Features**

I²C Protocol 17.2.3.1

The I^2C bus is a two-wire serial interface, consisting of a serial data line and a serial clock. These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a "transmitter" or "receiver," depending on the function of the device. Devices are considered slaves when performing data transfers, as the SoC will always be a Master. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

- The SoC is always the I²C master; and it supports multi-master mode.
- The SoC can support clock stretching by slave devices.
- The I2Cx_DATA line is a bidirectional signal and changes only while the I2Cx_CLK line is low, except for STOP, START, and RESTART conditions.
- The output drivers are open-drain or open-collector to perform wire-AND functions on the bus.
- The maximum number of devices on the bus is limited by the maximum capacitance specification of 400 pF. Refer Chapter 19, "Electrical Specifications" for more details.
- Data is transmitted in byte packages.

Indefined undefi I²C Modes of Operation 17.2.3.2

The I²C module can operate in the following modes:

- Standard mode (with a bit rate up to 100 Kb/s).
- Fast mode (with a bit rate up to 400 Kb/s).
- Fast Mode plus mode (with a bit rate up to 1 Mb/s).
- High-speed mode (with a bit rate up to 1.7 Mb/s).

The I²C can communicate with devices only using these modes as long as they are attached to the bus. Additionally, high speed mode, fast mode plus and fast mode devices are downward compatible.

- High-speed mode devices can communicate with fast mode and standard mode devices in a mixed speed bus system.
- Fast mode devices can communicate with standard mode devices in a 0-100 Kb/s I²C bus system.

However, according to the I^2C specification, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I²C bus system since they cannot follow the higher transfer rate and unpredictable states would occur.

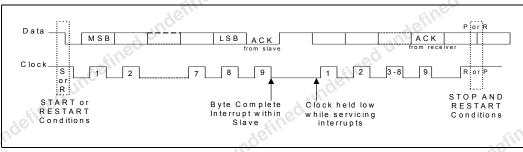
Refer Table 1 for more information on the I2C interface speed for different Sku's.



17.2.3.3 **Functional Description**

- The I²C master is responsible for generating the clock and controlling the transfer of data.
- The slave is responsible for either transmitting or receiving data to/from the master.
- The acknowledgement of data is sent by the device that is receiving data, which can be either a master or a slave.
- Each slave has a unique address that is determined by the system designer:
 - When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W), to determine if the master wants to transmit data or receive data from the slave.
 - The slave then sends an acknowledge (ACK) pulse after the address.
- If the master (master-transmitter) is writing to the slave (slave-receiver)
 - The receiver gets one byte of data.
 - This transaction continues until the master terminates the transmission with a STOP condition.
- If the master is reading from a slave (master-receiver)
 - The slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse.
 - This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in below figure.

Figure 26. Data Transfer on the I²C Bus



17.2.3.3.1 **START and STOP Conditions**

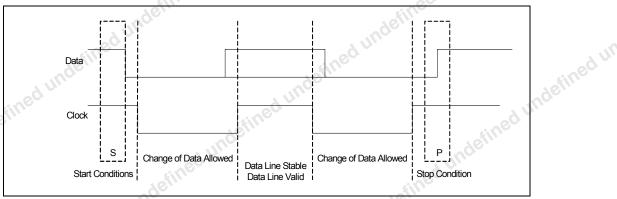
When the bus is idle, both the clock and data signals are pulled high through external pull-up resistors on the bus.

When the master wants to start a transmission on the bus, the master issues a START immed undefined undefined ut condition.



- This is defined to be a high-to-low transition of the data signal while the clock is • high.
- When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the data line while the clock is high. Figure 27 shows the timing of the START and STOP conditions.
- When data is being transmitted on the bus, the data line must be stable when the clock is high.

Figure 27. START and STOP Conditions



undefined undefined unde The signal transitions for the START/STOP conditions, as depicted above, reflect those undefined undefined observed at the output of the master driving the I^2C bus. Care should be taken when observing the data/clock signals at the input of the slave(s), because unequal line delays may result in an incorrect data/clock timing relationship.

NFC I²C 17.3

NFC device requires 1.8V I/Os.

For more information refer "TXE Interaction with NFC"

17.3.1 References

I²C-Bus Specification and User Manual, Revision 03: http://ics.nxp.com/support/ documents/interface/pdf/i2c.bus.specification.pdf

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SIO - High Speed UART 17.4

stined undefined undefined undefined The SoC implements two instances of high speed UART controller that support baud rates between 300 and 3686400. Hardware flow control is also supported.

Signal Descriptions 17.4.1 Indefined undefined

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 92. UART 1 Interface Signals undefined undefined

• Signal Name: The	ne name of th	e signal/pin.	
• Direction: The b	uffer direction	n can be either input, output, or I/O (bidirectional).	Inc
• Type: The buffer	type found in	Chapter 19, "Electrical Specifications".	
• Description: A b	orief explanati	on of the signal's function.	ndetin
UART 1 Interface S	ignals	Jefineo sinec	
Signal Name	Direction/ Type	Description	
UART1_DATAIN	I/O/ GPIOMV, MS	High-speed UART receive data input : This signal is muxed and may be used by other functions.	
UART1_DATAOUT	I/O/ GPIOMV, MS	High-speed UART transmit data: This signal is muxed and may be used by other functions.	defined un
UART1_RTS_N	I/O/ GPIOMV, MS	High-speed UART request to send: This signal is muxed and may be used by other functions.	d une
UART1_CTS_N	I/O/ GPIOMV, MS	High-speed UART clear to send: This signal is muxed and may be used by other functions.	
			1

undefined undefined ur Table 93. UART 2 Interface Signals

du		- no	runcuonor	
define Table 93.	UART 2 Interface	Signals	thed unc	
	Signal Name	Direction/ Type	Description	ndefine
	UART2_DATAIN	I/O/ GPIOMV, MS	High-speed UART receive data input: This signal is muxed and may be used by other functions.	ed un
tertined .	UART2_DATAOUT	I/O/ GPIOMV, MS	High-speed UART transmit data: This signal is muxed and may be used by other functions.	
ed unor	UART2_RTS_N	I/O/ GPIOMV, MS	High-speed UART request to send: This signal is muxed and may be used by other functions.	
ndefilit	UART2_CTS_N	I/O/ GPIOMV, MS	High-speed UART clear to send: This signal is muxed and may be used by other functions.	
	indefined un		Jeffined unde	red undefin
174 indefined		t undefi	Datashee	t
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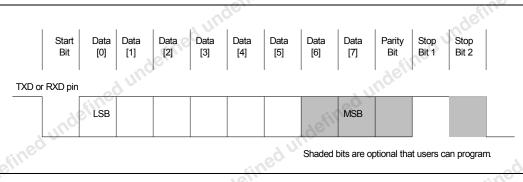
17.4.2 Features

17.4.2.1 **UART Function**

The UART transmits and receives data in bit frames as shown in Figure 29.

- Each data frame is between 7 and 12 bits long, depending on the size of data programmed and if parity and stop bits are enabled.
- The frame begins with a start bit that is represented by a high-to-low transition.
- Next, 5 to 8 bits of data are transmitted, beginning with the least significant bit. An optional parity bit follows, which is set if even parity is enabled and an odd number of ones exist within the data byte; or, if odd parity is enabled and the data byte contains an even number of ones.
- The data frame ends with one, one-and-one-half, or two stop bits (as programmed by users), which is represented by one or two successive bit periods of a logic one.

Figure 29. UART Data Transfer Flow



Each UART has a Transmit FIFO and a Receive FIFO and each holds 64 characters of data. There are two separate methods for moving data into/out of the FIFOs-Interrupts and Polling.

17.4.2.2 **Clock and Reset**

The BAUD rate generates from base frequency of 50 MHz.

17.4.2.3 **Baud Rate Generator**

The baud rates for the UARTs are generated with from the base frequency (Fbase) indicated in Table 94 by programming the DLH and DLL registers as divisor. The hexadecimal value of the divisor is (IER_DLH[7:0]<<8) | RBR_THR_DLL[7:0].

Fbase 44236800 Hz can be achieved by programming the DDS Multiplier as 44,236,800 (in decimal), and DDS Divisor as the system clock frequency in Hz. (50,000,000 in decimal when the system clock frequency is 50 MHz.) in the fined undefined undefine

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fined undefined undefine hed undefined undefined undefined The output baud rate 3686400 is equal to the base frequency divided by thirteen times the value of the divisor, as follows: baud rate = (Fbase) / (13 * divisor). The output baud rate for all other baud rates is equal to the base frequency divided by sixteen times the value of the divisor, as follows: baud rate = (Fbase) / (16 * divisor).

Table 94. **Baud Rates Achievable with Different DLAB Settings** Indefined undefined und

efined undefined und	DLH,DLL Divisor	DLH,DLL Divisor Hexadecimal	Baud Rate	ned undefined u
einec		Fbase 1: 47923200 Hz		, une
dell	1	0001	3686400	heo
d ull		Fbase 2: 44236800 Hz	AGI	
cin ^{e0.}	1	0001	2764800	
311.	3	0003	921600	
	6	0006	460800	cine ^O
	9	0009	307200	Activi
	12	000C	230400	nd undefined undefined
à	15	000F	184320	O _e o
4 UM	18	0012	153600	18fills
ine ^o	24	0018	115200	Inoc
defin	48	0030	57600	edu
afined undefined un	72	0048	38400	Inc
ed -	144	0090	19200	
	288	0120	9600	
	384	0180	7200	- C
	576	0240	4800	1. Stille
	768	0300	3600	inoc
	1152	0480	2400	du
10.	1536	0600	1800	ATING
ed	2304	0900	1200	ed undefined undefiner
1efille	4608	1200	600	du'
inoc	9216	2400	300	4ine-
defined undefined un	Use	d une	und und	

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Use

(intel) ed under

ined undefined undefined Each UART has a transmit FIFO and a receive FIFO, each FIFO holding 64 characters of data. Three separate methods move data into and out of the FIFOs: interrupts, DMA, and polled.

DMA Mode Operation 17.4.3.1

17.4.3.1.1 **Receiver DMA**

The data transfer from the HSUART to host memory is controlled by the DMA write channel. To configure the channel in write mode, channel direction in the channel control register needs to be programmed to "1". The software need to program the

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descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

17.4.3.1.2 Transmit DMA

The data transfer from host memory to HSUART is controlled by DMA read channel. To configure the channel in read mode, channel direction in the channel control register needs to be programmed to "0". The software need to program the descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

17.4.3.1.3 Removing Trailing Bytes in DMA Mode

When the number of entries in the Receive FIFO is less than its trigger level, and no additional data is received, the remaining bytes are called Trailing bytes. These are DMAed out by the DMA as it has visibility into the FIFO Occupancy register.

17.4.3.2 FIFO Polled-Mode Operation

With the FIFOs enabled (IIR_FCR.IID0_FIFOE bit set to 1), clearing IER_DLH[7] and IER_DLH[4:0] puts the serial port in the FIFO Polled Operation mode. Because the receiver and the transmitter are controlled separately, either one or both can be in Polled Operation mode. In this mode, software checks Receiver and Transmitter status using the Line Status Register (LSR). The processor polls the following bits for Receive and Transmit Data Service.

17.4.3.2.1 Receive Data Service

The processor checks data ready (LSR.DR) bit which is set when 1 or more bytes remains in the Receive FIFO or Receive Buffer Register (RBR_THR_DLL).

17.4.3.2.2 Transmit Data Service

The processor checks transmit data request LSR.THRE bit, which is set when the transmitter needs data.

The processor can also check transmitter empty LSR.TEMT, which is set when the Transmit FIFO or Holding register is empty.

17.4.3.2.3 Autoflow Control

Autonow Control

Autoflow Control uses Clear-to-Send (nCTS) and Request-to-Send (nRTS) signals to automatically control the flow of data between the UART and external modem. When autoflow is enabled, the remote device is not allowed to send data unless the UART asserts nRTS low. If the UART de-asserts nRTS while the remote device is sending data, the remote device is allowed to send one additional byte after nRTS is deasserted. An overflow could occur if the remote device violates this rule. Likewise, the UART is not

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allowed to transmit data unless the remote device asserts nCTS low. This feature increases system efficiency and eliminates the possibility of a Receive FIFO Overflow error due to long interrupt latency.

Autoflow mode can be used in two ways: Full autoflow, automating both nCTS and nRTS, and half autoflow, automating only nCTS. Full Autoflow is enabled by writing a 1 to bits 1 and 5 of the Modem Control Register (MCR). Auto-nCTS-Only mode is enabled by writing a 1 to bit 5 and a 0 to bit 1 of the MCR register.

17.4.3.2.4 **RTS (UART Output)**

When in full autoflow mode, nRTS is asserted when the UART FIFO is ready to receive data from the remote transmitter. This occurs when the amount of data in the Receive FIFO is below the programmable threshold value. When the amount of data in the Receive FIFO reaches the programmable threshold, nRTS is de-asserted. It will be asserted once again when enough bytes are removed from the FIFO to lower the data level below the threshold.

17.4.3.2.5 **CTS (UART Input)**

When in Full or Half-Autoflow mode, nCTS is asserted by the remote receiver when the receiver is ready to receive data from the UART. The UART checks nCTS before sending the next byte of data and will not transmit the byte until nCTS is low. If nCTS goes high while the transfer of a byte is in progress, the transmitter will complete this byte. , undefined undefined

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SIO - Pulse Width Modulation (PWM) 17.5

undefined undefined und The Pulse Width Modulation block allows control the frequency and duty cycle of an output signal. The SoC has 2 instances of the PWM interface.

17.5.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- undefined undefined un **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Figure 30. PWM Signals

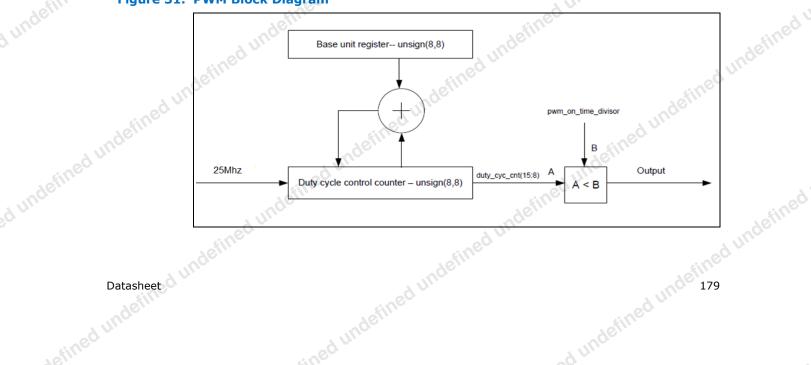
Signal Name	Direction/ Type	ed Unit Description
PWM[0]	I/O/ GPIOMV, MS	Pulse Width Modulation output 0.
PWM[1]	I/O/ GPIOMV, MS	Pulse Width Modulation output 1.
Features		4 under

undefined undefin 17.5.2

Features

The software controls the PWM block by updating the PWMCTRL register and setting the PWMCTRL.PWM SW UPDATE bit whenever a change in frequency or duty cycle of the PWM output signal is required. The PWM block applies the new settings at the start of the next output cycle and resets the PWMCTRL.PWM SW UPDATE bit. The SoC uses 25 MHz for the counter. Refer Figure 31 for PWM block diagram.

Figure 31. PWM Block Diagram



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There are two controls of the PWM output:

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- Frequency is controlled by the PWMCTRL.PWM_BASE_UNIT bits. The PWMCTRL.PWM_BASE_UNIT value is added to a 16 bit counter every clock cycle and the counter roll-over marks the start of a new cycle.
- **Duty cycle** is controlled by the PWMCTRL.PWM ON TIME DIVISOR setting (0 to 255). When the counter rolls-over it is reset and a new cycle starts with the output signal being 0, once the counter reaches the PWMCTRL.PWM ON TIME DIVISOR value the output toggles to 1 and stays high until the counter rolls over.

The PWM block is clocked by the 25 MHz oscillator clock. The output frequency can be estimated with the equation:

Target frequency = 25MHz * base_unit value/256.

NOTE: The larger the value of base unit, the larger the error that the PWM output frequency will have with respect to the equation above. For example any Base_unit_value > 128 will result in 12.5 MHz max frequency. Any value between 86 and 128 will result in 8.33 MHz output frequency. And accordingly the larger the base unit value the smaller duty cycle resolution. Maximum duty cycle resolution is 8 bits.

Table 95 illustrates the output frequency and duty-cycle resolution for different settings of the base_unit_value (when using 25 MHz oscillator clock).

Target Frequency	Base Unit Value	CLK Cycle Count	Duty Cycle Resolution	ined
12.5 MHz	>=128	1 uno	no resolution	detti
1.07 MHz	11	23	<8 bit resolution	dune
488 kHz	5	51	<8 bit resolution	CO
97.6 kHz	1	256	8 resolution	
48.8 kHz	0.5	Theoretically 512 but only 255 available since On Time Divisor is only 8b	>8bit	
0	0 0	0 100	Flat 0 output	

Table 95. **Example PWM Output Frequency and Resolution**

undefined undefined un **Register Map** 17.6

For more information on Serial IO registers refer Intel[®] Atom[™] Z8000 Processor Series undefined undefined undefined undefined undefined Datasheet (Volume 2 of 2), Doc ID:332066. , undefined undefined undefined undefined



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18.1

Platform Controller Unit (PCU) Overview

Platform Controller Unit (PCU) is a collection of HW blocks that are critical for implementing a Windows* compatible platform. These HW blocks include:

- "PCU Power Management Controller (PMC)"
- "PCU Fast Serial Peripheral Interface (SPI)"
 - For boot FW and system configuration data Flash storage
- "PCU Universal Asynchronous Receiver/Transmitter (UART)"
- "PCU Intel Legacy Block (iLB) Overview"

The PCU also implements some high level configuration features for BIOS/EFI boot.

Features

The key features of the individual blocks are as follows:

- Universal Asynchronous Receiver/Transmitter (UART)
 - 16550 controller compliant.
 - Reduced Signal Count: TX and RX only.
 - COM1 interface.
- Fast Serial Peripheral Interface (FST_SPI)
 - For SPI Flash, of up to 16MB size per chip select is supported. No other SPI peripherals are supported.
 - Stores boot FW and system configuration data.
 - Supports frequencies of 20 MHz, 33 MHz and 50 MHz.
- Power Management Controller (PMC)
 - Controls many of the power management features present in the SoC.
- Intel Legacy Block (iLB)
 - Supports legacy PC platform features.
 - Sub-blocks include LPC, GPIO, 8259 PIC, IO-APIC, 8254 timers, HPET timers and the RTC.

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Idefined undefine Platform Controller Unit (PCU) Overview

18.2 **PCU - Power Management Controller (PMC)**

defined undefined undefine Power Management Controller (PMC) controls many of the power management features present in the SoC.

Signal Descriptions 18.2.1 undefined undefined

Refer Chapter 2, "Physical Interfaces" for additional details.

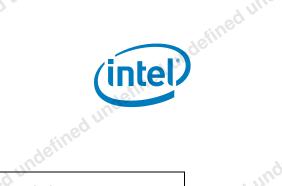
The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 96. PMC Signals (Sheet 1 of 2) undefined undefined

ed un	• Signal Name: The r	name of the	signal/pin.	
define	113		can be either input, output, or I/O (bidirectional).	d unc
711-			Chapter 19, "Electrical Specifications".	stineu
	• Description: A brief	r explanatio	n of the signal's function.	unde
Table 96.	PMC Signals (Sheet 1	of 2)	define	
Leftined L	Signal Name	Direction /Type	Description	
tined unou	PMC_ACPRESENT	I/O/ GPIOMV, MS	AC Present: This input pin indicates when the platform is plugged into AC power.	
under	PMC_BATLOW_N	I/O/ GPIOMV, MS	Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from the S4/S5 state. This signal can also be enabled to cause an SMI_N when asserted. In desktop configurations without a battery, this signal should be tied high to V1P8_S5.	d undefined un
d undefined undefined un	defined under	I/GPIOMV, MS	 Core Power OK: When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for 10 ms. It can be driven asynchronously. When it is negated, the SoC asserts PMC_PLTRST_N. NOTE: It is required that the power rails associated with PCI Express (typically the 3.3V, 5V, and 12V core well rails) have been valid for 99 ms prior to PMC_CORE_PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST_N deassertion. NOTE: PMC_CORE_PWROK must not glitch, even if PMC_RSMRST_N is low. 	ed undefined u
define	afined	I/O/ GPIOMV, MS	Platform Reset: The SoC asserts this signal to reset devices on the platform. The SoC asserts the signal during power-up and when software initiates a hard reset sequence through the Reset Control (RST_CNT) register.	d ^V
182 182 undefined	indefined und		Datashee	hed undefine
182			Datashee	t
ad undern.		undefine	defined b.	
1efine	sine	3 ~	od une	

ned underme Platform Controller Unit (PCU) Overview



	PMC Signals (Sheet 2	of 2)	define	
Die 90.	Signal Name	Direction /Type	Description	defined
ed undef	PMC_PWRBTN_N	I/O/ GPIOMV, MS	Power Button: The signal will cause SMI_N or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If the signal is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.	ndefine
	PMC_RSMRST_N	I/GPIOMV, MS	Resume Well Reset: Used for resetting the resume well. An external RC circuit is required to guarantee that the resume well power is valid prior to this signal going high.	lefine
ed unde	PMC_RSTBTN_N	I/O/ GPIOMV, MS	System Reset: This signal forces an internal reset after being debounced. <i>This signal is muxed and may be used by other functions.</i>	unos
	PMC_SLP_SOIX_N	I/O/ GPIOMV, MS	S0ix Sleep Control: This signal is for power plane control. It can be used to control system power when it is in a S0ix state.	
	PMC_SLP_S4_N	I/O/ GPIOMV, MS	S4 Sleep Control: This signal is for power plane control. It can be used to control system power when it is in a S4 (Suspend to Disk) or S5 (Soft Off) state.	
ined und	PMC_SUS_STAT_N	I/O/ GPIOMV, MS	Suspend Status: This signal is asserted by the SoC to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is muxed and may be used by other functions.	undefin
	PMC_SUSCLK	I/O/ GPIOMV, MS	Suspend Clock: This 32 kHz clock is an output of the RTC generator circuit for use by other chips for refresh clock. This signal is muxed and may be used by other functions.	4 undefin
tined un	PMC_SUSPWRDNACK	I/O/ GPIOMV, MS	Suspend Power Down Acknowledge: Asserted by the SoC when it does not require its Suspend well to be powered. This pin requires a pull-up to UNCORE_V1P8_G3. This signal is muxed and may be used by other functions.	
	idefined undefined i		undefined undefined undefined undefined	ed undefi
isheet o	<u>,</u>	adefined	undefined undefined undefined	33
	ined	UI.	-dunde.	

defined undefined undermeu 2 c ndefined undefined Table 96. PMC Signals (Sheet 2 of 2)

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ndefined undef Platform Controller Unit (PCU) Overview



18.2.2 Features

18.2.2.1 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The GEN_PMCON1.AG3E bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only two possible events that will wake the system after a power failure.

- PMC_PWRBTN_N: PMC_PWRBTN_N is always enabled as a wake event. When RSMRST N is low (G3 state), the PM1 STS EN.PWRBTN STS bit is reset. When the SoC exits G3 after power returns (PMC_RSMRST_N goes high), the PMC PWRBTN N signal is already high (because the suspend plane goes high before PMC RSMRST N goes high) and the PM1 STS EN.PWRBTN STS bit is 0b.
- **RTC Alarm:** The PM1 STS EN.RTC EN bit is in the RTC well and is preserved after a power loss. Like PM1_STS_EN.PWRBTN_STS the PM1_STS_EN.RTC_STS bit is cleared when PMC_RSMRST_N goes low.

The SoC monitors both PMC CORE PWROK and PMC RSMRST N to detect for power failures. If PMC_CORE_PWROK goes low, the GEN_PMCON1.PWR_FLR bit is set. If PMC_RSMRST_N goes low, GEN_PMCON1.SUS_PWR_FLR is set.

Table 97. **Transitions Due to Power Failure**

PMC_RSMRST_N goes lo Transitions Due to Pov	w, GEN_PMCON1.SUS_PW wer Failure	'R_FLR is set.	ined un
State at Power Failure	GEN_PMCON1.AG3E bit	Transition When Power Returns	nden
S0		S5 S0	ed u.
S4		54 50	
S5	nde ¹¹ 0	S5 S0	

Indefined undefined **Event Input Signals and Usage**

ined undefine The SoC has various input signals that trigger specific events. This section describes those signals and how they should be used.

PMC_PWRBTN_N (Power Button) 18.2.2.2.1

The PMC PWRBTN N signal operates as a "Fixed Power Button" as described in the Advanced Configuration and Power Interface specification. The signal has a 16 ms debounce on the input. The state transition descriptions are included in Table 98.

Note:

The transitions start as soon as the PMC_PWRBTN_N is pressed (but after the debounce logic), and does not depend on when the power button is released. imand undefined undefined ut

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Note:

During the time that the PMC_SLP_S4_N signal is stretched for the minimum assertion width (if enabled), the power button is not a wake event. Refer note below for more details.

Table 98. Transitions Due to Power Button

ed unoc	Present State	Event	Transition/Action	Comment
defined undefine	S0/Cx	PMC_PWRBTN_N goes low	SMI_N or SCI generated (depending on PM1_CNT.SCI_EN, PM1_STS_EN.PWRBTN_EN and SMI_EN.GBL_SMI_EN)	Software typically initiates a Sleep state
	S4/S5	PMC_PWRBTN_N goes low	Wake Event. Transitions to S0 state	Standard wakeup
Xe	G3	PMC_PWRBTN_N pressed	None	No effect since no power Not latched nor detected
odefined une	S0, S4	PMC_PWRBTN_N held low for at least 4 consecutive seconds	Unconditional transition to S5 state	No dependence on processor or any other subsystem
Jefined undefines	S0ix	PMC_PWRBTN_N goes low	Wake Event. Transitions to S0 state	PM1_STS_EN.PWRBTN_EN should be set since a SMI/SCI event is required.

Power Button Override Function

If PMC_PWRBTN_N is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the S5 state, regardless of present state (S0–S4), even if the PMC_CORE_PWROK is not active. In this case, the transition to the G2/S5 state should not depend on any particular response from the processor nor any similar dependency from any other subsystem.

The PMC_ PWRBTN_N status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable using the GEN_PMCON2.PWRBTN_LVL bit.

Note:

The 4 seconds PMC_PWRBTN_N assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the SoC is in a S0 state. If the PMC_PWRBTN_N signal is asserted and held active when the system is in a suspend state (S4), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

Note:

During the time that the SLP_S4_N signal is stretched for the minimum assertion width (if enabled by GEN_PMCON1.S4ASE), the power button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the power button waiting for the system to awake. Since a 4 seconds press of the power button is already defined as an unconditional power down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has

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expired, the power button awakes the system. Once the minimum PMC_SLP_S4_N power cycle expires, the power button must be pressed for another 4 to 5 seconds to create the override condition to S5.

18.2.2.2.2 Sleep Button

The Advanced Configuration and Power Interface specification defines an optional sleep button. It differs from the power button in that it only is a request to go from S0 to S4 (not S5). Also, in an S5 state, the power button can wake the system, but the sleep button cannot.

Although the SoC does not include a specific signal designated as a sleep button, one of the GPIO signals can be used to create a "Control Method" sleep button. Refer Advanced Configuration and Power Interface specification for implementation details.

18.2.2.2.3 PME_B0 (PCI Power Management Event Bus 0)

The GPE0a_STS.PME_B0_STS bit exists to implement PME_N-like functionality for any internal device on Bus 0 with PCI power management capabilities.

18.2.2.2.4 PMC_RSTBTN_N Signal

When the PMC_RSTBTN_N pin is detected as active after the 16 ms debounce logic, the SoC attempts to perform a "graceful" reset, by waiting for the relevant internal devices to signal their idleness. If all devices are idle when the pin is detected active, the reset occurs immediately; otherwise, a counter starts. If at any point during the count all devices go idle the reset occurs. If the counter expires and any device is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the PMC_RSTBTN_N input remains asserted or not. It cannot occur again until PMC_RSTBTN_N has been detected inactive after the debounce logic, and the system is back to a full S0 state with PMC_PLTRST_N inactive. Note that if RST_CNT.FULL_RST is set then PMC_RSTBTN_N will result in a full power cycle reset.

18.2.2.3 System Power Planes

The system has several independent power planes, as described in Table 99.

Note:

When a particular power plane is shut off, it should go to a 0 V level.

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Indefined undefined undefin Platform Controller Unit (PCU) Overview



ndefined undefin **System Power Planes** Table 99.

Table 99.	System P	ower Planes	od under	
	Plane	Controlled By	Description	eined
ed unde	Devices and Memory	PMC_SLP_S4_N	When PMC_SLP_S4_N goes active, power can be shut off to any circuit not required to wake the system from the S4/S5. Since the memory context does not need to be preserved in the S4/S5 state, the power to the memory can also be shut down.	nden
define		stined	S4 and S5 requests are treated the same so no PMC_SLP_S5_N signal is implemented.	
ined une	Devices	Implementation Specific	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.	
	Suspend	PMC_SUSPWRDNACK	The suspend power planes are generally left on whenever the system has a charged main battery or is plugged in to AC power.	undefine
odefined und		Lefiner	In some cases, it may be preferable to disable the suspend power planes in S4/S5 states to save additional power. This requires some external logic (such as an embedded controller) to ensure that a wake event is still possible (such as the power button).	
atined un		defined unde	When the SeC is enabled it is advised that the suspend power planes not be removed. Doing so may result in extremely long Sx exit times since the SeC if forced to consider it a cold boot which may, in turn, cause exit latency violations for software using the TXE.	

Power Plane Control with PMC SLP SOIX N and PMC SLP S4 N 18.2.2.3.1

The PMC_SLP_SOIX_N output signal can be used to cut power to any systems supplies that are not required during a S0ix system state.

Cutting power to the core may be done using the power supply, or by external FETs on the motherboard.

The PMC_SLP_S4_N output signal can be used to cut power to the system core supply, ined undefined as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

PMC SLP S4 N and Suspend-To-RAM Sequencing 18.2.2.3.2

The system memory suspend voltage regulator is controlled by the Glue logic. The PMC_SLP_S4_N signal should be used to remove power to system memory. The PMC_SLP_S4_N logic in the SoC provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

undefined und Note:

A undefined undefined undefined To use the minimum DRAM power-down feature that is enabled by the GEN PMCON1.S4ASE bit, the DRAM power must be controlled by the PMC SLP S4 N signal.

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18.2.2.3.3 PMC CORE PWROK Signal

When asserted, PMC CORE PWROK is an indication to the SoC that its core well power rails are powered and stable. PMC_CORE_PWROK can be driven asynchronously. When PMC_CORE_PWROK is low, the SoC asynchronously asserts PMC_PLTRST_N. PMC_CORE_PWROK must not glitch, even if PMC_RSMRST_N is low.

It is required that the power rails associated with PCI Express have been valid for 99 ms prior to PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST_N deassertion.

Note:

PMC RSTBTN N is recommended for implementing the system reset button. This saves external logic that is needed if the PMC CORE PWROK input is used. Additionally, it allows for better handling of the processor resets and avoids improperly reporting power failures.

PMC BATLOW_N (Battery Low) 18.2.2.3.4

The PMC BATLOW N input can inhibit waking from S4, and S5 states if there is not sufficient power. It also causes an SMI if the system is already in an S0 state.

18.2.2.4 SMI_N/SCI Generation

Upon any enabled SMI event taking place while the SMI_EN.EOS bit is set, the SoC will clear the EOS bit and assert SMI to the CPU core, which will cause it to enter SMM space. SMI assertion is performed using a Virtual Legacy Wire (VLW) message. Prior system generations (those based upon legacy processors) used an actual SMI_N pin.

Once the SMI message has been delivered, the SoC takes no action on behalf of active SMI events until Host software sets the End of SMI (EOS) bit. At that point, if any SMI events are still active, the SoC will send another SMI message.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts IRQs[11:9] or IRQs[23:20]. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRO or not. The interrupt remains asserted until all SCI sources are removed.

Table 100 shows which events can cause an SMI and SCI. Note that some events can be programmed to cause either an SMI or SCI. The usage of the event for SCI (instead of SMI) is typically associated with an ACPI-based system. Each SMI or SCI source has a corresponding enable and status bit. undefined undefined undefined

ned underme Platform Controller Unit (PCU) Overview



an undefined undefined undefined Table 100. Causes of SMI and SCI (Sheet 1 of 2)

	oller Unit (PCU) Over	(intel)				
ndefined un Table 100. C		ndefined un			ined une	
Table 100. C	Causes of SMI and	SCI (Sheet 1 of 2)		red une		
	d unob		ndefit	Interru	pt Result	2
Event	Status Indication ¹	Enable Condition		_EN. I_EN=1b		I_EN. I_EN=0b
defined L.		tined und	PM1_CNT .SCI_EN= 1b	PM1_CNT .SCI_EN= 0b	PM1_CNT. SCI_EN= 1b	PM1_CNT. SCI_EN=0 b
Power Button Override ³	PM1_STS_EN. PWRBTNOR_STS	None	SCI	None	SCI	None
RTC Alarm	PM1_STS_EN. RTC_STS	PM1_STS_EN_EN. RTC_EN=1b	SCI	SMI	SCI	None
Power Button Press	PM1_STS_EN. PWRBTN_STS	PM1_STS_EN_EN. PWRBTN_EN=1b	SCI	SMI	SCI	None
SMI_EN.BIOS_RLS bit written to 1b ⁴	PM1_STS_EN. GBL_STS	PM1_STS_EN_EN. GBL_EN=1b	0	S	SCI	stined v
ACPI Timer overflow (2.34 seconds)	PM1_STS_EN. TMROF_STS	PM1_STS_EN_EN. TMROF_EN =1b	SCI	SMI	SCI	None
GPI[n] ⁹	GPE0a_STS. CORE_GPI0_STS[n] ² or GPE0a_STS. SUS_GPI0_STS[n] ²	GPIO_ROUT[n] = 10b & GPE0a_EN. CORE_GPIO_EN[n] ² = 1b or	SCI	None	SCI	None
unde	inec	GPE0a_EN. SUS_GPIO_EN[n] ² =1 b	nedu			stined un
Internal, Bus 0, PME-Capable Agents (PME_B0)	GPE0a_STS. PME_B0_STS	GPE0_EN. PME_B0_EN=1b	SCI	SMI	SCI	None
BATLOW_N pin goes low	GPE0a_STS. BATLOW_STS_N	GPE0_EN. BATLOW_EN=1b	SCI	SMI	SCI	None
Software Generated GPE	GPE0a_STS. SWGPE_STS	GPE0_EN. SWGPE_EN=1b	SCI	SMI	SCI	None
DOSCI message from GUNIT ⁵	GPE0a_STS. GUNIT_STS	None (enabled by G-Unit ⁸)	SCI	None	SCI	None
ASSERT_SMI message from SPI ⁵	SMI_STS. SPI_SMI_STS	None (enabled by SPI controller)	ine s	MI	N	one
ASSERT_IS_SMI message from USB	SMI_STS. USB_IS_STS	SMI_EN. USB_IS_SMI_EN=1b	S	MI	N	one
ASSERT_SMI message from USB	SMI_STS.USB_STS	SMI_EN. USB_SMI_EN=1b		MI	define No	one
ASSERT_SMI message from iLB ⁵	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	S	MI sined U	No	one
Periodic timer expires	SMI_STS. PERIODIC_STS	SMI_EN. PERIODIC_EN=1b		MI	N	one
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ined undefined undefine Platform Controller Unit (PCU) Overview

Table 100. Causes of SMI and SCI (Sheet 2 of 2)

	afined			Interru	pt Result	
Event	Status	Enable Condition		_EN. I_EN=1b		[_EN. I_EN=0b
ed unde	Indication ¹	undefi	PM1_CNT .SCI_EN= 1b	PM1_CNT .SCI_EN= 0b	PM1_CNT. SCI_EN= 1b	PM1_CNT. SCI_EN=0 b
WDT first expiration	SMI_STS.TCO_STS	SMI_EN.TCO_EN=1b	S	MI	N	one
4 ms timer expires	SMI_STS. SWSMI_TMR_STS	SMI_EN. SWSMI_TMR_EN=1b	S	MI	stine N	one
PM1_CNT.SLP_EN bit written to 1b	SMI_STS. SMI_ON_SLP_EN_S TS	SMI_EN. SMI_ON_SLP_EN =1b	Sync	SMI ⁶	N	one
PM1_CNT.GBL_RLS vritten to 1b	SMI_STS.BIOS_STS	SMI_EN. BIOS_EN=1b	Sync	SMI ⁶	N	one
OOSMI message rom GUNIT ⁵	SMI_STS. GUNIT_SMI_STS	None (enabled by G-Unit ⁸)	S	MI	N	one
SSERT_IS_SMI nessage from iLB ⁵	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	Sync	SMI ⁷	ed N	one
GPI[n] ¹⁰	ALT_GPIO_SMI. CORE_GPIO_SMI_S TS[n] ² or ALT_GPIO_SMI. SUS_GPIO_SMI_ST S[n] ²	GPIO_ROUT[n]=01b & ALT_GPIO_SMI. CORE_GPIO_SMI_EN [n] ² =1b or ALT_GPIO_SMI. SUS_GPIO_SMI_EN[n] ² =1b	sined und	MI Lefined un	Setter N	one
JSB Per-Port Registers Write Enable bit is Changed from 0b to D	UPRWC.WE_STS & SMI_STS. USB_IS_STS	UPRWC. WE_SMI_E=1b & SMI_EN. USB_IS_SMI_EN=1b	Sync	SMI ⁶	defined	one

NOTES:

- 1. Most of the status bits (except otherwise is noted) are set according to event occurrence regardless to the enable bit.
- 2. GPIO status bits are set only if enable criteria is true. GPIO_ROUT[n]=10b & GPE0a EN.x GPIO EN[n] for GPE0a STS.x GPIO STS[n] (SCI). GPIO ROUT[n]=01b & ALT_GPIO_SMI. x_GPIO_SMI_EN[n]=1b for ALT_GPIO_SMI.x_GPIO_SMI_STS[n] (SMI).
- 3. When power button override occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PM1 STS EN.PWRBTNOR STS) is not cleared prior to setting PM1 CNT.SCI EN.
- 4. PM1_STS_EN.GBL_STS being set will cause an SCI, even if the PM1_CNT.SCI_EN bit is not set. Software must take great care not to set the SMI_ENBIOS_RLS bit (which causes PM1_STS_EN.GBL_STS to be set) if the SCI handler is not in place.
- 5. No enable bits for these SCI/SMI messages in the PMC. Enable capability should be implemented in the source unit.
- Atined undefined 6. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync veriment undefined undef SMI is holding completion to host till SYNC_SMI_ACK message is received from T-Unit. indefined undefi



- 7. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding the SSMI ACK message to iLB till SYNC SMI ACK message is received from T-Unit.
- 8. The G-Unit is an internal functional sub-block which forms part of the graphics functional block.
- 9. The GPE0a_STS.CORE_GPI0_STS[31:24] & GPE0a_EN.CORE_GPI0_EN[31:24] register bits correspond to GPIO S0 SC[7:0]. GPE0a STS.SUS GPIO STS[23:16] & GPE0a_EN.SUS_GPIO_EN[23:16] correspond to GPIO_S5[7:0].
- 10. The ALT_GPIO_SMI.CORE_GPIO_SMI_STS[31:24] &
- ALT GPIO SMI.CORE GPIO SMI EN[15:8] register bits correspond to GPIO S0 SC[7:0]. ALT_GPIO_SMI.SUS_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI.SUS_GPIO_SMI_EN[7:0] correspond to GPIO_S5[7:0].

fined undefined 18.2.2.5 **Platform Clock Support**

,d undefined The SoC supports up to 6 clocks (PMC_PLT_CLK[5:0]) with a frequency of 19.2 MHz. These clocks are available for general system use, where appropriate and each have Control and Frequency register fields associated with them.

18.2.2.6 INIT_N (Initialization) Generation

The INIT_N functionality is implemented as a 'virtual wire' internal to the SoC rather than a discrete signal. This virtual wire is asserted based on any one of the events described in below table. When any of these events occur, INIT N is asserted for 16 PCI clocks and then driven high.

stined undefined undefined INIT_N, when asserted, resets integer registers inside the CPU cores without affecting its internal caches or floating-point registers. The cores then begin execution at the power on Reset vector configured during power on configuration.

Table 101. INIT_N Assertion Causes

Cause
PORT92.INIT_NOW transitions from 0b to1b.
RST_CNT.SYS_RST = 0b and RST_CNT.RST_CPU transitions from 0b to 1b

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Note:

18.3 **PCU - Fast Serial Peripheral Interface (SPI)**

The SoC implements a SPI controller as the interface for BIOS Flash storage. This SPI Flash device is also required to support configuration storage for the firmware for the Trusted Execution Engine. The controller supports a maximum of two SPI Flash devices, using two chip select signals, with speeds of 14.28 MHz, 20 MHz, 25 MHz, 40 MHz or 50 MHz and both have to be Fast SPI. SoC Supports FAST SPI mode.

The default interface speed is 20 MHz.

SPI 'Fast mode' is guad mode.

Signal Descriptions 18.3.1

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

ndefined undef Table 102. SPI Signals

Signal Name	Direction /Type	Description	indefine
FST_SPI_CLK	I/O GPIO	Fast SPI Clock: When the bus is idle, the owner will drive the clock signal low.	
FST_SPI_CS[0]_N	I/O GPIO	Fast SPI Chip Select 0: Used as the SPI bus request signal for the first SPI Flash device.	
FST_SPI_CS[1]_N	I/O GPIO	Fast SPI Chip Select 1: Used as the SPI bus request signal for the second SPI Flash devices.	
FST_SPI_CS[2]_N	I/O GPIO	Fast SPI Chip Select 2: Used as the SPI bus request signal for the second SPI Flash devices.	
FST_SPI_D[3:0]	I/O GPIO	Fast SPI Data Pad: Data Input/output pin for the SoC.	undefill

Note:

18.3.2

red undefined undef All SPI signals are tri-stated when PMC RSMRST N and PMC CORE PWROK are asserted. FST_SPI_CS[0:2] and FST_SPI_CLK are not tri-stated.

Features

- 1) Descriptor Mode Capabilities
 - a)Two modes of operation
 - i)Descriptor mode with security access restrictions



ii)Non-Descriptor mode, no access security restrictions (ICH7 style)

- (1)BIOS Only
- (2)If the SPI Flash Signature is invalid, the SPI flash operates in nondescriptor mode
- a. Supports Flash that is divided into 5 regions and accessible by 3 masters
 - i)Regions (5)
 - (1) Flash Descriptor and Chipset Soft Straps
 - (2) BIOS
 - (3) TXE
 - (4) Platform Data
 - ii)Masters (3)
 - (1) Host CPU (for BIOS)
 - (2) TXE

iii)Regions are allowed to extend across multiple Flash components

iv)Regions are aligned to 4K blocks/sectors

b. Chipset Soft Strap region provides the ability to use Flash NVM as an alternative to hardware pullup/pulldown resistors for both SoC and the processor Complex

i)Each Unit that pulls Soft straps from SPI should have a default value that is used if the Flash Signature is invalid.

- c. The top of the Flash Descriptor contains the Flash Upper Map
- ii)This is used by software to define Flash vendor specific capabilities d. The top 256B of the flash descriptor is reserved for use by the OEM
- 2)Security Capabilities
 - Descriptor based Region Restriction: Hardware enforced security restricting master accesses to different regions
 - i)Flash Descriptor region settings define separate read/write access to each region per master.
 - ii)Uses SAI for master accesses security checking
 - (1)Soft Strap+fuse to disable sourceID and SAI checks

iii)Flash Security Override Pin Strap

(1)Removes all descriptor based security

- (2)Disables the write protection to the BIOS Protected Range 4 (PR4).
- iv)Each master can grant other masters read/write access to its region
- b. Protected Range Registers.
 - i)3 sets (one for each master) of Lockable Protected Range registers that can restrict program register accesses from the same master.ii)Can span multiple regions
 - ii)Can span multiple regions

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iii)Separate read and write protection

- iv)Special case: BIOS PR4 write protect values are received from Soft Strap and affect all masters.
- c. SMI Write Protection for BIOS
 - i)If enabled, will cause an SMI if a program register access occurs. The primary purpose of this requirement is to support SMI based BIOS update utilities.
- d. Illegal Instruction protection for instructions such as Chip Erase
- e. Lockable software sequencing opcodes
- 3)SPI Flash Access
 - a. Direct Read Access
 - b. Program Register Access
 - i)Hardware Sequencing
 - (1)Software Sequencing uses HW to provide the basic instructions of read, write, and erase.
 - ii)Software Sequencing

(1)Allows SW to use any legal Opcode

c. Support for Boot BIOS on SPI.

i)Non-boot BIOS that is accessible through program register only can be used on SPI when boot BIOS is located on some other interface.

d. Pre-fetching/Caching to improve performance

i)Separate 64B pre-fetch/cache each for HOST and SEC direct read accesses

4)SFDP Parameter Discoverability¹

- 5)Flash Component Capabilities
 - a. In Descriptor mode, supports two SPI Flash components using two separate chip select pins, CS0# and CS1#. Only one component supported in non-descriptor mode.

i)Components must have the same erasable block/sector size

- ii)Each component can be up to 16MB (32MB total addressable) using 24-bit addressing.
- b. 1.8V SPI I/O buffer VCC
- c. Supports the SPI Fast Read/Write instruction and frequencies of 20MHz, 33MHz and 50 MHz. Supports the SPI Dual Output Fast Read/Write instruction with frequencies of 20 MHz, 33 MHz and 50 MHz
- d. Supports the SPI Quad Output Fast Read/Write instruction with frequencies of 20 MHz, 33 MHz and 50 MHz
- e. Uses standardized Flash Instruction Set.
- f. Supports non-power of 2 flash sizes, with the following restrictions:



i)Only supported in Descriptor Mode.

- ii)BIOS accesses in non-descriptor mode to a non-binary flash size will not function properly.
- iii)The Flash Regions must be programmed to the actual size of the Flash Component(s).
- iv)If using two flash components, the 1st flash component (the one with the Flash Descriptor) must be of binary size. The 2nd flash component can be a non-binary size. If using only one flash component, it can be of non-binary size.
- v)The value programmed in the Flash Descriptor Component Density must be set to the next power of 2 value larger than the non-binary size.
- 8)Reset Capabilities
 - a. RSMRST#
 - i)When RSMRST# is asserted, SoC will tri-state with a weak pull-up all SPI pins
 - i)The SPI Controller will implement a sideband handshake((handshake is reset warn message)) with PMC when a host reset is requested to allow the SPI Flash controller to complete any outstanding atomic sequences and quiescence the SPI Bus

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18.4

PCU - Universal Asynchronous Receiver/ Transmitter (UART)

This section describes the Universal Asynchronous Receiver/Transmitter (UART) serial port integrated into the PCU. The UART may be controlled through programmed IO.

Note:

Only a minimal ball-count, comprising receive & transmit signals, UART port is implemented. Further, a maximum baud rate of only 115,200 bps is supported. For this reason, it is recommended that the UART port be used for debug purposes only.

18.4.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function.

Table 103. UART Signals

Signal Name	Direction /Type	Description
UARTO_DATAIN	I/GPIOHV, HS	COM1 Receive: Serial data input from device pin to the receive port. This signal is muxed and may be used by other functions.
UARTO_DATAOU T	O/GPIOHV, HS	COM1 Transmit: Serial data output from transmit port to the device pin. <i>This signal is muxed and may be used by other functions.</i>

18.4.2 Features

The serial port consists of a UART which supports a subset of the functions of the 16550 industry standard.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the processor. The processor may read the complete status of the UART at any time during the functional operation. Available status information includes the type and condition of the transfer operations being performed by the UART and any error conditions.

The serial port may operate in either FIFO or non-FIFO mode. In FIFO mode, a 16-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 16-byte Receive FIFO buffers data from the serial link until read by the processor.



led undefined und The UART includes a programmable baud rate generator which is capable of generating a baud rate of between 50 bps and 115,200 bps from a fixed baud clock input of 1.8432 MHz. The baud rate is calculated as follows:

Baud Rate Calculation:

BaudRate = $\frac{1.8432 \times 10^{4}}{100}$ 16 × Divisor

The divisor is defined by the Divisor Latch LSB and Divisor Latch MSB registers. Some common values are shown in Table 104.

ined undefined und Table 104. Baud Rate Examples

Table 104. Baud Rate	Examples	. u		
Desired Baud Rate	Divisor	Divisor Latch LSB Register	Divisor Latch MSB Register	untined und
115,200	1	1h	Oh	nder
57,600	2	2h	0h	
38,400	3	3h	Oh	1
19,200	6 du	6h	Oh	1
9,600	12	Ch	O Oh	-
4,800	24	18h	Oh	-
2,400	48	30h	0h	27.
1,200	96	60h	Oh	un un un
300	384	80h	1h	1 etine
50 aneo	2,304	Oh	9h	unor

The UART has interrupt support and those interrupts may be programmed to the user's requirements, minimizing the computing required to handle the communications link. Each UART may operate in a polled or an interrupt driven environment as configured by software.

18.4.2.1 **FIFO Operation**

18.4.2.1.1 **FIFO Interrupt Mode Operation**

Receiver Interrupt

When the Receive FIFO and receiver interrupts are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register (IIR), bit 0 = 1b), receiver interrupts occur as follows:

 The receive data available interrupt is invoked when the FIFO has reached its programmed trigger level. The interrupt is cleared when the FIFO drops below the programmed trigger level. in a undefined undefined unde

- The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, the bits are cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR = C6h), as before, has the highest priority. The receiver data available interrupt (IIR = C4h) is lower. The line status interrupt occurs only when the character at the top of the FIFO has errors.
- The COM1_LSR.DR bit is set to 1b as soon as a character is transferred from the shift register to the Receive FIFO. This bit is reset to 0b when the FIFO is empty.

Character Time Out Interrupt

intel) ed und

When the receiver FIFO and receiver time out interrupt are enabled, a character time out interrupt occurs when all of the following conditions exist:

- At least one character is in the FIFO.
- The last received character was longer than four continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- The most recent processor read of the FIFO was longer than four continuous character times ago.
- The receiver FIFO trigger level is greater than one.

The maximum time between a received character and a timeout interrupt is 160 ms at 300 baud with a 12-bit receive character (i.e., 1 start, 8 data, 1 parity, and 2 stop bits).

When a time out interrupt occurs, it is cleared and the timer is reset when the processor reads one character from the receiver FIFO. If a time out interrupt has not occurred, the time out timer is reset after a new character is received or after the processor reads the receiver FIFO.

Transmit Interrupt

When the transmitter FIFO and transmitter interrupt are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register, bit 0 = 1b), transmit interrupts occur as follows:

The Transmit Data Request interrupt occurs when the transmit FIFO is half empty or more than half empty. The interrupt is cleared as soon as the Transmit Holding Register is written (1 to 16 characters may be written to the transmit FIFO while servicing the interrupt) or the Interrupt Identification Register is read.

18.4.2.1.2 FIFO Polled Mode Operation

With the FIFOs enabled (FIFO Control register, bit 0 = 1b), setting Interrupt Enable register (IER), bits 3:0 = 000b puts the serial port in the FIFO polled mode of operation. Since the receiver and the transmitter are controlled separately, either one or both may be in the polled mode of operation. In this mode, software checks receiver and transmitter status through the Line Status Register (LSR). As stated in the register description:

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- LSR[0] is set as long as there is one byte in the receiver FIFO.
- LSR[1] through LSR[4] specify which error(s) has occurred for the character at the top of the FIFO. Character error status is handled the same way as interrupt mode. The Interrupt Identification Register is not affected since IER[2] = 0b.
- LSR[5] indicates when the transmitter FIFO needs data.
- LSR[6] indicates that both the transmitter FIFO and shift register are empty.
- LSR[7] indicates whether there are any errors in the receiver FIFO.

18.4.3 Use

18.4.3.1 Base I/O Address

COM1

The base I/O address for the COM1 UART is fixed to 3F8h.

18.4.3.2 Legacy Interrupt

COM1

The legacy interrupt assigned to the COM1 UART is fixed to IRQ4.

18.4.4 UART Enable/Disable

The COM1 UART may be enabled or disabled using the UART_CONT.COM1EN register bit. By default, the UART is disabled.

Note:

It is recommended that the UART be disabled during normal platform operation. An enabled UART can interfere with platform power management.

18.4.5 IO Mapped Registers

There are 12 registers associated with the UART. These registers share eight address locations in the IO address space. Table 105 shows the registers and their addresses as offsets of a base address. Note that the state of the COM1_LCR.DLAB register bit, which is the most significant bit (MSB) of the Serial Line Control register, affects the selection of certain of the UART registers. The COM1_LCR.DLAB register bit must be set high by the system software to access the Baud Rate Generator Divisor Latches.

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18.5

Table 105. Register Access List

9er.		indefine			defined	sined un-
Ć	intel	hed undefine	6	undefin	Platform Controller Unit (PCU) Overvio	unden
defined under	8.5	Register Ma	ap undefine		undefined	
nder. 1	Table 105.	Register Access	s List		sineo	ed un
		Register Address (Offset to Base IO Address)	COM1_LCR.DLA B Value	Register Access Type	Register Accessed	undefine
	ind	0h	0b	RO	Receiver Buffer ¹	<u>.</u>
sined unde		0h	0b	wo	Transmitter Holding ¹	
	in	0h	1b	RW	Divisor Latch LSB (Lowest Significant Bit) ¹	_
, unos		1h	0b	RW	Interrupt Enable ²	_
ed		1h	1b	RW	Divisor Latch MSB (Most Significant Bit) ²	_
4efil.		2h	xb	RO	Interrupt Identification ³	<u>اں .</u>
		2h	xb	WO	FIFO Control ³	the o
		3h	xb	RW	Line Control	det li
		4h	xb	RW	Modem Control ⁴	unc
		5h	xb	RO	Line Status	3.0
	dui	6h	xb	RO	Modem Status ⁴	_
. /		7h	xb	RW	Scratchpad	_
undefined unde		NOTES: 1. These registers (COM1_RX_TX_ 2. These registers 3. These registers (COM1_IIR).	_BUFFER). are consolidated i	n the Inter	river Buffer / Transmitter Holding Register rrupt Enable Register (COM1_IER) rrupt Identification / FIFO Control Register	-tined U

NOTES:

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- Jee



PCU - Intel Legacy Block (iLB) Overview 18.6

, undefined undefined unt The Intel Legacy Block (iLB) is a collection of disparate functional blocks that are critical for implementing the legacy PC platform features. These blocks include:

- PCU iLB Low Pin Count (LPC) Bridge"
- "PCU iLB Real Time Clock (RTC)"
- "PCU iLB 8254 Timers"
- "PCU iLB High Precision Event Timer (HPET)"
- "PCU iLB GPIO"
- "PCU iLB IO APIC"
- "PCU iLB 8259 Programmable Interrupt Controllers (PIC)"

ed undefined The iLB also implements a register range for configuration of some of those blocks along with support for Non-Maskable Interrupts (NMI).

18.6.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details as well as the subsequent sections.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 106. iLB Signals

• Iype: The b	uffer type fo	ound in Chapter 19, "Electrical Specifications".
• Description	: A brief ex	planation of the signal's function.
LB Signals		tined u.
Signal Name	Direction /Type	Description
NMI_N	I/GPIOMV, MS	Non-Maskable Interrupt: This is an NMI event indication into the SoC.
d UI		This signal is muxed and may be used by other functions.
Features		defined
Key Features		ed under under
The key features	of various	blocks are as follows:

18.6.2 Features

18.6.2.1

Key Features

The key features of various blocks are as follows:

- LPC Interface
 - Supports Low Pin Count (LPC) 1.1 Specification
 - No support for DMA or bus mastering
 - Supports Trusted Platform Module (TPM) 1.2

Idefined undefin Platform Controller Unit (PCU) Overview



- General Purpose Input Output •
 - Legacy control interface for SoC GPIOs
 - I/O mapped registers
- 8259 Programmable Interrupt Controller
- Supports Legacy interrupt
- etined undefined undefined undefined undefined undefined - 15 total interrupts through two cascaded controllers
- I/O mapped registers
- I/O Advanced Programmable Interrupt Controller
 - Supports Legacy-free interrupt
 - 115 total interrupts
 - Memory mapped registers
- 8254
 - Legacy timer support
 - Three timers with fixed uses: System Timer, Refresh Request Signal and Speaker Tone
 - I/O mapped registers
- HPET High Performance Event Timers
 - Supports Legacy-free timer
 - Three timers and one counter
 - Memory mapped registers
- Real-Time Clock (RTC)
 - 242 byte RAM backed by battery (aka CMOS RAM)
 - Can generate wake/interrupt when time matches programmed value
 - I/O and indexed registers

18.6.2.2 **Non-Maskable Interrupt**

NMI support is enabled by setting the NMI Enable (NMI_EN) bit, at IO Port 70h, Bit 7, to 1b.

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in .cri < Table 107.

Datasheet

undefined undefined undefined Platform Controller Unit (PCU) Overview



ndefined undefin Table 107. NMI Sources

ed undefined t	undefined u			Jefined und	
Table 107	. NMI Sources		d un		, unor
no	NMI Source	NMI Source Enabler/ Disabler	NMI Source Status	Alternate Configuration	ndefined
ed und	SERR# goes active NOTE: A SERR# is only generated internally in the SoC)	NSC.SNE	NSC.SNS	All NMI sources may, alternatively, generate a SMI by setting	
d undefine	IOCHK# goes active NOTE: A IOCHK# is only generated as a SERIRQ# frame	NSC.INE	NSC.INS	GNMI.NMI2SMIEN=1b	
undefinec	NMI goes active NOTE: Active can be defined as being on the positive or negative edge of the signal using the GNMI.GNMIED register bit.	GNMI.GNMIED	GNMI.GNMIS	GNMI.NMI2SMIST for observing SMI status	Indefined und
d und	Software sets the GNMI.NMIN register bit	GNMI.NMIN	GNMI.NMINS	defineo	
18.6.2.3	S0ix Support	<u>v</u>		dunc	-

ed unde 18.6.2.3 **S0ix Support**

There is no requirement to set "HPET_GCFG.EN" to 0b. Basically turn off HPET during S0i2/3. RTD3hot status is not a key requirement for OS anymore.

stined undefined The S1 state described in the HPET spec is a "CPU Stop Grant" condition. This condition is met during the S0i2/3 states, (although entry into S0i2/3 is performed in a different way).

18.6.3 V Use

18.6.3.1

S0ix Support

undefined undefi Prior to entry into S0i2 or S0i3 state, the driver/OS must set HPET_GCFG.EN to 0b to Jahundefined undefined undefined undefined Datasheet indicate RTD3hot status.

undefi

Jeffined undefin Platform Controller Unit (PCU) Overview



18.7 PCU - iLB - Low Pin Count (LPC) Bridge

The SoC implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the SoC resides in PCI Device 31, Function 0.

Note:

In addition to the LPC bridge interface function, D31:F0 contains other functional units including interrupt controllers, timers, power management, system management, GPIO, and RTC.

18.7.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 108. LPC Signals

atined	Signal Name	Direction/	Description	
	LPC_AD[3:0]	I/O/ GPIOHV, HS	LPC Multiplexed Command, Address, Data: Internal pull-ups are provided for these signals. <i>These signals are muxed and may be used by other functions.</i>	undefine
	LPC_CLKOUT[0]	I/O/ GPIOHV, HS	LPC Clock [0] Out: 19MHz PCI-like clock driven to LPC peripherals. These signals are muxed and may be used by other functions.	9.0.
-01	LPC_CLKOUT[1]	I/O/ GPIOHV, HS	LPC Clock [1] Out: 19MHz PCI-like clock driven to LPC peripherals. Can be configured as an input to compensate for board routing delays through Soft Strap. <i>These signals are muxed and may be used by other functions.</i>	
define	LPC_CLKRUN_N	I/O/ GPIOHV, HS	LPC Clock Run: Input to determine the status of LPC_CLK and an open drain output used to request starting or speeding up LPC_CLK. This is a sustained tri-state signal used by the central resource to request permission to stop or slow LPC_CLK. The central resource is responsible for maintaining the signal in the asserted state when LPC_CLK is running and deasserts the signal to request permission to stop or slow LPC_CLK. An internal pull-up is provided for this signal. <i>This signal is muxed and may be used by other functions.</i>	ed undefine
	LPC_FRAME_N	I/O/ GPIOHV, HS	LPC Frame: This signal indicates the start of an LPC cycle, or an abort. <i>This signal is muxed and may be used by other functions.</i>	
ndefined	LPC_SERIRQ	I/O/ GPIOHV, HS	Serial Interrupt Request: This signal implements the serial interrupt protocol. <i>This signal is muxed and may be used by other functions.</i> NOTE: A level shifter needs to be implemented on this signal.	
	204 ad undef	ined u.	Datashee	hed undern.

ndefined undefined Platform Controller Unit (PCU) Overview



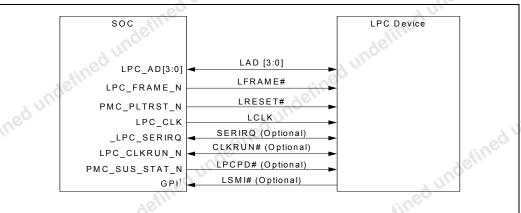
18.7.2 **Features**

The LPC interface to the SoC is shown in Figure 32. Note that the SoC implements all of the signals that are shown as optional, but peripherals are not required to do so.

Note:

The LPC controller does not implement bus mastering cycles or DMA.





NOTE: The General Purpose Input (GPI) must use a SMI capable GPIO: GPIO S0 SC[7:0].

indefined undefined unde **Memory Cycle Notes**

For cycles below 16M, the LPC Controller will perform standard LPC memory cycles. For cycles targeting firmware (BIOS/EFI code only), firmware memory cycles are used. Only 8-bit transfers are performed. If a larger transfer appears, the LPC controller will break it into multiple 8-bit transfers until the request is satisfied.

If the cycle is not claimed by any peripheral (and subsequently aborted), the LPC Controller will return a value of all 1's to the CPU.

18.7.2.2 Trusted Platform Module (TPM) 1.2 Support

The LPC interface supports accessing Trusted Platform Module (TPM) 1.2 devices via the LPC TPM START encoding. Memory addresses within the range FED00000h to FED40FFFh will be accepted by the LPC Bridge and sent on LPC as TPM special cycles. No additional checking of the memory cycle is performed.

Note:

This is different to the FED00000h to FED4BFFFh range implemented on some other Intel components since no Intel[®] Trusted Execution Technology (Intel[®] TXT) transactions are supported.

18.7.2.3 FWH Cycle Notes

If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.

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BIOS/EFI boot from LPC is not supported when Secure Boot is enabled.

18.7.2.4 Subtractive Decode

All cycles that are not decoded internally, and are not targeted for LPC (i.e., configuration cycles, IO cycles above 64KB and memory cycles above 16MB), will be sent to LPC with LPC_FRAME_N not asserted.

18.7.2.5 POST Code Redirection

Writes to addresses 80h - 8Fh in IO register space will also be passed to the LPC bus.

Note: Reads of these addresses do not result in any LPC transactions.

18.7.2.6 Power Management

18.7.2.6.1 LPCPD_N Protocol

Same timings as for PMC_SUS_STAT_N. After driving PMC_SUS_STAT_N active, the SoC drives LPC_FRAME_N low, and tri-states (or drives low) LPC_AD[3:0].

Note:

The Low Pin Count Interface Specification, Revision 1.1 defines the LPCPD_N protocol where there is at least 30 µs from LPCPD_N assertion to LRST_N assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The SoC asserts both PMC_SUS_STAT_N (connects to LPCPD_N) and PLTRST_N (connects to LRST_N) at the same time during a global reset. This is not inconsistent with the LPC LPCPD_N protocol.

18.7.2.6.2 Clock Run (CLKRUN)

When there are no pending LPC cycles, and SERIRQ is in quiet mode, the SoC can shut down the LPC clock. The SoC indicates that the LPC clock is going to shut down by deasserting the LPC_CLKRUN_N signal. LPC devices that require the clock to stay running should drive LPC_CLKRUN_N_N low within 4 clocks of its de-assertion. If no device drives the signal low within 4 clocks, the LPC clock will stop. If a device asserts LPC_CLKRUN_N, the SoC will start the LPC clock and assert LPC_CLKRUN_N.

Note:

The CLKRUN protocol is disabled by default. Refer Section 18.7.3.2.2, "Clock Run Enable" for further details.

18.7.2.7 Serialized IRQ (SERIRQ)

The interrupt controller supports a serial IRQ scheme. The signal used to transmit this information is shared between the interrupt controller and all peripherals that support serial interrupts. The signal line, LPC_SERIRQ, is synchronous to LPC clock, and follows the sustained tri-state protocol that is used by LPC signals. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

• S - Sample Phase: Signal driven low.

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- R Recovery Phase: Signal driven high.
- Turn-around Phase: Signal released.

The interrupt controller supports 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0- 1, 3-15), the four PCI interrupts, and the control signals SMI_N and IOCHK_N. Serial interrupt information is transferred using three types of frames:

- Start Frame: LPC SERIRQ line driven low by the interrupt controller to indicate the start of IRQ transmission.
- Data Frames: IRQ information transmitted by peripherals. The interrupt controller supports 21 data frames.
- Stop Frame: LPC_SERIRQ line driven low by the interrupt controller to indicate end of transmission and next mode of operation.

Start Frame 18.7.2.7.1

The serial IRQ protocol has two modes of operation which affect the start frame:

- Continuous Mode: The interrupt controller is solely responsible for generating the start frame.
- Quiet Mode: Peripheral initiates the start frame, and the interrupt controller completes it.

These modes are entered via the length of the stop frame.

Continuous mode must be entered first, to start the first frame. This start frame width is 8 LPC clocks. This is a polling mode.

In Quiet mode, the LPC SERIRO line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives LPC_SERIRQ low. The interrupt controller senses the line low and drives it low for the remainder of the Start Frame. Since the first LPC clock of the start frame was driven by the peripheral, the interrupt controller drives LPC SERIRO low for 1 LPC clock less than in continuous mode. This mode of operation allows for lower power operation.

18.7.2.7.2 **Data Frames**

Once the Start frame has been initiated, the LPC_SERIRQ peripherals start counting frames based on the rising edge of LPC_SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase:** During this phase, a device drives LPC_SERIRQ low if its corresponding interrupt signal is low. If its corresponding interrupt is high, then the LPC_SERIRQ devices tri-state LPC_SERIRQ. LPC_SERIRQ remains high due to pullup resistors.
- Recovery Phase: During this phase, a device drives LPC SERIRQ high if it was red undefinet driven low during the Sample Phase. If it was not driven during the sample phase, it remains tri-stated in this phase.
- Turn-around Phase: The device tri-states LPC_SERIRQ.

, undefined undefi Platform Controller Unit (PCU) Overview



18.7.2.7.3 **Stop Frame**

defined undefined und After the data frames, a Stop Frame will be driven by the interrupt controller. LPC_SERIRQ will be driven low for two or three LPC clocks. The number of clocks is determined by the SCNT.MD register bit. The number of clocks determines the next mode, as indicated in Table 109.

Table 109. SERIRQ, Stop Frame Width to Operation Mode Mapping

Stop Frame Width	Next Mode
Two LPC clocks	Quiet Mode: Any SERIRQ device initiates a Start Frame
Three LPC clocks	Continuous Mode: Only the interrupt controller initiates a Start Frame

18.7.2.7.4 **Serial Interrupts Not Supported**

There are four interrupts on the serial stream which are not supported by the interrupt controller. These interrupts are:

- IRQ0: Heartbeat interrupt generated off of the internal 8254 counter 0
- IRQ8: RTC interrupt can only be generated internally.
- IRQ13: This interrupt (floating point error) is not supported.

The interrupt controller will ignore the state of these interrupts in the stream.

undefined undefine 18.7.2.7.5 **Data Frame Format and Issues**

Table below shows the format of the data frames. The decoded INT[A:D]_N values are ANDed with the corresponding PCI-express input signals (PIRQ[A:D]_N). This way, the interrupt can be shared.

The other interrupts decoded via SERIRQ are also ANDed with the corresponding internal interrupts. For example, if IRQ10 is set to be used as the SCI, then it is ANDed with the decoded value for IRQ10 from the SERIRQ stream.

Table 110. SERIRO Interrupt Mapping

Undefinet. Table 110. S) from the SERIRQ stream.	ed u
	Data Frame #	Interrupt	Clocks Past Start Frame	Comment	ed undefilte
d ^v	1	IRQ0	2	Ignored. Can only be generated via the internal 8524	
atines	2	IRQ1	5	Before port 60h latch	
indefined undefines	3	SMI_N	8 defi	Causes SMI_N if low. Sets SMI_STS.ILB_SMI_STS register bit.	
stine	4	IRQ3	0 11	4 un	1
inde	5	IRQ4	14	filler	, be
<u>,</u> d	6	IRQ5	17	nder	1efine
208 undefined l	Indefine		d undef	Ined undefined Datashee	ned unos
1 Still-		65	neu	d ^{UI}	



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Data Frame #	Interrupt	Clocks Past Start Frame	Comment	lefine
7	IRQ6	20	ed un	100
8	IRQ7	23	18tine aneo	
9	IRQ8	26	Ignored. IRQ8_N can only be generated internally	
10	IRQ9	29	dum	
11	IRQ10	32	sines	
12	IRQ11	35	nder	
13	IRQ12	38	Before port 60h latch	
14	IRQ13	41	Ignored.	
15	IRQ14	44	Ignored	dein
16	IRQ15	47	ine ⁰	NU-
17	IOCHCK_N	50	Same as ISA IOCHCK_N going active.	
18	PCI INTA_N	53	um.	
19	PCI INTB_N	56	definec	
20	PCI INTC_N	59	redun]
21	PCI INTD_N	62	dem	ii)

Table 110. SERIRQ Interrupt Mapping

18.7.2.7.6 S0ix Support

During S0i2 and S0i3, the LPC and SERIRQ interfaces are disabled.

18.7.3 Usage

LPC Clock Delay Compensation 18.7.3.1

In order to meet LPC interface AC timing requirements, a LPC clock loop back is required. The operation of this loop back can be configured in two ways:

1. On the SOC: In this configuration, LPC_CLK[0] is looped back on itself on the SOC pad.

a. Benefit:

LPC_CLK[0] and LPC_CLK[1] are both available for system clocking

b. Drawback:

A undefined undefined undefined Clock delay compensation is less effective at compensating for mainboard delay

c. Soft Strap & Register Requirements: in a sum defined undefined ur

Soft Strap LPCCLK_SLC = 0b

Configuration is reflected by register bit LPCC.LPCCLK_SLC=0b

Soft Strap LPCCLK1_ENB = 0b (LPC_CLK[1] disabled) or 1b (LPC_CLK[1] enabled)

- Configuration is reflected by register bit LPCC.LPCCLK1EN=0b (LPC_CLK[1] disabled) or 1b (LPC_CLK[1] enabled)
- On the main board: In this configuration, LPC_CLK[0] is looped back to LPC_CLK[1] on the main board.
 - a. Benefit:

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Clock delay compensating in more effective at compensating for main board delay

b. Drawback:

Only LPC_CLK[0] is available for system clocking. LPC_CLK[1] must be disabled.

c. Soft Strap & Register Requirements:

Soft Strap LPCCLK_SLC = 1b

Configuration is reflected by register bit LPCC.LPCCLK_SLC=1b

Soft Strap LPCCLK1_ENB = 0b (LPC_CLK[1] disabled)

Configuration is reflected by register bit LPCC.LPCCLK1EN=0b

18.7.3.2 LPC Power Management

18.7.3.2.1 Clock Enabling

The LPC clocks can be enabled or disabled by setting or clearing, respectively, the LPCC.LPCCLK[1:0]EN bits.

18.7.3.2.2 Clock Run Enable

The Clock Run protocol is disabled by default and should only be enabled during operating system run-time, once all LPC devices have been initialized. The Clock Run protocol is enabled by setting the LPCC.CLKRUN_EN register bit.

18.7.3.3 SERIRQ Disable

Serialized IRQ support may be disabled by setting the OIC.SIRQEN bit to 0b.

18.7.4 References

- Low Pin Count Interface Specification, Revision 1.1 (LPC): http://www.intel.com/ design/chipsets/industry/lpc.htm.
- Serialized IRQ Support for PCI Systems, Revision 6.0: http://www.smsc.com/ media/Downloads_Public/papers/serirq60.doc.
- Implementing Industry Standard Architecture (ISA) with Intel[®] Express Chipsets (318244): http://www.intel.com/assets/pdf/whitepaper/318244.pdf.



PCU - iLB - Real Time Clock (RTC) 18.8

The SoC contains a real-time clock with 242 bytes of battery-backed RAM. The realtime clock performs two key functions-keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 kHz crystal and a 3.3 V battery.

The RTC supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC supports a date alarm that allows for scheduling a wake up event up to 30 undefined undefined und days in advance.

Indefined undefined 18.8.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

undefined undefined Table 111. RTC Signals

ndefineo	0	0	nd in Chapter 19, "Electrical Specifications". Ination of the signal's function.	d un
Table 111.	RTC Signals		Indefi	define
n	Signal Name	Direction /Type	Description	une
adefined u.	RTC_X1	I Analog	Crystal Input 1: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal can be driven with the desired clock rate.	
lefined une	RTC_X2	I Analog	Crystal Input 2: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal should be left floating.	
d unoc	RTC_RST_N	I	 RTC Reset: When asserted, this signal resets register bits in the RTC well. NOTE: Unless CMOS is being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. NOTE: In the case where the RTC battery is dead or missing on the platform, the signal should be deasserted before the PMC_RSMRST_N signal is deasserted. 	undefined
ed undefined under	RTC_TEST_N	ed undefi	RTC Battery Test: An external RC circuit creates a time delay for the signal such that it will go high (to ILB_RTC_3P3_G3) sometime after the battery voltage is valid. The RC time delay should be in the 10-20 ms range. This signal will be asserted just after suspend power is up if the coin cell battery is weak. NOTE: This signal may also be used for debug purposes, as part of a XDP port.	undefined
Datasheet	nden		ined undefine	60
retined un	a ta	ned unde	od undefill.	



18.8.2 Features

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 ms to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola* MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

18.8.2.1 Update Cycles

An update cycle occurs once a second, if the B.SET bit is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle starts at least 488 ms after A.UIP is asserted, and the entire cycle does not take more than 1984 ms to complete. The time and date RAM locations (00h to 09h) are disconnected from the external bus during this time.

18.8.3 Interrupts

The real-time clock interrupt is internally routed within the SoC both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the SoC, nor is it shared with any other interrupt. IRQ8# from the ILB_LPC_SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

18.8.3.1 Lockable RAM Ranges

The RTC battery-backed RAM supports two 8-byte ranges that can be locked: the RC.UL and RC.LL register bits. When the locking bits are set, the corresponding range in the RAM is not readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to re-lock the RAM range.

18.8.3.2 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in an SoC-based platform can be done by using a jumper on RTC_RST_N or a GPI. Implementations should not attempt to clear CMOS by using a jumper to pull RTC_VCC low.



Using RTC RST N to Clear CMOS 18.8.3.2.1

A jumper on RTC RST N can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTC_RST_N is strapped to ground, the GEN_PMCON1.RPS register bit will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTC_RST_N to be pulled up through a weak pull-up resistor. Table 112 shows which bits are set to their default state when RTC_RST_N is asserted. This RTC_RST_N jumper technique allows the jumper to be moved and then replaced-all while the system is powered off. Then, once booted, the Stined undefined undefined und GEN_PMCON1.RPS bit can be detected in the set state.

Table 112. Register Bits Reset by RTC RST N Assertion

			-8/1.	
	Register Bit	Bit(s)	Default State	undefined undefined
	RCRB_GENERAL_CONTROL.TS	1	xb	d unc
inde	GEN_PMCON1.PME_B0_S5_DIS	15	Ob	sined
defined undefined un	GEN_PMCON1.WOL_EN_OVRD	13	0b	nder
40fine	GEN_PMCON1.DIS_SLP_X_STRCH_SUS_UP	12	0b	d'un
unoc	GEN_PMCON1.RTC Reserved	8	Ob	stine
theo -	GEN_PMCON1.SWSMI_RATESEL	7:6	00b	
detti	GEN_PMCON1.S4MAW	5:4	00b	
Une	GEN_PMCON1.S4ASE	3	Ob	d undefined undefined
	GEN_PMCON1.RPS	2	1b	del
4	GEN_PMCON1.AG3E	0	0b	od un
, unc	PM1_STS_EN.RTC_EN	26	0b	stine
ineo -	PM1_STS_EN.PWRBTNOR_STS	11	0b	Inde
detti	PM1_CNT.SLP_TYP	12:10	0b	ed t
dune	GPE0a_EN.PME_B0_EN	13	0b	efill
stines	GPE0a_EN.BATLOW_EN	10	0b	[

undefined undefined und **Using GPI to Clear CMOS**

med undefined A jumper on a GPI can also be used to clear CMOS values. BIOS should detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again.

is a sum defined undefined undefined undefined un Warning: Do not implement a jumper on RTC_VCC to clear CMOS.

18.8.3.4 S0ix Support

During S0i3, the RTC interface is active.

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Note:





18.8.4 References

Accessing the Real Time Clock Registers and the NMI Enable Bit: http:// download.intel.com/design/intarch/PAPERS/321088.pdf.

IO Mapped Registers 18.8.5

The RTC internal registers and RAM is organized as two banks of 128 bytes each, called the standard and extended banks.

Note:

Note:

It is not possible to disable the extended bank.

The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A - D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through registers mapped to the standard I/ O space.

Registers reg_RTC_IR_type and reg_RTC_TR_type are used for data movement to and from the standard bank. Registers reg_RTC_RIR_type and reg_RTC_RTR_type are used for data movement to and from the extended bank. All of these registers have alias I/O locations, as indicated in Table 113.

Table 113. **I/O Registers Alias Locations**

I/O Registers Alias Loca	ations	ined un	ed
Register	Original I/O Location	Alias I/O Location	define
reg_RTC_IR_type	70h	74h	d une
reg_RTC_TR_type	71h	75h	sineu
reg_RTC_RIR_type	72h	76h	C
reg_RTC_RTR_type	73h	77h]

18.8.6 **Indexed Registers**

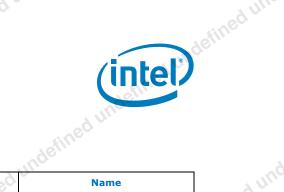
The RTC contains indexed registers that are accessed via the reg_RTC_IR_type and reg_RTC_TR_type registers.

Table 114. RTC Indexed Registers (Sheet 1 of 2)

	Start	End	Name
defined undefined u	00h	00h	Seconds
1efine	01h	01h	Seconds Alarm
unos	02h	02h	Minutes
. red	03h	03h	Minutes Alarm
Aefil'	04h	04h	Hours
	05h	05h	Hours Alarm
	06h	06h	Day of Week
214 anned	undefine	and undefined t	Datashee
Letined undefined	ined un	define	d undefined

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ned undernie .rm Platform Controller Unit (PCU) Overview



defined undefined undermeduter Table 114. RTC Indexed Registers (Sheet 2 of 2)

07h07hDay or Month08h08hMonth09h09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	07h07hDay of Month08h08hMonth09h09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	O7h Day of Month 08h 08h 09h 09h 0Ah 0Ah 0Bh 0Bh	Sta	art	End	Name
09h09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM		'h	07h	Day of Month
09h09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	09hYear0Ah0AhRegister A0Bh0BhRegister B0Ch0ChRegister C0Dh0DhRegister D0Eh7Fh114 Bytes of User RAM	80 09	ßh	08h	Month
ined undefined undefined undefined undefine	tined undefined undefined undefined undefine	tined undefined undefined undefined undefine	09	h	09h	Year
ined undefined undefined undefined undefine	tined undefined undefined undefined undefine	tined undefined undefined undefined undefine		۱h	0Ah	Register A
ined undefined undefined undefined undefine	tined undefined undefined undefined undefine	tined undefined undefined undefined undefine	CO OB			Register B
ined undefined undefined undefined undefine	tined undefined undefined undefined undefine	tined undefined undefined undefined undefine	00	Ch cin Bur	0Ch	Register C
ined undefined undefined u.	ined undefined undefined u.	ined undefined undefined u.	00	h dei	0Dh	Register D
ined undefined undefined undefined undefine	ined undefined undefined undefined undefine	ined undefined undefined undefined undefine	0E	th V	7Fh	114 Bytes of User RAM
sined undefined undefine	efined undefined	estimed undefined undefine	ined undefined	ned "	indefined uno	d undef
	efined under indefined undefined undefined undefined undefined undefined undefined	Jefined underined underine	tined undef	ined undefit.	red und	Jeffined undefinec

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PCU - iLB - 8254 Timers 18.9

stined undefined The 8254 contains three counters which have fixed uses including system timer and speaker tone. All registers are clocked by a 14.31818 MHz clock.

18.9.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional). indefined undefined
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

18.9.2 Features

18.9.2.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRO0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1, Refresh Request Signal

This counter is programmed for Mode 2 operation and impacts the period of the led undefin NSC.RTS register bit. Programming the counter to anything other than Mode 2 results in undefined behavior.

18.9.2.3 **Counter 2, Speaker Tone**

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to the NSC.SDE register bit.

18.9.2.4 S0ix Support

During S0i2 and S0i3, the 8254 timer is halted. A platform that requires the 8254 timer to be always active, should disable S0i2/3 using the S0ix_Enable register.

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18.9.3 Usage

18.9.3.1 **Timer Programming**

The counter/timers are programmed in the following fashion:

- 1. Write a control word to select a counter.
- 2. Write an initial count for that counter.
- 3. Load the least and/or most significant bytes (as required by Control Word Bits 5, 4) of the 16-bit counter.
- 4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- Control Word Command. Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- Counter Latch Command. Latches the current count so that it can be read by the system. The countdown process continues.
- Read Back Command. Reads the count value, programmed mode, the current Ained undefine state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 115 lists the six operating modes for the interval counters.

Table 115. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware re-triggerable one- shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
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Table 115. Counter Operating Modes

Counte	er Operating Modes	undefined under	
Mode	Function	Description	d une
3 sined	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.	Indefinec
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.	
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.	

18.9.3.2 **Reading from Interval Timer**

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

18.9.3.2.1 **Simple Read**

The first method is to perform a simple read operation. The counter is selected through Port 40h (Counter 0), 41h (Counter 1), or 42h (Counter 2).

Note:

Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of Counter 2, the count can be stopped by writing 0b to the NSC.TC2E register bit.

Counter Latch Command 18.9.3.2.2

The Counter Latch command, written to Port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

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18.9.3.2.3 Read Back Command

The Read Back command, written to Port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/ O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

Datasheet, d undermed underme If both count and status of a counter are latched, the first read operation from that undefined undefined undefined undefined undefined

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PCU - iLB - High Precision Event Timer (HPET) 18.10

This function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and three timers.

18.10.1 Features

18.10.1.1 Non-Periodic Mode - All Timers

This mode can be thought of as creating a one-shot. When a timer is set up for nonperiodic mode, it generates an interrupt when the value in the main counter matches the value in the timer's comparator register. As timers 1 and 2 are 32-bit, they will generate another interrupt when the main counter wraps.

TOCV cannot be programmed reliably by a single 64-bit write in a 32-bit environment unless only the periodic rate is being changed. If TOCV needs to be re-initialized, the following algorithm is performed:

- 1. Set T0C.TVS
- 2. Set T0CV[31:0]
- 3. Set T0C.TVS
- 4. Set T0CV[63:32]

Every timer is required to support the non-periodic mode of operation.

18.10.1.2 Periodic Mode - Timer 0 Only

When set up for periodic mode, when the main counter value matches the value in TOCV, an interrupt is generated (if enabled). Hardware then increases TOCV by the last value written to T0CV. During run-time, T0CV can be read to find out when the next periodic interrupt will be generated. Software is expected to remember the last value written to TOCV.

Example: if the value written to TOCV is 00000123h, then

- An interrupt will be generated when the main counter reaches 00000123h.
- TOCV will then be adjusted to 00000246h.
- Another interrupt will be generated when the main counter reaches 00000246h.
- T0CV will then be adjusted to 00000369h.

When the incremented value is greater than the maximum value possible for TOCV, the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h. undefined undefined unde



If software wants to change the periodic rate, it writes a new value to TOCV. When the timer's comparator matches, the new value is added to derive the next matching point. If software resets the main counter, the value in the comparator's value register must also be reset by setting T0C.TVS. To avoid race conditions, this should be done with the main counter halted. The following usage model is expected:

- 1. Software clears GCFG.EN to prevent any interrupts.
- 2. Software clears the main counter by writing a value of 00h to it.
- 3. Software sets T0C.TVS.
- 4. Software writes the new value in TOCV.
- 5. Software sets GCFG.EN to enable interrupts.

18.10.1.2.1 Interrupts

If each timer has a unique interrupt and the timer has been configured for edgetriggered mode, then there are no specific steps required. If configured to leveltriggered mode, then its interrupt must be cleared by software by writing a '1' back to the bit position for the interrupt to be cleared.

Interrupts associated with the various timers have several interrupt mapping options. Software should mask GCFG.LRE when reprogramming HPET interrupt routing to avoid spurious interrupts.

18.10.1.2.2 Mapping Option #1: Legacy Option (GCFG.LRE set)

Table 116. 8254 Interrupt Mapping

Mappir	ng Option #1	: Legacy Opti	ion (GCFG.LRE set)	ined
This for	ces the followi	ng mapping:	d unoc	undefin
. 8254 I	nterrupt Map	ping	define	nedt
Timer	8259 Mapping	APIC Mapping	Comment	
0	IRQ0	IRQ2	The 8254 timer will not cause any interrupts	
1	IRQ8	IRQ8	RTC will not cause any interrupts.	
2	T2C.IR	T2C.IRC	0.00	6

18.10.1.2.3 Mapping Option #2: Standard Option (GCFG.LRE cleared)

Each timer has its own routing control. The interrupts can be routed to various interrupts in the I/O APIC. T[2:0]C.IRC indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be shared with any other interrupts.

18.10.1.3 **S0ix Support**

During S0i1, the HPET is kept running. During S0i2 & S0i3, the HPET is halted.





18.10.1.4 S0ix Support

Prior to entry into S0i2 or S0i3 state, the driver/OS must set HPET_GCFG.EN to 0b to indicate RTD3_{hot} status.

18.10.2 References

IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0a: http:// www.intel.com/hardware design/hpetspec_1.pdf.

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18.11 PCU - iLB - GPIO

undefined undefined 187 GPIOs are available for use. Most of these GPIOs can be used as legacy GPIOs. This chapter describes their use as legacy GPIOs.

18.11.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional). ned undefined
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

18.11.2 **Features**

GPIOs can generate general purpose events (GPEs) on rising and/or falling edges.

GPIO Controller 18.11.2.1

The GPIO controllers handle all GPIO interface to SoC,

- GPIO NORTH used for Camera sensors, DFX, SVID, and Display Pins.
- GPIO SOUTHEAST Defines the pads/Pins for MMC/SD host controller, LPC pins, FAST SPI pins and Platform Clock.
- GPIO SOUTHWEST Defines the Pads/Pins for HS UART, I2S HS, LPE, PCIe and SPI pins.
- GPIO EAST Defines the Pads/Pins for SoC power state related signals of PMU and ISH pins.

ndefined undefin 18.11.3 Usage

defined undefined undefined Each GPIO has six registers that control how it is used, or report its status:

- Use Select
- I/O Select
- GPIO Level
- Trigger Positive Edge
- Trigger Negative Edge
- Trigger Status

ned undefinet The Use Select register selects a GPIO pin as a GPIO, or leaves it as its programmed function. This register must be set for all other registers to affect the GPIO.

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Idefined undefi Platform Controller Unit (PCU) Overview



The I/O Select register determines the direction of the GPIO.

The Trigger Positive Edge and Trigger Negative Edge registers enable general purpose events on a rising and falling edge respectively. This only applies to GPIOs set as input.

The Trigger Status register is used by software to determine if the GPIO triggered a GPE. This only applies to GPIOs set as input and with one or both of the Trigger modes enabled.

Additionally, there is one additional register for each S5 GPIO:

Wake Enable

ned undefined ut This register allows S5 GPIOs to trigger a wake event based on the Trigger registers' settings.

18.11.4 **GPIO** Registers

18.11.4.1 SD Card and LPC Pins (3.3V versus 1.8V Modes)

The CFIO cells for both the SD Card Pins (SDMMC3_*) and LPC (LPC_*) are 3.3V capable.

To use as 1.8V IOs:

Set power supply to 1.8V for the pads.

Set v1p8mode in family configuration register.

- Trigger a RCOMP cycle using Family RCOMP register
- Copy RCOMP value to Family p and n strength values.

Note:

Note:

All MMIO GPIO * PAD_VAL's must set Ienenb = 0 in order to read the pad_val of the .24 undefined undefined

All GPIO registers must be accessed as double words. Unpredictable results will occur

GPIO. This applies to RO GPIO's as well.

otherwise.

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18.12 PCU - iLB - Interrupt Decoding and Routing

The interrupt decoder is responsible for receiving interrupt messages from other devices in the SoC and decoding them for consumption by the interrupt router, the "PCU - iLB - 8259 Programmable Interrupt Controllers (PIC)" and/or the "PCU - iLB - IO APIC".

The interrupt router is responsible for mapping each incoming interrupt to the appropriate PIRQx, for consumption by the "PCU - iLB - 8259 Programmable Interrupt Controllers (PIC)" and/or the "PCU - iLB - IO APIC".

18.12.1 Features

18.12.1.1 Interrupt Decoder

The interrupt decoder receives interrupt messages from devices in the SoC. These interrupts can be split into two primary groups:

- For consumption by the interrupt router
- For consumption by the 8259 PIC

For Consumption by Interrupt Router

When a PCI-mapped device in the SoC asserts or de-asserts an INT[A:D] interrupt, an interrupt message is sent to the decoder. This message is decoded to indicate to the interrupt router which specific interrupt is asserted or de-asserted and which device the INT[A:D] interrupt originated from.

For Consumption by the 8259 PIC

When a device in the SoC asserts or de-asserts a legacy interrupt (IRQ), an interrupt message is sent to the decoder. This message is decoded to indicate to the 8259 PIC, which specific interrupt (IRQ[3, 4, 14 or 15]) was asserted or de-asserted.

18.12.1.2 Interrupt Router

The interrupt router aggregates the INT[A:D] interrupts for each PCI-mapped device in the SoC, received from the interrupt decoder, and the INT[A:D] interrupts direct from the Serialized IRQ controller. It then maps these aggregated interrupts to 8 PCI based interrupts: PIRQ[A:H]. This mapping is configured using the IR[31:0] registers.

PCI based interrupts PIRQ[A:H] are then available for consumption by either the 8259 PICs or the IO-APIC, depending on the configuration of the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH.

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Routing PCI Based Interrupts to 8259 PIC

The interrupt router can be programmed to allow PIROA-PIROH to be routed internally to the 8259 as ISA compatible interrupts IRQ 3-7, 9-12 & 14-15. The assignment is programmable through the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH. One or more PIRQs can be routed to the same IRQ input. If ISA Compatible Interrupts are not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive. When a PIRQx# is routed to undermed underme specified IRO line, software must change the IRO's corresponding ELCR bit to level sensitive mode. The SoC internally inverts the PIRQx# line to send an active high level .J). Hi .J). Hi .J). Hi undefined undefined

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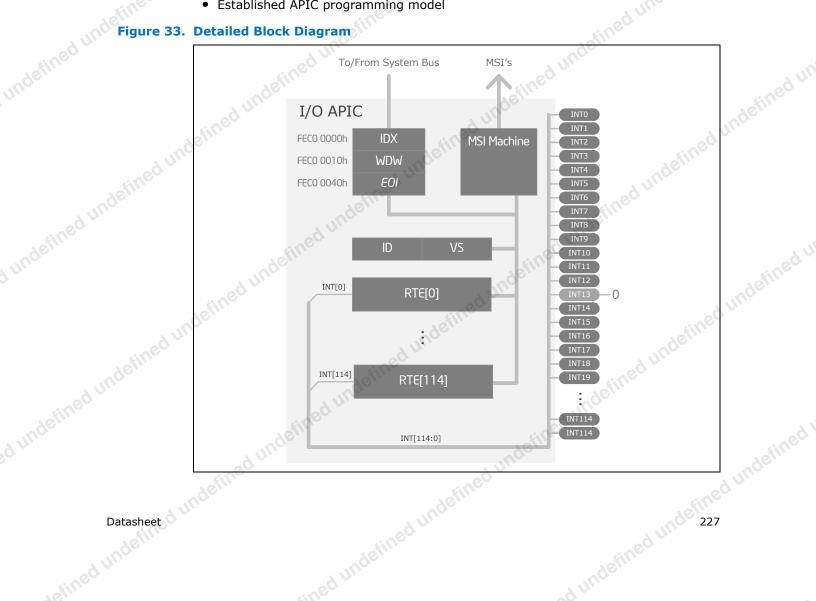
PCU - iLB - IO APIC 18.13

The IO Advanced Programmable Interrupt Controller (APIC) is used to support line interrupts more flexibly than the 8259 PIC. Line interrupts are routed to it from multiple sources, including legacy devices, via the interrupt decoder and serial IRQs, or they are routed to it from the interrupt router in the iLB. These line based interrupts are then used to generate interrupt messages targeting the local APIC in the processor.

18.13.1 **Features**

- 115 interrupt lines
 - IRQ0-114
- Edge or level trigger mode per interrupt
- Active low or high polarity per interrupt
- Works with local APIC in processor via MSIs
- MSIs can target specific processor core
- Established APIC programming model

Figure 33. Detailed Block Diagram

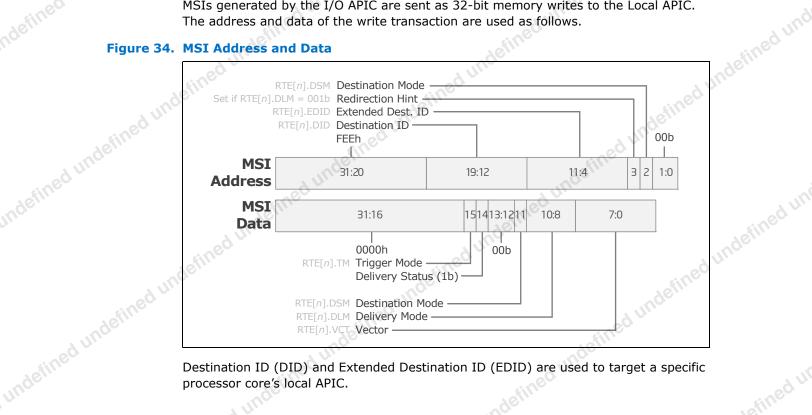




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MSIs generated by the I/O APIC are sent as 32-bit memory writes to the Local APIC. The address and data of the write transaction are used as follows.

Figure 34. MSI Address and Data



Destination ID (DID) and Extended Destination ID (EDID) are used to target a specific processor core's local APIC.

18.13.2 Usage

The I/O APIC contains indirectly accessed I/O APIC registers and normal memory mapped registers. There are three memory mapped registers:

- Index Register (IDX)
- Window Register (WDW)
- End Of Interrupt Register (EOI)

The Index register selects an indirect I/O APIC register (ID/VS/RTE[n]) to appear in the Window register.

The Window register is used to read or write the indirect register selected by the Index register.

The EOI register is written to by the Local APIC in the processor. The I/O APIC compares the lower eight bits written to the EOI register to the Vector set for each interrupt (RTE.VCT). All interrupts that match this vector will have their RTE.RIRR register cleared. All other EOI register bits are ignored. in a undefined undefined undefined

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Indirect I/O APIC Registers 18.13.3

ndefined unde These registers are selected with the IDX register, and read/written through the WDW register. Accessing these registers must be done as DW requests, otherwise unspecified behavior will result. Software should not attempt to write to reserved registers. Reserved registers may return non-zero values when read.

Note:

There is one pair of redirection (RTE) registers per interrupt line. Each pair forms a 64-

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PCU - iLB - 8259 Programmable Interrupt 18.14 **Controllers (PIC)**

SoC provides an ISA-compatible programmable interrupt controller (PIC) that incorporates the functionality of two, cascaded 8259 interrupt controllers.

18.14.1 **Features**

In addition to providing support for ISA compatible interrupts, this interrupt controller can also support PCI based interrupts (PIRQs) by mapping the PCI interrupt onto a compatible ISA interrupt line. Each 8259 controller supports eight interrupts, numbered 0–7. Table 117 shows how the controllers are connected.

Note:

atined undefined SoC does not implement any external PIRQ# signals. The PIRQs referred to in this chapter originate from the interrupt routing unit.

Table 117. Interrupt Controller Connections

adefined undefined	8259	8259 Input	Connected Pin / Function
raed une	Master	0	Internal Timer / Counter 0 output or HPET #0; determined by GCFG.LRE register bit
defin		1	IRQ1 using SERIRQ, Keyboard Emulation
une		2	Slave controller INTR output
	6	3	IRQ3 via SERIRQ, PIRQx or PCU UART 1
	stine	4	IRQ4 via SERIRQ or PIRQx
		5	IRQ5 via SERIRQ or PIRQx
undefined undefined unc		6	IRQ6 via SERIRQ or PIRQx
defin		7	IRQ7 via SERIRQ or PIRQx
d une	Slave	0	Inverted IRQ8# from internal RTC or HPET
sinec		1	IRQ9 via SERIRQ, SCI or PIRQx
nder		2	IRQ10 via SERIRQ, SCI or PIRQx
A UL		3	IRQ11 via SERIRQ, SCI, HPET or PIRQx
	e	4	IRQ12 via SERIRQ, PIRQx or mouse emulation
	detti.	5	None
200		6	PIRQx
sinec		7	IRQ15 via SERIRQ or PIRQx o

The SoC cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the SoC PIC.

Interrupts can be programmed individually to be edge or level, except for IRQ0, IRQ2 and IRQ8#.



Note:

fined undefined undefine ad undefined undefined und Active-low interrupt sources (such as a PIRQ#) are inverted inside the SoC. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term "high" indicates "active," which means "low" on an originating PIRO#.

18.14.1.1 **Interrupt Handling**

Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 118 defines the IRR, ISR, and IMR.

Table 118. Interrupt Status Registers

of any other pending interrupts. Table 118 defines the IRR, ISR, and IMR.	stined un
Description	Inde
Interrupt Request Register. This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode.	
Interrupt Service Register. This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.	
Interrupt Mask Register. This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.	10
	Interrupt Request Register. This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode. Interrupt Service Register. This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt. Interrupt Mask Register. This bit determines whether an interrupt is masked.

Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated into a Interrupt Acknowledge Cycle to the SoC. The PIC translates this command into two internal INTA# pulses expected by the 8259 controllers. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon the ICW2.IVBA bits, combined with the ICW2.IRL bits representing the interrupt within that controller.

Note:

in a makelined undefined undefined undefined undefined undefined References to ICWx and OCWx registers are relevant to both the master and slave 8259 controllers. Datasheet dundermed undermed undermed undermed undermed undermed undermed undermed undermed under the transfer to the transfer

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Table 119. Content of Interrupt Vector Byte

Table 119.	Content of Interrupt Vector	ad unoc	undefined unden.	
nder	Master, Slave Interrupt	Bits [7:3]	Bits [2:0]	ined un
	IRQ7,15	, uno	111	den
20	IRQ6,14	sine ⁰	110	
, uno	IRQ5,13	den	101	1
ineo	IRQ4,12	ICW2.IVBA	100	1
detti	IRQ3,11		011	1
med une	IRQ2,10		010	1
siner	IRQ1,9		001	
nder	IRQ0,8	ein ^e	000	dui
).	uno	der		fine

Hardware/Software Interrupt Sequence

- 1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
- 2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
- 3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle.
- 4. Upon observing the special cycle, the SoC converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
- 5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
- 6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
- ined undefi 7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

18.14.1.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the SoC, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/ O memory space: 20h for the master controller, and A0h for the slave controller.



ICW1

A write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

- 1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
- 2. The Interrupt Mask Register is cleared.
- 3. IRQ7 input is assigned priority 7.
- 4. The slave mode address is set to 7.

5. Special mask mode is cleared and Status Read is set to IRR.

ICW2

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the SoC, IRQ2 is used. Therefore, MICW3.CCC is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, ICW4.MM must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

18.14.1.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

OCW1 masks and unmasks interrupt lines.

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- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

Modes of Operation 18.14.1.4

Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt.

Interrupt priorities can be changed in the rotating priority mode.

Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave are recognized by the master and initiate interrupts to the processor. In the normal-nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.

Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2.REOI; the Rotation on Non-Specific EOI Command (OCW2.REOI=101b) and the rotate in automatic EOI mode which is set by (OCW2.REOI=100b). undefined undefined un



Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: OCW2.REOI=11xb, and OCW2.ILS is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (OCW2.REOI=111b) and OCW2.ILS=IRQ level to receive bottom priority.

Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting OCW3.PMC. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in Bit 7 if there is an interrupt, and the binary code of the highest priority level in Bits 2:0.

Edge and Level Triggered Mode

In ISA systems this mode is programmed using ICW1.LTIM, which sets level or edge for the entire controller. In the SoC, this bit is disabled and a register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned. undefined undefined unde

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18.14.1.5 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when the ICW4.AEOI bit is set to 1.

Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the SoC, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI.

An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

Note:

Both the master and slave PICs have an AEOI bit: MICW4.AEOI and SICW4.AEOI respectively. Only the MICW4.AEOI bit should be set by software. The SICW4.AEOI bit should not be set by software.

18.14.1.6 Masking Interrupts

Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

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The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without undefined issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern.

The special mask mode is set by OCW3.ESMM=1b & OCW3.SMM=1b, and cleared where OCW3.ESMM=1b & OCW3.SMM=0b.

18.14.1.7 S0ix Support

During S0i2 & S0i3, the 8259 PICs are disabled. A platform that requires the 8259 PICs to be always active, should disable S0i2/3 using the S0ix_Enable register.

18.14.2 **IO Mapped Registers**

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0 - 7), and at A0h and A1h for the slave controller (IRQ8 - 13). These registers have multiple functions, depending upon the data written to them. Table 120 is a description of the different register possibilities for each address.

Note:

The register descriptions after Table 120 represent one register possibility.

Table 120. I/O Registers Alias Locations

Table 120.	I/O Registers Alias Locati		ed unde	
	Registers	Original I/O Location	Alias I/O Locations	undefined un
ndefined und	ined t	dun	24h	nder
	MICW1	ned undefined un	28h	
dull	MICWI	inde	2Ch	
stinet	MOCW2	20h	30h	
	MOCW2 MOCW3		34h	
	d une		38h	
	sineu		3Ch	undefined
	der.	ined under 21h	25h	cine ⁰
	MICW2	unos	29h	defin
undefined un	MICW3	ined	2Dh	Un
711	MICW4	21h	31h	
red	MICW4	d une	35h	
defin	MOCW1	finet.	39h	
	, de		3Dh	
	ndefined undefined unde	m.	4 UNOC	
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Detectors	(n°	inde.	defili	7
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I/O Registers Alias Locations Table 120.

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indefine	1611	nec	sined un.	
Table 120. I/O Reg	isters Alias Locati	ions	undeit	7
	Registers	Original I/O Location	Alias I/O Locations	
2 U	no	nden	A4h	, efil
eineo	SICW1	ed un	A8h	JUOC
nder	60.0W2	define -	ACh	
ed u	SOCW2	A0h	B0h B4h	-
define	SOCW3	neo	B8h	-
Unc		í –	BCh	-
Jundefined undefinee	eq M.	<u>د</u>	A5h	-
	SICW2	- Miles	A9h	-
	SICW3	nder	ADh	204
stinec	SICW4	A1h	B1h	unu
inde.		defill	B5h	-
ined t	SOCW1	dunc	B9h	-
defin	ELCR1	4D0h	BDh N/A	-
		4D1h	N/A N/A	-
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Electrical Specifications 19

This chapter is categorized into the following sections:

- "Absolute Maximum and Minimum Specifications"
- "Thermal Specifications'
- "Storage Conditions"
- "Voltage and Current Specifications"
- "Crystal Specifications"
- "DC Specifications"

19.1

Absolute Maximum and Minimum Specifications

The absolute maximum and minimum specifications are used to specify conditions allowable outside of the functional limits of the SoC, but with possible reduced life expectancy once returned to function limits.

At conditions exceeding absolute specifications, neither functionality nor long term reliability can be expected. Parts may not function at all once returned to functional limits.

Although the processor contains protective circuitry to resist damage from Electrostatic discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Thermal Specifications

These specifications define the operating thermal limits of the SoC. Thermal solutions not designed to provide the following level of thermal capability may affect the longterm reliability of the processor and system, but more likely result in performance throttling to ensure silicon junction temperatures within specification.

This section specifies the thermal specifications for all SKUs. Some definitions are needed, however. "Tj Max" defines the maximum operating silicon junction temperature. Unless otherwise specified, all specifications in this document assume Tj Max as the worse case junction temperature. This is the temperature needed to ensure TDP specifications when running at guaranteed CPU and graphics frequencies. "TDP" defines the thermal dissipated power for a worse case estimated real world thermal scenario. "SDP", or scenario dissipated power, defines the thermal dissipated power under a lighter workload specific to a user scenario and at a lower thermal junction temperature than Tj Max. Note that turbo frequencies are opportunistically selected when thermal headroom exists. Automatic throttling along with a proper thermal solution ensure Tj Max will not be exceeded. , undefined undefined u

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Table 121. Thermal Specifications

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Thermal Specifications	nec	undefined un	ind
ndette	T4 Jefine	T3	undefined und
T _j Max	90 °C	90 °C	dein
T _j Min	0 °C	0 °C	dui
T _j @ Max. Steady State Power (SDP)	70 °C	70 °C	
SDP	2W	2.2 W	1
			_

ndefined undefined und **Storage Conditions**

This section specifies absolute maximum and minimum storage temperature and humidity limits for given time durations. Failure to adhere to the specified limits could result in physical damage to the component. If this is suspected, Intel recommends a visual inspection to determine possible physical damage to the silicon or surface components.

Table 122. Storage Conditions Prior to Board Attach

Symbol	Parameter	Min	Мах	
Tabsolute storage	Device storage temperature when exceeded for any length of time.	-25 °C	125 °C	ed
Tshort term storage	The ambient storage temperature and time for up to 72 hours.	-25 °C	85 °C	indefille
Tsustained storage	The ambient storage temperature and time for up to 30 months.	5 °C	40 °C	sd u
RHsustained storage	The maximum device storage relative humidity for up to 30 months.		60% @ 24 °C	

NOTES:

- Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount re-flow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
- Component product device storage temperature qualification methods may follow JESD22-A119 (low temperature) and JESD22-A103 (high temperature) standards when applicable for volatile memory.
- Component stress testing is conducted in conformance with JESD22-A104.
- The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag. undefined undefined undefined undefine in the sundefined undefined undefined



stined undefine 19.3.1 Post Board-Attach

Indefined und The storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component-level certification assessments post board-attach given the multitude of attach methods, socket types, and board types used by customers.

Provided as general guidance only, board-level Intel-branded products are specified and certified to meet the following temperature and humidity limits:

- Non-Operating Temperature Limit: -40 °C to 70 °C
- Humidity: 50% to 90%, non-condensing with a maximum wet-bulb of 28 °C

Voltage and Current Specifications 19.4

The I/O buffer supply voltages are specified at the SoC package balls. The tolerances shown in Table 138 are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 124 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the ndefined undefined decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Note:

The SoC is a pre-launch product. Voltage and current specifications are subject to change.

~0					
ndefineo	Platform Rail	lefined L	Voltage Tolerances	Max Icc	IUC
	V1P05A	UNCORE1_V1P05A_G3		gen	
		UNCORE2_V1P05A_G3		NU-	
	defi	DDR_V1P05A_G3	1.05 V		edu
	y nuc	USB3_V1P05A_G3	DC: ±2%	1700 mA	defined undefined u
		USBSSIC_V1P05A_G3	AC: ±2%		unos
	Jer.	F_V1P05A_G3			ineo -
undefined un		PCIECLK_V1P05A_G3			defini
stines	V1P15	CORE_V1P15_S0iX	1.15 V	2	UNC
inde		DDI_V1P15_S0iX		anostine	
		UNCORE_V1P15_S0iX	DC: ±2% AC: ±3%	2100 mA	
		F_V1P15_S0iX	6	U	
20	Idefined under	ined undefined undefine	ed undefine		sined undefined
Datasheet		ed unoc			
undefill		undefine		undefine	
		cined t		Jun	

Table 123. SoC Power Rail DC Specs and Max Current

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Inter	sined undefine		Electrical Specific	
tine	ed un		, unos	
nder	define			
Table 123. SoC Power Rail	DC Specs and Max Curren	t	deir	
Table 123. SoC Power Rail	4 ⁰	Voltage Tolerances	Max Icc	ad undefined
V1P2A	USBSSIC_V1P2A_G3	1.24 V		defin
stine	MIPI_V1P2A_G3	DC: ±2%	67 mA	dune
inde	USBHSIC_V1P2A_G3	AC: ±2%		
V1P8A	USB_V1P8A_G3		nde	
ACTIN	UNCORE_V1P8A_G3	1.8 V	d W	
unoc	GPIOSE_V1P8A_G3	DC: ±2%	971 mA	
ð.	GPION_V1P8A_G3	AC: ±2%	nde	
V1P8A V3P3A	F_V1P8A_G3	ed '	1 I	2
V3P3A	USB_V3P3A_G3	3.3 V	<u> </u>	stined undefined
od un	F_V3P3A_G3		196 mA	detin
stine	RTC_V3P3A_G5	DC: ±2% AC: ±2%		dun
V3P3A_V1P8A	SDIO_V3P3A_V1P8A_G3	1.8 V/3.3 V	<u> </u>	
V3P3A_V1P8A VSFR	LPC_V3P3A_V1P8A_S4	_		31.
leftin-		DC: ±2% AC: ±2%	d un	
VSFR	ICLK_VSFR_G3		1 etino	
VOLK	CORE0_VSFR_G3	1.05 V/1.24 V/ 1.35 V	Inde	
		d	<u>-</u>	
nde	CORE1_VSFR_G3	DC: ±2% AC: ±3%		lefined undefine
	UNCORE_VSFR_G3		<u> </u>	
VCC0	CORE_VCC0_S0IX	Refer Table 124	3200 mA	dun
	CORE_VCC0_SENSE		<u> </u>	Aines
VCC1	CORE_VCC1_SOIX	Refer Table 124	3200 mA	<u>ю.</u>
	CORE_VCC1_SENSE			
VNN	UNCORE_VNN_S4	Refer Table 124	2500 mA	
	UNCORE_VNN_SENSE		2500 mA	
VGG	DDI_VGG_S0iX	Refer	8000 mA	
	DDI_VGG_SENSE	Table 124		
VNN		unos		dein
etine		neo -		dun
Inoc	defi			
242 242 242 242	A UNC			ge.
Aefil .	UNCORE_VNN_S4 UNCORE_VNN_SENSE DDI_VGG_S0IX DDI_VGG_SENSE		od un	
nur.			etine	
	du		unor	
۸.				
ind	ю.	Aefili		
ed u.		4 Une		nden
1.efine				-dui.
inde	Act			siner
2	1 Une		Da	itasheet
define			du	
	den		sine	
	d un		nde	
			du.	

defined undefined undefined Table 123. SoC Power Rail DC Specs and Max Current



Platform Rail		Voltage Tolerances	Max Icc	ined
VDDQ	DDI1_VDDQ_G3	1.24 V/1.35 V		dem
	DDI2_VDDQ_G3	DC: ±2%		dull
	USB_VDDQ_G3	AC: ±2%		sines
VDDQG	DDR_VDDQG_S4		1900 -	ge.
	DDRCH0_VDDQG_S4	1.24 V/1.35 V	2500mA	
	DDRCH1_VDDQG_S4	DC: ±2%	etine	
	DDRSFRCH0_VDDQG_S4	AC: ±2%	0-	
i afin'	DDRSFRCH1_VDDQG_S4	ined i		6
V3P3RTC	RTC_V3P3RTC_G5	G5: 2-3 V at battery		definer
tinet	defined	Otherwise V3P3A (pre diode drop)	-	sined uno.

ndefined undefined Table 123. SoC Power Rail DC Specs and Max Current

NOTE:

- 1. RTC VCC average current draw (G5) is specified at 27°C under battery conditions
- 2. This value is applicable only for Z8350 and Z8300 SKUs.

undefined undefined und VCC and VNN Voltage Specifications

Table 124 and Table 138 list the DC specifications for the SoC power rails. They are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 124.	VCC and	VNN DO	C Voltage	Specifications
------------	---------	--------	-----------	-----------------------

Symbol Parameter Min Typ Max Unit Note CORE_VCC VID [Z8700, 28750] Core VID Target Range 0.6 1.30 V I CORE_VCC VID [Z8500, 28550] Core VID Target Range 0.6 1.28 V I CORE_VCC VID [Z8300, 28350] Core VID Target Range 0.6 1.13 V I CORE_VCC0_S0IX V _{CC0} for SoC Core 0 Refer VCC VID V 2 CORE_VCC1_S0IX V _{CC1} for SoC Core 1 Refer VCC VID V 2 UNCORE_VNN VID [Z8700] Uncore VID Target Range 0.4 1.28 V UNCORE_VNN VID [Z8300, Uncore VID Target Range 0.4 1.11 V I UNCORE_VNN_S4 V _{NN} for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0IX [Z8700] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0IX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0IX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V I									
CORE_VCC0_S0iX V _{CC0} for SoC Core 0 Refer VCC VID V 2 CORE_VCC1_S0iX V _{CC1} for SoC Core 1 Refer VCC VID V 2 UNCORE_VNN VID [Z8700] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8500] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8300, Uncore VID Target Range 0.4 1.1 V - UNCORE_VNN_S4 V _{NN} for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V -		Symbol	Parameter	Min	Тур	Max	Unit	Note	
CORE_VCC0_S0iX V _{CC0} for SoC Core 0 Refer VCC VID V 2 CORE_VCC1_S0iX V _{CC1} for SoC Core 1 Refer VCC VID V 2 UNCORE_VNN VID [Z8700] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8500] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8300, Z8350] Uncore VID Target Range 0.4 1.1 V - UNCORE_VNN_S4 V _{NN} for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V -	d un	CORE_VCC VID [Z8700, Z8750]	Core VID Target Range	0.6	26	1.30	V		
CORE_VCC0_S0iX V _{CC0} for SoC Core 0 Refer VCC VID V 2 CORE_VCC1_S0iX V _{CC1} for SoC Core 1 Refer VCC VID V 2 UNCORE_VNN VID [Z8700] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8500] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8300, Z8350] Uncore VID Target Range 0.4 1.1 V - UNCORE_VNN_S4 V _{NN} for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V -		CORE_VCC VID [Z8500, Z8550]	Core VID Target Range	0.6	, una	1.28	V		
CORE_VCC0_S0iX V _{CC0} for SoC Core 0 Refer VCC VID V 2 CORE_VCC1_S0iX V _{CC1} for SoC Core 1 Refer VCC VID V 2 UNCORE_VNN VID [Z8700] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8500] Uncore VID Target Range 0.4 1.28 V - UNCORE_VNN VID [Z8300, Uncore VID Target Range 0.4 1.1 V - UNCORE_VNN_S4 V _{NN} for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 0.9 V - DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V -	nder	CORE_VCC VID [Z8300, Z8350]	Core VID Target Range	0.6	0	1.13	V		du
UNCORE_VNN VID [Z8700] Uncore VID Target Range 0.4 1.28 V UNCORE_VNN VID [Z8500] Uncore VID Target Range 0.4 1.28 V UNCORE_VNN VID [Z8300, Uncore VID Target Range 0.4 1.1 V UNCORE_VNN_S4 V_NN for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8500] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V	U	CORE_VCC0_S0iX	V _{CC0} for SoC Core 0	Ret	fer VCC VII	D	V	2	stines
UNCORE_VNN VID [Z8500] Uncore VID Target Range 0.4 1.28 V UNCORE_VNN VID [Z8300, Z8350] Uncore VID Target Range 0.4 1.1 V UNCORE_VNN_S4 V _{NN} for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V 2 DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V 2 DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V 2		CORE_VCC1_S0iX	V _{CC1} for SoC Core 1	Ret	fer VCC VII	D	V	2	nde
UNCORE_VNN VID [Z8300, Z8350] Uncore VID Target Range 0.4 1.1 V		UNCORE_VNN VID [Z8700]	Uncore VID Target Range	0.4		1.28	V	ed i	P -
Z8350] VNN for SoC Uncore Refer VNN VID V 2 DDI_VGG_S0iX [Z8700] VGG for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8500] VGG for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8300, Z8350] VGG for SoC Display 0.4 1.1 V		UNCORE_VNN VID [Z8500]	Uncore VID Target Range	0.4		1.28	V		
DDI_VGG_S0iX [Z8700] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8500] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V			Uncore VID Target Range	0.4		1.1	V		
DDI_VGG_S0iX [Z8500] V _{GG} for SoC Display 0.4 0.9 V DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V	20	UNCORE_VNN_S4	V _{NN} for SoC Uncore	Ref	fer VNN VI	D	V	2	
DDI_VGG_S0iX [Z8300, Z8350] V _{GG} for SoC Display 0.4 1.1 V Datasheet 243		DDI_VGG_S0iX [Z8700]	V _{GG} for SoC Display	0.4	, uno	0.9	V		
Datasheet	der	DDI_VGG_S0iX [Z8500]	V _{GG} for SoC Display	0.4	leo	0.9	V		6-
Datasheet dunde inde inde inde inde inde inde inde i	d UII	DDI_VGG_S0iX [Z8300, Z8350]	V _{GG} for SoC Display	0.4		1.1	V		sines
sineo unoc		Datasheet ounderingeo	ed undefined undefine	ed un	und	Jefined	unde	243	unde

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Table 124. VCC and VNN DC Voltage Specifications

Symbol	Parameter	Min	Тур	Max	Unit	Note
CORE_VCC/UNCORE_VNN V _{BOOT}	Default target $V_{\text{CC}}/V_{\text{NN}}$ voltage for initial power up.	uden	1.0 or 1.1		V	3
VCC0/1 Tolerance	Tolerance of VCC0/1 voltage at VID target.	DC: ±2%	%	ed1		
VNN Tolerance	Tolerance of VNN voltage at VID target.	DC: ±2%	%	1		
VGG Tolerance	Tolerance of VGG voltage at VID target.	DC: ±2%	AC: ±3%	Inec	%	1

NOTES:

- 1. Contact local Intel representative for load line and tolerance details.
- 2. Each SoC is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two SoCs at the same frequency may have different settings within the VID range. Note this differs from the VID employed by the SoC during a power management event.
- 3. Refer VR12/IMVP7 Pulse Width Modulation specification for additional details. Either value is ok. Jeffined undefined

19.4.2 **CPU ESD LEVEL**

Table 125. CPU ESD level details

CPU Type	CDM	НВМ
T4/T3	±250v	±1000v

19.5

Crystal Specifications There are two crystal oscillators. One for RTC which maintains time and provides initial timing reference for power sequencing. The other is for the Integrated Clock, which covers clocking for the entire SoC.

Table 126. ILB RTC Crystal Specification

Cumhal	Devenetor	Min		Max	Units	Notes	
Symbol	Parameter	Min	Тур	Max	units	notes	undefined
F _{RTC}	Frequency	- co	32.768	-	kHz	1	d un
СТ _{РРМ}	Crystal frequency tolerance (refer notes)	ndefin	-	+/-20	ppm		800
P _{DRIVE}	Crystal drive load	-	0.1	0.5	uW	1	
C _{LOAD}	Crystal load capacitance		12.5		pF]
C _{SHUNT}	Crystal shunt capacitance	-	1.3	- , d	рF	1]
C_1/C_2	Load Capacitance tolerance			+/-10	%		1

NOTES:

1. These are the specifications needed to select a crystal oscillator for the RTC circuit.



2. Crystal tolerance impacts RTC time. A 10 ppm crystal is recommended for 1.7 s tolerance per ndefined und day, RTC circuit itself contributes addition 10 ppm for a total of 20 ppm in this example.

Table 127. Integrated Clock Crystal Specification

			<u> </u>				
	Symbol	Parameter	Min	Тур	Max	Units	Notes
	F _{ICLK}	Frequency	ine <u>o</u>	19.2	-	MHz	10
ned unc	T _{PPM}	Crystal frequency tolerance & stability	-	-	+/-30	ppm	in 1
	P _{DRIVE}	Crystal drive load	-	-	100	uW	1
defined undefinit	R _{ESR}	ESR	-	-	80	Ohm	1
	C _{LOAD}	Crystal load capacitance		12	Inos	pF	
den	C _{SHUNT}	Crystal shunt capacitance	-	0.75	-	pF	1
	C ₁ /C ₂	Load Capacitance tolerance		en	+/-10	%	
				100			

NOTE:

1. These are the specifications required to select a crystal oscillator for the Integrated Clock circuit. Crystal must be AT cut, fundamental, parallel resonance.

19.6

DC Specifications

Platform reference voltages are specified at DC only. V_{REF} measurements should be made with respect to the supply voltages specified in "Voltage and Current Specifications".

Note:

 $V_{IH/OH}$ Max and $V_{IL/OL}$ Min values are bounded by reference voltages.

The following DC Specifications are explained in this section:

- "Display DC Specification"
- "MIPI-Camera Serial Interface (CSI) DC Specification"
- "SDIO DC Specification"
- "SD Card DC Specification"
- "eMMC 4.51 DC Specification"
- "JTAG DC Specification"
- "LPDDR3 Memory Controller DC Specification"
- "USB 2.0 Host DC Specification"
- "USB 3.0 DC Specification"
- "SSIC DC Specification"
- "SPI and FST_SPI DC Specification"
- "Power Management/Thermal (PMC) and RTC DC Specification"
- "SVID DC Specification"
- in a undefined undefined undef GPIO DC Specification"

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- "SIO I2C DC Specification"
- "SIO UART DC Specification"
- "I2S (Audio) DC Specification"
- "PCI Express DC Specification"

Note:

fined undefined undefined undefined undefined Care should be taken to read all notes associated with each parameter.

19.6.1 **Display DC Specification**

- "Display Port DC Specification"
- "HDMI DC Specification"
- "Embedded Display Port DC Specification"
- "Display Port AUX Channel DC Specification"
- "Embedded Display Port AUX Channel DC Specification"
- "DDC Signal DC Specification"
- "MIPI DSI DC Specification"

undefined undefined ur **Display Port DC Specification**

Table 128. Display Port DC specification

		18/11						
ed un	DC specificati	ons for display interfaces:			6	S _I I,		
efine	• "Display F	Port DC Specification"			-d une			
Indefined under et.	• "HDMI DO	Specification"		nija	ed undf			. red v
	• "Embedde	ed Display Port DC Specifica	ation"	Inde.				ned undefined ut
		Port AUX Channel DC Speci						dun
In		ed Display Port AUX Channe		ecificatio	n″			
		nal DC Specification					inde.	
undefined undefined 19.6.1.1 Table 128.	-	DC Specification"				e		
d un		Inos				efili		
19.6.1.1	Display Por	rt DC Specification			dun			
unoc		Jeth		ii)	Jec.			ed !
Table 128.	Display Port	DC specification	-	nde		1		defin
	Symbol	Parameter	Min	Тур	Max	Units	Notes	ned undefined "
undefined undefined un	V _{TX-DIFFp-p-} Level0	Differential Peak-to-peak Output Voltage Level 0	0.34	0.4	0.46	V	def	IN CC
indefine	V _{TX-DIFFp-p-} Level1	Differential Peak-to-peak Output Voltage Level 1	0.51	0.6	0.68	V	d un	
leftined L	V _{TX-DIFFp-p-} Level2	Differential Peak-to-peak Output Voltage Level 2	0.69	0.8	0.92	v		
unoc	VT _{X-DIFFp-p-} Level3	Differential Peak-to-peak Output Voltage Level 3	0.85	1.2	1.38	V		Ined undefined
	sineo	No Pre-emphasis	0.0	0.0	0.0	dB		unde
	V _{TX-PREEMP-} RATIO	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB		ned
du	RATIO	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	-96	
efine		9.5 dB Pre-emphasis	7.5	9.5	11.4	dB	d une	
d undefined undefined u	V _{TX-DC-CM}	Tx DC Common Mode Voltage	0		2.0	Verin	^e	
adefine		afined			ned u			
dui		Inde		-9e				stine
246 246 undefined	stined	indefined undefined u		d une				sheet
	inde.		defini					sineu
246		2 V	n.				Datas	sheet
adefine		Lefineo					ned un	
ed un.		unde						
stine					-6'	71.		



ndefined undefined Table 128. Display Port DC specification

Table 128. [Display Port	DC specification						
etill	Symbol	Parameter	Min	Тур	Max	Units	Notes	d ur
-	RL _{TX-DIFF}	Differential Return Loss at 0.675GHz at Tx Package pins	12 dun	Jein,		dB		undefinec
red under		Differential Return Loss at 1.35 GHz at Tx Package pins	9			dB	ndefineo	
defin.	C _{TX}	TX Output Capacitance			1.5	pF	2	
	NOTES:	s line between 0.675 GHz and			ndef	In		

NOTES:

- 1. Straight loss line between 0.675 GHz and 1.35 GHz.
- ndefined undefined und 2. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX termination. undefined und

19.6.1.2 **HDMI DC Specification**

Table 129. HDMI DC specification undefined undefin

							_
Symbol	Parameter	Min	Тур	Max	Units	Notes	
Voff	Single Ended Standby (off), output voltage	-10		10	mV	1 @ AVcc	
Vswing	Single Ended output swing voltage	400	sine	600	mV		
V _{OH} (<=165 MHz)	Single Ended high level, output voltage	-10	uge.	10	mv	1 @ AVcc	undefine
V _{OH} (>165 MHz)	Single Ended high level, output voltage	-200		10	mV	1 @ AVcc	ed u.
V _{OL} (<=165 MHz)	Single Ended low level, output voltage	-600		-400	mV	1 @ AVcc	
V _{OL} (>165MH z)	Single Ended low level, output voltage	-700		-400	mV	1 @ AVcc	

Jundefined undefined und **Embedded Display Port DC Specification**

Table 130. Embedded Display Port DC Specification d undefined undefine

able 130.		isplay Port DC Specificat	6	_			- A CAL	led un
sineo	Symbol	Parameter	Min	Тур	Max	Units	Notes	
S/,	V _{TX-DIFFp-p-} Level0	Differential Peak-to-peak Output Voltage Level 0	0.18	0.2	0.22	ofine	1,2	
	V _{TX-DIFFp-p-} Level1	Differential Peak-to-peak Output Voltage Level 1	0.2	0.25	0.275	v	1,2	
	V _{TX-DIFFp-p-} Level2	Differential Peak-to-peak Output Voltage Level 2	0.27	0.3	0.33	V	1,2	defin
	defines		efined					ned unc.
sheet		d un					ndei	247

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Cincer		Lefined undefi			ons			
Table 130.	Embedded D	Display Port DC Specificat			indef	ined		
defill	Symbol	Parameter	Min	Тур	Max	Units	Notes	dunc
•	VT _{X-DIFFp-p-} Level3	Differential Peak-to-peak Output Voltage Level 3	0.315	0.35	0.385	V	1,2	odefine
ind	VT _{X-DIFFp-p-} Level4	Differential Peak-to-peak Output Voltage Level 4	0.36	0.4	0.44	V	1,2	d UI
lefined t	VT _{X-DIFFp-p-} Level5	Differential Peak-to-peak Output Voltage Level 5	0.405	0.45	0.495	V	1,2	
Idefined undefined und	VT _{X-DIFFp-p-} MAX	Maximum Allowed Differential Peak-to-peak Output Voltage			1.380	inv.	3	
lde.	V _{TX-DC-CM}	Tx DC Common Mode Voltage	0	defin	2.0	V	1,2,3	stined un
	ed	No Pre-emphasis	0.0	0.0	0.0	dB	1,2,3	nder
2	V _{TX-PREEMP-}	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB	1,2,3	du
	RATIO	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	1,2,3	
cine ⁰		9.5 dB Pre-emphasis	7.5	9.5	11.4	dB	1,2,3	1
ndefined undefined und	RL _{TX-DIFF}	Differential Return Loss at 0.675GHz at Tx Package pins	12		.nd	dB	4	
idefill.		Differential Return Loss at 1.35 GHz at Tx Package pins	9	defil	led u.	dB	4	stined ut
	C _{TX}	TX Output Capacitance		JUL	1.5	рF	5	der

Jefined undefined undefined **Table 130. Embedded Display Port DC Specification**

NOTES:

- 1. Steps between VTX-DIFFP-P voltages must be monotonic. The actual VTX-DIFFP-P-1 voltage must be equal to or greater than the actual VTX-DIFFP-P-0 voltage; the actual VTX-DIFFP-P-2 voltage must be greater than the actual VTX-DIFFP-P-1 voltage; etc.
- 2. The recommended minimum VTX-DIFFP-P delta between adjacent voltages is mV.
- 3. Allows eDP Source devices to support differential signal voltages compatible with eDP v1.3 (and lower) devices and designs.
- 4. Straight loss line between 0.675 GHz and 1.35 GHz.
- 5. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX d undefined



Display Port AUX Channel DC Specification 19.6.1.4

defined undefined un 19.6.1.4 Table 131.	left ⁱ	t AUX Channel DC Spe Innel DC Specification	cificati	on efined l	Inde.			aned un
	Symbol	Parameter	Min	Тур	Max	Units	Notes	undern.
a unde	V _{AUX-DIFFp-p}	AUX Peak-to-peak Voltage at a transmitting Device	0.29		1.38	V	1efined	
adefinec	V _{AUX} TERM_R	AUX CH termination DC resistance		100		ΩJſ	0.	
sined un	V _{AUX-DC-CM}	AUX DC Common Mode Voltage	0		2.0	V	2	
derr	V _{AUX} -TURN-CM	AUX turn around common mode voltage		Aefine ⁰	0.3	V	3	sined u
	I _{AUX_SHORT}	AUX Short Circuit Current Limit	ed un	0.	90	mA	4	unden
nd	C _{AUX}	AC Coupling Capacitor	75		200	nF	5	
ndefined undefined u	 Common mo Steady state Total drive ci All DisplayPo 	= 2* V _{AUXP} - V _{AUXM} ode voltage is equal to V _{bias_Tx} common mode voltage shift t urrent of the transmitter when ort Main Link lanes as well as A ced on the transmitter side. Pla nal.	it is short UX CH mu	ansmit and ted to its g ust be AC o	d receive round. coupled. A	AC coupli	ng capacito	rs

Table 131. DDI AUX Channel DC Specification

NOTES:

- 1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} V_{AUXM}|$
- Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
 Steady state common mode voltage shift between transmit and receive modes of operation.
- 4. Total drive current of the transmitter when it is shorted to its ground.
- undefined undefined 5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.

Embedded Display Port AUX Channel DC Specification 19.6.1.5

Table 132. Embedded Display Port AUX Channel DC Specification

deti	Symbol	Parameter	Min	Тур	Max	Units	Notes	
indefined undefine	V _{AUX-DIFFp-p}	AUX Peak-to-peak Voltage at a transmitting Device	0.29		1.38	v	1	
under	V _{AUXTERM_R}	AUX CH termination DC resistance		100	,O	Ω		fined
	V _{AUX-DC-CM}	AUX DC Common Mode Voltage	0 ed i		1.2	V	2	d under
ed un	V _{AUX} -TURN-CM	AUX turn around common mode voltage	SLL.		0.3	V	3 fin	
indefined undefinec	I _{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	4	
ed u	C _{AUX}	AC Coupling Capacitor	75		200	nF	5	
d undefine	NOTES: 1. V _{AUX-DIFFp-p} = 2. Common mo 3. Steady state	= 2* V _{AUXP} – V _{AUXM} de voltage is equal to V _{bias_Tx} common mode voltage shift b	(or V _{bias_f}	_{Rx}) voltage ansmit an	e. d receive	modes o	of operation.	odefined

NOTES:

- 1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} V_{AUXM}|$
- A modefined undefined undefined Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
 Steady state common mode voltage shift between transmit and receive modes of operation. re undefined undefin

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- intel red under
 - 4. Total drive current of the transmitter when it is shorted to its ground.
 - undefined undefined und 5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.

DDC Signal DC Specification 19.6.1.6

Table 133. DDC Signal DC Specification (DCC_DATA, DDC_CLK)

Symbol	Parameter	Min	Тур	Мах	Units	Notes
V _{REF}	I/O Voltage	GP	ION_V1P8A	_G3	V	
V _{IH}	Input High Voltage	0.75*V _{REF}		du.	V	1
V_{IL}	Input Low Voltage		i al	0.35*V _{REF}	V	2
V _{OL}	Output Low Voltage		Inor	0.45	V	3
Ii	Input Pin Leakage	-10	20	10	μA	4

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. This buffer reaches VOH/VOL with 3mA load.
- 4. For VIN between 0V and CORE_VCC_S0iX. Measured when driver is tri-stated.

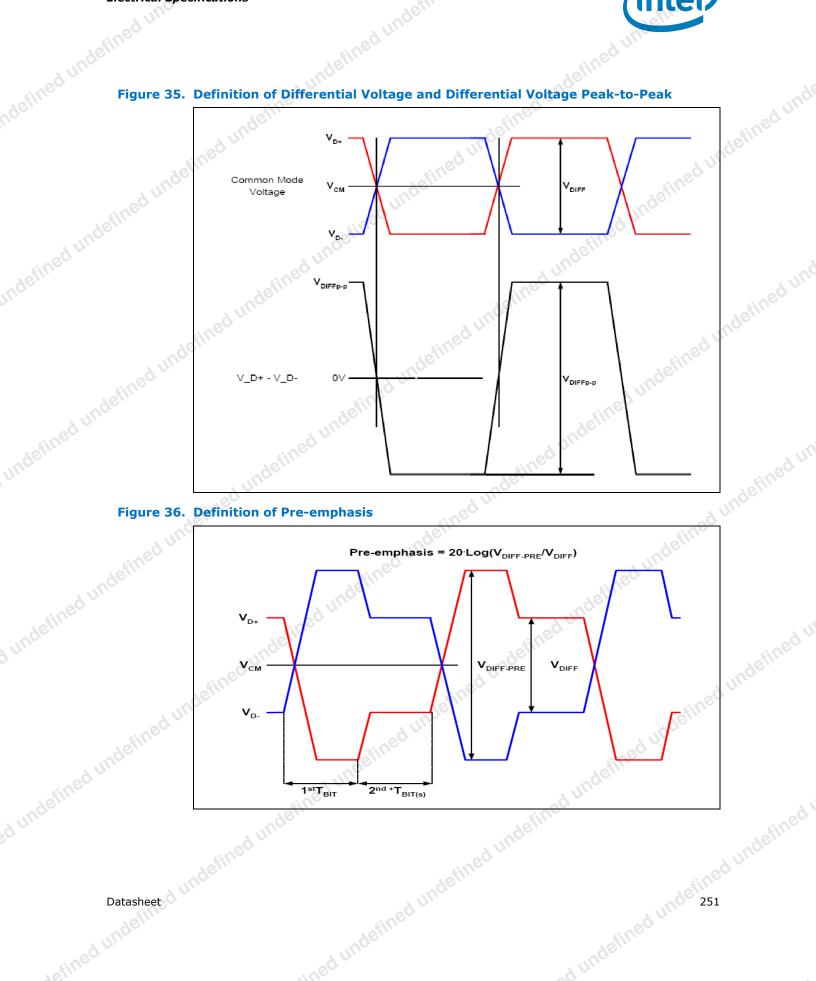
Table 134. DDC Misc Signal DC Specification (HPD, BKLTCTL, VDDEN, BKLTEN)

 This buffer reaches VOH/VOL with 3mA load. For VIN between 0V and CORE_VCC_S0iX. Measured when driver is tri-stated. DDC Misc Signal DC Specification (HPD, BKLTCTL, VDDEN, BKLTEN) Symbol Parameter Min Typ Max Units Notes									
Symbol	Parameter	Min	Тур	Мах	Units	Notes	ed V.		
V _{REF}	I/O Voltage	GPI	4_G3	V	den				
V_{IH}	Input High Voltage	0.75*V _{REF}			V	U 1			
V _{IL}	Input Low Voltage			0.35*V _{REF}	V	2			
Z _{pu}	Pull up Impedance	40	50	60	Ω	3			
Z _{pd}	Pull down Impedance	40	50	60	Ω	3			
Ii	Input Pin Leakage	-10		10	μA	4	ineo i		

NOTES:

- V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at CORE_VCC0_S0iX and CORE_VCC1_S0iX.
- 4. For VIN between 0V and CORE_VCC0_S0iX and CORE_VCC1_S0iX. Measured when driver is tri-stated.
- in a undefined undefined undefined 5. This buffer reaches VOH/VOL with 3mA load.







Jeffined undefined undefined **MIPI DSI DC Specification** 19.6.1.7

Table 135. MIPI DSI DC Specification

Intel		sined unde	Electrica	I				
red undefine 19.6.1.7		der			Indefined	uno-		
e ^d 19.6.1.7	MIPI DSI I	DC Specification			INOC			
Table 135		C Specification		sineo				
	Symbol	Parameter	Min.J	Nom.	Max.	Unit	Notes	ndefil.
	ILEAK	Pin Leakage current	-10	-	10	μA	_eò`	
dun	MIPI DSI HS		<u>.</u>				SUL	1
ndefine	V _{CMTX}	HS transmit static common-mode voltage	150	200	250	mV		-
led undefined un.	V _{CMTX(1,0)}	V _{CMTX} mismatch when output is differential-1 or differential-0	-	-	5 dem	mV		-
	IVODI UNC	HS transmit differential voltage	140	200	270	mV		defit
, ur	ΔV _{OD}	V _{OD} mismatch when output is Differential-1 or Differential-0	efined b	-	14	mV	sined	UNC
tined t	V _{OHHS}	HS output high voltage	-	-	360	mV		
undefin	Z _{OS}	Single-ended output impedance	40	50	62.5	Ω		-
ned undefined un	ΔZ _{OS}	Single-ended output impedance mismatch	-	-	10,00	%		-
	MIPI DSI LP	-TX Mode		stine				
	V _{OH}	Thevenin output high level	1.1	1.2	1.3	V		det
	V _{OL}	Thevenin output low level	-50	-	50	mV		Un
du	Z _{OLP}	Output impedance of LP transmitter	50	-	-	Ω	1 fine	
1efine	MIPI DSI LP	-RX Mode		•	·	dui		
unoc	V _{IH}	Logic 1 input voltage	880	-		mV		1
ined unde	V _{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV		-
	V _{HYST}	Input hysteresis	25	- stin	-	mV]
	VIHCD	Logic 1 Contention threshold	450	UTIOC	-	mV		unde
	VILCD	Logic 0 Contention threshold	define	-	200	mV	Aine	0

LOLP of Londerined underined underined underined rHY s **NOTE:** Deviates from MIPI D-PHY specification Rev 1.0, which has minimum ZOLP of 110 Ω .

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MIPI-Camera Serial Interface (CSI) DC Specification 19.6.2

Table 136. MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage **Parameters**

	Parameters			1	1	1		der
	Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes	
d une	I _{LEAK}	Pin Leakage current	-10		10	μA	in-	
stineu	MIPI-CSI H	S-RX Mode		<u> </u>	2	uno		
ined undefined une	V _{CMRX(DC)}	Common-mode voltage HS receive mode	70	-	330	mV	1	
	V _{IDTH}	Differential input high threshold	-	7 AU.	70	mV		
	V _{IDTL}	Differential input low threshold	-70	- ~	-	mV		ec
	V _{IHHS}	Single-ended input high voltage	<u> 96</u>	-	460	mV	ſ	retim
	V _{ILHS}	Single-ended input low voltage	-40	-	-	mV		no-
d unde	V _{TERM-EN}	Single-ended threshold for HS termination enable	-	-	450	mV	tinec	
	Z _{ID}	Differential input impedance	80	100	125	Ω		
tined undefined uns	MIPI-CSI L	P-RX Mode			sine			
. ned t	$V_{\rm IH}$	Logic 1 input voltage	880		pe-	mV		
	V _{IL}	Logic 0 input voltage, not in ULP state	-	ed-	550	mV		
	V _{IL-ULPS}	Logic 0 input voltage, ULP state	195K	-	300	mV		sine
	V _{HYST}	Input hysteresis	25	-	-	mV		der

19.6.3

SDIO DC Specification

Table 137 provides the SDIO DC Specification, for all other DC Specifications not listed in this table, refer to Table 160.

Table 137. SDIO DC Specification

	Specification			stined	une		ed u
Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes	defille
V _{OH}	Output High Voltage	1.4	ne <u>o</u>	-	V	Measured at I _{OH} maximum.	d une
I _{OH/} I _{OL}	Current at VoL/Voh	d ur-2	-	-	mA	inden	-

defined un 19.6.4 SD Card DC Specification

A undefined undefined undefined Table 138 provides the SD Card DC Specification, for all other DC Specifications not in a modefined undefined u listed in in this table, refer to Table 160.

Table 138. SD Card DC Specification

<i>Ve.</i>	ind	etine	define	ð ⁻		defined un
intel	nedt		undefined undefine	Electrical Spec	ifications	9e.
ed unde		C Specification		undefined unde		
	Symbol	Parameter	Min.	Max.	Unit	ndefined u
-	V _{REF}	I/O Voltage	SDIO_V3P3A	_V1P8A_G3		defin
.8	V _{OH(3.3)}	Output High Voltage	0.75*V _{REF}	_	vo	
afined undefined und	V _{OL(3.3)}	Output Low Voltage	under -	0.125*V _{REF}	v	
4 undern.	V _{IH (3.3)}	Input High Voltage (3.3 V)	0.625*V _{REF}	V _{REF} +0.3	V	
stinec	V _{IL (3.3)}	Input Low Voltage (3.3 V)	VSS-0.3	0.25*V _{REF}	V	ndefined
	V _{OH(1.8)}	Output High Voltage	1.40	_	V	
	V _{OL(1.8)}	Output Low Voltage	aned und	0.45	V	Inger.
efined undefined une	V _{IH (1.8)}	Input High Voltage (1.8 V)	1.27	2.00	efiver	
indefine	V _{IL (1.8)}	Input Low Voltage (1.8 V)	VSS-0.3	0.58	V	
med u	I _{OH/} I _{OL}	Current at VoL/Voh	-2	10 ⁽²⁾	mA	
efili	C _{LOAD}	total Load Capacitance	-	ed 40	pF	
defined undefined un	define	undefined undefine	ed undefined s	ined undefined ut	defined	undefine
etimed undefined un defined undefined un defined undefined un adefined undefined u	Indefine	Jundefined undefin	ned undefined unde	stimed undefined t	Datasheet	d undefin
offined un.		red unde		d undefil.		



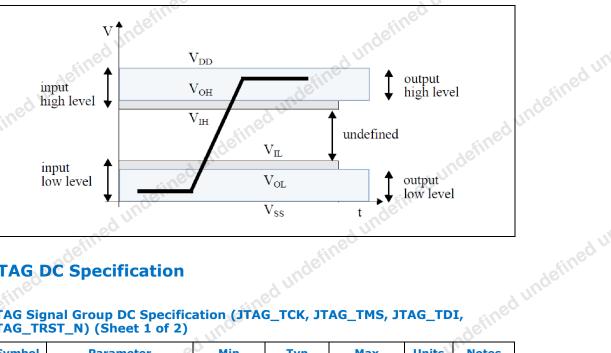
ndefined unde eMMC 4.51 DC Specification 19.6.5

Min Units Symbol Parameter Max GPIOSE V1P8A G3 V_{REF} I/O Voltage V_{REF} - 0.45 VOH Output HIGH voltage V _ 0.45 V Output LOW voltage Vol 0.65 * V_{REF} Input HIGH voltage V_{REF} + 0.3 V V_{IH} V_{IL} Input LOW voltage -0.3 0.35 * V_{REF} V C_L Bus Signal Line 30 pF _ capacitance \mathbf{I}_{IL} Input Leakage Current -10 10 μA IOL Output Leakage Current -10 10 μA

Table 139. eMMC 4.51 DC Electrical Specifications

NOTE: This buffer reaches VOH/VOL with 3mA load.

Figure 37. eMMC 4.51 DC Bus Signal Level



undefined undefined und **JTAG DC Specification**

Table 140. JTAG Signal Group DC Specification (JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TRST_N) (Sheet 1 of 2)

								-
indefinec	Symbol	Parameter	O Min	Тур	Max	Units	Notes	
unc	V _{REF}	I/O Voltage	GP:	ION_V1P8A	G3	in		
	$V_{\rm IH}$	Input High Voltage	0.75*V _{REF}		. uno-	V	1	
	V_{IL}	Input Low Voltage			0.35*V _{REF}	V	2	- 61
	R _{wpu}	Weak Pull Up Impedance	2.5	5	7.5	kΩ	3	sinet
, ur	defineo		odefin	led un			efine	d unde
Datasheet			dull.				255	
unden		med undefin			d und	efined		

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lefined undefined undefined Table 140. JTAG Signal Group DC Specification (JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TRST_N) (Sheet 2 of 2)

	Symbol	Parameter	Min	Тур	Max	Units	Notes	ined -
	R _{wpd}	Weak Pull Down Impedance	2.5	d un5	7.5	kΩ	3	Indetty
a un	R _{wpu-20K}	Weak Pull Up Impedance 20K	12		28	kΩ	4e ⁶¹	
definer	R _{wpd-40K}	Weak Pull Down Impedance 40K	20		70	kΩ	4	
whited undefine	NOTES:	unde			~9e			
define		defined as the minimum volta high value.	age level at	a receiving ag	ent that wil	ll be interpr	reted as a	
	2. V _{IL} is d	lefined as the minimum volta low value.	age level at	a receiving ag	ent that will	l be interpr	eted as a	fined .

NOTES:

- undefined undefined un 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at GPIO V1P8A G3.
- 4. Rwpu_40k and Rwpd_40k are only used for JTAG_TRST#.
- 5. This buffer reaches VOH/VOL with 3mA load.

Table 141. JTAG Signal Group DC Specification (JTAG_TDO)

CAN STREET								
ndein	Symbol	Parameter	Min	Тур	Мах	Units	Notes	
ed un	V _{REF}	I/O Voltage	GI	PION_V1P8A	A_G3	e		-
indefined undefin.	V _{IH}	Input High Voltage	0.75*V _{RE} F		cined un	V	1	od un
U.	V _{IL}	Input Low Voltage		.6	0.45*V _{REF}	V	2	fine
	Z _{pd}	Pull down Impedance	17.5	dun	35	Ω	3	inde
	R _{wpu}	Weak Pull Up Impedance	12	Ver	28	kΩ	3	edu
indefined undefined u	R _{wpd}	Weak Pull Down Impedance	20		70	kΩ	3611	
ndetti	NOTES:	18fin	2-			ined		_
nedu		lefined as the minimum vol high value.	tage level at	t a receiving	agent that w	ill be inter	preted as a	3
ndefit	2. V _{IL} is d	efined as the minimum volt low value.	age level at	a receiving	agent that wi	ll be inter	preted as a	-d u
u.		ed at GPIO_V1P8A_G3. Iffer reaches VOH/VOL with	3mA load.	Ind	Jett.			definee

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- ined undefined u 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at GPIO_V1P8A_G3.
- 4. This buffer reaches VOH/VOL with 3mA load.

Table 142. JTAG Signal Group DC Specification (JTAG_PRDY#, JTAG_PREQ#)

					-			
60	Symbol	Parameter	Min	Тур	Max	Units	Notes	
efined undefined	V _{REF}	I/O Voltage	GPIC	DN_V1P8A_	G3		d un	
unoc	V _{IH}	Input High Voltage	0.75*V _{REF}			V	1	
	V _{IL}	Input Low Voltage			0.45*V _{REF}	V	2	
	Z _{pd}	Pull down Impedance	17.5		35	Ω	3	
	R _{wpu}	Weak Pull Up Impedance	2.5	5	7.5	kΩ	3	d undefine
	defi	ne.		fined .				ned unc
256	d under		ed unde				Datash	eet
aned undefine		d und	efined unde			ndefin		
SULL					~~~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~			



NOTES:

- defined undefined undefined undefined 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at GPIO V1P8A G3.
- This buffer reaches VOH/VOL with 3mA load.

19.6.7 DDR3L-RS Memory Controller DC Specification

Table 143. DDR3L-RS Signal Group DC Specifications

Symbol	Parameter	Min	Туре	Max	Units	Notes	nı,
V _{IL}	Input Low Voltage		odefine	DDR_VREF - 200mV	V	1	Lefined un
VIH	Input High Voltage	DDR_VREF + 200mV	sined un		V	2, 3	mae
V _{OL}	Output Low Voltage	ed u	(DDR_VDDQG_S4 / 2)* (RON / (RON+RVTT_TERM))		a ur	3,4	
V _{OH}	Output High Voltage	defit	DDR_VDDQG_S4 - ((DDR_VDDQG_S4 / 2)* (RON/ (RON+RVTT_TERM))	ed undefi	NC V	3,4	tined ut
IIL	Input Leakage Current		ed under	5	μA	For all DDR Signals	undefine
R _{ON}	DDR3L-RS Clock Buffer strength	26	undefin	40	Ω	ndefine	
C _{IO}	DQ/DQS/DQS# DDR3L-RS IO Pin Capacitance	ndefines	3.0	def	n ^{pE}		

NOTES:

- 1. V_{IL} is defined as the maximum voltage level at the receiving agent that will be received as a logical low value. DDR VREF is normally DDR VDDQG S4
- V_{IH} is defined as the minimum voltage level at the receiving agent that will be received as a logical high value. DDR_VREF is normally DDR_VDDQG_S4
- 3. V_{IH} and V_{OH} may experience excursions above DDR_VDDQG_S4. However, input signal drivers must comply with the signal quality specifications.
- RON is DDR driver resistance whereas RTT TERM is DDR ODT resistance which is controlled by 4. DDR.
- 5. DDR3L-1333 CLK buffer Ron is 260hm and SR target is 4V/ns; DQ-DQS buffer Ron is 300hms and SR target is 4V/ns; CMD/CTL buffer Ron is 200hms and SR target is 1.8V/ns. undefined undefined undefined

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LPDDR3 Memory Controller DC Specification 19.6.8

	Symbol	Parameter	Min	Тур	Мах	Units	Notes	Inder
	DDR_VDDQG_S4	I/O Supply Voltage	1.14	1.24	1.26	V	. neò	
efined undefined ut	V _{IL}	Input Low Voltage	unde		DDR_VRE F - 200 mV	o v de	SU.	
ed und	V _{IH}	Input High Voltage	DDR_VREF + 200 mV		ndefine	V		
Stille	V _{OL}	Output Low Voltage	-	0.260	<u> </u>	V	1,2	
	V _{OH}	Output High Voltage	-	0.960	-	V	1,2	
	IILOU	Input Leakage Current	- 6	ino 5	-	μA	3,4	undefin
	R _{ON}	Clock Buffer strength	26		40	Ω	ec	
-01	C _{IO}	IO Pin Capacitance	INOL	3.0		pF	elli	
Jefined undefinee	test load. 2. LPDDR3-10 400hms an	_H is determined with 400 966 CLK buffer Ron is 35 ad SR target is 2V/ns; Cl the pin to VCC or VSS lea	Ohm and SR tar MD/CTL buffer R	get is 2.5V/ns	s; DQ-DQS b	uffer Ro	n is	

Table 144. LPDDR3 Signal Group DC Specifications

NOTES:

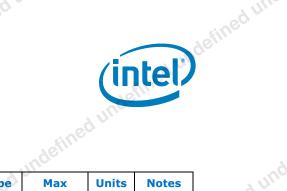
- 1. V_{OL} and V_{OH} is determined with 400hm buffer strength setting into a 600hm to 0.5x V1p5_ddr test load.
- d undefined undefined un 2. LPDDR3-1066 CLK buffer Ron is 350hm and SR target is 2.5V/ns; DQ-DQS buffer Ron is 400hms and SR target is 2V/ns; CMD/CTL buffer Ron is 300hms and SR target is 1.5V/ns. 3. Applies to the pin to VCC or VSS leakage current.
- 4. Applies to the pin to pin leakage current.

USB 2.0 Host DC Specification

Table 145. USB 2.0 Host DC Specification (Sheet 1 of 3)

unde	Symbol	Parameter	Min	Туре	Max	Units	Notes	
Jefined under 143.	Supply Vo	ltage			4 UNOS			
9e.	VBUS	High-power Port	4.75	61	5.25	V	2	d V
	VBUS	Low-power Port	4.20	"ger	5.25	V		efine
	Supply Cu	rrent	d	U				d undefined "
	ICCPRT	High-power Hub Port (out)	500			mA	0 is	
d	ICCUPT	Low-power Hub Port (out)	100			mA	der	
1efine	ICCHPF	High-power Function (in)			500	mA	011	
unos	ICCLPF	Low-power Function (in)			100	mA		
ndefined undefined	ICCINIT	Unconfigured Function/Hub (in)			100	mA		
	ICCSH	Suspended High-power Device			2.5	mA	15	ned
	ICCSL	Suspended Low-power Device		nde	500	μA		defille
	defin	60	sine	9.0				ed undefined
258	d une	aned undefined	unde				Datasheet	
, undefin		adefine				efined		
Lefineo		ined un.			d un			

19.6.9



Symbol	Parameter	Min	Туре	Max	Units	Notes
Input Lev	els for Low-/full-speed		Jetti,		1	<u>ı</u>
VIH	High (driven)	2.0			V	4
VIHZ	High (floating)	2.7		3.6	V	4
VIL	Low	-		0.8	V	4
VDI	Differential Input Sensitivity	0.2		undefin	ed un	(D+)- (D-) ;Figure ; Note 4
VCM Input Lev VHSSQ	Differential Common Mode Range	0.8 JI	define	2.5	v	Includes VDI range; Figure; Note 4
Input Lev	els for High-speed				nı,	0.0
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100		150	mV	
VHSDSC	High speed disconnect detection threshold (differential signal amplitude)	525	ndefine	625	mV	
definer	High-speed differential input signaling levels	fined t	P	-		16
VHSCM	High-speed data signaling common mode voltage range (guideline for receiver)	-50		500	mV	define
Output Le	evels for Low-/full-speed			S.	ner	
VOL	Low	0.0		0.8	V	4,5
VOH	High (Driven)	2.8		3.6	V	1.6
VOSE1	SE1	0.8	derit		V	
VCRS	Output Signal Crossover Voltage	1.3 4100		2.0	V	4,6
Output Le	evels for High-speed:	nde.				define
VHSOI	High-speed idle level	-10		10	mV	n.
VHSOH	High-speed data signaling high	360		440	mV	
VHSOL	High-speed data signaling low	-10		10	mV	
VCHIRPJ	Chirp J level (differential voltage)	700	- Fil	1100	mV	
undefine	voltage)	Indefined	UNOC		sined	undefine 259

defined undefined undernned ndefined undefined Table 145. USB 2.0 Host DC Specification (Sheet 2 of 3)

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Symbol	Parameter	Min	Туре	Max	Units	Notes
VCHIRPK	Chirp K level (differential voltage)	-900	ndern	-500	mV	
Decouplin	g Capacitance:	sines				ed
СНРВ	Downstream Facing Port Bypass Capacitance (per hub)	120			μF	detine
CRPB	Upstream Facing Port Bypass Capacitance	1.0		10.0	¢ΨF	9
Input Cap	oacitance for Low-/full-speed:			, unos	•	
CIND	Downstream Facing Port			150	pF	2
CINUB	Upstream Facing Port (w/o cable)		Indetti	100	pF	3
CEDGE	Transceiver edge rate control capacitance	definet		75	pF	lefine
Input Im	pedance for High-speed:	*			<i>U</i> ,	000
	TDR spec for high-speed termination			10	ineo	
Terminati	ons:			dune	1	1
RPU	Bus Pull-up Resistor on Upstream Facing Port	1.425	ndefin	1.575	kΩ	1.5 kΩ ±5%
RPD	Bus Pull-down Resistor on Downstream Facing Port	14.25		15.75	kΩ	1.5 kΩ ±5%
ZINP	Input impedance exclusive of pull-up/pull-down (for low-/full speed)	300			kΩ	ndefili
VTERM	Termination voltage for upstream facing port pull-up (RPU)	3.0	13-	3.6	V	
Terminati	ons in High-speed:		nde			
VHSTERM	Termination voltage in high speed	-10		10	mV	
RTERM	High Speed Termination	40	45	50	Ω	dem
VBUSD	VBUS Voltage drop for detachable cables	-	-	1	mV	nı.
 Measu Measu Measu 	detachable cables ured at A plug. ured at A receptacle. ured at B receptacle. ured at A or B connector. ured with RL of 1.425 kΩ to 3.6 V.	undefine	d undef	ined und	,e,	Datashee
	ined under			od un	defined	

Jefined undefined undefined USB 2.0 Host DC Specification (Sheet 3 of 3) **Table 145.**

NOTES:

- 1. Measured at A plug.
- 2. Measured at A receptacle.
- 3. Measured at B receptacle.
- 4. Measured at A or B connector.
- Me Me 5. Measured with RL of 1.425 k Ω to 3.6 V.



- 6. Measured with RL of 14.25 k Ω to GND.
- 7. Timing difference between the differential data signals.
- 8. Measured at crossover point of differential data signals.
- undefined und 9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330 mV.
- 10. Excluding the first transition from the Idle state.
- 11. The two transitions should be a (nominal) bit time apart.
- 12. For both transitions of differential signaling.
- 13. Must accept as valid EOP.
- 14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors .
- 15. For high power devices (non-hubs) when enabled for remote wakeup. red undefined
- 16. Specified by eye pattern templates.

Indefined undefined **USB HSIC DC Specification** 19.6.10

USB HSIC DC Electrical Specifications Table 146. undefined undefined

	SIC DC Specificat	ned un		thed w	Indefined
Symbol	Parameter	Min	Max	Units	
V _{REF}	I/O Voltage	USBHSIC_\	/1P2A_G3		
V _{OH}	Output HIGH voltage	0.75 * V _{REF}	10111 <u>-</u>	V	
V _{OI}	Output LOW voltage	-	0.25 * V _{REF}	V	
V_{IH}	Input HIGH voltage	0.65 * V _{REF}	V _{REF} + 0.3	V	6
V _{IL}	Input LOW voltage	-0.3	0.35 * V _{REF}	V	since
OD	I/O Pad Drive Strength	40	60	Ω	nde.
CL	Load capacitance	fine 1	5	pF	
ZI	I/O input impedance	240	-	kΩ	
Τ _Ι	Characteristic Trace Impedance	45	55	Ω	
	0 DC Specificatio DC transmitter specific		ed undefit		
JD 3.U	be transmitter specific	duoiis			

undefined undefined und **USB 3.0 DC Specification**

Table 147. USB 3.0 DC transmitter specifications

19.6.11	USB 3.0 DC	Specification		d unos			
Table 147.	USB 3.0 DC transmitter specifications						
	Symbol	Parameter	Min	Max	Units	Notes	unde
	UI	Unit Interval	199.94	200.06	ps	4 00	
sined un	V _{TX-DIFF-PP}	Differential peak-peak Tx voltage swing	0.8	1.2	V	nderm	1
undefined undefined un	V _{TX-DIFF-PP-LOW}	Low-Power Differential peak- peak Tx voltage swing	0.4	1.2	inev	1	
ein ^{e0}	R _{TX-DIFF-DC}	DC differential impedance	72	92	Ω]
ed under.	V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection	ndefil	0.6	V	2	Jefined '
, ur	Idefinet	odefine	d u.			efine	d unce
Datasheet		d un			4	261	
d undefil.		indefinec			efined		
1 efiner		ined v.		d unc			

(intel) red underme

Electrical Specificat	ons
Symbol Parameter Min Max Units Not	
Cue esure AC Coupling Capacitor 75 200 pE 3	es
C _{AC-COUPLING} AC Coupling Capacitor 75 200 nF 3	d u
T _{CDR-SLEW-MAX} Maximum slew rate 10 ms/s	efine
C _{TX-PARASITIC} Tx input capacitance for return - 1.25 pf 5	d unde
Eye Height 100 1200 mV 7,)
Eye Height1001200mV7,DjDeterministic Jitter-0.43UI7,8RjRandom Jitter-0.23UI6,7,8TjTotal Jitter-0.66UI7,8	,9
Rj Random Jitter - 0.23 UI 6,7,8	,10
Tj Total Jitter - 0.66 UI 7,8	,9

- undefined und 1. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for
- - 10. The Rj spec is calculated at 14.069 times the RMS random jitter for 10^{-12} BER.

Table 148. USB 3.0 DC LFPS specifications

ndefinec	 Measured after r Measured at the The eye height i 	.0° consecutive UI and extrapolat receiver equalization function. end of reference channel and cal s measured at the maximum ope alculated at 14.069 times the RMS	bles at TP1. ning.	hed und			undefined un
	USB 3.0 DC LFP	S specifications	d un				unde
d un	Symbol	Parameter	Min	Max	Units	Notes	
lefine.	T _{PERIOD}	neo	20	100	ns		
Inde	V _{CM-AC-LFPS}	defini	-	10	mV		
a undefined undefined un	V _{CM-AC-LFPS-} ACTIVE	redune	-	10,00	mV		
J unde	V _{TX-DIFF-PP-LFPS}	peak-peak Differential amplitude	0.8	1.2	V		fined U
-	V _{TX-DIFF-PP-LFPS-LP}	Low power peak-peak Differential amplitude	0.4	0.6	V		d under
	T _{RISEFALL2080}	defin	-	4	ns	nin	
ed v	Duty cycle	d une	40	60	%	uge.	
Indefilit	C _{TX-PARASITIC}	Tx input capacitance for return loss	-	1.25	pf	0.	
262 Letined undefined	Indefined unde	stimed undefined undefin	ned unde	tined und	0	Nije.	ed undefined
262 Lindefined		aned undefined unc		d un	defined	Datasheet	



ndefined undefined Table 149. USB 3.0 DC Receiver specifications

d undefined un Table 149.	USB 3.0 DC Rec	eiver specifications	-6	JUNOR		
	Symbol	Parameter	Min	Max	Units	Notes
	UI	Unit Interval	199.94	200.06	ps	1
	R _{RX-DC}	Receiver DC common mode impedance	18	30	Ω	2 11
d un.	R _{RX-DIFF-DC}	DC differential impedance	72	120	Ω	3
ed undefined undef	Z _{RX-HIGH-IMP-} DCPOS	DC input CM input for V>0 during reset or power down	25	-	kΩ	4
ed un.	V _{RX-LFPS-DETDIFFp} -	LFPS detect threshold	100	300	mV	
	f1	tolerance corner	- vec	4.9	MHz	
	J _{RJ}	Random Jitter	76 <u>-</u> 111	0.0121	UI rms	1
	J _{RJP-P}	Random Jitter peak-peak at 10 12	<u>, </u>	0.17	UI p-p	1,4 ndf
indi	Sj @0.5MHz	Sinusoidal Jitter	-	2	UI p-p	1,2,3
	Sj @1MHz	Sinusoidal Jitter	-	1	UI p-p	1,2,3
Aefine	Sj @2MHz	Sinusoidal Jitter	-	0.5	UI p-p	1,2,3
uno	Sj @f1MHz	Sinusoidal Jitter	-	0.2	UI p-p	1,2,3
	Sj @50MHz	Sinusoidal Jitter	-	0.2	UI p-p	1,2,3
red undefined unde	V_full_swing	transition bit differential voltage swing	etine	0.75	V р-р	1
	V_EQ_level	Non transition bit voltage (equalization)	unoe	-3	db	1

NOTES:

- 2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. however, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
- Jundefined undefined und undefined undefi 3. During the Rx tolerance test, SSC is generated by test equipment and present all the time.

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19.6.12

Table 150. SSIC DC Specification

Ter.	undefine		- 2	stined			stined un
intel	ned L	adet	ined unc		Electrical	Specific	cations
undefill		adefined un			defined	unde	
etin,	SSIC DC Specific			lefined u	no		tined un
	Symbol	Parameter	Min.	Nom.	Max.	Unit	under
roed und	R _{REF_RT}	Reference load for when the Transmitter is terminated.	fine	100		Ω Indef	ned
offined undefin	R _{REF_NT}	Reference load for when the Transmitter is not terminated.	10		ndefined	kΩ	
9e.	ZR	Reference impedance.		100		Ω	uned v
ed undefined un	V _{DIFF_DC_LA_RT_TX}	Large Amplitude differential TX DC voltage when the Transmitter is terminated. Defined for $R_{REF_RT}^1$ and test pattern ²	160 un	96.	240	mV	tined undefine
ndefilit	V _{DIFF_DC_LA_NT_TX}	Large Amplitude differential TX DC voltage when the Transmitter is not terminated. Defined for $R_{REF_NT}^3$ and test pattern ²	320	ndefined	480	mV	undefined
Indefined undefined un	VDIFF_DC_SA_RT_TX	voltage when the Transmitter is terminated. Defined for	100		130	mV	etined unde
	V _{DIFF_DC_SA_NT_TX}	R _{REF_RT} ¹ and test pattern ² Small Amplitude differential TX DC voltage when the Transmitter is not terminated. Defined for R _{REF_NT} ³ and test pattern ²	200	Indefined	260	mV	stined undefined
ndefined undefined		stined undefined un	•	ine	d undefil	led un	00
undefined undefined u	Indefined uno	du	ndefined	unden		Dat	tasheet
Lefined undern		aned undefines			od undefi	ined t	





Table 150. SSIC DC Specification

Table 150.	SSIC DC Specifi	cation			Jefined un	<i>le</i>	2
defill	Symbol	Parameter	Min.	Nom.	Max.	Unit	dunc
r.	V _{CM_LA_TX}	Large Amplitude common-mode TX voltage. Defined R _{REF_RT} ¹ and test pattern ²	160		260	mV	ed undefinee
undefined undefin.	V _{CM_SA_TX}	Small Amplitude common-mode TX voltage. Defined $R_{REF_RT}^1$ and test pattern ²	80	stined un	190	mV	ined unr
	C _{PIN_RX}	PIN Capacitance	-d-uno	0	1.5	pF	undefill

NOTES:

- 1. External reference load $R_{REF_{RT}}$ and a reference impedance $Z_{REF_{RT}}$ that conform to $SRL_{REF_{RT}}$ (return loss of Z_{REF_RT}).
- 2. Defined when driving both a DIF-N and a DIF-P LINE state.
- 3. External reference load R_{REF_NT} and capacitances at TXDP and at TXDN within the limit of C_{PIN_RX}.

undefined undefined 19.6.13 LPC DC Specification

Table 151. LPC 1.8V Signal Group DC Specification undefined undefined un

PC 1.8V	/ Signal Group DC S	Specification	unde	ned unde			undefined
Symbol	Parameter	Min	Тур	Max	Units	Notes	
V_{IH}	Input High Voltage	1.5	1.8	1.8 +0.5	VÒ	8	
V_{IL}	Input Low Voltage 🔬	-0.5	0	0.8	δV		
V _{OH}	Output High Voltage	0.9 x 1.8		76tu	V		
V _{OL}	Output Low Voltage			0.1 x 1.8	V		
I _{OH}	Output High Current		0.5	neo	mA		
I _{OL}	Output Low Current		-1.5		mA		
I _{LEAK}	Input Leakage Current	-10	dun	10	μA		under
C _{IN}	Input Capacitance	Yellin		10	pF	sines	

Table 152. LPC 3.3V Signal Group DC Specification (Sheet 1 of 2)

20								_
UI.	Symbol	Parameter	Min	Тур	Max	Units	Notes	
	V_{IH}	Input High Voltage	2.0	3.3	3.3 +0.5	V	1	
	V_{IL}	Input Low Voltage	-0.5	0	0.8	V	2	ed '
	V _{OH}	Output High Voltage	2.5	inde		V	3	defill
Datasheet	Idefine	ed undefin	ed undefit	^{led}	unde	stined	underine 265	d une
		Onis			20			A

.she

indefined unde



	Symbol	Parameter	Min	Тур	Max	Units	Notes
	V _{OL}	Output Low Voltage		der	0.4	V	3
	I _{ОН}	Output High Current		0.5		mA	3
6	I _{OL}	Output Low Current	sine	-1.5		mA	3 0
00.	I_{LEAK}	Input Leakage Current	-10		10	μA	76 ₍₁₁₎
	C_{IN}	Input Capacitance	V .		10	pF	5

Table 152. LPC 3.3V Signal Group DC Specification (Sheet 2 of 2)

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a tefined undefined undefined un logical high value, Applies to LPC_AD[3:0], LPC_CLKRUN_N.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value. Applies to LPC_AD[3:0], ILB_LPC_CLKRUN_N.
- 3. V_{OH} is tested with Iout=500uA, V_{OL} is tested with Iout=1500uA.
- 4. Applies to LPC AD[3:0], LPC CLKRUN N and LPC FRAME N.
- 5. LPC_SERIRQ is always a 1.8V I/O irrespective of the value of LPC_V1P8V3P3_S4.

19.6.14 SPI and FST_SPI DC Specification

Table 153. SPI and FST_SPI Signal Group DC Specification

					AC.			-
defined	Symbol	Parameter	Min	Тур	Мах	Units	Notes	
	V _{REF}	I/O Voltage	G	PIOSE_1P8A_	G3	V	3	edv
	V _{IH}	Input High Voltage	0.65 * V _{REF}	de.		V	2	1 efine
	V _{IL}	Input Low Voltage	-0.5	00	0.35 * V _{REF}	V	2	Inoc
	VOH	Output High Voltage	V _{REF} - 0.45		1.8V	V	1	ed t
24	V _{OL}	Output Low Voltage	nde		0.45	V	1	
	I _{OH}	Output High Current	90		2	mA	1	
ader.	I _{OL}	Output Low Current	-2			mA	1	
undefined undefined u	NOTES:	d unoc			inde			-
defill	1. Applies	to SPI1_CS[1:0], SPI1_CL to SPI1_MISO and SPI1_M		•	du			2
	3. The I/C inclusiv	buffer supply voltage is more of all noise from DC up to bandwidth limited oscillosco	easured at the 20 MHz. In te	esting, the v	oltage rails sh	ould be r	neasured	

NOTES:

- 1. Applies to SPI1_CS[1:0], SPI1_CLK, SPI1_MOSI.
- 2. Applies to SPI1_MISO and SPI1_MOSI.
- in a makelined undefined u 3. The I/O buffer supply voltage is measured at the SoC package pins. The tolerances shown are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz. 4. A undefined undefined und
 - oaa o naa undefined undefi 4. This buffer reaches VOH/VOL with 3mA load.



ndefined u

Power Management/Thermal (PMC) and RTC DC 19.6.15 Specification

Table 154. Power Management Signal Group DC Specification Indefined undefined unde

	Management/Th ication	iermal (F	MC) an	nd RTC E	C		Jeffined und
Power Ma Symbol	lanagement Signal Gro Parameter	Dup DC Spec	cification Typ	Мах	Units	Notes	ndetti.
V _{REF}	I/O Voltage	GP	IOSE_1P8A_0	G3	V	stine	-
V _{IH}	Input High Voltage	0.65 * V _{REF}	l		V	2	1
V _{IL}	Input Low Voltage	-0.5		0.35 * V _{REF}	e ^o v	2,3	1
V _{OH}	Output High Voltage	V _{REF} - 0.45		1.8V	V	1	-
V _{OL}	Output Low Voltage	i – – – – – – – – – – – – – – – – – – –		0.45	V	1	
I _{OH}	Output High Current	1	0	2	mA	1	d ui
I _{OL}	Output Low Current	-2	den		mA	1	etine

NOTES:

- 1. The data in this table apply to signals PMC ACPRESENT, PMC BATLOW N, PMC PLTRST N, PMC_PWRBTN_N,PMC_SLP_S4_N, PMC_SUS_STAT_N, PMC_SUSCLK[3:0], PMC_SUSPWRDNACK
- 2. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
- 3. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 4. This buffer reaches VOH/VOL with 3mA load.

Table 155. PMC_RSTBTN# 1.8V Core Well Signal Group DC Specification

	Symbol	Parameter	Min	Тур	Мах	Units	Notes	unoc
	VREF	I/O Voltage	UN	CORE_V1P8	3_G3	V	ane ⁰	
du'	V _{IH}	Input High Voltage	0.65* VREF			V	001	
afine	V _{IL}	Input Low Voltage			0.35* VREF	V V	2	
d unoc	NOTES:	ndefin			194	Inec		
		lefined as the minimum volt high value.	age level at a	receiving	agent that will	be interp	reted as a	
10 ⁶¹	2. V _{IL} is d	efined as the minimum volt	age level at a	receiving a	agent that will l	be interpr	eted as a	
		low value.		ndet				26

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value?
- 2. V_{II} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 156. Power Management and RTC Well Signal Group DC Specification

2	Symbol	Parameter	Min	Тур	Мах	Units	Notes
	VREF	I/O Voltage	RTC_	V3P3R	TC_G5		der.
	V_{IH}	Input High Voltage	2.0	-	-	V	1
	V_{IL}	Input Low Voltage	-	-	0.78	V	2

NOTES:

- A undefined undefined undefined 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value. is and undefined undefin



Table 157. RTC Well DC Specification

	undefin	led II.			ned uno		
	DC Specification			tined unt		1	d und
Symbol	Parameter	Min	Тур	Max	Units	Notes	sine
V _{IH}	Input High Voltage	2.3	Un	-	V	1	nder.
V _{IL}	Input Low Voltage	- sinet	-	0.78	V	2 0	71.

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 158. PROCHOT# Signal Group DC Specification

	Symbol	Uno Parameter	Min	Туре	Max	Units	Notes	Stine
	V _{REF}	I/O Voltage	GPI	ON_V1P8	A_G3			unde
	VIH	Input High Voltage	0.75*V _{REF}		V _{REF}	V	1.00	
du	V _{IL}	Input Low Voltage	Inos		0.45*V _{REF}	V	2	
	V _{OL}	Output Low Voltage	jo -		0.35 * V _{REF}	V		
nde	I _{OL}	Output Low Current			-5	mA		
stined un	NOTES:	, une		•	de		<u> </u>	

NOTES:

- red undefined 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. This buffer reaches VOH/VOL with 3mA load.

19.6.16 SVID DC Specification

Table 159. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT_N)

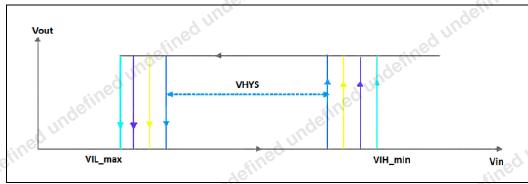
undefined	Symbol	Parameter	Min	Тур	Max	Units	Notes	
inde	V _{REF}	I/O Voltage	GPIC	N_V1P8	A_G3			d undefined u
	V _{IH}	Input High Voltage	0.65*V _{REF}		9er.	V	1	1efine
	V _{IL}	Input Low Voltage		0 V.	0.35*V _{REF}	V	1	unos
	V _{OH}	Output High Voltage	V _{REF} - 0.45	10	V _{REF}	V	1	ned t
0 b	V _{OL}	Output Low Voltage	inos		0.45	V	4	
stine	V _{HYS}	Hysteresis Voltage	0.1			V	d un	
Inde	R _{ON}	BUffer on Resistance	40		60	Ω	2	
ed undefined undefined u	ΙL	Leakage Current	-10		10	μA	3	
defille	C _{PAD}	Pad Capacitance			9 0	pF	4	
I UNC	V _{PIN}	Pin Capacitance			10	pF		ine ⁰
<i>,</i> 0	Z _{pd}	Pull down Impedance	35	50	70	Ω		detin
268	undefint	,	undef	Ineo			Datash	eet
268 undefined		aned undef	Ineo C			undefil	hed un	



NOTES:

- 1. GPIO_V1P8A_G3 refers to instantaneous voltage VSS_SENSE.
- 2. Measured at 0.31 * GPIO V1P8A G3.
- 3. V_{IN} between 0V and GPIO_V1P8A_G3.
- 4. CPAD includes die capacitance only. No package parasitic included.
- 5. This buffer reaches VOH/VOL with 3mA load.

Figure 38. Definition of VHYS



19.6.17 **GPIO DC Specification**

GPIO Buffer DC specifications.

Table 160. GPIO 1.8V Core Well Signal Group DC Specification

defined ^L Table 160.	Symbol	BV Core Well Signal Gr Parameter	Min	Тур	Мах	Units	Notes	ine ⁰
ndefined undefined und	V _{REF}	I/O Voltage		ON_V1P8A DSE_V1P8A			6	undefined
un ^c	V _{IH}	Input High Voltage	0.65*V _{REF}			V	etime	
	V _{IL}	Input Low Voltage	U.		0.35 * V _{REF}	V	100	
	V _{OH}	Output High Voltage	V _{REF} - 0.45		V _{REF}	V		
dune	V _{OL}	Output Low Voltage			0.45	V		
	V _{Hys}	Input Hysteresis	0.1		4 UN	V		
nde.	IL	Leakage Current	-10	¢.	10	mA		
	CLOAD	Load Capacitance	2	9e,	75	pF		fine
efined un	NOTE: Thi	s buffer reaches VOH/VOL v	with 3mA load	90.		-d ^w	Indefined	unc.
Indefined undefined un	NOTE: Thi	Output Low Voltage Input Hysteresis Leakage Current Load Capacitance s buffer reaches VOH/VOL v	with 3mA load	d L.	tined unde	tined	Indefined	unc



SIO - I²C DC Specification 19.6.18

Table 161. I²C Signal Electrical Specifications

undefill	SIO I	¹² C DC Specificat	ion		defin	led n.		
Table 161.		al Electrical Specificat		ndefil	led unc	I	Ι	terined un
	Symbol	Parameter	Min	Тур	Max	Units	Notes	UNOC
	AC V	I/O Voltage	GPI	OSE_V1P8/	A G3	V	e ^C	
	V _{REF}	1/O Voltage	0.	—	_			
d un	V _{REF}	Input High Voltage	0.7 * V _{REF}		_	V	detine	
offined un				_	0.3 * V _{REF}	V V	detime	-
undefined un	V _{IH}	Input High Voltage					detin	-
ed undefined un	V _{IH} V _{IL}	Input High Voltage			0.3 * V _{REF}	VU	Jenn	

NOTE: This buffer reaches VOH/VOL with 3mA load.

SIO - UART DC Specification 19.6.19

Refer to GPIO Buffer (1.8V) DC Specification, mentioned Section 19.6.17, "GPIO DC Specification"

I²S (Audio) DC Specification 19.6.20

tundefined undefined un Refer to the GPIO Buffer (1.8V) DC Specification, mentioned Section 19.6.17, "GPIO DC Specification"

PCI Express DC Specification 19.6.21

Table 162. PCI Express DC Receive Signal Characteristics

Symbol	Parameter	Min	Туре	Max	Unit	Notes	
V _{RXDIFF Gen1}	Differential RX Peak to Peak	175		1200	mV	1	
V _{RXDIFF Gen2}	Differential RX Peak to Peak	100		1200	mV	1	
fines	s differential peak to peak = 2*		9	3)			ed undefill
	27.	Gen		Gen 2		defin	1

Table 163. PCI Express DC Transmit Characteristics (Sheet 1 of 3)

6 beech	0 ³⁴	Devenuetor	UNOGe	n 1	Ge	n 2		deth
defille	Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
dune	UI	Unit Interval	399.88	400.12	199.94	200.06	ps	1
defined undefined	V _{TX-DIFF-} PP	Differential p-p Tx voltage swing	800	1200	800	1200	mV	
1.2	V _{TX} -DIFF-LP	Differential TX Peak to Peak (low power mode)	400	1200	400	1200	mV	
270	undefine		undef	ineo			[Datashee
thed undefine		d undefine				indef	ined	011
16th.		sinec				90.		



ndefined undefined

ger.	indf	stine		define	,o				defined un
Electrical Spe	cifications		Jefined U	nu		(in	tel	dett
ndefined undefined unc. Table 163.	PCI Expr	ess DC Transmit Charac	teristics	(Sheet 2	2 of 3)	atined	Inc		
ndefine	Symbol	Parameter	Ge			n 2	Unit	Notes	ed uno
	V _{TX-DE-} RATIO-	Tx de-emphasis level	Min 3 of incode	Max 4	Min 3	Max 4	db	ed u	ndefine
fined une	3.5DB V _{TX-DE-} RATIO-6DB	Tx de-emphasis	-	-	5.5	6.5	db		
ed under	T _{MIN-PULSE}	Instantaneous pulse width	-	-	0.9	efineo	UI		-
undefined undefined unde	T _{TX-EYE}	Transmitter Eye including all jitter sources	0.75	defi	0.75	-	UI		ofined und
und	T _{TX-EYE-} MEDIAN-to MAX-JITTER	Maximum time between the jitter median and max deviation from the median	ndefined	0.125	-	-	undf	2 stined	Inde
afined undefined	T _{TX-HF-DJ-} DD	Tx deterministic jitter > 1.5 MHz	-	-	-	0.15	UI	3	-
indefine	T _{RF-} MISMATCH	Tx rise/fall mismatch	-	-	neāu	0.1	UI		ed un
	T _{TX-RISE} - FALL	Transmitter rise and fall time	-	unde	0.15	-	UI		indefine
ed un	V _{TX-CM-AC-} PP	Tx AC peak-peak common mode voltage	Indefine	-	-	150	mVp p	efined	0.
ed undefine	V _{TX-DC-CM}	Transmitter DC common-mode voltage	0	3.6	0	3.6	V	4	
Sundefined undefined un	V _{TX-CM-DC-} LINEDELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	25	tined v	25	mV		undefined
ed ut	Z _{TX-DIFF-} DC	DC differential Tx impedance	80	120	-	120	Ω	define	P
ed undefine	I _{TX-SHORT}	Transmitter short-circuit current limit	-	90	-	90	mA	5	
Datasheet	2	current limit		'nð	efined	J.L.	•		ed undefined
	ndefineu		defin	led u.				Ain	ed unc
Datasheet		defined	June			undefi	nedu	nd ^{er} 27	1
Astined -		sined une				unde			



10	Symbol	ess DC Transmit Charact	Ge		· · · · · ·	n 2	Unit	Notes	
		Paralleter	Min	Max	Min	Max	Unit	Notes	1etine
ned undefined un	V _{TX-CM} -DC- ACTIVEIDLE -DELTA	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	defined	100	0	100	mV	stined	unoc
ined unor	V _{TX-IDLE} - DIFF-AC-p	Electrical Idle Differential Peak Output Voltage	0	20	0	20,10	mV		
	V _{TX-IDLE-} DIFF-DC	DC Electrical Idle Differential Output Voltage	-	- unde	1110	5	mV		ndefine
	T _{TX-DJ}	Tx deterministic jitter	Rine	-	-	57	ps	ed.	U.
20	T _{TX-RJ}	Tx Random jitter	uge.	-	-	3.41	ps	efille	
indefined	T _{TX-} MEDIAN-to MAX-JITTER	Maximum Transmitter Medium-to-max jitter	-	77	-	- fine	ps	<i>p</i> -	
	T _{TX-TJ}	Total Jitter @ BER 1E-12	-	-	-	105	ps		

Table 163. PCI Express DC Transmit Characteristics (Sheet 3 of 3)

NOTES:

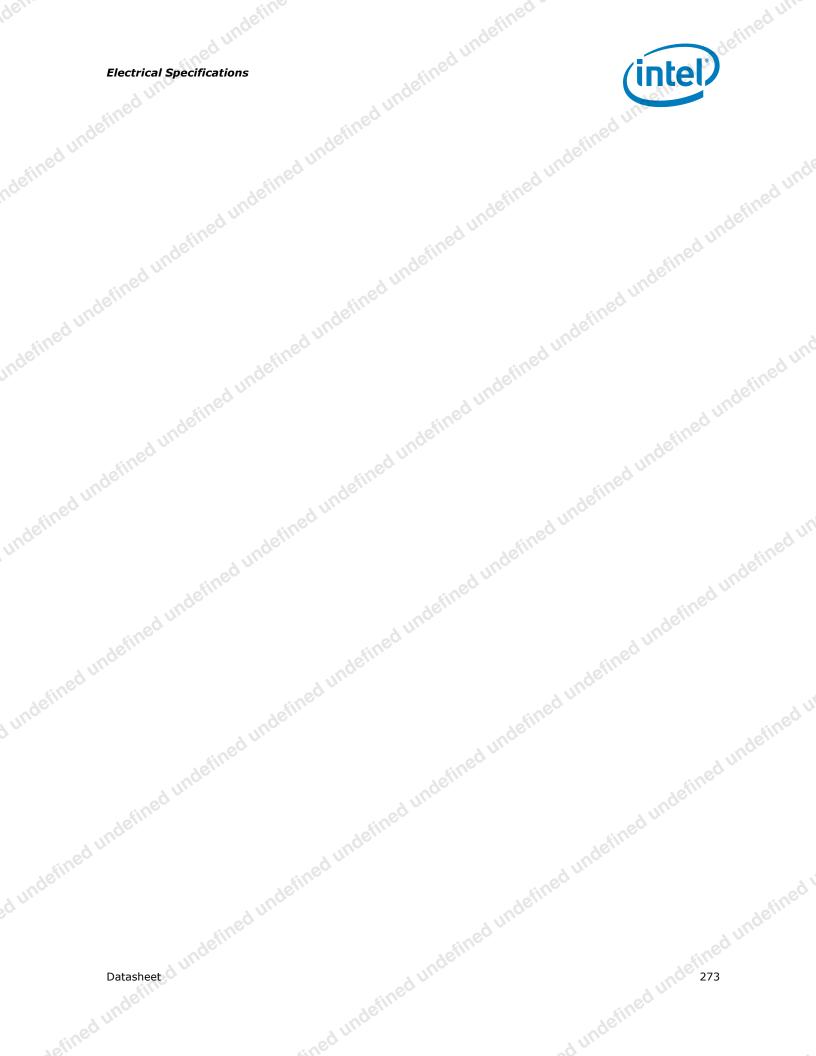
- 1. The specified UI is equivalent to a tolerance of +-300 ppm for each RefClk source. period does not account for SSC induced variations. SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.
- 2. Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function
- 3. Deterministic jitter only
- 4. The allowed DC common-mode voltage at a transmitter pin under any conditions.
- 5. The total single-ended current a transmitter can supply when shorted to ground.

Table 164. PCI Express DC Clock Request Input Signal Characteristics

Symbol	Parameter	Min	Туре	Max	Unit	Notes	
V _{REF}	I/O Voltage	UNC	ORE_V1F	98_S4			
V _{IL}	Input Low Voltage	2	une	0.3*V _{REF}	V	1	
V _{IH}	Input High Voltage	0.65*V _{REF}	P		V	1	90,

NOTE:

1. 3.3 V refers to UNCORE_3P3_S0 for signals in the core well. Refer Chapter 2, "Physical z, ' Interfaces" for signal and power well association. - p.



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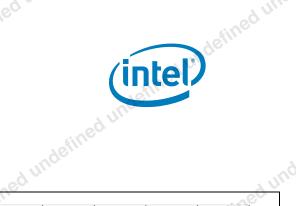
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Ballout and Ball Map 20

20.1 **Ballout**

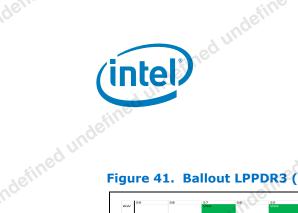
Figure 39. Ballout - DDR3L-RS (T3) Top View Part A

2	0.	1	Ballo	out				efined	UI.				2	unde
l	Figu	ure 39.	Ballout	- DDR3	BL-RS ('	ТЗ) Тор						hon	stined	
2		25	24	23	22	21	20	19	18	17	16	15	14	13
, unu	A	E PWR_RSVD_ BS	0 PWR_RSVD_0	DDR3_M0_DQ3)	UART0_DATAI		I2C6_CLK/NMI_		SD3_RCOMP	UART1_RT
neo	A	D VSS	DDR3_M0_DQ3	DDR3_M0_DQ3	3 VSS	DDR3_M0_DQ5			MMC1_RESET_	VSS	I2C6_DATA/SD 3_WP		UART1_DATAI N/UART0_DAT	VSS
ned unde	A	C DDR3_M0_DC	2S DDR3_M0_DM4	DDR3_M0_DQ3	3 DDR3_M0_DQ4 9	RESERVED	GPIO_SW93	LPE_I2S2_FRM	GPIO_SW78	I2C2_DATA		NFC_I2C_DATA	UART1_DATAC	
	A		23 DDR3_M0_DQS 4_N	DDR3_M0_DQS	S DDR3_M0_DQ4	RESERVED	PCIE_CLKREQ[0 LPE_12S2_CLK	I2C4_DATA/DD 1_DDC_DATA/		12C5_CLK	LPE_I2S0_DAT	LPE_I2S1_CLK	
	A	A DDR3_M0_D0	23 VSS	DDR3_M0_DQS 6_N	S DDR3_M0_DQ5 2	VSS	DDR3_CORE_P WROK	DDR3_DRAM_P		12C2_CLK	LPE_I2S0_CLK	LPE_I2S0_DAT AOUT	LPE_I2S1_FRM	GPIO_SE79
	Y	DDR3_M0_D0	23 DDR3_M0_DQ3	DDR3_M0_DQ5	DDR3_M0_DM6	DDR3_M0_DQ5	DDR3_M0_DQ5 4	5 1 1	I2C0_DATA	12C0_CLK	LPE_I2S0_FRM	DDI_VGG_S0iX	LPE_I2S1_DAT	LPE_I2S1_I
	v	x 2 0		DDR3_M0_DQ4	+ DDR3_M0_DQ4 2	DDR3_M0_DQ6	DDR3_M0_DQ5	VSS	VSS	VSS	I2C1_CLK	I2C1_DATA	DDI_VGG_S0X	SDIO_V3P3 V1P8A_G3
0	e	DDR3_M0_D0	2S DDR3_M0_DM5	DDR3_M0_DQ4	- + DDR3_M0_DQ4 6	VSS	DDR3_M0_DQ5	DDR_VDDQG_ S4	LPE_I2S2_DAT AOUT	DDI_VGG_S0iX	UNCORE_V1P8	UNCORE_V1P8 A_G3	DDI_VGG_S0iX	
ed ui	L	DDR3_M0_D0	as vss	DDR3_M0_DQS	S DDR3_M0_DQS	DDR3_M0_DQ6	DDR3_M0_DQ6	DDR3_M0_DRA		LPE_I2S2_DAT			DDI_VGG_S0iX	DDI_VGG_
ned und	т	DDR3_M0_D0	04 DDR3_M0_DQ4	DDR3_M0_DM7	7 DDR3_M0_DQ5	DDR3_M0_DQ6	DDR3_M0_DQ5	_	VSS	DDI_VGG_S0iX	DDI_VGG_SOX	DDI_VGG_S0iX	DDI_VGG_S0iX	DDI_VGG_
	R			DDR3_M0_DQ4	DDR3_M0_DQ4	VSS	VSS	VSS	DDR_V1P05A_	DDI_V1p05A_S	DDI_V1p05A_S	VSS	DDI_VGG_S0iX	DDI_VGG_
	P	DDR3_M0_O	DT DDR3_M0_ODT	DDR3_M0_CS1	DDR3_M0_CS0	DDR3_M0_WE_	DDR3_M0_CAS	6 DDRSFR_VDD0 G_S4	2 VSS	VSS	VSS	VSS	VSS	RESERVED
	N	DDR3_M0_M/	A7 VSS	DDR3_M0_MA2	2 DDR3_M0_RAS	VSS	_" DDR3_M0_MA1	DDR3_M0_BS1	VSS	VSS	VSS	CORE_VCC_S0	i CORE_VCC_S0	VSS
	N	1 DDR3_M0_M/	A1 DDR3_M0_MA0	DDR3_M0_MA1	1 DDR3_M0_MA4	DDR3_M0_BS0	DDR3_M0_MA3	VSS	DDR_VDDQG_	VSS	VSS	CORE_VCC_S0	i CORE_VCC_S0	i VSS
	204			DDR3_M0_MA1	1 DDR3_M0_MA5	VSS	DDR_VDDQG_	DDR_VDDQG_	DDR_VDDQG_	CORE_V1p05A _S0iX	F_V1p05A_S0i	CORE_VCC_S0	i CORE_VCC_S0	
JUN	K	DDR3_M0_M/	A1 DDR3_M0_MA6	DDR3_M0_MA1	1 DDR3_M0_BS2	DDR3_M0_CK1	DDR3_M0_CK1	VSS	DDR_VDDQG_ S4	-	^ F_V1p05A_S0i	CORE_VCC_S0	i VSS	05A_G3 VSS
ined ut	J	DDR3_M0_M/	A8 VSS	DDR3_M0_CK0	DDR3_M0_CK0	DDR3_M0_DQ2	DDR3_M0_DQ3	VSS	VSS	VSS	VSS	CORE_VCC_S0	i CORE_VCC_S0	i VSS
	H	DDR3_M0_M/	A1 DDR3_M0_MA0	 DDR3_M0_DQ2 7	-' 2 DDR3_M0_DQ3	VSS	DDR3_M0_DQS	5 DDR3_M0_DQS 3 N	DDR_V1P05A_	VSS	VSS	CORE_VCC_S0	i CORE0_VSFR_	UNCORE_V 5A_S0iX
	G	·		DDR3_M0_CKE	DDR3_M0_CKE	DDR3_M0_DQ2	DDR3_M0_DQ2	-	CORE_V1p05A	CORE_V1p05A _S0iX	VSS	CORE_VCC_S0	i CORE_VCC_S0	
	F	DDR3_M0_DO	21 DDR3_M0_DQ2	DDR3_M0_CKE	DDR3_M0_CKE	DDR3_M0_DQ2	DDR3_M0_DQ2	DDR3_M0_DM3		GPIO_N1/C0_B	GPIO_N2/C0_B		JTAG_TMS	JTAG_TDO
	E	DDR3_M0_D0	21 VSS	- DDR3_M0_DQ1	3 DDR3_M0_DQ1	VSS	DDR3_M0_DQ1	DDR3_M0_DQ1	VSS	GPIO_N0/C0_B	PM2_TX/C1_BP M2_TX GPIO_N4/C0_B PM0_TX/C1_BP	VSS	JTAG_TCK	JTAG_TRS
	C	DDR3_M0_DM	12 DDR3_M0_DQ2	DDR3_M0_DQ9	DDR3_M0_DQ1	DDR3_M0_DM1	DDR3_M0_DQ1	DDR3_M0_DQS 0_P	DDR3_M0_DQ0	ISH_GPIO[13]/C	MO TY	JTAG2_TMS	JTAG2_TDO	JTAG_PRD
	<u>00</u>	DDR3_M0_D0	2S DDR3_M0_DQS 2 P	DDR3_M0_DQ1	2 DDR3_M0_DQS 1 P	DDR3_M0_DQS	DDR3_M0_DQ8	DDR3_M0_DQS	DDR3_M0_DQ3	GPIO_N3/C0_B	GPIO_N6/C0_B PM3_TX/C1_BP	JTAG2_TCK	PMC_SUSCLK[2	GPIO_SUS
sined t	B	-	0 DDR3_M0_DQ2	DDR3_M0_DQ2			DDR3_M0_DQ5	-	DDR3_M0_DQ1	VSS	GPIO0_RCOMP		JTAG2_TDI	VSS
stined u	A		0 VSS	DDR3_M0_DQ1	DDR3_M0_DQ4					DDR_VDDQG_ S4	CORE_V1p05A _S0IX		GPIO_SUS0	GPIO_SUS9
				n, 1					L	Jerni-				<u> </u>
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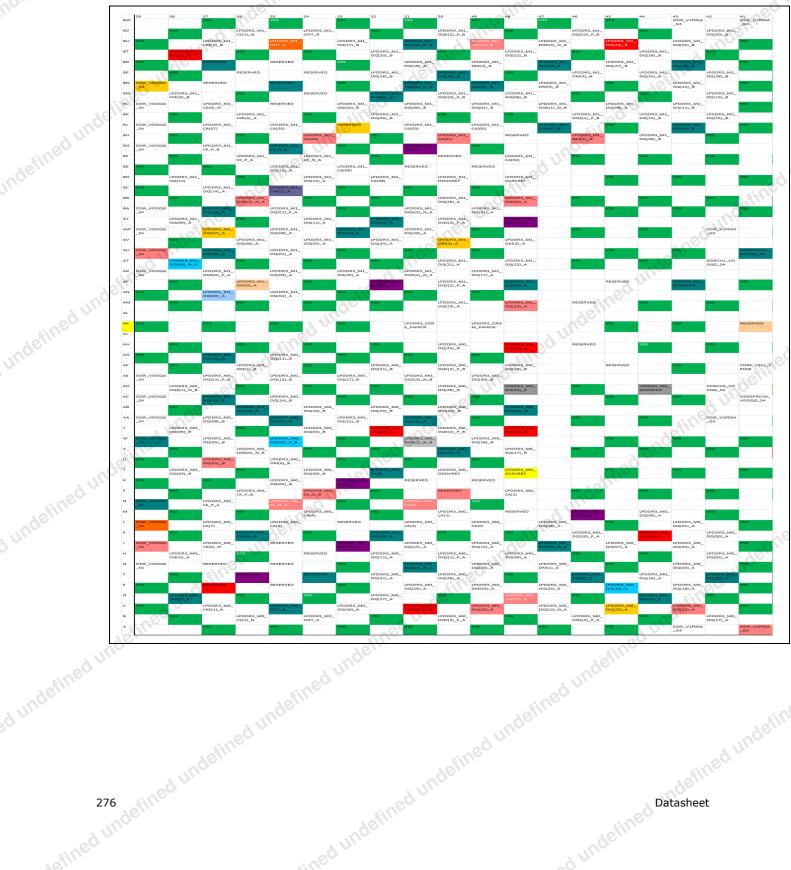


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	_	12	11	10	9	8	7	6	5	4	3	2	1	
	A	N N	neo	MMC1_RCOMP	SD3_CD_N	MMC1_RCLK/M MC1_RESET_N	0	DDI_VGG_S0IX		SD2_D[1]	PMC_PLT_CLK[5]/ISH_GPIO[15]		RESERVED	
	A	AD UART2_CTS_N		SD3_D[3]	VSS	MMC1_CLK	define	SD2_D[3]_CD_ N	SD2_CLK	SD2_D[0]	PWM[0]	PWM[1]/ISH_GPI O[10]/ISH_UAR	RESERVED	
		C UART2_RTS_N	FST_SPI_D[1]	SD3_D[0]	SD3_CLK	MMC1_D[5]	MMC1_D[4]	MMC1_D[3]	VSS	PMC_PLT_CLK[2]/ISH_GPIO[12]		ISH_GPI0[4]/I2S	ISH_GPIO[7]/I2S 4_DATAIN	
undefined undef	Ā	AB FST_SPI_CLK	FST_SPI_D[0]	SD3_D[2]	SD3_D[1]	SD3_1P8_EN	MMC1_D[6]	MMC1_D[2]	SD2_CMD			ISH_GPIO[0]/I2S 3_CLK	ICLK_ICOMP	
sined	A	A FST_SPI_CS[0] _N	VSS	SD3_CMD	SD3_PWREN_N	MMC1_D[0]	MMC1_D[7]	MMC1_CMD	ISH_I2C1_DAT A/ISH_SPI_MOS	ISH_GPIO[9]/ISH		VSS	ICLK_RCOMP	
Inder	Y	UART0_DATAO	VSS	RESERVED	USB_OC[0]_N	MMC1_D[1]	VSS	VSSA	PMC_PLTRST_ N	PMC_SUSCLK[0	PMC_WAKE_N	ISH_GPI0[1]/I2S 3_FS	ISH_GPIO[3]/I2S 3_DATAIN	ed '
		V VSS	VSS	RESERVED	UNCORE_V1P8 A_G3	VSS	ICLK_OSCIN	ICLK_OSCOUT	VSS	PMC_SLP_SOX _N	PMC_PWRBTN_ N		-deft	
	V	PMC_SUSPWR DNACK	PMC_RSTBTN_ N	UNCORE_V1P8 A_G3	VSS	RTC_V3P3RTC _G5	VSS	VSS	PMC_SUS_STA T_N	RESERVED	PCIE_REFCLK0 _P	PCIE_REFCLK0 _N	UNCORE_VNN_ S4	
	ī	DDI_VGG_SOX	DDI_VGG_S0iX	DDI_VGG_S0iX	F_V1P8A_G3	RTC_V3P3A_G 5	F_V3P3A_G3	RTC_TEST_N	RTC_RST_N	RTC_X2	RTC_X1	VSS	RTC_EXTPAD	
26	τ	DDI_VGG_S0iX	DDI_VGG_S0iX	UNCORE1_V1P 05A_G3	F_V1P05A_G3	VSS	F_V1P05A_G3	PMC_CORE_PW ROK	PMC_RSMRST_	PCIE_RCOMP_N	PCIE_RCOMP_P	PCIE_RXN0	PCIE_RXP0	
red un	R	VSS	DDI_VGG_S0iX	VSS	vss und	ICLK_VSFR_G3	F_V1P05A_G3	VSS	VSS	PCIE_TXP0	PCIE_TXN0			
undefined unde	P	VSS	DDI_VGG_S0iX	DDI_VGG_S0iX	UNCORE_VNN_ S4	VSS	PCIeCLK_V1P0 5A_G3	USB_DN0	USB3_RXN0	USB3_RCOMP_ N	USB3_RCOMP_ P	USB3_TXN0	USB3_TXP0	_0
U.	N	DDI_VGG_S0iX	DDI_VGG_S0iX	UNCORE_VNN_ S4	VSS	MPHY_1P05A_ G3	MPHY_1P05A_ G3	USB_DP0	USB3_RXP0	USB_HSIC_1_D ATA	USB_HSIC_1_S TROBE	VSS	USB_HSIC_RC OMP	ner
	N	UNCORE_VSFR	UNCORE_VNN_ S4	UNCORE_VNN_ S4	UNCORE_VNN_ S4	VSS	USBSSIC_V1P0 5A_G3	USB_DN2	USB_DP2	USB_DP3	USB_DN3	USB_HSIC_0_D ATA	USB_HSIC_0_S TROBE	
	L	UNCORE_VNN_ S4	UNCORE_VNN_ S4	UNCORE_VNN_ S4	UNCORE_VNN_ S4	USB_V3P3A_G 3	VSS	UNCORE_VSFR _G3	VSS	USB_DP1	USB_DN1	Jefine		
د		UNCORE_VNN_ S4	UNCORE_VNN_ S4	UNCORE_VNN_ S4	UNCORE_VNN_ S4	USBSSIC_V1P2 A_G3	DDI_USB_VDD Q_G3	DDI2_TXN3	DDI2_TXP3	DDI2_TXP1	DDI2_TXN1	USB_VBUSSNS	USB_OTG_ID	
d un	Ţ	VSS	VSS	UNCORE_VNN_ S4	UNCORE_VNN_ S4	USBHSIC_V1P2 A_G3	DDI_USB_VDD Q_G3	DDI0_TXN1	DDI2_AUXN	DDI2_TXN0	DDI2_TXP0	VSS	USB_RCOMP	
a undefined und	H	USB_V1P8A_G 3	USB_V1P8A_G 3	VSS	MIPL_V1P2A_G 3	DDI_USB_VDD Q_G3	USB_VDDQ_G3	DDI0_TXP1	DDI2_AUXP	DDI0_RCOMP_N	DDI0_RCOMP_P	DDI2_TXP2	DDI2_TXN2	
a une	G	RESERVED	VSS	VSS	MIPI_V1P2A_G 3	UNCORE_VSFR _G3	MCSI_1_CLKN	VSS	VSS	DDI0_TXN0	DDI0_TXP0			ine
	F	SVID_DATA	SVID_CLK	RESERVED	PROCHOT_N	MCSI_1_DN0	MCSI_1_CLKP	DDI0_TXN2	DDI0_TXP2	RESERVED	DDI0_TXP3	DDI0_TXN3	DDI0_AUXN	
	E	SVID_ALERT_N	VSS	DDI2_DDC_CLK /DDI1_DDC_CL		MCSI_1_DP0	VSS	VSS	MDSI_A_DN3	MDSI_A_DP3	MDSI_A_DN2	vss	DDI0_AUXP	
		VSS	GPIO_CAMERA SB08	GPIO_CAMERA SB09	DDI0_HPD	DDI1_BKLTCTL/ MDSL_A_TE/MD		MCSI_1_DP3	MCSI_2_CLKP	MDSI_A_CLKN	MDSI_A_DP2	DDI1_RCOMP_P	DDI1_RCOMP_N	
	000	JTAG_TDI	GPIO_CAMERA SB11	A/DDI1_DDC_D	A/DDI1_DDC_D	SLC TE DDI0_BKLTEN	MCSI_1_DP2	MCSI_1_DN3	MCSI_2_CLKN	MDSI_A_CLKP	MDSI_A_DP0	MDSI_A_DP1	MDSI_A_DN1	
efineo	B	PMC_SUSCLK[3		ATAMOSLODC GPIO_CAMERA SB10	VSS	DDI0_BKLTCTL		MCSI_1_DN1	VSS	MCSI_2_DN0	MCSI_2_DN1	MDSI_A_DN0	RESERVED	
ed undefined un	A	CORE_VCC_S0	i	DDI0_DDC_CLK /DDI1_DDC_CL	DDI0_VDDEN	MCSI_RCOMP		MCSI_1_DP1	MDSI_RCOMP	MCSI_2_DP0	MCSI_2_DP1	RESERVED		Sine
Ser.				KINDSI DDC. C	1	1	1		no-	1	1	1	nd'	S <i>J</i> ,,
		sheet	defili				ad unde	fineu				nije.	ed undr	
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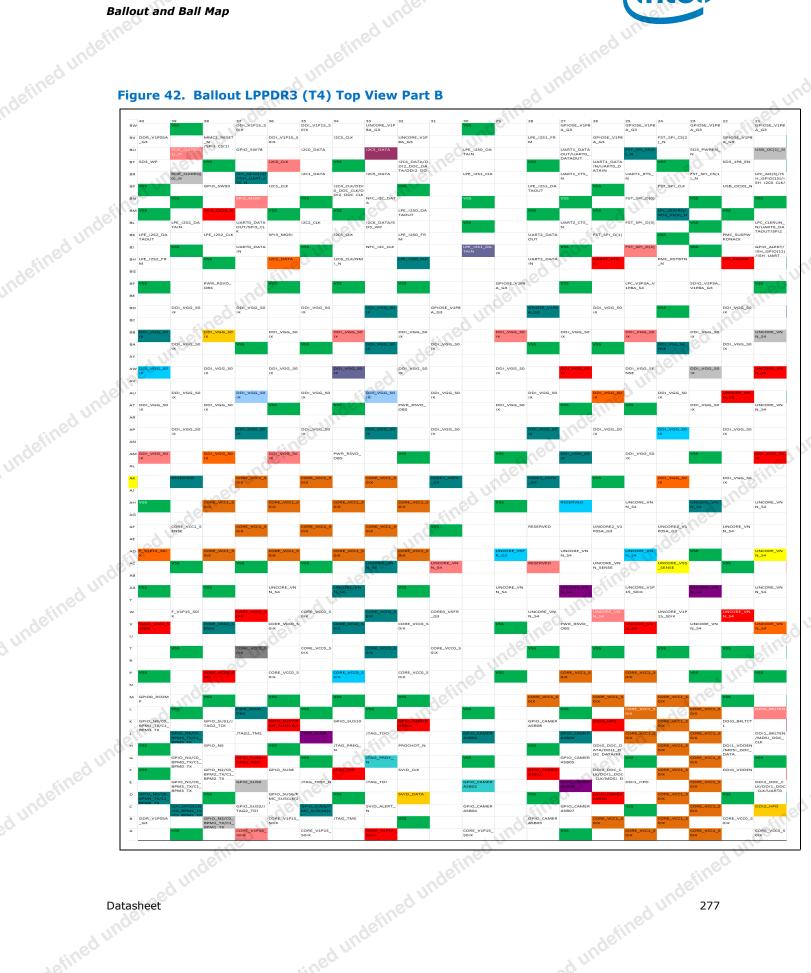


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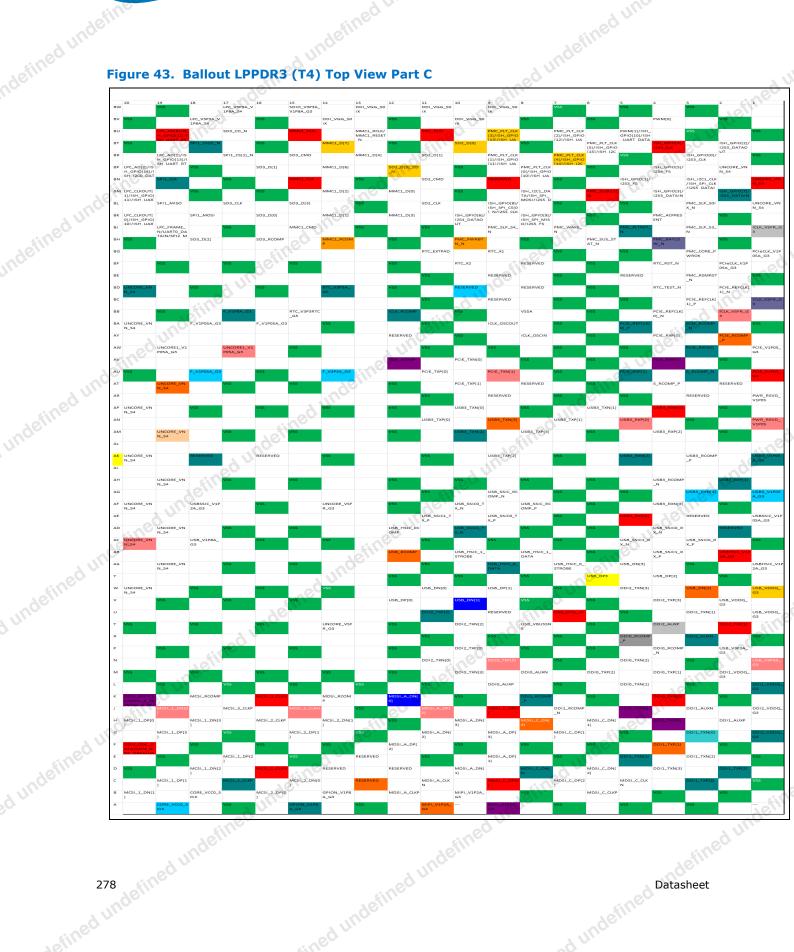
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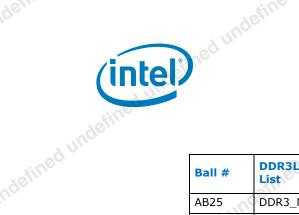
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A10 A12 A13	List DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK CORE_VCC_S0iX	ed v	AA21 AA22 AA23
A12	DDI1_DDC_CLK/ MDSI_DDC_CLK		
	MDSI_DDC_CLK		AA23
	CORE_VCC_S0iX		
۸13			AA24
AIJ	GPIO_SUS9		AA25
A14	GPIO_SUS0		AA3
A16	CORE_V1p05A_S0iX		
A17	DDR_VDDQG_S4		AA4
A18	DDR3_M0_DQ6	5	AA5
A2	RESERVED	Jeo.	
A20	DDR3_M0_DM0	~	A A C
A21	DDR3_M0_DQ2		AA6
A22	DDR3_M0_DQ4		AA7
A23	DDR3_M0_DQ17		AA8
A24	VSS		AA9
A25	PWR_RSVD_OBS		AB1
A3	MCSI_2_DP1		AB10
A4 00	MCSI_2_DP0	-6	AB11
A5	MDSI_RCOMP	IUG,	AB12
A6	MCSI_1_DP1	,	AB13
A8	MCSI_RCOMP		AB14
A9	DDI0_VDDEN		AB15
AA1	ICLK_RCOMP		AB16
AA10	SD3_CMD		AB17
AA11	VSS		
AA12	FST_SPI_CS0_N		AB18
AA13	GPIO_SE79	e	9.0.
AA14	LPE_I2S1_FRM	<i>fill</i>	
AA15	LPE_I2S0_DATAOUT		AB19
AA16	LPE_I2S0_CLK		AB2
AA17	I2C2_CLK		AB20
AA18	VSS		AB21
AA19	DDR3_DRAM_PWROK		AB22
AA2	VSS		AB23
AA20	DDR3_CORE_PWROK		AB24
	A16 A17 A18 A2 A20 A21 A22 A23 A24 A25 A3 A4 A5 A6 A8 A9 AA1 AA10 AA11 AA12 AA13 AA14 AA15 AA14 AA15 AA16 AA17 AA18 AA19 AA18 AA19 AA19	A16CORE_V1p05A_S0iXA17DDR_VDDQG_S4A18DDR3_M0_DQ6A2RESERVEDA20DDR3_M0_DM0A21DDR3_M0_DQ2A22DDR3_M0_DQ4A23DDR3_M0_DQ17A24VSSA25PWR_RSVD_OBSA3MCSI_2_DP1A4MCSI_2_DP0A5MDSI_RCOMPA6MCSI_RCOMPA7ICLK_RCOMPA11ICLK_RCOMPA11VSSAA12FST_SPI_CS0_NAA13GPIO_SE79AA14LPE_I2S1_FRMAA15LPE_I2S0_CLKAA18VSSAA19DDR3_DRAM_PWROKAA2VSS	A16CORE_V1p05A_S0iXA17DDR_VDDQG_S4A18DDR3_M0_DQ6A2RESERVEDA20DDR3_M0_DM0A21DDR3_M0_DQ2A22DDR3_M0_DQ4A23DDR3_M0_DQ17A24VSSA25PWR_RSVD_OBSA3MCSI_2_DP1A4MCSI_2_DP0A5MDSI_RCOMPA6MCSI_1_DP1A8MCSI_RCOMPA11ICLK_RCOMPAA10SD3_CMDAA11VSSAA12FST_SPI_CS0_NAA13GPI0_SE79AA14LPE_I2S1_FRMAA15LPE_I2S0_CLKAA18VSSAA19DDR3_DRAM_PWROKAA2VSS

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า	6	undefine	bru
	Ball #	DDR3L-RS Customer Pin List	ndefined und
. d V	AA21	VSS	no
20	AA22	DDR3_M0_DQ52	
	AA23	DDR3_M0_DQS6_N	
	AA24	VSS	
	AA25	DDR3_M0_DQ36	
	AA3	ISH_I2C1_CLK/ISH_SPI_CLK/ I2S5_DATAIN	
	AA4	ISH_GPIO9/ISH_SPI_MISO/ I2S5_FS	afined L.
Ined	AA5	ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	undefined un
	AA6	MMC1_CMD	
	AA7	MMC1_D7	
	AA8	MMC1_D0	
	AA9	SD3_PWREN_N	
	AB1	ICLK_ICOMP	
	AB10	SD3_D2	undefined
	AB11	FST_SPI_D0	Yetin.
ed	AB12	FST_SPI_CLK	une
(in	AB13	UART2 DATAOUT	
	AB14	LPE_I2S1_CLK	
	AB15	LPE I2SO DATAIN	
	AB16	12C5 CLK	
	AB17		ad u
efine	AB18	I2C4_DATA/ DDI1_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	a undefined "
	AB19	LPE_I2S2_CLK	
	AB2	ISH_GPIO0/I2S3_CLK	
	AB20	PCIE_CLKREQ0_N	
	AB21	RESERVED	
	AB22	DDR3_M0_DQ48	
	AB23	DDR3_M0_DQS6_P	ed
	AB24	DDR3_M0_DQS4_N	ACTINE
define	30.7.	DDR3_M0_DQ48 DDR3_M0_DQS6_P DDR3_M0_DQS4_N	ed une
		unden	
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Idefined undefine		adefined u			
	Ball #	DDR3L-RS Customer Pin List		Ball #	DD Lis
0	AB25	DDR3 M0 DQ33		AD1	RES
	AB3	ISH_GPIO2/I2S3_DATAOUT		AD10	SD3
ndefined undefined un	AB4	PMC_PLT_CLK3/ISH_GPIO13/	. ed	AD12	UAF
110	9.0	ISH_UART_RTS_N/SPI2_CLK	11.	AD13	VSS
ed t	AB5	SD2_CMD		AD14	UAF
defill	AB6	MMC1_D2			UAF
y une	AB7	MMC1_D6		AD16	I2C
	AB8	SD3_1P8_EN		AD17	VSS
	AB9	SD3_D1		AD18	ММ
	AC1	ISH_GPIO7/I2S4_DATAIN		AD2	PW
	AC10	SD3_D0		AD20	ISH
	AC11	FST_SPI_D1	sine		SD3
defined ur	AC12	UART2_RTS_N	8,	AD21	DDI
	AC13	UART1_CTS_N		AD22 AD23	VSS DDI
14-	AC14	UART1_DATAOUT/			-
	AC15	UARTO_DATAOUT		AD24	DDI
	AC15 AC16	NFC_I2C_DATA		AD25 AD3	VSS PWI
	AC10	NFC_I2C_CLK			<u> </u>
	AC17	I2C2_DATA		AD4	SD2
	ACIO	GPIO_SW78		AD5	SD2
	AC19	LPE_I2S2_FRM	Sin	AD6	SD2
. 24	AC2	ISH_GPIO4/I2S4_CLK		AD8	MM
	AC20	GPIO_SW93		AD9	VSS
	AC21	RESERVED		AE1	RES
	AC22	DDR3_M0_DQ49		AE10	MM
	AC23	DDR3_M0_DQ37		AE12	UAF
	AC24	DDR3_M0_DM4		AE13	
atined	AC25	DDR3_M0_DQS4_P		AE14 AE16	SD3 I2C
	11/2	PMC_PLT_CLK4/ISH_GPI014/ ISH_I2C0_DATA/SPI2_MISO		AE16 AE17	I2C
	AC4	PMC_PLT_CLK2/ISH_GPIO12/	defil	AE17 AE18	UAF
ed		ISH_UART_CTS_N/ SPI2_CS0_N		AE18 AE2	RES
efine	AC5	VSS		AE2 AE20	DDI
	AC5 AC6	MMC1 D3		AE20 AE21	DDI
	AC6 AC7	MMC1_D3		AE21 AE22	DDI
	AC7			AE22 AE23	DDI
	AC0	MMC1_D5		AE24	
defined undefined	AC9	SD3_CLK	ndefi	AE24	PW
tined uno		ed unden.			
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	leftine	
Ball #	DDR3L-RS Customer Pin List	undefined unde
AD1	RESERVED	
AD10	SD3_D3	
AD12	UART2_CTS_N	
AD13	VSS	
AD14	UART1_DATAIN/ UART0_DATAIN	
AD16	I2C6_DATA/SD3_WP	
AD17	VSS	
AD18	MMC1_RESET_N	y une
AD2	PWM1/ISH_GPIO10/ ISH_UART_DATAOUT	undefined und
AD20	SD3_WP	une
AD21	DDR3_M0_DQ51	
AD22	VSS	
AD23	DDR3_M0_DQ38	
AD24	DDR3_M0_DQ32	
AD25	VSS	
AD3	PWMO	d un
AD4	SD2_D0	sineu
AD5	SD2_CLK	ed undefined un
AD6	SD2_D3_CD_N	dun
AD8	MMC1_CLK	
AD9	VSS	
AE1	RESERVED	
AE10	MMC1_RCOMP	
AE12	UART2_DATAIN	
AE13	UART1_RTS_N	du'
AE14	SD3_RCOMP	ed undefined u
AE16	I2C6_CLK/NMI_N	Inde
AE17	I2C5_DATA	
AE18		
AE2	RESERVED	
AE20	DDR3_M0_RCOMPPD	
AE21	DDR3_M0_OCAVREF	
AE22	DDR3_M0_ODQVREF	
AE23	DDR3_M0_DQ35	
AE24	PWR_RSVD_OBS	defille
ined L.	Left	ned undefined t
	Datashee	it.
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	ned undef	ine adefined undefine	ndefined	
			d UI	
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efili		adefinec		
	Ball #	DDR3L-RS Customer Pin List	Ball #	o P
	AE25	PWR_RSVD_OBS	C16	G
defined undefi	AE3	PMC_PLT_CLK5/ISH_GPI015/ ISH_I2C0_CLK/SPI2_MOSI	C17	G
Inde	AE4	SD2_D1	C18	D
red	AE5	SD2_D2	C18	D
4efill	AE6	DDI_VGG_S0iX	C19 C2	M
	AE8	MMC1_RCLK/MMC1_RESET_N	C2	_
	AE9	SD3_CD_N	C20	D
	B1	RESERVED	-	D
	B10	GPIO_CAMERASB10	C22	D
	B12	PMC_SUSCLK3	C23	D
20	B13	VSS	C24	D
ndefined unde	B14	JTAG2_TDI	C25	D
	B16	GPIO0_RCOMP	C3	Μ
defin	B17	VSS	C4	Μ
	B18	DDR3_M0_DQ1	C5	Μ
	B2	MDSI_A_DN0	C6	M
	B20	DDR3_M0_DQ5	C7	M
	B21	VSS	C8	D
	B22	DDR3_M0_DQ7	C9	D
6	B23	DDR3_M0_DQ22	inec	U
Indefined und	B24	DDR3_M0_DQ20	. · ·	Μ
	B25	PWR_RSVD_OBS	D1	D
	B3	MCSI_2_DN1	D10	G
	B4	MCSI_2_DN0	D11	G
	B5	VSS	D12	V
	B6	MCSI_1_DN1	D13	J
	B8	DDI0_BKLTCTL	D14	
	B9	VSS	D15	J
	C1	MDSI_A_DN1	D16	G
undefined uni	C10	DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	D17	IS C
	C11	GPIO_CAMERASB11	D18	D
	C12	JTAG TDI	D19	D
	C12	GPIO SUS8	D2	D
	C13	PMC_SUSCLK2	D20	D
	C14		D21	D
Datasheet	define	JIAG2_TCK	efineo	
unoc		d une		
		cint ⁵		

	Ball #	DDR3L-RS Customer Pin List	ndefined
	C16	GPIO_N6/C0_BPM3_TX/ C1_BPM3_TX	definec
	C17	GPIO_N3/C0_BPM1_TX/ C1_BPM1_TX	anc.
	C18	DDR3_M0_DQ3	
	C19	DDR3_M0_DQS0_N	
	C2	MDSI_A_DP1	
	C20	DDR3_M0_DQ8	
	C21	DDR3_M0_DQS1_N	
	C22	DDR3_M0_DQS1_P	- ed
Ī	C23	DDR3_M0_DQ18	Jefill'
3	C24	DDR3_M0_DQS2_P	undefined
ļ	C25	DDR3_M0_DQS2_N	
Ī	C3	MDSI_A_DP0	-
Ī	C4	MDSI_A_CLKP	-
-	C5	MCSI_2_CLKN	-
	C6	MCSI_1_DN3	-
Ī	C7	MCSI_1_DP2	
Ī	C8	DDI0_BKLTEN	e
6	С9	DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/MDSI_C_TE	undefine
-	D1	DDI1_RCOMP_N	-
Ī	D10	GPIO_CAMERASB09	-
-	D11	GPIO_CAMERASB08	-
-	D12	VSS	-
-	D13	JTAG_PRDY_N	-
-	D14	JTAG2_TDO	- Aline
	D15	JTAG2_TMS	nder
6	D16	GPIO_N8/C0_BPM1_TX/ C1_BPM1_TX	d undefine
ŀ	D17	ISH_GPIO13/C0_BPM2_TX/ C1_BPM2_TX	1
ł	D18	DDR3_M0_DQ0	1
ļ	D19	DDR3_M0_DQS0_P	1
ļ	D2	DDI1_RCOMP_P	1
ŀ	D20	DDR3_M0_DQ15	
-	D21	DDR3_M0_DM1	7efii
		DDI1_RCOMP_P DDR3_M0_DQ15 DDR3_M0_DM1	ed ^{un}

Ballout and Ball Map

), .	define		define	Ò Ū
(intel) ed ut	defined undef	ined	une	
ed undefine D22	ndefine	_		
Ball #	DDR3L-RS Customer Pin List		Ball #	DD List
D22	DDR3_M0_DQ12	_	E7	VSS
D23	DDR3_M0_DQ9		E8	MC
D24	DDR3_M0_DQ21	ane ^C	E9	DD
D25	DDR3_M0_DM2		F1	DD
D3	MDSI_A_DP2		F10	RES
D4	MDSI_A_CLKN		F11	SVI
D5	MCSI_2_CLKP	1	F12	SVI
D6	MCSI_1_DP3	1	F13	JTA
D7	MCSI_1_DN2	1	F14	JTA
D24 D25 D3 D4 D5 D6 D7 D8	DDI1_BKLTCTL/MDSI_A_TE/ MDSI_C_TE	1	F15 F16	VSS GPI
D9	DDI0_HPD	ane	p. 10	C1
UNO E1	DDI0_AUXP	erni	F17	GPI
E1 E10 E11 E12 E13	DDI2_DDC_CLK/ DDI1_DDC_CLK/	1	F18	C1_ GPI
unos	UART0_DATAOUT/ MDSI_DDC_CLK/MDSI_A_TE		F19	DDI
E11	VSS	-	F2	DD
E11 E12	SVID ALERT N	-	F20	DDI
E12 E13	JTAG_TRST_N	-	F21	DDI
E13	JTAG_TCK	-	F22	DDI
	VSS		F23	DDI
E15	GPIO_N4/C0_BPM0_TX/	Jet II	F24	DDI
ed l'	C1_BPM0_TX		F25	DDI
E15 E16 E17 E18 E19 E2 E20	GPIO_N0/C0_BPM0_TX/ C1_BPM0_TX	1	F3 F4	DD RES
E18	VSS UN	1	F5	DD
E19	DDR3_M0_DQ10	1	F6	DD
E2	VSS	1	F7	MC
E20	DDR3_M0_DQ14	1	F8 1	MC
E21	VSS		F9	PRC
E22	DDR3_M0_DQ13	det !!	G10	VSS
E23	DDR3_M0_DQ11		G10 G11	VSS
E24	VSS	1	G12	RES
E25	DDR3_M0_DQ16		G12 G13	UNG
E3	MDSI_A_DN2		G13 G14	COF
E4	MDSI_A_DP3		G14 G15	CO
E5	MDSI_A_DN3		CIC	VSS
E6	VSS	1	7900	1.00
E5	MDSI_A_DN3	ndef	CIC	

Г	Ball #	Leftined UI
Γ	Ball #	10th
	bull #	DDR3L-RS Customer Pin List VSS MCSI_1_DP0 DDI2_HPD
-	E7	VSS
	E8	MCSI_1_DP0
red-	E9	DDI2_HPD
-	F1	DDI0_AUXN
	F10	RESERVED
	F11	SVID_CLK
_	F12	SVID_DATA
_	F13	JTAG_TDO
	F14	JTAG_TMS
	F15	VSS
ined	F16	JTAG_TDO JTAG_TMS VSS GPIO_N2/C0_BPM2_TX/ C1_BPM2_TX
	F17	GPIO_N1/C0_BPM3_TX/ C1_BPM3_TX
	F18	GPIO_DFX4
	F19	DDR3_M0_DM3
	F2	DDI0_TXN3
	F20	DDR3_M0_DQ24
	F21	DDR3_M0_DQ25
	F22	DDR3_M0_CKE3
300	F23	DDR3_M0_DQ24 DDR3_M0_DQ25 DDR3_M0_CKE3 DDR3_M0_CKE2 DDR3_M0_DQ23
37.	F24	DDR3_M0_DQ23
	F25	DDR3_M0_DQ19
	F3	DDI0_TXP3
	F4	RESERVED
	F5	DDI0_TXP2
	F6	DDI0_TXN2
	F7	MCSI_1_CLKP
-	F8	MCSI_1_DN0
011	F9	DDI0_TXP2 DDI0_TXN2 MCSI_1_CLKP MCSI_1_DN0 PROCHOT_N VSS
	G10	
	G11	VSS
	G12	RESERVED
	G13	UNCORE_V1p05A_S0iX
	G14	CORE_VCC_S0iX
	G15	CORE_VCC_S0iX
	G16	VSS
defin		CORE_VCC_SOIX CORE_VCC_SOIX VSS Datasheet
		4 undefine

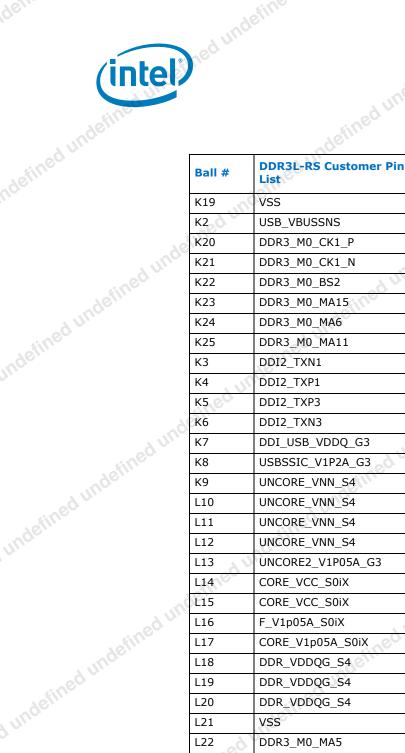


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Jefin .		ndefinec	_		
	Ball #	DDR3L-RS Customer Pin List		Ball #	P
	G17	CORE_V1p05A_S0iX		H8	D
	G18	CORE_V1p05A_S0iX	1	Н9	Μ
defined undefi	G19	DDR_V1P05A_G3	So I	J1	U
unoc	G20	DDR3_M0_DQ26	Ī	J10	U
ined i	G21	DDR3_M0_DQ28	Ī	J11	V
detin	G22	DDR3_M0_CKE0	Ī	J12	V
	G23	DDR3_M0_CKE1	Ī	J13	V
	G3	DDI0_TXP0	F	J14	С
	G4	DDI0_TXN0	F	J15	С
	G5	VSS	-	J16	V
	G6	VSS	1	J17	V
26	G7	MCSI_1_CLKN	100	J18	V
ndefined undef	G8	UNCORE_VSFR_G3	ŀ	J19	V
	G9	MIPI_V1P2A_G3	ŀ	J2	V
delli	H1	DDI2_TXN2	ŀ	J20	D
	H10	VSS	F	J21	D
	H11	USB_V1P8A_G3	-	J22	D
	H12	USB_V1P8A_G3	-	J23	D
	H13	UNCORE_V1p05A_S0iX	-	J24	V
	H14	CORE0_VSFR_G3	-	J25	D
undefined unde	H15	CORE_VCC_S0iX	- 0]3	D
d une	H16	VSS	-]4	D
	H17	VSS	-	J5	D
	H18	DDR_V1P05A_G3	-	J6	D
	H19	DDR3_M0_DQS3_N	-	J7	D
	H2	DDI2_TXP2	-	J8	U
	H20	DDR3_M0_DQS3_P	-	J9	U
	H21	VSS	ŀ	K1	U
	H22	DDR3_M0_DQ31	0	K10	U
	H23	DDR3_M0_DQ27	in	K10	U
undefined und	H24	DDR3_M0_MA09	F	K12	U
stine	H25	DDR3_M0_MA14	F	K13	V
inde	H3	DDI0_RCOMP_P	-	K14	V
	H4	DDI0_RCOMP_N	-	K15	C
	H5	DDI2_AUXP	-	K16	F
	H6	DDI0_TXP1	-	K17	C
	H7		F	K18	D
		000_1002_00		<u> </u>	
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		in the			

	DDR3L-RS Customer Pin	
Ball #	List	ndefined und
H8	DDI_USB_VDDQ_G3	sines
H9	MIPI_V1P2A_G3	nde.
]1	USB_RCOMP	P.,
J10	UNCORE_VNN_S4	
]11	VSS	
112	VSS	
113	VSS	
]14	CORE_VCC_S0iX	
115	CORE_VCC_S0iX	indefined un
J16	VSS	fine
117	VSS	inde
118	VSS	0.1
119	VSS	1
12	VSS uno	1
120	DDR3_M0_DQ30	1
J21	DDR3_M0_DQ29	1
122	DDR3_M0_CK0_P	
123	DDR3_M0_CK0_N	undefined un
J24	VSS	4efille
125	DDR3_M0_MA8	unc
13	DDI2_TXP0	>
]4	DDI2_TXN0	
15	DDI2_AUXN	
16	DDI0_TXN1	
17	DDI_USB_VDDQ_G3	
18	USBHSIC_V1P2A_G3	defined u
19	UNCORE_VNN_S4	ineo -
<1	USB_OTG_ID	d undefille
K10	UNCORE_VNN_S4	JUIL
K11	UNCORE_VNN_S4	<u> </u>
K12	UNCORE_VNN_S4	1
K13	VSS	1
K14	VSS	
K15	CORE_VCC_S0iX	
K16	F_V1p05A_S0iX	λ.
K17	CORE_V1p05A_S0iX	Finel
K18	DDR_VDDQG_S4	1 261
	H9 H1 H2 H2	H9 MIPI_V1P2A_G3 H9 MIPI_V1P2A_G3 H1 USB_RCOMP H1 VSS H1 VSS H1 VSS H1 VSS H1 CORE_VCC_SOIX H1 CORE_VCC_SOIX H1 CORE_VCC_SOIX H1 CORE_VCC_SOIX H1 CORE_VCC_SOIX H1 VSS H1 DDR3_M0_DQ30 H2 DDR3_M0_CK0_N H2 DDR3_M0_CK0_N H2 DDR3_M0_CK0_N H2 DDI2_TXP0 H4 DDI2_TXN0 H5 DDI2_AUXN H6 DDI0_TXN1 H7 DDI_

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DDR_VDDQG_S4

DDR_VDDQG_S4

DDR3_M0_MA5

DDR3_M0_MA1

UNCORE_VSFR_G3

USB_V3P3A_G3

UNCORE_VNN_S4

USB HSIC 0 STROBE

USB DN1

USB DP1

VSS

VSS

VSS

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3L-RS Customer Pin	Ball #	DDR3L-RS Customer Pin List UNCORE_VNN_S4 UNCORE_VNN_S4 UNCORE_VSFR_G3	, <i>1</i> 06
	M10	UNCORE_VNN_S4	
VBUSSNS	M11	UNCORE_VNN_S4	
3_M0_CK1_P	M12	UNCORE_VSFR_G3	
3_M0_CK1_N	M13	VSS	
3_M0_BS2	M14	CORE_VCC_S0iX	
3_M0_MA15	M15	CORE_VCC_S0iX	
3_M0_MA6	M16	VSS	
3_M0_MA11	M17	VSS DDR_VDDQG_S4 VSS USB_HSIC_0_DATA	
_TXN1	M18	DDR_VDDQG_S4	
_TXP1	M19	VSS	
 TXP3	M2	USB_HSIC_0_DATA	
 TXN3	M20	DDR3_M0_MA3	
USB_VDDQ_G3	M21	DDR3 M0 BS0	
SSIC_V1P2A_G3	M22	DDR3_M0_MA4	
DRE_VNN_S4	M23	DDR3_M0_MA13	
DRE_VNN_S4	M24	DDR3_M0_MA0	
DRE_VNN_S4	M25	DDR3_M0_MA12	
DRE_VNN_S4	M3 6	USB_DN3	UI.
DRE2_V1P05A_G3	M4	USB_DP3	
	M5	USB_DP2	
	M6	<u> </u>	
E_VCC_SOIX			
	M7	USBSSIC_V1P05A_G3	
E_V1p05A_S0iX	M8		
_VDDQG_S4	M9	UNCORE_VNN_S4	
_VDDQG_S4	N1	USB_HSIC_RCOMP	
_VDDQG_S4	N10	UNCORE_VNN_S4	
	N11	DDI_VGG_S0iX	
3_M0_MA5	N12	DDI_VGG_S0iX	
3_M0_MA1	N13	UNCORE_VNN_S4 DDI_VGG_S0iX DDI_VGG_S0iX VSS CORE_VCC_S0iX	
DN1	N14		
_DP1	N15	CORE_VCC_S0iX	
Sino	N16	VSS	
DRE_VSFR_G3	N17	VSS	
edu	N18	VSS	
_V3P3A_G3	N19	DDR3_M0_BS1	9,
DRE_VNN_S4	N2	VSS	
HSIC_0_STROBE	N20	DDR3_M0_MA10	
aned undefined undef	ine	DDR3_M0_BS1 VSS DDR3_M0_MA10 Datasheet	
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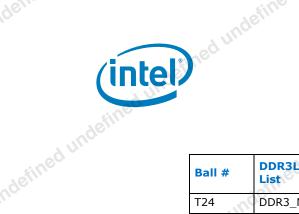


Ballout and Ball Map Jalle

Ball #DDR3L-RS CustoN21VSSN22DDR3_M0_RAS_NN23DDR3_M0_MA2N24VSSN25DDR3_M0_MA7	R1 R1 R1 R1 R1 R1 R1 R1 R1 R1 R1 R1 R1 R
N22 DDR3_M0_RAS_N N23 DDR3_M0_MA2 N24 VSS	ROBE R1
N23 DDR3_M0_MA2 N24 VSS	ROBE R1
N24 VSS	R1 R0BE R1
	ROBE R1
	ROBE R1
N3 USB_HSIC_1_ST	ra R1
N4 USB_HSIC_1_DA	
N5 USB3_RXP0	R1
N6 USB_DP0	R1
N7 MPHY_1P05A_G3	R1
N8 MPHY_1P05A_G3	R2
N9 VSS	R2
P1 USB3_TXP0	R2
P10 DDI_VGG_S0iX	R2
P11 DDI_VGG_S0iX	R3
P12 VSS	R4
P13 RESERVED	R5
P14 VSS	R6
P15 VSS	R7
P16 VSS	R8
P17 VSS	R9
P18 VSS	T1
P19 DDRSFR_VDDQG	_S4 T1
P2 USB3_TXN0	T1
P20 DDR3_M0_CAS_M	I T1
P21 DDR3_M0_WE_N	T1
P22 DDR3_M0_CS0_N	I T1
P23 DDR3_M0_CS1_N	T1
P24 DDR3_M0_ODT0	T1
P25 DDR3_M0_ODT1	Jefill T1
P3 USB3_RCOMP_P	T1
P4 USB3_RCOMP_N	T1
P5 USB3_RXN0	T2
P6 USB_DN0	T2
P7 PCIeCLK_V1P05A	_G3 T2
P8 VSS	T2
P9 UNCORE_VNN_S4	F T2
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adefined undefin	ed un	(intel) defined un	
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RS Customer Pin	Ball #	DDR3L-RS Customer Pin List VSS DDI_VGG_S0iX	
	R10	VSS	
M0_RAS_N	R11	DDI_VGG_S0iX	
M0_MA2	R12	VSS	
den	R13	DDI_VGG_S0iX	
M0_MA7	R14	DDI_VGG_S0iX	
SIC_1_STROBE	R15	VSS	
SIC_1_DATA	R16	DDI_V1p05A_S0iX	
RXP0	R17	DDI_V1p05A_S0iX	
PO	R18	DDI_V1p05A_S0iX DDR_V1P05A_G3 VSS VSS	11-
1P05A_G3	R19	VSS	
1P05A_G3	R20	VSS	
ć	R21	VSS	
ТХРО	R22	DDR3_M0_DQ45	
GG_S0iX	R23	DDR3_M0_DQ44	
GG_S0iX	R3	PCIE_TXN0	
inde	R4	PCIE_TXP0	
VED	R5	VSS	
	R6	VSS VSS F_V1P05A_G3	
	R7	F_V1P05A_G3	
	R8	ICLK_VSFR_G3	
.0	R9	VSS	
, inde	T1	PCIE_RXP0	
R_VDDQG_S4	T10	UNCORE1_V1P05A_G3	
TXN0	T11	DDI_VGG_S0iX	
M0_CAS_N	T12	DDI_VGG_S0iX	
MO_WE_N	T13	DDI_VGG_S0iX	5
M0_CS0_N	T14	DDI_VGG_S0iX	
M0_CS1_N	T15	DDI_VGG_S0iX DDI_VGG_S0iX DDI_VGG_S0iX DDI_VGG_S0iX DDI_VGG_S0iX DDI_VGG_S0iX	
M0_ODT0	T16	DDI_VGG_S0iX	
M0_ODT1	۲17 T17	DDI_VGG_S0iX	
RCOMP_P	T18	VSS	
RCOMP_N	T19	DDR_VDDQG_S4	
RXN0	T2	PCIE_RXN0	
NO	T20	DDR3_M0_DQ57	
K_V1P05A_G3	T21	DDR3_M0_DQ63	1
	T22	DDR3_M0_DQ56	
RE_VNN_S4	T23	DDR3_M0_DM7	
ned undefined unf	Jefines	DDR3_M0_DQ57 DDR3_M0_DQ63 DDR3_M0_DQ56 DDR3_M0_DM7 285	
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Ballout and Ball Map



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(intel)		afine undef	ined	711.	
tined undefine	Ball #	DDR3L-RS Customer Pin List		Ball #	DD Lis
-	T2 4	e ⁽¹⁾		1/12	9
_	T24	DDR3_M0_DQ41	-	V12	PM
_	T25 T3	DDR3_M0_DQ47	60	V13	UAI
96-	13 T4	PCIE_RCOMP_P	ino	V14	
d un	T5	PCIE_RCOMP_N		V15	UN
efine		PMC_RSMRST_N PMC_CORE_PWROK		V16	DD
Inde	T6	F_V1P05A_G3		V17	LPE
-ed t	T7			V18	DD
Still	Т8 Т9	VSS		V19	PCI
		F_V1P05A_G3		V2	DD
_	U1	RTC_EXTPAD		V20	VSS
	U10 U11	DDI_VGG_S0iX		V21	DD
	U12	DDI_VGG_S0iX	SUL.	V22	_
edu	U12 U13	DDI_VGG_S0iX		V23	DD DD
defilit	U14	DDI_VGG_S0iX		V24 V25	DD
4 UNC		DDI_VGG_S0iX			PCI
sin ^{eo}	U15	DDI_VGG_S0iX DDI_VGG_S0iX		V3 V4	RES
Jein,	U16 U17	LPE_I2S2_DATAIN		V4 V5	PM
-					VSS
-	U18	DDR_V1P05A_G3		V6	VS
	U19 U2	DDR3_M0_DRAMRST_N VSS	11/2	V7	
, un	U20	DDR3_M0_DQ62	er.	V8 V9	RTC VSS
cin ^{eo}	020				
70.	U21	DDR3_M0_DQ60	-	W10	RES
dun	U22	DDR3_M0_DQS7_P	-	W11	VSS
sinec	U23	DDR3_M0_DQS7_N	-	W12	VSS
lde.	U24	VSS	-	W13	SD:
		DDR3_M0_DQS5_N	-	W14	DD
	U3	RTC_X1		W15	120
-	U4 U5	RTC_X2	717	W16	I2C VSS
2 V.	U6	RTC_RST_N	96.	W17	VS
stines	U7	RTC_TEST_N F_V3P3A_G3		W18 W19	VS
unde.	U8	RTC_V3P3A_G5	-	W20	DD
edu	U9	F_V1P8A_G3	-	W20	DD
1etine	V1	UNCORE_VNN_S4	-	W21 W22	DD
,n ^{0,0}	V1 V10	76.	-	W23	DD
		UNCORE_V1P8A_G3 PMC_RSTBTN_N	-		PM
L	definee			N3 0.	PM
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all #	DDR3L-RS Customer Pin	
	List	defi
/12	PMC_SUSPWRDNACK	
13	UARTO_DATAIN	
/14	DDI_VGG_S0iX	
/15	UNCORE_V1P8A_G3	
/16	UNCORE_V1P8A_G3	
/17	DDI_VGG_S0iX	
/18	LPE_I2S2_DATAOUT	
/19	DDR_VDDQG_S4	ndef
/2	PCIE_REFCLK0_N	
/20	DDR3_M0_DQ59	. 8
/21	VSS	
/22	DDR3_M0_DQ46	
/23	DDR3_M0_DQ40	
/24	DDR3_M0_DM5	
/25	DDR3_M0_DQS5_P	
/3	PCIE_REFCLK0_P	
/4	RESERVED	
/5	PMC_SUS_STAT_N	
/6	VSS	
V7	VSS	unde
/8	RTC_V3P3RTC_G5	
/9	VSS	
W10	RESERVED	
W11	VSS	
W12	VSS	
W13	SDIO_V3P3A_V1P8A_G3	
W14	DDI_VGG_S0iX	
W15	VSS SDIO_V3P3A_V1P8A_G3 DDI_VGG_S0iX I2C1_DATA I2C1_CLK VSS VSS	6
W16	I2C1_CLK	U
W17	VSS	
W18	VSS	
W19	VSS	
W20	DDR3_M0_DQ58	
	DDR3_M0_DQ61	
W21	DDR3_M0_DQ42	
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N21 N22 N23	DDR3_M0_DQ42 DDR3_M0_DQ43 PMC_PWRBTN_N	



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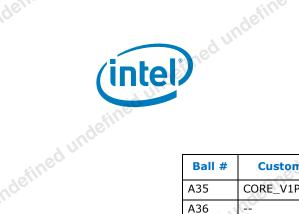
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		Ball #	DDR3L-RS Customer Pin List		Ball #	6 E
		W4	PMC_SLP_S0IX_N		Y2	I
		W5	VSS		Y20	D
	undefined undefi	W6	ICLK_OSCOUT	heo '	Y21	D
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	tined -	W8	VSS		Y23	D
	defini	W9	UNCORE_V1P8A_G3		Y24	D
24		Y1	ISH_GPIO3/I2S3_DATAIN		Y25	D
		Y10	RESERVED		Y3	Р
		Y11	VSS		Y4	P
		Y12	UART0_DATAOUT		Y5	Р
		Y13	LPE_I2S1_DATAIN	6	Y6	V
	det	Y14	LPE_I2S1_DATAOUT	sine	Y7	V
	dune	Y15	DDI_VGG_S0iX	7	Y8	Μ
		Y16	LPE_I2S0_FRM		Y9	U
	ude.	Y17	I2C0_CLK			
		Y18	I2C0_DATA			
1efine		Y19	DDR3_M0_DQ50			
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	Ball #	DDR3L-RS Customer Pin List
	Y2	ISH_GPIO1/I2S3_FS
0	Y20	DDR3_M0_DQ54
	Y21	DDR3_M0_DQ55
	Y22	DDR3_M0_DM6
	Y23	DDR3_M0_DQ53
	Y24	DDR3_M0_DQ34
	Y25	DDR3_M0_DQ39
	Y3	PMC_WAKE_N
	Y4	PMC_SUSCLK0
	Y5	PMC_PLTRST_N
	Y6	VSSA
	Y7	VSS
	Y8	MMC1_D1
	Y9	USB_OCO_N

	Y13	LPE_I2S1_DATAIN	6	Y6	VSSA
	Y14	LPE_I2S1_DATAOUT	sines	Y7	VSS
d une	Y15	DDI_VGG_S0iX	7	Y8	MMC1_D1
	Y16	LPE_I2S0_FRM	1	Y9	USB_OC0_N
nder	Y17	I2C0_CLK	1		cineo
ed u	Y18	I2C0_DATA			dein
lefine	Y19	DDR3_M0_DQ50			d ull
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		7		UNOC	USB_OCO_N
20.3	SoC 7	Γ4 Pin List Locatio	nnet		
ed un		a uno		Ball #	Customer Name -
	Ball #	Customer Name - LPDDR3		A22	d'
unos	A1	dell		A23	CORE_VCC1_S0iX
	A10	- dui		A24	unde
den	A11	MIPI_V1P2A_G3		A25	CORE_VCC1_S0iX
ULL	A12	<u>, nos</u>		A26	
	A13	VSS		A27	VSS
	A14		ein ^e	A28	
	A15	GPION_V1P8A_G3	96,	A29	
	A16			A3	VSS
dell	A17	VSS		A30	CORE_V1P15_S0iX
d ^{ull}	A18	unde		A31	deni
undefined undefined un	A19	CORE_VCC0_S0iX		A32	dun
Inde	A2	defill		A33	CORE_V1P15_S0iX
	A20	<u>nuc</u>		A34	<u>6.</u>
	A21	CORE_VCC0_S0iX		du	
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Ball #	Customer Name - LPDDR3	
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A23	CORE_VCC1_S0iX	_
A24	uno	
A25	CORE_VCC1_S0iX	undefined
A26		since
A27	VSS	unde.
A28		3 01
A29	46fm	
A3	VSS	
A30	CORE_V1P15_S0iX	
A31	- del.	
A32	- du''	
A33	CORE_V1P15_S0iX	ed
A34	<u>6</u>	defille
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	 CORE_V1P15_S0iX 283	7
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Ballout and Ball Map



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Ball	# Customer Name - LPDDR3		Ball #	Cu
A35	CORE_V1P15_S0iX		AA15	VSS
A36			AA16	
A37	CORE_V1P15_S0iX		AA17	VSS
429		eine	AA18	
A39	VSS	er,	AA19	UNCO
A4			AA2	
A40	AIREC		AA20	
	DDR_V1P05A_G3		AA20 AA21	UNCO
A38 A39 A4 A40 A41 A42 A43 A44	DDR_V1P05A_G3		AA21 AA22	
A42			AA22 AA23	
A43	DDR_V1P05A_G3	_		UNCO
. 0	0	_	AA24	
A45	VSS		AA25	UNCO
A46		76/11	AA26	
A47	VSS		AA27	UNCO
A48	sinet.		AA28	
A47 A47 A48 A49 A5 A50 A51 A52	VSS		AA29	UNCO
A5	VSS		AA3	VSS
A50	stine		AA30	60
A51	VSS		AA31	6.771.
AJZ	eò ¹¹		AA32	VSS
A53	VSS	225	AA33	
A54		961,	AA34	UNCO
A55	VSS		AA35	
A56	Aines		AA36	UNCO
A57	VSS		AA37	
A54 A55 A56 A57 A58 A59 A6 A7			AA38	VSS
A59	stine		AA39	
A6			AA4	e-
A7	VSS		AA40	VSS
A8		c.	AA41	
A9	MIPI_V1P2A_G3	nder	AA42	DDR_\
AA1	USBHSIC_V1P2A_G3	<u>*</u>	AA43	
AA10			AA44	VSS
A UNC AA11	VSS		AA45	
AA12			AA46	VSS
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AA14	- unou		AA48	<u>Ge</u>
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Ball #	Customer Name - LPDDR3	Indefined
AA15	VSS	ned t
AA16		Actin
AA17	VSS	IUC.
AA18		
AA19	UNCORE_VNN_S4	
AA2	dulli	
AA20	AINEC	
AA21	UNCORE_VNN_S4	
AA22	- dui	undefined
AA23	UNCORE_VNN_S4	
AA24		deth
AA25	UNCORE_V1P15_S0iX	un
AA26	sinet	
AA27	UNCORE_VNN_S4	
AA28	dun	
AA29	UNCORE_VNN_S4	
AA3	VSS	
AA30	d	
AA31	190°	
AA32	VSS	detin
AA33		undefined
AA34	UNCORE_VNN_S4	
AA35		
AA36	UNCORE_VNN_S4	
AA37		
AA38	VSS	
AA39		
AA4	CIII C	d undefined
AA40	VSS	dell
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AA42	DDR V1P05A G3	
AA43		
AA44	VSS	
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Ballout and Ball Map Jalle

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	Ball #	Customer Name - LPDDR3	Ball #	Custo
				70
	AA49	VSS	AB29	8
	AA5	USB_DN[3]	AB3	
	AA50		AB30	
defined unde	AA51	LPDDR3_M0_DQ[18]_B	AB31	
ed u.	AA52		AB32	
efine	AA53	LPDDR3_M0_DQ[21]_B	AB33	
	AA54	defini	AB34	
	AA55	LPDDR3_M0_DQ[07]_B	AB35	
	AA56	sineu	AB36	<u> </u>
	AA57	LPDDR3_M0_DQ[08]_B	AB37	
	AA58	S ²	AB38	
	AA59	DDR_VDDQG_S4	AB39	
	AA6		AB4	USB_SSI
ndefined und	AA7	USB_HSIC_0_STROBE	AB40	
efine	AA8	eo	AB41	
	AA9	USB_HSIC_0_DATA	AB42	
	AB1	dune	AB43	0
	AB10	USB_HSIC_1_STROBE	AB44	
	AB11	-dell'	AB45	21
	AB12	USB RCOMP	AB46	
	AB13		AB47	
Indefined un	AB14		AB48	LPDDR3
ed u.	AB15	, uno	AB49	
efine	AB16		AB5	
	AB17	defii.	AB50	LPDDR3
	AB18	- dun	AB51	
	AB19	Aineu	AB52	LPDDR3_
	AB15 AB2	USBHSIC_V1P2A_G3	AB52	
	AB2		AB55 AB54	LPDDR3
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ed v	AB22		AB56	LPDDR3_
undefined ut	AB23		AB57	
	AB24		AB58	VSS
	AB25	unc	AB59	
	AB26	wineu	AB6	VSS
	AB27	dell	AB7	<u>sino</u>
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AB32	48111
AB33	<u>uno</u>
AB34	Aneo
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AB37	len led v
AB38	
AB39	
AB4	USB_SSIC1_RX_P
AB40	dett
AB41	
AB42	dino
AB43	
AB44	-ed b
AB45	dunce
AB46	odeth
AB47	
AB48	LPDDR3_M0_DM[03]_B
AB49	1100
AB5	
AB50	LPDDR3_M0_DM[02]_B
AB51	unos
AB52	LPDDR3_M0_DQ[23]_B
AB53	<u>n</u> fines
AB54	 LPDDR3_M0_DQ[10]_B
AB55	
AB56	LPDDR3_M0_DQ[09]_B
AB57	uno
AB58	VSS
AB59	0/0/11
AB6	VSS
AB7	ather and
AB8	USB_HSIC_1_DATA
ed vi	unoc
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sined "	Ball #	Customer Name - LPDDR3	Ball #	Cu
delli	AB9	Anne	AC42	-20
	C1	VSS	AC43	VSS
Ā	AC10		AC44	
	AC11	VSS	AC45	VSS
defined undefined undefine	C12		AC46	
in ^{eo}	AC13		AC47	
dein	AC14	VSS	AC48	
	AC15		AC49	VSS
tine	AC16	VSS	AC5	USB_S
,	AC17		AC50	
	AC18	USB_V1P8A_G3	AC51	VSS
	AC19		AC51 AC52	
312	AC2		AC52	VSS
	AC20	UNCORE_VNN_S4	AC54	
sineu	AC21		AC55	LPDDF
dell	AC22	VSS	AC56	
duin	AC23		AC50 AC57	LPDDF
	AC23	UNCORE_VSS_SENSE		
F	-		AC58	
F	AC25		AC59	DDR_\
7	AC26	UNCORE_VNN_SENSE	AC6	
4	AC27		AC7	VSS
	AC28	RESERVED	AC8	
sineu A	AC29	ed ui	AC9	VSS
der	AC3	USB_SSIC0_RX_P	AD1	
	AC30	show	AD10	USB_S
Ą	AC31	UNCORE_VNN_S4	AD11	
A	AC32	defill	AD12	USB_H
A	AC33	UNCORE_VNN_S4	AD13	e-
	AC34	Q	AD14	
	AC35	VSS	AD15	VSS
a VA	AC36		AD16	
fine A	AC37	VSS	AD17	VSS
Inde.	AC38	defille	AD18	
d'	AC39	VSS	AD19	UNCO
4	AC4		AD2	RESER
Ą	AC40	detti	AD20	
ned underined v F F F	AC41	DDRSFRCH0_VDDQG_S4	AD21	UNCO
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AC43	VSS	defini
AC44		
AC45	VSS	
AC46		
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AC48	sines	
AC49	VSS	
AC5	USB_SSIC1_RX_N	. 0
AC50	140	
AC51	VSS	deth
AC52		Indefined
AC53	VSS	
AC54	- det	
AC55	LPDDR3_M0_DQ[14]_B	
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AC57	LPDDR3_M0_DQ[13]_B	
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AD17	VSS	
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AD19	UNCORE_VNN_S4	
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AD23	VSS	AD57	Jefine
AD24		AD58	LPDDR3_M0_DQS[1]_N_B
AD25	UNCORE_VNN_S4	AD59	
AD26	Inde	AD6	VSS
AD27	UNCORE_VNN_S4	AD7	A UNC
AD25 AD26 AD27 AD28	16/11	AD8	VSS
AD29	UNCORE_VSFR_G3	AD9	der
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AD48	LPDDR3_M0_DQ[25]_B	AE28	unde
AD49		AE29	
AD5 AD50 AD51 AD52		AE3	RESERVED
AD50	LPDDR3_M0_DQ[26]_B	AE30	, uno
AD51	Lefine	AE31	
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	AE54	
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	AE7	VSS
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20	AF1	
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	AE38			AF18	USBS:
	AE39		ine	AF19	
	AE4			AF2	VSS
	AE40	edt		AF20	UNCO
	AE41	46811		AF21	
	AE42	uno		AF22	UNCO
	AE43	neo		AF23	6
	AE44	961,		AF24	UNCO
	AE45	70		AF25	
	AE46			AF26	UNCO
d	AE47		2/10.	AF27	
-	AE48	uno		AF28	RESEF
	AE49	LPDDR3_M0_DQ[30]_B		AF29	
	AE5	USB3_RXP[3]		AF3	
	AE50	dunc		AF30	
	AE51	LPDDR3_M0_DQS[3]_N_B		AF31	VSS
	AE52	-der		AF32	40
	AE53	LPDDR3_M0_DQ[27]_B		AF33	CORE
	AE54		_	AF34	
2	AE55	LPDDR3_M0_DQ[12]_B	e'l'	AF35	CORE
	AE56	A UN		AF36	
	AE57	LPDDR3_M0_DQS[1]_P_B		AF37	CORE
	AE58	der		AF38	
	AE59	DDR_VDDQG_S4		AF39	CORE
	AE6	stine		AF4	USB3
	AE7	VSS		AF40	e-
	AE8	0		AF41	CORE
	AE9	USB_SSIC0_TX_P		AF42	
Ś	AF1		9e,	AF43	VSS
	AF10	USB_SSIC0_TX_N		AF44	
	AF11	- stine	1	AF45	RESE
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	AF14	UNCORE_VSFR_G3		AF48	LPDD
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	AF18	USBSSIC_V1P2A_G3
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10fine	AF21	ineo
unoc	AF22	UNCORE_VNN_S4
ned t	AF23	- A UN
	AF24	UNCORE2_V1P05A_G3
	AF25	tefine
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	AF27	
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3_M0_DQ[30]_B	AF29	Auno
XXP[3]	AF3	sineu
d uno	AF30	Joel
3_M0_DQS[3]_N_B	AF31	VSS CORE_VCC1_S0iX
	AF32	<u>ence</u>
3_M0_DQ[27]_B	AF33	CORE_VCC1_S0iX
	AF34	June
3_M0_DQ[12]_B	AF35	CORE_VCC1_S0iX
4 UNC	AF36	
3_M0_DQS[1]_P_B	AF37	CORE_VCC1_S0iX
den	AF38	Lefine
DDQG_S4	AF39	CORE_VCC1_SENSE
FINE	AF4	USB3_RXN[3]
	AF40	entre sine
	AF41	CORE_VSS1_SENSE
SICO_TX_P	AF42	CORE_VCC1_SENSE USB3_RXN[3] CORE_VSS1_SENSE VSS
nd.	AF43	VSS
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E_VSFR_G3	AF48	LPDDR3_M0_DQ[29]_B
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	AF51		AG31		
	AF52	LPDDR3_M0_DQ[31]_B	AG32		
y nur	AF53		AG33	lefting	
	AF54	VSS	AG34		
tined under	AF55		AG35		
	AF56	LPDDR3_M0_DM[1]_B	AG36	2011	
	AF57		AG37	A UNC	
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AH15	VSS		AH49	
AH16			AH5	
AH17	VSS		AH50	LPDDF
AH18	10/1/10		AH51	1.20
AH19	UNCORE_VNN_S4		AH52	VSS
AH2	USB3_RXP[1]		AH53	
1.100		111	AH54	VSS
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AH23	UNCORE VNN S4		AH57	
AH24			AH58	VSS
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AH26			AH6	VSS
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AH30	define		AJ10	
AH31			AJ11	
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AH51	140°C	ed v
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	AJ3	10461	AK1	USB3_V1P05A_G3	
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	AJ46		AK26	VSS	
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	Ball #	Customer Name - LPDDR3		Ball #	Cus
	AK37	CORE_VCC1_S0iX	_	AL17	~0
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X	AK4	6	ne	AL2	
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	AK41	RESERVED		AL21	
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	AK45	VSS		AL25	1000
	AK46	20		AL26	
	AK47			AL27	
	AK48		1/1	AL28	
Jefined undefined uni	AK49	LPDDR3_DRAM_PWROK		AL29	
	AK5	USB3_RXN[2]		AL3	
nder	AK50	76440		AL30	
dui	AK51	LPDDR3_CORE_PWROK		AL31	
atine	AK52			AL32	
	AK53	VSS		AL33	51000
	AK54	<u>2</u>		AL34	o*
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d u	AK57	VSS		AL37	
Idefined undefined un	AK58			AL38	
inde	AK50	VSS		AL30	
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ndefined undefined u	AL10	26.		AL44	
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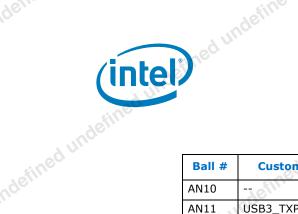
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AM16		•	AM5	
AM17	VSS		AM50	LPDI
AM18			AM51	
AM19	UNCORE_VNN_S4		AM52	VSS
AM2	VSS		AM53	
AM20	Stille	F	AM54	VSS
AM21	DDI_VGG_S0iX	F	AM55	
AM22		F	AM56	VSS
AM23	VSS	in	AM57	
AM24			AM58	VSS
AM25	DDI_VGG_S0iX	-		
AM26		-		VSS
AM27	DDI_VGG_S0iX	_		
AM28		-		USB
AM29	VSS		AM9	7.7
-			AN1	PWR
	Ball # AL50 AL51 AL52 AL53 AL54 AL55 AL56 AL57 AL58 AL59 AL6 AL7 AL8 AL9 AM10 AM11 AM12 AM13 AM14 AM15 AM16 AM17 AM18 AM12 AM13 AM14 AM12 AM13 AM14 AM12 AM13 AM14 AM12 AM13 AM14 AM15 AM20 AM21 AM20 AM21 AM23 AM24 AM25 AM26	Ball # Customer Name - LPDDR3 AL50 AL51 AL52 AL53 AL54 AL55 AL56 AL57 AL58 AL59 AL58 AL6 AL6 AL7 AL8 AL9 AM1 AM10 USB3_TXN[2] AM11 AM12 VSS AM13 AM14 AM15 VSS AM16 AM17 VSS AM18 AM20 AM20	Ball # Customer Name - LPDDR3 AL50 AL51 AL52 AL53 AL54 AL55 AL56 AL57 AL58 AL59 AL58 AL59 AL59 AL6 AL7 AL8 AL9 AL9 AM1 AM1 AM1 AM1 AM13 AM14 AM15 VSS AM16 AM17 VSS AM18 AM20 AM21 DDI_VGG_S0iX AM22	Ball # Customer Name - LPDDR3 AL50 AL51 AL52 AL53 AL54 AL56 AL57 AL58 AL58 AL59 AL58 AL59 AL6 AL59 AL6 AL6 AL7 AL6 AL7 AL6 AM1 AM1 AM1 AM1 AM10 USB3_TXN[2] AM11 AM12 VSS AM14 AM15 VSS AM16 AM17 VSS AM2 VSS AM2 AM51 AM52

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AM43	A UN	
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	AN20			AN54	
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	AN23			AN57	LPDDF
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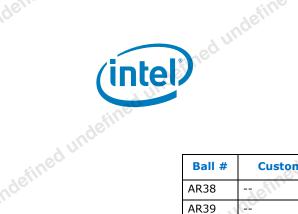
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d un	AP43	LPDDR3_M1_RCOMPPD	AR23	actine	
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d un	AP46	1005	AR26	40111	
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stine	AP52	LPDDR3_M1_DQ[16]_A	AR32	UINC	
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	AR54	-nole		AT34
	AR55	LPDDR3_M1_DQ[03]_A		AT35
	AR56		ci (AT36
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	AR58			AT38
	AR59	DDR_VDDQG_S4		AT39
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stines	AR7	VSS		AT40
	AR8	- lefill		AT41
	AR9	RESERVED	-	AT42
	AT1	2-	-	AT43
	AT10	PCIE_TXP[1]	asi l	AT44
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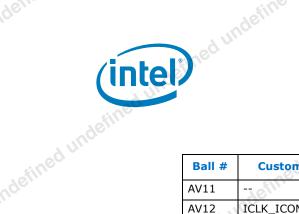
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AT51		AU31	DDI_VGG_S0iX	21
AT51 AT52	VSS	AU32		
AT52		AU33	DDI_VGG_S0iX	
	VSS	AU34		
AT54 AT55 AT56 AT57		AU35	DDI_VGG_S0iX	
AT55	VSS	AU35 AU36		
AT50 AT57		AU30 AU37	DDI_VGG_S0iX	
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AT58	LPDDR3_M1_DQS[0]_N_A	AU38		
AT59		AU39	DDI_VGG_S0iX	2
AT6	VSS	AU4		
AT7		AU40		Yer.
AT8	RESERVED	AU41	DDRSFRCH1_VDDQG_S4	
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	PCIE_TXP[0]	AU45	VSS	
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AU14	F_V3P3A_G3	AU48	122	sine
AU15	0 ^v	AU49	VSS	
AU16	VSS	AU5	PCIE_RXP[1]	
AU17	del	AU50		
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AU2		AU53	VSS	
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AU22	UNCORE_VNN_S4	AU56	302	
AU23	0	AU57	LPDDR3_M1_DQ[02]_A	ndefine
AU24	DDI_VGG_S0iX	AU58		
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AU26	DDI_VGG_S0iX	AU6	Inde	
AU27		AU7	VSS	
AU28		AU8	detill	
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1	AV14	6	20	AV48	LPDDF
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fines	AV19			AV52	LPDDF
	AV2	VSS		AV53	1200
	AV20	<u>76</u> 2		AV54	LPDDF
_	AV21			AV55	
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d un	AV23	Inde		AV57	
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	AV28			AV8	VSS
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AV48	LPDDR3_M1_DM[2]_A
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AV50	LPDDR3_M1_DM[3]_A
AV51	- Ner
AV52	LPDDR3_M1_DQ[24]_A
AV53	1010
AV54	 LPDDR3_M1_DQ[24]_A LPDDR3_M1_DQ[05]_A
AV55	Auno
AV56	LPDDR3_M1_DQ[06]_A
AV57	"Jett
AV58	VSS
AV59	- stine
AV6	VSS
AV7	- ed
AV8	VSS
4V9	
AW1	PCIE_V1P05_G3
AW10	stine
W11	VSS
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W13	48/100
W14	UNO
AW15	VSS
W16	e ^m .
AW17	
AW18	
W19	UNCORE1_V1P05A_G3
AW2	- unou
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AW21	UNCORE_VNN_S4
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der	AW25	DDI_VGG_SENSE	AW59	DDR_VDDQG_S4	d un
	AW26	<u>0</u>	AW6		Aines
	AW27	DDI_VGG_S0iX	AW7	VSS	ge.
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inde	AW57	LPDDR3_M1_DQ[07]_A	AY37	EULEO	,d
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, unc	AY44	96.		B24	COR
lefined undefined un	AY45	- dune		B25	
	AY46	tine		B26	COR
	AY47	-der		B27	14
		LPDDR3_M1_DQ[27]_A		B28	GPIC
	AY49			B29	
	AY5		$U_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_$	B3	
	AY50	LPDDR3_M1_DQS[3]_P_A		B30	
10th	AY51			B31	
unos	AY52	LPDDR3_M1_DQ[25]_A		B32	VSS
hed undefined un	AY53	dun		B33	
	AY54	LPDDR3_M1_DQ[11]_A		B34	JTAC
	AY55	dell		B35	<u>41</u> 0
	AY56	VSS		B36	COR
	AY57			B37	
	AY58	LPDDR3_M1_DQ[09]_A	SUL	B38	GPIC
<i>d V</i>	AY59			230	C1_
	AY6	VSS		B39	
				B4	VSS
d V.	AY7			B40	DDR
	AY8	ICLK_OSCIN		B41	
	AY9	68111		B42	LPD
ed undefined l	B1			B43	
		MIPI_V1P2A_G3		B44	VSS
	B11		ai	B45	
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	B13				
	B14	GPION_V1P8A_G3		B47	
ed u.	B15	uno-		B48	VSS
	B16	MCSI_2_DP[0]		B49	
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0*	BB20	76/11		BB54	VSS
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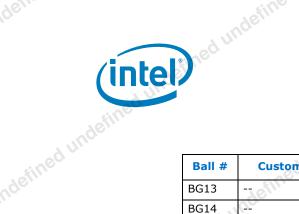
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	BF25	LPC_V3P3A_V1P8A_S4	BF59		nder
	BF26	63	BF6	VSS	
ed undefined undefined un	BF27	VSS	BF7	lefine	
	BF28	of <u>01.</u>	BF8	RESERVED	
-dell.	BF29	GPIOSE_V1P8A_G3	BF9	ineo	
du''	BF3	unde	BG1	PCIeCLK_V1P05A_G3	
atine	BF30		BG10	dunc	
inde	BF31	Jenn	BG11	RTC_EXTPAD	d
du	BF32	VSS	BG12	<u> </u>	efine
	Snis	vined undefined undef	dui	 RTC_EXTPAD 309	uno
	gerr.		100-	- ned	
2 UI	-	nde		Actine	
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ed u		Unoc		den	
efine				dun	

Ballout and Ball Map



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ined	Ball #	Customer Name - LPDDR3	1	Ball #	Cus
	BG13	- Alline	-	BG47	~ed
_	BG14	<u>0</u> 66.	-	BG48	
_	BG15			BG49	VSS
4	BG16	6	ne	BG5	VSS
efined undefined unde	BG17			BG50	
sineo	BG18	- 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,		BG51	LPDDR
dem	BG19	- infine-		BG52	
dulli	BG2	inde		BG53	VSS
fines	BG20			BG54	እ
	BG21	401111		BG55	LPDDR
_	BG22 🔊	<u>70</u> 0.		BG56	
_	BG23			BG57	LPDDR
-	BG24		(n)	BG58	
d un	BG25	Inde		BG59	DDR_\
since	BG26			BG6	
inder	BG27	46111		BG7	VSS
ed u.	BG28	<u>_</u> <u>_</u> <u>U</u> nO		BG8	
	BG29		-	BG9	RTC_X
	BG3	PMC_CORE_PWROK		BH1	<u> </u>
_	BG30		-	BH10	PMC_F
	BG31			BH11	
.0	BG32		ein	BH12	VSS
7 0	BG33	, uno		BH13	
etine	BG34	ined		BH14	MMC1
Inde	BG35	detti	-	BH15	
red	BG36	- dune	-	BH16	SD3_F
Jefill	BG37	- sinev		BH17	
	BG38		-	BH18	SD3_D
	BG39	<u>.</u>	-	BH19	
_	BG4		-	BH2	VSS
. T	BG40		er'	BH20	VSS
-0-	BG40 BG41			BH21	
16tine	BG41 BG42	- sineo	-	BH21 BH22	LPC_R
unos					LFC_K
ineo -	BG43		-	BH23	PMC_F
detin	BG44		-	BH24	
	BG45	- nder,	-	BH25	
	BG46	<u>d</u> un		BH26	UART2
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1efin-		in ^{eo}			

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	ined unde	
Ball #	Customer Name - LPDDR3	6
BG47	rec	
BG48		
BG49	VSS	
BG5	VSS	
BG50	dein	
BG51	LPDDR3_M1_CA[06]	
BG52	sinet	
BG53	VSS	
BG54	- 600	
BG55	LPDDR3_M1_CK_N_B	
BG56	Aetine	
BG57	vss LPDDR3_M1_CK_P_B	
BG58	690	
BG59	DDR_VDDQG_S4	
BG6	<u>A</u> UNC	
BG7	VSS	
BG8		
BG9	RTC_X1	
BH1	dans da	
BH10	PMC_PWRBTN_N	
BH11	RTC_X1 PMC_PWRBTN_N	
BH12	VSS	
BH12 BH13		
BH14	MMC1 RCOMP	
BH15		
BH16	76,	
BH17		
BH18	SD3_D[2]	
BH19	SD3_RCOMP SD3_D[2] VSS	
BH2	VSS	
BH20	V55	
BH21		
BH22	LPC_RCOMP	
BH23		
BH24	PMC_RSTBTN_N	
BH25	tine	
BH26	UART2_RTS_N	
	A UNC	
111-	PMC_RSTBTN_N UART2_RTS_N	
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		48fine			
	Ball #	Customer Name - LPDDR3	Ball #	Customer Name - LPDDR3	
	_		_		NU .
	BH27		BH7		
	BH28	UART2_DATAIN	BH8	VSS	etili
S. S.	BH29	2	BH9	· / L ,	
	BH3		BJ1	ICLK_VSFR_G3	
ned unde	BH30		BJ10	deili	
nu	BH31	60	BJ11	VSS	
	BH32	LPE_I2S0_CLK	BJ12	siner	
	BH33	June	BJ13	VSS	
	BH34	I2C6_CLK/NMI_N	BJ14		. 1
	BH35	CONTRACTOR OF CO	BJ15	MMC1_CMD	
	BH36	I2C2_DATA	BJ16		deth
	BH37		BJ17	VSS	
nde	BH38	VSS	BJ18	sined	
ined une	BH39	uno	BJ19	LPC_FRAME_N/UART0_DATAIN/	
	BH4	PMC_BATLOW_N		SPI2_MISO	
	BH40	LPE_I2S2_FRM	BJ2	sines	
	BH41	A UNC	BJ20	<u>-</u> <u>-</u> <u>-</u> <u>-</u> <u>-</u> <u>-</u> <u>-</u> <u>-</u> <u>-</u> <u></u>	
	BH42	VSS	BJ21	GPIO_ALERT/ISH_GPIO[11]/ ISH_UART_DATAIN	
	BH43	-9°	BJ22		e o
	BH44	LPDDR3_M1_DQ[09]_B	BJ22 BJ23	VSS	detin
	BH45				no.
fined und	BH46	LPDDR3_M1_DM[1]_B	BJ24		
ed u.	BH47		BJ25	FST_SPI_D[2]	
	BH48	RESERVED	BJ26	June	
	BH49		BJ27	VSS	
	BH5		BJ28		
	BH50	LPDDR3_M1_CA[01]	BJ29	d UT	
	BH51		BJ3	PMC_SLP_S3_N	. ne
	BH52	VSS	BJ30	LPE_I2S1_DATAIN	undefine
	BH53		BJ31		n
22.	BH54	LPDDR3_M1_CA[04]	BJ32		
efined un	вн54 ВН55	LPDDR3_MI_CA[04]	BJ33	NFC_I2C_CLK	
efin		ev.	BJ34	d ^u	
	BH56	VSS	BJ35	VSS	
	BH57		BJ36	mole	
	BH58	VSS	BJ37	UARTO_DATAIN	
	BH59	96/1	BJ38		
	BH6	PMC_SUS_STAT_N	BJ39	VSS	detin.
tasheet	ndefine	sined undefined unde	tineo	UARTO_DATAIN VSS 311	UI
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Ba			Ball #	Cus
BJ4	- afine		BK2	VSS
BJ4			BK20	LPC_C
BJ4	24		Une	ISH_U
		ine!	BK21	
UNO BJ4		<u>'96</u>],	BK22	PMC_S
BJ44	····		BK23	
BJ4			BK24	VSS
BJ40			BK25	
B)4: B)4: B)4: B)4: B)4: B)4: B)4: B)4:	A.Y.		BK26	FST_S
BJ48			BK27	ineo.
BJ49			BK28	UART2
BJ5	PMC_PLTRST_N		BK29	
		- ine	ВКЗ	
BJ5		nde.	BK30	
BJ5 BJ5 BJ5 BJ5 BJ5 BJ5 BJ5 BJ5			BK31	
BJ53			BK32	LPE_I
BJ54			BK33	
BJ5	0		BK34	I2C5
B15			BK35	de l'
			BK36	SPI3_
BJ5			BK37	
BJ58		717	BK38	LPE_I
BJ5		<u></u>	BK39	
BJ59 BJ6 BJ7 BJ8 BJ9 BK1 BK1		0.1	BK4	PMC_/
BJ7	PMC_WAKE_N		BK40	LPE_I
BJ8	- unoc		BK41	
BJ9	PMC_SLP_S4_N		BK42	LPDDF
BK1	- 16/11		BK42 BK43	
BRI			BK44	LPDDF
BK1			BK45	
BK1		il.	BK46	LPDDF
BK1 BK1 BK1 BK1 BK1 BK1 BK1 BK1		nolo	BK40 BK47	
BK1			BK48	VSS
BK1	5			
BK1	6 SD3_D[0]		BK49	
BK1	7		BK5	
BK1	8 SPI1_MOSI		BK50	VSS
BK1	$9 - u^{n}$		BK51	
	sinet		BK52	LPDDF
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Ball #	Customer Name - LPDDR3	
3K2	VSS	20
зк20	LPC_CLKOUT[0]/ISH_GPIO[10]/ ISH_UART_DATAOUT	tined u
3K21		
3K22	PMC_SUSPWRDNACK	
3K23	inoe	
3K24	VSS	
3K25	20/11/2	
3K26	FST_SPI_D[1]	
3K27	aneo.	6
ЗК28	UART2_DATAOUT	
3K29	Indi	stined
BK3		
3K30	define	
3K31	Unoc	
3K32	LPE_I2S0_FRM	
BK33	detill	
3K34	I2C5_CLK	
3K35	HAUGO .	
ЗК36	SPI3_MOSI	atino
3K37	un ^c	Jefined
ЗК38	LPE_I2S2_CLK	
3K39		
3K4	PMC_ACPRESENT	
3K40	LPE_I2S2_DATAOUT	
3K41	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
3K42	LPDDR3_M1_DQ[15]_B	
3K43	etine .	e
3K44	LPDDR3_M1_DQ[10]_B	define
3K45		
3K46	LPDDR3_M1_DQS[1]_P_B	
3K47		
3K48	VSS	
3K49	Lefine	
BK5	unde	
BK50	VSS	
3K51	Xe ^{ff}	nja
ЗК52 🗸	LPDDR3_M1_DQ[03]_B	der
nes	 VSS LPDDR3_M1_DQ[03]_B Datasheet	

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	Ball #	Customer Name - LPDDR3	Ball	
	BK53	- SINCO	BL32	20
	BK54	VSS	BL33	12C6_[
	BK55		BL33	
20	BK55	LPDDR3_M1_CKE[0]_A	BL35	I2C2 (
defined unde	BK50 BK57		BL35	
red	BK57 BK58	VSS	BL30	UARTO
96tm.	BK50 BK59		BL38	
	BK6	VSS	BL39	LPE_I2
	BK7		BL4	
	BK8	ISH_GPIO[9]/ISH_SPI_MISO/	BL40	00
	DIG	12S5_FS	BL41	VSS
	BK9		BL41 BL42	
2	BL1	UNCORE_VNN_S4	BL42	LPDDR
ndefined und	BL10			LPDDR
	BL11	SD2 CLK	BL44	
dell.	BL12		BL45	LPDDR
	BL13	VSS	BL46	
	BL14		BL47	LPDDR
	BL15	SD3_D[3]	BL48	0
	BL16	20 <u>—</u> 111	BL49	LPDDR
	BL17	SD3_CLK	BL5	VSS
	BL18		BL50	
Indefined un	BL19	SPI1_MISO	BL51	LPDDR
	BL2		BL52	
nder.	BL20	101110	BL53	LPDDR
	BL21	LPC_CLKRUN_N/	BL54	
	DLLI	UARTO_DATAOUT/SPI2_CLK	BL55	RESER
	BL22	Yellin	BL56	inec.
	BL23	VSS	BL57	LPDDR
	BL24		BL58	
	BL25	FST_SPI_D[3]	BL59	DDR_V
du	BL26		BL6	
undefined	BL27	UART2_CTS_N	BL7	VSS
	BL28	Activ	BL8	
	BL29	, une	BL9	ISH_G I2S5_0
	BL3	PMC_SLP_SOIX_N	DM1	
	BL30	VSS	BM1	0
	BL31	1.71 U.C.	BM10	VSS
		P	BM11	
	dell			
-01	Indefine	ined undefined und		
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		Aefin		
Junos		· UNC-		

Ball #	Customer Name - LPDDR3 I2C6_DATA/SD3_WP 	
BL32	2 <u>0</u>	
BL33	I2C6_DATA/SD3_WP	
BL34		
BL35	I2C2_CLK	
BL36	defin	
BL37	UART0_DATAOUT/SPI3_CLK	
BL38		
BL39	LPE_I2S2_DATAIN	
BL4		
BL40		
BL41	VSS	
BL42	vnoc	
BL43	LPDDR3_M1_DQ[11]_B	
BL44	den	
BL45	LPDDR3_M1_DQ[08]_B	
BL46	sinec	
BL47	LPDDR3_M1_DQS[1]_N_B	
BL48		
BL49	LPDDR3_M1_DQ[01]_B	
BL5		
BL50	dune	
BL51	LPDDR3_M1_DQ[00]_B	
BL52		
BL53	LPDDR3_M1_DQ[02]_B	
BL54	Lefine	
BL55	RESERVED	
BL56	-7.0°	2
BL57	LPDDR3_M1_CS[0]_N	
BL58	nder	
BL59	 LPDDR3_M1_CS[0]_N DDR_VDDQG_S4 	
BL6	181100	
BL7	VSS	
BL8	ineo	
BL9	ISH_GPIO[8]/ISH_SPI_CS[0]_N/ I2S5_CLK	
BM1	Theo	
BM10	VSS	
BM11	nder	
	12S5_CLK 	
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Ball # BM12	adefined	
Ball #	Customer Name - LPDDR3	
BM12	MMC1_D[0]	В
BM13		В
BM14	MMC1_D[2]	B
BM15	6	n ^e B
BM16	VSS	В
BM17		В
BM18	VSS	В
BM19	Inde	В
BM2	ISH_GPIO[7]/I2S4_DATAIN	В
BM15 BM16 BM17 BM18 BM19 BM2 BM20	LPC_CLKOUT[1]/ISH_GPIO[11]/ ISH_UART_DATAIN	B
BM21		В
BM22	VSS	lin B
BM23 BM24 BM25 BM26 BM27 BM28 BM29	Inde	
BM24	LPC_SERIRQ/SPI2_CS[0]_N	B
BM25	40/11	В
BM26	VSS	В
BM27	- aneo	В
BM28	VSS	
BM29	(<i>\\</i>)``	В
BM3		В
BM30		B
BM31	uno	B
BM32	LPE_I2S0_DATAOUT	В
BM33	dell	B
BM30 BM31 BM32 BM33 BM34 BM35 BM36 BM37	VSS	B
BM35	sine	B
BM36	VSS	B
	<u>0.</u>	B
BM38	SPI3_CS[0]_N	
BM39		B
BM4	ISH_GPIO[3]/I2S3_DATAIN	B
BM40	VSS	B
BM41		B
BM42	LPDDR3_M1_DQ[13]_B	B
BM43		B
BM44	. 0'	_
BM45	¢~	
BM39 BM4 BM40 BM41 BM42 BM43 BM43 BM44 BM45	vss de	В

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Ball #		
-	Customer Name - LPDDR3	ndefined u
3M46	VSS	
3M47		detili
3M48		
3M49	nneo	
3M5	dell'	
3M50	LPDDR3_M1_DQS[0]_P_B	
3M51		
3M52	LPDDR3_M1_DQ[04]_B	
3M53	0 n.	
3M54	RESERVED	Indefined
BM55		den
3M56	VSS	
BM57	sines	
3M58	LPDDR3_M1_CKE[0]_B	
3M59		
BM6	PMC_SUSCLK[0]	
3M7	inde	
3M8	ISH_I2C1_DATA/ISH_SPI_MOSI/ I2S5_DATAOUT	undefined
3M9		<i>defill</i>
3N1	UNCORE_VNN_S4	Un
3N10		
3N11	SD2_CMD	
3N12	dune	
3N13	VSS	
3N14	index	
3N15	MMC1_CLK	
3N16	- FILE	undefined
3N17	VSS	dein
3N18	2	un
3N19	SPI1_CLK	
3N2	,,dell	
3N20		
3N21	VSS	
3N22		
3N23	VSS	
3N24	-0 ¹¹¹⁰	
3N25	FST_SPI_D[0]	den
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Ball #	Customer Name - LPDDR3	Ball #	<u>و</u>
BN26	18/11	BN6	5 <u>0</u>
BN27	VSS	BN7	VSS
BN28		BN8	
BN29	60	BN9	RES
BN29 BN3 BN30	ISH_I2C1_CLK/ISH_SPI_CLK/ I2S5_DATAIN	BP1	
BN30	VSS	BP10	VSS
BN31		BP11	
BN31 BN32	dunc	BP12	SD2
BN32 BN33	NFC I2C DATA	BP13	6
		BP14	MMC
BN34		BP15	
BN35	VSS	BP16	SD3
BN36 BN37 BN38 BN39		BP17	
BN37	SPI3_MISO	BP18	VSS
BN38		BP19	
BN39	VSS	BP2	UNC
BIN4	dunc	BP20	LPC_
BN40			ISH_
BN41	VSS	BP21	<u>_</u>
BN42	22	BP22	USB
BN43	LPDDR3_M1_DQ[12]_B	BP23	
BN44 BN45 BN46 BN47 BN48		BP24	FST_
BN45	VSS	BP25	
BN46	cineo	BP26	VSS
BN47	LPDDR3_M1_DM[0]_B	BP27	
BN48	dunc	BP28	LPE_
BN49	LPDDR3_M1_DQ[05]_B	BP29	0
BN5	ISH_GPIO[1]/I2S3_FS	BP3	12
BN50	2	BP30	
BN51	LPDDR3_M1_DQS[0]_N_B	BP31	
	((BP32	VSS
BN52 BN53	VSS	BP33	
BN53 BN54		BP33 BP34	I2C4
BN52 BN53 BN54 BN55	RESERVED	DF 34	DDI
	RESERVED	BP35	
BN56		BP36	I2C1
BN57	RESERVED	BP37	40
_			GPIC
BN58 BN59	DDR_VDDQG_S4		

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3N6	20	defined un
BN7	VSS	fine
3N8		de.
3N9	RESERVED	
3P1	Aething	-
3P10	VSS	
3P11	aneo	-
3P12	SD2_D[3]_CD_N	
3P13		
3P14	MMC1_D[6]	edv
BP15		ndefined
BP16	SD3_D[1]	JUN .
BP17	sineo	1
BP18	VSS]
BP19	duin]
BP2	UNCORE_VNN_S4	1
BP20	LPC_AD[2]/ISH_GPIO[14]/ ISH_12C0_DATA	undefined
BP21	100	red
BP22	USB_OC[0]_N	defille
BP23		un
BP24	FST_SPI_CLK	
BP25	den	
BP26	VSS	
BP27	stines	
BP28	LPE_I2S1_DATAOUT]
BP29	ed u	undefined
BP3	170 -	sineo
BP30		dein
BP31		UI.
BP32	VSS	
BP33	Inde	
BP34	I2C4_CLK/DDI0_DDC_CLK/ DDI2_DDC_CLK/MDSI_DDC_CLK	
BP35	inder]
BP36	I2C1_CLK	1
BP37	SULE	ine'
BP38	GPIO_SW93	detin
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	I2C1_CLK GPIO_SW93 315	5

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tined undefined b		idefilit		
	Ball #	Customer Name - LPDDR3]	Ball #
	BP39	- afine	ł	BR19
	BP4	ISH_GPIO[5]/I2S4_FS	1	Ae
	BP40	VSS		BR2
2	BP41	6	ne	BR20
etimed undefined und	BP42	LPDDR3_M1_DQ[28]_B		BR21
	BP43		Ì	0022
dell	BP44	LPDDR3_M1_DQ[31]_B	Ì	BR22
dull'	BP45	Inde	Ì	BR23
	BP46	LPDDR3_M1_DM[3]_B	Ì	BR24
0*	BP47	26/11	Ì	BR25
	BP48	VSS	1	BR26
	BP49			BR27
	BP5		ine	BR28
dun	BP50	LPDDR3_M1_DQ[19]_B		BR29
	BP51		1	BR3
	BP52	LPDDR3_M1_DQ[16]_B	1	BR30
Jefined undefined un	BP53	, UN	1	BR31
efine	BP54	RESERVED	ł	BR32
	BP55		1	BR33
	BP56	RESERVED	1	BR34
	BD57			BR35
	BP58	VSS	2/17	BR36
du	BP59			BR37
atine	BP6	VSS	•	BR38
inde	BP7		•	BR39
defined undefined un	BP8	PMC_PLT_CLK[0]/ISH_GPIO[10]/	ł	BR4
4etm.		ISH_UART_DATAOUT		BR40
	BP9	- nde]	BR41
	BR1	VSS]	BR42
	BR10		e	BR43
	BR11	SD2_D[1]	Jei,	BR44
ed -	BR12	dui		BR45
ndefined undefined u	BR13	MMC1_D[4]]	BR46
d une	BR14	nde]	BR47
	BR15	SD3_CMD]	BR48
dein	BR16	- stine	1	BR49
	BR17	SPI1_CS[1]_N	1	BR5
	BR18	jê [°]	1	BR50
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10fin-		aneo .		

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	A UT	
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Ball #	Customer Name - LPDDR3	
BR19	LPC_AD[1]/ISH_GPIO[13]/ ISH_UART_RTS_N	ndefined un
BR2		
3R20		
3R21	LPC_AD[3]/ISH_GPI0[15]/ ISH_I2C0_CLK/SPI2_MOSI	
3R22		
BR23	FST_SPI_CS[1]_N	
3R24	unoc	
3R25	UART1_RTS_N	20
BR26	<u></u>	
BR27	UART1_CTS_N	undefined
3R28		01.
3R29	ofines	
BR3	ISH_GPIO[0]/I2S3_CLK	
BR30	LPE_I2S1_CLK	
BR31	Jefine	
BR32	unos	
BR33	I2C5_DATA	undefined
3R34	52- 	sineu
3R35	I2C1_DATA	nder
3R36		, UT
3R37	ISH_GPIO[12]/ISH_UART_CTS_N	
3R38	unos	
3R39	PCIE_CLKREQ[0]_N	
BR4	- 2011	
3R40	- duno	
3R41	VSS	~0
3R42	<u>e</u>	atine
3R43	LPDDR3_M1_DQ[29]_B	d undefined
3R44		
3R45	LPDDR3_M1_DQ[27]_B	
3R46		
3R47	LPDDR3_M1_DQ[23]_B	
3R48		
3R49	LPDDR3_M1_DM[2]_B	
BR5	VSS	
BR50	<u>0</u>	retine
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1. Stine	Ball #	Customer Name - LPDDR3	Ball #	Customer Name - LPDDR3	Indi
nac	BR51	LPDDR3_M1_DQ[18]_B	BT30	1 <u>55.</u>	ed th
	BR52		BT31		defill
	BR53	VSS	BT32	I2C4_DATA/DDI2_DDC_DATA/ DDI2_DDC_DATA/	10.
	BR54			MDSI_DDC_DATA	
ed u	BR55	RESERVED	BT33	den	
Lefine	BR56		BT34	VSS	
unoc	BR57	RESERVED	BT35	stines	
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defili	BR59	VSS	BT37		un ^r
JUL	BR6	<u>, cer</u>	BT38	VSS	^O 9nia
	BR7	PMC_PLT_CLK[4]/ISH_GPIO[14]/ ISH_I2C0_DATA/SPI2_MISO	BT39		dell
	BR8		BT4	ISH_GPIO[4]/I2S4_CLK	
Inor	BR9	PMC_PLT_CLK[1]/ISH_GPIO[11]/	BT40	SD3_WP	
ned t	DR9	ISH_UART_DATAIN/SPI2_CS[1]_N	BT41		
definit	BT1	siner	BT42	VSS	
d une	BT10	SD2_D[0]	BT43	Veline	
sinec	BT11		BT44	LPDDR3_M1_DQ[26]_B	
undefined undefined uno.	BT12	VSS	BT45		d ul
Un	BT13	(+0	BT46	VSS	fine
	BT14	MMC1_D[7]	BT47		inde.
	BT15		BT48	LPDDR3_M1_DQ[21]_B	01
d une	BT16	VSS	BT49	46fitt	
	BT17		BT5	, , , , , , , , , , , , , , , , , ,	
oder	BT18	SPI1_CS[0]_N	BT50	VSS	
od un.	BT19	uno	BT51	den	
atine	BT2	ISH_GPIO[2]/I2S3_DATAOUT	BT52	LPDDR3_M1_DQ[20]_B	
Inde	BT20	VSS	BT53	ATT OCC	ed v
undefined undefined und	BT21	97000	BT54	VSS	undefined
	BT22	SD3_1P8_EN	BT55		uno
	BT23		BT56	VSS	
ed undefined undefined un	BT24	VSS	BT57	den	
stine	BT25		BT58	LPDDR3_M1_CKE[1]_A	
inde	BT26	UART1_DATAIN/UART0_DATAIN	BT59	sinet]
red	BT27	dune	BT6	PMC_PLT_CLK[5]/ISH_GPIO[15]/]
defill	BT28	VSS		ISH_I2C0_CLK/SPI2_MOSI	
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	BT3	75,,	BT8	VSS	detin
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ined T	Ball #	Customer Name - LPDDR3		Ball #	Cus
E	ЗТ9	- AINE		BU41	VSS
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E	3U10			BU43	LPDDF
	3U11	SD2_D[2]	ne	BU44	
efined undefined und E	3U12			BU45	LPDDF
in eo	3U13	MMC1_RCLK/MMC1_RESET_N		BU46	
den	3U14			BU47	LPDDF
ed ullie	3U15	MMC1_D[5]		BU48	
AIN ^{CC}	3U16			BU49	LPDDF
©` E	3U17	SD3_CD_N		BU5	PWM[:
E	3U18 🔊	0 <u>-</u> 22		~9e	ISH_U
	3U19	LPC_AD[0]/ISH_GPIO[12]/		BU50	
		ISH_UART_CTS_N	n_{ij}	BU51	LPDDF
Betimed undefined un E	3U2			BU52	
AIN ^{ec}	3U20			BU53	LPDDF
nder E	3U21	USB_OC[1]_N		BU54	
E	3U22	UNO		BU55	LPDDF
E	3U23	SD3_PWREN_N		BU56	
E	3U24	denn		BU57	LPDDF
	3U25	FST_SPI_CS[0]_N		BU58	
E	3U26			BU59	VSS
Idefined undefined undefined undefined	3U27	UART1_DATAOUT/	117	BU6	
d un		UART0_DATAOUT		BU7	PMC_F
efine	3U28	- ed			ISH_U
Inde	3U29	defili		BU8	
Edu	3U3	VSS		BU9	PMC_F ISH_U
Aefine E	3U30	LPE_I2S0_DATAIN		BV1	
IO E	3U31	dell'		BV1	0
E	3U32	4-UII			DDI_V
E	3U33	I2C3_DATA		BV11	
, e	3U34		e	BV12	VSS
ed V E	3U35	I2C0_DATA		BV13	
ndefined undefined v E	3U36			BV14	DDI_V
E	3U37	GPIO_SW78		BV15	
E	3U38	- dun		BV16	VSS
E	3U39	PCIE_CLKREQ[1]_N		BV17	
E	3U4	- nder		BV18	LPC_V
	3U40	90.		BV19	<u>Ge</u>
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3U41	VSS	d UN
3U42		
3043	LPDDR3_M1_DQ[25]_B	
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3043 3046		
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BU47	LPDDR3_M1_DQS[3]_N_B	
BU48		
BU49	LPDDR3_M1_DQ[22]_B	20
305	PWM[1]/ISH_GPIO[10]/ ISH_UART_DATAOUT	undefined
BU50		unos
3U51	LPDDR3_M1_DQS[2]_N_B	
3U52	define	
BU53	LPDDR3_M1_DQ[17]_B	
BU54	aneo	
3U55	LPDDR3_M1_ODT_A	
BU56	dune	
BU57	LPDDR3_M1_CKE[1]_B	undefined
3U58		retine
3U59	VSS	uno
BU6		
BU7	PMC_PLT_CLK[2]/ISH_GPIO[12]/ ISH_UART_CTS_N/SPI2_CS[0]_N	
3U8	aneo	
3U9	PMC_PLT_CLK[3]/ISH_GPIO[13]/ ISH_UART_RTS_N/SPI2_CLK	
BV1		-9
BV10	DDI_VGG_S0iX	d undefined
3V11		inde.
3V12	VSS	9.
BV13	48/1/1	
3V14	DDI_VGG_S0iX	
BV15	ined	
3V16	VSS	
BV17	dunc	
BV18	LPC_V3P3A_V1P8A_S4	
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	GPIOSE_V1P8A_G3	BV55	LPDDR3_M1_CS[1]_N	-
BV22 BV23 BV24 BV25		BV50 BV57		-
BV23	FST_SPI_CS[2]_N	BV57 BV58	VSS	-
BV24		BV58 BV59		-
BV25	GPIOSE_V1P8A_G3	BV39 BV6	VSS	-
BV20		BV0 BV7		-
BV27 BV28	LPE_I2S1_FRM	BV8	VSS	defined
BV28		BV8 BV9		- siner
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BV30		BW10		-
BV31		BW11	DDI_VGG_S0iX	-
BV31 BV32 BV33	UNCORE_V1P8A_G3	BW12	0	-
		BW13	DDI_VGG_S0iX	_
BV34	I2C3_CLK	BW14		-
BV35		BW15	SDIO_V3P3A_V1P8A_G3	-
BV36	DDI_V1P15_S0iX	BW16		- lefine
BV37		BW17	LPC_V3P3A_V1P8A_S4	inde
BV38	MMC1_RESET_N /SPI3_CS[1]_N	BW18		-
BV39 BV4 BV40 BV41		BW19	VSS	-
BV4	PWM[0]	BW2		-
BV40	DDR_V1P05A_G3	BW20		-
		BW21	GPIOSE_V1P8A_G3	-
BV42	LPDDR3_M1_DQ[30]_B	BW22		-
BV43		BW23	GPIOSE_V1P8A_G3	-
BV44	VSS	BW24		undefin
BV45		BW25	GPIOSE_V1P8A_G3	unu
BV46	LPDDR3_M1_DQS[3]_P_B	BW26		-
BV47 BV48 BV49 BV5		BW27	GPIOSE_V1P8A_G3	4
BV48	VSS	BW28	June	4
BV49	defill	BW29		4
		BW3	VSS	4
BV50	LPDDR3_M1_DQS[2]_P_B	BW30	VSS	4
BV51	1011	BW31	RING	
BV52	VSS	BW32) ⁴ -	dein
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ined	Ball #	Customer Name - LPDDR3]	Ball #	Cus
	BW33	UNCORE_V1P8A_G3		C13	RESER
	BW34	<u>66. – – – – – – – – – – – – – – – – – – </u>		C14	
	BW35	DDI_V1P15_S0iX		C15	MCSI
20	BW36	@	ne	C16	
atimed undefined unde	BW37	DDI_V1P15_S0iX		C17	MCSI
sineo	BW38			C18	
dell	BW39	VSS		C19	MCSI
dui	BW4	Inde	-	C2	
since	BW40			C20	እ
0	BW41	DDR_V1P05A_G3		C21	DDI2
	BW42 🔊	<u>19</u>	-	C22	
	BW43	DDR_V1P05A_G3		C23	CORE
0	BW44		$\langle n \rangle$	C24	
Jeffined undefined une	BW45	VSS	1	C25	VSS
stine	BW46			C26	
inde	BW47	VSS		C27	GPIO_
edu	BW48	dune		C28	
efill	BW49	VSS		C29	
-	BW5	VSS		C3	DDI1_
T T	BW50	<u>2</u>		C30	GPIO_
	BW51	VSS		C31	
171.	BW52		SUI	C32	
ed u	BW53	VSS		C33	SVID
defille	BW54	sinec		C34	
y unc	BW55	VSS		C35	GPIO_
defined undefined un	BW56			C36	
dein	BW57	VSS		C37	GPIO_
<u> </u>	BW58	INOP		C38	e
T T	BW59	0		C39	ISH_G
	BW6		Ś	neu	C1_BP
10	BW7	VSS	Pe,	C4	
ndefined undefined u	BW8			C40	
dein	BW9	DDI_VGG_S0iX		C41	VSS
d ^{ull}	C1	VSS		C42	
sines	C10			C43	LPDDF
nde	C11	MDSI_A_CLKN		C44	
	C12	<u>z uno</u>		C45	LPDDF
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C13	RESERVED	d ur
C14		sineu
215	MCSI_2_DN[0]	
C16		
C17	MCSI 1 CLKP	
C18		
C19	MCSI_1_DP[1]	
C2	0	
C20	- dune	
C21	DDI2_HPD	ed l
C22		Jefine
C23	CORE_VCC1_S0iX	undefined
C24		
C25	VSS	
C26	- dunc	
C27	GPIO_CAMERASB07	
C28	nder	
C29		
С3	DDI1_TXP[3]	
C30	GPIO_CAMERASB04	defi
C31		undefined
C32	Aino	
C33	SVID_ALERT_N	
C34		
C35	GPIO_SUS5/PMC_SUSCLK[1]	
C36	- unos	
C37	GPIO_SUS3/JTAG2_TDI	
C38	C.I.I.	
C39	ISH_GPIO[13]/C0_BPM2_TX/	d undefined
er	C1_BPM2_TX	jd V
C4	26//.	
C40		
C41	VSS	
C42		
C43	LPDDR3_M0_DQ[22]_A	
C44		
C45	LPDDR3_M0_DQ[23]_A	retime
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nder.	C47	LPDDR3_M0_DQS[2]_N_A	D27	22	d un
	C48	<u></u>	D28	VSS	stines
	C49	LPDDR3_M0_DQ[25]_A	D29		Ide.
	C5	MDSI_C_CLKN	D3		
d un	C50		D30	Yetti,	
sinec	C51	LPDDR3_M0_DQS[3]_N_A	D31	- dune	
nde	C52	46/11	D32	SVID_DATA	
edu	C53	LPDDR3_M0_DQ[30]_A	D33	- oder	
defin	C54	- inco	D34	VSS	Inc
ndefined undefined unde	C55	LPDDR3_M0_ODT_B	D35	1 ¹²	ined t
	C56		D36	GPIO_SUS6/PMC_SUSCLK[2]	defin.
	C57	LPDDR3_M0_CKE[1]_A	D37		ne
ind	C58	Left	D38	VSS	
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Aefine	C6	aneo	D4	DDI1_TXN[3]	
y nuno	C7	MDSI_C_DP[2]	D40	GPIO_N0/C0_BPM0_TX/	
	C8	d ^{UII}	D41	C1_BPM0_TX	
den	C9	MDSI_C_DP[0]	D41 D42	VSS	dun
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	D10	MDSI_A_DN[1]	D44	LPDDR3_M0_DQ[21]_A	nde
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dui.	D15	mae	D49		
afine	D16	MCSI_1_CLKN	D45		
Inde	D17	efilt	D3	VSS	undefined
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			D51	LPDDR3_M0_DQ[27]_A	una
	D2	DDI1_TXP[2]	D52		
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etine	D21		D55		
a undefined undefined un	D22	VSS	D56	VSS	
ed the	D23		D57		
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der	E12	Stiller	
	E13	RESERVED	
	E14		
	E15	VSS	
	E16	76	
	E17	MCSI_1_DP[2]	
	E18		10
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Indefined un	E2		
nder	E20		
	E21	DDI2_DDC_CLK/DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/MDSI_A_TE	
	E22	-mde	-
	E23	CORE_VCC1_S0iX	_
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, ur	E25	DDI1_HPD	-
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	E28		
	E29		_
	E3	DDI1_TXN[2]	_
	E30	GPIO_CAMERASB02	
	E31		
	E32		212
<u>م</u> ن	E32 E33	JTAG_TDI	
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nee	E39	GPIO_N1/C0_BPM3_TX/	d une
_C_DN[0]	Acti	C1_BPM3_TX	sineu
	E4		
á.	E40		
ndel.	E41	VSS	
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ed	E45	LPDDR3_M0_DQ[20]_A	undefined uni
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_1_DP[2]	E48		unac
	E49	LPDDR3_M0_DM[03]_A	
Inde	E5	DDI1_TXN[1]	
ed t	E50	A UNC	
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_DDC_CLK/DDI1_DDC_CLK/	E52	- dell	
D_DATAOUT/	E53	VSS	710
_DDC_CLK/MDSI_A_TE	E54	ATRO	ed -
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_VCC1_S0iX	E56		Une
	E57	RESERVED	
_HPD	E58	del'	
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_CAMERASB06	E6	stine	
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TVN[2]	E8		20
TXN[2]	E9	MDSI_A_DP[1]	
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	F10	VSS	du
TDI	F11		
	F12	MDSI_A_DP[2]	
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10-	F19		F50	LPDDR3_M0_DQ[28]_A	ned
	F2	VSS	F51		defin
	F20	DDI2_DDC_DATA/ DDI1_DDC_DATA/UART0_DATAIN/	F52	LPDDR3_M0_DQ[31]_A	
inde		MDSI_DDC_DATA/MDSI_C_TE	F53		
	F21	A UNC	F54	RESERVED	
defille	F22	DDI0_VDDEN	F55		
Jefined undefined under	F23	der	F56	RESERVED	
	F24	CORE_VCC1_S0IX	F57		
en	F25		F58	VSS	A UN
	F26	DDI0_DDC_CLK/DDI1_DDC_CLK/	F59		
		MDSI_DDC_CLK	F6	VSS	der
2	F27		6 F7		
Jefined undefined uno	F28	GPIO_CAMERASB11	F8	VSS	
	F29		F9		
detti	F3	440	G1	DDI2_VDDQ_G3	
dune	F30		G10		
	F31		G11	MDSI_A_DN[2]	
	F32	SVID_CLK	G12		du
	F33		G13	VSS	erine
	F34	JTAG_TCK	G14		INOC
	F35		G15	MCSI_2_DP[1]	
dull	F36 F37	GPIO_SUS8	G16 G17	VSS	
	F37				
inde.	F38	GPIO_N2/C0_BPM2_TX/ C1_BPM2_TX	G18 G19	 MCSI_1_DP[3]	
red	F39	duno	G19 G2		
	F4	DDI1_TXP[1]	G2 G20		undefined
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	F42	LPDDR3_M0_DQ[19]_A	G22 G23	CORE_VCC1_S0iX	Un
2	F43		G23 G24		
ed u.	F44	LPDDR3_M0_DQ[16]_A	G24 G25	VSS	
1efin-	F45		G25 G26		
, uno-	F46	LPDDR3_M0_DM[2]_A	G26 G27	 GPIO_CAMERASB05	
	F47		G27 G28		
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G30 VSS G31 G32 G32 G33 JTAG_PRDY_N G34 G35 VSS G36 G36 G37 GPIO_SUS4/JTAG2_TDO G38 G39 GPIO_N4/C0_BPM0_TX/ C1_BPM0_TX G40 G41 VSS G42 G43 LPDDR3_M0_DQ[03]_A G44 G45 VSS G46 G47 LPDDR3_M0_DM[1]_A G48 G49 LPDDR3_M0_DQ[10]_A G50 G50 H3 H3 H3 H3 H3 H26 DD10_N G47 LPDDR3_M0_DQ[1]_N_A G50 H3 H3		ed ut	ndefine	2	undefil	led -
G31 H10 G32 H11 G32 H12 VSS G33 JTAG_PRDY N H13 G34 H14 MCSL G35 VSS H13 G36 H14 MCSL G37 GPIO_SUS4/JTAG2_TDO H13 G38 H18 MCSL G38 H18 MCSL G40 H18 MCSL G41 VSS H19 G41 VSS H22 DDI1 G42 H24 CORE G44 G64 H24 CORE G44 G64 H24 CORE G45 VSS G5 VSS H29 G50 G51 LPDDR3_M0_DQS[1]_N_A H32 PROC G51 LPDDR3_M0_DQS[1]_N_A G52 H33	undering		odefined undefi	nec		
G31 H10 G32 H11 G32 H12 VSS G33 JTAG_PRDY N H13 G34 H14 MCSL G35 VSS H13 G36 H14 MCSL G37 GPIO_SUS4/JTAG2_TDO H13 G38 H18 MCSL G38 H18 MCSL G40 H18 MCSL G41 VSS H19 G41 VSS H22 DDI1 G42 H24 CORE G44 G64 H24 CORE G44 G64 H24 CORE G45 VSS G5 VSS H29 G50 G51 LPDDR3_M0_DQS[1]_N_A H32 PROC G51 LPDDR3_M0_DQS[1]_N_A G52 H33		Ball #		1		Cus
G31 G32 G33 JTAG_PRDY_N G34 G35 VSS G36 G37 GPIO_SUS4/JTAG2_TDO G38 G39 GPIO_SUS4/JTAG2_TDO G38 G39 GPIO_NA/CO_BPMO_TX/ G4 G41 VSS G42 G43 LPDDR3_MO_DQ[03]_A G44 G43 LPDDR3_MO_DQ[03]_A G44 G43 LPDDR3_MO_DQ[10]_A G44 G45 VSS G46 G43 LPDDR3_MO_DQ[10]_A G44 G45 VSS G50 G51 LPDDR3_MO_DQS[1]_N_A G52 G53 VSS G54 G55 RESERVED G56 G57 RESERVED G58		G30	VSS	-	H10	MDSI
G33 JTAG_PRDY_N G34 G35 VSS G36 G37 GPI0_SUS4/JTAG2_TDO G38 G39 GPI0_N4/C0_BPM0_TX/ G4 G41 VSS G42 G43 LPDDR3_M0_DQ[03]_A G44 G43 LPDDR3_M0_DM[1]_A G44 G43 LPDDR3_M0_DQ[10]_A G44 G45 VSS G46 G45 VSS G46 G47 LPDDR3_M0_DQ[10]_A G48 G50 G51 LPDDR3_M0_DQS[1]_N_A G52 G53 VSS G54 G55 RESERVED G56 G57 RESERVED G58 G59 DDR_VDDQG_S4 G6 G59 <td< td=""><td></td><td>G31</td><td></td><td>-</td><td>H11</td><td></td></td<>		G31		-	H11	
G34 G35 VSS G36 G37 GPIO_SUS4/JTAG2_TDO G38 G39 GPIO_N4/CO_BPMO_TX/ G39 GPIO_N4/CO_BPMO_TX/ G40 G41 VSS G42 G43 IPDDR3_MO_DQ[03]_A G44 G45 VSS G46 G47 IPDDR3_M0_DQ[03]_A G48 G47 IPDDR3_M0_DQ[10]_A G48 G50 G51 IPDDR3_M0_DQS[1]_N_A G52 G53 VSS G50 G51 IPDDR3_M0_DQS[1]_N_A G52 G53 VSS G54 G55 RESERVED G56 G57 RESERVED G58 G59 DDR_VDDQG_S4 G64 G57 </td <td></td> <td>G32</td> <td></td> <td></td> <td>H12</td> <td>VSS</td>		G32			H12	VSS
C1_BPM0_TX H2 DDI1 G4 H2 MCSI G40 H2 DDI1 G41 VSS H2 DDI1 G42 H2 DDI1 G43 LPDDR3_M0_DQ[03]_A H24 CORE G44 G45 VSS H26 DDI0 G45 VSS G46 H26 DDI0 G46 G47 LPDDR3_M0_DM[1]_A H27 G48 G5 VSS H29 G50 VSS G50 H30 G51 LPDDR3_M0_DQS[1]_N_A H31 G52 G53 VSS H30 G53 VSS G54 H30 H34 JTA6 H35 H30 H35 G55 RESERVED H33 G54 G55 G56 H36 VSS		G33	JTAG_PRDY_N	ine	H13	
C1_BPM0_TX H2 DDI1 G4 H2 MCSI G40 H2 DDI1 G41 VSS H2 DDI1 G42 H2 DDI1 G43 LPDDR3_M0_DQ[03]_A H24 CORE G44 G45 VSS H26 DDI0 G45 VSS G46 H26 DDI0 G46 G47 LPDDR3_M0_DM[1]_A H27 G48 G5 VSS H29 G50 VSS G50 H30 G51 LPDDR3_M0_DQS[1]_N_A H31 G52 G53 VSS H30 G53 VSS G54 H30 H34 JTA6 H35 H30 H35 G55 RESERVED H33 G54 G55 G56 H36 VSS	un ¹	G34	34		H14	MCSI
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C1_BPM0_TX H2 DDII G4 H20 MCSI G40 H21 G41 VSS H22 DDII G42 H22 DDII G43 LPDDR3_M0_DQ[03]_A H24 CORE G44 G45 VSS H26 DDII G45 VSS G46 H26 DDII G45 VSS G48 H26 DDII G48 G48 H26 DDII G47 LPDDR3_M0_DM[1]_A H27 H28 VSS G49 LPDDR3_M0_DQS[1]_N_A H30 G50 G51 LPDDR3_M0_DQS[1]_N_A H31 H30 H30 H33 G51 LPDDR3_M0_DQS[1]_N_A G52 H34 JTA6_ G52 G55 RESERVED H33 G54 G56 H36 <	8°	G39	GPIO N4/C0 BPM0 TX/	-	H19	0
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G40 G41 VSS G42 G43 LPDDR3_M0_DQ[03]_A G44 G45 VSS G46 G47 LPDDR3_M0_DM[1]_A G48 G49 LPDDR3_M0_DQ[10]_A G5 VSS G50 G51 LPDDR3_M0_DQS[1]_N_A G52 G53 VSS G54 G55 RESERVED G56 G57 RESERVED G58 G59 DDR_VDDQG_S4 G6 G7 MDSI_C_DP[1] G8 H4 DD11_ H40 VSS		G4				
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G55 RESERVED H34 JTAG_ G56 H35 G57 RESERVED H36 VSS G58 H38 GPIO_ G59 DDR_VDDQG_S4 H39 G7 MDSI_C_DP[1] H4 DDI1_ G8 H40 VSS G9 MDSI_A_DP[3] H41 H1 H42 LPDDF	d un	G52		-	H31	
G55 RESERVED H34 JTAG_ G56 H35 G57 RESERVED H36 VSS G58 H38 GPIO_ G59 DDR_VDDQG_S4 H39 G7 MDSI_C_DP[1] H4 DDI1_ G8 H40 VSS G9 MDSI_A_DP[3] H41 H1 H42 LPDDF	stines	G52		-	H32	PROCH
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G58 H37 G59 DDR_VDDQG_S4 H38 GPI0_ G6 H39 G7 MDSI_C_DP[1] H4 DDI1_ G8 H40 VSS G9 MDSI_A_DP[3] H41 H1 H42 LPDDF		76.		in the	H36	VSS
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116	MCSI_2_CLKP	
117		
118	MCSI_1_DN[3]	
119	1400 <u></u>	. 6
12	DDI1_AUXP	Indefined
120	MCSI_1_DP[0]	
121		
122	DDI1_VDDEN/MDSI_DDC_DATA	
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120	DDI1_DDC_DATA/	60
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132	PROCHOT_N	
133	TUNES	undefined
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	H50	LPDDR3_M0_DQS[1]_P_A	J30	GPIC
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	H6	MDSI_C_DN[1]		C1_I
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		MDSI_C_DN[3]	J40	
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d V.	J11	MDSI_A_DP[0]	J45	LPDI
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ned undefined un	J14	11.10	J48	
		MCSI_2_CLKN	J49	LPDI
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	J19	MCSI_1_DN[0]	J51	LPDI
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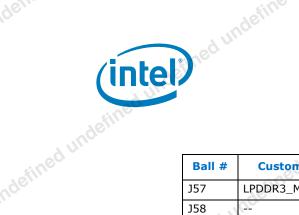
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349	LPDDR3_M0_DQ[14]_A	undefined
J5	DDI0_TXP[0]	
J50	Inde	
J51	LPDDR3_M0_DQ[15]_A	
J52	Lefill	
J53	LPDDR3_M0_DQ[13]_A	
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-	J59	DDR_VDDQG_S4		K39	
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dull	K1	- inde	-	K42	LPDDF
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0	K11	2011		K44	LPDDF
	K12	MDSI_A_DN[0]	-	K45	
	K13			K46	LPDDF
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Jeffined undefined une	K15	Inde		K48	VSS
stines	K16	MCSI_3_CLKN		K49	
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edu	K18	MCSI_RCOMP	-	K50	VSS
efine	K19			K51	
	K2	VSS		K52	LPDDF
	K20	DDI1_BKLTCTL/MDSI_A_TE/	-	К53	
	sines	MDSI_C_TE		K54	VSS
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defined undefined un	K22	DDI0_BKLTCTL		K56	LPDDF
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	K27	- nde		K7	E.
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a une	K32	GPIO_CAMERASB01		L12	
sineu	K33	- du		L13	VSS
dell	K34	GPIO_SUS10		L14	
	K35			L15	VSS
	K36	GPIO_SUS7/PMC_SUSCLK[3]		L16	
326 undefined	Inderr	GPIO_SUS7/PMC_SUSCLK[3]	nde	ine	
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	Ballout and Ball Map	
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K4	DDI0_TXN[0]	
K40	GPIO_N8/C0_BPM1_TX/ C1_BPM1_TX	
K41		
K42	LPDDR3_M0_DQ[00]_A	
K43	, uno	
K44	LPDDR3_M0_DQ[05]_A	du
K45	<u> </u>	
K46	LPDDR3_M0_DQS[0]_P_A	undefined
K47	0	V [*]
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K49	- unot	
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K50	VSS	
K51	- J UNC	
K52	LPDDR3_M0_DQ[12]_A	-d 1
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K54	VSS	undefined
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K56	LPDDR3_M0_CKE[0]_B	
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K58	VSS	
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afine	L21	DDI0_BKLTEN	L55	LPDDR3_M0_CA[5]	
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10	L27	VSS	C L7	VSS	
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	142	LPDDR3_M0_DQ[01]_A	M22 M23		
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nder	L49	LPDDR3_M0_CA[0]	M29		.6
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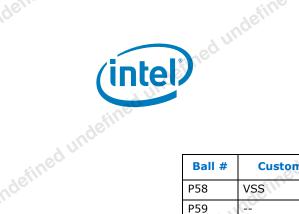
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M42	VSS	N22	
M43	tines	N23	
M44	LPDDR3_M0_DQ[06]_A	N24	
M45		N25	
M46	LPDDR3_M0_DM[0]_A	N26	
M47	-noie.	N27	6777
M48	RESERVED	N28	
M49		N29	
M5		N3	VSS
M50	LPDDR3_M0_CA[1]	N30	
M51		N31	
M52	VSS	N32	
M53		N33	
M54	LPDDR3_M0_CA[4]	N34	0
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M55	VSS	N36	
		N36	
M57			
M58	VSS	N38	
M59		N39	
M6	DDI0_TXP[2]	N4	
M7	unc	N40	
M8	DDI0_AUXN	N41	
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N1	USB_V3P3A_G3	N43	<u>Ge</u>
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	N6	cineo	P4	DDI0_RCOMP_N	<i>.</i>
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R59	VSS	
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	39			V19	VSS
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U	49	VSS		V29	VSS
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	50		SUL	V30	
	51	VSS		V31	
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	54			V34	CORE
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	59	VSS)ej	V39	
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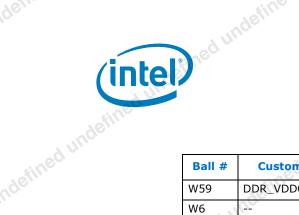
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W22	UNCORE_VNN_S4	W56	<u>4</u> Un	
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Y42	tetin	-
Y43	uno	-
Y44	inco	-
Y45	dein	
Y46		ind
Y47	140°	edu
Y48	LPDDR3_M0_DQ[20]_B	undefined und
Y49		uno
Y5		7
Y50	LPDDR3_M0_DQS[2]_P_B	
Y51	dun	
Y52	LPDDR3_M0_DQ[22]_B	
Y53	noe	
Y54	LPDDR3_M0_DQ[04]_B	undefined un
Y55	tile.	sineo
Y56	VSS	dein
Y57		a un
Y58	LPDDR3_M0_DQ[06]_B	
Y59		
Y6	USB_DP[3]	-
Y7	48/11	
Y8	VSS	
Y9	-in ^{eo}	d'u'
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Package Information



ndefined undefin Package Information 21

ndefined unde The SoC comes in Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Care should be taken to avoid contact with the package inside this area.

ndefined undefi **SoC Attributes** 21.1

Table 165. SoC Attributes

defined undefined uno 11.1 Table 165	DOTTOM SIC	ie. Care snoui	a de taken to avoid	contact with the p	
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Table 165	5. SoC Attril	butes			sined
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ed un		Ball count	1380	592	detri
efine		Ball pitch	0.4mm	0.65mm	24
		Z-height	0.937mm	1.002mm	
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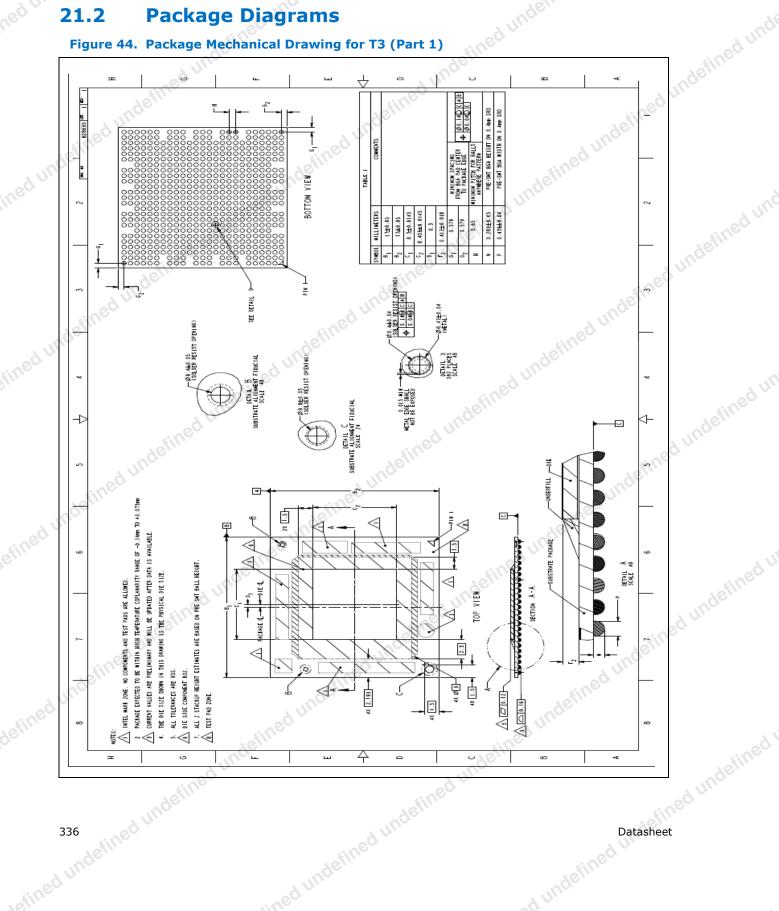
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Package Information



Package Diagrams 21.2

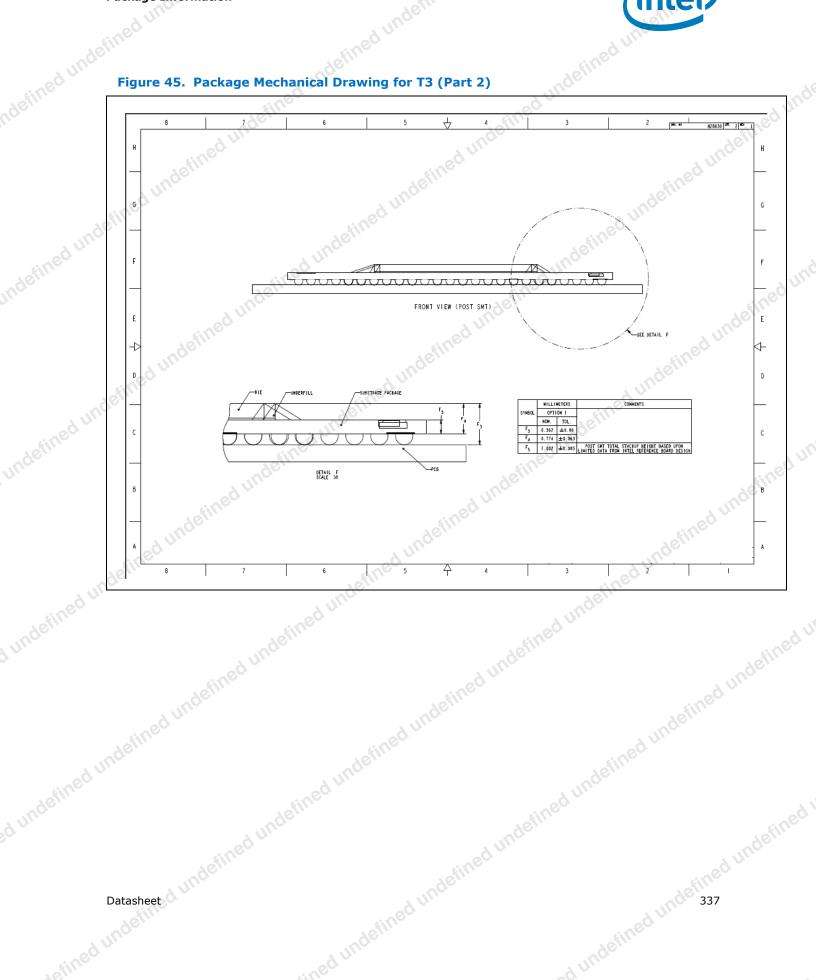
Figure 44. Package Mechanical Drawing for T3 (Part 1)



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Package Information





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Package Information

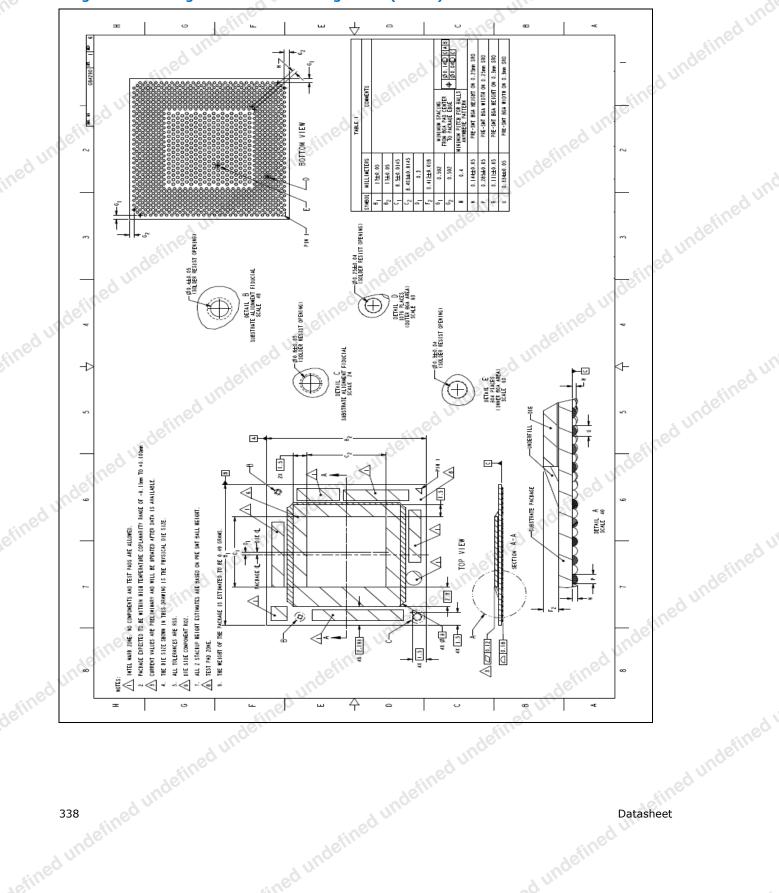


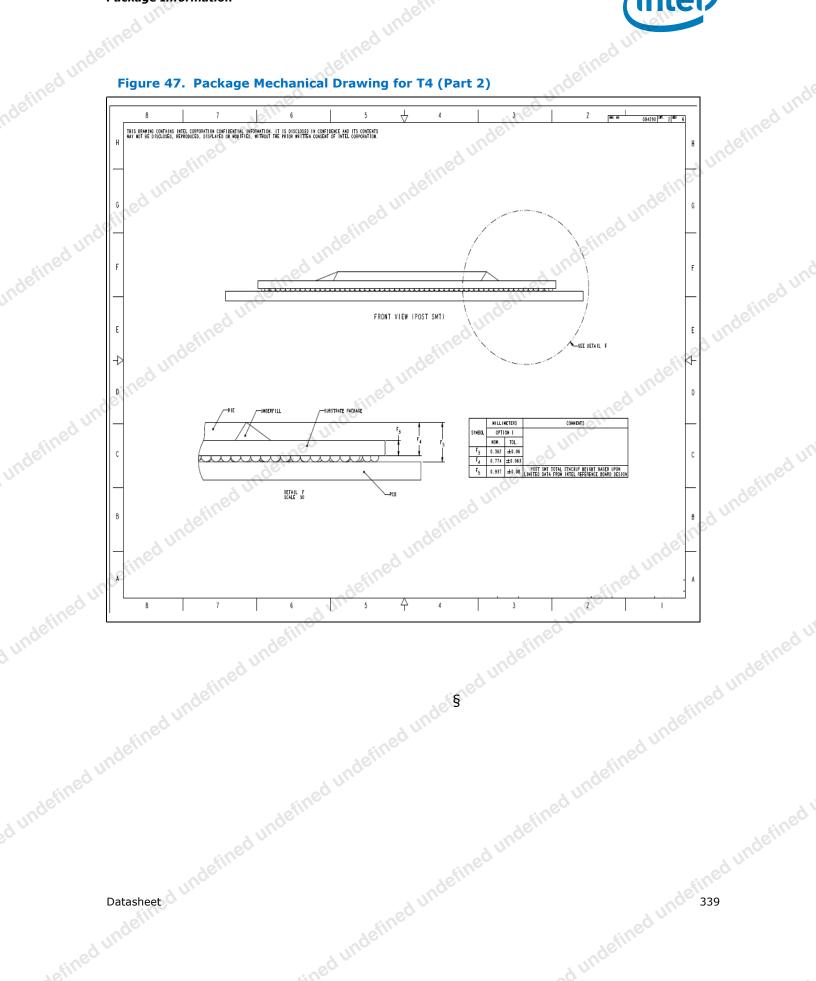
Figure 46. Package Mechanical Drawing for T4 (Part 1)

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