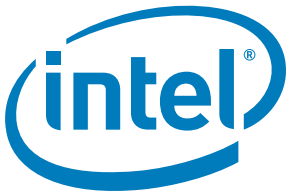


Mobile Intel® 965 Express Chipset Family

Datasheet

Revision 003

June 2007

Contents

Figures

Tables

Revision History

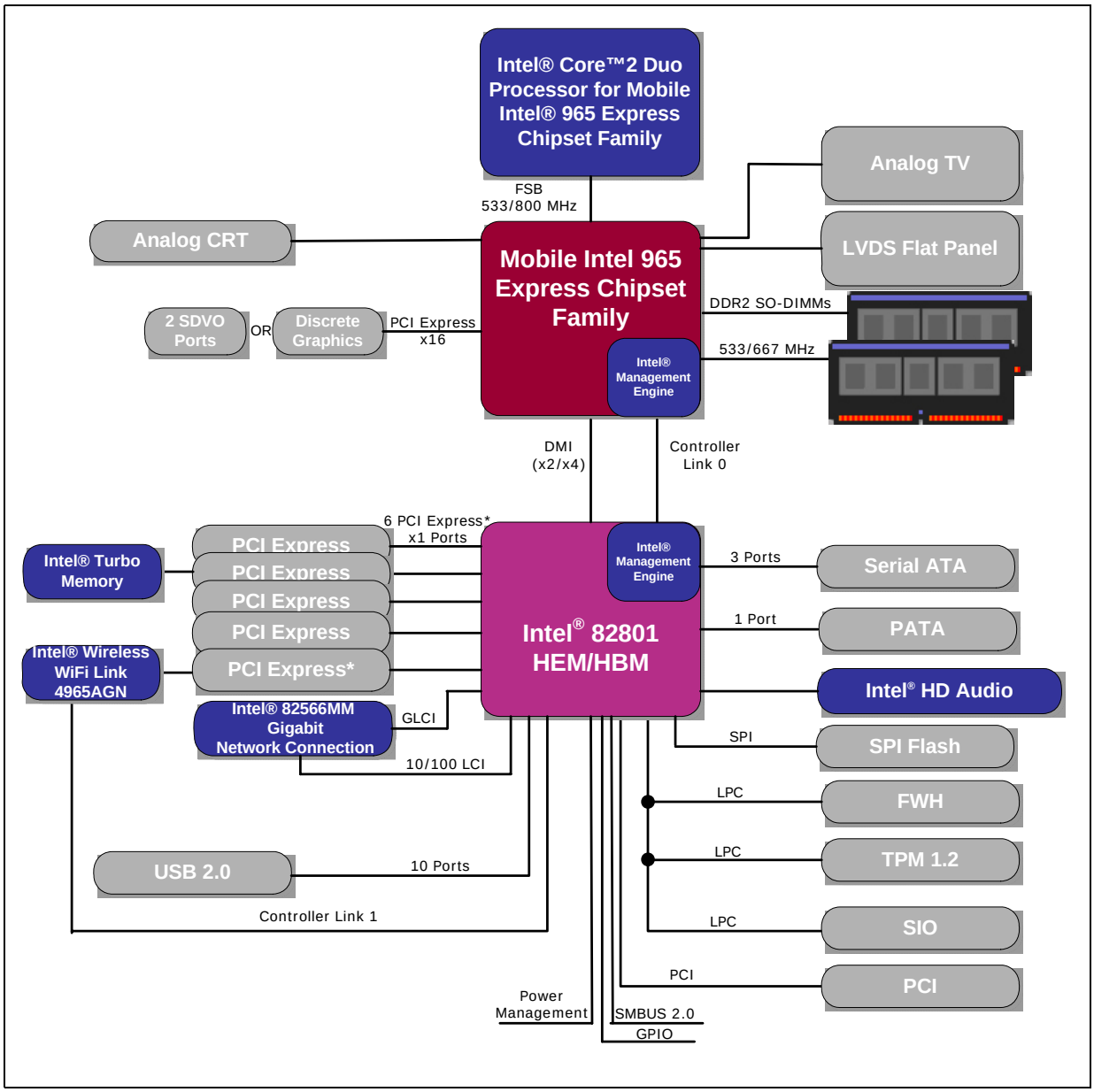
Revision Number	Description	Revision Date
001	Initial Release	May 2007
002	Changes made to disclaimer page	June 2007
003	• Chapter 1 — Updated Figure 1 — Added Section 1.3 - Mobile Intel® GL960 Express Chipset Feature Support — Added Section 1.4 - Mobile Intel® GME965 Express Chipset Feature Support — Added Section 1.5 - Mobile Intel® GLE960 Express Chipset Feature Support — Section 1.1.6 - Replaced “Support for Intel 82801 GBM/GHM (base variant) only” with “Support for Intel 82801 HEM\HBM (base variant) only“ — Section 18.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 18.1.2 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 20.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 20.1.2 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 21.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 21.1.2 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 21.2 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 21.2.2 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.1.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.2 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.2.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.3 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.3.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.4 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset — Section 22.4.1 - Added notes to Host Bridge Device ID for support for Mobile Intel GME965 and GLE960 Express Chipset	June 2007

§

1 Introduction

The Mobile Intel® 965 Express Chipset family is designed for use in Intel's next generation Intel® Centrino® Duo processor technology. Figure 1 provides a system block diagram.

Figure 1. Intel® Centrino® Duo Processor Technology with Mobile Intel® 965 Express Chipset Family (G)MCH



The Mobile Intel 965 Express Chipset family (also referred to as (G)MCH) can be enabled to support either integrated graphics or external graphics. When external graphics is enabled, the x16 PCI Express* Graphics attach port is utilized, and the integrated graphics ports are disabled.

1.1 Mobile Intel® PM965 Express Chipset Feature Support

1.1.1 Processor Support

- Intel® Core™2 Duo Mobile Processor for Mobile Intel 965 Express Chipset Family
- 533-MHz and 800-MHz FSB support
- Source synchronous double-pumped (2x) address
- Source synchronous quad-pumped (4x) data
- Intel® Dynamic Front Side Bus Frequency Switching
- Support for DBI (Data Bus Inversion)
- Support for MSI (Message Signaled Interrupt)
- 36-bit interface to addressing, allowing the CPU to access the entire 64 GB of the (G)MCH memory address space
- 12-deep, in-order queue to pipeline FSB commands
- AGTL+ bus driver with integrated AGTL termination resistors

1.1.2 System Memory Support

- Supports dual-channel DDR2 SDRAM
- One SO-DIMM connector (or memory module) per channel
- Two memory channel configurations supported
  - — Dual channel interleaved
  - — Dual channel asymmetric
- Maximum memory supported: 4 GB
- Intel® Flex Memory Technology support
- 64-bit wide per channel
- Support for DDR2 at 667 MHz and 533 MHz
- 256-Mb, 512-Mb, and 1-Gb memory technologies supported
- Support for x8 and x16 devices
- Support for DDR2 On-Die Termination (ODT)
- Supports partial writes to memory using data mask signals (DM)
- Dynamic rank power-down
- No support for Fast Chip Select mode
- No support for ECC

1.1.3 Discrete Graphics using PCI Express* Graphics Attach Port

- One 16-lane (x16) PCI Express port for external PCI Express-based graphics card
  - — May also be configured as a PCI Express x1 port

1.1.4 Direct Management Interface

- Chip-to-chip interface between (G)MCH and 82801 GBM/GHM
- Configurable as x2 or x4 DMI lanes
- DMI x2 lanes reversed is not supported
- DMI polarity inversion is supported
- 2-GB/s (1-GB/s each direction) point-to-point interface to Intel® 82801 GBM/GHM
- 32-bit downstream address
- DMI asynchronously coupled to core
- APIC and MSI interrupt messaging support
- Supports SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.1.5 Power Management

- Supports ACPI 3.0
- S States: S0, S3, S4, S5
- C States: C0, C1, C1E, C2, C2E, C3, C4, C4E and Intel® Enhanced Deeper Sleep states
- M States: M0, M1, M-off
- PCI Express Link States: L0, L0s, L1, L2/L3 ready, L3
- H_CPUSLP# output
- H_DPWR# support
- Intel® Rapid Memory Power Management (Intel® RMPM)
- Intel® Dynamic Front Side Bus Frequency Switching

1.1.6 Security and Manageability (Intel® Active Management Technology)

- Remote Asset Management
- Remote Diagnosis and Repair
- Remote Agent Presence
- Wireless OOB Management
- System Defense Network Isolation
- Mobile Power Management Policies
- Third-party Non-Volatile Storage
- Intel® Active Management Technology (Intel® AMT) 2.5 with both wired and wireless LAN support

- Controller Link interface to Intel 82801 HEM/HBM for extended manageability functionality

1.1.7 Package

- FCBGA
- Ball Count: 1299 balls
- Package Size: 35 mm x 35 mm
- Ball pitch: Variable pitch; 31.5-mil minimum pitch

1.1.8 Intel® Stable Image Platform Program

Supported

1.2 Mobile Intel® GM965 Express Chipset Feature Support

All features supported by Mobile Intel PM965 Express Chipset are supported by Mobile Intel® GM965 Chipset unless otherwise noted below. Additional features are also listed.

1.2.1 PCI Express Graphics Attach Port

- One 16-lane (x16) PCI Express port for external PCI Express-based graphics card
  - — May also be configured as a PCI Express x1 port for video capture
- Lane reversal is supported
- Polarity Inversion is supported

1.2.2 Integrated Graphics

- Mobile Intel® Graphics Media Accelerator X3100 (Mobile Intel® GMA X3100)
- Supports a QXGA maximum resolution of 2048 x 1536 at 60-Hz, 32-bpp reduced blanking timing (driver limited)†
- 500-MHz core render clock at 1.05-V core voltage
- Supports Analog TV-Out, LVDS, Analog CRT and SDVO
- Intel® Smart 2D Display Technology (Intel® S2DDT)
- Video Capture via x1 concurrent PCI Express port
- Dynamic Video Memory Technology (DVMT 4.0; 384 Maximum)
- Intel® Clear Video Technology
  - — MPEG-2 Hardware Acceleration
  - — WMV9 Hardware Acceleration
  - — ProcAmp
  - — Advanced Pixel Adaptive De-interlacing
  - — Sharpness Enhancement
  - — De-noise Filter
  - — High Quality Scaling

  - — Film Mode Detection and Correction
  - — Intel® TV Wizard
- Microsoft DirectX* 9
- Intermediate Z
- SGI OpenGL* 1.5
- Hardware Pixel Shader 3.0
- HW rotation

Note: †Indicated maximum resolutions may not be supported on all ports or in all dual display configurations.

1.2.2.1 Analog CRT

- Integrated 300-MHz RAMDAC
- For supported resolutions, refer to the OMP tool
- Support for CRT hot plug

1.2.2.2 Dual Channel LVDS

- For supported resolutions, refer to the OMP tool
- 25-112 MHz single/dual channel
  - — Single channel LVDS interface support: 1 x 18-bpp OR 1 x 24-bpp (Type 1 only), compatible with VESA LVDS color mapping)
  - — Dual channel LVDS interface support: 2 x 18-bpp panel support or 2 x 24-bpp panel (Type 1 only)
  - — TFT panel type supported
- Pixel dithering for 18-bit TFT panel to emulate 24-bpp true color displays
- Panel Fitting, Panning, and Center mode supported
- Standard Panel Working Group (SPWG) v.3.5 specification compliant
- Spread spectrum clocking supported
- Panel power sequencing support
- Integrated PWM interface for LCD backlight inverter control

1.2.2.3 Analog TV-Out

- Three integrated 10-bit DACs
- MacroVision* support
- Overscaling
- NTSC/PAL
- Component, S-Video, TV D connector, and Composite Output Interfaces
- SDTV 480i support†
- EDTV 480p support†
- HDTV 720p, 1080i support†
- True HDTV 1080p support†

† The Mobile Intel GM965 and GL960 Express chipsets support the equivalent PAL resolutions.

1.2.2.4 SDVO Ports

- Two SDVO ports supported
  - SDVO pins are muxed onto the PCI Express Graphics attach port pins
  - DVI 1.0 support for External Digital Monitor
  - HDCP 1.2 support
  - Display Hot Plug support
  - Second CRT support
- Supports appropriate external SDVO components (HDMI, DVI, LVDS, Analog TV-Out, Analog CRT)
- I^2C* channel provided for control
- SDTV 480i support†
- EDTV 480p support†
- HDTV 720p, 1080i support†
- True HDTV 1080p support†

† The Mobile Intel GM965 and GL960 Express chipsets supports the equivalent PAL resolutions.

1.2.3 Power Management

- Graphics Display Adapter States: D0, D3
- Intel® Display Power Saving Technology (Intel® DPST) 3.0
- Intel® Smart 2D Display Technology (Intel® S2DDT)
- Dynamic Display Power Optimization* (D^2PO) Panel Support
- Intel® Automatic Display Brightness
- Intel® Display Refresh Rate Switching

1.2.4 Intel Stable Image Platform Program

- Supported

1.3 Mobile Intel® GL960 Express Chipset Feature Support

All features supported by Mobile Intel GM965 Express Chipset are supported by Mobile Intel® GL960 Express Chipset unless otherwise noted below. Additional features are also listed.

1.3.1 Processor Support

- Intel® Celeron® processor
- 533-MHz FSB support

1.3.2 System Memory Support

- Support for DDR2 at 533 MHz only
- Maximum memory supported: 2 GB

1.3.3 PCI Express Graphics Attach Port

- PCI Express* Graphics is disabled

1.3.4 Integrated Graphics

- 400-MHz core render clock at 1.05-V core voltage

1.3.5 ICH Support

- Support for Intel 82801 HBM (base variant) only

1.3.6 Power Management

All Power Management features supported by Mobile Intel PM965 Express Chipset are supported by Mobile Intel GL960 Express Chipset unless otherwise noted below.

- Intel RMPM is not supported
- Intel Dynamic Front Side Bus Frequency Switching is not supported

1.3.7 Intel Advanced Management Technology

- Not supported

1.3.8 Intel Stable Image Platform Program

- Not supported

1.4 Mobile Intel® GME965 Express Chipset Feature Support

All features supported by Mobile Intel GM965 Express Chipset shall be supported by Mobile Intel GME965 Express Chipset unless otherwise noted below. Additional features are also listed below.

1.4.1 Integrated Graphics

1.4.1.1 Analog TV-Out

- No Macrovision* support

1.5 Mobile Intel® GLE960 Express Chipset Feature Support

All features supported by Mobile Intel GL960 Express Chipset shall be supported by Mobile Intel GLE960 Express Chipset unless otherwise noted below. Additional features are also listed below.

1.5.1 Integrated Graphics

1.5.1.1 Analog TV-Out

- No Macrovision support

1.6 Terminology

(Sheet 1 of 2)

Term	Description
ACPI	Advanced Configuration and Power Interface
CPU	Central Processing Unit or processor
CRT	Cathode Ray Tube
DBI	Dynamic Bus inversion
DDR2	Second generation Double Data Rate SDRAM memory technology.
DMI	Direct Media Interface. The chip-to-chip interconnect between the chipset and the 82801 GBM/GHM. It is an Intel proprietary interface.
DVI*	Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group) DVI Spec. Rev. 1.0.
ECC	Error Correction Code
FSB	Front Side Bus. Connection between chipset and the processor. Also known as the Host interface.
(G)MCH	Graphics Memory Controller Hub
HDMI	High Definition Multimedia Interface - HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. It transmits all ATSC HDTV standards and supports 8-channel digital audio, (additional details available through http://www.hdmi.org).
Host	This term is used synonymously with processor.
I^2C	Inter-IC (a two wire serial bus created by Philips).
iDCT	Inverse Discrete Cosine Transform.
Intel® 82801 HEM\HBM	The I/O Controller Hub component that contains the primary PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the (G)MCH over a proprietary interconnect called DMI. Also referred to as Intel ICH8M throughout the document.
INTx	An interrupt request signal where X stands for interrupts A,B,C and D.
ISIPP	Intel® Stable Image Platform Program.
LCD	Liquid Crystal Display
LFP	Local Flat Panel

(Sheet 2 of 2)

Term	Description
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
NCTF	Non-Critical to Function
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
PWM	Pulse Width Modulation
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
SDVO	Serial Digital Video Out (SDVO). Digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For the (G)MCH, it is multiplexed on a portion of the x16 graphics PCI Express* interface.
SDVO Device	Third-party codec that utilizes SDVO as an input. May have a variety of output formats, including HDMI, DVI, LVDS, TV-out, etc.
TMDS	Transition Minimized Differential Signaling.
TTM	Time to Market
VLD	Variable Length Decoding
VTT	Front Side Bus Power Supply (VCCP)
x1	A Link or Port with one Physical Lane
x16	A Link or Port with sixteen Physical Lanes

1.7 Reference Documents

Document	Document No./Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express Specification 1.1	http://www.pcisig.com
PCI Express Architecture Mobile Graphics Low Power Addendum to the PCI Express Base Specification Revision 1.0	http://www.pcisig.org
Standard Panel Working Group (SPWG) v.3.5 Specification	http://www.spwg.org/
Mobile Intel® 965 Express Chipset Family Specification Updatehttp://www.intel.com/design/mobile/specupdt/316273.htm	http://www.intel.com/design/mobile/specupdt/316273.htm
Intel® Core™2 Duo Processor for Mobile Intel® 965 Express Chipset Family Datasheet	http://www.intel.com/design/mobile/datashts/316745.htm

Document	Document No./Location
Intel® Core™2 Duo Processor for Mobile Intel® 965 Express Chipset Family Specification Update	http://www.intel.com/design/mobile/specupdt/316746.htm.
JEDEC Double Data Rate 2 (DDR2) SDRAM Specification	http://www.jedec.com
DDR2 JEDEC Specification Addendum	http://www.intel.com/technology/memory/#Specs
Intel® I/O Controller Hub 8 (ICH8) Datasheet	www.intel.com/design/chipsets/datashts/313056.htm
Intel® I/O Controller Hub 8 (ICH8) Specification Update	http://www.intel.com/design/chipsets/specupdt/313057.htm
VESA Specification	http://www.vesa.org
TIA/EIA-644 Standard	http://www.tiaonline.org
Digital Visual Interface (DVI) Specification	http://www.ddwg.org/downloads.asp

2 Signal Description

This section describes the (G)MCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type:

Notations	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

Signal	Description
AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The (G)MCH integrates AGTL+ termination resistors, and supports V_{TT} from 0.83 V to 1.65 V (including guardbanding).
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications. The buffers are not 3.3-V tolerant. Refer to the PCI Express specification.
CMOS	CMOS buffers. 1.5-V tolerant
HVCMOS	High Voltage CMOS buffers. 3.3-V tolerant
LVCMOS	Low Voltage CMOS buffers. Vtt tolerant
COD	CMOS Open Drain buffers. 3.3-V tolerant
SSTL-1.8	Stub Series Termination Logic: These are 1.8-V capable buffers. 1.8-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
LVDS	Low Voltage Differential signal interface
Ref	Voltage reference signal

Note: System Address and Data Bus signals are logically inverted signals. The actual values are inverted from what appears on the system bus. This must be considered and the addresses and data bus signals must be inverted inside the (G)MCH. All processor control signals follow normal convention: A 0 indicates an active level (low voltage), and a 1 indicates an active level (high voltage).

Note: All pins marked RSVD should be left NC.

2.1 Host Interface

Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the host bus (VCCP).

2.1.1 Host Interface Signals

Signal Name	Type	Description
H_A#[35:3]	I/O AGTL+ 2X	**Host Address Bus:** HA#[35:3] connects to the processor address bus. During processor cycles the HA#[35:3] are inputs. The (G)MCH drives HA#[35:3] during snoop cycles on behalf of PCI Express/ Integrated Graphics or ICH8M. HA#[35:3] are transferred at 2x rate. Note that the address is inverted on the processor bus.
H_ADS#	I/O AGTL+	**Host Address Strobe:** The system bus owner asserts H_ADS# to indicate the first of two cycles of a request phase. The (G)MCH can also assert this signal for snoop cycles and interrupt messages.
H_ADSTB#[1:0]	I/O AGTL+ 2X	**Host Address Strobe:** HA#[31:3] connects to the processor address bus. During processor cycles, the source synchronous strobes are used to transfer HA#[35:3] and HREQ#[4:0] at the 2x transfer rate. Strobe — Address Bits HADSTB#0 — HA#[15:3], HREQ#[4:0] HADSTB#1 — HA#[35:16
H_AVREF H_DVREF	I A	**Host Reference Voltage:** Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface.
H_BNR#	I/O AGTL+	**Host Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
H_BPRI#	O AGTL+	**Host Bus Priority Request:** The (G)MCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the H_LOCK# signal was asserted.
H_BREQ#	I/O AGTL+	**Host Bus Request:** The (G)MCH pulls the processor bus H_BREQ# signal low during H_CPURST#. The signal is sampled by the processor on the active-to-inactive transition of H_CPURST#. H_BREQ# should be tri-stated after the hold time requirement has been satisfied.

Signal Name	Type	Description
H_CPURST#	O AGTL+	**Host CPU Reset:** The H_CPURST# pin is an output from the (G)MCH. The (G)MCH asserts H_CPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. H_CPURST# allows the processor to begin execution in a known state.
H_CPUSLP#	O LVCMOS	**Host CPU Sleep:** When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. (This is a CMOS type buffer with Vtt - NOT 3.3 volts).
H_D#[63:0]	I/O AGTL+ 4X	**Host Data:** These signals are connected to the processor data bus. HD#[63:0] are transferred at 4x rate. Note that the data signals are inverted on the processor bus depending on the HDINV#[3:0] signals.
H_DBSY#	I/O AGTL+	**Host Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
H_DEFER#	O AGTL+	**Host Defer:** Signals that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
H_DINV#[3:0]	I/O AGTL+	**Host Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. H_DINV# Data Bits H_DINV#3 H_D#[63:48] H_DINV#2 H_D#[47:32] H_DINV#1 H_D#[31:16] H_DINV#0 H_D#[15:0]
H_DPWR#	I/O AGTL+	**Host Data Power:** Used by (G)MCH to indicate that a data return cycle is pending within 2 H_CLK cycles or more. Processor uses this signal during a read-cycle to activate the data input buffers in preparation for H_DRDY# and the related data.
H_DRDY#	I/O AGTL+	**Host Data Ready:** Asserted for each cycle that data is transferred.

Signal Name	Type	Description
H_DSTBP#[3:0] H_DSTBN#[3:0]	I/O AGTL+ 4X	**Host Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD#[63:0] and HDINV#[3:0] at the 4x transfer rate. Strobe — Data Bits H_DSTBP#3, H_DSTBN#3 — H_D#[63:48], H_DINV#[3] H_DSTBP#2, H_DSTBN#2 — H_D#[47:32], H_DINV#[2] H_DSTBP#1, H_DSTBN#1 — H_D#[31:16], H_DINV#[1] H_DSTBP#0, H_DSTBN#9 — H_D#[15:0], H_DINV#[0]
H_HIT#	I/O AGTL+	**Host Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with H_HITM# by the target to extend the snoop window.
H_HITM#	I/O AGTL+	**Host Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with H_HIT# to extend the snoop window.
H_LOCK#	I AGTL+	**Host Lock:** All processor bus cycles sampled with the assertion of H_LOCK# and H_ADS#, until the negation of H_LOCK# must be atomic.
H_RCOMP	I/O A	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
H_REQ#[4:0]	I/O AGTL+ 2X	**Host Request Command:** Defines the attributes of the request. H_REQ#[4:0] are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
H_RS#[2:0]	O AGTL+	**Host Response Status:** Indicates the type of response according to the following the table: H_RS#[2:0] — Response type 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by (G)MCH) 100 — Hard Failure (not driven by (G)MCH) 101 — No data response 110 — Implicit Write back 111 — Normal data response
H_SCOMP H_SCOMP#	I/O A	**Host SCOMP:** Slew Rate Compensation for the Host Interface.

Signal Name	Type	Description
H_SWING	I A	**Host Voltage Swing:** These signals provide reference voltages used by the H_RCOMP circuits.
H_TRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
THERMTRIP#	O AGTL+	**Connects between the Processor and the Intel ICH8M:** Assertion of THERMTRIP# (Thermal Trip) indicates the (G)MCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the (G)MCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the (G)MCH core junction temperature. To protect (G)MCH, its core voltage (Vcc) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the (G)MCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.

2.2 DDR2 Memory Interface

2.2.1 DDR2 Memory Channel A Interface

Signal Name	Type	Description
SA_BS[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank.
SA_CAS#	O SSTL-1.8	**CAS Control Signal:** Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SDRAM commands.
SA_DM[7:0]	O SSTL-1.8 2x	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane.
SA_DQ[63:0]	I/O SSTL-1.8 2x	**Data Bus:** DDR2 Channel A data signal interface to the SDRAM data bus.
SA_DQS#[7:0]	I/O SSTL-1.8 2x	**Data Strobe Complements:** These are the complementary strobe signals.

Signal Name	Type	Description
SA_DQS[7:0]	I/O SSTL-1.8 2x	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS[7:0]# during read and write transactions.
SA_MA[14:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SA_RAS#	O SSTL-1.8	**RAS Control Signal:** Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SDRAM commands.
SA_RCVEN#	I SSTL-1.8	**Clock Input:** Used to emulate source-synch clocking for reads. Leave as No Connect.
SA_WE#	O SSTL-1.8	**Write Enable Control Signal:** Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM commands.

2.2.2 DDR2 Memory Channel B Interface

Signal Name	Type	Description
SB_BS[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank.
SB_CAS#	O SSTL-1.8	**CAS Control signal:** Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SDRAM commands.
SB_DM[7:0]	O SSTL-1.8 2x	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane.
SB_DQ[63:0]	I/O SSTL-1.8 2x	**Data Bus:** DDR2 Channel B data signal interface to the SDRAM data bus.
SB_DQS#[7:0]	I/O SSTL-1.8 2x	**Data Strobe Complements:** These are the complementary strobe signals.
SB_DQS[7:0]	I/O SSTL-1.8 2x	**Data Strobes:** SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS[7:0]# during read and write transactions.

Signal Name	Type	Description
SB_MA[14:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SB_RAS#	O SSTL-1.8	**RAS Control Signal:** Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SDRAM commands.
SB_RCVEN#	I SSTL-1.8	**Clock Input:** Used to emulate source-synch clocking for reads. Leave as No Connect.
SB_WE#	O SSTL-1.8	**Write Enable Control Signal:** Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM commands.

2.2.3 DDR2 Memory Common Signals

Signal Name	Type	Description
SM_CK#[1:0] SM_CK#[4:3]	O SSTL-1.8	**SDRAM Inverted Differential Clock:** (2 per SO-DIMM) These are the SDRAM Inverted Differential Clock signals.
SM_CK[1:0] SM_CK[4:3]	O SSTL-1.8	**SDRAM Differential Clock:** (2 per SO-DIMM) These are the SDRAM Differential Clock signals The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM.
SM_CKE[1:0] SM_CKE[4:3]	O SSTL-1.8	**Clock Enable:** (1 per Rank): SM_CKE[4:3] and SM_CKE[1:0] is used: • to initialize the SDRAMs during power-up, • to power-down SDRAM ranks, • to place all SDRAM ranks into and out of self-refresh during STR.
SM_CS#[3:0]	O SSTL-1.8	**Chip Select:** (1 per Rank): These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
SM_ODT[3:0]	O SSTL-1.8	**On Die Termination:** Active Termination Control.

2.2.4 DDR2 Memory Reference and Compensation

Signal Name	Type	Description
SM_RCOMP	I A	**System Memory Impedance Compensation:** Requires pull-up resistor.
SM_RCOMP#	I A	**System Memory Impedance Compensation:** Requires pull-down resistor.
SM_RCOMP_VOH	I A	Swing voltage for pull-up impedance compensation.
SM_RCOMP_VOL	I A	Swing voltage for pull-down impedance compensation.
SM_VREF	I A	**System Memory Reference Voltage** for all data and data strobe signals (two signals).

2.3 PCI Express Based Graphics Interface Signals

Unless otherwise specified, these signals are AC coupled.

Signal Name	Type	Description
PEG_COMPI	I A	PCI Express* Graphics Input Current Compensation.
PEG_COMPO	I A	PCI Express Graphics Output Current and Resistance Compensation.
PEG_RX[15:0] PEG_RX#[15:0]	I PCI Express	PCI Express Graphics Receive Differential Pair.
PEG_TX[15:0] PEG_TX#[15:0]	O PCI Express	PCI Express Graphics Transmit Differential Pair.

2.3.1 Serial DVO and PCI Express*-Based Graphics Signal Mapping

SDVO and PCI Express interface for graphics architecture are muxed together. Table 1 shows the signal mapping.

Table 1. SDVO and PCI Express Based Graphics Port Signal Mapping (Sheet 1 of 2)

SDVO Mode	PCI Express Mode
SDVOB_RED	PEG_TXP0
SDVOB_RED#	PEG_TXN0
SDVOB_GREEN	PEG_TXP1
SDVOB_GREEN#	PEG_TXN1
SDVOB_BLUE	PEG_TXP2
SDVOB_BLUE#	PEG_TXN2
SDVOB_CLK	PEG_TXP3

Table 1. SDVO and PCI Express Based Graphics Port Signal Mapping (Sheet 2 of 2)

SDVO Mode	PCI Express Mode
SDVOB_CLK#	PEG_TXN3
SDVOC_RED	PEG_TXP4
SDVOC_RED#	PEG_TXN4
SDVOC_GREEN	PEG_TXP5
SDVOC_GREEN#	PEG_TXN5
SDVOC_BLUE	PEG_TXP6
SDVOC_BLUE#	PEG_TXN6
SDVOC_CLK	PEG_TXP7
SDVOC_CLK#	PEG_TXN7
SDVO_TV_CLKIN	PEG_RXP0
SDVO_TV_CLKIN#	PEG_RXN0
SDVO_INT	PEG_RXP1
SDVO_INT#	PEG_RXN1
SDVO_FLD_STALL	PEG_RXP2
SDVO_FLD_STALL#	PEG_RXN2

2.4 DMI – (G)MCH to ICH Serial Interface

Signal Name	Type	Description
DMI_RXN[3:0] DMI_RXP[3:0]	I PCI Express	**DMI input from ICH:** Direct Media Interface receive differential pair.
DMI_TXN[3:0] DMI_TXP[3:0]	O PCI Express	**DMI output to ICH:** Direct Media Interface transmit differential pair.

2.5 Integrated Graphics Interface Signals

2.5.1 CRT DAC Signals

Signal Name	Type	Description
CRT_BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_BLUE#	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
CRT_GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_GREEN#	O A	**GREEN# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
CRT_HSYNC	O HVCMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”.
CRT_RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_RED#	O A	**RED# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
CRT_TVO_IREF	O A	**Resistor Set and TV Reference Current:** Set point resistor for the internal color palette DAC and TV reference current. A 1.3 kΩ ±0.5% resistor is required between CRT_TVO_IREF and motherboard ground.
CRT_VSYNC	O HVCMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable).

2.5.2 Analog TV-out Signals

Signal Name	Type	Description
TV_DCONSEL[1:0]	O HVCMOS	**TV D-connector Select:** Selects appropriate full-voltage discernment signals for TV-out D-connector.
TVA_DAC	O A	**TVDAC Channel A Output:** Can map to any one of the following: • Composite Video, Blank, and Sync (CVBS) • Component Pb
TVA_RTN	O A	**Current Return for TV DAC Channel A:** Connect to ground on board.
TVB_DAC	O A	**TVDAC Channel B Output:** Can map to any one of the following: Svideo - Y Component Y
TVB_RTN	O A	**Current Return for TV DAC Channel B:** Connect to ground on board.
TVC_DAC	O A	**TVDAC Channel C Output:** Can map to any one of the following: Svideo - C Component Pr
TVC_RTN	O A	**Current Return for TV DAC Channel C:** Connect to ground on board.

2.5.3 LVDS Signals

Signal Name	Type	Description
LDVS Channel A		
LVDSA_CLK	O LVDS	**LVDS Channel A differential clock output – positive**
LVDSA_CLK#	O LVDS	**LVDS Channel A differential clock output – negative**
LVDSA_DATA#[3:0]	O LVDS	**LVDS Channel A differential data output – negative**
LVDSA_DATA[3:0]	O LVDS	**LVDS Channel A differential data output – positive**
LDVS Channel B		
LVDSB_CLK	O LVDS	**LVDS Channel B differential clock output – positive**
LVDSB_CLK#	O LVDS	**LVDS Channel B differential clock output – negative**
LVDSB_DATA#[3:0]	O LVDS	**LVDS Channel B differential data output – negative**
LVDSB_DATA[3:0]	O LVDS	**LVDS Channel B differential data output – positive**
Lfp Panel Power and Backlight Control		
L_BKLT_CTRL	O HVCMOS	**Panel backlight brightness control** Panel brightness control.
L_BKLT_EN	O HVCMOS	**LVDS backlight enable** Panel backlight enable control.
L_VDD_EN	O HVCMOS	**LVDS panel power enable** Panel power control enable control.
LVDS Reference Signals		
LVDS_IBG	I/O Ref	**LVDS Reference Current**. A pull down resistor of 2.4 kΩ ±1% is needed
LVDS_VBG	O A	**Reserved** No connect
LVDS_VREFH	I Ref	**Reserved** Can be connected to GND or left as No Connect.
LVDS_VREFL	I Ref	**Reserved** Can be connected to GND or left as No Connect.

2.5.4 Serial DVO Interface

All of the pins in this section are multiplexed with the upper eight lanes of the PCI Express interface.

Signal Name	Type	Description
SDVO B Interface		
SDVOB_BLUE	O PCI Express	**Serial Digital Video B Blue Data:** Multiplexed with PEG_TXP2
SDVOB_BLUE#	O PCI Express	**Serial Digital Video B Blue Data Complement:** Multiplexed with PEG_TXN2
SDVOB_GREEN	O PCI Express	**Serial Digital Video B Green Data:** Multiplexed with PEG_TXP1
SDVOB_GREEN#	O PCI Express	**Serial Digital Video B Green Data Complement:** Multiplexed with PEG_TXN1
SDVOB_RED	O PCI Express	**Serial Digital Video B Red Data:** Multiplexed with PEG_TXP0
SDVOB_RED#	O PCI Express	**Serial Digital Video B Red Data Complement:** Multiplexed with PEG_TXN0
SDVOB_CLK	O PCI Express	**Serial Digital Video B Clock:** Multiplexed with PEG_TXP3
SDVOB_CLK#	O PCI Express	**Serial Digital Video B Clock Complement:** Multiplexed with PEG_TXN3
SDVO C Interface		
SDVOC_BLUE	O PCI Express	**Serial Digital Video Channel C Blue:** Multiplexed with PEG_TXP6
SDVOC_BLUE#	O PCI Express	**Serial Digital Video C Blue Complement:** Multiplexed with PEG_TXN6
SDVOC_GREEN	O PCI Express	**Serial Digital Video C Green:** Multiplexed with PEG_TXP5
SDVOC_GREEN#	O PCI Express	**Serial Digital Video C Green Complement:** Multiplexed with PEG_TXN5
SDVOC_RED	O PCI Express	**Serial Digital Video C Red Data:** Multiplexed with PEG_TXP4
SDVOC_RED#	O PCI Express	**Serial Digital Video C Red Complement:** Multiplexed with PEG_TXN4
SDVOC_CLK	O PCI Express	**Serial Digital Video C Clock:** Multiplexed with PEG_TXP7
SDVOC_CLK#	O PCI Express	**Serial Digital Video C Clock Complement:** Multiplexed with PEG_TXN7

Signal Name	Type	Description
SDVO Common Signals		
SDVO_FLDSTALL	I PCI Express	**Serial Digital Video Field Stall:** Multiplexed with PEG_RXP2
SDVO_FLDSTALL#	I PCI Express	**Serial Digital Video Field Stall Complement:** Multiplexed with PEG_RXN2
SDVO_INT	I PCI Express	**Serial Digital Video Input Interrupt:** Multiplexed with PEG_RXP1
SDVO_INT#	I PCI Express	**Serial Digital Video Input Interrupt Complement:** Multiplexed with PEG_RXN1
SDVO_TV_CLKIN	I PCI Express	**Serial Digital Video TVOUT Synchronization Clock:** Multiplexed with PEG_RXP0
SDVO_TV_CLKIN#	I PCI Express	**Serial Digital Video TVOUT Synchronization Clock Complement:** Multiplexed with PEG_RXN0

2.5.5 Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
CRT_DDC_CLK	I/O COD	CRT DDC clock monitor control support
CRT_DDC_DATA	I/O COD	CRT DDC Data monitor control support
L_CTRL_CLK	I/O COD	Control signal (clock) for External SSC clock chip control – optional
L_CTRL_DATA	I/O COD	Control signal (data) for External SSC clock chip control – optional
L_DDC_CLK	I/O COD	EDID support for flat panel display
L_DDC_DATA	I/O COD	EDID support for flat panel display
SDVO_CTRL_CLK	I/O COD	Control signal (clock) for SDVO device
SDVO_CTRL_DATA	I/O COD	Control signal (data) for SDVO device

2.6 Intel® Management Engine Interface Signals

These signals are the Intel® Management Engine Interface between the (G)MCH and the ICH.

Signal Name	Type	Description
CL_CLK	Supply Independent CMOS	Controller Link Bi Directional Clock
CL_DATA	Supply Independent CMOS	Controller Link Bi Directional Data
CL_PWROK	I HVCMOS	Controller Link Power OK
CL_RST#	I CMOS	Controller Link reset
CL_VREF	I A	External reference voltage for Controller Link input buffers

2.7 PLL Signals

Signal Name	Type	Description
DPLL_REF_CLK	I Diff Clk	**Display PLLA Differential Clock In:** 96-MHz Display PLL Differential Clock In, no SSC support.
DPLL_REF_CLK#	I Diff Clk	**Display PLLA Differential Clock In Complement:** Display PLL Differential Clock In Complement - no SSC support.
DPLL_REF_SSCLK	I Diff Clk	**Display PLLB Differential Clock In:** 100-MHz Optional Display PLL Differential Clock In for SSC support – **NOTE:** Differential Clock input for optional SSC support for LVDS display.
DPLL_REF_SSCLK#	I Diff Clk	**Display PLLB Differential Clock In Complement:** Optional Display PLL Differential Clock In Complement for SSC support. **NOTE:** Differential Clock input for optional SSC support for LVDS display.
HPLL_CLK	I Diff Clk	**Differential Host Clock In:** Differential clock input for the Host PLL. Used for phase cancellation for FSB transactions. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Also used to generate core and system memory internal clocks. This is a low voltage differential signal and runs at ¼ the FSB data rate.

Signal Name	Type	Description
HPLL_CLK#	I Diff Clk	**Differential Host Clock Input Complement**
PEG_CLK	I Diff Clk	**Differential PCI Express Based Graphics/DMI Clock In:** These pins receive a differential 100-MHZ Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
PEG_CLK#	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In complement**

2.8 Reset and Miscellaneous Signals

Signal Name	Type	Description
CLKREQ#	O COD	**External Clock Request:** (G)MCH drives CLK_REQ# to control the PCI Express* differential clock input to itself.
GFX_VID[3:0]	O A	Reserved
GFX_VR_EN	O A	Reserved
ICH_SYNC#	O HVCMOS	**ICH Synchronization:** Asserted to synchronize with ICH on faults. ICH_SYNC# must be connected to ICH8M's MCH_SYNC# signal.
PMSYNC# (PM_BM_BUSY#)	I HVCMOS	**(G)MCH Power Management Sync:** PMSYNC# is used to indicate some Cx state transition information between ICH and (G)MCH.
DPRSLPVR	I/O HVCMOS	**Deeper Sleep - Voltage Regulator:** Deeper Sleep Voltage signal from ICH8M.
PM_DPRSTP#	I LVCMOS	**Deeper Sleep State:** Deeper Sleep State signal coming from ICH8M.
PM_EXT_TS#[1:0]	I HVCMOS	**External Thermal Sensor Input:** If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling.
PWROK	I HVCMOS	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that (G)MCH clocks have been stable for at least 1 us, and that (G)MCH power supplies have been stable for at least 1 ms. When asserted this signal also ensures that signals coming out of the (G)MCH are stable. This input buffer is 3.3-V tolerant.

Signal Name	Type	Description
RSTIN#	I HVCMOS	**Reset In:** When asserted this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the ICH8M. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3-V tolerant.
TEST1	I HVCMOS	**Test 1:** This signal should be tied to ground.
TEST2	I HVCMOS	**Test 2:** This signal should be tied to ground.
NC	NC	**No Connects:** This signals should be left as no connects.

2.9 Non-Critical to Function (NCTF)

Adding non-critical to function (NCTF) solder balls to Intel chipset packages can improve the overall package-to-board solder joint strength and reliability. Ball locations/signal IDs followed with the suffix of NCTF have been designed into the package footprint.

Note: In some cases, where board stresses are excessive, these balls may crack partially or completely. However, cracks in the NCTF balls will have no impact to Intel product performance or reliability.

2.10 Power and Ground

Voltage	Ball Name	Description
Host		
1.05	VTT	Host Interface I/O Voltage
1.05	VTTLF	These balls are internally connected to power and require a decoupling capacitor.
System Memory		
1.8	VCC_SM	I/O Voltage
1.8	VCC_SM_LF	These balls are internally connected to power and require a decoupling capacitor.
1.8	VCC_SM_CK	Clock I/O Voltage
1.25	VCCA_SM	I/O Logic and DLL voltage
1.25	VCCA_SM_CK	Clock logic voltage

Voltage	Ball Name	Description
PCI Express* Based Graphics / DMI		
1.05	VCC_PEG	Analog, I/O Logic, and Term Voltage for PCI Express* Based Graphics
3.3	VCCA_PEG_BG	Band Gap Voltage for PCI Express Based Graphics
Ground	VSSA_PEG_BG	Band Gap Ground for PCI Express Based Graphics
1.25	VCCA_PEG_PLL	Analog PLL Voltage for PCI Express Based Graphics
1.25	VCCD_PEG_PLL	Digital PLL Voltage for PCI Express Based Graphics
1.25	VCC_DMI	TX Analog and Term Voltage for DMI
1.05	VCC_RXR_DMI	Rx and I/O Logic for DMI
PLL		
1.25	VCCA_HPLL	Host PLL Analog Supply
1.25	VCCD_HPLL	Host PLL Digital Supply
1.25	VCCA_MPLL	MPLL Analog circuits
1.25	VCCA_DPLLA	Display A PLL power supply
1.25	VCCA_DPLLB	Display B PLL power supply
High Voltage		
3.3	VCC_HV	HV buffer power supply
CRT		
3.3	VCC_SYNC	HSYNC/VSYNC power supply
3.3	VCCA_CRT_DAC	Analog power supply
1.5	VCCD_QDAC	Quiet digital power supply (same as VCCD_QDAC for TV)
1.5	VCCD_CRT	Level shifter voltage
LVDS		
1.8	VCCD_LVDS	Digital power supply
1.8	VCC_TX_LVDS	I/O power supply
1.8	VCCA_LVDS	Analog power supply
Ground	VSSA_LVDS	Analog ground
TV		
1.5	VCCD_TVDAC	TV DAC power supply
3.3	VCCA_TVA_DAC	TV Out Channel A power supply
3.3	VCCA_TVB_DAC	TV Out Channel Bpower supply
3.3	VCCA_TVC_DAC	TV Out Channel Cpower supply
1.5	VCCD_QDAC	Quiet Digital TV DAC Power Supply (same as VCCDQ_DAC for CRT)
3.3	VCCA_DAC_BG	TV DAC Band Gap power (3.3 V)
Ground	VSSA_DAC_BG	TV DAC Band Gap ground

Voltage	Ball Name	Description
Intel® Management Engine Interface		
1.05	VCC_AXM	Controller Link / Intel® Management Engine Interface voltage supply
Graphics Core		
1.05	VCC	Core chipset voltage supply
1.05	VCC_AXG	Graphics voltage supply
1.25	VCC_AXD	Memory voltage supply
1.25	VCC_AXF	I/O voltage supply
Ground	VSS	Ground
NC	VSS_SCB	Sacrificial Corner Balls for improved package reliability. These signals are connected to GND on the chipset package, and can be connected to GND or left as NC on the platform (can be left as test points). **NOTE**: There is no functional impact if these signals are grounded.

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3 Host Interface

3.1 FSB Source Synchronous Transfers

The chipset supports the Intel Core 2 Duo processor subset of the Enhanced Mode Scalable bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals.

The address signals are double pumped and a new address can be generated every other bus clock. At bus clock speeds of 133-MHz, 166-MHz and 200-MHz, address signals run at 266 MT/s, 333 MT/s and 400 MT/s, which amounts to a maximum address queue rate of 64, 83 and 100 Mega-addresses/seconds, respectively.

Data signals are quad pumped and an entire 64-B cache line can be transferred in two bus clocks. At 133-MHz, 166-MHz and 200-MHz bus clock, data signals run at 533-MHz, 667-MT/s and 800-MT/s for a maximum bandwidth of 4.3-GB/s, 5.3-GB/s and 6.4-GB/ seconds, respectively.

3.2 FSB IOQ Depth

The scalable bus supports up to 12 simultaneous outstanding transactions. The chipset has a 12-deep IOQ.

3.3 FSB OOQ Depth

The (G)MCH supports only one outstanding deferred transaction on the FSB.

3.4 FSB AGTL+ Termination

The (G)MCH integrates AGTL+ termination resistors on die.

3.5 FSB Dynamic Bus Inversion

The (G)MCH supports dynamic bus inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. H_DINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

H_DINV#[3:0]	Data Bits
H_DINV#0	H_D#[15:0]
H_DINV#1	H_D#[31:16]
H_DINV#2	H_D#[47:32]
H_DINV#3	H_D#[63:48]

Whenever the processor or the (G)MCH drives data, each 16-bit segment is analyzed. If there are more than eight (out of sixteen) signals driven low on the H_D# bus, a corresponding H_DINV# signal is asserted. As a result, the data is inverted prior to

being driven on the bus. Whenever the processor or the (G)MCH receives data, it monitors H_DINV#[3:0] to determine if the corresponding data segment should be inverted.

3.6 FSB Interrupt Overview

The processor supports FSB interrupt delivery. It does **not** support the APIC serial bus interrupt delivery mechanism. Interrupt-related messages are encoded on the FSB as Interrupt Message Transactions. FSB interrupts may originate from the CPU(s) on the FSB, or from a downstream device on the DMI or PCI Express Graphics Attach. In the latter case, the (G)MCH drives the Interrupt Message Transaction on the FSB.

In the IOxAPIC environment, an interrupt is generated from the IOxAPIC to a processor in the form of an upstream memory write. The ICH contains IOxAPICs, and its interrupts are generated as upstream DMI Memory Writes. Furthermore, the PCI Specification and PCI Express Specification define Message Signaled Interrupts (MSIs) that are also in the form of Memory Writes. A PCI device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC. The IOxAPIC in turn generates an interrupt as an upstream DMI Memory Write. Alternatively, the MSI may directly route to the FSB. The target of an MSI is dependent on the address of the interrupt Memory Write. The (G)MCH forwards upstream DMI and PCI Express Graphics Attach low priority Memory Writes to address 0FEEx_xxxxh to the FSB as Interrupt Message Transactions.

The (G)MCH also broadcasts EOI cycles generated by a processor downstream to the PCI Express Port and DMI interfaces.

3.7 APIC Cluster Mode Support

APIC Cluster mode support is required for backward compatibility with existing software, including various operating systems. For example, beginning with Microsoft Windows* 2000 operating system, there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

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4 System Address Map

This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

The chipset supports up to 64 GB of addressable memory space and 64 kB + 3 B of addressable I/O space. There is a programmable memory address space under the 1-MB region, which is divided into regions that can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only.

The (G)MCH does not support:

- PCI dual address cycle (DAC) mechanism
- PCI Express 64-bit prefetchable memory transactions
- Any other addressing mechanism that allows addressing of greater than 4 GB on either the DMI or PCI Express interface.
- The (G)MCH does not limit DRAM space in hardware. There is no hardware lock to stop someone from inserting more memory than is addressable.

It is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges, which may be mapped to PCI Express, DMI, or to the Integrated Graphics Device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the IGD respectively. The (G)MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

- Device 0
  - EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time-based weighted round-robin arbitration (4-kB window).
  - MCHBAR – Memory mapped range for internal (G)MCH registers.
  - PCIEXBAR – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification (64-MB, 128-MB, or 256-MB window).
  - DMIBAR –This window is used to access registers associated in the MCH/ICH (DMI) register memory range (4-kB window).
  - GGC – (G)MCH graphics control register. Used to select the amount of main memory that is pre-allocated to support the IGD in VGA (non-linear) and Native (linear) modes (0 to 64-MB options).
- Device 1, Function 0:
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window. (PMUBASE/PMULIMIT) - are applicable for 36-bit SKUs.
  - IOBASE1/IOLIMIT1 – PCI Express port IO access window.

- Device 2, Function 0:
  - GTTMMADR - IGD registers integrated graphics translation table location and integrated graphics instruction port (1-MB window).
  - IOBAR – I/O access window for integrated graphics. Through this window address/data register pair, using I/O semantics, the IGD and integrated graphics instruction port registers can be accessed. Note this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTMMADR table.
  - GMADR – Integrated graphics translation window (256-MB window).
- Device 2, Function 1:
  - MMADR – Function 1 IGD registers and integrated graphics instruction port (512-kB window).
- Device 3, Function 0:
  - MEI_MMIBAR - Function 0 Intel® Management Engine Interface (MEI) memory mapped registers (16-B window).
- Device 3, Function 1:
  - MEI2_MMBAR - Function 0 Intel® MEI memory mapped registers (16-B window).
- Device 3, Function 2:
  - PCMDBA- Function 2 I/O space used in Native Mode for the Primary Controller's Command Block (8-B window).
  - PCTLBA - Function 2 I/O space used in Native Mode for the Primary Controller's Control Block (4-B window).
  - SCMDBA - Function 2 /O space used in Native Mode for the Secondary Controller's Command Block (8-B window).
  - SCTLBA - Function 2 I/O space used in Native Mode for the Secondary Controller's Control Block (4-B window).
  - LBAR - Function 2 I/O space for the SFF-8038i mode of operation (aka Bus Master IDE) (16-B window).
- Device 3, Function 3:
  - KTIBA - Function 3 Keyboard and Text IO Block (8-B window).
  - KTMBA - Function 3 Keyboard and Text Memory Block (8-B window).

The rules for the above programmable ranges are:

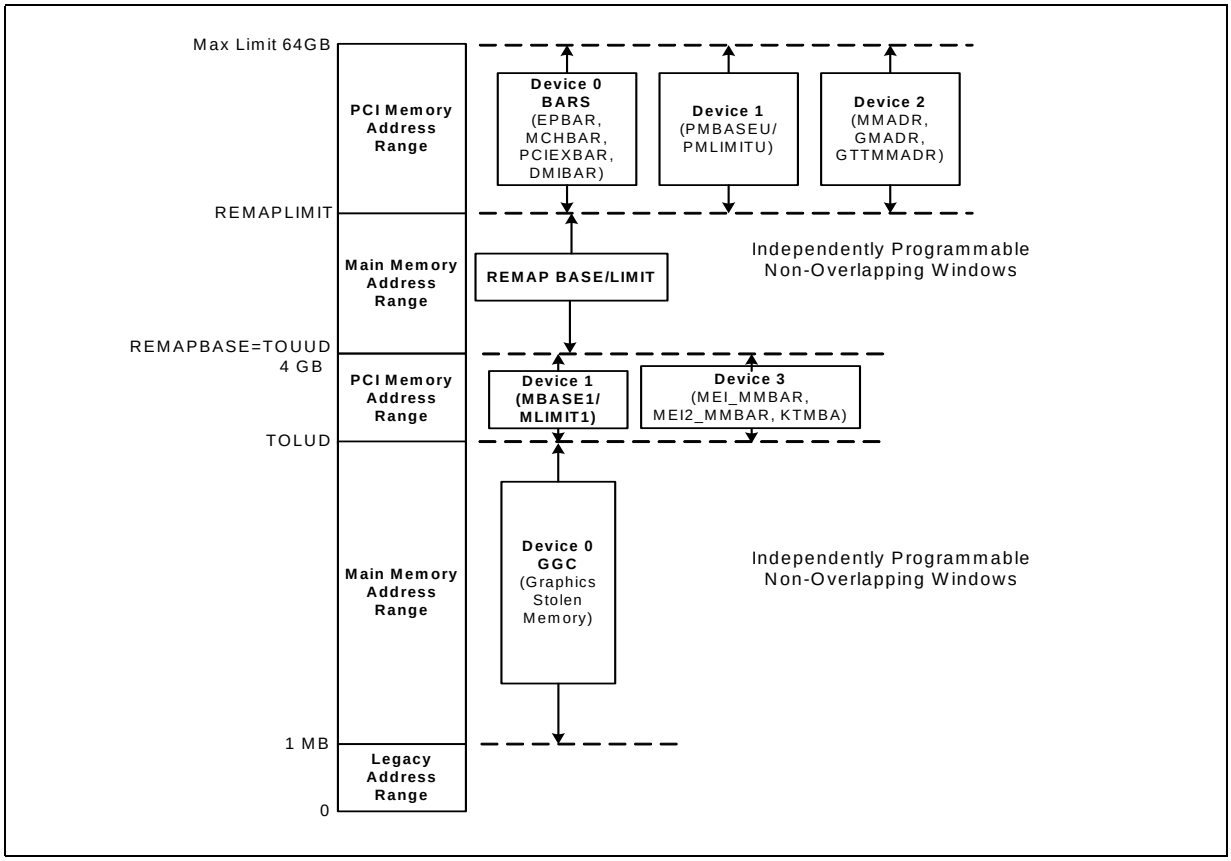
1. ALL of these ranges MUST be unique and NON-OVERLAPPING.

Note: It is the BIOS or system designers responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.

2. In the case of overlapping ranges with memory, the memory decode is given priority.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA range writes. Note that peer to peer cycles to the integrated graphics VGA range are not supported.

Figure 2 represents system memory address map in a simplified form.

Figure 2. System Address Ranges



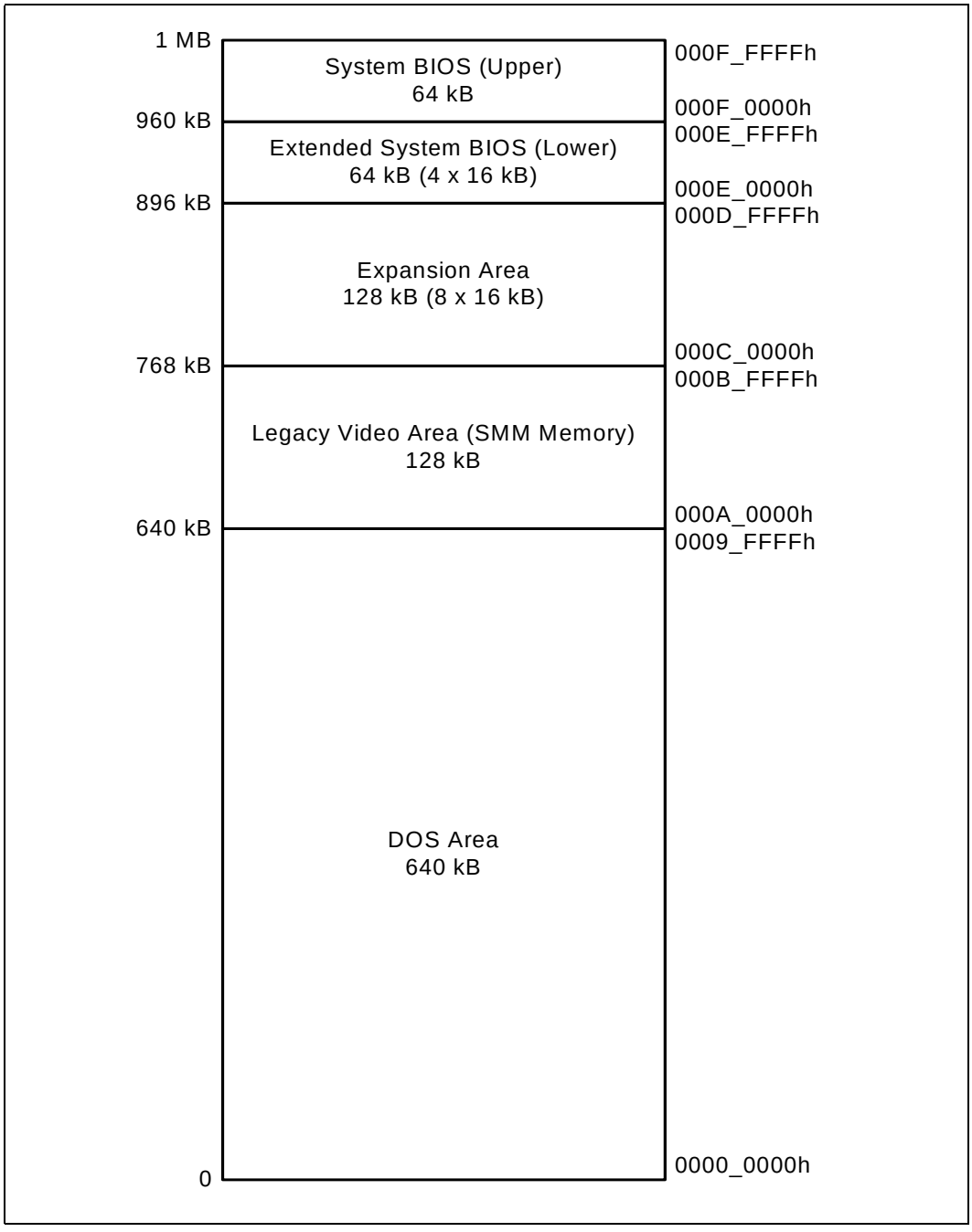
NOTE: BARs mapped to the REMAPLIMIT-64 GB space can also be mapped to the TOLUD 4-GB space. (G)MCH variants not supporting 36-bit addressing will require these BARs to be mapped to the TOLUD 4-GB space.

4.1 Legacy Address Range

This area is divided into the following address regions:

- 0 to 640-kB – MS-DOS* area
- 640 to 768-kB – Legacy Video Buffer area
- 768 to 896 kB in 16-kB sections (total of eight sections) – Expansion area
- 896 to 960 kB in 16-kB sections (total of four sections) – Extended System BIOS area
- 960-kB to 1-MB Memory – System BIOS area

Figure 3. DOS Legacy Address Range



4.1.1 DOS Range (0000_0000h – 0009_FFFFh)

The DOS area is 640 kB (0000_0000h to 0009_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

4.1.2 Legacy Video Area (000A_0000h to 000B_FFFFh)

The legacy 128-kB VGA memory range, frame buffer, (000A_0000h to 000B_FFFFh) can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the (G)MCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA Enable and MDAP). This region is also the default for SMM space.

4.1.2.1 Compatible SMRAM Address Range (000A_0000h to 000B_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A 0000h to 000B FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

4.1.2.2 Monochrome Adapter (MDA) Range (000B_0000h to 000B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the (G)MCH must decode cycles in the MDA range (000B_0000h to 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

4.1.3 Expansion Area (000C_0000h to 000D_FFFFh)

This 128-kB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16-kB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through (G)MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 2. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
000C_0000h to 000C_3FFFh	W/R	Add-on BIOS
000C_4000h to 000C_7FFFh	W/R	Add-on BIOS
000C_8000h to 000C_BFFFh	W/R	Add-on BIOS
000C_C000h to 000C_FFFFh	W/R	Add-on BIOS
000D_0000h to 000D_3FFFh	W/R	Add-on BIOS
000D_4000h to 000D_7FFFh	W/R	Add-on BIOS
000D_8000h to 000D_BFFFh	W/R	Add-on BIOS
000D_C000h to 000D_FFFFh	W/R	Add-on BIOS

4.1.4 Extended System BIOS Area (000E_0000h to 000E_FFFFh)

This 64-kB area (000E_0000h to 000E_FFFFh) is divided into four, 16-kB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
000E_0000h to 000E_3FFFh	W/R	BIOS Extension
000E_4000h to 000E_7FFFh	W/R	BIOS Extension
000E_8000h to 000E_BFFFh	W/R	BIOS Extension
000E_C000h to 000E_FFFFh	W/R	BIOS Extension

4.1.5 System BIOS Area (000F_0000h to 000F_FFFFh)

This area is a single 64-kB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI. By manipulating the Read/Write attributes, the (G)MCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 4. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
000F_0000h to 000F_FFFFh	WE RE	BIOS Area

4.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 kB to 1 MB comprise what is also known as the PAM Memory Area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there normally will not be IWB cycles targeting DMI.

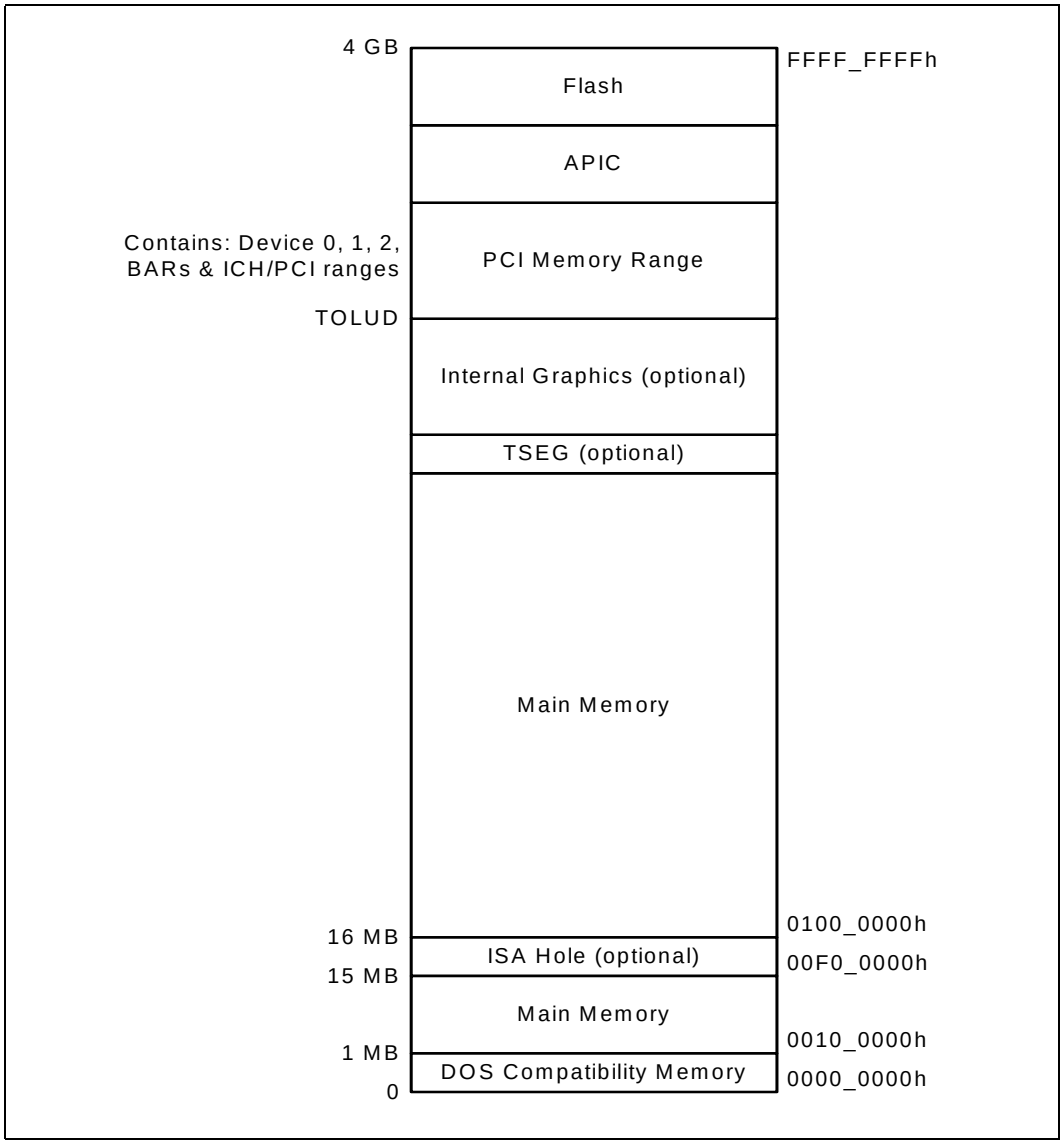
However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RD it is possible to get IWB cycles targeting DMI. This may occur for DMI-originated cycles to disabled PAM regions.

For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled” the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

4.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the (G)MCH (as programmed in the TOLUD register). All accesses to addresses within this range are forwarded by the (G)MCH to the DRAM unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

Figure 4. Main Memory Address Range (0 to 4 GB)



4.2.1 ISA Hole (15 MB to 16 MB)

A hole can be created at 15 MB to 16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15-MB to 16-MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used for validation by customer teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-MB to 16-MB window.

4.2.2 Top Segment (TSEG)

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. System management software may partition this region of memory so it is accessible only by system management software. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, DMI, and integrated graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses (see Table 6). Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

4.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. Table 5 details the location and attributes of the regions. How to enable and disable these ranges are described in the (G)MCH Control Register Device 0 (GGC).

Table 5. Pre-allocated Memory Example for 512-MB DRAM, 64-MB VGA, and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h to 1BEF_FFFFh	R/W	Available System Memory 447 MB
1BF0_0000h to 1BFF_FFFFh	SMM Mode Only - Processor Reads	TSEG Address Range & Pre-allocated Memory
1C00_0000h t 1FFF_FFFFh	R/W	Pre-allocated Graphics VGA memory 64 MB when IGD is enabled

4.3 PCI Memory Address Range (TOLUD to 4 GB)

This address range, from the top of physical memory to 4 GB (top of addressable memory space supported by the (G)MCH) is normally mapped to the DMI Interface.

Exceptions to this mapping include the BAR memory mapped regions, which include: EPBAR, MCHBAR, and DMIBAR.

In the PCI Express port, there are two exceptions to this rule:

- Addresses decoded to the PCI Express memory window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express.
- Addresses decoded to PCI Express configuration space are mapped based on Bus, Device, and Function number. (PCIEXBAR range).

Note: AGP Aperture no longer exists with PCI Express.

In an integrated graphics configuration, there are three exceptions to this rule:

1. Addresses decoded to the Graphics Memory Range (GMADR range).
2. Addresses decoded to the Graphics Translation Table range (GTTADR range).
3. Addresses decoded to the Memory Mapped Range of the Integrated Graphics Device (MMADR range). There is a MMADR range for Device 2 Function 0 and a MMADR range for Device 2 Function 1. Both ranges are forwarded to the integrated graphics device.

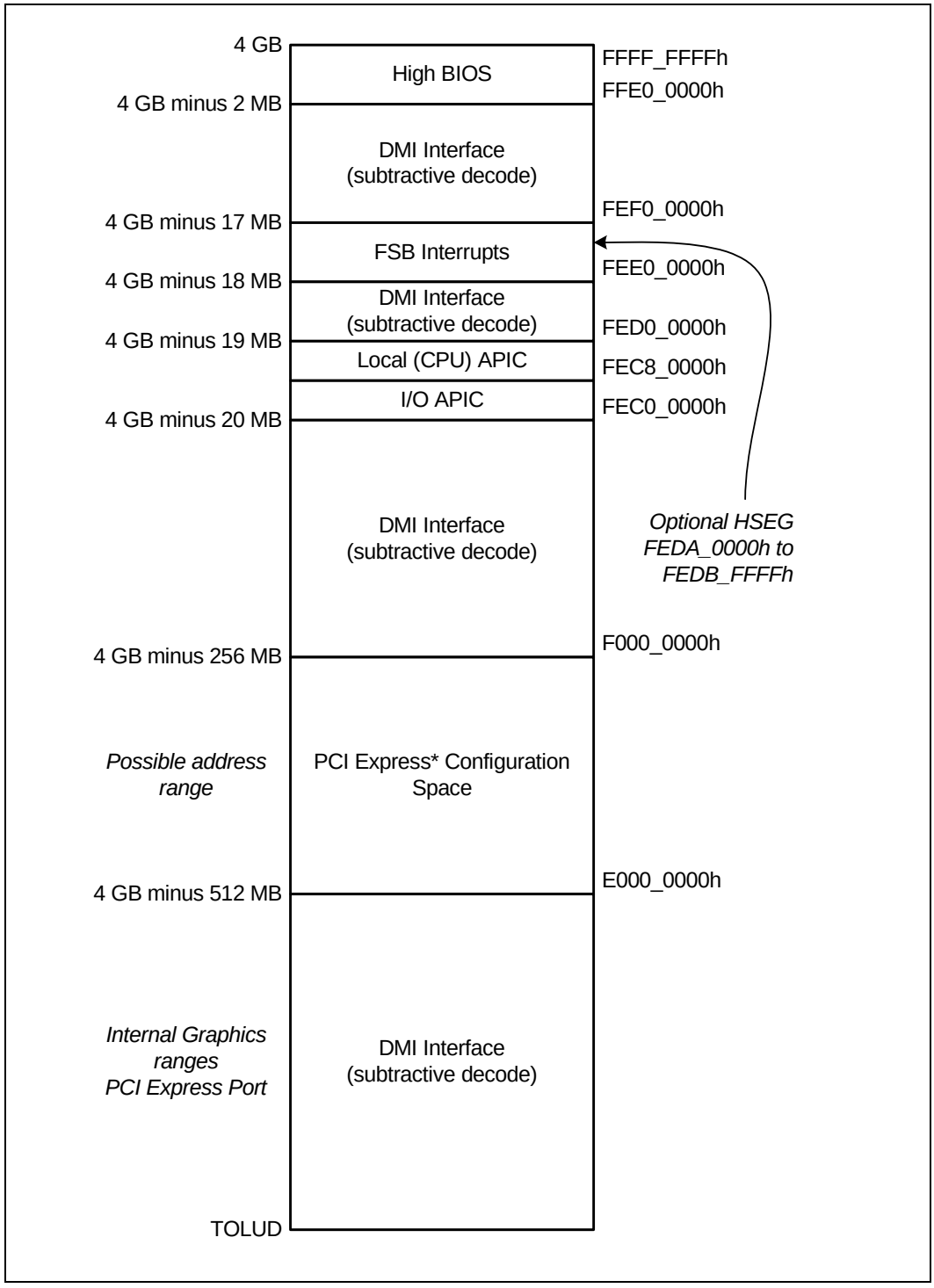
In an Intel Management Engine configuration, there are exceptions to this rule.

1. Addresses decoded to the Intel® Management Engine Intel® MEI MMIO range (MEI_MMIBAR)
2. Addresses decoded to the Intel Management Engine Intel MEI2 MMIO range (MEI2_MMIBAR)
3. Addresses decoded to the Intel Management Engine IDER MMIO range (PCMDBA, PCTLBA, SCMDBA, SCTLBA, LBAR)
4. Addresses decoded to the Intel Management Engine keyboard and Text MMIO range (KTIBA, KTMBA)

The exceptions listed above for integrated graphics and the PCI Express ports **MUST NOT overlap with APIC Configuration Space, FSB Interrupt Space and High BIOS Address Range.**

Note: With the exception of certain BARs, all the above mentioned BARs can be mapped in the TOUUD to 64-GB range in the case of chipset variants supporting 36-bit addressing. See Figure 2 for details.

Figure 5. PCI Memory Address Range



4.3.1 APIC Configuration Space (FEC0_0000h to FECF_FFFFh)

This range is reserved for APIC configuration space that includes the default I/O APIC configuration space from FEC0_0000h to FEC7_0FFFh. The default Local (processor) APIC configuration space goes from FEC8_0000h to FECF_FFFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the processor. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC0_0000h (4 GB minus 20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64 kB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH portion of the chip set or as a stand-alone component(s).

I/O APIC units are located beginning at the default address FEC0_0000h. The first I/O APIC are located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where x is I/O APIC unit number 0 through F (hex). This address range will normally be mapped to DMI.

Note: There is no provision to support an I/O APIC device on PCI Express.

4.3.2 HSEG (FEDA_0000h to FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h to 000B_FFFFh. Non-SMM mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All cache line writes with WB attribute or implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

4.3.3 FSB Interrupt Memory Space (FEE0_0000 to FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express, integrated graphics, or DMI may issue a Memory Write to 0FEEx_xxxxh. The (G)MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting H_TRDY#. This Memory Write cycle does not go to DRAM.

4.3.4 High BIOS Area

The top 2 MB (FFE0_0000h to FFFF_FFFFh) of the PCI Memory Address Range is reserved for system BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to DMI so that the upper subset of this region aliases to the 16-MB minus 256-kB range. The actual address space required for the BIOS is less than 2 MB, but the minimum processor MTRR range for this region is 2 MB, so a full 2 MB must be considered.

4.4 Main Memory Address Space (4 GB to TOUUD)

Earlier chipsets supported a maximum main memory size of 4-GB total memory. This would result in a hole between TOLUD (Top of Low Usable DRAM) and 4 GB when main memory size approached 4 GB, resulting in a certain amount of physical memory being inaccessible to the system.

The new reclaim configuration registers (TOUUD, REMAPBASE, REMAPLIMIT) exist to reclaim lost main memory space. The greater than 32-bit reclaim handling are handled similar to other MCHs.

Upstream read and write accesses above 36-bit addressing will be treated as invalid cycles by PCI Express Graphics and DMI.

The Top of Memory (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO above TOM). TOM is used to allocate the Intel Management Engine stolen memory. The Intel Management Engine stolen size register reflects the total amount of physical memory it has stolen. The Intel Management Engine stolen memory is located at the top of physical memory, and the memory base is calculated by subtracting the amount of memory stolen by the Intel Management Engine from TOM.

The Top of Upper Usable DRAM (TOUUD) register reflects the total amount of addressable memory. If reclaim is disabled, TOUUD will reflect TOM minus Intel Management Engine's stolen size. If reclaim is enabled, then it will reflect the reclaim limit. Also, the reclaim base is the same as TOM minus Intel Management Engine stolen memory size to the nearest 64-MB alignment.

4.4.1 Memory Re-Map Background

The following examples of Memory Mapped I/O devices are typically located below 4 GB:

- High BIOS
- H-Seg
- T-Seg
- Graphics Stolen Memory
- XAPIC
- Local APIC
- FSB Interrupts
- Mbase / Mlimit
- Memory Mapped I/O space that supports only 32-bit addressing

The (G)MCH provides the capability to remap or reclaim the physical memory overlapped by the Memory Mapped I/O logical address space. The (G)MCH re-maps physical memory from the Top of Low Usable DRAM (TOLUD) boundary up to the 4-GB boundary to an equivalent sized logical address range located just below the Intel Management Engine's stolen memory.

4.4.2 Memory Remapping (or Reclaiming)

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the REMAPBASE register. The top of the re-map window is defined by the value in the REMAPLIMIT register. An address that falls within this window is remapped to the physical memory starting at the address defined by the TOLUD register. The TOLUD register must by 64-MB aligned when remapping is enabled, but can be 1-MB aligned when remapping is disabled.

4.5 PCI Express Configuration Address Space

The Device 0 register (PCIEXBAR), defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This is a 256-MB block of addresses below top of addressable memory (currently 4 GB) and is aligned to a 256-MB boundary. BIOS must assign this address range in such a way that it will not conflict with any other address ranges.

4.5.1 PCI Express Graphics Attach

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Prefetchable Memory Base (PMBASE/ PMBASEU) and Prefetchable Memory Limit (PMLIMIT/PMLIMITU) registers.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

$$Memory\_Base\_Address \leq Address \leq Memory\_Limit\_Address$$

$$Prefetchable\_Memory\_Base\_Address \leq Address \leq Prefetchable\_Memory\_Limit\_Address$$

It is essential to support a separate Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the (G)MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the Device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

4.5.2 Graphics Aperture

Unlike AGP, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the (G)MCH has no APBASE and APSIZE registers.

4.6 Graphics Memory Address Ranges

The (G)MCH can be programmed to direct memory accesses to IGD when addresses are within any of three ranges specified via registers in (G)MCH's Device 2 configuration space.

- The Memory Map Base Register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the Top-of-Main-DRAM and below high BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so they do not steal any physical DRAM memory space.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

4.6.1 Graphics Register Ranges

The VGA and Extended VGA registers can be accessed via standard VGA I/O locations as well as via memory-mapped locations. In addition, the memory map contains allocation ranges for various functions. The memory space address listed for each register is an offset from the base memory address programmed into the MMADR register (PCI configuration offset 14h). The same memory space can be accessed via dword accesses to I/OBAR. Through the IOBAR, I/O registers MMIO_index and MMIO_data are written.

VGA and Extended VGA Control Registers (0000_0000h to 0000_0FFFh):

These registers are located in both I/O space and memory space. The VGA and Extended VGA registers contain the following register sets: General Control/Status, Sequencer (SRxx), Graphics Controller (GRxx), Attribute Controller (ARxx), VGA Color Palette, and CRT Controller (CRxx) registers.

Instruction, Memory, and Interrupt Control Registers (0000_1000h to 0000_2FFFh):

The Instruction and Interrupt Control registers are located in space and contain the types of registers listed in the following sections.

4.6.2 I/O Mapped Access to Device 2 MMIO Space

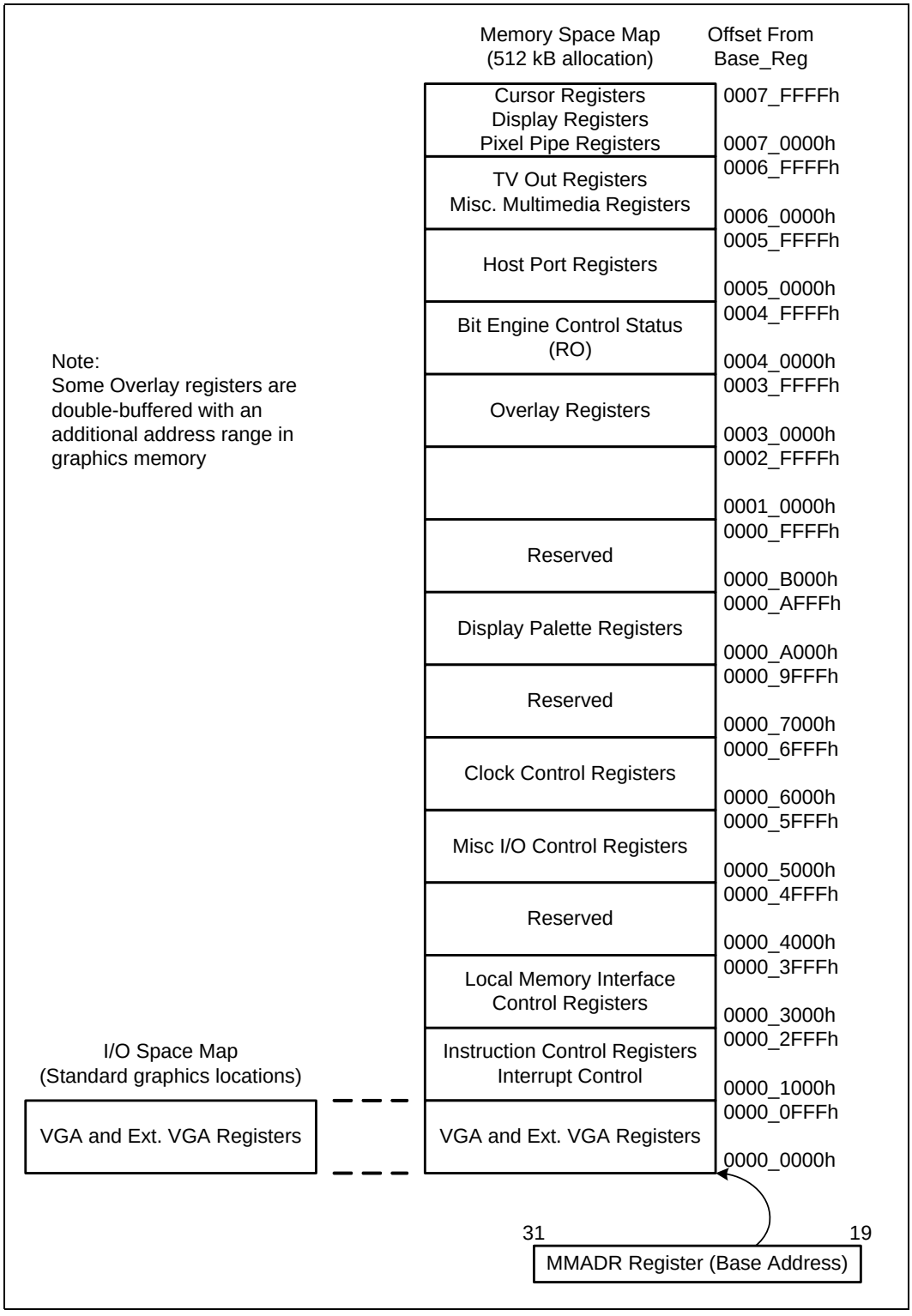
If Device 2 is enabled, and Function 0 within Device 2 is enabled, then IGD registers can be accessed using the IOBAR.

MMIO_Index: MMIO_INDEX is a 32-bit register. An I/O write to this port loads the address of the MMIO register that needs to be accessed. I/O Reads returns the current value of this register.

MMIO_Data: MMIO_DATA is a 32-bit register. An I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register.

The memory and I/O maps for the graphics registers are shown in Figure 6, except PCI Configuration registers, which are described in Volume 2 of this document.

Figure 6. Graphics Register Memory and I/O Map



4.7 System Management Mode (SMM)

SMM uses main memory for System Management RAM (SMRAM). The (G)MCH supports:

- Compatible SMRAM (C_SMRAM)
- High Segment (HSEG)T
- Top of Memory Segment (TSEG)

SMRAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. (G)MCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI and PCI Express masters are not allowed to access the SMM space.

4.7.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 6 describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

Table 6. SMM Space Definition Summary

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD minus STOLEN minus TSEG) to (TOLUD minus STOLEN)	(TOLUD minus STOLEN minus TSEG) to (TOLUD minus STOLEN)

4.8 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any PCI devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR must not target DRAM from A_0000-F_FFFF.

4.8.1 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1) the Compatible SMM space is effectively disabled. Processor originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 7. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

4.8.2 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at power up. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 8. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	X	X	X	X	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	X	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	X	Invalid	Invalid
1	1	X	X	0	Disable	Disable
1	1	0	X	1	Enable	Enable
1	1	1	X	1	Enable	Disable

4.8.3 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to SMM space.

4.8.4 Processor WB Transaction to an Enabled SMM Address Space

Processor Writeback transactions (REQ[1]# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

4.9 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into (G)MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

4.10 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the processor bus. The (G)MCH generates either DMI or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge the (G)MCH contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement a configuration space access mechanism.

The processor allows 64 kB plus 3 B to be addressed within the I/O space. The (G)MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64 kB plus 3 B locations. Note that the upper three locations can be accessed only during I/O address wrap-around when processor

bus H_A#16 address signal is asserted. H_A#16 is asserted on the processor bus whenever an I/O access is made to 4 bytes from address 0000_FFFDh, 0000_FFFEh, or 0000_FFFFh. H_A#16 is also asserted when an I/O access is made to 2 bytes from address 0000_FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the integrated graphics device if it is enabled. The mechanisms for integrated graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

For the processor, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The (G)MCH will break this into two separate transactions. This was not done on chipsets prior to the Intel® 915 Express Chipset family. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into two transactions by the processor.

4.10.1 PCI Express I/O Address Mapping

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in (G)MCH Device 1 configuration space.

The (G)MCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

I/O_Base_Address ≤ Processor I/O Cycle Address ≤ I/O_Limit_Address.

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The (G)MCH also forwards accesses to the legacy VGA I/O ranges according to the settings in the Device 1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the DMI Interface/PCI. The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the (G)MCH will decode legacy monochrome IO ranges and forward them to the DMI Interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

Note: The (G)MCH Device 1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI Express.

4.11 (G)MCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000 to 000A_FFFF

MDA = 000B_0000 to 000B_7FFF

VGAB = 000B_8000 to 000B_FFFF

MAINMEM = 0100_0000 to TOLUD

4.11.1 Legacy VGA and I/O Range Decode Rules

The legacy 128-kB VGA memory range 000A_0000h to 000B_FFFFh can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the (G)MCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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5 System Memory Controller

5.1 Functional Overview

The chipset system memory controller supports DDR2 SDRAMs.

Dual memory channel organizations are supported:

- Dual-channel Interleaved (Single SO-DIMM per channel)
- Dual-channel Asymmetric (Single SO-DIMM per channel)

Each channel has a 64-bit data interface and the frequencies supported are 533 MHz and 667 MHz.

Note: The chipset supports only one SO-DIMM connector per channel.

Each channel can have one or two ranks populated. There can be a maximum of four ranks (two double-sided SO-DIMMs) populated.

Table 9. System Memory Organization Support for DDR2

DDR2								
Tech	SDRAM Org	SO-DIMM size	SO-DIMM Org	Banks	Ranks	Page Size (dev/ module)	Max Capacity (2 SO-DIMMs)	Freq
256 Mb	x8	256 MB	32Mx64	4	1	1K/8K	512 MB	533/667
256 Mb	x16	128 MB	16Mx64	4	1	1K/4K	256 MB	533/667
256 Mb	x16	256 MB	32Mx64	4	2	1K/4K	512 MB	533/667
512 Mb	x8	512 MB	64Mx64	4	1	1K/8K	1 GB	533/667
512 Mb	x8	1 GB	128Mx64	4	2	1K/8K	2 GB	533/667
512 Mb	x16	256 MB	32Mx64	4	1	1K/8K	512 MB	533/667
512 Mb	x16	512 MB	64Mx64	4	2	2K/8K	1 GB	533/667
1 Gb	x8	1 GB	128Mx64	8	1	2K/8K	2 GB	533/667
1 Gb	x8	2 GB	256Mx64	8	2	1K/8K	4 GB	533/667

5.2 Memory Channel Access Modes

The system memory controller supports two styles of memory access (dual-channel Interleaved and dual-channel Asymmetric). Rules for populating SO-DIMM slots are included in this chapter.

5.2.1 Dual Channel Interleaved Mode

This mode provides maximum performance on real applications. Addresses alternate between the channels after each cache line (64-byte boundary). The channel selection address bit is controlled by DCC[10:9]. If a second request sits behind the first, and that request is to an address on the second channel, that request can be sent before data from the first request has returned. Due to this feature, some progress is made even during page conflict scenarios. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawback of conventional Interleaved mode is that the system designer must populate both channels of memory so that they have equal capacity; however, the technology and device width may vary from one channel to the other.

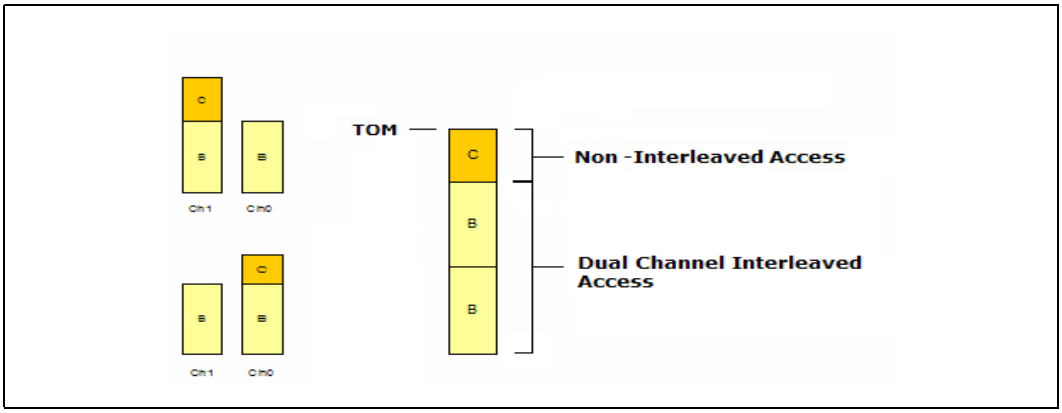
5.2.1.1 Intel® Flex Memory Technology (Dual Channel Interleaved Mode with Unequal Memory Population)

The (G)MCH supports interleaved addressing in dual-channel memory configurations even when the two channels have unequal amounts of memory populated. This is called Intel® Flex Memory Technology.

Intel Flex memory provides higher performance with different sized channel populations than Asymmetric mode (where no interleaving is used) by allowing some interleaving.

The memory addresses up to the twice the size of the smaller SO-DIMM are interleaved on a 64-B boundary using address bit 6 (including any XOR-ing already used in interleaved mode). Above this, the rest of the address space is assigned to the remaining memory in the larger channel. Figure 7 shows various configurations of memory populations.

Figure 7. Intel® Flex Memory Technology Operation



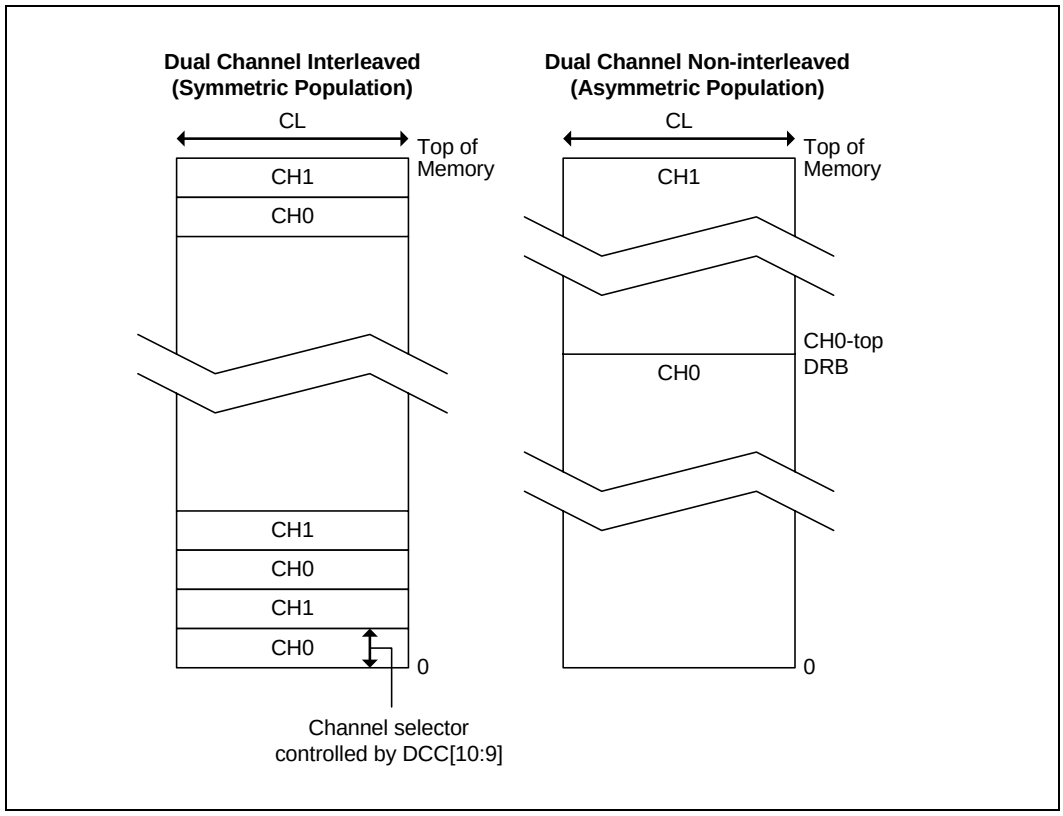
NOTES:

1. **B:** Smaller of the two physical memory amounts: (Accessed in Dual-Channel Interleaved mode)
2. **C:** Extra memory populated over B: (Accessed in non-interleaved mode)
3. To enable Intel Flex Memory Technology, BIOS should program both channels' DRBs (DRAM Rank Boundaries) to the size of memory in that channel, as if for fully interleaved memory (should not add the top of one channel to the other as in Asymmetric mode). Interleaved mode operation should also be enabled.
4. To disable Intel Flex Memory Technology, BIOS should program as usual for the Asymmetric mode.

5.2.2 Dual Channel Non-Interleaved Mode

This mode trades performance for system design flexibility, by allowing unequal amounts of memory to be populated in the two channels. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A, then addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth is limited. The system designer may populate or not populate any rank on either channel, including either degenerate single channel case. Because channel A is addressed first, when using only one channel, channel A should be the channel used.

Figure 8. System Memory Styles



5.3 DRAM Technologies and Organization

- All standard 256-Mb, 512-Mb, and 1-Gb technologies and addressing are supported for x16 and x8 devices. For detailed memory organization support, please refer to Table 9.
- The (G)MCH supports various page sizes. Page size is individually selected for every rank; 4 k and 8 k for Interleaved and Asymmetric dual-channel modes.
- The DRAM sub-system supports only dual channel with 64-bit width per channel.
- The number of ranks each channel can have populated is one or two.
- Mixed mode, double-sided SO-DIMMs (x8 and x16 on the same SO-DIMM) are not supported.

5.3.1 Rules for Populating SO-DIMM Slots

In all modes, the frequency of system memory is the lowest frequency of all SO-DIMMs in the system, as determined through the SPD registers on the SO-DIMMs. The chipset supports only one SO-DIMM connector per channel.

- In dual-channel Interleaved mode, both SO-DIMM slots must be populated, and the total amount of memory in each channel must be the same. The device technologies may differ.
- In dual-channel Asymmetric mode, the total memory in the two channels need not be equal (one slot could even be unpopulated). **When populating only one channel, channel A should be populated.**

5.3.2 Pin Connectivity for Dual Channel Modes

Table 10. DDR2 Dual Channel Pin Connectivity

Dual Channel		
JEDEC Pin Mapping	**Channel A**	**Channel B**
CK[1:0]	SM_CK[1:0]	SM_CK[4:3]
CKB[1:0]	SM_CK#[1:0]	SM_CK#[4:3]
CSB[1:0]	SM_CS#[1:0]	SM_CS#[3:2]
CKE[1:0]	SM_CKE[1:0]	SM_CKE[4:3]
ODT[1:0]	SM_ODT[1:0]	SM_ODT[3:2]
BS[2:0]	SA_BS[2:0]	SB_BS[2:0]
MA[14:0]	SA_MA[14:0]	SB_MA[14:0]
RAS#	SA_RAS#	SB_RAS#
CAS#	SA_CAS#	SB_CAS#
WE#	SA_WE#	SB_WE#
DQ[63:0]	SA_DQ[63:0]	SB_DQ[63:0]
DQS[7:0]	SA_DQS[7:0]	SB_DQS[7:0]
DQS[7:0]#	SA_DQS#[7:0]	SB_DQS#[7:0]
DM[7:0]	SA_DM[7:0]	SB_DM[7:0]

5.4 DRAM Clock Generation

The chipset generates two differential clock pairs for every supported SO-DIMM. There are a total of four clock pairs driven directly by the (G)MCH to two SO-DIMMs.

5.5 DDR2 On Die Termination

On die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DQS/DQS# and DM signal for x8 configurations via the ODT control pin. The ODT improves signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT also improves signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves instead of on the motherboard. The (G)MCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted SO-DIMM rank to enable or disable their termination resistance.

ODT operation follows these general rules:

WRITE

1. Chipset: ODT off
2. DRAM:
   — If one slot populated but has two ranks, turn on termination in the written rank.
   — If one slot/one rank, turn on that rank's termination.

READ

1. Chipset: ODT on
2. DRAM: ODT off

5.6 DRAM Power Management

5.6.1 Self Refresh Entry and Exit Operation

When entering the Suspend-To-RAM (STR) state, (G)MCH will flush pending cycles and then enter all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices will perform self-refresh.

5.6.2 Dynamic Power Down Operation

The chipset implements aggressive CKE control to dynamically put the DRAM devices in a power down state. The (G)MCH controller can be configured to put the devices in *active power down* (CKE deassertion with open pages) or *precharge power down* (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages are needed to be closed before putting the devices in power down mode.

If dynamic power down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

5.6.3 DRAM I/O Power Management

(G)MCH implements several power-saving features, where different groups of IO buffers are disabled when safe to do so in a dynamic fashion, thereby saving IO power. These features are listed below.

- SO-DIMM clock gating disable—The chipset has two clock pairs per SO-DIMM. If only one SO-DIMM is populated, it allows the other two clock pairs to be disabled.
- Unused CKE pins can be tri-stated.
- Address and control tri-state enable—If CKE for any given rank is deasserted, the CS# to that rank is disabled. If all CKEs are deasserted (such as in S3), all address and control buffers (excluding CKEs) are disabled.

- Self refresh master/slave DLL disable—When all the SDRAMs ranks have been put in a self-refresh state, all DLLs are disabled.
- Data sense amp disable (self refresh, dynamic)—When all the SDRAM ranks have been put in a self-refresh state, or during normal operation if no memory accesses are pending, the sense amplifiers for all data buffers are turned off.
- Output only sense amp disable—Sense amplifiers of all IO buffers that are functionally outputs only (everything except DQ and DQS) are turned off.
- RCVEN DLL disable—The (G)MCH has DLLs for timing the RCVEN signal. If only one SO-DIMM is populated, the unused DLLs are turned off.

5.7 System Memory Throttling

The chipset has two independent mechanisms, (G)MCH thermal management and DRAM thermal management, that causes system memory bandwidth throttling. For more information on system memory throttling, see Section 11.2.

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6 PCI Express Based External Graphics

See the *PCI Express Specification* for details on PCI Express.

This (G)MCH is part of a PCI Express root complex that connects a host processor/ memory subsystem to a PCI Express hierarchy. The control registers for this functionality are located in Device 1 configuration space and two root complex register blocks (RCRBs).

6.1 PCI Express Architecture

Compatibility with the PCI addressing model (a load - store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI plug-and-play specification. The initial speed of 2.5-GHz (250 MHz internally) results in 2.5 GB/s direction that provides a 250-MB/s communications channel in each direction (500 MB/s total) and is close to twice the data rate of classic PCI per lane.

The PCI Express architecture is specified in layers. The layers include:

- Transaction layer
- Data Link Layer
- Physical layer

PCI Express uses packets to communicate information between components. Packets are formed in the transaction and data link layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side the reverse process occurs and packets get transformed from their physical layer representation to the data link layer representation and finally (for transaction layer packets) to the form that can be processed by the transaction layer of the receiving device.

6.1.1 Transaction Layer

The upper layer of the PCI Express architecture, the transaction layer's primary responsibility is the assembly and disassembly of transaction layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The transaction layer also manages flow control of TLPs.

6.1.2 Data Link Layer

This middle layer in the PCI Express stack serves as an intermediate stage between the transaction layer and the physical layer. Responsibilities include link management, error detection, and error correction.

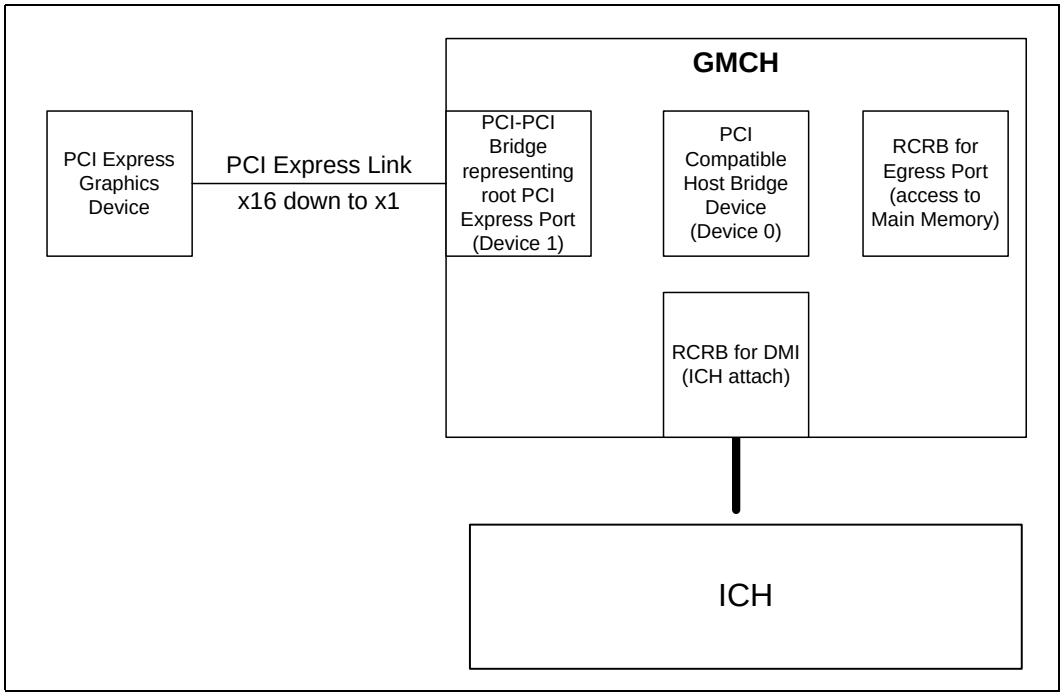
6.1.3 Physical Layer

The physical layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

6.2 PCI Express Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 9. PCI Express Related Register Structures in (G)MCH



PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification. PCI Express configuration space is divided into a PCI-compatible region, which consists of the first 256 bytes of a logical device's configuration space and an extended PCI Express region, which consists of the remaining configuration space. The PCI compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the PCI Express Enhanced Configuration Mechanism section.

The PCI Express host bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only.

See the PCI Express Specification for details of both the PCI compatible and PCI Express enhanced configuration mechanisms and transaction rules.

6.3 Serial Digital Video Output (SDVO)

The SDVO description is located here because it is muxed onto the PCI Express x16 port pins. The AC/DC specifications are identical to the PCI Express Graphics interface.

SDVO electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependent upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, an SDVO port will transmit display data in a high-speed, serial format across differential AC coupled signals. An SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

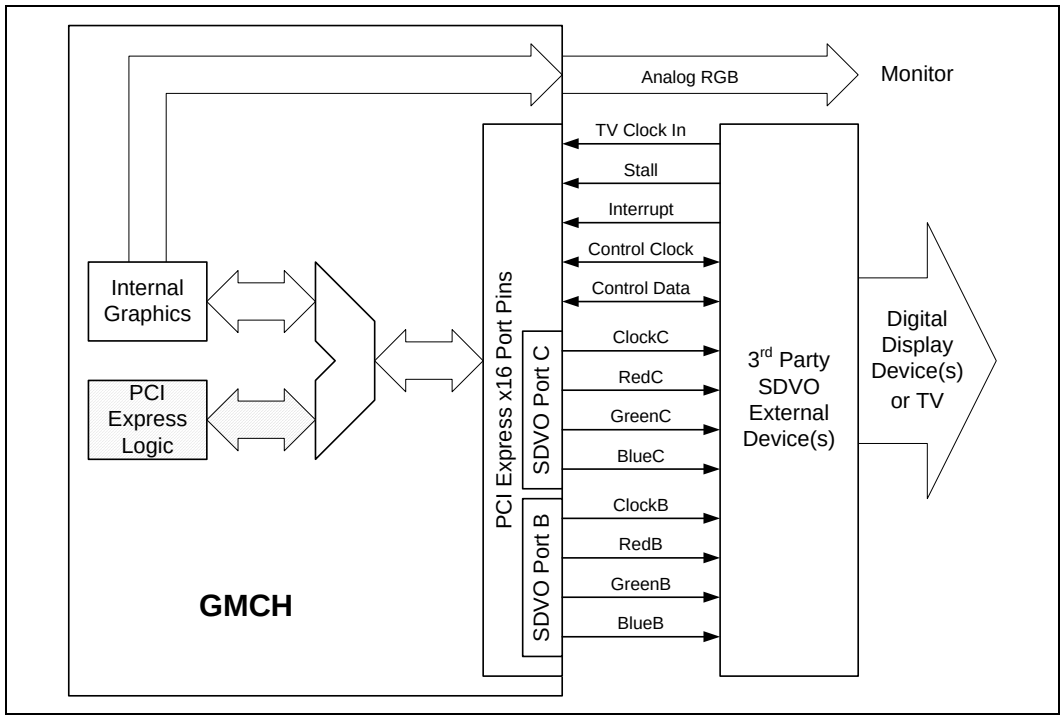
6.3.1 SDVO Capabilities

SDVO ports can support a variety of display types including LVDS, DVI, HDMI, TV-Out, and external CE type devices.

The chipset utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings. The integrated graphics controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface.

The SDVO port defines a two-wire, point-to-point communication path between the SDVO device and (G)MCH. The SDVO Control Clock (SDVO_CTRL_CLK) and data (SDVO_CTRL_DATA) provide similar functionality to I^2C. However unlike I^2C, this interface is intended to be point-to-point (from the (G)MCH to the SDVO device) and will require the SDVO device to act as a switch and direct traffic from the SDVO Control bus to the appropriate receiver. Additionally, the SDVO Control bus is able to run at faster speeds (up to 1 MHz) than a traditional I^2C interface would.

Figure 10. SDVO Conceptual Block Diagram



6.3.2 Concurrent SDVO/PCI Express Operation

The (G)MCH supports concurrent operation of the SDVO port with video capture via x1 PCI Express interface. Note that the only type of data supported over the x1 PCI Express link is video capture.

SDVO slot reversal is also supported on the GM965/GME965 chipset. The (G)MCH will allow SDVO and x1 PCI Express to operate concurrently on the PCI Express-based Graphics link.

The PCI Express lanes comprise a standard PCI Express link and must always originate with lane 0 on the PCI Express connector. The only supported PCI Express width when SDVO is present is x1.

This concurrency is supported in reversed and non-reversed configurations. Mirroring / Reversing are always about the axis between lanes 7 and 8. When SDVO is reversed, SDVO Lane 0 corresponds to what would be PCI Express pin/connector lane 15 (mirrored to higher lane numbers).

Table 12 shows hardware reset straps used to determine which of the six configurations below is desired.

Table 12. Concurrent SDVO / PCI Express* Configuration Strap Controls

Configuration Number	Description	Slot Reversed Strap (CFG9)	SDVO Present Strap (SDVO_CTRLDATA)	SDVO/PCI Express Concurrent Strap (CFG20)
1	PCI Express*-only not reversed	High	Low	Low
2	PCI Express-only Reversed	Low	Low	Low
3	SDVO-only not reversed	High	High	Low
4	SDVO-only Reversed	Low	High	Low
5	SDVO and PCI Express not reversed	High	High	High
6	SDVO and PCI Express Reversed	Low	High	High

NOTE: Details of the implementations corresponding to the configuration number are shown below.

Figure 11. SDVO/PCI Express Non-Reversed Configurations

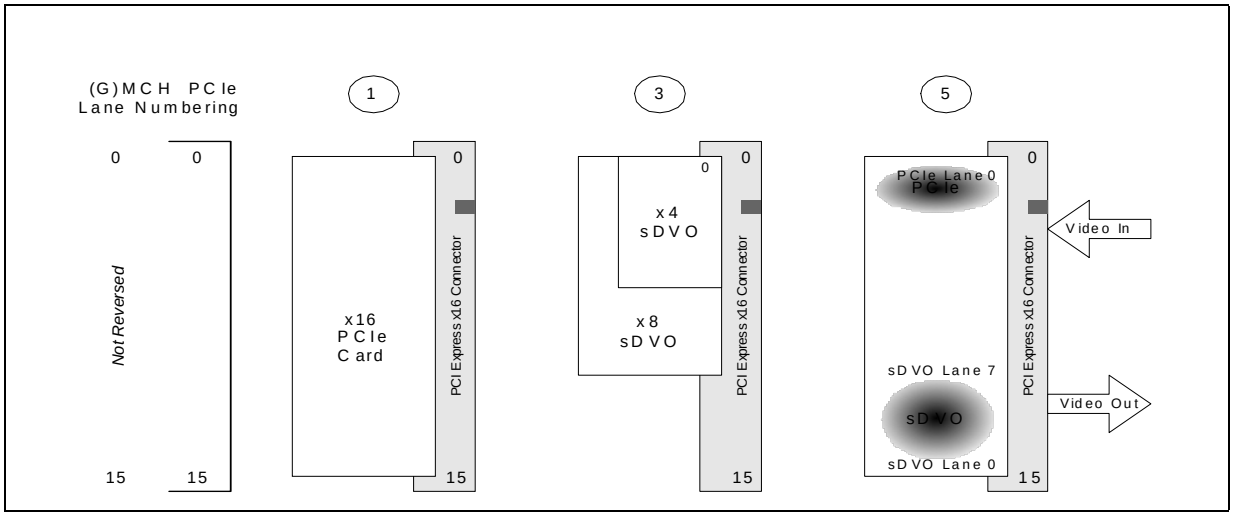
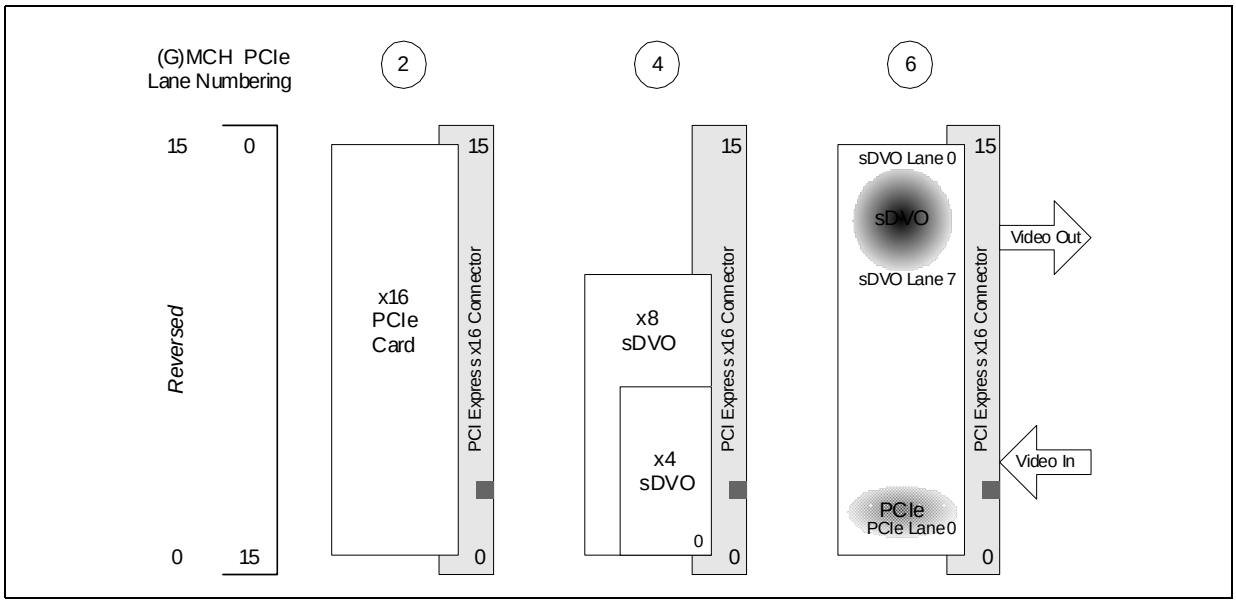


Figure 12. SDVO/PCI Express* Reversed Configurations



6.3.2.1 SDVO Signal Mapping

Table 13 shows the mapping of SDVO signals to the PCI Express lanes in the various possible configurations as determined by the strapping configuration. Note that slot-reversed configurations do not apply to the Integrated graphics-only variants.

Table 13. Configuration-wise Mapping of SDVO Signals on the PCI Express Interface

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal (3)	SDVO Only – Reversed (4)	Concurrent SDVO and PCI Express – Normal (5)	Concurrent SDVO and PCI Express – Reversed (6)
SDVOB_RED#	EXP_TXN0	EXP_TXN15	EXP_TXN15	EXP_TXN0
SDVOB_RED	EXP_TXP0	EXP_TXP15	EXP_TXP15	EXP_TXP0
SDVOB_GREEN#	EXP_TXN1	EXP_TXN14	EXP_TXN14	EXP_TXN1
SDVOB_GREEN	EXP_TXP1	EXP_TXP14	EXP_TXP14	EXP_TXP1
SDVOB_BLUE#	EXP_TXN2	EXP_TXN13	EXP_TXN13	EXP_TXN2
SDVOB_BLUE	EXP_TXP2	EXP_TXP13	EXP_TXP13	EXP_TXP2
SDVOB_CLKN	EXP_TXN3	EXP_TXN12	EXP_TXN12	EXP_TXN3
SDVOB_CLKP	EXP_TXP3	EXP_TXP12	EXP_TXP12	EXP_TXP3
SDVOC_RED#	EXP_TXN4	EXP_TXN11	EXP_TXN11	EXP_TXN4
SDVOC_RED	EXP_TXP4	EXP_TXP11	EXP_TXP11	EXP_TXP4
SDVOC_GREEN#	EXP_TXN5	EXP_TXN10	EXP_TXN10	EXP_TXN5
SDVOC_GREEN	EXP_TXP5	EXP_TXP10	EXP_TXP10	EXP_TXP5
SDVOC_BLUE#	EXP_TXN6	EXP_TXN9	EXP_TXN9	EXP_TXN6
SDVOC_BLUE	EXP_TXP6	EXP_TXP9	EXP_TXP9	EXP_TXP6
SDVOC_CLKN	EXP_TXN7	EXP_TXN8	EXP_TXN8	EXP_TXN7
SDVOC_CLKP	EXP_TXP7	EXP_TXP8	EXP_TXP8	EXP_TXP7
SDVO_TVCLKIN#	EXP_RXN0	EXP_RXN15	EXP_RXN15	EXP_RXN0
SDVO_TVCLKIN	EXP_RXP0	EXP_RXP15	EXP_RXP15	EXP_RXP0
SDVOB_INT#	EXP_RXN1	EXP_RXN14	EXP_RXN14	EXP_RXN1
SDVOB_INT	EXP_RXP1	EXP_RXP14	EXP_RXP14	EXP_RXP1
SDVO_FLDSTALL#	EXP_RXN2	EXP_RXN13	EXP_RXN13	EXP_RXN2
SDVO_FLDSTALL	EXP_RXP2	EXP_RXP13	EXP_RXP13	EXP_RXP2
SDVOC_INT#	EXP_RXN5	EXP_RXN10	EXP_RXN10	EXP_RXN5
SDVOC_INT	EXP_RXP5	EXP_RXP10	EXP_RXP10	EXP_RXP5

6.4 SDVO Modes

The port can be dynamically configured in several modes:

- Standard—Baseline SDVO functionality. Supports pixel rates between 25 and 200 MP/s. Utilizes three data pairs to transfer RGB data.
- Dual Standard—Utilizes standard data streams across both SDVO B and SDVO C. Both channels can only run in standard mode (three data pairs) and each channel supports pixel rates between 25 and 200 MP/s. There are two types of dual standard modes:

— Dual Independent Standard—In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVO B will not be the same as the data stream across SDVO C.

— Dual Simultaneous Standard—In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVO B is the same as the data stream across SDVO C. The display timings are identical, but the transfer timings may not be; that is, SDVO B Clocks and Data may not be perfectly aligned with SDVO C Clock and Data as seen at the SDVO device(s). Since this utilizes just a single data stream, it utilizes a single pixel pipeline within the (G)MCH.

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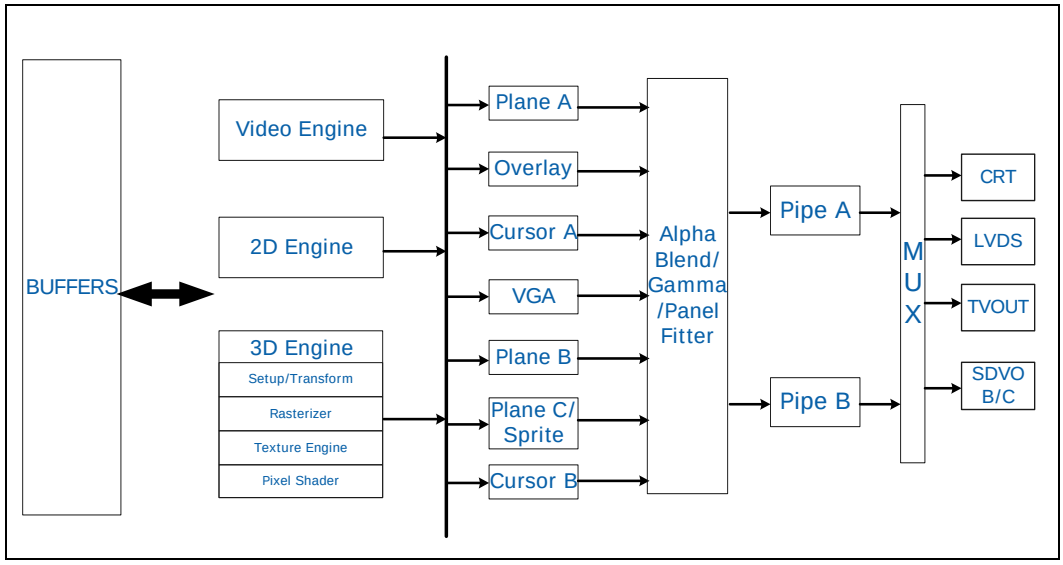
7 Integrated Graphics Controller

The (G)MCH graphics is powered by the Mobile Intel® GMA X3100, bringing new levels of richness and realism to DirectX 9 enabled applications. It supports eight programmable Execution cores, enabling greater performance than previous generation chipsets.

The Mobile Intel GMA X3100 contain several types of components, which include: the engines, planes, pipes and ports. The Mobile Intel GMA X3100 has a 3D/2D Instruction Processing unit to control the 3D and 2D engines. The Mobile Intel GMA X3100's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to memory, which are then retrieved and processed by the Mobile Intel GMA X3100 planes.

Figure 13. (G)MCH Graphics Controller Block Diagram



The Mobile Intel GMA X3100 contains a variety of planes, such as display, overlay, cursor and VGA. A plane consists of a rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The Mobile Intel GMA X3100 has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe.

The entire Mobile Intel GMA X3100 is fed with data from its memory controller. The Mobile Intel GMA X3100 performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (for example, single-channel DDR2 533 MHz), the rest of the Mobile Intel GMA X3100 will also be affected.

7.1 Graphics Processing

7.1.1 3D Graphics Pipeline

- Additional processing capability added to the Geometry stage with a vertex shader, geometry shader, and clipper.
- A deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive.
- Optimized using current and future Intel processor family for advance software based transform and lighting (geometry processing) as defined by Microsoft DirectX API.
- Rasterization engine converts vertices to pixels and the texture engine applies textures to pixels.
- Rasterization engine takes textured pixels and applies lighting and other environmental affects to produce the final pixel value.
- From the rasterization stage the final pixel value is written to the frame buffer in memory so that it can be displayed.

7.1.2 3D Engine

Mobile Intel GMA X3100 supports:

- 32-bit full precision floating point operations, as against 24-bit in previous chipsets
- Up to eight Multiple Render Targets (MRTs), further optimizing performance in execution of instructions.
- Acceleration for all Microsoft DirectX 9 and SGI OpenGL 1.5 required features as well as other additional features. Some of the key features supported are:
  - The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the Setup Engine, Rasterizer, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.
  - The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

7.1.2.1 Setup Engine

The setup stage of the pipeline takes the input data associated with each vertex of 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the Mobile Intel GMA X3100 maintains sub-pixel accuracy.

7.1.2.1.1 3D Primitives and Data Formats Support

The 3D primitives rendered are points, lines, discrete triangles, line strips, triangle strips, triangle fans and polygons. In addition to this, The Mobile Intel GMA X3100 supports the Microsoft DirectX Flexible Vertex Format (FVF), which enables the application to specify a variable length of parameter list obviating the need for sending unused information to the hardware. Strips, Fans and Indexed Vertices, as well as FVF, improve the vertex rate delivered to the setup engine significantly.

7.1.2.1.2 Pixel Accurate “Fast” Scissoring and Clipping Operation

- Supports 2D clipping to the scissor rectangle, avoiding processing pixels that fall outside the rectangle.
- Clipping and scissoring in hardware reduce the need for software to clip objects, and thus improve performance.
- During the setup stage, clips objects to the scissor window.

7.1.2.1.3 Depth Bias

Supports source Depth Biasing in the Setup Engine. Depth Bias value is specified in the vertex command packet on a per primitive basis. The value ranges from -1 to 1. The Depth Bias value is added to the z value of the vertices. By using Depth Bias, it is possible to offset the destination z value (compare value) before comparing with the new z value.

7.1.2.1.4 Backface Culling

As part of the setup, the Mobile Intel GMA X3100 discards polygons from further processing, if they are facing away from or towards the user’s viewpoint, thus optimizing all further steps.

7.1.2.1.5 Color Shading Modes

The Raster engine supports the Flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex’s attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has a different value.

7.1.2.1.6 Occlusion Query

Occlusion query is a new addition on the Mobile Intel GMA X3100. It optimizes application performance by minimizing overhead on the depth buffer. It also enables support for new features and effects such as Lens Flare.

7.1.2.2 Rasterizer

Working on a per-polygon basis, the rasterizer uses the vertex and edge information is used to identify all pixels affected by features being rendered.

7.1.2.2.1 Pixel Rasterization Rules

The Mobile Intel GMA X3100 supports both SGI OpenGL and D3D* pixel rasterization rules to determine whether a pixel is filled by the triangle or line. For both D3D and OpenGL modes, a top-left filling convention for filling geometry will be used. Pixel rasterization rule on rectangle primitive is also supported using the top-left fill convention.

7.1.2.2.2 Pixel Pipeline

The pixel pipeline function combines for each pixel:

- Interpolated vertex components from the scan conversion function
- Texel values from the texture samplers
- Pixel's current values from the color and/or depth buffers

This combination is performed via a programmable pixel shader engine, followed by a pipeline for optional pixel operations performed in a specific order. The result of these operations can be written to the color and depth buffers.

7.1.2.3 Texture Engine

The Mobile Intel GMA X3100 allows an image, pattern, or video to be placed on the surface of a 3D polygon.

The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the rasterizer. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear and bilinear interpolation), and YUV to RGB conversions. Enhancements to the texture engine include dynamic filtering of up to 16 samples in anistropic filtering, as compared to a maximum of 4 samples in on previous chipsets.

7.1.2.3.1 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance.

7.1.2.3.2 Texture Formats and Storage

Supports up to 128 bits of color for textures, including support for textures with floating point components.

7.1.2.3.3 Texture Decompression

DirectX supports Texture Compression to reduce the bandwidth required to deliver textures. As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide a mechanism for compressing textures. Texture decompression formats supported include DXT1, DXT2, DXT3, DXT4, DXT5, FXT1, BC4 and BC5.

7.1.2.3.4 Texture ChromaKey

ChromaKey describes a method of removing a specific color or range of colors from a texture map before it is applied to an object. For the nearest texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For linear texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

7.1.2.3.5 Texture Map Filtering

- Supports many texture mapping modes. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

- Supports up to 14 levels of detail (LODs) ranging in size from 8192 X 8192 to 1 x 1 texels. Textures need not be square. Included in the texture processor is a texture cache, which provides efficient MIP mapping.

7.1.2.3.6 Multiple Texture Composition

Performs multiple texture composition. This allows the combination of two or more MIP maps to produce a new one with new LODs and texture attributes in a single or iterated pass. Flexible vertex format support allows multitexturing because it makes it possible to pass more than one texture in the vertex structure.

7.1.2.3.7 Cubic Environment Mapping

The Mobile Intel GMA X3100 supports cubic reflection mapping over spheres and circles since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

- A texture map for each of the six cube faces can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction.
- Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces is calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.
- Supports multiple texture map surfaces arranged into a cubic environment map is supported.
- Supports CLAMP and CUBE texture address mode for Cube maps.
- Supports new format for Compressed Cube maps that allow each MIP/face to exist in its own compression block.

7.1.2.3.8 Hardware Pixel Shader

A pixel shader serves to manipulate a pixel, usually to apply an effect on an image, for example; realism, bump mapping, shadows, and explosion effects. It is a graphics function that calculates effects on a per-pixel basis.

7.1.2.3.9 Color Dithering

Color Dithering helps to hide color quantization errors. Color Dithering takes advantage of the human eye's propensity to average the colors in a small area. Input color, alpha, and fog components are converted from 5 or 6-bit component to 8-bit components by dithering. Dithering is performed on blended textured pixels with random lower bits to avoid visible boundaries between the relatively discrete 5/6-bit colors. Dithering is not performed on components containing 8 bits or more.

7.1.2.3.10 Vertex and Per Pixel Fogging

Fog is simulated by attenuating the color of an object with the fog color as a function of distance. The higher the density (lower visibility for distant objects).

The Mobile Intel GMA X3100 supports both types of fog operations, vertex and per pixel or table fog:

- Per-vertex (linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small.
- Per-pixel (non-linear) fogging. the per-vertex technique results in unnatural fogging with large polygons (such as a ground plane depicting an airport runway).

7.1.2.3.11 Alpha Blending (Frame Buffer)

Alpha Blending adds the property of transparency or opacity to an object. Alpha blending combines a source pixel color (RSGSBS) and alpha (AS) component with a destination pixel color (RDGDBD) and alpha (AD) component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha are supported.

7.1.2.3.12 Color Buffer Formats: 8, 16, 32, 64 or 128 Bits Per Pixel (Destination Alpha)

The raster engine will support 8-, 16-, 32-, 64- and 128-bit color buffer formats. The 8-bit format is used to support planar YUV420 format, which is used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z is allowed to mix.

Supports both double and triple buffering, where one buffer is the primary buffer used for display and one or two are the back buffer(s) used for rendering.

The frame buffer contains at least two hardware buffers: the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). Rendering to one and displaying from the other remove the possibility of image tearing and speeds up the display process over a single buffer. The instruction set of the Mobile Intel GMA X3100 provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

7.1.2.3.13 Depth Buffer

The raster engine can read and write from this buffer and use the data in per fragment operations that determine whether resultant color and depth value of the pixel for the fragment are to be updated or not.

7.1.2.3.14 Stencil Buffer

The Raster engine provides 8-bit stencil buffer storage in 32- and 64-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis, conditionally eliminating a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows and constructive solid geometry rendering.

7.1.2.3.15 Intermediate Z

Supports intermediate Z test, which avoids pixel processing on occluded polygons for enhanced 3D graphics performance

7.1.3 2D Engine

Contains BLT functionality, and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions such as Alpha BLTs, arithmetic (bilinear) stretch BLTs, rotations, transposing pixel maps, limited color space conversion, and DIBs make use of the 3D renderer.

7.1.3.1 Video Graphics Array Registers

The 2D registers are a combination of registers for the original Video Graphics Array (VGA) and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

7.1.3.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows operating systems. The 128-bit, Mobile Intel GMA X3100 BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The Mobile Intel GMA X3100 BLT engine:

- Can expand monochrome data into a color depth of 8, 16, or 32 bits.
- Supports Opaque and Transparent transfers.
  - — Opaque transfers move the data specified to the destination.
  - — Transparent transfers compare destination color to source color and write according to the mode of transparency selected.
- Horizontally and vertically aligns data at the destination. If the destination for the BLT overlaps with the source memory location, the Mobile Intel GMA X3100 can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, pattern, and destination) defined by Microsoft, including transparent BLT.
- Provides instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing.
- Can perform hardware clipping during BLTs.

7.1.3.3 HW Rotation

The Mobile Intel GMA X3100 has made it possible for the primary display of a Dual Display Clone configuration to be independently rotated at 180º when secondary display is in normal mode (0°) or vice versa. This is achieved by hardware accelerated rotation.

7.1.4 Video Engine

7.1.4.1 Dynamic Video Memory Technology (DVMT 4.0)

DVMT is an enhancement of the Unified Memory Architecture (UMA) concept, wherein the optimum amount of memory is allocated for balanced graphics and system performance. DVMT ensures the most efficient use of available memory—regardless of frame buffer or main memory size—for balanced 2D/3D graphics performance and system performance. DVMT dynamically responds to system requirements and applications' demands, by allocating the proper amount of display, texturing and buffer memory after the operating system has booted. For example, a 3D application when launched may require more vertex buffer memory to enhance the complexity of objects or more texture memory to enhance the richness of the 3D environment. The operating system views the Intel Graphics Driver as an application, which uses Direct AGP to request allocation of additional memory for 3D applications, and returns the memory to the operating system when no longer required.

7.1.4.2 Intel® Clear Video Technology

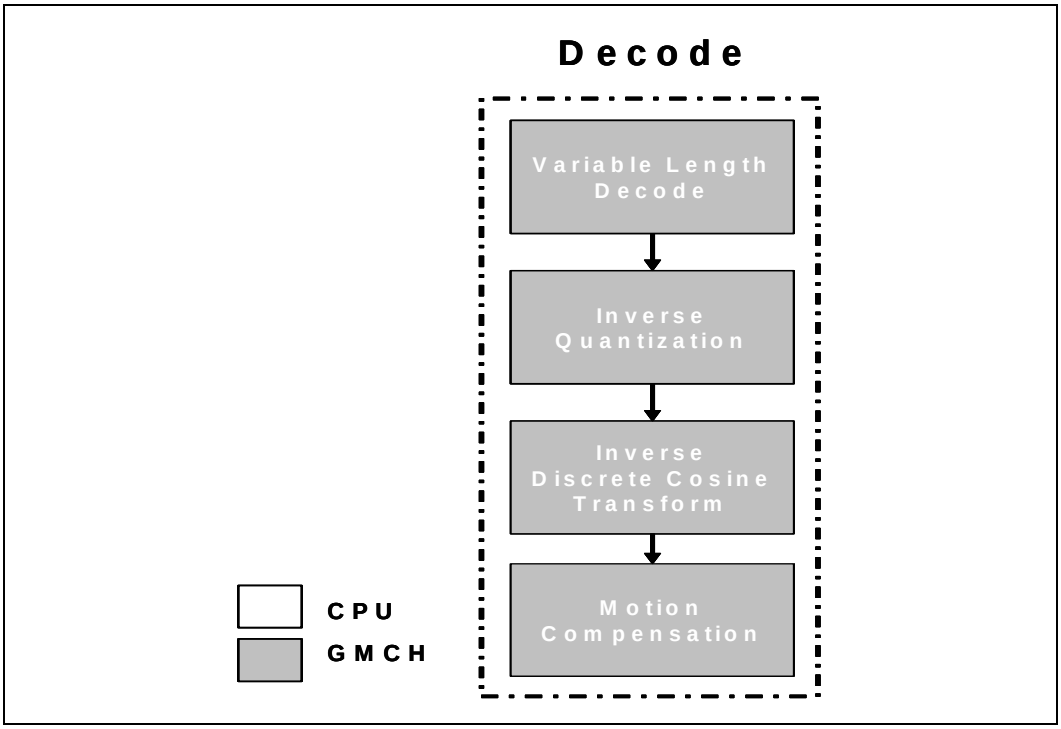
Intel® Clear Video Technology enables new features such as:

- MPEG-2 Hardware Acceleration
- WMV9 Hardware Acceleration
- ProcAmp
- Advanced Pixel Adaptive De-interlacing
- Sharpness Enhancement
- De-Noise Filter
- High Quality scaling
- Film mode detection and correction
- Intel® TV Wizard to deliver an outstanding media experience on the Mobile Intel GMA X3100

7.1.4.2.1 MPEG-2 Hardware Acceleration

MPEG-2 content format is one of the most prevalent formats for video content. Partitioning the MPEG-2 workload between the integrated graphics device and the CPU allows for reduced workload when performing simultaneous support of up to two streams of video. Figure 14 illustrates the hardware acceleration provided by the Mobile Intel GMA X3100 for the MPEG-2 decode pipeline.

Figure 14. MPEG-2 Decode Stage



7.1.4.2.2 WMV9 Hardware Acceleration

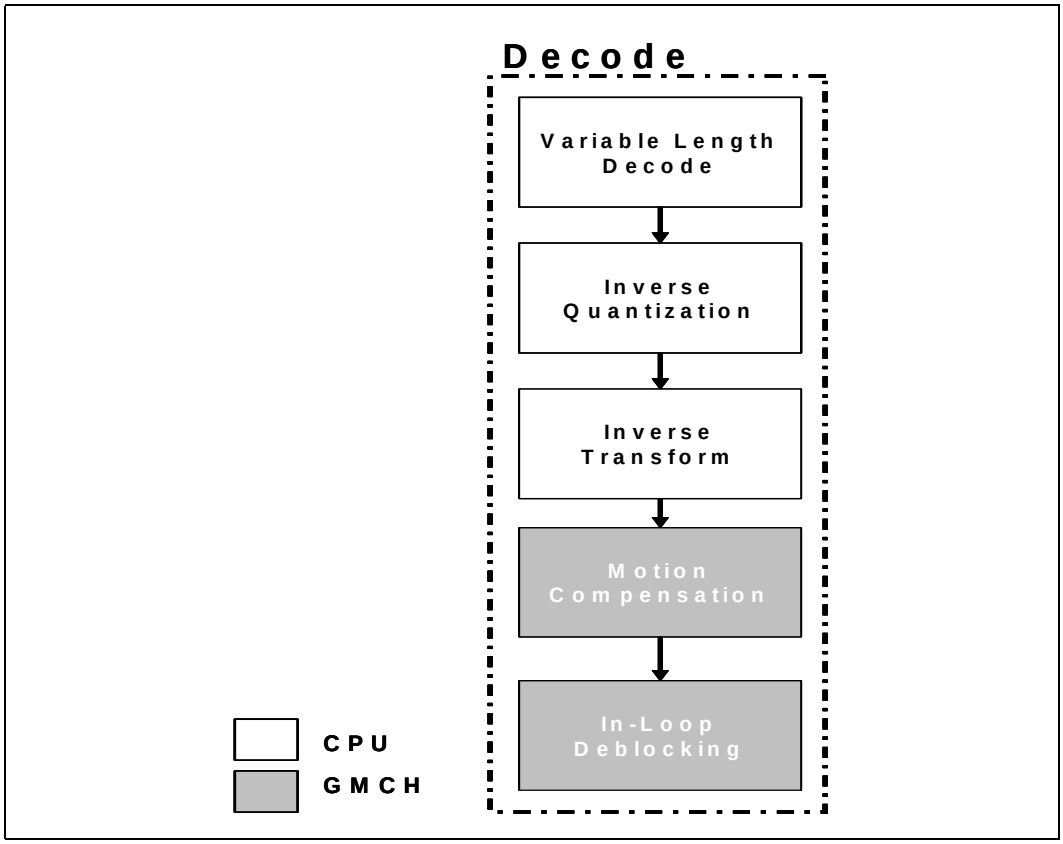
VC-1 is the name given to the WMV9 standard submitted by Microsoft for SMPTE approval. The SMPTE body expanded the scope of VC-1 to also comprehend interlaced content as well as various different transport streams needed for CE and broadcast use. VC-1 content is a format growing in popularity and will be a key format for future high definition content, as both HD-DVD and Blu-Ray* DVD specifications require VC-1 support.

WMV9 is bitstream compatible with VC-1, however it is optimized for progressive content only and thus has different software entry points than standard VC-1. The Mobile Intel GMA X3100 core provides hardware acceleration for the WMV9 stages indicated in Figure 15.

Note: The various decode stages of WMV9 are typically referred to by letter.

The Mobile Intel GMA X3100 core provides hardware acceleration for the WMV9b stage of the decode pipeline, specifically, this accelerates the motion compensation and in-loop deblocking stages for progressive content.

Figure 15. WMV9 Decode Stage



7.1.4.2.3 ProcAmp

ProcAmp is the short name for “Processing Amplifier”. It is an amplifier to adjust video visual attributes, such as brightness, contrast, hue and saturation. These adjustments are typically controlled by users through the video player application. However when using Microsoft’s DXVA driver interface, the ProcAmp calls to the Mobile Intel GMA X3100 core are utilized to perform image enhancements on a frame by frame basis.

7.1.4.2.4 Advanced Pixel Adaptive De-interlacing

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. These fields have alternating lines of data and thus must be adapted for use on progressive PC displays. There are several basic schemes to deinterlace the video stream: line replication, vertical filtering, field merging and vertical temporal filtering. All of these create varying degrees of visual artifacts.

The Mobile Intel GMA X3100 core brings with it enhanced hardware integration allowing de-interlacing of video content for a high quality experience with interlaced formats. It also reduces static and motion artifacts with an edge adaptive spatial, temporal filter and motion detector. A pixel adaptive de-interlacing algorithm provides enhanced picture clarity for interlaced content. Hardware acceleration off loads post-processing from CPU to chipset to reduce CPU utilization, further improving performance.

7.1.4.2.5 Film Mode Detection and Correction

A special case of deinterlacing deals with *pulled down* content.

For example, when broadcasting a typical movie over NTSC TV, 3:2 pull down converts 24 progressive frames/sec into 60 interlaced fields/sec. Playing back such an encoded stream using typical deinterlacing methods misses an opportunity to achieve significantly enhanced visual quality. By detecting the repetitive 3:2 cadence, Intel Clear Video Technology can recreate the original progressive frames by working with the original progressive content and artifacts are minimized.

Making use of Intel Clear Video Technology's Film Mode Cadence Detection and Correction features is fully transparent to video playback software. Playback software need only request the highest level of deinterlacing be utilized. Intel Clear Video Technology will automatically apply the necessary algorithms for perfect deinterlacing if a recognized cadence is observed. Otherwise, the highest level of deinterlacing supported is utilized.

7.1.4.2.6 Sharpness Enhancement

Intel's sharpness enhancement filters reduce the appearance of artifacts by identifying and operating on the edges within an image. By applying noise reduction algorithms specifically on shape edges and improving contrast ratios in these specific regions, Intel Clear Video Technology helps mitigate artifacts that typically accompany high-scale ratios.

7.1.4.2.7 De-noise Filter

When working with analog video streams, capturing, converting, and duplicating the content will inject analog noise into the stream; thus degrading the overall video quality. Digital video streams can also exhibit similar artifacts as a result of their original capture or their subsequent compression. Noise artifacts are most noticeable in regions of the image that contain large areas of solid colors.

Traditional de-noise algorithms often suppress fine detail within an image by mistaking the detail for noise. However, Intel Clear Video Technology leverages its motion detection algorithms to dramatically reduce the appearance of randomized noise in video streams while accurately preserving fine detail. By realizing that noise artifacts are nondeterministic in their motion, Intel's de-noise filters are able to differentiate between noise and valid video data.

7.1.4.2.8 High Quality Scaling

Intel Clear Video Technology's high quality scaling utilizes advanced filtering techniques allowing video to be up-scaled or down-scaled to fit any playback window. This includes non-square scaling. In addition to the obvious benefits of traditional video playback, this also allows for the accurate and efficient mixing of differently sized video streams.

The Mobile Intel GMA X3100 core utilizes a 4x4 (polyphase) filter, a 4x4 (bicubic) filter, as well as a 2x2 (bilinear) filter. This allows for playback applications to strike a balance between video quality and performance overhead in specific scenarios.

7.1.4.2.9 Intel® TV Wizard

Intel TV Wizard is a new, independent GUI application that is packaged with the Intel Graphics driver. Currently PC to TV interaction needs adjustments to get a good quality picture on TV. The application is used by end-users to configure their TV display outputs in a pre-defined sequence.

7.1.4.3 Sub-Picture Support

Sub-picture is used for subtitles for movie captions and menus used to provide some visual operation environments.

The Mobile Intel GMA X3100:

- Supports sub-picture by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels.
- Utilizes multiple methods when dealing with sub-pictures.
- Enables the Mobile Intel GMA X3100 to work with all sub-picture formats.

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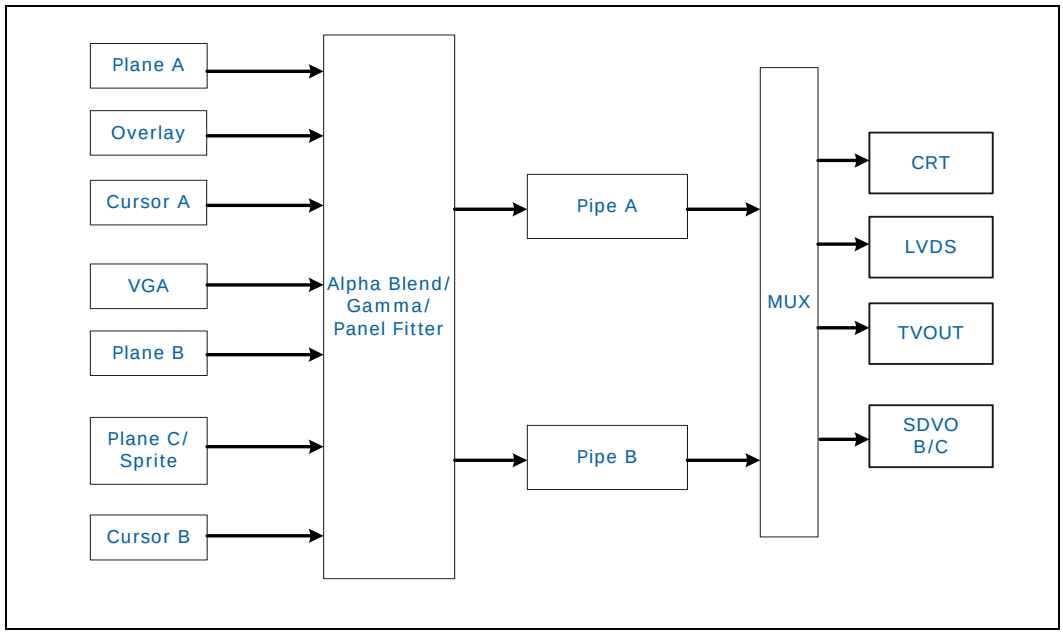
8 Graphics Display Interfaces

The graphics display converts a set of source images or surfaces, combines them and sends them out at the proper timing to an output interface connected to a display device. The data can be converted from one format to another, stretched or shrunk, and color corrected or gamma converted.

Figure 16. Mobile Intel Gx965 Express Chipset Display Block Diagram



8.1 Display Overview

Integrated graphics display on the (G)MCH can be broken down into three components:

- Display Planes
- Display Pipes
- Display Ports

8.2 Display Planes

The (G)MCH contains a variety of planes, such as Plane A and Plane B, Cursor, Overlay, and Sprite. A plane consists of a rectangular-shaped image that has characteristics such as source, size, position, method, and format. These planes attach to source surfaces, which are rectangular areas in memory with a similar set of characteristics. They are also associated with a particular destination pipe.

8.2.1 DDC (Display Data Channel)

DDC is a standard defined by VESA. DDC allows communication between the host system and display. Both configuration and control information can be exchanged allowing Plug and Play systems to be realized. Support for DDC 1 and 2 is implemented. The chipset uses the CRT_DDC_CLK and CRT_DDC_DATA signals to communicate with the analog monitor.

8.2.1.1 Source/Destination Color Keying/ChromaKeying

Overlay source/destination ChromaKeying enables blending of the overlay with the underlying graphics background. Destination color keying/ChromaKeying can be used to handle occluded portions of the overlay window on a pixel by pixel basis that is actually an underlay. Destination ChromaKeying would only be used for YUV pass through to TV. Destination color keying supports a specific color as well as alpha blending.

8.2.1.2 Gamma Correction

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

8.3 Display Pipes

The display consists of two pipes:

- Display Pipe A
- Display Pipe B

A pipe consists of a set of combined planes and a timing generator. The timing generators provide the basic timing information for each of the display pipes. The (G)MCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe.

The Mobile Intel Gx965 Chipset has flexibility to support all display types from both display pipes with enhanced 3 x 3 panel fitter. It also enables support for 7 x 5 scaling for external TV monitors with over-scan control for HDTV displays.

8.3.1 Clock Generator Units (DPLL)

The clock generator units provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25-350 MHz. Accuracy for VESA timing modes is required to be within ± 0.5%.

The DPLL can take a reference frequency from the external reference input (DPLL_REF_CLK / DPLL_REF_CLK#, DPLL_REF_SSCLK / DPLL_REF_SSCLK#), or the TV clock input (TVCLKIN).

8.4 Display Ports

Display Ports is the destination for the display pipe. These are the places where the data finally appears to devices outside the graphics device. The (G)MCH has one dedicated:

- Analog Display Port CRT
- LVDS Display Port
- Analog TV Out
- SDVO (B&C)

Table 14. Display Port Characteristics

Interface Protocol		(Analog) RGB DAC	LVDS	Port B (Digital) SDVO 1.0	Port C (Digital) SDVO 1.0
SIGNALS	HSYNC	Yes Enable/ Polarity	Encoded during blanking codes		
	VSYNC	Yes Enable/ Polarity	Encoded during blanking codes		
	BLANK	No	No	Encoded	Encoded
	STALL	No	No	Yes	Yes
	Field	No	No	No	No
	Display_Enable	No	Yes	Encoded	Encoded
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1			
Pixel Aspect Ratio		Square†	Square		
Voltage		RGB 0.7V p-p	1.2 VDC 300 mV p-p	Scalable 1.x V	
Clock		NA	7x Differential (dual channel) 3.5x Differential (Single channel)		
Max Rate		300 Mpixel	224 MPixel (dual channel) 112 Mpixel (single channel)	200 Mpixel	
Format		Analog RGB	Multiple 18 bpp or 24 bpp Type 1 (single channel only)	RGB 8:8:8 YUV 4:4:4	
Control Bus		DDC1	Optional DDC	GMBUS	
External Device		No	No	TMDS/LVDS Transmitter /TV Encoder	
Connector		VGA/DVI-I		DVI/CVBS/S-Video/Component/ SCART	

8.4.1 Analog Display Port CRT

The analog display port provides an RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT-based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

Table 15. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

8.4.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. Three 8-bit DACs provide the R, G, and B signals to the monitor.

8.4.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internally, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support is included.

8.4.2 LVDS Display Port

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then locked into the registers to prevent unwanted corruption of the values. From that point, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes. These mode changes include VGA to VGA, VGA to HiRes, HiRes to VGA, and HiRes to HiRes. The transmitter can operate in a variety of modes and supports several data formats. The display stream from the display pipe is sent to the LVDS transmitter port at the dot clock frequency, which is determined by the panel timing requirements.

Functionality includes:

- LVDS output runs at a fixed multiple of the dot clock frequency, which is determined by the mode of operation; single or dual channel. The serializer supports 6-bit or 8-bit color and single or dual channel operating modes.
  - — A single channel, depending on configuration and mode, can take 18 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) and output

them on three differential data pair outputs; or 24 bits of RGB plus 3 bits of timing control output on four differential data pair outputs.

— A dual channel interface converts 36 or 48 bits of color information plus the 3 bits of timing control, and outputs it on six or eight sets of differential data outputs, respectively.

- Used in conjunction with the pipe functions of panel scaling and 6- to 8-bit dither.
- Used in conjunction with the panel power sequencing and additional associated functions.

Note: When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not being used. When disabled, individual or sets of pairs will enter a low power state. When the port is disabled all pairs enter a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

8.4.2.1 LVDS Interface Signals

There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each. The phase locked transmit clock is transmitted in parallel with the data being sent out over the data pairs and over the LVDS clock pair.

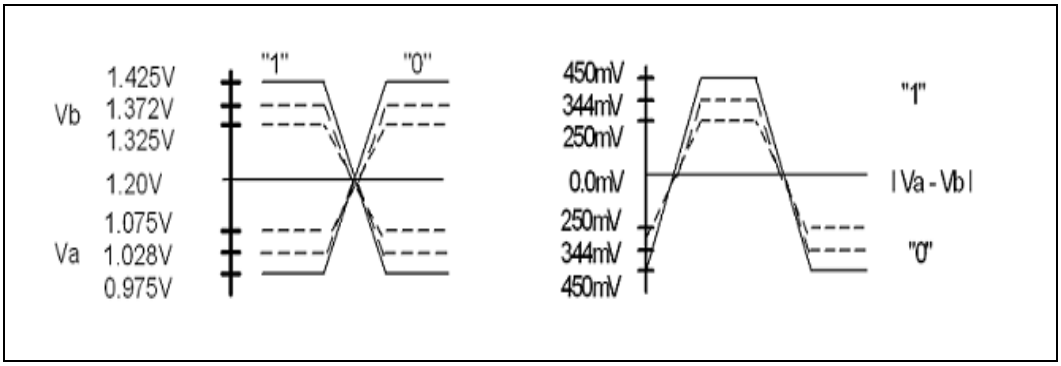
Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, they each operate at the same frequency, each carrying a portion of the data. The maximum pixel rate is increased to 224 MP/s but may be limited to less than that due to restrictions elsewhere in the circuit.

The LVDS Port enable bit enables or disables the entire LVDS interface. When the port is disabled, it is in a low power state. Once the port is enabled, individual driver pairs are disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0's output.

8.4.2.2 LVDS Data Pairs and Clock Pairs

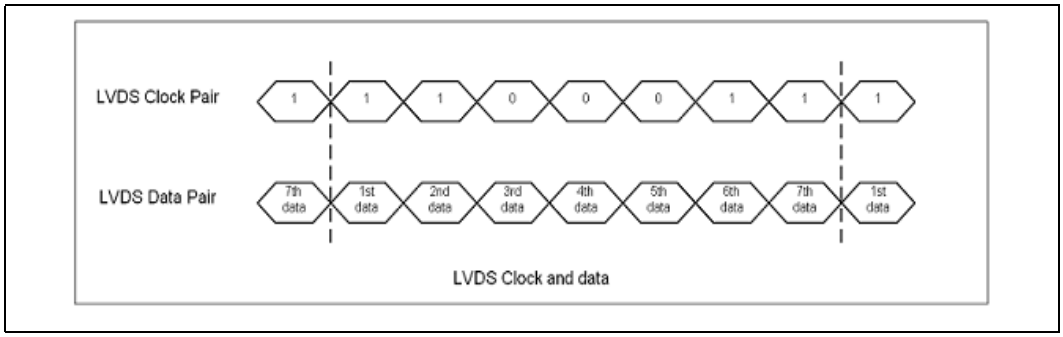
The LVDS data and clock pairs are identical buffers and differ only in the use defined for that pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. The pixel bus data to serial data mapping options are specified elsewhere. A single or dual clock pair is used to transfer clocking information to the LVDS receiver. A serial pattern of 1100011 represents one cycle of the clock. Figure 17 shows a pair of LVDS signals and swing voltage.

Figure 17. LVDS Signals and Swing Voltage



1's and 0's are represented by the differential voltage between the pair of signals.

Figure 18. LVDS Clock and Data Relationship



8.4.2.3 LVDS Pair States

The LVDS pairs can be put into one of five states:

- Powered down tri-state. When in powered down state, the circuit tri-states on both the output pins for the entire channel.
- Powered down 0 V. When in powered down state, the circuit enters a low power state and drives out 0 V.
- Common mode. The common mode tri-state is both pins of the pair set to the common mode voltage.
- Send zeros. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data, regardless of what the actual data is with the clock lines and timing signals sending the normal clock and timing data.
- Active state. When in the active state several data formats are supported.

8.4.2.4 Single Channel versus Dual Channel Mode

In the single channel mode, only Channel A is used. In the dual channel mode, both Channel A and Channel B pins are used concurrently to drive one LVDS display.

In single channel mode, Channel A is capable of supporting 24-bpp display panels of Type 1 only (compatible with VESA LVDS color mapping). In dual channel mode, Channel A and B are capable of supporting 24-bpp panels of Type 1.

Dual channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel is used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel is sent out Channel A. All horizontal timings for active, sync, and blank are limited to be on two pixel boundaries in the two channel modes.

8.4.2.5 LVDS Channel Skew

When in dual channel mode, the two channels must meet the panel requirements with respect to the inter channel skew.

8.4.2.6 LVDS PLL

The Display PLL is used to synthesize the clocks that control transmission of the data across the LVDS interface. The three operations that are controlled are the pixel rate, the load rate, and the IO shift rate. These are synchronized to each other and have specific ratios based on single channel or dual channel mode. If the pixel clock is

considered the 1x rate, a 7x or 3.5x speeds the IO_shift clock needed for the high speed serial outputs setting the data rate of the transmitters. The load clock will have either a 1x or 0.5x ratio to the pixel clock.

8.4.2.7 Panel Power Sequencing

In order to meet the panel power timing specification requirements two signals, LFP_VDD_EN and LFP_BKLT_EN, are provided to control the timing sequencing function of the panel and the backlight power supplies.

A defined power sequence is recommended when enabling or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met.

Figure 19. Panel Power Sequencing

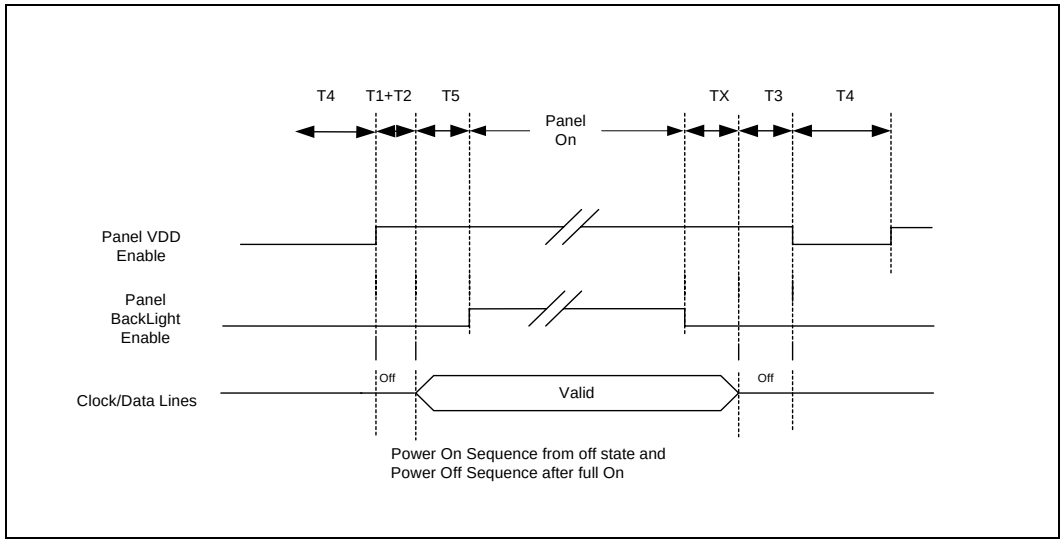


Table 16. Panel Power Sequencing Timing Parameters

Panel Power Sequence Timing Parameters			Min	Max	Name	Units
Spec Name	From	To				
Vdd On	0.1 Vdd	0.9 Vdd	0	10	T1	ms
LVDS Active	Vdd Stable On	LVDS Active	0	50	T2	ms
Backlight	LVDS Active	Backlight on	200		T5	ms
Backlight State	Backlight Off	LVDS off	X	X	TX	ms
LVDS State	LVDS Off	Start power off	0	50	T3	ms
Power cycle Delay	Power Off	Power On Sequence Start	400	0	T4	ms

8.4.3 SDVO Digital Display Port

8.4.3.1 SDVO

The (G)MCH utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings. SDVO ports can support a variety of display types:

- LVDS
- DVI
- Analog TV-Out
- Analog CRT
- HDMI
- External CE type devices

8.4.3.2 SDVO LVDS

The (G)MCH may use the SDVO port to drive an LVDS transmitter. Flat panel is a fixed resolution display. The (G)MCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities.

The (G)MCH will provide unscaled mode where the display is centered on the panel. Scaling in the LVDS transmitter through the SDVO stall input pair is also supported.

8.4.3.3 SDVO DVI

DVI, a 3.3-V flat panel interface standard, is a prime candidate for SDVO. The (G)MCH provides unscaled mode where the display is centered on the panel. Monitor Hot Plug functionality is supported for DVI devices.

8.4.3.4 SDVO Analog TV-Out

The SDVO port supports both standard and high-definition TV displays in a variety of formats. The SDVO port generates the proper blank and sync timing, but the external encoder is responsible for generation of the proper format signal and output timings.

(G)MCH will support NTSC/PAL standard definition formats. The (G)MCH will generate the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal.

The TV-out interface on (G)MCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVCLKIN[+/-] that the (G)MCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

8.4.3.5 SDVO Analog CRT

The chipset supports SDVO Analog CRT which has similar characteristics as the Integrated Analog CRT (24 bpp, 225-MHz Pixel clock).

8.4.3.6 SDVO HDMI

HDMI is a 3.3-V interface that uses TMDS encoding, and requires an active level shifter to get 3.3-V DC coupling. The (G)MCH supports the mandatory features of HDMI Specification 1.3. When combined with a HDMI-compliant external device and connector, the external HDMI device can support standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. The (G)MCH has a high speed interface to a digital display (for example, flat panel or digital TV).

8.4.3.7 External CE Type Devices

8.4.3.7.1 TMDS

The (G)MCH is compliant with DVI Specification 1.0. DVI requires an SDVO device. The (G)MCH supports panel fitting in the transmitter, receiver, or an external device.

8.4.3.7.2 Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing is generated with pixel granularity to allow more overscan ratios to be supported.

8.4.3.7.3 Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps.

8.4.3.7.4 Analog Content Protection

Analog content protection may be provided through the external encoder.

8.4.3.7.5 Connectors

Target TV connector support includes the CVBS, S-Video, Analog Component (YPbPr), and SCART connectors. The external TV encoder will determine the method of support.

8.4.3.7.6 Control Bus

The SDVO port defines a two-wire communication path between the SDVO device(s) and (G)MCH. Traffic destined for the PROM or DDC will travel across the Control bus, and will then require the SDVO device to act as a switch and direct traffic from the Control bus to the appropriate receiver. Additionally, the Control bus is able to operate at up to 1 MHz.

8.5 Multiple Display Configurations

(G)MCH can support up to two different images on different display devices because it has several display ports available for its two pipes. Parameters include:

- Timings and resolutions for these two images may be different.
- The (G)MCH can not operate in parallel with an external PCI Express graphics device.
- The (G)MCH can work in conjunction with a PCI graphics adapter.

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9 Power Management

9.1 Overview

- ACPI 3.0 Support
  - — Global states: G0, G1, G2, G3
  - — System states: S0, S3Cold, S4, S5
  - — Processor states: C0, C1, C1E, C2, C2E, C3, C4, C4E, Intel Enhanced Deeper Sleep state
  - — Integrated Graphics Display Device states: D0, D1, D2, D3
  - — Integrated Graphics Display Adapter states: D0, D3
- (G)MCH Interface Power Management State Support
  - — PCI Express Link states: L0, L0s, L1, L2/ L3 ready, L3
  - — DMI states: L0, L0s, L1, L2/ L3 ready, L3
  - — System Memory: Power up, Pre-charge Power down, Active Power down, Self-Refresh
  - — SDVO: D0, D1, D2, D3
- Intel Management Engine Power Management State Support
  - — Intel Management Engine states: M0, M1, Moff
- (G)MCH State Combinations
- Additional Power Management Features:
  - — Front Side Bus Interface
    - —Intel Dynamic Front Side Bus Frequency Switching
    - —H_DPWR#
    - —H_CPUSLP#
  - — PCI Express Graphics / DMI interfaces
    - —CLKREQ#
  - — System Memory Interface
    - —Intel RMPM
    - —Disabling Unused System Memory Outputs
    - —Dynamic Power Down of Memory
  - — Integrated Graphics
    - —Intel DPST 3.0
    - —Intel S2DDT
    - —Dynamic Display Power Optimization (D^2PO) Panel Support
    - —Intel Automatic Display Brightness
    - —Intel Display Refresh Rate Switching

9.2 ACPI 3.0 Support

9.2.1 System States

State	Description
G0/S0	Full On
G1/S1	Not supported
G1/S1	Not supported
G1/S2	Not supported
G1/S3-Cold	Suspend to RAM (STR). Context saved to memory (S3-Hot is not supported by Mobile Intel® Gx965/PM965 Express Chipset)
G1/S4	Suspend to Disk (STD). All power lost (except wakeup on ICH)
G2/S5	Soft off. All power lost (except wakeup on ICH). Total reboot
G3	Mechanical off. All power (AC and battery) removed from system

9.2.2 Processor States

State	Description
C0	Full On
C1/C1E	Auto Halt
C2/C2E	Stop Grant. Clock stopped to processor core
C3	Deep Sleep. Clock to processor stopped
C4/C4E/Intel® Enhanced Deeper Sleep	Deeper Sleep. Same as C3 with reduced voltage on the processor

9.2.3 Integrated Graphics Display Device States

State	Description
D0	Display active
D1	Low power state, low latency recovery, standby display
D2	Suspend display
D3	Power off display

9.2.4 Integrated Graphics Display Adapter States

State	Description
D0	Full on, display active
D3	Display off

9.3 (G)MCH Interface Power Management State Support

9.3.1 PCI Express Link States

State	Description
L0	Full on—Active transfer state
L0s	First Active Power Management low power state—Low exit latency
L1	Lowest Active Power Management—Longer exit latency
L2/L3 Ready	Lower link state with power applied—Long exit latency
L3	Lowest power state (power off)—Longest exit latency

9.3.1.1 Dynamic Power Management on I/O

- Active power management support using L0, L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

9.3.2 DMI States

Same as PCI Express Link states.

9.3.3 System Memory States

State	Description
Power up	CKE asserted. Active mode
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed
Active Power down	CKE deasserted (not self-refresh) with minimum one bank active
Self-Refresh	CKE deasserted using device self-refresh

9.3.4 SDVO

State	Description
D0	Display Active
D1	Low power state, low latency recovery, Standby display
D2	Suspend display
D3	Power off display

9.3.4.1 Dynamic Power Management on I/O

- Disabling of SDVO places all SDVO logic and I/O in minimum power state.

9.4 Intel Management Engine Power Management State Support

State	Description
M0	Intel® Management Engine—Full On
M1	Only Intel Management Engine Clocks/Power Rails are enabled in M1-state
Moff	Intel Management Engine—Full Off

9.5 (G)MCH State Combinations

(G)MCH supports the state combinations listed in the Table 17 and Table 18.

Table 17. G, S and C State Combinations

Global (G) State	Sleep (S) State	CPU (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto Halt
G0	S0	C2/C2E	Stop Grant	On	Stop Grant
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C4/C4E/Intel® Enhanced Deeper Sleep state	Deeper Sleep	On	Deep Sleep with lower processor voltage than C3
G1	S3	power off		Off, except RTC	Suspend to RAM
G1	S4	power off		Off, except RTC	Suspend to Disk
G2	S5	power off		Off, except RTC	Soft Off
G3	NA	power off		Power Off	Hard Off

Table 18. D, S, and C State Combinations

Graphics Adapter (D) State	Sleep (S) State	CPU (C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1/C1E	Auto-Halt, Displaying
D0	S0	C2/C2E	Stop Grant, Displaying
D0	S0	C3	Deep Sleep, Displaying
D0	S0	C4/C4E/Intel® Enhanced Deeper Sleep state	Deeper Sleep, Displaying
D3	S0	Any	Not Displaying
D3	S3	---	Not Displaying (G)MCH may power off
D3	S4	---	Not Displaying Suspend to disk

9.6 Additional Power Management Features

9.6.1 Front Side Bus Interface

9.6.1.1 Intel Dynamic Front Side Bus Frequency Switching

Intel Dynamic Front Side Bus Frequency Switching is a feature where the processor and chipset work together in order to allow a virtual change in the bus clock frequency, thereby reducing frequency by up to half. Reduced frequency allows the processor core voltage to be lowered, thereby consuming less power while still active.This state is exposed as a processor performance state (P-state) and is also known as super LFM.

9.6.1.2 H_DPWR#

H_DPWR# signal disables processor sense amps when no read return data is pending.

9.6.1.3 CPU Sleep (H_CPUSLP#) Signal Definition

- The processor's sleep signal (SLP#) reduces power in the processor by gating off unused clocks. This signal can be driven only by the (G)MCH's H_CPUSLP# signal.
- The (G)MCH host interface controller will ensure that no transactions are initiated on the FSB without having first met the required timing from the SLP# deassertion to the assertion of BPRI#.
- (G)MCH will control H_CPUSLP# and enforce the configured timing rules associated with this. This allows the (G)MCH to enforce the timing of the SLP# deassertion to BPRI# assertion during C3 to C2 or C3 to C0 transitions.

9.6.2 PCI Express Graphics/DMI interfaces

9.6.2.1 CLKREQ# - Mode of Operation

The CLKREQ# signal is driven by the (G)MCH to control the PCI Express clock to the external graphics and the DMI clock. When both the DMI and PCI Express links (if supported) are in L1, with CPU in C4, C4E or Intel Enhanced Deeper Sleep state, the (G)MCH deasserts CLKREQ# to the clock chip, allowing it to gate the GCLK differential clock pair to the (G)MCH, in turn disabling the PCI Express and DMI clocks inside the (G)MCH. For the (G)MCH to support CLKREQ# functionality, ASPM must enabled on the platform.

9.6.3 System Memory Interface

The main memory is power managed during normal operation and in low power ACPI Cx states.

9.6.3.1 Intel Rapid Memory Power Management (Intel RMPM)

This technique is to allow all rows of memory to be self-refreshed, with all on chip DLLs off and all SO-DIMM clocks off as long as possible during C3 and above, to reduce power consumption. This is accomplished by adding a mechanism in the memory controller to allow for self-refresh entry and exit during C3 and above and allow for single-row self refresh exit during C3 and above.

Intel Rapid Memory Power Management conditionally places memory into self-refresh based on C state, PCI Express link states, and graphics/display activity. Though the dependencies on this behavior are configurable, the target usage is shown in the table below.

Table 19. Targeted Memory State Conditions

Mode	Memory State with Integrated Graphics	Memory State with External Graphics
C0, C1, C2	Dynamic memory rank power down based on idle conditions	Dynamic memory rank power down based on idle conditions
C3, C4, Intel® Enhanced Deeper Sleep	Dynamic memory rank power down based on idle conditions If graphics engine is idle, no display requests, and permitted display configuration, then enter self-refresh. Otherwise use dynamic memory rank power down based on idle conditions	Dynamic memory rank power down based on idle conditions If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power down based on idle conditions
S3	Self Refresh Mode	Self Refresh Mode
S4, S5	Memory power down (contents lost)	Memory power down (contents lost)

9.6.3.2 Disabling Unused System Memory Outputs

Any System Memory (SM) interface signals that go to a SO-DIMM connector in which they are not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) are tri-stated.

The benefits of disabling unused SM signals are:

- Reduce power consumption.
- Reduce possible overshoot/undershoot signal quality issues seen by the (G)MCH I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated (as determined by the DRAM Rank Boundary Register values) then the corresponding chip select and SCKE signals will not be driven.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

9.6.3.3 Dynamic Power Down of Memory

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. If the pages for a rank have all been closed at the time of power down, then the device will enter the precharge power-down state. If pages remain open at the time of power-down the devices will enter the active power-down state.

9.6.4 Integrated Graphics

9.6.4.1 Intel Display Power Saving Technology 3.0

When enabled, the Intel DPST feature dynamically reduces the power (up to 25%) of the panel backlight based on the brightness distribution in each video frame being displayed.

9.6.4.2 Intel Smart 2D Display Technology

Intel S2DDT reduces memory reads, thereby reducing read data power consumption. Intel S2DDT improves most CPU benchmarks due to reduced CPU to memory read latency. The Intel S2DDT engine periodically compresses the front frame buffer data and stores it in a compressed frame buffer. In the upcoming frames, the display engine reads the compressed lines from the compressed frame buffer instead of reading uncompressed lines from the original frame buffer. Lines that were not compressed or lines that were modified since the last compression are displayed from the uncompressed (original) frame buffer.

9.6.4.3 Dynamic Display Power Optimization* (D^2PO) Panel Support

D²PO* is a liquid crystal drive technology developed by Toshiba Matsushita Display Technology Co., Ltd. (TMD) that reduces the power consumption of the LCD for notebook PCs. Intel's implementation of D²PO Panel Support feature employs this LCD technology dynamically to achieve significant power savings while maintaining a high quality visual experience.

9.6.4.4 Intel Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This technique provides both potential power savings and usability benefit by automatically decreasing the backlight in dark environments and increasing the backlight in bright environments.

9.6.4.5 Intel Display Refresh Rate Switching

Intel Display Refresh Rate Switching is a method of saving power by automatically switching the LCD refresh rate. This method switches between two display timings stored in either the LCD EDID Detailed Timing Descriptors or in the Video BIOS Table. The refresh rate switching will occur during an AC/DC event or when the system boots or resumes from S3/S4 in either AC or battery mode.

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10 Absolute Maximum Ratings

Table 20 specifies the (G)MCH's absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

Caution: At conditions outside functional operation condition limits neither functionality nor long-term reliability can be expected.

Caution: Although the (G)MCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 20. Absolute Maximum Ratings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes[1]
T_{die}	Die temperature under bias	0	105	°C	1
$T_{storage}$	Storage temperature	-55	150	°C	2,3
(G)MCH					
V_{CC}	1.05-V core supply voltage with respect to V_{SS}	-0.3	1.155	V	
V_{CC_AXG}	1.05-V graphics voltage with respect to V_{SS}	-0.3	1.375	V	
V_{CC_AXD}	1.25-V DDR2 IO voltage with respect to V_{SS}	-0.3	1.375	V	4
V_{CC_AXM}	1.05 Manageability Engine voltage with respect to V_{SS}	-0.3	1.155	V	
Host Interface					
V_{TT} (FSB V_{CCP})	1.05-V AGTL+ buffer DC input voltage with respect to V_{SS}	-0.3	1.32	V	
V_{CC_AXF}	1.25-V DC input voltage for AGTL+ buffer logic with respect to V_{SS}	-0.3	1.375	V	
DDR2 Interface (533 MTs/ /667 MTs)					
V_{CC_SM}	1.8-V DDR2 supply voltage with respect to V_{SS}	-0.3	2.1	V	
$V_{CC\_SM\_CK}$	1.8-V DDR2 clock IO voltage with respect to V_{SS}	-0.3	2.1	V	
V_{CCA_SM}	1.25-V DDR2 voltage connects to IO logic and DLLs with respect to V_{SS}	-0.3	1.375	V	
$V_{CCA\_SM\_CK}$	1.25-V DDR2 voltage for clock module to avoid noise with respect to V_{SS}.	-0.3	1.375	V	

Table 20. Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes[1]
DMI /PCI Express Graphics/SDVO Interface					
V_{CC_PEG}	1.05-V PCI Express supply voltage with respect to V_{SS}	-0.3	1.375	V	
V_{CC_DMI}	1.25-V DMI terminal supply voltage with respect to V_{SS}	-0.3	1.375	V	
$V_{CCR\_RX\_DMI}$	1.05-V RX and IO logic voltage for DMI	-0.3	1.375	V	
$V_{CCA\_PEG\_BG}$	3.3-V analog band gap voltage with respect to $V_{SSA\_PEG\_BG}$	-0.3	3.63	V	
Controller LINK					
					5
CRT DAC Interface (8 bit DAC)					
$V_{CCA\_CRT\_DAC}$	3.3-V DAC IO supply voltage	-0.3	3.63	V	
V_{CC_SYNC}	3.3-V CRT sync supply voltage	-0.3	3.63	V	
V_{CCD_QCRT}	1.5-V CRT quiet digital voltage	-0.3	1.65	V	
V_{CCD_CRT}	1.5-V CRT level shifter supply	-0.3	1.65	V	
HV CMOS Interface					
V_{CC_HV}	3.3-V supply voltage with respect to V_{SS}	-0.3	3.63	V	
TV OUT Interface (10 bit DAC)					
V_{CCD_TVDAC}	1.5-V TV supply	-0.3	1.65	V	
$V_{CCA\_TVA\_DAC}$ $V_{CCA\_TVB\_DAC}$ $V_{CCA\_TVC\_DAC}$	3.3-V TV analog supply	-0.3	3.63	V	
$V_{CCA\_DAC\_BG}$	3.3-V TV DAC band gap voltage	-0.3	3.63	V	
V_{CCD_QTVDAC}	1.5-V quiet supply	-0.3	1.65	V	
LVDS Interface					
V_{CCD_LVDS}	1.8-V LVDS digital power supply	-0.3	1.98	V	
$V_{CC\_TX\_LVDS}$	1.8-V LVDS data/clock transmitter supply voltage with respect to V_{SS}	-0.3	1.98	V	
V_{CCA_LVDS}	1.8-V LVDS analog supply voltage with respect to V_{SS}	-0.3	1.98	V	
PLL Analog Power Supplies					
V_{CCA_HPLL}, V_{CCD_HPLL}, V_{CCA_MPLL}, $V_{CCA\_PEG\_PLL}$, $V_{CCD\_PEG\_PLL}$, V_{CCA_DPLLA}, V_{CCA_DPLLB}	1.25-V power supply for various PLL	-0.3	1.375	V	

NOTES:
1. Functionality is not guaranteed for parts that exceed Tdie temperature above 105ºC. Tdie is measured at top center of the package. Full performance may be affected if the on-die thermal sensor is enabled.
2. Possible damage to the (G)MCH may occur if the (G)MCH storage temperature exceeds 150ºC. Intel does not guarantee functionality for parts that have exceeded temperatures above 150ºC due to spec violation.
3. Storage temperature is applicable to storage conditions only. In this scenario, the device must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging.
4. Relevant for Controller Link as well.
5. See V_{CC_AXD}

10.1 Power Characteristics

Table 21. Mobile Intel 965 Express Chipset Family Thermal Design Power Numbers

SKU	TDP	Unit	Notes
Mobile Intel® GM965/GME965 Express Chipset (render clock 500 MHz)	13.5	W	1
Mobile Intel GM965/GME965 Express Chipset (render clock 400 MHz)	12		
Mobile Intel GM965/GME965 Express Chipset (mini-note)	10.5		
Mobile Intel GM965/GME965 Express Chipset (sub-note)	9.5		
Mobile Intel® PM965 Express Chipset	8		
Mobile Intel® GL960/GLE960 Express Chipset	<13.5		

Table 22. Power Characteristics (Sheet 1 of 3)

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
T_{die}	Die temperature under bias		0		105	°C	1
$T_{storage}$	Storage temperature		-55		150	°C	2
(G)MCH							
I_{VCC}	1.05-V core supply current (external GFX)				1310.	mA	3, 5
I_{VCC}	1.05-V core supply current (integrated GFX)				1572.62	mA	3, 5
I_{VCC_AXG}	1.05-V graphics core supply current				7700	mA	3, 5
I_{VCC_AXM}	1.05-V Manageability Engine supply current				540	mA	

Table 22. Power Characteristics (Sheet 2 of 3)

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
Host Interface							
I_{VTT} FSB at 533 MHz	V_{TT} supply current (1.05 V)				700	mA	
I_{VTT} FSB at 667 MHz	V_{TT} supply current (1.05 V)				770	mA	
I_{VTT} FSB at 800 MHz	V_{TT} supply current (1.05 V)				850	mA	
DMI /PCI Express Graphics/SDVO Interface							
I_{VCC_PEG}	1.05-V PCI Express supply voltage with respect to V_{SS}				1310	mA	3, 4, 8
I_{VCC_DMI}	1.25-V DMI termination supply voltage with respect to V_{SS}				100	mA	
$I_{VCCR\_RX\_DMI}$	1.05-V IO logic voltage for DMI				260	mA	
$I_{VCCA\_PEG\_BG}$	3.3-V analog band gap voltage with respect to $V_{SSA\_PEG\_BG}$				400	µA	
Controller Link							
I_{VCC_AXM}							9
CRT DAC Interface (8 bit DAC)							
$I_{VCCA\_CRT\_DAC}$	3.3-V DAC IO supply voltage				70	mA	3, 8
I_{VCC_SYNC}	3.3-V CRT sync supply voltage				10	mA	3, 8
I_{VCCD_QCRT}	1.5-V CRT quiet digital voltage				0.5	mA	
I_{VCCD_CRT}	1.5-V CRT digital power supply				60	mA	
HV CMOS Interface							
I_{VCC_HV}	3.3-V supply voltage with respect to V_{SS}				100	mA	3
TV OUT Interface (10 bit DAC)							
I_{VCCD_TVDAC}	1.5-V TV supply				60	mA	3, 8
$I_{VCCA\_TVA\_DAC}$ $I_{VCCA\_TVB\_DAC}$ $I_{VCCA\_TVC\_DAC}$	3.3-V TV analog supply				40 40 40	mA	3, 8
$I_{VCCA\_DAC\_BG}$	3.3-V TV analog supply				5	mA	3
I_{VCCD_QTVDAC}	1.5-V quiet supply				0.5	mA	
LVDS Interface							
I_{VCCD_LVDS}	1.8-V LVDS digital power supply				150	mA	3
$I_{VCC\_TX\_LVDS}$	1.8-V LVDS data/clock transmitter supply voltage with respect to V_{SS}				100	mA	

Table 22. Power Characteristics (Sheet 3 of 3)

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
I_{VCCA_LVDS}	1.8-V LVDS analog supply voltage with respect to V_{SS}				10	mA	3
PLL Analog Power Supplies							
I_{VCCA_HPLL}	Host PLL supply current	VCCA_HPLL			50	mA	3
I_{VCCD_HPLL}	HPLL supply current for digital interface	VCCD_HPLL			250	mA	3
I_{VCCA_DPLLA} I_{VCCA_DPLLB}	Display PLLA supply current Display PLLB supply current	VCCA_DPLLA VCCA_DPLLB			100	mA	3
I_{VCCA_MPLL}	Memory PLL supply current	VCCA_MPLL			150	mA	3
$I_{VCCA\_PEG\_PLL}$ $I_{VCCD\_PEG\_PLL}$	PEG PLL supply current	VCCA_PEG_PLL VCCD_PEG_PLL			90	mA	3

NOTES:
1. This specification is the thermal design power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to concoct higher power synthetic workloads that write but never read. Under realistic read/write conditions, this higher power workload can only be transient and is accounted in the Icc (maximum) specification. Tdie is measured at the top center of the package.
2. These current levels can happen simultaneously, and can be summed into one supply.
3. Estimate is only for maximum current coming through the chipset's supply balls.
4. Rail includes PLL current.
5. Includes worst-case leakage.
6. Calculated for highest stretch goal frequencies.
7. I_{CCMAX} is determined on a per-interface basis, and all cannot happen simultaneously.
8. I_{CCMAX} number includes maximum current for all signal names listed in the table.
9. See I_{VCC_AXD}.

Table 23. DDR2 (533 MTs/667 MTs) Power Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{VCCSM}	DDR2 System Memory Interface (1.8 V, 533 MTs) supply current		1 Channel 2 Channel	1395 2700	mA	
I_{VCCSM}	DDR2 System Memory Interface (1.8 V, 667 MTs) supply current		1 Channel 2 Channel	1700 3300	mA	
I_{VCCSM_CK}	DDR2 System Memory Interface Clock supply current			200	mA	
I_{VCCA_SM} (533MT/s)	1.25-V DDR2 IO logic and DLLs supply current			550	mA	
I_{VCCA_SM} (667MT/s)	1.25-V DDR2 IO logic and DLLs supply current			735	mA	
$I_{VCCA\_SM\_CK}$	1.25-V DDR2 supply current for clock module.			35	mA	
I_{SUS_VCCSM}	DDR2 System Memory interface (1.8 V) standby supply current			5	mA	1

Table 23. DDR2 (533 MTs/667 MTs) Power Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90-V) supply current			20	µA	
I_{SUS_SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90-V) standby supply current			10	µA	1
I_{TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8-V) supply current			30	mA	
I_{SUS_TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8-V) standby supply current			0	mA	

NOTES:
1. Standby in Table 23 refers to system memory in Self Refresh during S3 (STR).

Table 24. V_{CC} Auxiliary Rail Power Characteristics

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{VCC_AXD}	Supply current for HSIO			515	mA	1,2
I_{VCC_AXF}	Supply current FSB IO			495	mA	1

NOTES:
1. Calculated for highest frequency of operation.
2. Relevant for Controller Link as well.

10.2 Thermal Characteristics

The (G)MCH is designed for operation at die temperatures between 0°C and 105°C. The thermal resistance of the package is given in the following table.

Table 25. Mobile Intel 965 Express Chipset Family Package Thermal Resistance

Parameter	Airflow Velocity in Meters/Second	
	0 m/s (0 LFM)	1 m/s (200 LFM)
Ψ_{jt} (°C/Watt)[1]	23.5 C/W	18.3 C/W
Θ_{ja} (°C/Watt)[1]	0.5 C/W	0.9 C/W

NOTES:
1. Estimate.

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11 Thermal Management

System level thermal management requires two solutions:

1. Robust Thermal Solution Design: The system's thermal solution should be capable of dissipating the platform's thermal design power while keeping all components below the relevant Tdie_max under the intended usage conditions. Such conditions include ambient air temperature and available airflow inside the laptop.
2. Thermal Failsafe Protection Assistance: As a backup to the thermal solution, the system design should provide additional thermal protection for the components. The failsafe assistance mechanism reduces the risk of damage by excessive thermal stress in situations where the thermal solution is inadequate or has failed.

Details on implementing these solutions are provided in the following sections.

11.1 Internal Thermal Sensors

The (G)MCH incorporates two on-die thermal sensors for thermal management. The thermal sensors may be programmed to cause hardware throttling and/or software interrupts. Hardware throttling includes render and main memory programmable throttling thresholds. Sensor trip points may also be programmed to generate interrupts or integrated graphics interrupt. Table 26 shows the internal thermal sensor trip points, which are listed in the order of increasing temperature.

Table 26. Trip Points

Trip Point	Description
Aux0, 1, 2, 3 Temperature Trip Points	May be set dynamically and provide an interrupt to ACPI (or other software) when crossed in either direction. Do not automatically cause any hardware throttling but may be used by software to trigger interrupts. Should be programmed for software and firmware control via interrupts.
Hot	Set at the temperature at which the MCH must start throttling. It may enable (G)MCH throttling when the temperature is exceeded. May provide an interrupt to ACPI (or other software) when it is crossed in either direction. Software could optionally set this as an interrupt when the temperature exceeds this level setting. Should be set to throttle (G)MCH to avoid maximum Tj of 110°C.
Catastrophic	Set at the temperature at which the (G)MCH must be shut down immediately without any software support. The catastrophic trip point may be programmed to generate an interrupt, enable throttling, or immediately shut down the system (via Halt, or via THERMTRIP# assertion). Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register to select what type of interrupt is generated. Crossing a trip point is implemented as edge detection, used to trigger the interrupts. Either edge (i.e., crossing the trip point in either direction) generates the interrupt. Should be set to halt operation to avoid maximum Tj of 130°C.

NOTE: Contact your Intel representative for recommended Trip Point programming. Thermal sensors are not located in hotspot of (G)MCH. Thermal sensors may be up to 4°C lower than maximum Tj of (G)MCH. Trip Points should be set to account for temperature offset between thermal sensors and maximum Tj hotspot and thermal sensor accuracy.

11.1.1 Thermal Sensor Accuracy

- Thermal sensor accuracy for (G)MCH is ±8 °C from approximately +80°C to Tj-max of 110°C.
- Temperature reading accuracy from Thermal sensor will degrade further with junction temperatures below +80°C.
- Temperature readings from thermal sensor may not be available below +40°C.
- (G)MCH may not operate above Tj-max of +110°C.

Note: Software may program the Tcat, Thot, and Taux trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low) temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.

11.1.2 Sample Programming Model

Intel reference and driver code do not use the thermal sensor interrupts.

11.1.2.1 Setting Trip Point for Hot Temperature and Generating an SERR Interrupt

- Program the Thermal Hot Temperature Setting Register (TSTTPA1.HTPS or TSTTPA2.HTPS).
- In Thermal Sensor Control Register (TSC1 or TSC2), set the thermal sensor enable bit (TSE), and the hysteresis value (if applicable).
- In Thermal Error Command Register (TERRCMD), set the SERR on Hot Thermal Sensor Event (bit 4).
- Program the global thermal interrupt enabling registers.

11.1.2.2 Temperature Rising above the Hot Trip Point

- The TIS [Hot Thermal Sensor Interrupt Event] is set when SERR interrupt is generated.
- Clear this bit of the TIS register to allow subsequent interrupts of this type to get registered.
- Clear the global thermal sensor event bit in the Error Status register.
- In thermal sensor status register (TSS), the Hot Trip indicator (HTI) bit is set if this condition is still valid by the time the software gets to read the register.

11.1.2.3 Determining the Current Temperature as Indicated by the Thermometer

- In the Thermal Sensor Control register (TSC1) set the thermal sensor enable bit (TSE) and the hysteresis value (if applicable).
- Read the value in the Thermometer Reading register (TR). Allow enough time for the entire thermometer sequence to complete (less than 1.3 msec = 512 * 256 / 100 MHz for hraw clock of 100 MHz) in 512 clock mode. Reading is not valid unless TSS [Thermometer Output Valid] = 1.

11.1.3 Hysteresis Operation

- Hysteresis provides a small amount of positive feedback to the thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point.
- The digital hysteresis offset is programmable to be 0,1, 2…15, which corresponds to an offset in the range of approximately 0 to 7°C.

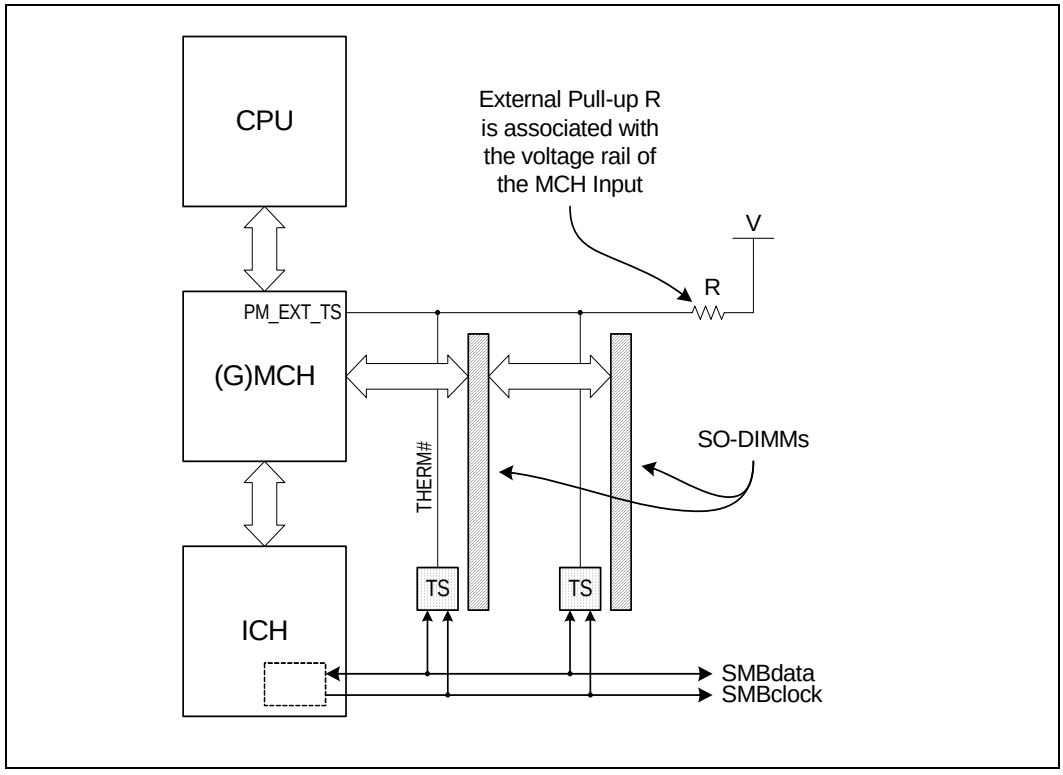
11.2 External Thermal Sensor Interface

Customers have the ability to determine the settings for platform throttling via external thermal sensors.

These external thermal sensors can be enabled to measure temperature of external components, such as memory. Multiple thermal sensors can also be wired together, which allows thermal sensing from multiple components that are separate; that is, two memory SO-DIMMs. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the over-temp through the serial interface. However, since the SO-DIMM's are located on the same Memory Bus Data lines, any (G)MCH-based Read Throttle applies equally.

Note: The use of external sensors that include an internal pull-up resistor on the open-drain thermal trip output is discouraged; however, it may be possible, depending on the size of the pull up and the voltage of the thermal sensor.

Figure 20. Platform External Thermal Sensor



11.3 Thermal Throttling Options

With the internal and external thermal sensors now enabled, the (G)MCH has two independent mechanisms that cause system memory throttling.

- (G)MCH Thermal Management: This is to ensure that the (G)MCH is operating within thermal limits. The mechanism can be initiated by a thermal sensor (internal) trip or by virtual thermal sensor bandwidth measurement exceeding a programmed threshold via a weighted input averaging filter.
- DRAM Thermal Management ensures that the DRAM chips are operating within thermal limits. The (G)MCH can control the amount of (G)MCH initiated bandwidth per rank to a programmable limit via a weighted input averaging filter.

11.4 THERMTRIP# Operation

Assertion of the (G)MCH's THERMTRIP# (Thermal Trip) indicates that its junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the (G)MCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the core junction temperature. Once activated, THERMTRIP# remains latched until RSTIN# is asserted.

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12 DC Characteristics

See Section 2 for signal type and corresponding buffer description.

Table 27. Signal Groups (Sheet 1 of 4)

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	I/O AGTL+	H_ADS#, H_BNR#, H_BREQ#,H_DBSY#, H_DRDY#, H_DINV#[3:0], H_A#[35:3], H_ADSTB#[1:0], H_D#[63:0],H_DSTBP#[3:0], H_DPWR#, H_DSTBN#[3:0], H_HIT#, H_HITM#, H_REQ#[4:0]	
(b)	O AGTL+	H_BPRI#, H_CPURST#, H_DEFER#, H_TRDY#, H_RS#[2:0], THERMTRIP#	
(c)	O LVCMOS	H_CPUSLP	
(d)	I AGTL+	H_LOCK#	
(e)	I A	H_AVREF, H_DVREF, H_SWING	
	I/O A	H_RCOMP, H_SCOMP, H_SCOMP#	
Serial DVO or PCI-Express Graphics Interface Signal Groups			
(f)	I PCI Express*	**PCI-E GFX Interface:** PEG_RX[15:0], PEG_RX#[15:0] **SDVO Interface:** SDVO_TVCLKIN#, SDVO_TVCLKIN, SDVO_INT, SDVO_INT#, SDVO_FLD_STALL#, SDVO_FLD_STALL	Refer to EDS for SDVO & PCI Express GFX pin mapping
(g)	O PCI Express	**PCI-E GFX Interface:** PEG_TX[15:0], PEG_TX#[15:0] **SDVO Interface:** SDVOB_RED#, SDVOB_RED, SDVOB_GREEN#, SDVOB_GREEN, SDVOB_BLUE#, SDVOB_BLUE, SDVOB_CLK, SDVOB_CLK#, SDVOC_RED#/SDVOB_ALPHA#, SDVOC_RED/ SDVOB_ALPHA, SDVOC_GREEN#, SDVOC_GREEN, SDVOC_BLUE#, SDVOC_BLUE, SDVOC_CLK, SDVOC_CLK#	Refer to EDS for SDVO & PCI Express GFX pin mapping
(h)	I A	PEG_COMPO PEG_COMPI	Analog PCI-E GFX/SDVO I/F compensation signals

Table 27. Signal Groups (Sheet 2 of 4)

Signal Group	Signal Type	Signals	Notes
DDR2 Interface Signal Groups			
(l)	I/O SSTL-1.8	SA_DQ[63:0], SB_DQ[63:0] SA_DQS[7:0], SB_DQS[7:0], SA_DQS[7:0]#, SB_DQS#[7:0]	
(j)	O SSTL-1.8	SA_DM[7:0], SB_DM[7:0], SA_MA[14:0], SB_MA[14:0], SA_BS[2:0], SB_BS[2:0], SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS#, SA_WE#, SB_WE#, SM_ODT[3:0], SM_CKE[3:0], M_CS#[3:0], SM_CK[1:0], SM_CK#[1:0], SM_CK[4:3], SM_CK#[4:3]	
	I SSTL-1.8	SA_RCVEN#, SB_RCVEN#	
(k)	I A	SM_VREF	
LVDS Signal Groups			
(l)	O LVDS	LVDSA_DATA[3:0], LVDSA_DATA#[3:0], LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA[3:0], LVDSB_DATA#[3:0], LVDSB_CLK, LVDSB_CLK#	
(m)	I/O Ref	LVDS_IBG	
	I Ref	LVDS_VBG, LVDS_VREFH, LVDS_VREFL	
CRT DAC Signal Groups			
(n)	O A	CRT_RED, CRT_RED#, CRT_GREEN, CRT_GREEN#, CRT_BLUE, CRT_BLUE#	Refer to CRT/ analog VESA spec & EDS
(o)	O A	CRT_TVO_IREF	Current mode reference pin. DC spec. not required
(p)	O HVCMOS	CRT_HSYNC, CRT_VSYNC	Refer to CRT/ analog VESA spec & EDS
TV DAC Signal Groups			
(q)	O A	TVA_DAC, TVB_DAC, TVC_DAC, TVA_RTN, TVB_RTN, TVC_RTN	
	O HVCMOS	TV_DCONSEL[1:0]	
(ae)	TV DAC band gap and channel supply	VCCA_TVA_DAC,VCCA_TVB_DAC, VCCA_TVC_DAC, VCCA_DAC_BG	

Table 27. Signal Groups (Sheet 3 of 4)

Signal Group	Signal Type	Signals	Notes
Clocks, Reset, and Miscellaneous Signal Groups			
(s)	HVCMOS input	PM_EXT_TS[1:0]#,	
(t)	Low voltage diff. clock input	HCLKP(BCLK0/BCLK), HCLKN(BCLK1/BCLK#), DREF_CLKP, DREF_CLKN, DREF_SSCLKP, DREF_SSCLKN, GCLKP, GCLKN	
(u)	O HVCMOS	L_VDD_EN, L_BKLT_EN, L_BKLT_CRTL, CLK_REQ#, ICH_SYNC#	
(ua)	O A	GFX_VID[3:0], GFX_VR_EN	
(v)	I HVCMOS	PMSYNC# (PM_BM_BUSY#)	
(va)	I/O COD	CRT_DDC_CLK, CRT_DDC_DATA, L_DDC_CLK, L_DDC_DATA, SDVO_CTRL_CLK, SDVO_CTRL_DATA, L_CRTL_CLK, L_CRTL_DATA	DDC and GMBUS support signals
	I Diff clock	DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#, HPLL_CLK, HPLL_CLK#, PEG_CLK, PEG_CLK#	PLL signals
(w)	AGTL+ input/output	CFG[17:3]	
(x)	I HVCMOS	RSTIN#, PWROK, CFG[20:18], H_BSEL[2:0] / CFG[2:0], PM_EXT_TS#[1:0, TEST1, TEST2	
(xa)	I LVCMOS	PM_DPRSTP#	
I/O Buffer Supply Voltages			
(y)	AGTL+ termination voltage	VTT (Vccp)	
(z)	SDVO, DMI, PCI Express GFX voltages	VCC3G, VCCA_3GBG	
(aa)	1.8-V DDR2 supply voltage	VCCSM	
(ab)	(G)MCH core	VCC	
(ac)	HV supply voltage	VCCHV	
(ad)	TV DAC supply voltage	VCCD_TVDAC, VCCDQ_TVDAC	
(ae)	TV DAC band gap and channel supply	VCCA_TVDACA,VCCA_TVDACB, VCCA_TVDACC	
(af)	CRT DAC supply voltage	VCCA_CRTDAC, VCCDQ_CRT, VCCD_CRT, VCC_SYNC	
(ag)	PLL supply voltages	VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	
(ah)	1.8-V LVDS digital supply	VCCD_LVDS	

Table 27. Signal Groups (Sheet 4 of 4)

Signal Group	Signal Type	Signals	Notes
(ai)	1.8-V LVDS Data/ clock transmitter supply	VCCTX_LVDS	
(aj)	1.8-V LVDS analog supply	VCCA_LVDS	
(ak)	1.25-V power supply for DDR2 DLL, DDR2 IO and FSB IO	VCC_AXD and VCC_AXF	
Controller Link Signals			
(al)	VCC-independent CMOS I/O	CL_DATA, CL_CLK,	
(al)	HVCMOS input	CL_PWROK	
(al)	CMOS input	CL_RST#,	
(al)	Analog input	CL_VREF	

12.1 General DC Characteristics

The I/O buffer supply voltage is measured at the (G)MCH package pins. The tolerances shown in Table 28 are inclusive of all noise from DC up to 20 MHz. Table 28 also indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail.

Voltages connected to a filter should be measured at the input of the filter. If the platform decoupling guidelines cannot be met, tradeoffs between the voltage regulator output DC tolerance and the decoupling performance of the capacitor network are necessary to stay within the voltage tolerances.

Table 28. DC Characteristics (Sheet 1 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage							
V_{TT}	(y)	1.05-V Host AGTL+ termination voltage	0.9975	1.05	1.1025	V	
V_{CC_AXF}		1.25-V DC input voltage for AGTL+ IO logic	1.1875	1.25	1.3125	V	
V_{CC}	(ab)	1.05-V (G)MCH core supply voltage	0.9975	1.05	1.1025	V	
V_{CC_AXG}		1.05-V graphics voltage	0.9975	1.05	1.1025	V	16
V_{CC_AXM}		1.05-V Intel® Management Engine voltage	0.9975	1.05	1.1025	V	
V_{CC_SM}	(aa)	DDR2 I/O supply voltage	1.7	1.8	1.9	V	

Table 28. DC Characteristics (Sheet 2 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
$V_{CC\_SM\_CK}$		1.8-V DDR2 clock IO voltage	1.7	1.8	1.9	V	
V_{CCA_SM}		1.25-V DDR2 voltage connects to IO logic and DLLs	1.1875	1.25	1.3125	V	
V_{CC_AXD}		1.25-V DDR2 high speed IO logic voltage and controller link IO	1.1875	1.25	1.3125	V	
$V_{CCA\_SM\_CK}$		1.25-V DDR2 IO logic voltage for SM clocks	1.1875	1.25	1.3125	V	
V_{CC_PEG}	(z)	1.05-V PCI Express supply voltage	0.9975	1.05	1.1025	V	
V_{CC_DMI}		1.25-V TX analog and term voltage for DMI	1.1875	1.25	1.3125	V	
$V_{CCR\_RX\_DMI}$		1.05-V Rx and I/O logic for DMI	0.9975	1.05	1.1025	V	
$V_{CCA\_PEG\_BG}$		3.3-V analog band gap voltage	3.135	3.3	3.465	V	
V_{CCHV}	(ac)	HV CMOS supply voltage	3.135	3.3	3.465	V	
V_{CCD_TVDAC}	(ad)	TV DAC supply voltage	1.425	1.5	1.575	V	
V_{CCD_QTVDAC}	(ad)	TV DAC quiet supply voltage	1.425	1.5	1.575	V	
$V_{CCA\_TVA\_DAC}$ $V_{CCA\_TVB\_DAC}$ $V_{CCA\_TVC\_DAC}$ $V_{CCA\_DAC\_BG}$	(ae)	TV DAC analog & band gap supply voltage	3.135	3.3	3.465	V	
$V_{CCA\_CRT\_DAC}$	(af)	CRT DAC supply voltage	3.135	3.3	3.465	V	
V_{CC_SYNC}	(af)	CRT DAC SYNC supply voltage	3.135	3.3	3.465	V	
V_{CCD_QCRT}		1.5-V CRT quiet digital voltage	1.425	1.5	1.575		
V_{CCD_CRT}		1.5-V CRT digital power supply	1.425	1.5	1.575		
V_{CCA_HPLL} V_{CCA_MPLL} V_{CCD_HPLL} $V_{CCA\_PEG\_PLL}$ $V_{CCD\_PEG\_PLL}$ V_{CCA_DPLLA} V_{CCA_DPLLB}	(ag)	Various PLLS analog supply voltages	1.1875	1.25	1.3125	V	
V_{CCD_LVDS}	(ah)	Digital LVDS supply voltage	1.7	1.8	1.9	V	
$V_{CC\_TX\_LVDS}$	(ai)	Data/clock transmitter LVDS supply voltage	1.7	1.8	1.9	V	

Table 28. DC Characteristics (Sheet 3 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{CCA_LVDS}	(aj)	Analog LVDS supply voltage	1.7	1.8	1.9	V	
Reference Voltages							
H_VREF	(e)	Host address and data reference voltage	2/3 x VTT – 1%	2/3 x VTT	2/3 x VTT + 1%	V	
H_SWING	(e)	Host compensation reference voltage	0.3125x VTT – 1%	0.3125 x VTT	0.3125x VTT + 1%	V	
SM_VREF	(k)	DDR2 reference voltage	0.49 x VCCSM	0.50 x VCCSM	0.51 x VCCSM	V	
Host Interface							
V_{IL_H}	(a, d, w)	Host AGTL+ input low voltage	-0.10	0	(2/3 x VTT) – 0.1	V	
V_{IH_H}	(a, d, w)	Host AGTL+ input high voltage	(2/3 x VTT) + 0.1	VTT (1.05)	VTT + 0.1	V	
V_{OL_H}	(a, b, w)	Host AGTL+ output low voltage			0.3125 x VTT) + 0.1	V	
V_{OH_H}	(a, b, w)	Host AGTL+ output high voltage	VTT-0.1		VTT	V	
I_{OL_H}	(a, b, w)	Host AGTL+ output low current			VTT_{max} / ($Rterm_{min}$ - Rpd_{min})	mA	5
I_{LEAK_H}	(a, d, w)	Host AGTL+ input leakage current			± 10	µA	
C_{PAD}	(a, d, w)	Host AGTL+ input capacitance	1.2		2.5	pF	
V_{OL_H}	(c)	CMOS output low voltage			0.1 VTT	V	I_{OL} = 1 mA
V_{OH_H}	(c)	CMOS output high voltage	0.9 VTT		VTT	V	I_{OH} = 1 mA
DDR2 Interface							
$V_{IL(DC)}$	(l)	DDR2 input low voltage			SM_VREF _ 0.125	V	
$V_{IH(DC)}$	(l)	DDR2 input high voltage	SM_VREF + 0.125			V	
$V_{IL(AC)}$	(i)	DDR2 input low voltage			SM_VREF _ 0.250	V	
$V_{IH(AC)}$	(i)	DDR2 input high voltage	SM_VREF + 0.250			V	

Table 28. DC Characteristics (Sheet 4 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{OL}	(i, j)	DDR2 output low voltage			0.3	V	2
V_{OH}	(i, j)	DDR2 output high voltage	1.5			V	2
I_{LEAK}	(i)	Input leakage Current			±10	µA	
$C_{I/O}$	(i, j)	DDR2 input/output pin capacitance	1.0		4.0	pF	
1.05 V PCI Express Interface 1.1 (includes PCI Express GFX and SDVO)							
$V_{TX-DIFF\ P-P}$	(f, g)	Differential peak to peak output voltage	0.400		1.2	V	3, 4
V_{TX_CM-ACp}	(f, g)	AC peak common mode output voltage			20	mV	3
$Z_{TX-DIFF-DC}$	(f, g)	DC differential TX impedance	80	100	120		
$V_{RX-DIFF\ p-p}$	(f, g)	Differential input peak to peak voltage	0.175		1.2	V	3, 4
V_{RX_CM-ACp}	(f, g)	AC peak common mode input voltage			150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(s)	Input low voltage			0.8	V	
V_{IH}	(s)	Input high voltage	2.0			V	
I_{LEAK}	(s)	Input leakage current			± 10	µA	
C_{IN}	(s)	Input capacitance	3.0		6.0	pF	
V_{IL}	(t)	Input low voltage	-0.3			V	5, 13, 14
V_{IH}	(t)	Input high voltage			1.15	V	5, 12, 13
V_{CROSS}	(t)	Crossing voltage	0.300		0.550	V	6, 11, 15
ΔV_{CROSS}	(t)	Range of crossing points	NA	NA	0.140	V	6, 11, 9
V_{SWING}	(t)	Differential output swing	0.300			V	5, 10
I_{LEAK}	(t)	Input leakage current	-5		+5	µA	5, 7
C_{PAD}	(t)	Pad capacitance	0.95	1.2	1.45	pF	5, 8
V_{OL}	(u)	Output low voltage (CMOS outputs)			0.4	V	
V_{OH}	(u)	Output high voltage (CMOS outputs)	2.8			V	
I_{OL}	(u)	Output low current (CMOS outputs)			1	mA	@V_{OL_HI} max
I_{OH}	(u)	Output high current (CMOS outputs)	-1			mA	@V_{OH_HI} min
V_{IL}	(v)	Input low voltage (DC)			0.8	V	
V_{IH}	(v)	Input high voltage (DC)	1.55			V	

Table 28. DC Characteristics (Sheet 5 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I_{LEAK}	(v)	Input leakage current			±10	µA	
C_{IN}	(v)	Input capacitance			10	pF	
V_{IL}	(x)	Input low voltage			0.8	V	
V_{IH}	(x)	Input high voltage	2.0			V	
I_{LEAK}	(x)	Input leakage current			±10	µA	
C_{IN}	(x)	Input capacitance			10	pF	
LVDS Interface: Functional Operating Range (VCC=1.8 V±5%)							
V_{OD}	(l)	Differential output voltage	250	350	450	mV	17
ΔV_{OD}	(l)	Change in V_{OD} between complementary output states			50	mV	17
V_{OS}	(l)	Offset voltage	1.125	1.25	1.375	V	17
ΔV_{OS}	(l)	Change in V_{OS} between complementary output states			50	mV	17
I_{Os}	(l)	Output short circuit current		-3.5	-10	mA	17
I_{OZ}	(l)	Output TRI-STATE current		± 1	± 10	µA	17
Controller Link							
V_{IL}	(al)	Input low voltage			0.277	V	
V_{IH}	(al)	Input high voltage	0.427			V	
I_{LEAK}	(al)	Input leakage current			±20	µA	
C_{IN}	(al)	Input capacitance			2.0	pF	
I_{OL}	(al)	Output low current (CMOS outputs)			1.0	mA	@V_{OL_HI} max
I_{OH}	(al)	Output high current (CMOS outputs)	6			mA	@V_{OH_HI} min
V_{OL}	(al)	Output low voltage (CMOS outputs)			0.06	V	
V_{OH}	(al)	Output high voltage (CMOS outputs)	0.6			V	
SDVO_CTRLDATA, SDVO_CTRLCLK							
V_{IL}		Input low voltage			0.75	V	
V_{IH}		Input high voltage	1.75			V	
I_{LEAK}		Input leakage current			±10	µA	
C_{IN}		Input capacitance			10.0	pF	
V_{OL}		Output low voltage			0.4	V	

Table 28. DC Characteristics (Sheet 6 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
CRT_DDC_DATA, CRT_DDC_CLK, L_DDC_CLK, L_DDC_DATA, L_CRTL_CLK, L_CTRL_DATA, TV_DCONSEL_0, TV_DCONSEL_1, CLKREQ#							
V_{IL}		Input low voltage			0.9	V	
V_{IH}		Input high voltage	2.1			V	
I_{LEAK}		Input leakage current			±10	µA	
C_{IN}		Input capacitance			10.0	pF	
V_{OL}		Output low voltage			0.4	V	
L_VDDEN, L_BKLTEN, L_BKLTCTL, DFGT_VID[3:0], DFGT_VR_EN							
V_{IL}		Input low voltage			0.9	V	
V_{IH}		Input high voltage	2.1			V	
I_{LEAK}		Input leakage current			±10	µA	
C_{IN}		Input capacitance			10.0	pF	
V_{OL}		Output low voltage (CMOS outputs)			0.4	V	
V_{OH}		Output high voltage (CMOS outputs)	2.7			V	
CFG_RSVD[2:0], DPRSLPVR, PM_EXTTS#[1:0]							
V_{IL}		Input low voltage			0.9	V	
V_{IH}		Input high voltage	2.1			V	
I_{LEAK}		Input leakage current			±10	µA	
C_{IN}		Input capacitance			10.0	pF	
PM_DPRSTP# VCC = 1.05V							
V_{IL}		Input low voltage			0.3VCC	V	
V_{IH}		Input high voltage	0.7 VCC			V	
I_{LEAK}		Input leakage current			±10	µA	
C_{IN}		Input capacitance			10.0	pF	

NOTES:

2. Determined with 2x (G)MCH DDR2 buffer strength settings into a 50 Ω to 0.5 x VCCSM (DDR2) test load.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in transmitter compliance eye diagram of PCI Express specification and measured over any 250 consecutive TX UIs. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements.
4. For low voltage PCI Express (PCI Express Graphics/SDVO) interface:

Symbol	Parameter	Min	Typ	Max	Unit
R_{TT}	Termination resistance	50	55	61	Ω
R_{CN}	Buffer on resistance	22	25	28	Ω

5. Unless otherwise noted, all specifications in this table apply to all FSB frequencies.

6. Crossing voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
7. For Vin between 0 V and V_H.
8. Cpad includes die capacitance only. No package parasitics are included.
9. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 6.
10. Measurement taken from differential waveform.
11. Measurement taken from single-ended waveform.
12. "Steady state" voltage, not including Overshoots or Undershoots.
13. The maximum voltage including overshoot.
14. The minimum voltage including undershoot.
15. Only applies to the differential rising edge (Clock rising and Clock# falling).
16. If a variable VRM is used the V_{CC_AXG} should be ±5% of the nominal setting (the setting shown is of 1.05 V).
17. All LVDS active lanes must be terminated with 100-Ω resistors for correct Vos performance and measurement.

12.2 CRT DAC DC Characteristics

Table 29. CRT DAC DC Characteristics: Functional Operating Range (VCCADAC = 3.3 V ±5%)

Parameter	Min	Typical	Max	Units	Notes
DAC resolution		8		Bits	(1) Measured at low frequency
Maximum luminance (full-scale)	0.665	0.700	0.770	V	(2, 4, 5) white video level voltage
Minimum luminance		0.000		V	(3) Measured at DC. Black video level voltage
LSB current		73.2		µA	(4, 5)
Integral linearity (INL)	-1.0		+1.0	LSB	(6)
Differential linearity (DNL)	-1.0		+1.0	LSB	(6)
Video channel-channel voltage amplitude mismatch			6	%	(7)
Monotonicity	Guaranteed				

NOTES:
1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Maximum steady-state amplitude.
3. Minimum steady-state amplitude.
4. Defined for a double 75-Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA video signal standards.
7. Max full-scale voltage difference among R, G, B outputs (percentage of steady-state full-scale voltage).

12.3 TV DAC DC Characteristics

Table 30. TV DAC DC Characteristics: Functional Operating Range (VCCATVDAC [A,B,C] = 3.3 V ±5%)

Parameter	Min	Typical	Max	Units	Notes
DAC resolution		10		Bits	Measured at low frequency
ENOB (Effective number of bits)	7.5			Bits	@ NTSC/PAL Video BW
Max luminance (full scale)	1.235	1.3	1.365	V	For composite video signal Note: 1, 3, 4
Maximum luminance (full scale)	1.045	1.1	1.155	V	For S-Video signal Note: 1, 3, 4
Maximum luminance (full scale)	0.665	0.7	0.735	V	For component video signal Note: 1, 3, 4
Minimum luminance	-0.1	0	+0.1	mV	Measured at DC, Note: 2
Integral linearity (INL)	-2.5		+2.5	LSB	Note: 5
Differential linearity (DNL)	-0.5		+0.5	LSB	Note: 5
SNR	48			dB	RMS @ NTSC/PAL video BW
Video channel-channel voltage amplitude mismatch	-3		+3	%	Note: 6
Monotonicity	Guaranteed				

NOTES:
1. Maximum steady-state amplitude.
2. Minimum steady-state amplitude.
3. Defined for a double 75-Ω termination.
4. Set by external reference resistor value.
5. INL and DNL measured and calculated based on the method given in VESA video signal standards.
6. Maximum full-scale voltage difference among the outputs (percentage of steady-state full-scale voltage).

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13 Clocking

13.1 Overview

The (G)MCH has a total of four PLLs that are used for many internal clocks. The PLLs are:

- Host PLL—Generates the main core clocks in the host clock domain. Can also be used to generate memory and integrated graphics core clocks. Uses the Host clock (HPLL_CLK /HPLL_CLK#) as a reference.
- PCI Express PLL—Generates all PCI Express related clocks, including the DMI that connects to the ICH. This PLL uses the 100 MHz (PEG_CLK / PEG_CLK#) as a reference.
- Display PLL A—Generates the internal clocks for Display A or Display B. Uses the low voltage 96-MHz differential clock, DPLL_REF_CLK / DPLL_REF_CLK#, as a reference.
- Display PLL B—Generates the internal clocks for Display A or Display B. Uses the low voltage 96-MHz differential clock, DPLL_REF_CLK / DPLL_REF_CLK#, as a reference. Also may optionally use DPLL_REF_SSCLK / DPLL_REF_SSCLK#as a reference for SSC support for LVDS display.

13.2 (G)MCH Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
HPLL_CLK / HPLL_CLK#	133, 167, 200	Host / Memory / Graphics Core
PEG_CLK / PEG_CLK#	100 MHz	PCI Express / DMI PLL
DPLL_REF_CLK / DPLL_REF_CLK#	96 MHz	Display PLL A or B
DPLL_REF_SSCLK / DPLL_REF_SSCLK#	96 MHz (Non-SSC) 100 MHz (SSC)	Display PLL B

13.3 Host/Memory/Graphics Core Clock Frequency Support

Table 31. Host/Memory/Graphics Clock Frequency Support for 1.05-V Core Voltage for the Mobile Intel GM965 and GL960 Express Chipsets

Host (MHz)	Memory (MHz)	Display Clock (MHz)	Render Clock (MHz)
533	DDR2 533	320	267(GM965/GL960)/320(GM965/GL960)/400(GM965/GL960)
533	DDR2 533	200	267(GM965/GL960)
667	DDR2 533	333	267(GM965)/333(GM965)
667	DDR2 667	333	250(GM965)/333(GM965)/400(GM965)/500(GM965)
800	DDR2 533	320	267(GM965)/320(GM965)/400(GM965)
800	DDR2 667	333	250(GM965)/333(GM965)/400(GM965)/500(GM965)
800	DDR2 667	200	500(GM965)

Note: All supported frequencies for GM965/GL960 apply for GME965/GLE960 respectively

Table 32. Host/Memory/Graphics Clock Frequency Support for 1.05-V Core Voltage for the Mobile Intel GM965/GM965 (mini-note)/GM965 (sub-note), GL960 and PM965 Express Chipsets

SKU	GM965	GM965 (mini-note)	GM965 (sub-note)	GL960	PM965
Max FSB (MHz)	800	800	533	533	800
Max Memory (MHz)	DDR2 667	DDR2 533	DDR2 533	DDR2 533	DDR2 667
Max Display Clock (MHz)	333	320	320	320	N/A
Recommended Max Render Clock (MHz)	500	320	267	400	N/A

Note: All supported frequencies for GM965/GL960 apply for GME965/GLE960 respectively

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14 (G)MCH Strapping Configuration

Table 33. (G)MCH Strapping Signals and Configuration

Pin Name	Strap Description	Configuration	Pull Up Rail	Notes
CFG[2:0]	FSB Frequency Select	010 = FSB 800 MHz 011 = FSB 667 MHz 001 = FSB 533 MHz Others: Reserved	1.05 V	1, 2, 3
CFG[4:3]	Reserved			
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (default)	1.05 V	1, 2, 3
CFG[8:6]	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Lane Reversed 1 = Normal mode (default; lanes numbered in order)	1.05 V	1, 2, 3
CFG[11:10]	Reserved			
CFG[13:12]	XOR/ALL-Z	00 = Reserved 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (default)	1.05 V	1, 2,3
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disabled 1 = Dynamic ODT enabled (default)		1, 2, 3
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal mode (default; lanes numbered in order) 1 = Lane reversed	3.3 V	1, 2, 3
CFG20	Concurrent SDVO / PCI Express	0 = Only SDVO or PCI Express is operational (default) 1 = SDVO and PCI Express operate simultaneously through the PCI Express Graphics attach port	3.3 V	1, 2, 3
SDVO_CTRL_DATA	SDVO Present	0 = No SDVO Card Present (default) 1 = SDVO Card Present	2.5 V	all

NOTES:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. Default values do not require pull-up/pull-down resistors.
3. Pull-up/Pull-down resistor value should be 4-kΩ ±5%.
4. No need for pull-up resistor if an SDVO Add In card is being use.

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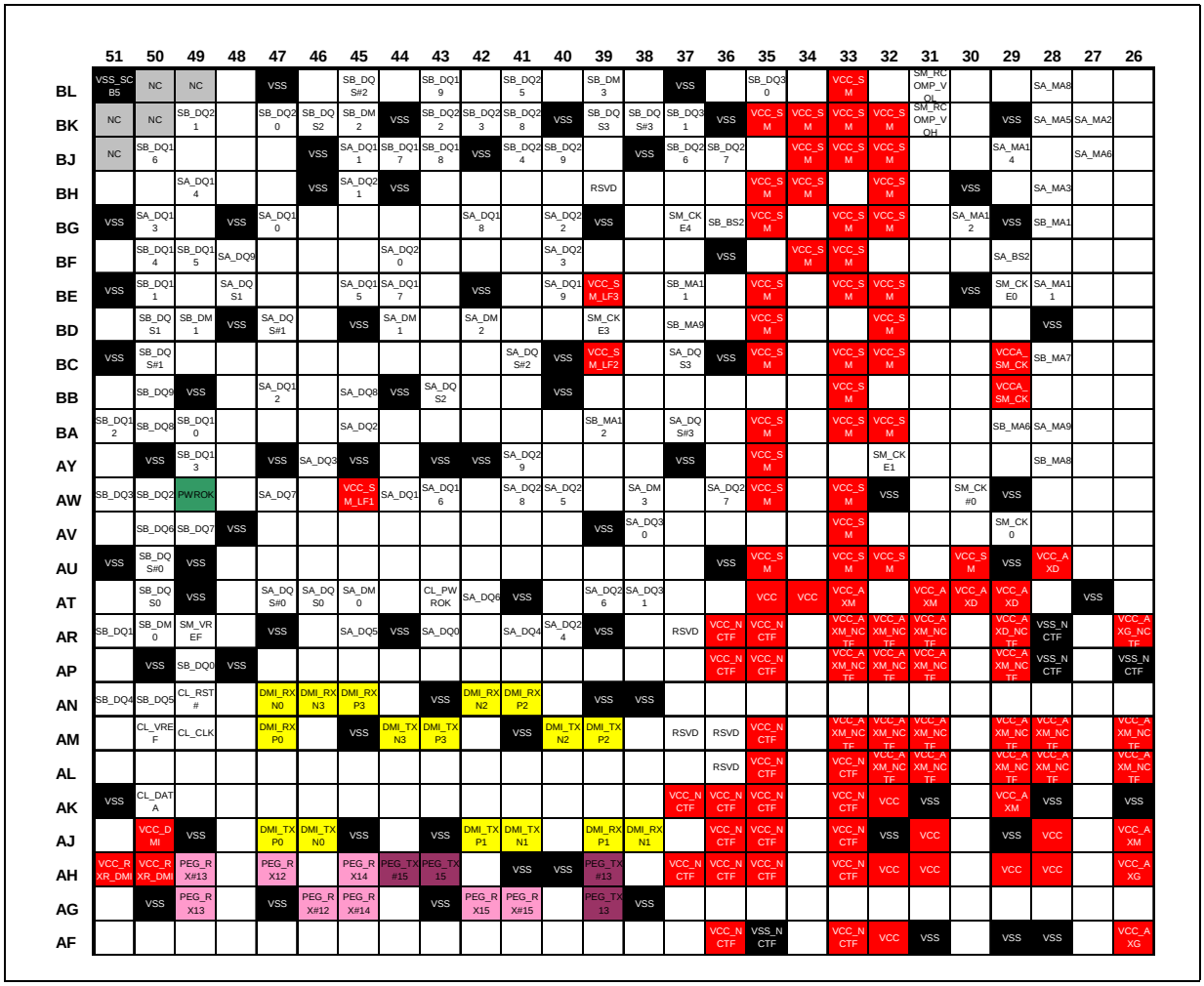
15 Ballout and Package Information

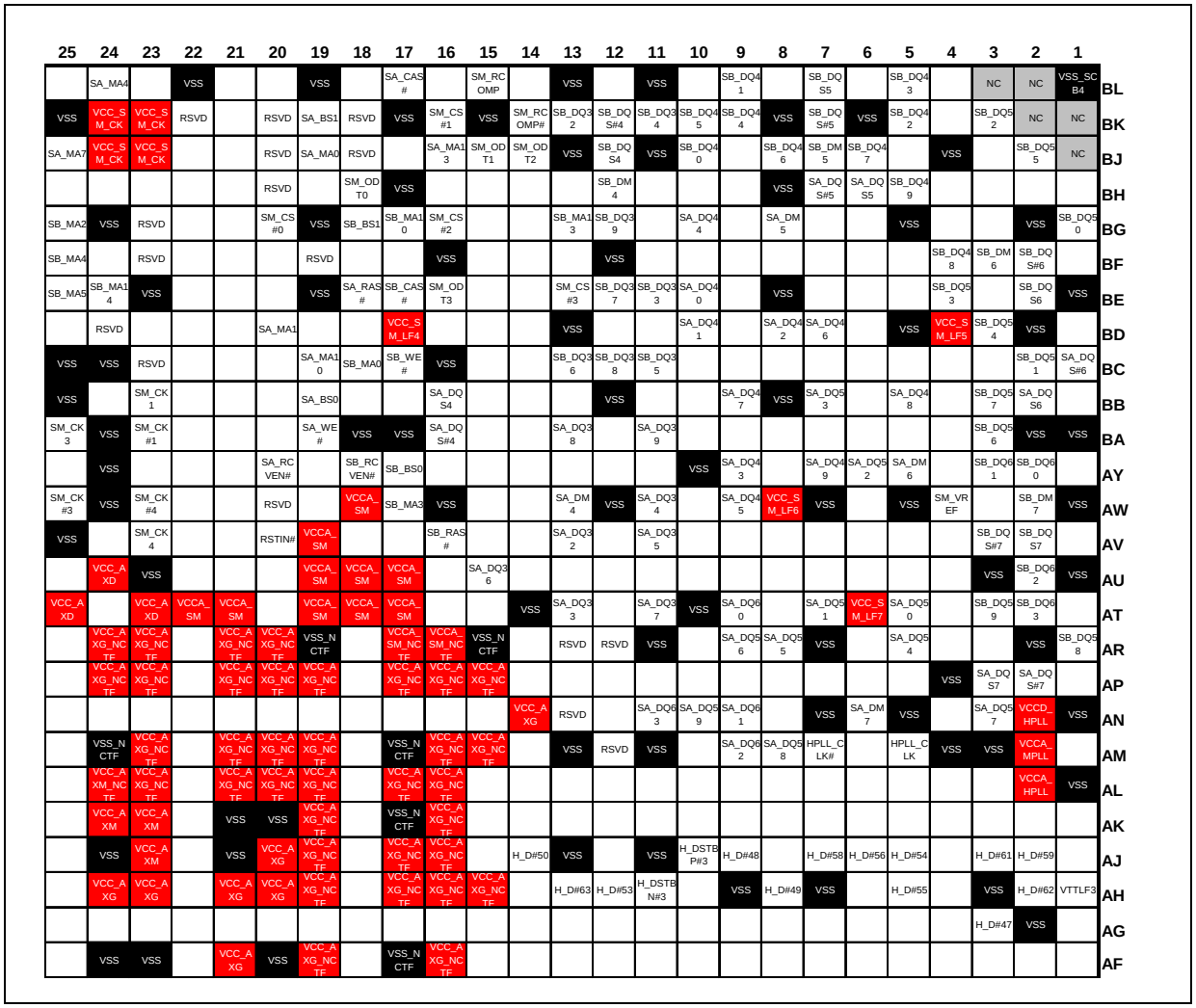
15.1 (G)MCH Ballout Diagrams

Figure 21. Ballout Diagram (Top View) Upper Left Quadrant



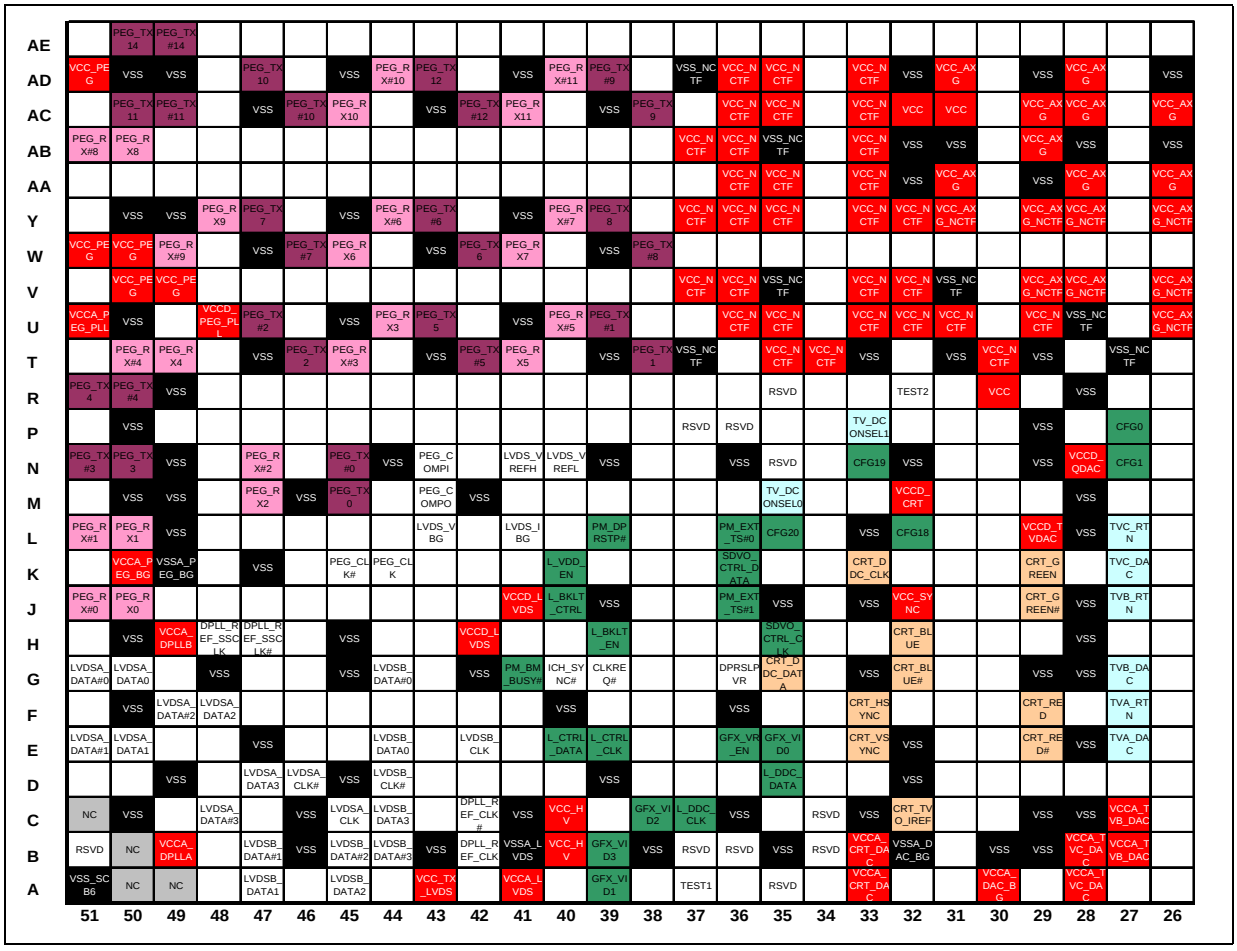
	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
BL	VSS_SCB5	NC	NC		VSS		SB_DQS#2		SB_DQ19		SB_DQ25		SB_DM3		VSS		SB_DQ30		VCC_SM		SM_RCOMP_VOL			SA_MA8		
BK	NC	NC	SB_DQ21		SB_DQ20	SB_DQS2	SB_DM2	VSS	SB_DQ22	SB_DQ23	SB_DQ28	VSS	SB_DQS3	SB_DQS#3	SB_DQ31	VSS	VCC_SM	VCC_SM	VCC_SM	VCC_SM	SM_RCOMP_VOH		VSS	SA_MA5	SA_MA2	
BJ	NC	SB_DQ16				VSS	SA_DQ11	SB_DQ17	SB_DQ18	VSS	SB_DQ24	SB_DQ29		VSS	SB_DQ26	SB_DQ27		VCC_SM	VCC_SM	VCC_SM			SA_MA14		SA_MA6	
BH			SA_DQ14			VSS	SA_DQ21	VSS					RSVD				VCC_SM	VCC_SM		VCC_SM		VSS		SA_MA3		
BG	VSS	SA_DQ13		VSS	SA_DQ10					SA_DQ18		SA_DQ22	VSS		SM_CKE4	SB_BS2	VCC_SM		VCC_SM	VCC_SM		SA_MA12	VSS	SB_MA1		
BF		SB_DQ14	SB_DQ15	SA_DQ9				SA_DQ20				SA_DQ23				VSS		VCC_SM	VCC_SM				SA_BS2			
BE	VSS	SB_DQ11		SA_DQS1			SA_DQ15	SA_DQ17		VSS		SA_DQ19	VCC_SM_LF3		SB_MA11		VCC_SM		VCC_SM	VCC_SM		VSS	SM_CKE0	SA_MA11		
BD		SB_DQS1	SB_DM1	VSS	SA_DQS#1		VSS	SA_DM1		SA_DM2			SM_CKE3		SB_MA9		VCC_SM			VCC_SM				VSS		
BC	VSS	SB_DQS#1									SA_DQS#2	VSS	VCC_SM_LF2		SA_DQS3	VSS	VCC_SM		VCC_SM	VCC_SM			VCCA_SM_CK	SB_MA7		
BB		SB_DQ9	VSS		SA_DQ12		SA_DQ8	VSS	SA_DQS2			VSS							VCC_SM				VCCA_SM_CK			
BA	SB_DQ12	SB_DQ8	SB_DQ10				SA_DQ2						SB_MA12		SA_DQS#3		VCC_SM		VCC_SM	VCC_SM			SB_MA6	SA_MA9		
AY		VSS	SB_DQ13		VSS	SA_DQ3	VSS		VSS	VSS	SA_DQ29				VSS		VCC_SM			SM_CKE1				SB_MA8		
AW	SB_DQ3	SB_DQ2	PWROK		SA_DQ7		VCC_SM_LF1	SA_DQ1	SA_DQ16		SA_DQ28	SA_DQ25		SA_DM3		SA_DQ27	VCC_SM		VCC_SM	VSS		SM_CK#0	VSS			
AV		SB_DQ6	SB_DQ7	VSS									VSS	SA_DQ30					VCC_SM				SM_CK0			
AU	VSS	SB_DQS#0	VSS													VSS	VCC_SM		VCC_SM	VCC_SM		VCC_SM	VSS	VCC_AXD		
AT		SB_DQS0	VSS		SA_DQS#0	SA_DQS0	SA_DM0		CL_PWROK	SA_DQ6	VSS		SA_DQ26	SA_DQ31			VCC	VCC	VCC_AXM		VCC_AXM	VCC_AXD	VCC_AXD		VSS	
AR	SB_DQ1	SB_DM0	SM_VREF		VSS		SA_DQ5	VSS	SA_DQ0		SA_DQ4	SA_DQ24	VSS		RSVD	VCC_NCTF	VCC_NCTF		VCC_AXM_NCTF	VCC_AXM_NCTF	VCC_AXM_NCTF		VCC_AXD_NCTF	VSS_NCTF		VCC_AXG_NCTF
AP		VSS	SB_DQ0	VSS												VCC_NCTF	VCC_NCTF		VCC_AXM_NCTF	VCC_AXM_NCTF	VCC_AXM_NCTF		VCC_AXM_NCTF	VSS_NCTF		VSS_NCTF
AN	SB_DQ4	SB_DQ5	CL_RST#		DMI_RXN0	DMI_RXN3	DMI_RXP3		VSS	DMI_RXN2	DMI_RXP2		VSS	VSS												
AM		CL_VREF	CL_CLK		DMI_RXP0		VSS	DMI_TXN3	DMI_TXP3		VSS	DMI_TXN2	DMI_TXP2		RSVD	RSVD	VCC_NCTF		VCC_AXM_NCTF	VCC_AXM_NCTF	VCC_AXM_NCTF		VCC_AXM_NCTF	VCC_AXM_NCTF		VCC_AXM_NCTF
AL																RSVD	VCC_NCTF		VCC_NCTF	VCC_AXM_NCTF	VCC_AXM_NCTF		VCC_AXM_NCTF	VCC_AXM_NCTF		VCC_AXM_NCTF
AK	VSS	CL_DATA													VCC_NCTF	VCC_NCTF	VCC_NCTF		VCC_NCTF	VCC	VSS		VCC_AXM	VSS		VSS
AJ		VCC_DMI	VSS		DMI_TXP0	DMI_TXN0	VSS		VSS	DMI_TXP1	DMI_TXN1		DMI_RXP1	DMI_RXN1		VCC_NCTF	VCC_NCTF		VCC_NCTF	VSS	VCC		VSS	VCC		VCC_AXM
AH	VCC_RXR_DM	VCC_RXR_DM	PEG_RX#13		PEG_RX12		PEG_RX14	PEG_TX#15	PEG_TX15		VSS	VSS	PEG_TX#13		VCC_NCTF	VCC_NCTF	VCC_NCTF		VCC_NCTF	VCC	VCC		VCC	VCC		VCC_AXG
AG		VSS	PEG_RX13		VSS	PEG_RX#12	PEG_RX#14		VSS	PEG_RX15	PEG_RX#15		PEG_TX13	VSS												
AF																VCC_NCTF	VSS_NCTF		VCC_NCTF	VCC	VSS		VSS	VSS		VCC_AXG

Figure 22. Ballout Diagram (Top View) Upper Right Quadrant



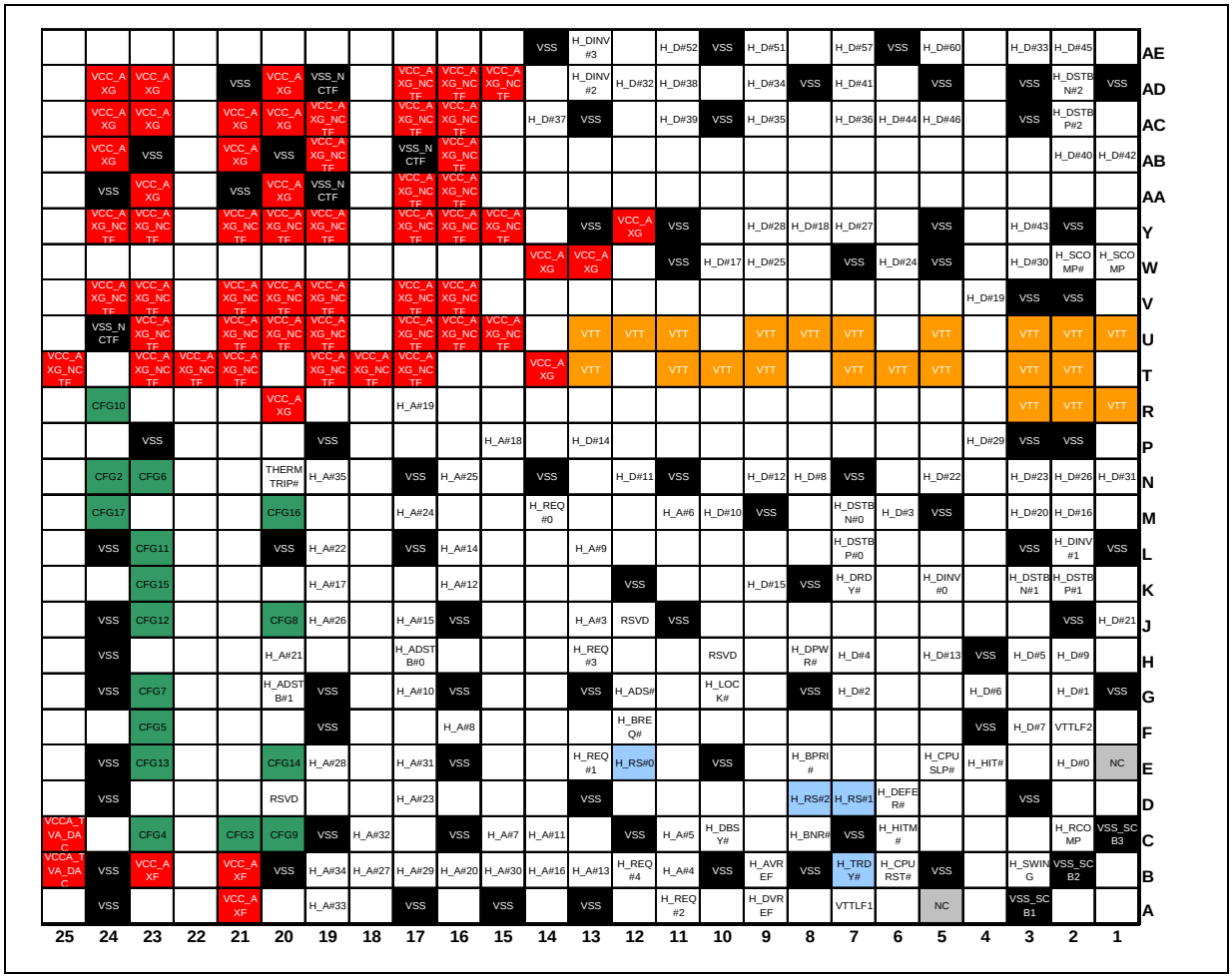
25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	SA_MA4		VSS			VSS		SA_CAS#		SM_RCOMP		VSS		VSS		SB_DQ41		SB_DQS5		SB_DQ43		NC	NC	VSS_SCB4	BL
VSS	VCC_SM_CK	VCC_SM_CK	RSVD		RSVD	SA_BS1	RSVD	VSS	SM_CS#1	VSS	SM_RCOMP#	SB_DQ32	SB_DQS#4	SB_DQ34	SB_DQ45	SB_DQ44	VSS	SB_DQS#5	VSS	SB_DQ42		SB_DQ52	NC	NC	BK
SA_MA7	VCC_SM_CK	VCC_SM_CK			RSVD	SA_MA0	RSVD		SA_MA13	SM_ODT1	SM_ODT2	VSS	SB_DQS4	VSS	SB_DQ40		SB_DQ46	SB_DM5	SB_DQ47		VSS		SB_DQ55	NC	BJ
					RSVD		SM_ODT0	VSS					SB_DM4				VSS	SA_DQS#5	SA_DQS5	SB_DQ49					BH
SB_MA2	VSS	RSVD			SM_CS#0	VSS	SB_BS1	SB_MA10	SM_CS#2			SB_MA13	SB_DQ39		SA_DQ44		SA_DM5			VSS			VSS	SB_DQ50	BG
SB_MA4		RSVD				RSVD			VSS				VSS								SB_DQ48	SB_DM6	SB_DQS#6		BF
SB_MA5	SB_MA14	VSS				VSS	SA_RAS#	SB_CAS#	SM_ODT3			SM_CS#3	SB_DQ37	SB_DQ33	SA_DQ40		VSS				SB_DQ53		SB_DQS6	VSS	BE
	RSVD				SA_MA1			VCC_SM_LF4				VSS			SA_DQ41		SA_DQ42	SA_DQ46		VSS	VCC_SM_LF5	SB_DQ54	VSS		BD
VSS	VSS	RSVD				SA_MA10	SB_MA0	SB_WE#	VSS			SB_DQ36	SB_DQ38	SB_DQ35										SB_DQ51	SA_DQS#6	BC
VSS		SM_CK1				SA_BS0			SA_DQS4				VSS			SA_DQ47	VSS	SA_DQ53		SA_DQ48		SB_DQ57	SA_DQS6		BB
SM_CK3	VSS	SM_CK#1				SA_WE#	VSS	VSS	SA_DQS#4			SA_DQ38		SA_DQ39								SB_DQ56	VSS	VSS	BA
	VSS				SA_RCVEN#		SB_RCVEN#	SB_BS0							VSS	SA_DQ43		SA_DQ49	SA_DQ52	SA_DM6		SB_DQ61	SB_DQ60		AY
SM_CK#3	VSS	SM_CK#4			RSVD		VCCA_SM	SB_MA3	VSS			SA_DM4	VSS	SA_DQ34		SA_DQ45	VCC_SM_LF6	VSS		VSS	SM_VREF		SB_DM7	VSS	AW
VSS		SM_CK4			RSTIN#	VCCA_SM			SB_RAS#			SA_DQ32		SA_DQ35								SB_DQS#7	SB_DQS7		AV
	VCC_AXD	VSS				VCCA_SM	VCCA_SM	VCCA_SM		SA_DQ36												VSS	SB_DQ62	VSS	AU
VCC_AXD		VCC_AXD	VCCA_SM	VCCA_SM		VCCA_SM	VCCA_SM	VCCA_SM			VSS	SA_DQ33		SA_DQ37	VSS	SA_DQ60		SA_DQ51	VCC_SM_LF7	SA_DQ50		SB_DQ59	SB_DQ63		AT
	VCC_AXG_NCTF	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF	VSS_NCTF		VCCA_SM_NCTF	VCCA_SM_NCTF	VSS_NCTF		RSVD	RSVD	VSS		SA_DQ56	SA_DQ55	VSS		SA_DQ54			VSS	SB_DQ58	AR
	VCC_AXG_NCTF	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF	VCC_AXG_NCTF											VSS	SA_DQS7	SA_DQS#7		AP
											VCC_AXG	RSVD		SA_DQ63	SA_DQ59	SA_DQ61		VSS	SA_DM7	VSS		SA_DQ57	VCCD_HPLL	VSS	AN
	VSS_NCTF	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF	VCC_AXG_NCTF		VSS_NCTF	VCC_AXG_NCTF	VCC_AXG_NCTF		VSS	RSVD	VSS		SA_DQ62	SA_DQ58	HPLL_CLK#		HPLL_CLK	VSS	VSS	VCCA_MPLL		AM
	VCC_AXM_NCTF	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF														VCCA_HPLL	VSS	AL
	VCC_AXM	VCC_AXM		VSS	VSS	VCC_AXG_NCTF		VSS_NCTF	VCC_AXG_NCTF																AK
	VSS	VCC_AXM		VSS	VCC_AXG	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF		H_D#50	VSS		VSS	H_DSTBP#3	H_D#48		H_D#58	H_D#56	H_D#54		H_D#61	H_D#59		AJ
	VCC_AXG	VCC_AXG		VCC_AXG	VCC_AXG	VCC_AXG_NCTF		VCC_AXG_NCTF	VCC_AXG_NCTF	VCC_AXG_NCTF		H_D#63	H_D#53	H_DSTBN#3		VSS	H_D#49	VSS		H_D#55		VSS	H_D#62	VTTLF3	AH
																						H_D#47	VSS		AG
	VSS	VSS		VCC_AXG	VSS	VCC_AXG_NCTF		VSS_NCTF	VCC_AXG_NCTF																AF

Figure 23. Ballout Diagram (Top View) Lower Left Quadrant



	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
AE		PEG_TX 14	PEG_TX #14																							
AD	VCC_PE G	VSS	VSS		PEG_TX 10		VSS	PEG_R X#10	PEG_TX 12		VSS	PEG_R X#11	PEG_TX #9		VSS_NC TF	VCC_N CTF	VCC_N CTF		VCC_N CTF	VSS	VCC_AX G		VSS	VCC_AX G		VSS
AC		PEG_TX 11	PEG_TX #11		VSS	PEG_TX #10	PEG_R X10		VSS	PEG_TX #12	PEG_R X11		VSS	PEG_TX 9		VCC_N CTF	VCC_N CTF		VCC_N CTF	VCC	VCC		VCC_AX G	VCC_AX G		VCC_AX G
AB	PEG_R X#8	PEG_R X8													VCC_N CTF	VCC_N CTF	VSS_NC TF		VCC_N CTF	VSS	VSS		VCC_AX G	VSS		VSS
AA																VCC_N CTF	VCC_N CTF		VCC_N CTF	VSS	VCC_AX G		VSS	VCC_AX G		VCC_AX G
Y		VSS	VSS	PEG_R X9	PEG_TX 7		VSS	PEG_R X#6	PEG_TX #6		VSS	PEG_R X#7	PEG_TX 8		VCC_N CTF	VCC_N CTF	VCC_N CTF		VCC_N CTF	VCC_N CTF	VCC_AX G_NCTF		VCC_AX G_NCTF	VCC_AX G_NCTF		VCC_AX G_NCTF
W	VCC_PE G	VCC_PE G	PEG_R X#9		VSS	PEG_TX #7	PEG_R X6		VSS	PEG_TX 6	PEG_R X7		VSS	PEG_TX #8												
V		VCC_PE G	VCC_PE G												VCC_N CTF	VCC_N CTF	VSS_NC TF		VCC_N CTF	VCC_N CTF	VSS_NC TF		VCC_AX G_NCTF	VCC_AX G_NCTF		VCC_AX G_NCTF
U	VCCA_P EG_PLL	VSS		VCCD_ PEG_PL L	PEG_TX #2		VSS	PEG_R X3	PEG_TX 5		VSS	PEG_R X#5	PEG_TX #1			VCC_N CTF	VCC_N CTF		VCC_N CTF	VCC_N CTF	VCC_N CTF		VCC_N CTF	VSS_NC TF		VCC_AX G_NCTF
T		PEG_R X#4	PEG_R X4		VSS	PEG_TX 2	PEG_R X#3		VSS	PEG_TX #5	PEG_R X5		VSS	PEG_TX 1	VSS_NC TF		VCC_N CTF	VCC_N CTF	VSS		VSS	VCC_N CTF	VSS		VSS_NC TF	
R	PEG_TX 4	PEG_TX #4	VSS														RSVD			TEST2		VCC		VSS		
P		VSS													RSVD	RSVD			TV_DC ONSEL1				VSS		CFG0	
N	PEG_TX #3	PEG_TX 3	VSS		PEG_R X#2		PEG_TX #0	VSS	PEG_C OMPI		LVDS_V REFH	LVDS_V REFL	VSS			VSS	RSVD		CFG19	VSS			VSS	VCCD_ QDAC	CFG1	
M		VSS	VSS		PEG_R X2	VSS	PEG_TX 0		PEG_C OMPO	VSS							TV_DC ONSEL0			VCCD_ CRT				VSS		
L	PEG_R X#1	PEG_R X1	VSS						LVDS_V BG		LVDS_I BG		PM_DP RSTP#			PM_EXT _TS#0	CFG20		VSS	CFG18			VCCD_T VDAC	VSS	TVC_RT N	
K		VCCA_P EG_BG	VSSA_P EG_BG		VSS		PEG_CL K#	PEG_CL K				L_VDD_ EN				SDVO_ CTRL_D ATA			CRT_D DC_CLK				CRT_G REEN		TVC_DA C	
J	PEG_R X#0	PEG_R X0									VCCD_L VDS	L_BKLT _CTRL	VSS			PM_EXT _TS#1	VSS		VSS	VCC_SY NC			CRT_G REEN#	VSS	TVB_RT N	
H		VSS	VCCA_ DPLLB	DPLL_R EF_SSC LK	DPLL_R EF_SSC LK#		VSS			VCCD_L VDS			L_BKLT _EN				SDVO_ CTRL_C LK			CRT_BL UE				VSS		
G	LVDSA_ DATA#0	LVDSA_ DATA0		VSS			VSS	LVDSB_ DATA#0		VSS	PM_BM _BUSY#	ICH_SY NC#	CLKRE Q#			DPRSLP VR	CRT_D DC_DAT A		VSS	CRT_BL UE#			VSS	VSS	TVB_DA C	
F		VSS	LVDSA_ DATA#2	LVDSA_ DATA2								VSS				VSS			CRT_HS YNC				CRT_RE D		TVA_RT N	
E	LVDSA_ DATA#1	LVDSA_ DATA1			VSS			LVDSB_ DATA0		LVDSB_ CLK		L_CTRL _DATA	L_CTRL _CLK			GFX_VR _EN	GFX_VI D0		CRT_VS YNC	VSS			CRT_RE D#	VSS	TVA_DA C	
D			VSS		LVDSA_ DATA3	LVDSA_ CLK#	VSS	LVDSB_ CLK#					VSS				L_DDC_ DATA			VSS						
C	NC	VSS		LVDSA_ DATA#3		VSS	LVDSA_ CLK	LVDSB_ DATA3		DPLL_R EF_CLK #|	VSS	VCC_H V		GFX_VI D2	L_DDC_ CLK	VSS		RSVD	VSS	CRT_TV O_IREF			VSS	VSS	VCCA_T VB_DAC	
B	RSVD	NC	VCCA_ DPLLA		LVDSB_ DATA#1	VSS	LVDSB_ DATA#2	LVDSB_ DATA#3	VSS	DPLL_R EF_CLK	VSSA_L VDS	VCC_H V	GFX_VI D3	VSS	RSVD	RSVD	VSS	RSVD	VCCA_ CRT_DA C	VSSA_D AC_BG		VSS	VSS	VCCA_T VC_DA C	VCCA_T VB_DAC	
A	VSS_SC B6	NC	NC		LVDSB_ DATA1		LVDSB_ DATA2		VCC_TX _LVDS		VCCA_L VDS		GFX_VI D1		TEST1		RSVD		VCCA_ CRT_DA C			VCCA_ DAC_B G		VCCA_T VC_DA C		

Figure 24. Ballout Diagram (Top View) Lower Right Quadrant



15.2 Ball List (Listed by Interface)

15.2.1 Analog TV-out

Signal	Ball
TV_DCONSEL0	M35
TV_DCONSEL1	P33
TVA_DAC	E27

Signal	Ball
TVA_RTN	F27
TVB_DAC	G27
TVB_RTN	J27

Signal	Ball
TVC_DAC	K27
TVC_RTN	L27

15.2.2 CRT DAC

Signal	Ball
CRT_BLUE	H32
CRT_BLUE#	G32
CRT_GREEN	K29

Signal	Ball
CRT_GREEN#	J29
CRT_HSYNC	F33
CRT_RED	F29

Signal	Ball
CRT_RED#	E29
CRT_TVO_IREF	C32
CRT_VSYNC	E33

15.2.3 DDC and GMBus

Signal	Ball
CRT_DDC_CLK	K33
CRT_DDC_DATA	G35
L_CTRL_CLK	E39

Signal	Ball
L_CTRL_DATA	E40
L_DDC_CLK	C37
L_DDC_DATA	D35

Signal	Ball
SDVO_CTRL_CLK	H35
SDVO_CTRL_DATA	K36

15.2.4 DMI

Signal	Ball
DMI_RXN0	AN47
DMI_RXN1	AJ38
DMI_RXN2	AN42
DMI_RXN3	AN46
DMI_RXP0	AM47
DMI_RXP1	AJ39

Signal	Ball
DMI_RXP2	AN41
DMI_RXP3	AN45
DMI_TXN0	AJ46
DMI_TXN1	AJ41
DMI_TXN2	AM40

Signal	Ball
DMI_TXN3	AM44
DMI_TXP0	AJ47
DMI_TXP1	AJ42
DMI_TXP2	AM39
DMI_TXP3	AM43

15.2.5 Host Interface

Signal	Ball
H_A#10	G17
H_A#11	C14
H_A#12	K16
H_A#13	B13
H_A#14	L16
H_A#15	J17
H_A#16	B14
H_A#17	K19
H_A#18	P15
H_A#19	R17
H_A#20	B16
H_A#21	H20
H_A#22	L19
H_A#23	D17
H_A#24	M17
H_A#25	N16
H_A#26	J19
H_A#27	B18
H_A#28	E19
H_A#29	B17
H_A#3	J13
H_A#30	B15
H_A#31	E17
H_A#32	C18
H_A#33	A19
H_A#34	B19
H_A#35	N19
H_A#4	B11
H_A#5	C11
H_A#6	M11
H_A#7	C15
H_A#8	F16
H_A#9	L13
H_ADS#	G12
H_ADSTB#0	H17
H_ADSTB#1	G20

Signal	Ball
H_D#13	H5
H_D#14	P13
H_D#15	K9
H_D#16	M2
H_D#17	W10
H_D#18	Y8
H_D#19	V4
H_D#2	G7
H_D#20	M3
H_D#21	J1
H_D#22	N5
H_D#23	N3
H_D#24	W6
H_D#25	W9
H_D#26	N2
H_D#27	Y7
H_D#28	Y9
H_D#29	P4
H_D#3	M6
H_D#30	W3
H_D#31	N1
H_D#32	AD12
H_D#33	AE3
H_D#34	AD9
H_D#35	AC9
H_D#36	AC7
H_D#37	AC14
H_D#38	AD11
H_D#39	AC11
H_D#4	H7
H_D#40	AB2
H_D#41	AD7
H_D#42	AB1
H_D#43	Y3
H_D#44	AC6
H_D#45	AE2

Signal	Ball
H_D#56	AJ6
H_D#57	AE7
H_D#58	AJ7
H_D#59	AJ2
H_D#6	G4
H_D#60	AE5
H_D#61	AJ3
H_D#62	AH2
H_D#63	AH13
H_D#7	F3
H_D#8	N8
H_D#9	H2
H_DBSY#	C10
H_DEFER#	D6
H_DINV#0	K5
H_DINV#1	L2
H_DINV#2	AD13
H_DINV#3	AE13
H_DPWR#	H8
H_DRDY#	K7
H_DSTBN#0	M7
H_DSTBN#1	K3
H_DSTBN#2	AD2
H_DSTBN#3	AH11
H_DSTBP#0	L7
H_DSTBP#1	K2
H_DSTBP#2	AC2
H_DSTBP#3	AJ10
H_DVREF	A9
H_HIT#	E4
H_HITM#	C6
H_LOCK#	G10
H_RCOMP	C2
H_REQ#0	M14
H_REQ#1	E13
H_REQ#2	A11

Signal	Ball
H_AVREF	B9
H_BNR#	C8
H_BPRI#	E8
H_BREQ#	F12
H_CPURST#	B6
H_CPUSLP#	E5
H_D#0	E2
H_D#1	G2
H_D#10	M10
H_D#11	N12
H_D#12	N9

Signal	Ball
H_D#46	AC5
H_D#47	AG3
H_D#48	AJ9
H_D#49	AH8
H_D#5	H3
H_D#50	AJ14
H_D#51	AE9
H_D#52	AE11
H_D#53	AH12
H_D#54	AJ5
H_D#55	AH5

Signal	Ball
H_REQ#3	H13
H_REQ#4	B12
H_RS#0	E12
H_RS#1	D7
H_RS#2	D8
H_SCOMP	W1
H_SCOMP#	W2
H_SWING	B3
H_TRDY#	B7
THERMTRIP#	N20

15.2.6 LVDS

Signal	Ball
L_BKLT_CTRL	J40
L_BKLT_EN	H39
L_VDD_EN	K40
LVDS_IBG	L41
LVDS_VBG	L43
LVDS_VREFH	N41
LVDS_VREFL	N40
LVDSA_CLK	C45
LVDSA_CLK#	D46

Signal	Ball
LVDSA_DATA#0	G51
LVDSA_DATA#1	E51
LVDSA_DATA#2	F49
LVDSA_DATA#3	C48
LVDSA_DATA0	G50
LVDSA_DATA1	E50
LVDSA_DATA2	F48
LVDSA_DATA3	D47
LVDSB_CLK	E42

Signal	Ball
LVDSB_CLK#	D44
LVDSB_DATA#0	G44
LVDSB_DATA#1	B47
LVDSB_DATA#2	B45
LVDSB_DATA#3	B44
LVDSB_DATA0	E44
LVDSB_DATA1	A47
LVDSB_DATA2	A45
LVDSB_DATA3	C44

15.2.7 Intel® Management Engine Interface

Signal	Ball
CL_CLK	AM49
CL_DATA	AK50

Signal	Ball
CL_PWROK	AT43
CL_RST#	AN49

Signal	Ball
CL_VREF	AM50

15.2.8 Memory Interface

Signal	Ball
SA_BS0	BB19
SA_BS1	BK19
SA_BS2	BF29

Signal	Ball
SA_DQS#6	BC1
SA_DQS#7	AP2
SA_DQS0	AT46

Signal	Ball
SB_DQ47	BJ6
SB_DQ48	BF4
SB_DQ49	BH5

Signal	Ball
SA_CAS#	BL17
SA_DM0	AT45
SA_DM1	BD44
SA_DM2	BD42
SA_DM3	AW38
SA_DM4	AW13
SA_DM5	BG8
SA_DM6	AY5
SA_DM7	AN6
SA_DQ0	AR43
SA_DQ1	AW44
SA_DQ10	BG47
SA_DQ11	BJ45
SA_DQ12	BB47
SA_DQ13	BG50
SA_DQ14	BH49
SA_DQ15	BE45
SA_DQ16	AW43
SA_DQ17	BE44
SA_DQ18	BG42
SA_DQ19	BE40
SA_DQ2	BA45
SA_DQ20	BF44
SA_DQ21	BH45
SA_DQ22	BG40
SA_DQ23	BF40
SA_DQ24	AR40
SA_DQ25	AW40
SA_DQ26	AT39
SA_DQ27	AW36
SA_DQ28	AW41
SA_DQ29	AY41
SA_DQ3	AY46
SA_DQ30	AV38
SA_DQ31	AT38
SA_DQ32	AV13
SA_DQ33	AT13
SA_DQ34	AW11
SA_DQ35	AV11

Signal	Ball
SA_DQS1	BE48
SA_DQS2	BB43
SA_DQS3	BC37
SA_DQS4	BB16
SA_DQS5	BH6
SA_DQS6	BB2
SA_DQS7	AP3
SA_MA0	BJ19
SA_MA1	BD20
SA_MA10	BC19
SA_MA11	BE28
SA_MA12	BG30
SA_MA13	BJ16
SA_MA14	BJ29
SA_MA2	BK27
SA_MA3	BH28
SA_MA4	BL24
SA_MA5	BK28
SA_MA6	BJ27
SA_MA7	BJ25
SA_MA8	BL28
SA_MA9	BA28
SA_RAS#	BE18
SA_RCVEN#	AY20
SA_WE#	BA19
SB_BS0	AY17
SB_BS1	BG18
SB_BS2	BG36
SB_CAS#	BE17
SB_DM0	AR50
SB_DM1	BD49
SB_DM2	BK45
SB_DM3	BL39
SB_DM4	BH12
SB_DM5	BJ7
SB_DM6	BF3
SB_DM7	AW2
SB_DQ0	AP49
SB_DQ1	AR51

Signal	Ball
SB_DQ5	AN50
SB_DQ50	BG1
SB_DQ51	BC2
SB_DQ52	BK3
SB_DQ53	BE4
SB_DQ54	BD3
SB_DQ55	BJ2
SB_DQ56	BA3
SB_DQ57	BB3
SB_DQ58	AR1
SB_DQ59	AT3
SB_DQ6	AV50
SB_DQ60	AY2
SB_DQ61	AY3
SB_DQ62	AU2
SB_DQ63	AT2
SB_DQ7	AV49
SB_DQ8	BA50
SB_DQ9	BB50
SB_DQS#0	AU50
SB_DQS#1	BC50
SB_DQS#2	BL45
SB_DQS#3	BK38
SB_DQS#4	BK12
SB_DQS#5	BK7
SB_DQS#6	BF2
SB_DQS#7	AV3
SB_DQS0	AT50
SB_DQS1	BD50
SB_DQS2	BK46
SB_DQS3	BK39
SB_DQS4	BJ12
SB_DQS5	BL7
SB_DQS6	BE2
SB_DQS7	AV2
SB_MA0	BC18
SB_MA1	BG28
SB_MA10	BG17
SB_MA11	BE37

Signal	Ball
SA_DQ36	AU15
SA_DQ37	AT11
SA_DQ38	BA13
SA_DQ39	BA11
SA_DQ4	AR41
SA_DQ40	BE10
SA_DQ41	BD10
SA_DQ42	BD8
SA_DQ43	AY9
SA_DQ44	BG10
SA_DQ45	AW9
SA_DQ46	BD7
SA_DQ47	BB9
SA_DQ48	BB5
SA_DQ49	AY7
SA_DQ5	AR45
SA_DQ50	AT5
SA_DQ51	AT7
SA_DQ52	AY6
SA_DQ53	BB7
SA_DQ54	AR5
SA_DQ55	AR8
SA_DQ56	AR9
SA_DQ57	AN3
SA_DQ58	AM8
SA_DQ59	AN10
SA_DQ6	AT42
SA_DQ60	AT9
SA_DQ61	AN9
SA_DQ62	AM9
SA_DQ63	AN11
SA_DQ7	AW47
SA_DQ8	BB45
SA_DQ9	BF48
SA_DQS#0	AT47
SA_DQS#1	BD47
SA_DQS#2	BC41

Signal	Ball
SB_DQ10	BA49
SB_DQ11	BE50
SB_DQ12	BA51
SB_DQ13	AY49
SB_DQ14	BF50
SB_DQ15	BF49
SB_DQ16	BJ50
SB_DQ17	BJ44
SB_DQ18	BJ43
SB_DQ19	BL43
SB_DQ2	AW50
SB_DQ20	BK47
SB_DQ21	BK49
SB_DQ22	BK43
SB_DQ23	BK42
SB_DQ24	BJ41
SB_DQ25	BL41
SB_DQ26	BJ37
SB_DQ27	BJ36
SB_DQ28	BK41
SB_DQ29	BJ40
SB_DQ3	AW51
SB_DQ30	BL35
SB_DQ31	BK37
SB_DQ32	BK13
SB_DQ33	BE11
SB_DQ34	BK11
SB_DQ35	BC11
SB_DQ36	BC13
SB_DQ37	BE12
SB_DQ38	BC12
SB_DQ39	BG12
SB_DQ4	AN51
SB_DQ40	BJ10
SB_DQ41	BL9
SB_DQ42	BK5
SB_DQ43	BL5

Signal	Ball
SB_MA12	BA39
SB_MA13	BG13
SB_MA14	BE24
SB_MA2	BG25
SB_MA3	AW17
SB_MA4	BF25
SB_MA5	BE25
SB_MA6	BA29
SB_MA7	BC28
SB_MA8	AY28
SB_MA9	BD37
SB_RAS#	AV16
SB_RCVEN#	AY18
SB_WE#	BC17
SM_CK#0	AW30
SM_CK#1	BA23
SM_CK#3	AW25
SM_CK#4	AW23
SM_CK0	AV29
SM_CK1	BB23
SM_CK3	BA25
SM_CK4	AV23
SM_CKE0	BE29
SM_CKE1	AY32
SM_CKE3	BD39
SM_CKE4	BG37
SM_CS#0	BG20
SM_CS#1	BK16
SM_CS#2	BG16
SM_CS#3	BE13
SM_ODT0	BH18
SM_ODT1	BJ15
SM_ODT2	BJ14
SM_ODT3	BE16
SM_RCOMP	BL15
SM_RCOMP#	BK14
SM_RCOMP_VOH	BK31

Signal	Ball
SA_DQS#3	BA37
SA_DQS#4	BA16
SA_DQS#5	BH7

Signal	Ball
SB_DQ44	BK9
SB_DQ45	BK10
SB_DQ46	BJ8

Signal	Ball
SM_RCOMP_VOL	BL31
SM_VREF	AW4
SM_VREF	AR49

15.2.9 No Connects

Signal	Ball
NC	BJ51
NC	BK2
NC	E1
NC	A5
NC	C51
NC	B50

Signal	Ball
NC	A50
NC	A49
NC	BK51
NC	BK50
NC	BL50

Signal	Ball
NC	BL49
NC	BL3
NC	BL2
NC	BK1
NC	BJ1

15.2.10 PCI Express Based Graphics

Signal	Ball
PEG_COMPI	N43
PEG_COMPO	M43
PEG_RX#0	J51
PEG_RX#1	L51
PEG_RX#10	AD44
PEG_RX#11	AD40
PEG_RX#12	AG46
PEG_RX#13	AH49
PEG_RX#14	AG45
PEG_RX#15	AG41
PEG_RX#2	N47
PEG_RX#3	T45
PEG_RX#4	T50
PEG_RX#5	U40
PEG_RX#6	Y44
PEG_RX#7	Y40
PEG_RX#8	AB51
PEG_RX#9	W49
PEG_RX0	J50

Signal	Ball
PEG_RX12	AH47
PEG_RX13	AG49
PEG_RX14	AH45
PEG_RX15	AG42
PEG_RX2	M47
PEG_RX3	U44
PEG_RX4	T49
PEG_RX5	T41
PEG_RX6	W45
PEG_RX7	W41
PEG_RX8	AB50
PEG_RX9	Y48
PEG_TX#0	N45
PEG_TX#1	U39
PEG_TX#10	AC46
PEG_TX#11	AC49
PEG_TX#12	AC42
PEG_TX#13	AH39
PEG_TX#14	AE49

Signal	Ball
PEG_TX#4	R50
PEG_TX#5	T42
PEG_TX#6	Y43
PEG_TX#7	W46
PEG_TX#8	W38
PEG_TX#9	AD39
PEG_TX0	M45
PEG_TX1	T38
PEG_TX10	AD47
PEG_TX11	AC50
PEG_TX12	AD43
PEG_TX13	AG39
PEG_TX14	AE50
PEG_TX15	AH43
PEG_TX2	T46
PEG_TX3	N50
PEG_TX4	R51
PEG_TX5	U43
PEG_TX6	W42

Signal	Ball
PEG_RX1	L50
PEG_RX10	AC45
PEG_RX11	AC41

Signal	Ball
PEG_TX#15	AH44
PEG_TX#2	U47
PEG_TX#3	N51

Signal	Ball
PEG_TX7	Y47
PEG_TX8	Y39
PEG_TX9	AC38

15.2.11 PLL

Signal	Ball
DPLL_REF_CLK	B42
DPLL_REF_CLK#	C42
DPLL_REF_SSCLK	H48

Signal	Ball
DPLL_REF_SSCLK#	H47
HPLL_CLK	AM5
HPLL_CLK#	AM7

Signal	Ball
PEG_CLK	K44
PEG_CLK#	K45

15.2.12 Power and Ground

Signal	Ball
VCC	AT35
VCC	AT34
VCC	AK32
VCC	AJ31
VCC	AJ28
VCC	AH32
VCC	AH31
VCC	AH29
VCC	AH28
VCC	AF32
VCC	AC32
VCC	AC31
VCC	R30
VCC_AXD	AU28
VCC_AXD	AU24
VCC_AXD	AT30
VCC_AXD	AT29
VCC_AXD	AT25
VCC_AXD	AT23
VCC_AXD_NCTF	AR29
VCC_AXF	B23
VCC_AXF	B21
VCC_AXF	A21
VCC_AXG	AN14

Signal	Ball
VCC_SM	BK35
VCC_SM	BK34
VCC_SM	BK33
VCC_SM	BK32
VCC_SM	BJ34
VCC_SM	BJ33
VCC_SM	BJ32
VCC_SM	BH35
VCC_SM	BH34
VCC_SM	BH32
VCC_SM	BG35
VCC_SM	BG33
VCC_SM	BG32
VCC_SM	BF34
VCC_SM	BF33
VCC_SM	BE35
VCC_SM	BE33
VCC_SM	BE32
VCC_SM	BD35
VCC_SM	BD32
VCC_SM	BC35
VCC_SM	BC33
VCC_SM	BC32
VCC_SM	BB33

Signal	Ball
VSS	AH9
VSS	AH7
VSS	AH3
VSS	AG50
VSS	AG47
VSS	AG43
VSS	AG38
VSS	AG2
VSS	AF31
VSS	AF29
VSS	AF28
VSS	AF24
VSS	AF23
VSS	AF20
VSS	AE14
VSS	AE10
VSS	AE6
VSS	AD50
VSS	AD49
VSS	AD45
VSS	AD41
VSS	AD32
VSS	AD29
VSS	AD26

Signal	Ball
VCC_AXG	AJ20
VCC_AXG	AH26
VCC_AXG	AH24
VCC_AXG	AH23
VCC_AXG	AH21
VCC_AXG	AH20
VCC_AXG	AF26
VCC_AXG	AF21
VCC_AXG	AD31
VCC_AXG	AD28
VCC_AXG	AD24
VCC_AXG	AD23
VCC_AXG	AD20
VCC_AXG	AC29
VCC_AXG	AC28
VCC_AXG	AC26
VCC_AXG	AC24
VCC_AXG	AC23
VCC_AXG	AC21
VCC_AXG	AC20
VCC_AXG	AB29
VCC_AXG	AB24
VCC_AXG	AB21
VCC_AXG	AA31
VCC_AXG	AA28
VCC_AXG	AA26
VCC_AXG	AA23
VCC_AXG	AA20
VCC_AXG	Y12
VCC_AXG	W14
VCC_AXG	W13
VCC_AXG	T14
VCC_AXG	R20
VCC_AXG_NCTF	AR26
VCC_AXG_NCTF	AR24
VCC_AXG_NCTF	AR23
VCC_AXG_NCTF	AR21
VCC_AXG_NCTF	AR20
VCC_AXG_NCTF	AP24

Signal	Ball
VCC_SM	BA35
VCC_SM	BA33
VCC_SM	BA32
VCC_SM	AY35
VCC_SM	AW35
VCC_SM	AW33
VCC_SM	AV33
VCC_SM	AU35
VCC_SM	AU33
VCC_SM	AU32
VCC_SM	AU30
VCC_SM_CK	BK24
VCC_SM_CK	BK23
VCC_SM_CK	BJ24
VCC_SM_CK	BJ23
VCC_SM_LF1	AW45
VCC_SM_LF2	BC39
VCC_SM_LF3	BE39
VCC_SM_LF4	BD17
VCC_SM_LF5	BD4
VCC_SM_LF6	AW8
VCC_SM_LF7	AT6
VCC_SYNC	J32
VCC_TX_LVDS	A43
VCCA_CRT_DAC	B33
VCCA_CRT_DAC	A33
VCCA_DAC_BG	A30
VCCA_DPLLA	B49
VCCA_DPLLB	H49
VCCA_HPLL	AL2
VCCA_LVDS	A41
VCCA_MPLL	AM2
VCCA_PEG_BG	K50
VCCA_PEG_PLL	U51
VCCA_SM	AW18
VCCA_SM	AV19
VCCA_SM	AU19
VCCA_SM	AU18
VCCA_SM	AU17

Signal	Ball
VSS	AD21
VSS	AD8
VSS	AD5
VSS	AD3
VSS	AD1
VSS	AC47
VSS	AC43
VSS	AC39
VSS	AC13
VSS	AC10
VSS	AC3
VSS	AB32
VSS	AB31
VSS	AB28
VSS	AB26
VSS	AB23
VSS	AB20
VSS	AA32
VSS	AA29
VSS	AA24
VSS	AA21
VSS	Y50
VSS	Y49
VSS	Y45
VSS	Y41
VSS	Y13
VSS	Y11
VSS	Y5
VSS	Y2
VSS	W47
VSS	W43
VSS	W39
VSS	W11
VSS	W7
VSS	W5
VSS	V3
VSS	V2
VSS	U50
VSS	U45

Signal	Ball
VCC_AXG_NCTF	AP23
VCC_AXG_NCTF	AP21
VCC_AXG_NCTF	AP20
VCC_AXG_NCTF	AP19
VCC_AXG_NCTF	AP17
VCC_AXG_NCTF	AP16
VCC_AXG_NCTF	AP15
VCC_AXG_NCTF	AM23
VCC_AXG_NCTF	AM21
VCC_AXG_NCTF	AM20
VCC_AXG_NCTF	AM19
VCC_AXG_NCTF	AM16
VCC_AXG_NCTF	AM15
VCC_AXG_NCTF	AL23
VCC_AXG_NCTF	AL21
VCC_AXG_NCTF	AL20
VCC_AXG_NCTF	AL19
VCC_AXG_NCTF	AL17
VCC_AXG_NCTF	AL16
VCC_AXG_NCTF	AK19
VCC_AXG_NCTF	AK16
VCC_AXG_NCTF	AJ19
VCC_AXG_NCTF	AJ17
VCC_AXG_NCTF	AJ16
VCC_AXG_NCTF	AH19
VCC_AXG_NCTF	AH17
VCC_AXG_NCTF	AH16
VCC_AXG_NCTF	AH15
VCC_AXG_NCTF	AF19
VCC_AXG_NCTF	AF16
VCC_AXG_NCTF	AD17
VCC_AXG_NCTF	AD16
VCC_AXG_NCTF	AD15
VCC_AXG_NCTF	AC19
VCC_AXG_NCTF	AC17
VCC_AXG_NCTF	AC16
VCC_AXG_NCTF	AB19
VCC_AXG_NCTF	AB16
VCC_AXG_NCTF	AA17

Signal	Ball
VCCA_SM	AT22
VCCA_SM	AT21
VCCA_SM	AT19
VCCA_SM	AT18
VCCA_SM	AT17
VCCA_SM_CK	BC29
VCCA_SM_CK	BB29
VCCA_SM_NCTF	AR17
VCCA_SM_NCTF	AR16
VCCA_TVA_DAC	C25
VCCA_TVA_DAC	B25
VCCA_TVB_DAC	C27
VCCA_TVB_DAC	B27
VCCA_TVC_DAC	B28
VCCA_TVC_DAC	A28
VCCD_CRT	M32
VCCD_HPLL	AN2
VCCD_LVDS	J41
VCCD_LVDS	H42
VCCD_PEG_PLL	U48
VCCD_TVDAC	L29
VCCD_QDAC	N28
VSS	T33
VSS	R28
VSS	T31
VSS	T29
VSS	BL47
VSS	BL37
VSS	BL22
VSS	BL19
VSS	BL13
VSS	BL11
VSS	BK44
VSS	BK40
VSS	BK36
VSS	BK29
VSS	BK25
VSS	BK17
VSS	BK15

Signal	Ball
VSS	U41
VSS	T47
VSS	T43
VSS	T39
VSS	R49
VSS	P50
VSS	P29
VSS	P23
VSS	P19
VSS	P3
VSS	P2
VSS	N49
VSS	N44
VSS	N39
VSS	N36
VSS	N32
VSS	N29
VSS	N17
VSS	N14
VSS	N11
VSS	N7
VSS	M50
VSS	M49
VSS	M46
VSS	M42
VSS	M28
VSS	M9
VSS	M5
VSS	L49
VSS	L33
VSS	L28
VSS	L24
VSS	L20
VSS	L17
VSS	L3
VSS	L1
VSS	K47
VSS	K12
VSS	K8

Signal	Ball
VCC_AXG_NCTF	AA16
VCC_AXG_NCTF	Y31
VCC_AXG_NCTF	Y29
VCC_AXG_NCTF	Y28
VCC_AXG_NCTF	Y26
VCC_AXG_NCTF	Y24
VCC_AXG_NCTF	Y23
VCC_AXG_NCTF	Y21
VCC_AXG_NCTF	Y20
VCC_AXG_NCTF	Y19
VCC_AXG_NCTF	Y17
VCC_AXG_NCTF	Y16
VCC_AXG_NCTF	Y15
VCC_AXG_NCTF	V29
VCC_AXG_NCTF	V28
VCC_AXG_NCTF	V26
VCC_AXG_NCTF	V24
VCC_AXG_NCTF	V23
VCC_AXG_NCTF	V21
VCC_AXG_NCTF	V20
VCC_AXG_NCTF	V19
VCC_AXG_NCTF	V17
VCC_AXG_NCTF	V16
VCC_AXG_NCTF	U26
VCC_AXG_NCTF	U23
VCC_AXG_NCTF	U21
VCC_AXG_NCTF	U20
VCC_AXG_NCTF	U19
VCC_AXG_NCTF	U17
VCC_AXG_NCTF	U16
VCC_AXG_NCTF	U15
VCC_AXG_NCTF	T25
VCC_AXG_NCTF	T23
VCC_AXG_NCTF	T22
VCC_AXG_NCTF	T21
VCC_AXG_NCTF	T19
VCC_AXG_NCTF	T18
VCC_AXG_NCTF	T17
VCC_AXM	AT33

Signal	Ball
VSS	BK8
VSS	BK6
VSS	BJ46
VSS	BJ42
VSS	BJ38
VSS	BJ13
VSS	BJ11
VSS	BJ4
VSS	BH46
VSS	BH44
VSS	BH30
VSS	BH17
VSS	BH8
VSS	BG51
VSS	BG48
VSS	BG39
VSS	BG29
VSS	BG24
VSS	BG19
VSS	BG5
VSS	BG2
VSS	BF36
VSS	BF16
VSS	BF12
VSS	BE51
VSS	BE42
VSS	BE30
VSS	BE23
VSS	BE19
VSS	BE8
VSS	BE1
VSS	BD48
VSS	BD45
VSS	BD28
VSS	BD13
VSS	BD5
VSS	BD2
VSS	BC51
VSS	BC40

Signal	Ball
VSS	J39
VSS	J35
VSS	J33
VSS	J28
VSS	J24
VSS	J16
VSS	J11
VSS	J2
VSS	H50
VSS	H45
VSS	H28
VSS	H24
VSS	H4
VSS	G48
VSS	G45
VSS	G42
VSS	G33
VSS	G29
VSS	G28
VSS	G24
VSS	G19
VSS	G16
VSS	G13
VSS	G8
VSS	G1
VSS	F50
VSS	F40
VSS	F36
VSS	F19
VSS	F4
VSS	E47
VSS	E32
VSS	E28
VSS	E24
VSS	E16
VSS	E10
VSS	D49
VSS	D45
VSS	D39

Signal	Ball
VCC_AXM	AT31
VCC_AXM	AK29
VCC_AXM	AK24
VCC_AXM	AK23
VCC_AXM	AJ26
VCC_AXM	AJ23
VCC_AXM_NCTF	AR33
VCC_AXM_NCTF	AR32
VCC_AXM_NCTF	AR31
VCC_AXM_NCTF	AP33
VCC_AXM_NCTF	AP32
VCC_AXM_NCTF	AP31
VCC_AXM_NCTF	AP29
VCC_AXM_NCTF	AM33
VCC_AXM_NCTF	AM32
VCC_AXM_NCTF	AM31
VCC_AXM_NCTF	AM29
VCC_AXM_NCTF	AM28
VCC_AXM_NCTF	AM26
VCC_AXM_NCTF	AL32
VCC_AXM_NCTF	AL31
VCC_AXM_NCTF	AL29
VCC_AXM_NCTF	AL28
VCC_AXM_NCTF	AL26
VCC_AXM_NCTF	AL24
VCC_DMI	AJ50
VCC_HV	C40
VCC_HV	B40
VCC_NCTF	AR36
VCC_NCTF	AR35
VCC_NCTF	AP36
VCC_NCTF	AP35
VCC_NCTF	AM35
VCC_NCTF	AL35
VCC_NCTF	AL33
VCC_NCTF	AK37
VCC_NCTF	AK36
VCC_NCTF	AK35
VCC_NCTF	AK33

Signal	Ball
VSS	BC36
VSS	BC25
VSS	BC24
VSS	BC16
VSS	BB49
VSS	BB44
VSS	BB40
VSS	BB25
VSS	BB12
VSS	BB8
VSS	BA24
VSS	BA18
VSS	BA17
VSS	BA2
VSS	BA1
VSS	AY50
VSS	AY47
VSS	AY45
VSS	AY43
VSS	AY42
VSS	AY37
VSS	AY24
VSS	AY10
VSS	AW32
VSS	AW29
VSS	AW24
VSS	AW16
VSS	AW12
VSS	AW7
VSS	AW5
VSS	AW1
VSS	AV48
VSS	AV39
VSS	AV25
VSS	AU51
VSS	AU49
VSS	AU36
VSS	AU29
VSS	AU23

Signal	Ball
VSS	D32
VSS	D24
VSS	D13
VSS	D3
VSS	C50
VSS	C46
VSS	C41
VSS	C36
VSS	C33
VSS	C29
VSS	C28
VSS	C19
VSS	C16
VSS	C12
VSS	C7
VSS	B46
VSS	B43
VSS	B38
VSS	B35
VSS	B30
VSS	B29
VSS	B24
VSS	B20
VSS	B10
VSS	B8
VSS	B5
VSS	A24
VSS	A17
VSS	A15
VSS	A13
VSS_NCTF	AR28
VSS_NCTF	AR19
VSS_NCTF	AR15
VSS_NCTF	AP28
VSS_NCTF	AP26
VSS_NCTF	AM24
VSS_NCTF	AM17
VSS_NCTF	AK17
VSS_NCTF	AF35

Signal	Ball
VCC_NCTF	AJ36
VCC_NCTF	AJ35
VCC_NCTF	AJ33
VCC_NCTF	AH37
VCC_NCTF	AH36
VCC_NCTF	AH35
VCC_NCTF	AH33
VCC_NCTF	AF36
VCC_NCTF	AF33
VCC_NCTF	AD36
VCC_NCTF	AD35
VCC_NCTF	AD33
VCC_NCTF	AC36
VCC_NCTF	AC35
VCC_NCTF	AC33
VCC_NCTF	AB37
VCC_NCTF	AB36
VCC_NCTF	AB33
VCC_NCTF	AA36
VCC_NCTF	AA35
VCC_NCTF	AA33
VCC_NCTF	Y37
VCC_NCTF	Y36
VCC_NCTF	Y35
VCC_NCTF	Y33
VCC_NCTF	Y32
VCC_NCTF	V37
VCC_NCTF	V36
VCC_NCTF	V33
VCC_NCTF	V32
VCC_NCTF	U36
VCC_NCTF	U35
VCC_NCTF	U33
VCC_NCTF	U32
VCC_NCTF	U31
VCC_NCTF	U29
VCC_NCTF	T35
VCC_NCTF	T34
VCC_NCTF	T30

Signal	Ball
VSS	AU3
VSS	AU1
VSS	AT49
VSS	AT41
VSS	AT27
VSS	AT14
VSS	AT10
VSS	AR47
VSS	AR44
VSS	AR39
VSS	AR11
VSS	AR7
VSS	AR2
VSS	AP50
VSS	AP48
VSS	AP4
VSS	AN43
VSS	AN39
VSS	AN38
VSS	AN7
VSS	AN5
VSS	AN1
VSS	AM45
VSS	AM41
VSS	AM13
VSS	AM11
VSS	AM4
VSS	AM3
VSS	AL1
VSS	AK51
VSS	AK31
VSS	AK28
VSS	AK26
VSS	AK21
VSS	AK20
VSS	AJ49
VSS	AJ45
VSS	AJ43
VSS	AJ32

Signal	Ball
VSS_NCTF	AF17
VSS_NCTF	AD37
VSS_NCTF	AD19
VSS_NCTF	AB35
VSS_NCTF	AB17
VSS_NCTF	AA19
VSS_NCTF	V35
VSS_NCTF	V31
VSS_NCTF	U28
VSS_NCTF	U24
VSS_NCTF	T37
VSS_NCTF	T27
VSS_SCB1	A3
VSS_SCB2	B2
VSS_SCB3	C1
VSS_SCB4	BL1
VSS_SCB5	BL51
VSS_SCB6	A51
VSSA_DAC_BG	B32
VSSA_LVDS	B41
VSSA_PEG_BG	K49
VTT	U13
VTT	U12
VTT	U11
VTT	U9
VTT	U8
VTT	U7
VTT	U5
VTT	U3
VTT	U2
VTT	U1
VTT	T13
VTT	T11
VTT	T10
VTT	T9
VTT	T7
VTT	T6
VTT	T5
VTT	T3

Signal	Ball
VCC_PEG	AD51
VCC_PEG	W51
VCC_PEG	W50
VCC_PEG	V50
VCC_PEG	V49
VCC_RXR_DMI	AH51
VCC_RXR_DMI	AH50
VCC_SM	BL33

Signal	Ball
VSS	AJ29
VSS	AJ24
VSS	AJ21
VSS	AJ13
VSS	AJ11
VSS	AH41
VSS	AH40

Signal	Ball
VTT	T2
VTT	R3
VTT	R2
VTT	R1
VTTLF1	A7
VTTLF2	F2
VTTLF3	AH1

15.2.13 Reserved and Test

Signal	Ball
RSVD	A35
RSVD	B37
RSVD	B36
RSVD	B34
RSVD	C34
RSVD	BF23
RSVD	BG23
RSVD	BJ20
RSVD	BK22
RSVD	BC23
RSVD	BD24
RSVD	BH39
RSVD	AR12

Signal	Ball
RSVD	BF19
RSVD	BH20
RSVD	BK18
RSVD	BJ18
RSVD	AW20
RSVD	BK20
RSVD	P36
RSVD	P37
RSVD	R35
RSVD	N35
RSVD	J12
RSVD	H10
RSVD	AR13

Signal	Ball
RSVD	AM12
RSVD	AN13
RSVD	AR37
RSVD	AM36
RSVD	AL36
RSVD	AM37
RSVD	D20
RSVD	B51
TEST1	A37
TEST2	R32

15.2.14 Strappings

Signal	Ball
CFG0	P27
CFG1	N27
CFG3	C21
CFG4	C23
CFG5	F23
CFG6	N23
CFG7	G23

Signal	Ball
CFG8	J20
CFG9	C20
CFG10	R24
CFG11	L23
CFG12	J23
CFG13	E23
CFG14	E20

Signal	Ball
CFG15	K23
CFG16	M20
CFG17	M24
CFG18	L32
CFG19	N33
CFG2	N24
CFG20	L35

15.2.15 Reset and Miscellaneous

Signal	Ball
CLKREQ#	G39
DPRSLPVR	G36
GFX_VID0	E35
GFX_VID1	A39
GFX_VID2	C38

Signal	Ball
GFX_VID3	B39
GFX_VR_EN	E36
ICH_SYNC#	G40
PMSYNC# (PM_BM_BUSY#)	G41
PM_DPRSTP#	L39

Signal	Ball
PM_EXT_TS#0	L36
PM_EXT_TS#1	J36
PWROK	AW49
RSTIN#	AV20

15.3 Ball List (Listed by Ball)

Ball	Signal
A11	H_REQ#2
A13	VSS
A15	VSS
A17	VSS
A19	H_A#33
A21	VCC_AXF
A24	VSS
A28	VCCA_TVC_DAC
A3	VSS_SCB1
A30	VCCA_DAC_BG
A33	VCCA_CRT_DAC
A35	RSVD
A37	TEST1
A39	GFX_VID1
A41	VCCA_LVDS
A43	VCC_TX_LVDS
A45	LVDSB_DATA2
A47	LVDSB_DATA1
A49	NC
A5	NC
A50	NC
A51	VSS_SCB6
A7	VTTLF1
A9	H_DVREF
B10	VSS

Ball	Signal
V16	VCC_AXG_NCTF
V17	VCC_AXG_NCTF
V19	VCC_AXG_NCTF
V2	VSS
V20	VCC_AXG_NCTF
V21	VCC_AXG_NCTF
V23	VCC_AXG_NCTF
V24	VCC_AXG_NCTF
V26	VCC_AXG_NCTF
V28	VCC_AXG_NCTF
V29	VCC_AXG_NCTF
V3	VSS
V31	VSS_NCTF
V32	VCC_NCTF
V33	VCC_NCTF
V35	VSS_NCTF
V36	VCC_NCTF
V37	VCC_NCTF
V4	H_D#19
V49	VCC_PEG
V50	VCC_PEG
W1	H_SCOMP
W10	H_D#17
W11	VSS
W13	VCC_AXG

Ball	Signal
AR37	RSVD
AR39	VSS
AR40	SA_DQ24
AR41	SA_DQ4
AR43	SA_DQ0
AR44	VSS
AR45	SA_DQ5
AR47	VSS
AR49	SM_VREF
AR5	SA_DQ54
AR50	SB_DM0
AR51	SB_DQ1
AR7	VSS
AR8	SA_DQ55
AR9	SA_DQ56
AT10	VSS
AT11	SA_DQ37
AT13	SA_DQ33
AT14	VSS
AT17	VCCA_SM
AT18	VCCA_SM
AT19	VCCA_SM
AT2	SB_DQ63
AT21	VCCA_SM
AT22	VCCA_SM

Ball	Signal
B11	H_A#4
B12	H_REQ#4
B13	H_A#13
B14	H_A#16
B15	H_A#30
B16	H_A#20
B17	H_A#29
B18	H_A#27
B19	H_A#34
B2	VSS_SCB2
B20	VSS
B21	VCC_AXF
B23	VCC_AXF
B24	VSS
B25	VCCA_TVA_DAC
B27	VCCA_TVB_DAC
B28	VCCA_TVC_DAC
B29	VSS
B3	H_SWING
B30	VSS
B32	VSSA_DAC_BG
B33	VCCA_CRT_DAC
B34	RSVD
B35	VSS
B36	RSVD
B37	RSVD
B38	VSS
B39	GFX_VID3
B40	VCC_HV
B41	VSSA_LVDS
B42	DPLL_REF_CLK
B43	VSS
B44	LVDSB_DATA#3
B45	LVDSB_DATA#2
B46	VSS
B47	LVDSB_DATA#1
B49	VCCA_DPLLA
B5	VSS
B50	NC

Ball	Signal
W14	VCC_AXG
W2	H_SCOMP#
W3	H_D#30
W38	PEG_TX#8
W39	VSS
W41	PEG_RX7
W42	PEG_TX6
W43	VSS
W45	PEG_RX6
W46	PEG_TX#7
W47	VSS
W49	PEG_RX#9
W5	VSS
W50	VCC_PEG
W51	VCC_PEG
W6	H_D#24
W7	VSS
W9	H_D#25
Y11	VSS
Y12	VCC_AXG
Y13	VSS
Y15	VCC_AXG_NCTF
Y16	VCC_AXG_NCTF
Y17	VCC_AXG_NCTF
Y19	VCC_AXG_NCTF
Y2	VSS
Y20	VCC_AXG_NCTF
Y21	VCC_AXG_NCTF
Y23	VCC_AXG_NCTF
Y24	VCC_AXG_NCTF
Y26	VCC_AXG_NCTF
Y28	VCC_AXG_NCTF
Y29	VCC_AXG_NCTF
Y3	H_D#43
Y31	VCC_AXG_NCTF
Y32	VCC_NCTF
Y33	VCC_NCTF
Y35	VCC_NCTF
Y36	VCC_NCTF

Ball	Signal
AT23	VCC_AXD
AT25	VCC_AXD
AT27	VSS
AT29	VCC_AXD
AT3	SB_DQ59
AT30	VCC_AXD
AT31	VCC_AXM
AT33	VCC_AXM
AT34	VCC
AT35	VCC
AT38	SA_DQ31
AT39	SA_DQ26
AT41	VSS
AT42	SA_DQ6
AT43	CL_PWROK
AT45	SA_DM0
AT46	SA_DQS0
AT47	SA_DQS#0
AT49	VSS
AT5	SA_DQ50
AT50	SB_DQS0
AT6	VCC_SM_LF7
AT7	SA_DQ51
AT9	SA_DQ60
AU1	VSS
AU15	SA_DQ36
AU17	VCCA_SM
AU18	VCCA_SM
AU19	VCCA_SM
AU2	SB_DQ62
AU23	VSS
AU24	VCC_AXD
AU28	VCC_AXD
AU29	VSS
AU3	VSS
AU30	VCC_SM
AU32	VCC_SM
AU33	VCC_SM
AU35	VCC_SM

Ball	Signal
B51	RSVD
B6	H_CPURST#
B7	H_TRDY#
B8	VSS
B9	H_AVREF
C1	VSS_SCB3
C10	H_DBSY#
C11	H_A#5
C12	VSS
C14	H_A#11
C15	H_A#7
C16	VSS
C18	H_A#32
C19	VSS
C2	H_RCOMP
C20	CFG9
C21	CFG3
C23	CFG4
C25	VCCA_TVA_DAC
C27	VCCA_TVB_DAC
C28	VSS
C29	VSS
C32	CRT_TVO_IREF
C33	VSS
C34	RSVD
C36	VSS
C37	L_DDC_CLK
C38	GFX_VID2
C40	VCC_HV
C41	VSS
C42	DPLL_REF_CLK#
C44	LVDSB_DATA3
C45	LVDSA_CLK
C46	VSS
C48	LVDSA_DATA#3
C50	VSS
C51	NC
C6	H_HITM#
C7	VSS

Ball	Signal
Y37	VCC_NCTF
Y39	PEG_TX8
Y40	PEG_RX#7
Y41	VSS
Y43	PEG_TX#6
Y44	PEG_RX#6
Y45	VSS
Y47	PEG_TX7
Y48	PEG_RX9
Y49	VSS
Y5	VSS
Y50	VSS
Y7	H_D#27
Y8	H_D#18
Y9	H_D#28
AA16	VCC_AXG_NCTF
AA17	VCC_AXG_NCTF
AA19	VSS_NCTF
AA20	VCC_AXG
AA21	VSS
AA23	VCC_AXG
AA24	VSS
AA26	VCC_AXG
AA28	VCC_AXG
AA29	VSS
AA31	VCC_AXG
AA32	VSS
AA33	VCC_NCTF
AA35	VCC_NCTF
AA36	VCC_NCTF
AB1	H_D#42
AB16	VCC_AXG_NCTF
AB17	VSS_NCTF
AB19	VCC_AXG_NCTF
AB2	H_D#40
AB20	VSS
AB21	VCC_AXG
AB23	VSS
AB24	VCC_AXG

Ball	Signal
AU36	VSS
AU49	VSS
AU50	SB_DQS#0
AU51	VSS
AV11	SA_DQ35
AV13	SA_DQ32
AV16	SB_RAS#
AV19	VCCA_SM
AV2	SB_DQS7
AV20	RSTIN#
AV23	SM_CK4
AV25	VSS
AV29	SM_CK0
AV3	SB_DQS#7
AV33	VCC_SM
AV38	SA_DQ30
AV39	VSS
AV48	VSS
AV49	SB_DQ7
AV50	SB_DQ6
AW1	VSS
AW11	SA_DQ34
AW12	VSS
AW13	SA_DM4
AW16	VSS
AW17	SB_MA3
AW18	VCCA_SM
AW2	SB_DM7
AW20	RSVD
AW23	SM_CK#4
AW24	VSS
AW25	SM_CK#3
AW29	VSS
AW30	SM_CK#0
AW32	VSS
AW33	VCC_SM
AW35	VCC_SM
AW36	SA_DQ27
AW38	SA_DM3

Ball	Signal
C8	H_BNR#
D13	VSS
D17	H_A#23
D20	RSVD
D24	VSS
D3	VSS
D32	VSS
D35	L_DDC_DATA
D39	VSS
D44	LVDSB_CLK#
D45	VSS
D46	LVDSA_CLK#
D47	LVDSA_DATA3
D49	VSS
D6	H_DEFER#
D7	H_RS#1
D8	H_RS#2
E1	NC
E10	VSS
E12	H_RS#0
E13	H_REQ#1
E16	VSS
E17	H_A#31
E19	H_A#28
E2	H_D#0
E20	CFG14
E23	CFG13
E24	VSS
E27	TVA_DAC
E28	VSS
E29	CRT_RED#
E32	VSS
E33	CRT_VSYNC
E35	GFX_VID0
E36	GFX_VR_EN
E39	L_CTRL_CLK
E4	H_HIT#
E40	L_CTRL_DATA
E42	LVDSB_CLK

Ball	Signal
AB26	VSS
AB28	VSS
AB29	VCC_AXG
AB31	VSS
AB32	VSS
AB33	VCC_NCTF
AB35	VSS_NCTF
AB36	VCC_NCTF
AB37	VCC_NCTF
AB50	PEG_RX8
AB51	PEG_RX#8
AC10	VSS
AC11	H_D#39
AC13	VSS
AC14	H_D#37
AC16	VCC_AXG_NCTF
AC17	VCC_AXG_NCTF
AC19	VCC_AXG_NCTF
AC2	H_DSTBP#2
AC20	VCC_AXG
AC21	VCC_AXG
AC23	VCC_AXG
AC24	VCC_AXG
AC26	VCC_AXG
AC28	VCC_AXG
AC29	VCC_AXG
AC3	VSS
AC31	VCC
AC32	VCC
AC33	VCC_NCTF
AC35	VCC_NCTF
AC36	VCC_NCTF
AC38	PEG_TX9
AC39	VSS
AC41	PEG_RX11
AC42	PEG_TX#12
AC43	VSS
AC45	PEG_RX10
AC46	PEG_TX#10

Ball	Signal
AW4	SM_VREF
AW40	SA_DQ25
AW41	SA_DQ28
AW43	SA_DQ16
AW44	SA_DQ1
AW45	VCC_SM_LF1
AW47	SA_DQ7
AW49	PWROK
AW5	VSS
AW50	SB_DQ2
AW51	SB_DQ3
AW7	VSS
AW8	VCC_SM_LF6
AW9	SA_DQ45
AY10	VSS
AY17	SB_BS0
AY18	SB_RCVEN#
AY2	SB_DQ60
AY20	SA_RCVEN#
AY24	VSS
AY28	SB_MA8
AY3	SB_DQ61
AY32	SM_CKE1
AY35	VCC_SM
AY37	VSS
AY41	SA_DQ29
AY42	VSS
AY43	VSS
AY45	VSS
AY46	SA_DQ3
AY47	VSS
AY49	SB_DQ13
AY5	SA_DM6
AY50	VSS
AY6	SA_DQ52
AY7	SA_DQ49
AY9	SA_DQ43
BA1	VSS
BA11	SA_DQ39

Ball	Signal
E44	LVDSB_DATA0
E47	VSS
E5	H_CPUSLP#
E50	LVDSA_DATA1
E51	LVDSA_DATA#1
E8	H_BPRI#
F12	H_BREQ#
F16	H_A#8
F19	VSS
F2	VTTLF2
F23	CFG5
F27	TVA_RTN
F29	CRT_RED
F3	H_D#7
F33	CRT_HSYNC
F36	VSS
F4	VSS
F40	VSS
F48	LVDSA_DATA2
F49	LVDSA_DATA#2
F50	VSS
G1	VSS
G10	H_LOCK#
G12	H_ADS#
G13	VSS
G16	VSS
G17	H_A#10
G19	VSS
G2	H_D#1
G20	H_ADSTB#1
G23	CFG7
G24	VSS
G27	TVB_DAC
G28	VSS
G29	VSS
G32	CRT_BLUE#
G33	VSS
G35	CRT_DDC_DATA
G36	DPRSLPVR

Ball	Signal
AC47	VSS
AC49	PEG_TX#11
AC5	H_D#46
AC50	PEG_TX11
AC6	H_D#44
AC7	H_D#36
AC9	H_D#35
AD1	VSS
AD11	H_D#38
AD12	H_D#32
AD13	H_DINV#2
AD15	VCC_AXG_NCTF
AD16	VCC_AXG_NCTF
AD17	VCC_AXG_NCTF
AD19	VSS_NCTF
AD2	H_DSTBN#2
AD20	VCC_AXG
AD21	VSS
AD23	VCC_AXG
AD24	VCC_AXG
AD26	VSS
AD28	VCC_AXG
AD29	VSS
AD3	VSS
AD31	VCC_AXG
AD32	VSS
AD33	VCC_NCTF
AD35	VCC_NCTF
AD36	VCC_NCTF
AD37	VSS_NCTF
AD39	PEG_TX#9
AD40	PEG_RX#11
AD41	VSS
AD43	PEG_TX12
AD44	PEG_RX#10
AD45	VSS
AD47	PEG_TX10
AD49	VSS
AD5	VSS

Ball	Signal
BA13	SA_DQ38
BA16	SA_DQS#4
BA17	VSS
BA18	VSS
BA19	SA_WE#
BA2	VSS
BA23	SM_CK#1
BA24	VSS
BA25	SM_CK3
BA28	SA_MA9
BA29	SB_MA6
BA3	SB_DQ56
BA32	VCC_SM
BA33	VCC_SM
BA35	VCC_SM
BA37	SA_DQS#3
BA39	SB_MA12
BA45	SA_DQ2
BA49	SB_DQ10
BA50	SB_DQ8
BA51	SB_DQ12
BB12	VSS
BB16	SA_DQS4
BB19	SA_BS0
BB2	SA_DQS6
BB23	SM_CK1
BB25	VSS
BB29	VCCA_SM_CK
BB3	SB_DQ57
BB33	VCC_SM
BB40	VSS
BB43	SA_DQS2
BB44	VSS
BB45	SA_DQ8
BB47	SA_DQ12
BB49	VSS
BB5	SA_DQ48
BB50	SB_DQ9
BB7	SA_DQ53

Ball	Signal
G39	CLKREQ#
G4	H_D#6
G40	ICH_SYNC#
G41	PMSYNC# (PM_BM_BUSY#)
G42	VSS
G44	LVDSB_DATA#0
G45	VSS
G48	VSS
G50	LVDSA_DATA0
G51	LVDSA_DATA#0
G7	H_D#2
G8	VSS
H10	RSVD
H13	H_REQ#3
H17	H_ADSTB#0
H2	H_D#9
H20	H_A#21
H24	VSS
H28	VSS
H3	H_D#5
H32	CRT_BLUE
H35	SDVO_CTRL_CLK
H39	L_BKLT_EN
H4	VSS
H42	VCCD_LVDS
H45	VSS
H47	DPLL_REF_SSCLK#
H48	DPLL_REF_SSCLK
H49	VCCA_DPLLB
H5	H_D#13
H50	VSS
H7	H_D#4
H8	H_DPWR#
J1	H_D#21
J11	VSS
J12	RSVD
J13	H_A#3

Ball	Signal
AD50	VSS
AD51	VCC_PEG
AD7	H_D#41
AD8	VSS
AD9	H_D#34
AE10	VSS
AE11	H_D#52
AE13	H_DINV#3
AE14	VSS
AE2	H_D#45
AE3	H_D#33
AE49	PEG_TX#14
AE5	H_D#60
AE50	PEG_TX14
AE6	VSS
AE7	H_D#57
AE9	H_D#51
AF16	VCC_AXG_NCTF
AF17	VSS_NCTF
AF19	VCC_AXG_NCTF
AF20	VSS
AF21	VCC_AXG
AF23	VSS
AF24	VSS
AF26	VCC_AXG
AF28	VSS
AF29	VSS
AF31	VSS
AF32	VCC
AF33	VCC_NCTF
AF35	VSS_NCTF
AF36	VCC_NCTF
AG2	VSS
AG3	H_D#47
AG38	VSS
AG39	PEG_TX13
AG41	PEG_RX#15

Ball	Signal
BB8	VSS
BB9	SA_DQ47
BC1	SA_DQS#6
BC11	SB_DQ35
BC12	SB_DQ38
BC13	SB_DQ36
BC16	VSS
BC17	SB_WE#
BC18	SB_MA0
BC19	SA_MA10
BC2	SB_DQ51
BC23	RSVD
BC24	VSS
BC25	VSS
BC28	SB_MA7
BC29	VCCA_SM_CK
BC32	VCC_SM
BC33	VCC_SM
BC35	VCC_SM
BC36	VSS
BC37	SA_DQS3
BC39	VCC_SM_LF2
BC40	VSS
BC41	SA_DQS#2
BC50	SB_DQS#1
BC51	VSS
BD10	SA_DQ41
BD13	VSS
BD17	VCC_SM_LF4
BD2	VSS
BD20	SA_MA1
BD24	RSVD
BD28	VSS
BD3	SB_DQ54
BD32	VCC_SM
BD35	VCC_SM
BD37	SB_MA9

Ball	Signal
J16	VSS
J17	H_A#15
J19	H_A#26
J2	VSS
J20	CFG8
J23	CFG12
J24	VSS
J27	TVB_RTN
J28	VSS
J29	CRT_GREEN#
J32	VCC_SYNC
J33	VSS
J35	VSS
J36	PM_EXT_TS#1
J39	VSS
J40	L_BKLT_CTRL
J41	VCCD_LVDS
J50	PEG_RX0
J51	PEG_RX#0
K12	VSS
K16	H_A#12
K19	H_A#17
K2	H_DSTBP#1
K23	CFG15
K27	TVC_DAC
K29	CRT_GREEN
K3	H_DSTBN#1
K33	CRT_DDC_CLK
K36	SDVO_CTRL_DATA
K40	L_VDD_EN
K44	PEG_CLK
K45	PEG_CLK#
K47	VSS
K49	VSSA_PEG_BG
K5	H_DINV#0
K50	VCCA_PEG_BG
K7	H_DRDY#
K8	VSS
K9	H_D#15

Ball	Signal
AG42	PEG_RX15
AG43	VSS
AG45	PEG_RX#14
AG46	PEG_RX#12
AG47	VSS
AG49	PEG_RX13
AG50	VSS
AH1	VTTLF3
AH11	H_DSTBN#3
AH12	H_D#53
AH13	H_D#63
AH15	VCC_AXG_NCTF
AH16	VCC_AXG_NCTF
AH17	VCC_AXG_NCTF
AH19	VCC_AXG_NCTF
AH2	H_D#62
AH20	VCC_AXG
AH21	VCC_AXG
AH23	VCC_AXG
AH24	VCC_AXG
AH26	VCC_AXG
AH28	VCC
AH29	VCC
AH3	VSS
AH31	VCC
AH32	VCC
AH33	VCC_NCTF
AH35	VCC_NCTF
AH36	VCC_NCTF
AH37	VCC_NCTF
AH39	PEG_TX#13
AH40	VSS
AH41	VSS
AH43	PEG_TX15
AH44	PEG_TX#15
AH45	PEG_RX14
AH47	PEG_RX12
AH49	PEG_RX#13
AH5	H_D#55

Ball	Signal
BD39	SM_CKE3
BD4	VCC_SM_LF5
BD42	SA_DM2
BD44	SA_DM1
BD45	VSS
BD47	SA_DQS#1
BD48	VSS
BD49	SB_DM1
BD5	VSS
BD50	SB_DQS1
BD7	SA_DQ46
BD8	SA_DQ42
BE1	VSS
BE10	SA_DQ40
BE11	SB_DQ33
BE12	SB_DQ37
BE13	SM_CS#3
BE16	SM_ODT3
BE17	SB_CAS#
BE18	SA_RAS#
BE19	VSS
BE2	SB_DQS6
BE23	VSS
BE24	SB_MA_14
BE25	SB_MA5
BE28	SA_MA11
BE29	SM_CKE0
BE30	VSS
BE32	VCC_SM
BE33	VCC_SM
BE35	VCC_SM
BE37	SB_MA11
BE39	VCC_SM_LF3
BE4	SB_DQ53
BE40	SA_DQ19
BE42	VSS
BE44	SA_DQ17
BE45	SA_DQ15
BE48	SA_DQS1

Ball	Signal
L1	VSS
L13	H_A#9
L16	H_A#14
L17	VSS
L19	H_A#22
L2	H_DINV#1
L20	VSS
L23	CFG11
L24	VSS
L27	TVC_RTN
L28	VSS
L29	VCCD_TVDAC
L3	VSS
L32	CFG18
L33	VSS
L35	CFG20
L36	PM_EXT_TS#0
L39	PM_DPRSTP#
L41	LVDS_IBG
L43	LVDS_VBG
L49	VSS
L50	PEG_RX1
L51	PEG_RX#1
L7	H_DSTBP#0
M10	H_D#10
M11	H_A#6
M14	H_REQ#0
M17	H_A#24
M2	H_D#16
M20	CFG16
M24	CFG17
M28	VSS
M3	H_D#20
M32	VCCD_CRT
M35	TV_DCONSEL0
M42	VSS
M43	PEG_COMPO
M45	PEG_TX0
M46	VSS

Ball	Signal
AH50	VCC_RXR_DMI
AH51	VCC_RXR_DMI
AH7	VSS
AH8	H_D#49
AH9	VSS
AJ10	H_DSTBP#3
AJ11	VSS
AJ13	VSS
AJ14	H_D#50
AJ16	VCC_AXG_NCTF
AJ17	VCC_AXG_NCTF
AJ19	VCC_AXG_NCTF
AJ2	H_D#59
AJ20	VCC_AXG
AJ21	VSS
AJ23	VCC_AXM
AJ24	VSS
AJ26	VCC_AXM
AJ28	VCC
AJ29	VSS
AJ3	H_D#61
AJ31	VCC
AJ32	VSS
AJ33	VCC_NCTF
AJ35	VCC_NCTF
AJ36	VCC_NCTF
AJ38	DMI_RXN1
AJ39	DMI_RXP1
AJ41	DMI_TXN1
AJ42	DMI_TXP1
AJ43	VSS
AJ45	VSS
AJ46	DMI_TXN0
AJ47	DMI_TXP0
AJ49	VSS
AJ5	H_D#54
AJ50	VCC_DMI
AJ6	H_D#56
AJ7	H_D#58

Ball	Signal
BE50	SB_DQ11
BE51	VSS
BE8	VSS
BF12	VSS
BF16	VSS
BF19	RSVD
BF2	SB_DQS#6
BF23	RSVD
BF25	SB_MA4
BF29	SA_BS2
BF3	SB_DM6
BF33	VCC_SM
BF34	VCC_SM
BF36	VSS
BF4	SB_DQ48
BF40	SA_DQ23
BF44	SA_DQ20
BF48	SA_DQ9
BF49	SB_DQ15
BF50	SB_DQ14
BG1	SB_DQ50
BG10	SA_DQ44
BG12	SB_DQ39
BG13	SB_MA13
BG16	SM_CS#2
BG17	SB_MA10
BG18	SB_BS1
BG19	VSS
BG2	VSS
BG20	SM_CS#0
BG23	RSVD
BG24	VSS
BG25	SB_MA2
BG28	SB_MA1
BG29	VSS
BG30	SA_MA12
BG32	VCC_SM
BG33	VCC_SM
BG35	VCC_SM

Ball	Signal
M47	PEG_RX2
M49	VSS
M5	VSS
M50	VSS
M6	H_D#3
M7	H_DSTBN#0
M9	VSS
N1	H_D#31
N11	VSS
N12	H_D#11
N14	VSS
N16	H_A#25
N17	VSS
N19	H_A#35
N2	H_D#26
N20	THERMTRIP#
N23	CFG6
N24	CFG2
N27	CFG1
N28	VCCD_QDAC
N29	VSS
N3	H_D#23
N32	VSS
N33	CFG19
N35	RSVD
N36	VSS
N39	VSS
N40	LVDS_VREFL
N41	LVDS_VREFH
N43	PEG_COMPI
N44	VSS
N45	PEG_TX#0
N47	PEG_RX#2
N49	VSS
N5	H_D#22
N50	PEG_TX3
N51	PEG_TX#3
N7	VSS
N8	H_D#8

Ball	Signal
AJ9	H_D#48
AK16	VCC_AXG_NCTF
AK17	VSS_NCTF
AK19	VCC_AXG_NCTF
AK20	VSS
AK21	VSS
AK23	VCC_AXM
AK24	VCC_AXM
AK26	VSS
AK28	VSS
AK29	VCC_AXM
AK31	VSS
AK32	VCC
AK33	VCC_NCTF
AK35	VCC_NCTF
AK36	VCC_NCTF
AK37	VCC_NCTF
AK50	CL_DATA
AK51	VSS
AL1	VSS
AL16	VCC_AXG_NCTF
AL17	VCC_AXG_NCTF
AL19	VCC_AXG_NCTF
AL2	VCCA_HPLL
AL20	VCC_AXG_NCTF
AL21	VCC_AXG_NCTF
AL23	VCC_AXG_NCTF
AL24	VCC_AXM_NCTF
AL26	VCC_AXM_NCTF
AL28	VCC_AXM_NCTF
AL29	VCC_AXM_NCTF
AL31	VCC_AXM_NCTF
AL32	VCC_AXM_NCTF
AL33	VCC_NCTF
AL35	VCC_NCTF
AL36	RSVD
AM11	VSS
AM12	RSVD
AM13	VSS

Ball	Signal
BG36	SB_BS2
BG37	SM_CKE4
BG39	VSS
BG40	SA_DQ22
BG42	SA_DQ18
BG47	SA_DQ10
BG48	VSS
BG5	VSS
BG50	SA_DQ13
BG51	VSS
BG8	SA_DM5
BH12	SB_DM4
BH17	VSS
BH18	SM_ODT0
BH20	RSVD
BH28	SA_MA3
BH30	VSS
BH32	VCC_SM
BH34	VCC_SM
BH35	VCC_SM
BH39	RSVD
BH44	VSS
BH45	SA_DQ21
BH46	VSS
BH49	SA_DQ14
BH5	SB_DQ49
BH6	SA_DQS5
BH7	SA_DQS#5
BH8	VSS
BJ1	NC
BJ10	SB_DQ40
BJ11	VSS
BJ12	SB_DQS4
BJ13	VSS
BJ14	SM_ODT2
BJ15	SM_ODT1
BJ16	SA_MA13
BJ18	RSVD
BJ19	SA_MA0

Ball	Signal
N9	H_D#12
P13	H_D#14
P15	H_A#18
P19	VSS
P2	VSS
P23	VSS
P27	CFG0
P29	VSS
P3	VSS
P33	TV_DCONSEL1
P36	RSVD
P37	RSVD
P4	H_D#29
P50	VSS
R1	VTT
R17	H_A#19
R2	VTT
R20	VCC_AXG
R24	CFG10
R28	VSS
R3	VTT
R30	VCC
R32	TEST2
R35	RSVD
R49	VSS
R50	PEG_TX#4
R51	PEG_TX4
T10	VTT
T11	VTT
T13	VTT
T14	VCC_AXG
T17	VCC_AXG_NCTF
T18	VCC_AXG_NCTF
T19	VCC_AXG_NCTF
T2	VTT
T21	VCC_AXG_NCTF
T22	VCC_AXG_NCTF
T23	VCC_AXG_NCTF
T25	VCC_AXG_NCTF

Ball	Signal
AM15	VCC_AXG_NCTF
AM16	VCC_AXG_NCTF
AM17	VSS_NCTF
AM19	VCC_AXG_NCTF
AM2	VCCA_MPLL
AM20	VCC_AXG_NCTF
AM21	VCC_AXG_NCTF
AM23	VCC_AXG_NCTF
AM24	VSS_NCTF
AM26	VCC_AXM_NCTF
AM28	VCC_AXM_NCTF
AM29	VCC_AXM_NCTF
AM3	VSS
AM31	VCC_AXM_NCTF
AM32	VCC_AXM_NCTF
AM33	VCC_AXM_NCTF
AM35	VCC_NCTF
AM36	RSVD
AM37	RSVD
AM39	DMI_TXP2
AM4	VSS
AM40	DMI_TXN2
AM41	VSS
AM43	DMI_TXP3
AM44	DMI_TXN3
AM45	VSS
AM47	DMI_RXP0
AM49	CL_CLK
AM5	HPLL_CLK
AM50	CL_VREF
AM7	HPLL_CLK#
AM8	SA_DQ58
AM9	SA_DQ62
AN1	VSS
AN10	SA_DQ59
AN11	SA_DQ63
AN13	RSVD
AN14	VCC_AXG
AN2	VCCD_HPLL

Ball	Signal
BJ2	SB_DQ55
BJ20	RSVD
BJ23	VCC_SM_CK
BJ24	VCC_SM_CK
BJ25	SA_MA7
BJ27	SA_MA6
BJ29	SA_MA_14
BJ32	VCC_SM
BJ33	VCC_SM
BJ34	VCC_SM
BJ36	SB_DQ27
BJ37	SB_DQ26
BJ38	VSS
BJ4	VSS
BJ40	SB_DQ29
BJ41	SB_DQ24
BJ42	VSS
BJ43	SB_DQ18
BJ44	SB_DQ17
BJ45	SA_DQ11
BJ46	VSS
BJ50	SB_DQ16
BJ51	NC
BJ6	SB_DQ47
BJ7	SB_DM5
BJ8	SB_DQ46
BK1	NC
BK10	SB_DQ45
BK11	SB_DQ34
BK12	SB_DQS#4
BK13	SB_DQ32
BK14	SM_RCOMP#
BK15	VSS
BK16	SM_CS#1
BK17	VSS
BK18	RSVD
BK19	SA_BS1
BK2	NC
BK20	RSVD

Ball	Signal
T27	VSS_NCTF
T29	VSS
T3	VTT
T30	VCC_NCTF
T31	VSS
T33	VSS
T34	VCC_NCTF
T35	VCC_NCTF
T37	VSS_NCTF
T38	PEG_TX1
T39	VSS
T41	PEG_RX5
T42	PEG_TX#5
T43	VSS
T45	PEG_RX#3
T46	PEG_TX2
T47	VSS
T49	PEG_RX4
T5	VTT
T50	PEG_RX#4
T6	VTT
T7	VTT
T9	VTT
U1	VTT
U11	VTT
U12	VTT
U13	VTT
U15	VCC_AXG_NCTF
U16	VCC_AXG_NCTF
U17	VCC_AXG_NCTF
U19	VCC_AXG_NCTF
U2	VTT
U20	VCC_AXG_NCTF
U21	VCC_AXG_NCTF
U23	VCC_AXG_NCTF
U24	VSS_NCTF
U26	VCC_AXG_NCTF
U28	VSS_NCTF
U29	VCC_NCTF

Ball	Signal
AN3	SA_DQ57
AN38	VSS
AN39	VSS
AN41	DMI_RXP2
AN42	DMI_RXN2
AN43	VSS
AN45	DMI_RXP3
AN46	DMI_RXN3
AN47	DMI_RXN0
AN49	CL_RST#
AN5	VSS
AN50	SB_DQ5
AN51	SB_DQ4
AN6	SA_DM7
AN7	VSS
AN9	SA_DQ61
AP15	VCC_AXG_NCTF
AP16	VCC_AXG_NCTF
AP17	VCC_AXG_NCTF
AP19	VCC_AXG_NCTF
AP2	SA_DQS#7
AP20	VCC_AXG_NCTF
AP21	VCC_AXG_NCTF
AP23	VCC_AXG_NCTF
AP24	VCC_AXG_NCTF
AP26	VSS_NCTF
AP28	VSS_NCTF
AP29	VCC_AXM_NCTF
AP3	SA_DQS7
AP31	VCC_AXM_NCTF
AP32	VCC_AXM_NCTF
AP33	VCC_AXM_NCTF
AP35	VCC_NCTF
AP36	VCC_NCTF
AP4	VSS
AP48	VSS
AP49	SB_DQ0
AP50	VSS
AR1	SB_DQ58

Ball	Signal
BK22	RSVD
BK23	VCC_SM_CK
BK24	VCC_SM_CK
BK25	VSS
BK27	SA_MA2
BK28	SA_MA5
BK29	VSS
BK3	SB_DQ52
BK31	SM_RCOMP_VOH
BK32	VCC_SM
BK33	VCC_SM
BK34	VCC_SM
BK35	VCC_SM
BK36	VSS
BK37	SB_DQ31
BK38	SB_DQS#3
BK39	SB_DQS3
BK40	VSS
BK41	SB_DQ28
BK42	SB_DQ23
BK43	SB_DQ22
BK44	VSS
BK45	SB_DM2
BK46	SB_DQS2
BK47	SB_DQ20
BK49	SB_DQ21
BK5	SB_DQ42
BK50	NC
BK51	NC
BK6	VSS
BK7	SB_DQS#5
BK8	VSS
BK9	SB_DQ44
BL1	VSS_SCB4
BL11	VSS
BL13	VSS
BL15	SM_RCOMP
BL17	SA_CAS#
BL19	VSS

Ball	Signal
U3	VTT
U31	VCC_NCTF
U32	VCC_NCTF
U33	VCC_NCTF
U35	VCC_NCTF
U36	VCC_NCTF
U39	PEG_TX#1
U40	PEG_RX#5
U41	VSS
U43	PEG_TX5
U44	PEG_RX3
U45	VSS
U47	PEG_TX#2
U48	VCCD_PEG_PLL
U5	VTT
U50	VSS
U51	VCCA_PEG_PLL
U7	VTT
U8	VTT
U9	VTT

Ball	Signal
AR11	VSS
AR12	RSVD
AR13	RSVD
AR15	VSS_NCTF
AR16	VCCA_SM_NCTF
AR17	VCCA_SM_NCTF
AR19	VSS_NCTF
AR2	VSS
AR20	VCC_AXG_NCTF
AR21	VCC_AXG_NCTF
AR23	VCC_AXG_NCTF
AR24	VCC_AXG_NCTF
AR26	VCC_AXG_NCTF
AR28	VSS_NCTF
AR29	VCC_AXD_NCTF
AR31	VCC_AXM_NCTF
AR32	VCC_AXM_NCTF
AR33	VCC_AXM_NCTF
AR35	VCC_NCTF
AR36	VCC_NCTF

Ball	Signal
BL2	NC
BL22	VSS
BL24	SA_MA4
BL28	SA_MA8
BL3	NC
BL31	SM_RCOMP_VOL
BL33	VCC_SM
BL35	SB_DQ30
BL37	VSS
BL39	SB_DM3
BL41	SB_DQ25
BL43	SB_DQ19
BL45	SB_DQS#2
BL47	VSS
BL49	NC
BL5	SB_DQ43
BL50	NC
BL51	VSS_SCB5
BL7	SB_DQS5
BL9	SB_DQ41

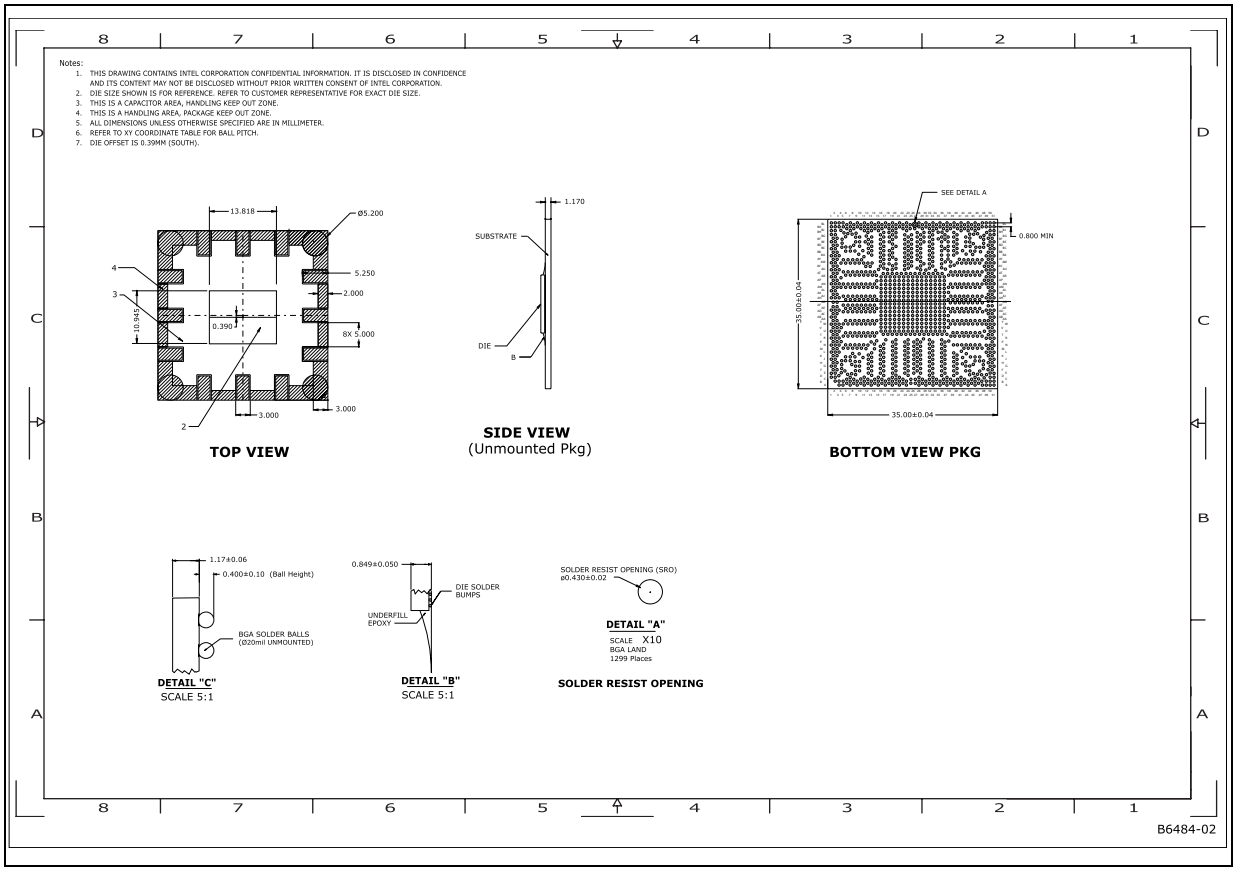
15.4 Package

The (G)MCH is provided in an 1299-ball, FCBGA package.

Caution: Avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

- Tolerances:
  - — X: ±0.1
  - — XX: ±0.05
- Angles: ±1.0 degrees
- Package parameters: 35.0 mm x 35.0 mm
- Land metal diameter: 524 microns
- Solder resist opening: 430 microns

Figure 25. (G)MCH Mechanical Drawing



NOTES:

1. **Capacitor Area, Handling Keep Out Zone**: Handling refers to any equipment such as pick and place, trays, or shipping media. Capacitor Area Handling Keep Out Zone means all equipment mentioned above should stay out of this area to not interfere with capacitors that may be placed in this area. Use of an insulating material between the capacitors and any thermal solution is recommended to prevent capacitor shorting.
2. **Handling Area, Package Keep Out Zone**: Package Keep Out Zone means capacitors may not be placed in this area since this is the area where we allow handling; that is, pick and place.
3. Dimensions are in millimeters.
4. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994.

§

16 (G)MCH Register Description

16.1 Register Terminology

Abbreviation	Definition
RO	**Read Only bit(s).** Writes to these bits have no effect. This may be a status bit or a static value.
RS/WC	**Read Set / Write Clear bit(s).** The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect.
R/W	**Read / Write bit(s).** These bits can be read and written by software. Hardware may only change the state of this bit by reset.
R/WC	**Read / Write Clear bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WC/S	**Read / Write Clear / Sticky bit(s).** These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/W/B	**Read / Write / Blind bit(s).** These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit.
R/W/K	**Read / Write / Key bit(s).** These bits can be read and written by software. Additionally this bit, when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).
R/W/L	**Read / Write / Lockable bit(s).** These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/L/K	**Read / Write / Lockable / Key bit(s).** These bits can be read and written by software. Additionally this bit is a Key bit that, when set, prohibits this bit field and/or some other specified bit fields from being writeable (bit fields become Read Only).

Abbreviation	Definition
R/W/S	**Read / Write / Sticky bit(s).** These bits can be read and written by software. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/WSC	**Read / Write Self Clear bit(s).** These bits can be read and written by software. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent software read could retrieve a 1.
R/WSC/L	**Read / Write Self Clear / Lockable bit(s).** These bits can be read and written by software. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent software read could retrieve a 1. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WC	**Read Write Clear bit(s).** These bits can be read and written by software. However, a write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WO	**Write Once bit(s).** Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	**Write Only.** These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.

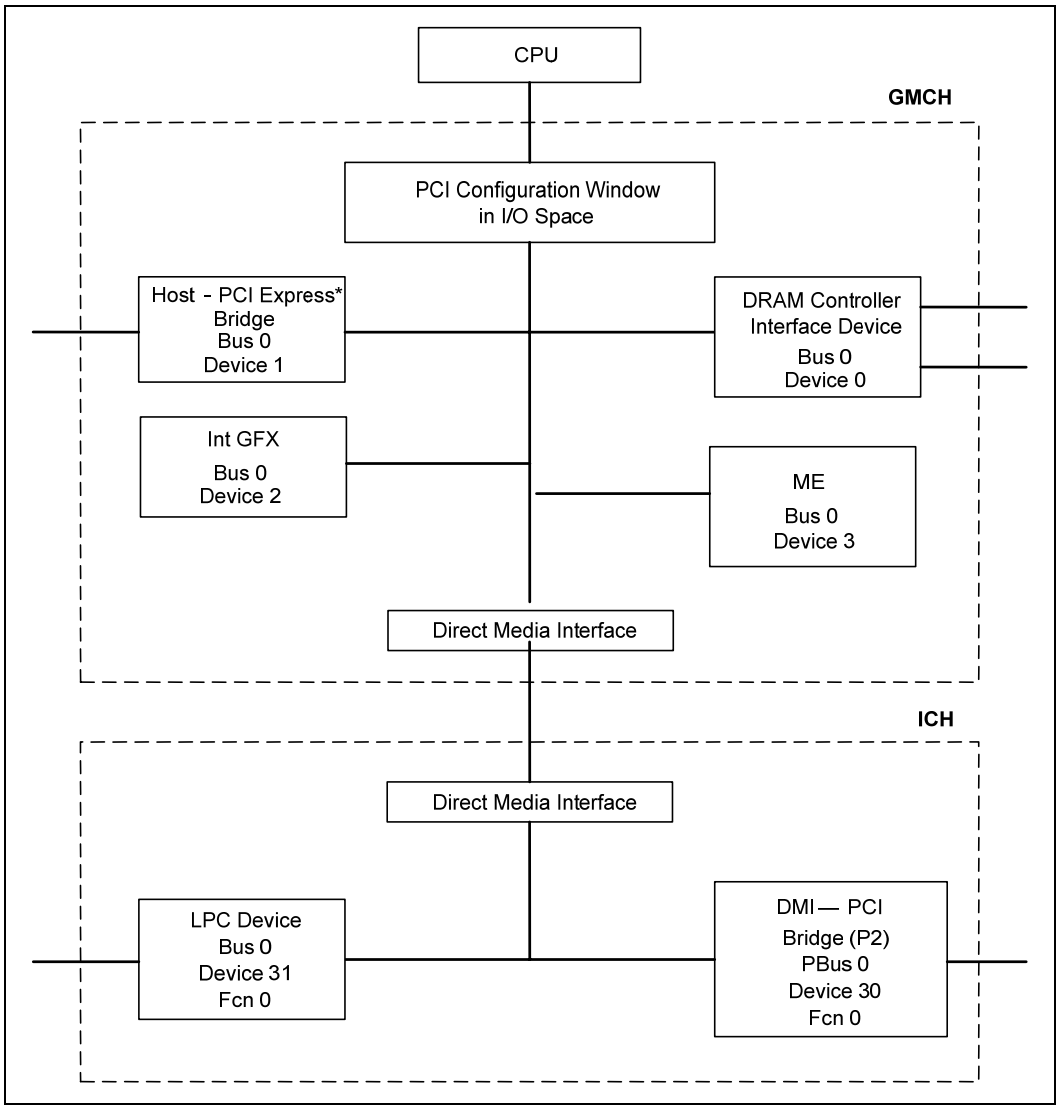
17 (G)MCH Configuration Process and Registers

17.1 Platform Configuration Structure

The DMI physically connects the (G)MCH and the ICH; so, from a configuration standpoint, the DMI is logically PCI Bus 0. As a result, all devices internal to the (G)MCH and the ICH appear to be on PCI Bus 0. The system's primary PCI expansion bus is physically attached to the ICH and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express X16 graphics attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI Bus 0.

Note: A physical PCI Bus 0 does not exist and that DMI and the internal devices in the (G)MCH and ICH logically constitute PCI Bus 0 to configuration software.

Figure 27. Conceptual Chipset Platform PCI Configuration Diagram



The (G)MCH contains three PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI Bus 0.

Device 0: Host Bridge/DRAM Controller. Logically this appears as a PCI device residing on PCI Bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other (G)MCH-specific registers.

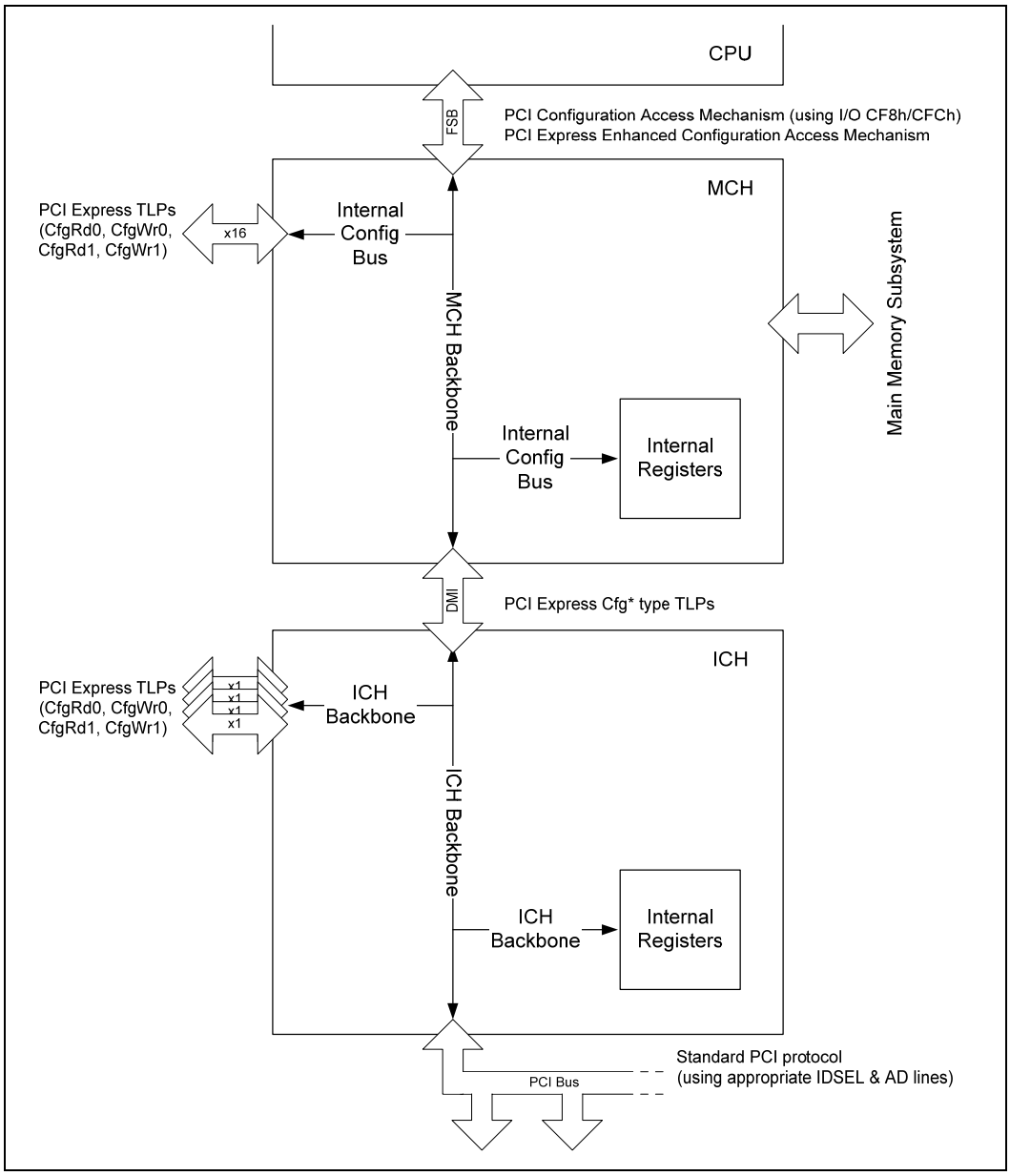
Device 1: Host-PCI Express Bridge. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI Bus 0 and is compliant with *PCI Express Specification Revision 1.0.* Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.

Device 2: Internal Graphics Control. Logically, this appears as a PCI device residing on PCI Bus 0. Physically, Device 2 contains the configuration registers for 3D, 2D, and display functions.

17.2 Configuration Mechanisms

The CPU is the originator of configuration cycles so the FSB is the only interface in the platform where these mechanisms are used. Internal to the (G)MCH transactions received through both configuration mechanisms are translated to the same format.

Figure 28. Chipset Configuration Paths and Transaction Types



17.2.1 Standard PCI Configuration Mechanism

A detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles is described below.

The PCI specification defines a slot based "configuration space" that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI

configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the (G)MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the CPU's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal (G)MCH configuration registers, DMI or PCI Express.

17.2.2 Logical PCI Bus 0 Configuration Mechanism

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The Host-DMI Bridge entity within the (G)MCH is hardwired as Device 0 on PCI Bus 0. The Host-PCI Express Bridge entity within the (G)MCH is hardwired as Device 1 on PCI Bus 0. Device 2 contains the control registers for the Integrated Graphics Controller. The ICH decodes the Type 0 access and generates a configuration access to the selected internal device.

17.2.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and falls outside the range claimed by the Host-PCI Express bridge (not between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register), the (G)MCH will generate a Type 1 DMI Configuration Cycle. A[1:0] of the DMI request packet for the Type 1 configuration cycle will be "01". Bits 31:2 of the CONFIG_ADDRESS register will be translated to the A[31:2] field of the DMI request packet of the configuration cycle as shown below. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the ICH via the DMI, the ICH compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH's devices, the DMI, or a downstream PCI bus.

Figure 29. DMI Type 0 Configuration Address Translation

CONFIG_ADDRESS

31	30:28	27:24	23:16	15:11	10:8	7:2	1	0
1	Reserved	0	0	Device Number	Function	Register Number	x	x

DMI Type 0 Configuration Address Extension

31:28	27:16	15:11	10:8	7:2	1	0
Reserved		Device Number	Function	Register Number	0	0

Figure 30. DMI Type 1 Configuration Address Translation

CONFIG_ADDRESS

31	30:28	27:24	23:16	15:11	10:8	7:2	1	0
1	Reserved	0	Bus Number	Device Number	Function	Register Number	x	x

DMI Type 1 Configuration Address Extension

31:28	27:16	15:11	10:8	7:2	1	0
Reserved	Bus Number	Device Number	Function	Register Number	0	1

17.2.4 PCI Express Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by *PCI Specification Revision 2.3*. PCI Express configuration space is divided into a PCI 2.3-compatible region, which consists of the first 256 bytes of a logical device's configuration space and a PCI Express extended region which consists of the remaining configuration space.

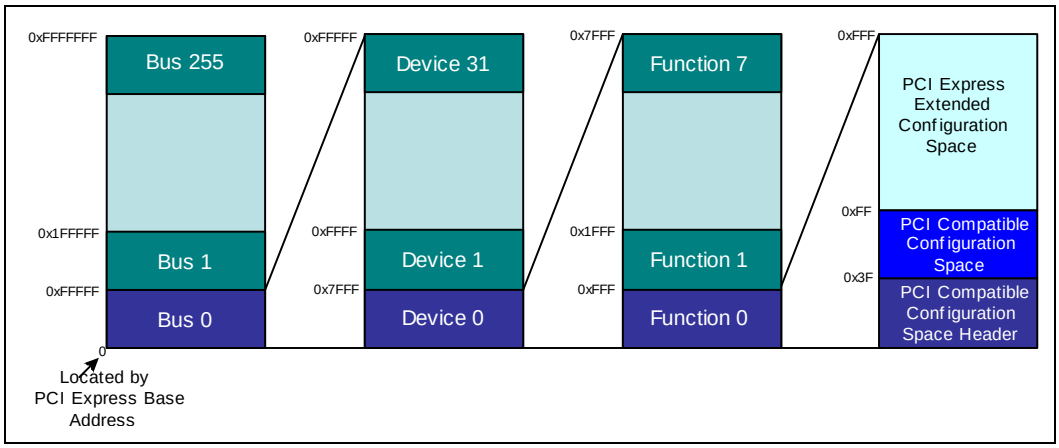
The PCI-compatible region can be accessed using either the mechanism defined in the previous Standard PCI Configuration Mechanism or using the PCI Express Enhanced Configuration Mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express Enhanced Configuration Mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the Dword to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express Enhanced Configuration Mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported

by the system firmware to the operating system. There is a register, PCIEXBAR, which defines the base address for the block of addresses below top 4 GB for the configuration space associated with busses, devices and functions that are potentially a part of the PCI Express root complex hierarchy. In the PCIEXBAR register there exist controls to limit the size of this reserved memory mapped space. 256 MB is the amount of address space required to reserve space for every bus, device, and function that could possibly exist. Options for 128 MB and 64 MB exist in order to free up those addresses for other uses. In these cases, the number of busses and all of their associated devices and functions are limited to 128 or 64 busses, respectively.

The PCI Express Configuration Transaction Header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

Figure 31. Memory Map to PCI Express Device Configuration Space



As with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

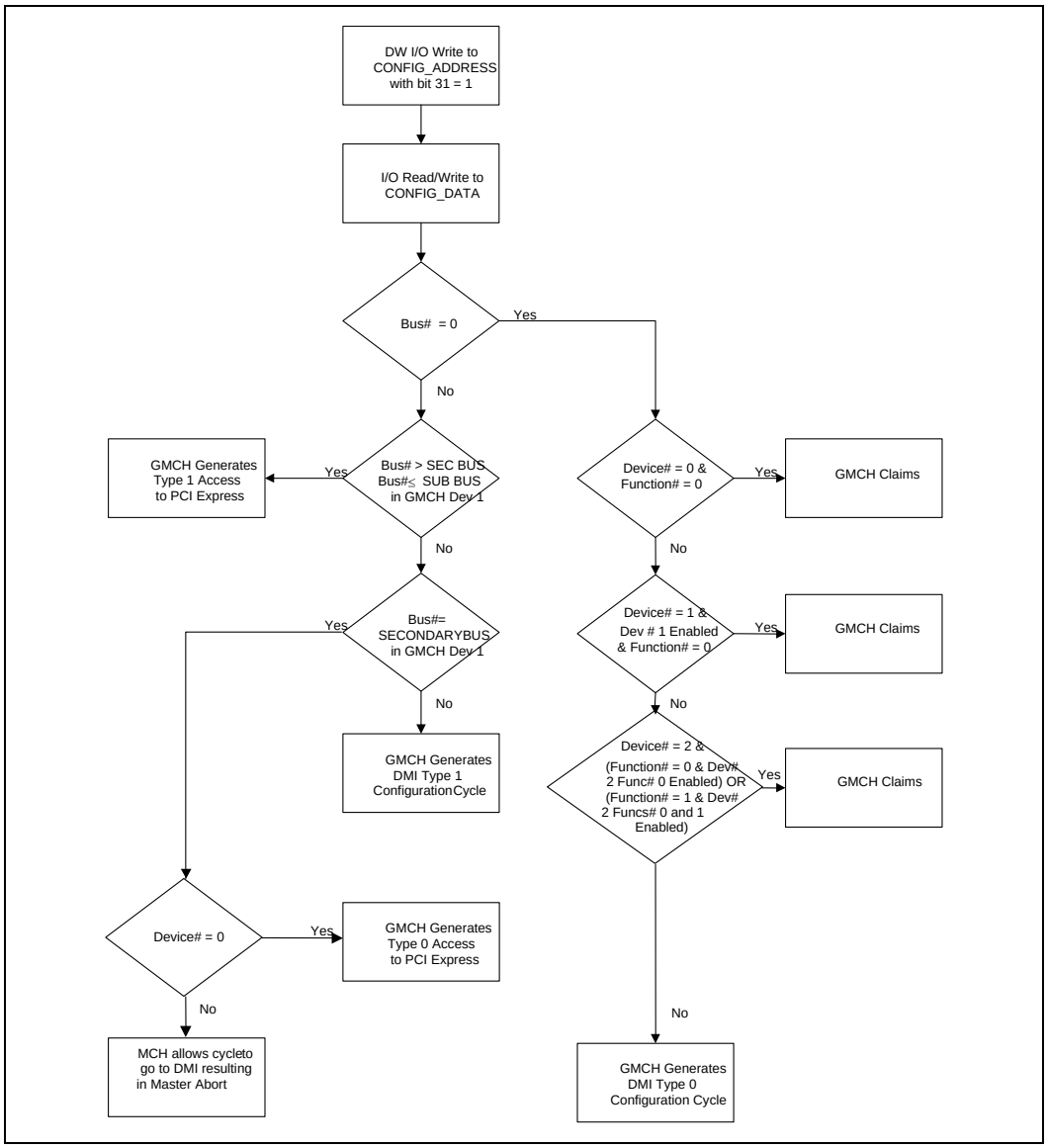
To access this space (steps 1, 2, 3 are done only once by BIOS):

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 0 of the PCIEXBAR register.
2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.
3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 KB) + (function number * 4 KB) + (1 B * offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write or read that register.

17.3 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express Graphics. The (G)MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the (G)MCH or to one of these two interfaces. Configuration cycles to the ICH internal devices and Primary PCI (including downstream devices) are routed to the ICH via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port device or associated link.

Figure 32. (G)MCH Configuration Cycle Flowchart



17.3.1 Internal Device Configuration Accesses

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device.

If the targeted PCI Bus 0 device exists in the (G)MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

17.3.2 Bridge Related Configuration Accesses

Configuration accesses on PEG or DMI are PCI Express Configuration TLPs.

Bus Number [7:0] is Header Byte 8 [7:0]

Device Number [4:0] is Header Byte 9 [7:3]

Function Number [2:0] is Header Byte 9 [2:0]

And special fields for this type of TLP:

Extended Register Number [3:0] is Header Byte 10 [3:0]

Register Number [5:0] is Header Byte 11 [7:2]

See the PCI Express specification for more information on both the PCI 2.3-compatible and PCI Express Enhanced Configuration Mechanism and transaction rules.

17.3.2.1 PCI Express Graphics Configuration Accesses

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access matches the Device 1 Secondary Bus Number, a PCI Express Type 0 Configuration TLP is generated on the PEG link targeting the device directly on the opposite side of the link. This should be Device 0 on the bus number assigned to the PEG link (likely Bus 1).

The device on other side of link must be Device 0. The (G)MCH will Master Abort any Type 0 Configuration access to a non-zero Device number. If there is to be more than one device on that side of the link there must be a bridge implemented in the downstream device.

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register) but doesn't match the Device 1 Secondary Bus Number, a PCI Express Type 1 Configuration TLP is generated on the secondary side of the PEG link.

PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PEG or DMI (i.e., translated to configuration writes).

17.3.2.2 DMI Configuration Accesses

Accesses to disabled (G)MCH internal devices, bus numbers not claimed by the Host-PEG bridge, or PCI Bus 0 devices not part of the (G)MCH will subtractively decode to the ICH and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the Bus Number is zero, the (G)MCH will generate a Type 0 Configuration Cycle TLP on DMI. If the Bus Number is non-zero, and falls outside the range claimed by the Host-PEG bridge, the (G)MCH will generate a Type 1 Configuration Cycle TLP on DMI.

The ICH routes configurations accesses in a manner similar to the (G)MCH. The ICH decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus 0 may be claimed by an internal device. The ICH compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration access is meant for Primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH, but remain unclaimed by any device or bridge will result in a master abort.

17.3.2.3 Configuration Retry

For both PEG and DMI, any configuration request (read or write) that receives a Configuration Request Retry Completion Status (CRS) will be reissued as a new transaction. The CRS terminates the original request TLP, but the (G)MCH will synthesize a subsequent request. The new config TLP which gets “reissued” due to CRS will have a new Sequence Number, but the TLP fields (tag, address, data, attributes, requestor ID, etc) will be the same as the original TLP.

While this is happening, no completion will be sent to the originator of the configuration cycle (the CPU). A completion will not be sent to the CPU until the (G)MCH receives a successful completion, an Unsupported Request or Completer Abort completion, or the completion times out (if completion timeout is enabled).

This mechanism mimics the behavior on a legacy PCI bus, where any request that is retried will retry indefinitely.

No devices in the ICH ever return CRS. The (G)MCH is the only root complex device that handles CRS. The ICH just forwards to the (G)MCH all completions independent of completion status.

17.4 (G)MCH Registers

The (G)MCH internal registers (I/O Mapped, Configuration, and PCI Express Extended Configuration registers) are accessible by the Host CPU. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG_ADDRESS which can only be accessed as a Dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in Dword (32-bit) quantities.

Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled "Reserved.” Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and

then written back. Note the software does not need to perform read, merge, or write operation for the configuration address register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or “Intel Reserved.” The (G)MCH responds to accesses to Reserved address locations by completing the host cycle. When a Reserved register location is read, a zero value is returned. (Reserved registers can be 8-, 16-, or 32-bit in size). Writes to Reserved registers have no effect on the (G)MCH. Registers that are marked as Intel Reserved must not be modified by system software. Writes to Intel Reserved registers may cause system failure. Reads to Intel Reserved registers may return a non-zero value.

Upon a Full Reset, the (G)MCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options, or the states of poly-silicon fuses. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.

17.5 I/O Mapped Registers

The (G)MCH contains two registers that reside in the CPU I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

17.5.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DW
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access	Default Value	Description
31	R/W	0b	**Configuration Enable (CFGE):** When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24	RO	00h	**Reserved**
23:16	R/W	00h	**Bus Number:** If the Bus Number is programmed to 00h, the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is >=3 and not equal to 7), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by Device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of Device 1, a Type 0 PCI Configuration cycle will be generated on PCI Express-G. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of Device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of Device 1 a Type 1 PCI configuration cycle will be generated on PCI Express-G. This filed is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.
15:11	R/W	00h	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00" the (G)MCH decodes the Device Number field. The (G)MCH is always Device 0 for the Host bridge entity, Device 1 for the Host-PCI Express entity. Therefore, when the Bus Number=0 and the device equals 0, 1, 2 or 7 the internal (G)MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express and DMI Configuration cycles.

Bit	Access	Default Value	Description
10:8	R/W	000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express and DMI Configuration cycles.
7:2	R/W	00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express and DMI Configuration cycles.
1:0	RO	00b	**Reserved**

17.5.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access	Default Value	Description
31:0	R/W	0000 0000h	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the Bus, Device, Function, and Offset of the register to be accessed.

§

18 Host Bridge Device 0 Configuration Registers (D0:F0)

Warning: Address locations that are note listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

18.1 Device 0 Configuration Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	0	1	8086h	RO
Device Identification	DID	2	3	2A00h[1] 2A10h[2]	RO
PCI Command	PCICMD	4	5	0006h	RO; R/W
PCI Status	PCISTS	6	7	0090h	RO; R/WC
Revision Identification	RID	8	8	00h	RO
Class Code	CC	9	B	060000h	RO
Reserved		C	C		
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HDR	E	E	00h	RO
Reserved		F	2B		
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Reserved		30	33		
Capabilities Pointer	CAPPTR	34	34	E0h	RO
Egress Port Base Address	EPBAR	40	47	0000000000000000h	R/W/L; RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
(G)MCH Memory Mapped Register Range Base	MCHBAR	48	4F	0000000000000000h	R/W/L; RO; R/W
Reserved		50	51		
(G)MCH Graphics Control Register (Device 0)	GGC	52	53	0030h	RO; R/W/L
Device Enable	DEVEN	54	57	000043DBh	RO; R/W/L
Reserved		58	5F		
PCI Express Register Range Base Address	PCIEXBAR	60	67	00000000E0000000h	R/W/L; RO; R/W
MCH-ICH Serial Interconnect Ingress Root Complex	DMIBAR	68	6F	0000000000000000h	R/W; R/W/L; RO
Reserved		70	77		
PM I/O BAR Register Definition	PMIOBAR	78	7B	00000000h	R/W/L; RO
Reserved		7C	8F		
Programmable Attribute Map 0	PAM0	90	90	00h	RO; R/W/L
Programmable Attribute Map 1	PAM1	91	91	00h	RO; R/W/L
Programmable Attribute Map 2	PAM2	92	92	00h	RO; R/W/L
Programmable Attribute Map 3	PAM3	93	93	00h	RO; R/W/L
Programmable Attribute Map 4	PAM4	94	94	00h	RO; R/W/L
Programmable Attribute Map 5	PAM5	95	95	00h	RO; R/W/L
Programmable Attribute Map 6	PAM6	96	96	00h	RO; R/W/L
Legacy Access Control	LAC	97	97	00h	R/W/L; RO
Remap Base Address Register	REMAPBASE	98	99	03FFh	RO; R/W/L

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Remap Limit Address Register	REMAPLIMIT	9A	9B	0000h	RO; R/W/L
Reserved		9C	9C		
System Management RAM Control	SMRAM	9D	9D	02h	RO; R/W/L; R/W
Extended System Management RAM Control	ESMRAMC	9E	9E	38h	R/W/L; R/WC; RO
Reserved		9F	9F		
Top Of Memory	TOM	A0	A1	0001h	RO; R/W/L
Top of Upper Usable DRAM	TOUUD	A2	A3	0000h	R/W/L
Reserved		A4	AF		
Top of Low Used DRAM Register	TOLUD	B0	B1	0010h	R/W/L; RO
Reserved		B2	C7		
Error Status	ERRSTS	C8	C9	0000h	RO; R/WC/S
Error Command	ERRCMD	CA	CB	0000h	RO; R/W
Reserved		CC	DB		
Scratchpad Data	SKPD	DC	DF	00000000h	R/W
Capability Identifier	CAPID0	E0	E9	0000000000 00010A0009 h	RO
(G)MCH Dev0 Test	CRLT	F0	F0	00h	RO; R/WO
Reserved		F1	FF		

NOTES:

1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel® GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

18.1.1 VID - Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

18.1.2 DID - Device Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2-3h
Default Value: 2A00h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	2A00h[1] 2A10h[2]	**Device Identification Number (DID):** Identifier assigned to the (G)MCH core/primary PCI device.

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

18.1.3 PCICMD - PCI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: 4-5h
Default Value: 0006h
Access: RO; R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9	RO	0b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back write. Since Device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.

Bit	Access	Default Value	Description
8	R/W	0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have an SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over (G)MCH ICH Serial Interface (DMI) to the ICH. If this bit is set to a 1, the (G)MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the (G)MCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the (G)MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	RO	0b	**Parity Error Enable (PERRE):** PERRB is not implemented by the (G)MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	RO	0b	**VGA Palette Snoop Enable (VGASNOOP):** The (G)MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** The (G)MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	RO	0b	**Special Cycle Enable (SCE):** The (G)MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	RO	1b	**Bus Master Enable (BME):** The (G)MCH is always enabled as a master on DMI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	RO	1b	**Memory Access Enable (MAE):** The (G)MCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	RO	0b	**I/O Access Enable (IOAE):** This bit is not implemented in the (G)MCH and is hardwired to a 0. Writes to this bit position have no effect.

18.1.4 PCISTS - PCI Status

B/D/F/Type: 0/0/0/PCI
Address Offset: 6-7h
Default Value: 0090h
Access: RO; R/WC
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** The (G)MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	R/WC	0b	**Signaled System Error (SSE):** This bit is set to 1 when the (G)MCH Device 0 generates an SERR message over DMI for any enabled Device 0 error condition or Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers. Software clears this bit by writing a 1 to it.
13	R/WC	0b	**Received Unsupported Request (RURS):** This bit is set when the (G)MCH generates a DMI request that receives a Unsupported request completion. Software clears this bit by writing a 1 to it.
12	R/WC	0b	**Received Completion Abort Status (RCAS):** This bit is set when the (G)MCH generates a DMI request that receives a completion abort. Software clears this bit by writing a 1 to it.
11	RO	0b	**Signaled Target Abort Status (STAS):** The (G)MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the (G)MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	RO	00b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the (G)MCH.
8	RO	0b	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the (G)MCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	RO	1b	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the (G)MCH.
6:5	RO	00b	**Reserved**

Bit	Access	Default Value	Description
4	RO	1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this Device/Function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP Capability standard register resides.
3:0	RO	0h	**Reserved**

18.1.5 RID - Revision Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch.

18.1.6 CC - Class Code

B/D/F/Type: 0/0/0/PCI
Address Offset: 9-Bh
Default Value: 060000h
Access: RO
Size: 24 bits

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 06h, indicating a bridge device.
15:8	RO	00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of bridge into which the (G)MCH falls. The code is 00h indicating a host bridge.
7:0	RO	00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

18.1.7 MLT - Master Latency Timer

B/D/F/Type: 0/0/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Reserved**

18.1.8 HDR - Header Type

B/D/F/Type: 0/0/0/PCI
Address Offset: Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**PCI Header (HDR):** This field always returns 0 to indicate that the (G)MCH is a single function device with standard header layout. Reads and writes to this location have no effect.

18.1.9 SVID - Subsystem Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2C-2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

18.1.10 SID - Subsystem Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2E-2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

18.1.11 CAPPTR - Capabilities Pointer

B/D/F/Type: 0/0/0/PCI
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	E0h	**Pointer to the Offset of the First Capability ID Register Block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

18.1.12 EPBAR - Egress Port Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 40-47h
Default Value: 0000000000000000h
Access: R/W/L; RO; R/W
Size: 64 bits

This is the base address for the Egress Port Root Complex MMIO configuration space. This window of addresses contains the Egress Port Root Complex Register set for the PCI Express Hierarchy associated with the (G)MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.2-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to EPBAREN [bit 0 of this register].

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:12	R/W/L	000000h	**Egress Port RCRB Base Address:** This field corresponds to bits 35 to 12 of the base address Egress port RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the Egress Port RCRB and associated registers.
11:1	RO	000h	**Reserved**
0	R/W/L	0b	**EPBAR Enable (EPBAREN):** 0: EPBAR is disabled and does not claim memory. 1: EPBAR memory mapped accesses are claimed and decoded appropriately.

18.1.13 MCHBAR - (G)MCH Memory Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI
Address Offset: 48-4Fh
Default Value: 0000000000000000h
Access: R/W/L; RO; R/W
Size: 64 bits

This is the base address for the (G)MCH MMIO Configuration space. There is no physical memory within this 16-KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 54h, bit 28].

140h to 15Fh: Channel 0 System Memory Throttling.

1C0h to 1DFh: Channel 1 System Memory Throttling.

C80h to CEFh: Thermal Sensor Control.

F30h to F4Fh: PCI Express Throttling Control.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:14	R/W/L	000000h	**(G)MCH Memory Map Base Address:** This field corresponds to bits 35 to 14 of the base address MCHBAR configuration space. BIOS will program this register resulting in a base address for a 16-KB block of contiguous memory address space. This register ensures that a naturally aligned 16-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the (G)MCH register set.
13:1	RO	0000h	**Reserved**
0	R/W/L	0b	**MCHBAR Enable (MCHBAREN):** 0: MCHBAR is disabled and does not claim any memory. 1: MCHBAR memory mapped accesses are claimed and decoded appropriately.

18.1.14 GGC - (G)MCH Graphics Control Register (Device 0)

B/D/F/Type: 0/0/0/PCI
Address Offset: 52-53h
Default Value: 0030h
Access: RO; R/W/L
Size: 16 bits

Bit	Access	Default Value	Description
15:7	RO	000000000b	**Reserved**
6:4	R/W/L	011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Stolen Memory Bases is located between (TOLUD - SMSize) to TOUD. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0. Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. 101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. 110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. 111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. **NOTE:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.
3:2	RO	00b	**Reserved**
1	R/W/L	0b	**IGD VGA Disable (IVD):** 0: Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80.
0	RO	0b	**Reserved**

18.1.15 DEVEN - Device Enable

B/D/F/Type: 0/0/0/PCI
Address Offset: 54-57h
Default Value: 000043DBh
Access: RO; R/W/L
Size: 32 bits

Bit	Access	Default Value	Description
31:10	RO	0000h	**Reserved**
9:6	R/W/L	1b	**Reserved**
5	RO	0b	**Reserved**
4	R/W/L	1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible. If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.
3	R/W/L	1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden. 1: Bus 0 Device 2 Function 0 is enabled and visible. If this (G)MCH does not have internal graphics capability (CAPID0[33] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2	RO	0b	**Reserved**
1	R/W/L	1b	**PCI Express Graphics Port Enable (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden. Also gates PCI Express internal clock (lgclk) and asserts PCI Express internal reset (lgrstB). 1: Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities (CAPID0[32] and CAPID0[77]), SDVO presence HW strap and SDVO/PCIe concurrent HW strap..
0	RO	1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

18.1.16 PCIEXBAR - PCI Express Register Range Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 60-67h
Default Value: 00000000E0000000h
Access: R/W/L; RO; R/W
Size: 64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the (G)MCH. There is not actual physical memory within this 256-MB window that can be addressed. Each PCI Express Hierarchies requires a PCI Express BASE register. The (G)MCH supports one PCI Express hierarchy.

On reset, this register is disabled and must be enabled by writing a 1 to PCIEXBAREN [Dev 0, offset 54h, bit 31].

If the PCI Express Base Address [bits 35:28] were set to Fh, an overlap with the High BIOS area, APIC would result. Software must ensure that these ranges do not overlap. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). If a system is populated with more than 3.5 GB, either the PCI Express Enhanced Access mechanism must be disabled or the value in TOLUD must be reduced to report that only 3.5 GB are present in the system to allow a value of Eh for the PCI Express Base Address (assuming that all PCI 2.3-compatible configuration space fits above 3.75 GB).

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:28	R/W/L	00001110b	**PCI Express Base Address:** This field corresponds to bits 35 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits 3:1 of this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within total 36-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows : PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB The address used to access the PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB = PCI Express Base Address + 32 KB. Remember that this address is the beginning of the 4-KB space that contains both the PCI-compatible configuration space and the PCI Express extended configuration space.

Bit	Access	Default Value	Description
27	R/W/L	0b	**128-MB Address Mask:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	R/W/L	0b	**64-MB Base Address Mask:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
25:3	RO	000000h	**Reserved**
2:1	R/W/L	00b	**Length:** This field describes the length of this region - Enhanced Configuration Space Region/Buses Decoded 00: 256 MB (Buses 0-255). Bits 31:28 are decoded in the PCI Express Base Address field. 01: 128 MB (Buses 0-127). Bits 31:27 are decoded in the PCI Express Base Address field. 10: 64 MB (Buses 0-63). Bits 31:26 are decoded in the PCI Express Base Address field. 11: Reserved
0	R/W/L	0b	**PCIEXBAR Enable (PCIEXBAREN):** 0: PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR register bits 31:28 are R/W with no functionality behind them. 1: The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the (G)MCH.

18.1.17 DMIBAR - MCH-ICH Serial Interconnect Ingress Root Complex

B/D/F/Type: 0/0/0/PCI
Address Offset: 68-6Fh
Default Value: 0000000000000000h
Access: R/W; R/W/L; RO
Size: 64 bits

This is the base address for the DMI Root Complex MMIO configuration space. This window of addresses contains the DMI Root Complex Register set for the PCI Express Hierarchy associated with the (G)MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to RCBAREN [Dev 0, offset 54h, bit 29]

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:12	R/W/L	000000h	**DMI Root Complex MMIO Register Set Base Address:** This field corresponds to bits 35 to 12 of the base address DMI RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the DMI RCRB registers.
11:1	RO	000h	**Reserved**
0	R/W/L	0b	**DMIBAR Enable (DMIBAREN):** 0: DMIBAR is disabled and does not claim any memory. 1: DMIBAR memory mapped accesses are claimed and decoded appropriately.

18.1.18 PMIOBAR - PM I/O BAR Register Definition

B/D/F/Type: 0/0/0/PCI
Address Offset: 78-7Bh
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:6	R/W	000h	**Base Address:** Base address of the PM I/O Space.
5:1	RO	00h	**Reserved**
0	R/W	0b	**PM I/O BAR Enable:** BIOS should enable this bit after the base address for the PM I/O Bar is decided and allocated. This enable can be programmed while the Base Address is programmed. HOST Cluster should not positively decode level reads to PM I/O BAR base unless the space is enabled.

18.1.19 PAM0 - Programmable Attribute Map 0

B/D/F/Type:	0/0/0/PCI
Address Offset:	90h
Default Value:	00h
Access:	RO; R/W/L
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h-0FFFFFh.

The (G)MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 640-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the CPU read accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size.

Accesses to the entire PAM region (000C_0000h to 000F_FFFFh) from DMI and PCI Express Graphics Attach low priority will be forwarded to main memory. The PAM read enable and write enable bits are not functional for these accesses. In other words, a full set of PAM decode/attribute logic is not being implemented. Also note that the (G)MCH may hang if a PCI Express Graphics Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM). For these reasons the following critical restriction is placed on the programming of the PAM regions:

At the time that a DMI or PCI Express Graphics Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0F0000-0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000 to 0FFFFF. 00: DRAM Disabled: All accesses are directed to DMI. 01: Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0	RO	0h	**Reserved**

18.1.20 PAM1 - Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI
Address Offset: 91h
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h-0C7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0C4000-0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0C0000-0C3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000 to 0C3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

18.1.21 PAM2 - Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI
Address Offset: 92h
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h-0CFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0CC000-0CFFFF Attribute (HIENABLE):** Reserved 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0C8000-0CBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000 to 0CBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

18.1.22 PAM3 - Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI
Address Offset: 93h
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h-0D7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0D4000-0D7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000 to 0D7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0D0000-0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000 to 0D3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

18.1.23 PAM4 - Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI
Address Offset: 94h
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0DC000-0DFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000 to 0DFFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0D8000-0DBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000 to 0DBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

18.1.24 PAM5 - Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI
Address Offset: 95h
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0E4000-0E7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0E0000-0E3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

18.1.25 PAM6 - Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI
Address Offset: 96h
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h-0EFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	R/W/L	00b	**0EC000-0EFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0EC000 to 0EFFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	**Reserved**
1:0	R/W/L	00b	**0E8000-0EBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E8000 to 0EBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

18.1.26 LAC - Legacy Access Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 97h
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

Bit	Access	Default Value	Description
7	R/W/L	0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0: No memory hole. 1: Memory hole from 15 MB to 16 MB.
6:1	RO	00h	**Reserved**
0	R/W/L	0b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if Device 1's VGA Enable bit is not set. If Device 1's VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh are forwarded to DMI. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express-G if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O:3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh (including ISA address aliases, A[15:10] are not used in decode). Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN / MDAP / Description 0 / 0 / All references to MDA and VGA space are routed to HI 0 / 1 / Illegal Combination 1 / 0 / All VGA and MDA references are routed to PCI Express Graphics Attach 1 / 1 / All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to HI.

18.1.27 REMAPBASE - Remap Base Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 98-99h
Default Value: 03FFh
Access: RO; R/W/L
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:0	R/W/L	3FFh	**Remap Base Address[35:26]:** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0's. Thus the bottom of the defined memory range will be aligned to a 64-MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled. This field defaults to 3FFh. **NOTE:** Bit 0 (Address Bit 26) must be a 0

18.1.28 REMAPLIMIT - Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 9A-9Bh
Default Value: 0000h
Access: RO; R/W/L
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:0	R/W/L	000h	**Remap Limit Address [35:26]:** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Limit Address are assumed to be F's. Thus the top of the defined range will be one less than a 64-MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. This field defaults to 00h. **NOTE:** Bit 0 (Address Bit 26) must be a 0.

18.1.29 SMRAM - System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Dh
Default Value: 02h
Access: RO; R/W/L; R/W
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access	Default Value	Description
7	RO	0b	**Reserved**
6	R/W/L	0b	**SMM Space Open (D_OPEN):** (When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W	0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	R/W/L	0b	**SMM Space Locked (D_LCK):** When D_LCK is set to a 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, G_SMRARE, C_BASE_SEG, H_SMRAM_EN, GMS, TOLUD, TOM, TSEG_SZ, and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W/L	0b	**Global SMRAM Enable (G_SMRARE):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.

Bit	Access	Default Value	Description
2:0	RO	010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the (G)MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

18.1.30 ESMRAMC - Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Eh
Default Value: 38h
Access: R/W/L; R/WC; RO
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Enable High SMRAM (H_SMRAME):** Controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/WC	0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when CPU has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO	1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the (G)MCH .
4	RO	1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the (G)MCH.
3	RO	1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the (G)MCH.

Bit	Access	Default Value	Description
2:1	R/W/L	00b	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. 00: 1-MB Tseg. (TOLUD: Graphics Stolen Memory Size - 1M) to (TOLUD - Graphics Stolen Memory Size). 01: 2-MB Tseg (TOLUD: Graphics Stolen Memory Size - 2M) to (TOLUD - Graphics Stolen Memory Size). 10: 8-MB Tseg (TOLUD: Graphics Stolen Memory Size - 8M) to (TOLUD - Graphics Stolen Memory Size). 11: Reserved Once D_LCK has been set, these bits become read only.
0	R/W/L	0b	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

18.1.31 TOM - Top of Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A0-A1h
Default Value: 0001h
Access: RO; R/W/L
Size: 16 bits

This register contains the size of physical memory. BIOS determine the memory size reported to the OS using this register.

Bit	Access	Default Value	Description
15:9	RO	00h	**Reserved**
8:0	R/W/L	001h	**Top of Memory:** This register reflects the total amount of populated physical memory. This is also the amount of addressable physical memory when remapping is used appropriate to ensure that no physical memory is wasted. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address bits 35:27 (128-MB granularity). Bits 26:0 are assumed to be 0.

18.1.32 TOUUD - Top of Upper Usable DRAM

B/D/F/Type:	0/0/0/PCI
Address Offset:	A2-A3h
Default Value:	0000h
Access:	R/W/L
Size:	16 bits

Configuration software must set this value to TOM minus all Manageability Engine stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 64-MB aligned since reclaim limit is 64-MB aligned. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4 GB.

Bit	Access	Default Value	Description
15:0	R/W/L	0000h	**Top of Upper Usable DRAM (TOUUD):** This register contains bits 35 to 20 of an address one byte above the maximum DRAM memory above 4 GB that is usable by the operating system. Configuration software must set this value to TOM minus all Manageability Engine stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 64-MB aligned since reclaim limit is 64-MB aligned. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4 GB.

18.1.33 TOLUD - Top of Low Used DRAM Register

B/D/F/Type:	0/0/0/PCI
Address Offset:	B0-B1h
Default Value:	0010h
Access:	R/W/L; RO
Size:	16 bits

This 16 bit register defines the Top of Low Usable DRAM. Graphics Stolen Memory and TSEG are within dram space defined under TOLUD. From the Top of Low Usable DRAM, (G)MCH claims 1 to 64 MBs of DRAM for internal graphics if enabled and 1, 2 or 8 MBs of DRAM for TSEG if enabled.

Note: Even if the OS does not need any PCI space, TOLUD can only be programmed to FFh. This ensures that addresses within 128 MB below 4 GB that are reserved for APIC

Bit	Access	Default Value	Description
15:4	R/W/L	001h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4 G that is usable by the operating system. Address bits 31 down to 20 programmed to a "001h" implies a minimum memory size of 1 M. Configuration software must set this value to the smaller of the following 2 choices : - maximum amount memory in the system minus Intel® Management Engine stolen memory plus 1 byte or - the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than that value programmed in this register. This register must not be set to 00000h Note that the Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. **NOTE:** This register **must** be 64-M aligned when reclaim is enabled.
3:0	RO	0h	**Reserved**

18.1.34 ERRSTS - Error Status

B/D/F/Type: 0/0/0/PCI
Address Offset: C8-C9h
Default Value: 0000h
Access: RO; R/WC/S
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**Reserved**
14:13	R/WC/S	00b	**Reserved**
12	R/WC/S	0b	**(G)MCH Software Generated Event for SMI:** This indicates the source of the SMI was a Device 2 Software Event.
11	R/WC/S	0b	**(G)MCH Thermal Sensor Event for SMI/SCI/SERR:** Indicates that a (G)MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10	RO	0b	**Reserved**
9	R/WC/S	0b	**LOCK to Non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the (G)MCH has detected a lock operation to memory space that did not map into DRAM.
8	R/WC/S	0b	**Received Refresh Timeout Flag (RRTOF):** This bit is set when 1024 memory core refreshes are enqueued.
7	R/WC/S	0b	**DRAM Throttle Flag (DTF):** 0: Software has cleared this flag since the most recent throttling event. 1: Indicates that a DRAM Throttling condition occurred.
6:0	RO	00h	**Reserved**

18.1.35 ERRCMD - Error Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CA-CBh
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:12	RO	0h	**Reserved**
11	R/W	0b	**SERR on (G)MCH Thermal Sensor Event (TSESERR):** 0: Reporting of this condition via SERR messaging is disabled. 1: The (G)MCH generates a SERR DMI special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event.
10	RO	0b	**Reserved**
9	R/W	0b	**SERR on LOCK to Non-DRAM Memory (LCKERR):** 0: Reporting of this condition via SERR messaging is disabled. 1: The (G)MCH will generate a DMI SERR special cycle whenever a CPU lock cycle is detected that does not hit DRAM
8	R/W	0b	**SERR on DRAM Refresh Timeout (DRTOERR):** 0: Reporting of this condition via SERR messaging is disabled. 1: The (G)MCH generates an SERR DMI special cycle when a DRAM Refresh timeout occurs.
7	R/W	0b	**SERR on DRAM Throttle Condition (DTCERR):** 0: Reporting of this condition via SERR messaging is disabled. 1: The (G)MCH generates an SERR DMI special cycle when a DRAM Read or Write Throttle condition occurs.
6:0	RO	00h	**Reserved**

18.1.36 SKPD - Scratchpad Data

B/D/F/Type: 0/0/0/PCI
Address Offset: DC-DFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access	Default Value	Description
31:0	R/W	00000000h	**Scratchpad Data:** 1 Dword of data storage.

18.1.37 CAPID0 - Capability Identifier

B/D/F/Type: 0/0/0/PCI
Address Offset: E0-E9h
Default Value: 000000000000010A0009h
Access: RO
Size: 80 bits

Bit	Access	Default Value	Description
79	RO	0b	**Reserved**
78	RO	0b	**X4 DMI Link Width Capability Disable:** 0: MCH - ICH Serial Interface is capable of X4 or X2 link widths. 1: MCH - ICH Serial Interface is a X2 link, not capable of X4.
77	RO	0b	**Concurrent PCI-E and SDVO Enable :** Controls whether concurrent use of PCI-E Graphics Port and SDVO is allowed. 0: Concurrent PCIe and SDVO is not allowed. 1: Concurrent PCIe and SDVO is allowed.
76:62	RO	0000b	**Reserved**
61:58	RO	0000b	**Compatibility Revision ID:** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. For the A-0 Stepping, this value is 00h.
57:45	RO	0b	**Reserved**
44:42	RO	000b	**GFX Software Capability ID** Used to communicate Graphics SKU information to the Graphics Driver software, which can enable/disable certain features based on the product SKU.

Bit	Access	Default Value	Description
41:37	RO	0b	**Reserved**
36:35	RO	00b	**Reserved**
34	RO	0b	**Serial Digital Video Out Enable:** 0: (G)MCH Not capable of serial digital video output. 1: (G)MCH capable of serial digital video output.
33	RO	0b	**Internal Graphics Disable:** 0: There is a graphics engine within this GMCH. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the GMCH. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Device 1 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GMCH Control Register). Graphics Memory is pre-allocated above TSEG Memory. 1: There is no graphics engine within this GMCH. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, All clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1. DEVEN [4:3] (Device 0, offset 54h) are forced to 00have no meaning. Device 2 Functions 0 and 1 are disabled and hidden. In addition, the memory decoding for LT trusted graphics registers at 0xFED305xx is also disabled.
32	RO	0b	**PCI Express Port Disable:** 0: There is a PCI Express GFX Attach on this GMCH. Device 1 and associated memory spaces are accessible. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1 and VGA settings controlling internal graphics VGA if internal graphics is enabled. 1: There is no PCI Express GFX Attach on this (G)MCH. Device 1 and associated memory and IO spaces are disabled. In addition, Next_Pointer = 00h, VGA memory and IO cannot decode to the PCI Express interface. VGA memory and IO cannot decode to the PCI Express interface. From a Physical Layer perspective, all 16 lanes are powered down and the link does not attempt to train.
31	RO	0b	**Reserved**

Bit	Access	Default Value	Description
30	RO	0b	**DDR2 Frequency Capability:** 0: (G)MCH capable of "All" memory frequencies (DDR2 667 MHz or lower). 1: (G)MCH capable of up to DDR2-533. This field controls which values may be written to the Memory Frequency Select field 6:4 of the Clocking Configuration Register (MCHBAR Offset C00h). Any attempt to write an unsupported value will be ignored.
29:28	RO	00b	**FSB Capability:** These values are determined by the BSEL[2:0] frequency straps. Any unsupported straps will render the GMCH host interface inoperable. 01: (G)MCH capable of up to FSB 800 MHz. 10-11: (G)MCH capable of up to FSB 667 MHz.
27:24	RO	1h	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO	0Ah	**CAPID Length:** This field has the value 0Ah to indicate the structure length (10 bytes).
15:8	RO	00h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO	09h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

18.1.38 CRLT – (G)MCH Dev0 Test

B/D/F/Type: 0/0/0/PCI
Address Offset: F0h
Default Value: 00h
Access: RO; R/WO
Size: 8 bits

Bit	Access	Default Value	Description
7:1	RO	00h	**Reserved**
0	R/WO	0b	**Intel® Management Engine Stolen Memory Lock (ME_SM_LOCK2)**: ME_SM_LOCK2 can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. BIOS will initialize config bits related to dram decode and then use ME_SM_LOCK2 to "lock down" the dram decode in the future so that no application software (or BIOS itself) can violate the integrity.

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19 Device 0 Memory Mapped I/O Register

Note: All accesses to the Memory Mapped registers must be made as a single Dword (4 bytes) or less. Access must be aligned on a natural boundary.

19.1 Device 0 Memory Mapped I/O Registers

A variety of timing and control registers have been moved to MMR space of Device 0 due to space constraints.

To simplify the read/write logic to the SRAM, BIOS is required to write and read 32-bit aligned Double Words. The SRAM includes a separate Write Enable for every Double Word.

The BIOS read/write cycles are performed in a memory mapped IO range that is setup for this purpose in the PCI configuration space, via standard PCI range scheme.

19.2 Device 0 MCHBAR Chipset Control Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		00	3F		
Front Side Bus Power Management Control 3	FSBPMC3	40	43	00000000h	RO; R/W
Front Side Bus Power Management Control 4	FSBPMC4	44	47	00000002h	R/W
FSB Snoop Control	FSBSNPCTL	48	4B	80800000h	RO; R/W
Reserved		4C	8F		
CPU Sleep Timing Control	SLPCTL	90	93	00005055h	RO; R/W
Front Side Bus Power Management Control 5	FSBPMC5	94	97	00010080h	R/W
Reserved		98	1FF		

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DRAM Channel Control	DCC	200	203	00000000h	RO; R/W; R/W/L
DRAM Channel Control 2	DCC2	204	207	00000000h	RO; R/W/L
Reserved		208	217		
Write Cache Control	WCC	218	21B	A4008000h	RO; R/W
Reserved		21C	21F		
Main Memory Arbiter Control_0	MMARB0	220	223	00000264h	RO; R/W
Main Memory Arbiter Control_1	MMARB1	224	227	00000000h	RO; R/W
Reserved		228	22F		
SB Test Register	SBTEST	230	233	340A0000h	RO; R/W
Reserved		234	2BF		

19.2.1 FSBPMC3 – Front Side Bus Power Management Control 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 40-43h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.2 FSBPMC4 – Front Side Bus Power Management Control 4

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 44-47h
Default Value: 00000002h
Access: R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.3 FSBSNPCTL – FSB Snoop Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 48-4Bh
Default Value: 80800000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.4 SLPCTL – CPU Sleep Timing Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 90-93h
Default Value: 00005055h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.5 FSBPMC5 – Front Side Bus Power Management Control 5

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 94-97h
Default Value: 00010080h
Access: R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.6 DCC - DRAM Channel Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 200-203h
Default Value: 00000000h
Access: RO; R/W; R/W/L
Size: 32 bits

This register controls how the DRAM channels work together. It affects how the CxDRB registers are interpreted and allows them to steer transactions to the correct channel.

Bit	Access	Default Value	Description
31:29	RO	000b	**Reserved**
28:24	R/W	00h	**Reserved**
23	RO	0b	**Reserved**

Bit	Access	Default Value	Description
22:21	R/W	00b	**Select for EMRS Commands:** This field applies only when the Mode Select (SMS) bits = 100, implying an EMRS command. 00: Bank 1 (BS[2:0] = 001), EMRS(1) 01: Bank 2 (BS[2:0] = 010), EMRS(2) 10: Bank 3 (BS[2:0] = 011), EMRS(3) 11: Reserved
20	R/W	0b	**Independent Dual Channel IC/SMS Enable:** 0: IC and SMS controls in DCC register control both system memory channels. 1: IC and SMS bits in C0/1DRC0 register control each system memory channel independently.
19	R/W	0b	**Initialization Complete (IC):** See register description in C0DRC0[29].
18:16	R/W	000b	**Mode Select (SMS):** See register description in C0DRC0[6:4].
15	R/W	0b	**Reserved**
14:11	RO	0000b	**Reserved**
10	R/W/L	0b	**Channel XOR Disable (CXRDIS):** 0: Channel XOR Randomization is enabled. 1: Channel XOR Randomization is disabled.
9	R/W/L	0b	**Reserved**
8:2	RO	0000000b	**Reserved**
1	R/W/L	0b	**DRAM Addressing Mode Control (DAMC):** 0: Single Channel/Dual Channel Asymmetric. 1: Dual Channel symmetric.
0	RO	0b	**Reserved**

19.2.7 DCC2 - DRAM Channel Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 204-207h
Default Value: 00000000h
Access: RO; R/W/L
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:0	R/W/L	0000h	**Intel® Management Engine Size (MESZ):** This register indicates total memory which is mapped to ME-UMA(Sx) region operation (1-MB Granularity).

19.2.8 WCC - Write Cache Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 218-21Bh
Default Value: A4008000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.9 MMARB0 - Main Memory Arbiter Control_0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 220-223h
Default Value: 00000264h
Access: RO; R/W
Size: 32 bits
BIOS Optimal Default 0h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.10 MMARB1 - Main Memory Arbiter Control_1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 224-227h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.2.11 SBTEST - SB Test Register

B/D/F/Type: 0/0/0/MCHBAR Chipset
Address Offset: 230-233h
Default Value: 340A0000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.3 Device 0 MCHBAR Clock Controls

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Clocking Configuration	CLKCFG	C00	C03	00000200h	RO; R/W
Reserved		C04	C13		
Unit Power Management Control 1	UPMC1	C14	C15	0223h	RO; R/W
CPunit Control	CPCTL	C16	C17	00A0h	RO; R/W
Reserved		C18	C1B		
Sticky Scratchpad Data	SSKPD	C1C	C1D	0000h	R/W/S
Reserved		C1E	C1F		
Unit Power Management Control 2	UPMC2	C20	C21	0001h	RO; R/W
Reserved		C22	C33		
Host-Graphics Interface Power Management Control 1	HGIPMC1	C34	C37	00000000h	R/W
Host-Graphics Interface Power Management Control 2	HGIPMC2	C38	C3B	00000000h	R/W
Reserved		C3C	C67		

19.3.1 CLKCFG - Clocking Configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C00-C03h
Default Value: 00000200h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31	R/W	0b	**Reserved**
30:28	RO	000b	**Reserved**
27:15	R/W	0000h	**Reserved**
14	R/W	0b	**HW Dynamic FSB Frequency Switching Enable:** 0: OFF 1: ON
7	R/W	0b	**VHCLK Polarity in Half-mode (VHCLK_polarity):** Dynamic FSB Frequency Switching vhclk inversion in ½-frequency mode. 0: Do not invert polarity 1: Invert vhclk polarity when entering ½-frequency mode
6:4	RO	000b	**Memory Frequency Select:** The clock config straps, update the default value of this register. 011: 533 100: 667 others: Reserved
3	R/W	0b	**Reserved**
2:0	RO	000b	**FSB Frequency Select:** Reflects the State of BSEL pins from the Processor. BSEL(2:0) selects the FSB frequency as defined below: 001: FSB533 011: FSB667 010: FSB800 Others: Reserved Attempts to strap values to unsupported frequencies will shut down the host PLL.

19.3.2 UPMC1 – Unit Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C14-C15h
Default Value: 0223h
Access: RO; R/W
Size: 16 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.3.3 CPCTL - CPunit Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C16-C17h
Default Value: 00A0h
Access: RO; R/W
Size: 16 bits

This register bit shall contain the default value unless otherwise indicated in the BIOS Specification.

19.3.4 SSKPD - Sticky Scratchpad Data

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C1C-C1Dh
Default Value: 0000h
Access: R/W/S
Size: 16 bits

This register holds 16 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers. This Register is reset on PWROK.

Bit	Access	Default Value	Description
15:0	R/W/S	0000h	**Scratchpad Data:** 1 WORD of data storage.

19.3.5 UPMC2 – Unit Power Management Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C20-C21h
Default Value: 0001h
Access: RO; R/W
Size: 16 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.3.6 HGIPMC1 – Host-Graphics Interface Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C34-C37h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.3.7 HGIPMC2 – Host-Graphics Interface Power Management Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: C38-C3Bh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.4 Device 0 MCHBAR ACPI Power Management Controls

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
C2 to C3 Transition Timer	C2C3TT	F00	F03	00000000h	RO; R/W
C3 to C4 Transition Timer	C3C4TT	F04	F07	00000000h	RO; R/W
Reserved		F08	F0D		
Memory Interface Power Management Control	MIPMC	F0E	F0E	00h	R/W
Reserved		F0F	F13		
Self-Refresh Channel Status	SLFRCS	F14	F17	00000000h	R/WC; RO
Reserved		F18	FAF		

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Graphics Interface Power Management Control 1	GIPMC1	FB0	FB0	00h	RO; R/W
Reserved		FB1	FB7		
Front Side Bus Power Management Control 1	FSBPMC1	FB8	FBB	00h	RO; R/W
Reserved		FBC	FBF		
Unit Power Management Control 3	UPMC3	FC0	FC3	00000000h	RO; R/W
Reserved		FFC	FFF		

19.4.1 C2C3TT - C2 to C3 Transition Timer

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F00-F03h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:19	RO	0000h	**Reserved**
18:7	R/W	000h	**C2 to C3 Transition Timer (C2C3TT):** Dual purpose timer in 128-core clock granularity. Number of core clocks to wait between last snoop from PEG or DMI to a Req_C3 DMI message being issued. Timer is activated only when the WAIT_C3 message from DMI has been received when in C2. 000 = 128 host clocks FFF = 524288 host clocks MSI's, for the purpose of this register, are handled as snoops.
6:0	RO	00h	**Reserved**

19.4.2 C3C4TT - C3 to C4 Transition Timer

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F04-F07h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:19	RO	0000h	**Reserved**
18:7	R/W	000h	**C3 to C4 Transition Timer (C34TT):** 128-core clock granularity. Number of core clocks to wait between last snoop from PEG or DMI to a Req_C4 DMI message being issued. Timer is activated only when the WAIT_C4 message from DMI has been received when in C3. **NOTES:** 000 = 128 host clocks FFF = 524288 host clocks MSI's, for the purpose of this register, are handled as snoops.
6:0	RO	00h	**Reserved**

19.4.3 MIPMC - Memory Interface Power Management Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F0Eh
Default Value: 00h
Access: R/W
Size: 8 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS specification.

19.4.4 SLFRCS - Self-Refresh Channel Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F14-F17h
Default Value: 00000000h
Access: RO; R/WC
Size: 32 bits

This register is reset by PWROK only.

Bit	Access	Default Value	Description
31:2	RO	00000000h	**Reserved**
1	R/WC	0b	**Warm Reset Event Occurred (RST_EVNT):** Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. If Memory has not been initialized yet, then memory will not be put into self refresh and the Reset_Warn_Ack message will not be sent.
0	R/WC	0b	**Channels in Self-refresh:** Set by power management hardware after both memory channels are placed in self refresh as a result of a Power State or a Reset Warn sequence, Cleared by Power management hardware before starting self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing a 1 in a warm reset (H_CPURST# asserted while PWROK is asserted) exit sequence. 0: Both Channels are not guaranteed to be in self refresh. 1: Both Channels are in self refresh.

19.4.5 GIPMC1 – Graphics Interface Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FB0h
Default Value: 00h
Access: RO; R/W
Size: 8 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.4.6 FSBPMC1 – Front Side Bus Power Management Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FB8h
Default Value: 00h
Access: RO; R/W
Size: 8 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.4.7 UPMC3 – Unit Power Management Control 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: FC0-FC3h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits
BIOS Optimal Default 0h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.5 Device 0 MCHBAR Thermal Management Controls

Note: The Intel Express Chipset has two internal thermal sensors. The set of registers from MCHBAR Offset 1000h to 101Fh correspond to Thermal Sensor 1 and the set of registers from MCHBAR Offset 1040h to 105Fh correspond to Thermal Sensor 2 respectively.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		1000	1000		
Thermal Sensor Control 1	TSC1	1001	1002	0000h	R/W/L; R/W; R/WC
Reserved		1003	1003		
Thermal Sensor Status 1	TSS1	1004	1005	0000h	RO
Thermometer Read 1	TR1	1006	1006	FFh	RO
Thermometer Offset 1	TOF1	1007	1007	00h	R/W
Relative Thermometer Read 1	RTR1	1008	1008	00h	RO
Reserved		1009	100A		
Thermometer Integrator Control 1	TIC1	100B	100B	00h	RO; R/W/L

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Thermometer Moving Average Control 1	TMAC1	100C	100C	00h	R/W/L; RO
Thermometer Moving Average 1	TMA1	100D	100D	00h	RO
Thermometer Sample Integrator 1	TSI1	100E	100E	00h	RO
Temperature Sensor1 Power Management	TSPM1	100F	100F	00h	R/W
Thermal Sensor Temperature Trip Point A1	TSTTPA1	1010	1013	00000000h	RO; R/W/L; R/WO
Thermal Sensor Temperature Trip Point B1	TSTTPB1	1014	1017	00000000h	R/W/L
Thermal Calibration Offset 1	TCO1	1018	1018	00h	R/W/L
Reserved		1019	101B		
Hardware Throttle Control 1	HWTHROTCTRL1	101C	101C	00h	R/W/L; RO; R/WO
TCO Fuse 1	TCOFUSE1	101D	101D	_0xxx__xxxx_h	R/WC; RO
Thermal Interrupt Status 1	TIS1	101E	101F	0000h	R/WC
Reserved		1020	1040		
Thermal Sensor Control 2	TSC2	1041	1042	0000h	R/WC; R/W/L; R/W
Reserved		1043	1043		
Thermal Sensor Status 2	TSS2	1044	1045	0000h	RO
Thermometer Read 2	TR2	1046	1046	FFh	RO
Thermometer Offset 2	TOF2	1047	1047	00h	R/W
Relative Thermometer Read 2	RTR2	1048	1048	00h	RO
Reserved		1049	104A		
Thermometer Integrator Control 2	TIC2	104B	104B	00h	RO; R/W/L
Thermometer Moving Average Control 2	TMAC2	104C	104C	00h	R/W/L; RO
Thermometer Moving Average 2	TMA2	104D	104D	00h	RO
Thermometer Sample Integrator 2	TSI2	104E	104E	00h	RO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Temperature Sensor2 Power Management	TSPM2	104F	104F	00h	R/W
Thermal Sensor Temperature Trip Point A2	TSTTPA2	1050	1053	00000000h	RO; R/W/L; R/WO
Thermal Sensor Temperature Trip Point B2	TSTTPB2	1054	1057	00000000h	R/W/L
Thermal Calibration Offset 2	TCO2	1058	1058	00h	R/W/L
Reserved		1059	105B		
Hardware Throttle Control 2	HWTHROTCTRL2	105C	105C	00h	RO; R/W/L; R/WO
TCO Fuse 2	TCOFUSE2	105D	105D	_0xxx__xxxx_h	RO; R/WC
Thermal Interrupt Status 2	TIS2	105E	105F	0000h	R/WC
Reserved		1060	1069		
Thermometer Mode Enable and Rate	TERATE	1070	1070	00h	R/W
Reserved		1071	107F		
Thermal Sensor Rate Control	TSRCTRL	1080	1080	06h	R/W
Reserved		1081	10DF		
In Use Bits	IUB	10E0	10E3	00000000h	RO; R/WC
Thermal Error Command	TERRCMD	10E4	10E4	00h	R/W
Thermal SMI Command	TSMICMD	10E5	10E5	00h	R/W
Thermal SCI Command	TSCICMD	10E6	10E6	00h	R/W
Thermal INTR Command	TINTRCMD	10E7	10E7	00h	R/W
External Thermal Sensor Control and Status	EXTTSCS	10EF	10EF	00h	R/W; R/WO; R/W/L; RO

19.5.1 TSC1 - Thermal Sensor Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1001-1002h
Default Value: 0000h
Access: R/W/L; R/W; R/WC
Size: 16 bits
BIOS Optimal Default 00h

This register controls the operation of the internal thermal sensor located in the graphics hot spot.

Bit	Access	Default Value	Description
15	R/W/L	0b	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO1 bit 7. 0: Disabled 1: Enabled
14	R/W	0b	**Reserved**
13:10	R/W	0000b	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0000: digital hysteresis disabled, no offset added to trip temperature 0001: offset is 1 LSB added to each trip temperature when tripped ... 0100: ~3.0ºC (Recommended setting) ... 1110: 14 LSB added to each trip temperature when tripped 1111: 15 LSB added to each trip temperature when tripped
9	R/W/L	0b	**Reserved**
8	R/WC	0b	**In Use (IU):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor.
7:0	RO	00h	**Reserved**

19.5.2 TSS1 - Thermal Sensor Status 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1004-1005h
Default Value: 0000h
Access: RO
Size: 16 bits
BIOS Optimal Default 00h

This read only register provides trip point and other status of the thermal sensor.

Bit	Access	Default Value	Description
15:11	RO	0h	**Reserved**
10	RO	0b	**Thermometer Mode Output Valid:** 1: Thermometer mode is able to converge to a temperature and that the TR1 register is reporting a reasonable estimate of the thermal sensor temperature. 0: Thermometer mode is off, or that temperature is out of range, or that the TR1 register is being looked at before a temperature conversion has had time to complete.
9:6	RO	0h	**Reserved**
5	RO	0b	**Catastrophic Trip Indicator (CTI):** A 1 indicates that the internal thermal sensor temperature is above the catastrophic setting.
4	RO	0b	**Hot Trip Indicator (HTI):** A 1 indicates that the internal thermal sensor temperature is above the Hot setting.
3	RO	0b	**Aux3 Trip Indicator (A3TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux3 setting.
2	RO	0b	**Aux2 Trip Indicator (A2TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux2 setting.
1	RO	0b	**Aux1 Trip Indicator (A1TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux1 setting.
0	RO	0b	**Aux0 Trip Indicator (A0TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux0 setting.

19.5.3 TR1 - Thermometer Read 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1006h
Default Value: FFh
Access: RO
Size: 8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled.

Bit	Access	Default Value	Description
7:0	RO	FFh	**Thermometer Reading (TR):** Provides the current counter value. The current counter value corresponds to thermal sensor temperature if TSS1 [10] = 1. This register has a straight binary encoding that will range from 0 to FFh.

19.5.4 TOF1 - Thermometer Offset 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1007h
Default Value: 00h
Access: R/W
Size: 8 bits

This register is used for programming the thermometer offset.

Bit	Access	Default Value	Description
7:0	R/W	00h	**Thermometer Offset (TOF):** This value is used to adjust the current thermometer reading so that the TR1 value is not relative to a specific trip or calibration point, and is positive going for positive increases in temperature. The initial default value is 00h and software must determine the correct temperature adjustment that corresponds to a zero reading by reading the fuses and referring to the temperature tables, and then programming the computed offset into this register.

19.5.5 RTR1 - Relative Thermometer Read 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1008h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the relative temperature.

Bit	Access	Default Value	Description
7:0	RO	00h	**Relative Thermometer Reading (RTR1):** In Thermometer mode, this register reports the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to TOF1. TR1 and TSTTPA1.HTPS can both vary between 0 and 255. But RTR1 will be clipped between 127 to keep it an 8-bit number. See also TSS1[10].

19.5.6 TIC1 - Thermometer Integrator Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 100Bh
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits
BIOS Optimal Default 0h

This register controls the operation of the integrator filter. For a given thermal solution the inter-component thermals may be on the order of tens of seconds, while intra-component transients may be on the order of milliseconds, the filters are programmable for a range of time intervals.

Bit	Access	Default Value	Description
7	R/W/L	0b	**TIC1 Lock (TIC1LOCK):** This bit secures this register. Once a 1 is written to this bit, all the bits of this register become read-only.
6	RO	0b	**TIC1 Samples (TIC1SAMP):** When set to 1, this bit indicates that enough samples have been collected by the integrator over the interval specified by TIC1[2:0].
5	R/W/L	0b	**Reserved**
4:3	RO	0h	**Reserved**
2:0	R/W/L	0h	**Sample Interval for the Integrator (TICINTRVL):** Sample interval for the integrator 000: p = 4 001: p = 6 010: p = 8 011: p = 10 100: p = 12 101: p = 14 110-111: Reserved This time constant must be greater than or equal to the time constant of the moving average filter (TMAC1[2:0]).

19.5.7 TMAC1 - Thermometer Moving Average Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 100Ch
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits
BIOS Optimal Default 0h

This register controls the operation of the moving average filter. For a given thermal solution the inter-component thermals may be on the order of tens of seconds, while intra-component transients may be on the order of milliseconds, the filters are programmable for a range of time intervals.

Bit	Access	Default Value	Description
7	R/W/L	0b	**TMAC1 Lock (TMACLOCK):** This bit secures this register. Once a 1 is written to this bit, all of the configuration register bits are read-only.
6	RO	0b	**TMAC1 Samples (TMAC1SAMP):** When set to 1, this bit indicates that enough samples have been collected by the moving average filter over the interval specified by TMCM.
5:5	RO	0h	**Reserved**
4	R/W/L	0b	**Throttle Test Mode Enable (TME):** This bit is used to shorten the filter. 0: Normal Operation 1: Filter time constant is at 2^27
3:3	RO	0h	**Reserved**
2:0	R/W/L	0h	**Sample Interval for the Moving Average (TMCINTRVL):** Sample interval for the moving average 000: Reserved 001: alpha = 1/4 (p=2) 010: alpha = 1/16 (p=4) 011: alpha = 1/64 (p=6) 100-111: Reserved

19.5.8 TMA1 - Thermometer Moving Average 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 100Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register provides a moving average of the thermometer samples.

Bit	Access	Default Value	Description
7:0	RO	00h	**Thermometer Reading Moving Average (TMA):** This register provides a moving average of thermometer samples. The average is derived via weighted recursive filter with DC pass-through meaning that when the temperature is stable it will read the current temperature. This represents the sample over the interval set in TIC1, TMAC1. After a hardware reset, or when the sample interval is changed, the filter will be cleared and the current temperature will be displayed.

19.5.9 TSI1 - Thermometer Sample Integrator 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 100Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Thermometer Sample Integrator (TSI):** The integrator accumulates the thermometer samples and integrates over the interval programmed in TIC1, TMAC1. After a hardware reset, or when the sample interval is changed, the filter will be cleared and the current temperature will be displayed.

19.5.10 TSPM1 - Temperature Sensor1 Power Management

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	100Fh
Default Value:	00h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	00h

This register specifies the power management C-state dependencies for the temperature sensor.

Bit	Access	Default Value	Description
7:1	RO	0h	**Reserved**
0	R/W	0b	**Disable Temperature Sensor When in Lower C-states (DTSCSTATE):** 1: When in C2, C3, C4, etc. disable the Temperature Sensor. 0: Do not disable temperature sensor. When the temperature sensor has been disabled, power is no longer being applied.

19.5.11 TSTTPA1 - Thermal Sensor Temperature Trip Point A1

B/D/F/Type: 0/0/0/MCHBAR Thermal
Address Offset: 1010-1013h
Default Value: 00000000h
Access: RO; R/W/L; R/WO
Size: 32 bits
BIOS Optimal Default 00h

This register:

- Sets the target values for some of the trip points in thermometer mode.
- Reports the relative thermal sensor temperature.

See also TSTTPB1.

Bit	Access	Default Value	Description
31	R/WO	0b	**Lock Bit For Aux0, Aux1, Aux2 and Aux3 Trip Points (AUXLOCK):** This bit, when written to a 1, locks the Aux x Trip point settings. This lock is reversible. The reversing procedure is: following sequence must be done in order without any other configuration cycles in-between write testtp2 04C1C202 write testtp2x 04C1C202 write testtp2x 04C1C202 write testtp2 04C1C202 It is expected that the Aux x Trip point settings can be changed dynamically when this lock is not set.
30:24	RO	0h	**Reserved**
23:16	RO	00h	**Reserved**
15:8	R/W/L	00h	**Hot Trip Point Setting (HTPS):** Sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	R/W/L	00h	**Catastrophic Trip Point Setting (CTPS):** Sets the target for the Catastrophic trip point. Lockable via TCO bit 7.

19.5.12 TSTTPB1 - Thermal Sensor Temperature Trip Point B1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1014-1017h
Default Value: 00000000h
Access: R/W/L
Size: 32 bits

This register sets the target values for some of the trip points in the Thermometer mode. See also TSTTPA1.

Bit	Access	Default Value	Description
31:24	R/W/L	00h	**Aux3 Trip Point Setting (A3TPS):** Sets the target value for the Aux3 trip point. Lockable by TSTTPA1[31].
23:16	R/W/L	00h	**Aux2 Trip Point Setting (A2TPS):** Sets the target value for the Aux2 trip point. Lockable by TSTTPA1[31].
15:8	R/W/L	00h	**Aux1 Trip Point Setting (A1TPS):** Sets the target value for the Aux1 trip point. Lockable by TSTTPA1[31].
7:0	R/W/L	00h	**Aux0 Trip Point Setting (A0TPS):** Sets the target value for the Aux0 trip point. Lockable by TSTTPA1[31].

19.5.13 TCO1 - Thermal Calibration Offset 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1018h
Default Value: 00h
Access: R/W/L
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Lock Bit for Catastrophic (LBC):** This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of TSTTPA1[15-0], bits 15 and 9 of TSC1. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6:0	R/W/L	00h	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This field is Read/Write and can be modified by Software unless locked by setting bit 7 of this register. Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register. Note for TCO operation: While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation.

Register Field Value	Binary Value
00h to 3Fh	000 0000 to 011 1111
41h to 7Fh	100 0001 to 111 1111

19.5.14 HWTHROTCTRL1 - Hardware Throttle Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 101Ch
Default Value: 00h
Access: R/W/L; RO; R/WO
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Internal Thermal Hardware Throttling Enable Bit (ITHTE):** This bit is a master enable for internal thermal sensor-based hardware throttling 0: Hardware actions via the internal thermal sensor are disabled. 1: Hardware actions via the internal thermal sensor are enabled.
6:5	RO	00b	**Reserved**
4	R/W/L	0b	**Throttling Zone Selection (TZS):** This bit determines what temperature zones will enable auto throttling. This register applies to internal thermal sensor throttling. Lockable by bit0 of this register. See also the throttling registers in PCI configuration space Device 0 which is used to enable or disable throttling 0: Hot, Aux2, and Catastrophic. 1: Hot and Catastrophic.
3	R/W/L	0b	**Halt on Catastrophic (HOC):** When this bit is set, THRMTRIP# is asserted on catastrophic trip to bring the platform down. A system reboot is required to bring the system out of a halt from the thermal sensor. Once the catastrophic trip point is reached, THRMTRIP# will stay asserted even if the catastrophic trip deasserts before the platform is shut down.
2:1	R/W/L	00b	**Reserved**
0	R/WO	0b	**Reserved**

19.5.15 TCOFUSE1 - TCO Fuse 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 101Dh
Default Value: _0xxx__xxxx_h
Access: R/WC; RO
Size: 8 bits

Bit	Access	Default Value	Description
7	R/WC	0b	**INUSE_STS (INUSESTS):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the resource managed by this bit must write a 1 to this bit if it reads a 0, in order to allow other software threads to claim it.
6:0	RO	N/A	**TCO Fuses (TCOFUSE):** This 7 bit field gives the value of the trimming fuses for TCO. The register always reports the settings of all 7 thermal fuses. Note for TCO operation: While this is a seven bit field, the 7th bit is sign extended to 9 bits for TCO operation. Register Field Value: Binary Value 00h to 3Fh: 000 0000 to 011 1111 41h to 7Fh: 100 0001 to 111 1111

19.5.16 TIS1 - Thermal Interrupt Status 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 101E-101Fh
Default Value: 0000h
Access: R/WC
Size: 16 bits
BIOS Optimal Default 0h

Bit	Access	Default Value	Description
15:14	RO	0h	**Reserved**
13	R/WC	0b	**Was Catastrophic Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
12	R/WC	0b	**Was Hot Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
11	R/WC	0b	**Was Aux3 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux3 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
10	R/WC	0b	**Was Aux2 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux2 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
9	R/WC	0b	**Was Aux1 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux1 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
8	R/WC	0b	**Was Aux0 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux0 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
7:6	RO	0h	**Reserved**

Bit	Access	Default Value	Description
5	R/WC	0b	**Catastrophic Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0: No trip for this event. Software must write a 1 to clear this status bit.
4	R/WC	0b	**Hot Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
3	R/WC	0b	**Aux3 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
2	R/WC	0b	**Aux2 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
1	R/WC	0b	**Aux1 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux1 Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
0	R/WC	0b	**Aux0 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux0 Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.

19.5.17 TSC2 - Thermal Sensor Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1041-1042h
Default Value: 0000h
Access: R/WC; R/W/L; R/W
Size: 16 bits
BIOS Optimal Default 00h

This register controls the operation of the internal thermal sensor located in the memory hot spot.

Bit	Access	Default Value	Description
15	R/W/L	0b	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO2 bit 7. 0: Disabled 1: Enabled
14	R/W	0b	**Reserved**
13:10	R/W	0000b	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0000 = digital hysteresis disabled, no offset added to trip temperature 0001 = offset is 1 LSB added to each trip temperature when tripped ... 0100~3.0ºC (Recommended setting) ... 1110 = offset is 14 LSB added to each trip temperature when tripped 1111 = offset is 15 LSB added to each trip temperature when tripped
9	R/W/L	0b	**Reserved**
8	R/WC	0b	**In Use (IU):** Software semaphore bit. After a full H/W (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor.
7:0	RO	0h	**Reserved**

19.5.18 TSS2 - Thermal Sensor Status 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1044-1045h
Default Value: 0000h
Access: RO
Size: 16 bits
BIOS Optimal Default 00h

This read only register provides trip point and other status of the thermal sensor.

Bit	Access	Default Value	Description
15:11	RO	0h	**Reserved**
10	RO	0b	**Thermometer Mode Output Valid (TMOMVAL2):** A 1 indicates the Thermometer mode is able to converge to a temperature and that the TR2 register is reporting a reasonable estimate of the thermal sensor temperature. A 0 indicates the Thermometer mode is off, or that temperature is out of range, or that the TR2 register is being looked at before a temperature conversion has had time to complete.
9	RO	0b	**Reserved**
8:6	RO	0h	**Reserved**
5	RO	0b	**Catastrophic Trip Indicator (CTI):** A 1 indicates that the internal thermal sensor temperature is above the catastrophic setting.
4	RO	0b	**Hot Trip Indicator (HTI):** A 1 indicates that the internal thermal sensor temperature is above the Hot setting.
3	RO	0b	**Aux3 Trip Indicator (A3TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux3 setting.
2	RO	0b	**Aux2TripIndicator (A2TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux2 setting.
1	RO	0b	**Aux1TripIndicator (A1TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux1 setting.
0	RO	0b	**Aux0TripIndicator (A0TI):** A 1 indicates that the internal thermal sensor temperature is above the Aux0 setting.

19.5.19 TR2 - Thermometer Read 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1046h
Default Value: FFh
Access: RO
Size: 8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled.

Bit	Access	Default Value	Description
7:0	RO	FFh	**Thermometer Reading (TR):** Provides the current counter value. The current counter value corresponds to thermal sensor temperature if TSS2[10] = 1 . This register has a straight binary encoding that will range from 0 to FFh.

19.5.20 TOF2 - Thermometer Offset 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1047h
Default Value: 00h
Access: R/W
Size: 8 bits

This register is used to program the thermometer offset

Bit	Access	Default Value	Description
7:0	R/W	00h	**Thermometer Offset (TOF):** This value is used to adjust the current thermometer reading so that the TR value is not relative to a specific trip or calibration point, and is positive going for positive increases in temperature. The initial default value is 00h and software must determine the correct temperature adjustment that corresponds to a zero reading by reading the fuses and referring to the temperature tables, and then programming the computed offset into this register.

19.5.21 RTR2 - Relative Thermometer Read 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1048h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the relative temperature.

Bit	Access	Default Value	Description
7:0	RO	00h	**Relative Thermometer Reading (RTR2):** In Thermometer mode, this register reports the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to TOF2. TR2 and TSTTPA2.HTPS can both vary between 0 and 255. But RTR2 will be clipped between 127 to keep it an 8-bit number. See also TSS2[10].

19.5.22 TIC2 - Thermometer Integrator Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 104Bh
Default Value: 00h
Access: RO; R/W/L
Size: 8 bits
BIOS Optimal Default 0h

This register controls the operation of the integrator filter. For a given thermal solution the inter-component thermals may be on the order of tens of seconds, while intra-component transients may be on the order of milliseconds, the filters are programmable for a range of time intervals.

Bit	Access	Default Value	Description
7	R/W/L	0b	**TIC2 Lock (TIC2LOCK):** This bit secures this register. Once a 1 is written to this bit, all the bits of this register become read-only.
6	RO	0b	**TIC2 Samples (TIC2SAMP):** When set to 1 this bit indicates that enough samples have been collected by the integrator over the interval specified by TIC2[2:0].
5	R/W/L	0b	**Throttle Test Mode Enable (TME):** This bit is used to shorten the filter. 0: Normal Operation 1: Filter time constant is at 2^7
4:3	RO	0h	**Reserved**
2:0	R/W/L	0h	**Sample interval for the integrator (TICINTRVL):** Sample interval for the integrator 000: p = 4 001: p = 6 010: p = 8 011: p = 10 100: p = 12 101: p = 14 110-111: Reserved This time constant must be greater than or equal to the time constant of the moving average filter (TMAC2[2:0]).

19.5.23 TMAC2 - Thermometer Moving Average Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 104Ch
Default Value: 00h
Access: R/W/L; RO
Size: 8 bits
BIOS Optimal Default 0h

This register controls the operation of the moving average filter. For a given thermal solution the inter-component thermals may be on the order of tens of seconds, while intra-component transients may be on the order of milliseconds, the filters are programmable for a range of time intervals.

Bit	Access	Default Value	Description
7	R/W/L	0b	**TMAC2 Lock (TMACLOCK):** This bit secures this register Once a 1 is written to this bit, all of the configuration register bits are read-only.
6	RO	0b	**TMAC2 Samples (TMAC2SAMP):** When set to 1 this bit indicates that enough samples have been collected by the moving average filter over the interval specified by TMCM.
5:5	RO	0h	**Reserved**
4	R/W/L	0b	**Throttle Test Mode Enable (TME):** This bit is used to shorten the filter. 0: Normal Operation 1: Filter time constant is at 2^27
3:3	RO	0h	**Reserved**
2:0	R/W/L	0h	**Sample Interval for the Moving Average (TMCINTRVL):** Sample interval for the moving average 000: alpha = 1 (p=0) 001: alpha = 1/4 (p=2) 010: alpha = 1/16 (p=4) 011: alpha = 1/64 (p=6) 100-111: Reserved

19.5.24 TMA2 - Thermometer Moving Average 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 104Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register provides a moving average of the thermometer samples.

Bit	Access	Default Value	Description
7:0	RO	00h	**Thermometer Reading Moving Average (TMA):** This register provides a moving average of thermometer samples. The average is derived via weighted recursive filter with DC pass-through meaning that when the temperature is stable it will read the current temperature. This represents the sample over the interval set in TIC2, TMAC2. After a hardware reset, or when the sample interval is changed, the filter will be cleared and the current temperature will be displayed.

19.5.25 TSI2 - Thermometer Sample Integrator 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 104Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Thermometer Sample Integrator (TSI):** The integrator accumulates the thermometer samples and integrates over the interval programmed in TIC2, TMAC2. After a hardware reset, or when the sample interval is changed, the filter will be cleared and the current temperature will be displayed.

19.5.26 TSPM2 - Temperature Sensor2 Power Management

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 104Fh
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 00h

This register specifies the power management C-state dependencies for the temperature sensor.

Bit	Access	Default Value	Description
7:1	RO	0h	**Reserved**
0	R/W	0b	**Disable Temperature Sensor When in Lower C-states (DTSCSTATE):** 1: When in C2, C3, C4, etc. Disable the Temperature Sensor. 0: Do not disable temperature sensor. When the temperature sensor has been disabled, power is no longer being applied.

19.5.27 TSTTPA2 - Thermal Sensor Temperature Trip Point A2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1050-1053h
Default Value: 00000000h
Access: RO; R/W/L; R/WO
Size: 32 bits
BIOS Optimal Default 00h
This register:

- Sets the target values for some of the trip points in thermometer mode.
- Reports the relative thermal sensor temperature.

See also TSTTPB2.

Bit	Access	Default Value	Description
31	R/WO	0b	**Lock Bit for Aux0, Aux1, Aux2 and Aux3 Trip Points (AUXLOCK):** This bit, when written to a 1, locks the Aux x Trip point settings. This lock is reversible. The reversing procedure is that the following sequence must be done in order without any other configuration cycles in between. write testtp2 04C1C202 write testtp2x 04C1C202 write testtp2x 04C1C202 write testtp2 04C1C202 **NOTE:** It is expected that the Aux x Trip point settings can be changed dynamically when this lock is not set.
30:24	RO	0h	**Reserved**
23:16	RO	00h	**Reserved**
15:8	R/W/L	00h	**Hot Trip Point Setting (HTPS):** Sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	R/W/L	00h	**Catastrophic Trip Point Setting (CTPS):** Sets the target for the Catastrophic trip point. Lockable via TCO bit 7.

19.5.28 TSTTPB2 - Thermal Sensor Temperature Trip Point B2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1054-1057h
Default Value: 00000000h
Access: R/W/L
Size: 32 bits

This register sets the target values for some of the trip points in the Thermometer mode. See also TSTTPA2.

Bit	Access	Default Value	Description
31:24	R/W/L	00h	**Aux3 Trip Point Setting (A3TPS):** Sets the target value for the Aux3 trip point. Lockable by TSTTPA2[31].
23:16	R/W/L	00h	**Aux2 Trip Point Setting (A2TPS):** Sets the target value for the Aux2 trip point. Lockable by TSTTPA2[31].
15:8	R/W/L	00h	**Aux1 Trip Point Setting (A1TPS):** Sets the target value for the Aux1 trip point. Lockable by TSTTPA2[31].
7:0	R/W/L	00h	**Aux0 Trip Point Setting (A0TPS):** Sets the target value for the Aux0 trip point. Lockable by TSTTPA2[31].

19.5.29 TCO2 - Thermal Calibration Offset 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1058h
Default Value: 00h
Access: R/W/L
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Lock Bit for Catastrophic (LBC):** This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of TSTTPA2[15-0], bits 15 and 9 of TSC2. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6:0	R/W/L	00h	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This field is Read/Write and can be modified by Software unless locked by setting bit 7 of this register. The fuses cannot be programmed via this register. Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register. **Note for TCO operation:** While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation.

Register Field Value	Binary Value
00h to 3Fh	000 0000 to 011 1111
41h to 7Fh	100 001 to 111 1111

19.5.30 HWTHROTCTRL2 - Hardware Throttle Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 105Ch
Default Value: 00h
Access: RO; R/W/L; R/WO
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	**Internal Thermal Hardware Throttling Enable bit (ITHTE):** This bit is a master enable for internal thermal sensor-based hardware throttling. 0: Hardware actions via the internal thermal sensor are disabled. 1: Hardware actions via the internal thermal sensor are enabled.
6:5	RO	00b	**Reserved**
4	R/W/L	0b	**Throttling Zone Selection (TZS):** This bit determines what temperature zones will enable auto throttling. This register applies to internal thermal sensor throttling. Lockable by bit0 of this register. See also the throttling registers in PCI config space Device 0 which is used to enable or disable throttling. 0: Hot, Aux2, and Catastrophic. 1: Hot and Catastrophic.
3	R/W/L	0b	**Halt on Catastrophic (HOC):** When this bit is set, THRMTRIP# is asserted on catastrophic trip to bring the platform down. A system reboot is required to bring the system out of a halt from the thermal sensor. Once the catastrophic trip point is reached, THRMTRIP# will stay asserted even if the catastrophic trip deasserts before the platform is shut down.
2:1	R/W/L	00b	**Reserved**
0	R/WO	0b	**Reserved**

19.5.31 TCOFUSE2 - TCO Fuse 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 105Dh
Default Value: _0xxx__xxxx_h
Access: RO; R/WC
Size: 8 bits

Bit	Access	Default Value	Description
7	R/WC	0b	**INUSE_STS (INUSESTS):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the resource managed by this bit must write a one to this bit if it reads a 0, in order to allow other software threads to claim it.
6:0	RO	N/A	**TCO Fuses (TCOFUSE):** This 7-bit field gives the value of the trimming fuses for TCO. The register always reports the settings of all 7 thermal fuses. Note for TCO operation: While this is a seven bit field, the 7th bit is sign extended to 9 bits for TCO operation.

Register Field Value	Binary Value
00h to 3Fh	000 0000 to 011 1111
41h to 7Fh	100 001 to 111 1111

19.5.32 TIS2 - Thermal Interrupt Status 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 105E-105Fh
Default Value: 0000h
Access: R/WC
Size: 16 bits
BIOS Optimal Default 0h

Bit	Access	Default Value	Description
15:14	RO	0h	**Reserved**
13	R/WC	0b	**Was Catastrophic Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
12	R/WC	0b	**Was Hot Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
11	R/WC	0b	**Was Aux3 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux3 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
10	R/WC	0b	**WasAux2ThermalSensorInterruptEvent:** 0: No trip for this event. 1: Indicates that an Aux2 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
9	R/WC	0b	**Was Aux1 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux1 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
8	R/WC	0b	**Was Aux0 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux0 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point. Software must write a 1 to clear this status bit.
7:6	RO	0h	**Reserved**

Bit	Access	Default Value	Description
5	R/WC	0b	**Catastrophic Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
4	R/WC	0b	**Hot Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
3	R/WC	0b	**Aux3 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
2	R/WC	0b	**Aux2 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
1	R/WC	0b	**Aux1 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux1 Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.
0	R/WC	0b	**Aux0 Thermal Sensor Interrupt Event:** 0: No trip for this event. 1: Indicates that an Aux0 Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. Software must write a 1 to clear this status bit.

19.5.33 TERATE - Thermometer Mode Enable and Rate

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1070h
Default Value:	00h
Access:	R/W;
Size:	8 bits
BIOS Optimal Default	0h

This common register helps select between the analog and the thermometer mode and also helps select the DAC settling timer.

This register bit field shall contain the default value unless otherwise indicated in the BIOS specification.

19.5.34 TSRCTRL - Thermal Sensor Rate Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1080h
Default Value:	06h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	0h

This register controls the conversion duration and slow clock duration of the thermal sensor.

Bit	Access	Default Value	Description
7:4	RO	0h	**Reserved**
3	R/W	0b	**conversion duration (TSCD):** 0: 128 fast clocks 1:32 fast clocks (normal mode operation)
2:0	R/W	110b	Slow clock control (SCC): Sample interval for the slow clock. 000: 25 6 µsec (will not work with all settings for fast clock) 001: 512 µsec (will not work with all settings for fast clock) 010: 1024 µsec 011: 2048 µsec 100: 4096 µsec 101: 8192 µsec 110: 16384 µsec (normal thermometer mode operation, pre-silicon) 111: 32768 µsec Legal settings must obey following restriction: 100 µsec for thermal sensor settling +32 * fast clock + 1 µsec clock granularity < slow clock control setting if Conversion duration = 0 100 µsec for thermal sensor settling +128 * fast clock + 1 µsec clock granularity < slow clock control setting if Conversion duration = 1

19.5.35 IUB - In Use Bits

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10E0-10E3h
Default Value: 00000000h
Access: RO; R/WC
Size: 32 bits

Semaphore bits available for SW.

Bit	Access	Default Value	Description
31:25	RO	00h	**Reserved**
24	R/WC	0b	**In Use Bit3 (IU3):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it.
23:17	RO	00h	**Reserved**
16	R/WC	0b	**In Use Bit2 (IU2):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it.
15:9	RO	00h	**Reserved**
8	R/WC	0b	**In Use Bit1 (IU1):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it.
7:1	RO	00h	**Reserved**
0	R/WC	0b	**In Use Bit0 (IU0):** Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it.

19.5.36 TERRCMD - Thermal Error Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10E4h
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 0h

This register select which errors are generate a SERR DMI interface special cycle, as enabled by ERRCMD [SERR Thermal Sensor event].The SERR and SCI must not be enabled at the same time for the thermal sensor event.

Bit	Access	Default Value	Description
7:6	RO	0h	**Reserved**
5	R/W	0b	**SERR on Catastrophic Thermal Sensor Event:** 0: Disable. 1: Enable.
4	R/W	0b	**SERR on Hot Thermal Sensor Event:** 0: Disable. 1: Enable.
3	R/W	0b	**SERR on Aux3 Thermal Sensor Event:** 0: Disable. 1: Enable.
2	R/W	0b	**SERR on Aux2 Thermal Sensor Event:** 0: Disable. 1: Enable.
1	R/W	0b	**SERR on Aux1 Thermal Sensor Event:** 0: Disable. 1: Enable.
0	R/W	0b	**SERR on Aux0 Thermal Sensor Event:** 0: Disable. 1: Enable.

19.5.37 TSMICMD - Thermal SMI Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10E5h
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 0h

This register selects specific errors to generate a SMI DMI cycle, as enabled by the SMI Error Command Register[SMI on Thermal Sensor Trip] .

Bit	Access	Default Value	Description
7:6	RO	0h	**Reserved**
5	R/W	0b	**SMI on Catastrophic Thermal Sensor Trip:** 0: Disable. 1: Enable.
4	R/W	0b	**SMI on Hot Thermal Sensor Trip:** 0: Disable. 1: Enable.
3	R/W	0b	**SMI on Aux3 Thermal Sensor Trip:** 0: Disable. 1: Enable.
2	R/W	0b	**SMI on Aux2 Thermal Sensor Trip:** 0: Disable. 1: Enable.
1	R/W	0b	**SMI on Aux1 Thermal Sensor Trip:** 0: Disable. 1: Enable.
0	R/W	0b	**SMI on Aux0 Thermal Sensor Trip:** 0: Disable. 1: Enable.

19.5.38 TSCICMD - Thermal SCI Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10E6h
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 0h

This register selects specific errors to generate a SCI DMI cycle, as enabled by the SCI Error Command Register[SCI on Thermal Sensor Trip].The SCI and SERR must not be enabled at the same time for the thermal sensor event.

Bit	Access	Default Value	Description
7:6	RO	0h	**Reserved**
5	R/W	0b	**SCI on Catastrophic Thermal Sensor Trip:** 0: Disable. 1: Enable.
4	R/W	0b	**SCI on Hot Thermal Sensor Trip:** 0: Disable. 1: Enable.
3	R/W	0b	**SCI on Aux3 Thermal Sensor Trip:** 0: Disable. 1: Enable.
2	R/W	0b	**SCI on Aux2 Thermal Sensor Trip:** 0: Disable. 1: Enable.
1	R/W	0b	**SCI on Aux1 Thermal Sensor Trip:** 0: Disable. 1: Enable.
0	R/W	0b	**SCI on Aux0 Thermal Sensor Trip:** 0: Disable. 1: Enable.

19.5.39 TINTRCMD - Thermal INTR Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10E7h
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 0h

This register selects specific errors to generate an INT DMI cycle.

Bit	Access	Default Value	Description
7:6	RO	0h	**Reserved**
5	R/W	0b	**INTR on Catastrophic Thermal Sensor Trip:** 1 = A INTR DMI cycle is generated by (G)MCH.
4	R/W	0b	**INTR on Hot Thermal Sensor Trip:** 1 = A INTR DMI cycle is generated by (G)MCH.
3	R/W	0b	**INTR on Aux3 Thermal Sensor Trip:** 1 = A INTR DMI cycle is generated by (G)MCH.
2	R/W	0b	**INTR on Aux2 Thermal Sensor Trip:** 1 = A INTR DMI cycle is generated by (G)MCH.
1	R/W	0b	**INTR on Aux1 Thermal Sensor Trip:** 1 = A INTR DMI cycle is generated by (G)MCH.
0	R/W	0b	**INTR on Aux0 Thermal Sensor Trip:** 1 = A INTR DMI cycle is generated by (G)MCH.

19.5.40 EXTTSCS - External Thermal Sensor Control and Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 10EFh
Default Value: 00h
Access: R/W; R/WO; R/W/L; RO
Size: 8 bits
BIOS Optimal Default 0h

Bit	Access	Default Value	Description
7	R/WO	0b	**External Sensor Enable:** Setting this bit to 1 locks the lockable bits in this register. This bit may only be set to a zero by a hardware reset. Once locked, writing a 0 to bit has no effect. If both internal sensor throttling and external write sensor throttling are enabled, either can initiate throttling. 0: External Sensor input is disabled. 1: External Sensor input is enabled.
6	R/W/L	0b	**Throttling Type Select (TTS):** Lockable by EXTTSCS [7]. If External Thermal Sensor Enable = 1, then 0: DRAM throttling based on the settings in the Device 0 MCHBAR DRAM Throttling Control register (C0DTC). 1: (G)MCH throttling, based on the settings in the Device 0 MCHBAR (C0GTC).
5	R/W/L	0b	**EXTTS1 Action Select (AS1):** Lockable by EXTTSCS [7] = 1. 0: The external sensor trip functions same as a Thermometer mode hot trip. 1: The external sensor trip functions as a Thermometer mode aux0 trip. See clarification note below. **NOTE: This bit is N/A when fast C4e exit is enabled.**
4	R/W/L	0b	**EXTTS0 Action Select (AS0):** Lockable by EXTTSCS [7]. 0: The external sensor trip functions same as a Thermometer mode catastrophic trip. 1: The external sensor trip functions same as a Thermometer mode hot trip. **NOTE: See clarification note below.**
3	RO	0b	**EXTTS0 Trip Indicator (S0TI):** A 1 indicates that an externally monitored temperature is exceeding the programmed setting of an external thermal sensor.
2	RO	0b	**EXTTS1 Trip Indicator (S1TI):** A 1 indicates that an externally monitored temperature is exceeding the programmed setting of an external thermal sensor. **This bit is N/A when fast C4e exit is enabled.**

Bit	Access	Default Value	Description
1:1	RO	0h	**Reserved**
0	R/W	0b	**External Thermal Sensor Signals Routing Control:** 0: Route all external sensor signals to affect internal thermal sensor 1 registers, as appropriate. 1: Route all external sensor signals to affect internal thermal sensor 2 registers, as appropriate.

19.6 MCHBAR Render Thermal Throttling

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		1100	1101	0000h	R/W
VID and Frequency Relationship Table 1	VIDFREQ1	1110	1113	00000000h	R/W
Reserved		1114	111F		
Internal to External VID Mapping Table 1	INTTOEXT1	1120	1123	00000000h	R/W; RO
Internal to External VID Mapping Table 2	INTTOEXT2	1124	1127	00000000h	R/W; RO
Internal to External VID Mapping Table 3	INTTOEXT3	1128	112B	00000000h	R/W; RO
Reserved		112C	11AF		
Thermal State Control	THERMSTCTL	11B0	11B3	00000000h	R/W
Render Standby State Control	RSTDBYCTL	11B8	11BB	00000000h	R/W
Reserved		11BC	11BF		
VID Control	VIDCTL	11C0	11C3	00000000h	R/W
VID Control 1	VIDCTL1	11C4	11C7	00000000h	R/W
Reserved		11C8	11E9		

19.6.1 VIDFREQ1 - VID and Frequency Relationship Table 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1110-1113h
Default Value: 00000000h
Access: R/W;
Size: 32 bits
BIOS Optimal Default 0000h

Bit	Access	Default Value	Description
31:28	RO	0h	**Reserved**
27:24	R/W	0000b	**VID Point -- P0 (VIDP0):**
23:20	RO	0h	**Reserved**
19:16	R/W	0000b	**P0 Frequency (P0FREQ):**
15:12	RO	0h	**Reserved**
11:8	R/W	0000b	**VID Point -- P1 (VIDP1):**
7:4	RO	0h	**Reserved**
3:0	R/W	0000b	**Reserved**

19.6.2 INTTOEXT1 - Internal to External VID Mapping Table 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1120-1123h
Default Value: 00000000h
Access: R/W; RO;
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	**Reserved**
27:24	R/W	0000b	**External Mapping for Internal Mapping 15 (MAP15):** External mapping for internal mapping 15
23:20	RO	0h	**Reserved**
19:16	R/W	0000b	**External Mapping for Internal Mapping 14 (MAP14)**
15:12	RO	0h	**Reserved**
11:8	R/W	0000b	**External Mapping for Internal Mapping 13 (MAP13)**
7:4	RO	0h	**Reserved**
3:0	R/W	0000b	**External Mapping for Internal Mapping 12 (MAP12)**

19.6.3 INTTOEXT2 - Internal to External VID Mapping Table 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1124-1127h
Default Value: 00000000h
Access: R/W; RO;
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	**Reserved**
27:24	R/W	0000h	**External Mapping for Internal Mapping 11 (MAP11)**
23:20	RO	0h	**Reserved**
19:16	R/W	0000b	**External Mapping for Internal Mapping 10 (MAP10)**
15:12	RO	0h	**Reserved**
11:8	R/W	0000b	**External Mapping for Internal Mapping 9 (MAP9)**
7:4	RO	0h	**Reserved**
3:0	R/W	0000b	**External Mapping for Internal Mapping 8 (MAP8)**

19.6.4 INTTOEXT3 - Internal to External VID Mapping Table 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1128-112Bh
Default Value: 00000000h
Access: R/W; RO;
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	**Reserved**
27:24	R/W	0h	**External Mapping for Internal Mapping 7 (MAP7)**
23:20	RO	0h	**Reserved**
19:16	R/W	0000b	**External Mapping for Internal Mapping 6 (MAP6)**
15:12	RO	0h	**Reserved**
11:8	R/W	0000b	**External Mapping for Internal Mapping 5 (MAP5)**
7:4	RO	0h	**Reserved:**
3:0	R/W	0000b	**External Mapping for Internal Mapping 4 (MAP4)**

19.6.5 THERMSTCTL - Thermal State Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 11B0-11B3h
Default Value: 00000000h
Access: R/W;
Size: 32 bits
BIOS Optimal Default 00000h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification

19.6.6 RSTDBYCTL - Render Standby State Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 11B8-11BBh
Default Value: 00000000h
Access: R/W;
Size: 32 bits
BIOS Optimal Default 000h

Bit	Access	Default Value	Description
31	R/W	0b	**Reserved**
30	R/W	0b	**RS2 Enable (RS2EN):** 0: RS2 not enabled 1: RS2 enabled
29:0	R/W	0000000h	**Reserved**

19.6.7 VIDCTL - VID Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 11C0-11C3h
Default Value: 00000000h
Access: R/W;
Size: 32 bits

Bit	Access	Default Value	Description
31:24	R/W	00h	**VID Up Time (VIDUPTIME):** 0 = 255 µs 1 = 1 µs 255 = 255 µs
23:16	R/W	00h	**VID Down Time (VIDDNTIME):** 0 = 255 µs 1 = 1 µs 255 = 255 µs
15:0	R/W	0000h	**Reserved**

19.6.8 VIDCTL1 - VID Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 11C4-11C7h
Default Value: 00000000h
Access: R/W;
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

Bit	Access	Default Value	Description
31:0	R/W	00000000h	**Reserved**

19.7 Device 0 MCHBAR DRAM Controls

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel 0 DRAM Rank Boundary 0/1	C0DRB01	1200	1203	00000000h	RO; R/W
Reserved		1204	1207		
Channel 0 DRAM Rank 0,1 Attribute	C0DRA	1208	120B	00000000h	RO; R/W
Channel 0 DRAM Clock Disable	C0DCLKDIS	120C	120F	00000000h	RO; R/W
Channel 0 DRAM Timing Register 0	C0DRT0	1210	1213	34B10461h	R/W; RO
Channel 0 DRAM Timing Register 1	C0DRT1	1214	1217	11E08463h	RO; R/W
Channel 0 DRAM Timing Register 2	C0DRT2	1218	121B	2200105Fh	RO; R/W
Channel 0 DRAM Timing Register 3	C0DRT3	121C	121F	01056101h	RO; R/W
Channel 0 DRAM Timing Register 4	C0DRT4	1220	1223	29503C32h	RO; R/W
Channel 0 DRAM timing Register 5	C0DRT5	1224	1227	62C32020h	RO; R/W
Reserved		1228	122F		
Channel 0 DRAM Controller Mode 0	C0DRC0	1230	1233	40000002h	RO; R/W
Channel 0 DRAM Controller Mode 1	C0DRC1	1234	1237	00000000h	RO; R/W
Channel 0 DRAM Controller Mode 2	C0DRC2	1238	123B	00000000h	RO; R/W
Reserved		123C	124F		
Channel 0 Adaptive Idle Timer Control	C0AIT	1250	1257	0000000000000000h	RO; R/W
Reserved		1258	126B		
Channel 0 (G)MCH Throttling Event Weight 1	C0DTEW1	126C	126F	00000000h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel 0 (G)MCH Throttling Event Weight	C0GTEW	1270	1273	00000000h	R/W/L
Channel 0 (G)MCH Throttling Control	C0GTC	1274	1277	00000000h	R/W/L; RO
Channel 0 DRAM Rank Throttling Passive Event	C0DTPEW	1278	127F	0000000000000000h	RO; R/W/L
Channel 0 DRAM Rank Throttling Active Event	C0DTAEW	1280	1287	0000000000000000h	RO; R/W/L
Channel 0 DRAM Throttling Control	C0DTC	1288	128B	00000000h	R/W/L; RO
Reserved		128C	12FF		
Channel 1 DRAM Rank Boundary 0/1	C1DRB01	1300	1303	00000000h	RO; R/W
Reserved		1304	1307	00000000h	RO; R/W
Channel 1 DRAM Rank 0,1 Attribute	C1DRA	1308	130B	00000000h	RO; R/W
Channel 1 DRAM Clock Disable	C1DCLKDIS	130C	130F	00000000h	RO; R/W
Channel 1 DRAM Timing Register 0	C1DRT0	1310	1313	34B10461h	RO; R/W
Channel 1 DRAM Timing Register 1	C1DRT1	1314	1317	11E08463h	RO; R/W
Channel 1 DRAM Timing Register 2	C1DRT2	1318	131B	2200105Fh	RO; R/W
Channel 1 DRAM Timing Register 3	C1DRT3	131C	131F	01056101h	RO; R/W
Channel 1 DRAM Timing Register 4	C1DRT4	1320	1323	29503C32h	RO; R/W
Channel 1 DRAM timing register 5	C1DRT5	1324	1327	62C32020h	R/W; RO
Reserved		1328	132B	29503C32h	RO; R/W
Channel 1 DRAM Controller Mode 0	C1DRC0	1330	1333	40000002h	RO; R/W
Channel 1 DRAM Controller Mode 1	C1DRC1	1334	1337	00000000h	RO; R/W
Channel 1 DRAM Controller Mode 2	C1DRC2	1338	133B	00000000h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		133C	134F		
Channel 1 Adaptive Idle Timer Control	C1AIT	1350	1357	0000000000000000h	RO; R/W
Reserved		1358	136B		
Channel 1 (G)MCH Throttling Event Weight 1	C1DTEW1	136C	136F	00000000h	RO; R/W
Channel 1 (G)MCH Throttling Event Weight	C1GTEW	1370	1373	00000000h	R/W/L
Channel 1 (G)MCH Throttling Control	C1GTC	1374	1377	00000000h	R/W/L; RO
Channel 1 DRAM Rank Throttling Passive Event	C1DTPEW	1378	137F	0000000000000000h	RO; R/W/L
Channel 1 DRAM Rank Throttling Active Event	C1DTAEW	1380	1387	0000000000000000h	RO; R/W/L
Channel 1 DRAM Throttling Control	C1DTC	1388	138B	00000000h	R/W/L; RO
Reserved		138C	13AF		

19.7.1 C0DRB01 - Channel 0 DRAM Rank Boundary 0/1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1200-1203h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

The DRAM Rank Boundary Register defines the upper boundary address of each DRAM rank with a granularity of 32. These registers are used to determine which chip select will be active for a given address.

In all modes, if a DIMM is single-sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Bit	Access	Default Value	Description
31:25	RO	00h	**Reserved**

Bit	Access	Default Value	Description
24:16	R/W	000h	**Channel 0 DRAM Rank 1 Boundary Address (DRB1):** This 9-bit value defines the upper and lower addresses for each DRAM rank. Bits 7:2 are compared against Address 32:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0's.
15:9	RO	00h	**Reserved**
8:0	R/W	000h	**Channel 0 DRAM Rank 0 Boundary Address (DRB0):** This 9-bit value defines the upper and lower addresses for each DRAM rank. Bits 7:2 are compared against Address 32:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0's.

19.7.2 C0DRB23 - Channel 0 DRAM Rank Boundary 2/3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1204-1207h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

.

Bit	Access	Default Value	Description
31:0	RO	00000000h	**Reserved**

19.7.3 C0DRA - Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1208-120Bh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

The **DRAM Rank Attribute Registers** define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks.

Bit	Access	Default Value	Description
31:22	RO	00h	**Reserved**
21	RO	0b	**Reserved**
20:19	R/W	00b	**Rank 1 Bank Architecture:** 00: 4 Bank 01: 8 Bank 10 - 11: Reserved
18	RO	0b	**Reserved**
17:16	R/W	00b	**Rank 0 Bank Architecture:** 00: 4 Bank 01: 8 Bank 10 - 11: Reserved
15:7	RO		**Reserved**
6:4	R/W	000b	**Channel 0 DRAM Odd Rank 1 Attribute (DRA1):** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4 KB 011: 8 KB Others: Reserved
3	RO	0b	**Reserved**
2:0	R/W	000b	**Channel 0 DRAM Even Rank 0 Attribute (DRA0):** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated 001: Reserved 010: 4 KB 011: 8 KB Others: Reserved

19.7.4 C0DCLKDIS - Channel 0 DRAM Clock Disable

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 120C-120Fh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register can be used to disable the System Memory Clock signals to each DIMM slot, which can significantly reduce EMI and Power concerns for clocks that go to unpopulated DIMMs. Clocks should be enabled based on whether a slot is populated, and what kind of DIMM is present:

Since there are multiple clock signals assigned to each rank of a DIMM, it is important to clarify exactly which rank width field affects which clock signal.

Channel	Rank Clocks	Affected
0	0 or 1	SM_CK_1:0
1	2 or 3	SM_CK_4:3

Bit	Access	Default Value	Description
31:4	RO	0000000h	**Reserved**
3	R/W	0b	**DIMM Clock Gate Enable Pair 3:** 0: Tri-state the corresponding clock pair. 1: Enable the corresponding clock pair.
2	R/W	0b	**DIMM Clock Gate Enable Pair 2:** 0: Tri-state the corresponding clock pair. 1: Enable the corresponding clock pair.
1	R/W	0b	**DIMM Clock Gate Enable Pair 1:** 0: Tri-state the corresponding clock pair. 1: Enable the corresponding clock pair.
0	R/W	0b	**DIMM Clock Gate Enable Pair 0:** 0: Tri-state the corresponding clock pair. 1: Enable the corresponding clock pair.

19.7.5 C0DRT0 - Channel 0 DRAM Timing Register 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1210-1213h
Default Value: 34B10461h
Access: R/W; RO
Size: 32 bits

This 32-bit register defines the timing parameters for all devices in this channel. The BIOS programs this register with the "least common denominator" values for each channel after reading configuration registers of each device in each channel.

Bit	Access	Default Value	Description
31	RO	0b	**Reserved**
30:26	R/W	0dh	**Back to Back Write to Precharge Command Spacing (same bank) (B2BWR2PCSB):** This field determines the number of clocks between write command and a subsequent precharge command to the same bank. The minimum number of clocks is calculated based on this formula DDR2: DDR2: WL+ BL/2 + t WR 0h to 9h: Reserved Ah to 13h: Allowed **NOTE:** Write Recovery time (tWR). Write recovery time is a standard DDRI/II timing parameter that determines minimum time between a write command and a subsequent precharge command to the same bank. This parameter is programmable on DDR-II DIMMs and the value used above must match the largest delay programmed in any DIMM in the system. Minimum recommended values are documented below: tWR (on CK) 4 Clocks: DDR2 533 5 Clocks: DDR2 667
25:24	RO	00b	**Reserved**

Bit	Access	Default Value	Description
23:20	R/W	Bh	**Back-to-Back Write to Read Command Spacing (Same Rank):** This field determines the number of clocks between write command and a subsequent read command to the same rank. The minimum number of clocks is calculated based on this formula: DDR2: WL + BL/2 + t WTR 0h - 7h: Reserved 8h - Fh: Allowed **NOTE:** Write to Read Command delay (tWTR). The tWTR is a standard DDR timing parameter and is used to time a RD command after a WR command to the same row. Following are the values used for tWTR 2 Clocks - CL = DDR2 533 3 Clocks - DDR2 667
19:18	RO	00b	**Reserved**
17:15	R/W	010b	**Back to Back Write-Read Command Spacing (Different Rank):** This field determines the number of turnaround clocks on the data bus that needs to be inserted between write command and a subsequent read command. The minimum spacing of commands is calculated based on the formula: Spacing = BL/2 + TA (wr-rd) + WL - CL BL is the burst length which is 8 TA is the required write to read DQ turnaround on the bus. Can be set to 1,2, or 3 CK using this register CL is CAS Latency WL is Write Latency **Encoding** — **BL8 CMD Spacing** 110 — 9 101 — 8 100 — 7 011 — 6 010 — 5 001 — 4 000 — 3
14	RO	0b	**Reserved**

Bit	Access	Default Value	Description
13:10	R/W	1h	**Back-to-Back Read-Write Command Spacing:** This field determines the number of turnaround clocks between the read command and a subsequent write command. Same and different rank The minimum spacing of commands is calculated based on the formula: Spacing = CL + BL/2 + TA (wr-rd) - WL BL is the burst length which is 8 TA is the required read to write DQ turnaround on the bus. Can be set to 1,2,3, 4 CK for DDR2 CL is CAS Latency WL is Write Latency **Encoding — BL8 CMD Spacing** 0111 — 12 0110 — 11 0101 — 10 0100 — 9 0011 — 8 0010 — 7 0001 — 6 0000 — 5 The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest DIMM is large.
9:8	RO	00b	**Reserved**
7:5	R/W	011b	**Back-to-back Write Command Spacing (Different Rank):** This field controls the turnaround time on the DQ bus for WR-WR sequence to different ranks in one channel. The minimum spacing of commands is calculated based on the formula **DDR2 = BL/2 + TA** **Encoding — Turnaround — BL8 CMD Spacing** 100 — 4 turnaround clocks on DQ — 8 011 — 3 turnaround clocks on DQ — 7 010 — 2 turnaround clocks on DQ — 6 001 — 1 turnaround clocks on DQ — 5 000 — 0 turnaround clocks on DQ — 4 The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest DIMM is large.
4:3	RO	00b	**Reserved**

Bit	Access	Default Value	Description
2:0	R/W	001b	**Back-to-Back Read Command Spacing (Different Rank):** This field controls the turnaround time on the DQ bus for Rd-RD sequence to different ranks in one channel. The minimum spacing of commands is calculated based on the formula **DDR2 = BL/2 + TA** **Encoding** **Turnaround** **BL8 CMD Spacing** 101 6 turnaround clocks on DQ 10 100 5 turnaround clocks on DQ 9 011 4 turnaround clocks on DQ 8 010 3 turnaround clocks on DQ 7 001 2 turnaround clocks on DQ 6 000 1 turnaround clocks on DQ 5 The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest DIMM is large.

19.7.6 C0DRT1 - Channel 0 DRAM Timing Register 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1214-1217h
Default Value: 11E08463h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:30	RO	00b	**Reserved**
29:28	R/W	01b	**Read to Precharge (tRTP):** These bits control the number of clocks that are inserted between a read command to a row precharge command to the same rank. Encoding tRTP 00: BL/2 (DDR2 533) 01: BL/2+1 (DDR2 667) 10: Reserved 11: Reserved
27:26	RO	00b	**Reserved**
25:21	R/W	0Fh	**Activate to Precharge Delay (tRAS):** This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings. Recommended values: 0Ch: DDR2 533 0Fh: DDR2 667

Bit	Access	Default Value	Description
20:19	RO	00b	**Reserved**
18	R/W	0b	**Precharge to Precharge Delay:** Control Pre to Pre delay between the different banks of the same rank. 0: 1 Clock 1: 2 Clock
17:16	RO	00b	**Reserved**
15	R/W	1b	**Pre-All to Activate Delay (tRPALL):** This is applicable only to 8-bank architectures. Must be set to 1 if any Rank is populated with 8-bank device technology. 0: tRPALL = tRP 1: tRPALL = tRP + 1
14:13	RO	00b	**Reserved**
12:10	R/W	001b	**Activate to Activate delay (tRRD):** Control Act to Act delay between the different banks of the same rank. Trr is specified in "ns". 10 ns for 2-KB page size and 7.5 ns for 1-KB page size. Bios should round up to the nearest number of clocks and use the maximum applicable value. 000 = 2 Clock 001 = 3 Clock 010 = 4 Clocks 011 = 5 Clocks 100 = 6 Clocks
9:8	RO	00b	**Reserved**
7:5	R/W	011b	**DRAM RASB to CASB Delay (tRCD):** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. Encoding tRCD 000 2 DRAM Clocks 001 3 DRAM Clocks 010 4 DRAM Clocks 011 5 DRAM Clocks 100 6 DRAM Clocks 101 7 DRAM Clocks 110 8 DRAM Clocks. 111 Reserved
4:3	RO	00b	**Reserved**

Bit	Access	Default Value	Description
2:0	R/W	011b	**DRAM RASB Precharge (tRP):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. Encoding tRP 000: 2 DRAM Clocks. 001: 3 DRAM Clocks 010: 4 DRAM Clocks 011: 5 DRAM Clocks 100: 6 DRAM clocks 101: 7 DRAM clocks. 110: 8 DRAM clocks 111: Reserved

19.7.7 C0DRT2 - Channel 0 DRAM Timing Register 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1218-121Bh
Default Value: 2200105Fh
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:29	R/W	001b	**Reserved**
28:27	RO	00b	**Reserved**
26:24	R/W	010b	**CKE Deassert Duration:** 000 = Reserved 001 = Reserved 010 = 3 clocks 011 = 4 clocks 100 = 5 clocks 101 - 111 = Reserved Must be set to 010 for DDR2
23:22	RO	00b	**Reserved**
21:17	R/W	00h	**Rolling Activate Window (tFAW):** Number of clks in a rolling activate window. A rolling activate window allows only 4 activates to a given rank in that window of time. 0-6 - Reserved 7-1B - Allowed 1C-1F – Reserved
16:15	RO	0h	**Reserved**
14:12	R/W	1h	**Fast Exit Active / Precharge Power Down to Any Command (tXP):** Power down exit time is tracked from the clock in which we sample CKE active, after exit from dynamic power down, until the clock which we drive a command (ACT/PRE/RD/WR). Following are the options provided. 001 = Power Down Exit time is set to 2 clocks. (DDR2 533, DDR2 667). Others = Reserved
11:10	RO	0h	**Reserved**

Bit	Access	Default Value	Description
9:6	R/W	1h	**Slow Exit Precharge Power Down Exit to Read / Write CS# (tXPDLL):** Power down exit time is tracked from the clock in which we sample CKE active, after exit from dynamic power down, until the clock which we drive a command (ACT/PRE/RD/WR). Following are the options provided. 0001 = Power Down Exit time is set to 2 clocks. (DDR2 533, DDR2 667) Others = Reserved
5	RO	0h	**Reserved**
4:0	R/W	1Fh	**Reserved**

19.7.8 C0DRT3 - Channel 0 DRAM Timing Register 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 121C-121Fh
Default Value: 01056101h
Access: RO; R/W
Size: 32 bits

Note: If the existing fields does not support the required delay time, then these values have to be counted in half frequency clocks instead of full freq clocks.

Bit	Access	Default Value	Description
31:30	RO	00b	**Reserved**
29:28	R/W	00b	**Reserved**
27:26	R/W	00b	**Self Refresh Exit to Non-Read Write Command (tXS):** 00 = tRFC + 10 clocks 01 = tRFC + 20 clocks 10 = value in[29:28] - (trfc + 20) clocks 11 = reserved
25:23	R/W	010b	**CASB Latency (tCL):** This value is programmable on DDR2 DIMMs. The value programmed here must match the CAS Latency of every DDR2 DIMM in the system. **Encoding — DDR2 CL** 000 — 3 001 — 4 010 — 5 011 — 6 100 — 7 101 — Reserved
22:21	RO	00b	**Reserved**

<table>
<tr><th>Bit</th><th>Access</th><th>Default Value</th><th>Description</th></tr>
<tr><td>20:13</td><td>R/W</td><td>2Bh</td><td>Refresh Cycle Time (tRFC):
Refresh cycle time is measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank, required to perform a read or write.
For DDR2 on Mobile Intel® 965 Express chipset , tRFC needs to follow the values recommended in the table below:-

<table>
<tr><th>Para-meter</th><th>Sym</th><th>256 Mb</th><th>512 Mb</th><th>1 Gb</th><th>2 Gb</th></tr>
<tr><td>Refresh to Active/ Refresh Command Time</td><td>tRFC</td><td>75 ns</td><td>105 ns</td><td>127.5 ns</td><td>195 ns</td></tr>
<tr><td>DDR2 533</td><td></td><td>20 (mem clks)</td><td>28 (mem clks)</td><td>34 (mem clks)</td><td>52 (mem clks)</td></tr>
<tr><td>DDR2 677</td><td></td><td>25 (mem clks)</td><td>35 (mem clks)</td><td>43 (mem clks)</td><td>65 (mem clks)</td></tr>
</table>
</td></tr>
<tr><td>12:11</td><td>RO</td><td>00b</td><td>Reserved</td></tr>
<tr><td>10:7</td><td>R/W</td><td>2h</td><td>Reserved</td></tr>
<tr><td>6:3</td><td>RO</td><td>0h</td><td>Reserved</td></tr>
<tr><td>2:0</td><td>R/W</td><td>001b</td><td>Write Latency (tWL):
For DDR2 this register is programmed to CL -1
000 - 2 - DDR2 - CL3
001 - 3 - DDR2 - CL4
010 - 4 - DDR2 - CL5
011 - 5 - DDR2 - CL6
100 - 6 - DDR2 - CL7
100 - 7 - DDR2 - CL8
Others are Reserved</td></tr>
</table>

19.7.9 C0DRT4 - Channel 0 DRAM Timing Register 4

B/D/F/Type: 0/0/0/MCHBAR Chipset
Address Offset: 1220-1223h
Default Value: 29503C32h
Access: RO; R/W
Size: 32 bits

If the existing fields does not support the required delay time, then these values have to be counted in half freq clocks instead of full freq clocks.

Bit	Access	Default Value	Description
31:27	R/W	05h	**DIMM Clock Stability Timer:** Number of clocks to wait after a self refresh exit before asserting CKE to bring the DIMMs out of self refresh
26:17	R/W	0A8h	**Master DLL Lock Timer:** This is the time taken for the master DLL in the Write, RCVEN and the DQS buffer to lock. This value must be programmed by BIOS based on memory controller clock (mdclk) freq and the DLL lock time requirements.
16	RO	0h	**Reserved**
15:10	R/W	0Fh	**IO Pad Reset Time:** This is the number of clocks taken for all of the system memory buffers to reset when the IOPADRST is deasserted. This value must be programmed by the BIOS based on the memory controller clock frequency (one fourth of DDR rate).
9	RO	0h	**Reserved**
8:0	R/W	032h	**Write Slave DLL Lock Timer:** This is the time taken for the Slave DLL in the Write, RCVEN and the DQS buffer to lock. This value must be programmed by BIOS based on memory controller clock freq and the DLL lock time requirements.

19.7.10 C0DRT5 - Channel 0 DRAM Timing Register 5

B/D/F/Type: 0/0/0/MCHBAR Chipset
Address Offset: 1224-1227h
Default Value: 62C32020h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:28	R/W	6h	**Reserved**
27:26	RO	00b	**Reserved**
25:22	R/W	Bh	**TS Read Delay:** Time taken for the TS read data to come back from the MPR register in the DRAM Min Time := BL/2 + CL + 2
21	RO	0b	**Reserved**
20:12	R/W	032h	**Read Slave DLL Lock Timer:** This is the time taken for the Slave DLL in the Write, RCVEN and the DQS buffer to lock. This value must be programmed by BIOS based on memory controller clock freq and the DLL lock time requirements.
11	RO	0b	**Reserved**
10:8	R/W	000b	**Reserved**
7:4	R/W	2h	**Read Diff Amp Select (DIFFAMPSEL):** The number of whole memory clocks to wait after sending a read command before asserting DIFFAMP.
3	R/W	0b	**Reserved**
2:1	R/W	00b	**DQ / DQS Sense Amp Duration**
0	R/W	0b	**Reserved**

19.7.11 C0DRC0 - Channel 0 DRAM Controller Mode 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1230-1233h
Default Value: 40000002h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:30	RO	01b	**Reserved**
29	R/W	0b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28	RO	0b	**Reserved**
27:24	RO	0h	**Reserved**
23:22	RO	0h	**Reserved**
21:20	RO	00b	**Reserved**
19:18	RO	00b	**Reserved**
17	RO	0h	**Reserved**
16	R/W	0h	**Address/Control Assertion Rule (ACAR):** Defines the number of clock cycles the MA, RASB, CASB, WEB are asserted. 0: always 2n rule (address and CMD are driven the clock prior to CSB assertion) 1: always 1n Rule (address and CMD are always driven on the same clock as CSB)
15	RO	0h	**Reserved**
14	RO	0b	**Reserved**
13:11	RO	0h	**Reserved**
10:8	R/W	000b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 010: Refresh enabled. Refresh interval 7.8 µsec 011: Refresh enabled. Refresh interval 3.9 µsec Other: Reserved
7	RO	0h	**Reserved**
6:4	R/W	000b	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. 000: Post Reset state. When the (G)MCH exits reset (power-up or otherwise), the mode select field is cleared to “000”.

Bit	Access	Default Value	Description
			During any reset sequence, while power is applied and reset is active, the (G)MCH deasserts all CKE signals. After internal reset is deasserted, CKE signals remain deasserted for some time (minimum 35us) and then are asserted. During suspend, (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, (G)MCH will be reset - which will clear this bit field to “000” and maintain CKE signals deasserted. After internal reset is deasserted, CKE signals remain deasserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, (G)MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. 001: NOP Command Enable - All CPU cycles to DRAM result in a NOP command on the DRAM interface. 010: All Banks Pre-charge Enable - All CPU cycles to DRAM result in an “all banks precharge” command on the DRAM interface. 011: Mode Register Set Enable - All CPU cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. **For DDR2** MA[6:4] need to be driven based on the value programmed in the Additive Latency field. **Additive Latency MA[5:3]** 0.0 Clocks 000 1.0 Clocks 001 2.0 Clocks 010 3.0 Clocks 011 4.0 Clocks 100 MA[10] must be set to 0 to enable DQSB strobe complements. For the remaining bit fields, refer to the JEDEC spec for DDR-II. 101: Reserved 110: CBR Refresh Enable: In this mode all CPU cycles to DRAM result in a CBR cycle on the DRAM interface 111: Normal operation
3	R/W	0b	**Burst Length (BL):** The burst length is the number of QWORDS returned by a DIMM per read command, when not interrupted. This bit is used to select the DRAM controller's Burst Length operation mode. It must be set to match to the behavior of the DIMM. 1: Burst Length of 8

Bit	Access	Default Value	Description
2	RO	0h	**Reserved**
1:0	RO	10b	**DRAM Type (DT):** Used to select between supported SDRAM types. 10: Second Revision Dual Data Rate (DDR2) SDRAM Other: Reserved

19.7.12 C0DRC1 - Channel 0 DRAM Controller Mode 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1234-1237h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:28	R/W	0h	**Reserved**
27	RO	0b	**Reserved**
26:24	R/W	000b	**Reserved**
23:20	RO	0h	**Reserved**
19:16	R/W	0h	**CKE Tri-state Enable Per Rank:** Bit 16 corresponds to rank 0 0: CKE is not tri-stated. 1: CKE is tri-stated. This is set only if the Rank is physically not populated.
15:13	RO	000b	**Reserved**
12	R/W	0b	**CS# Tri-state Enable (CSBTRIEN):** When set to a 1, the DRAM the controller will tri-state CS# when the corresponding CKE is deasserted. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
11	R/W	0b	**Address Tri-state Enable (ADRTRIEN):** When set to a 1, the DRAM controller will tri-state the MA, CMD, and CSB (CSB if lines only when all CKEs are deasserted. CKEs deassert based on Idle timer or max rank count control. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
10:7	RO	0h	**Reserved**
6	R/W	0b	**Reserved**
5:4	RO	00b	**Reserved**
3	R/W	0b	**Reserved**
2:0	RO	000b	**Reserved**

19.7.13 C0DRC2 - Channel 0 DRAM Controller Mode 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1238-123Bh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	**Reserved**
27:24	R/W	0h	**DRAM ODT Tri-state Enable Per Rank:** Bit 24 corresponds to rank 0 0: ODT is not tri-stated. 1: ODT is tri-stated. This is set only if the Rank is physically not populated.
23:14	RO	000h	**Reserved**
13	R/W	0b	**Clock Control to DQ Buffers:** 0: Clocks to DQ buffers are on for reads. 1: Clocks to DQ buffers are off for reads. Clock does not need to run once the first read or write to this channel has occurred. BIOS will set this bit once it has done the first read from this channel.
12	R/W	0b	**Reserved**
11:9	RO	000b	**Reserved**
8:0	RO	000h	**Reserved**

19.7.14 C0AIT - Channel 0 Adaptive Idle Timer Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1250-1257h
Default Value: 0000000000000000h
Access: RO; R/W
Size: 64 bits

This register controls Characteristics of Adaptive Idle Timer Mechanism. This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

19.7.15 C0DTEW1 - Channel 0 (G)MCH Throttling Event Weight 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 126C-126Fh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register contains programmable Event weights that are input into the averaging filter.

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:8	R/W	00h	**Toggle Write Event Weight:** This value is input to the filter if, in a given clock, a data write toggle assertion is detected
7:0	R/W	00h	**Toggle Read Event Weight:** This value is input to the filter if, in a given clock, a data read toggle assertion is detected

19.7.16 C0GTEW - Channel 0 (G)MCH Throttling Event Weight

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1270-1273h
Default Value: 00000000h
Access: R/W/L
Size: 32 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	Description
31:24	R/W/L	00h	**Read Weight:** This value is input to the filter if in a given clock there is a valid read command being issued on the memory bus.
23:16	R/W/L	00h	**Write Weight:** This value is input to the filter if in a given clock there is a valid write command being issued on the memory bus.
15:8	R/W/L	00h	**Command Weight:** This value is input to the filter if in a given clock there is a valid command other than a read or a write being issued on the memory bus.
7:0	R/W/L	00h	**Idle Weight:** This value is input to the filter if in a given clock there is no command being issued on the memory bus. If command and address are tri-stated a value of 0 is input to the filter. If command and address are under reduced drive strength after this value is divided by 2 and input to the filter.

19.7.17 C0GTC - Channel 0 (G)MCH Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1274-1277h
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	Description
31	R/W/L	0b	**(G)MCH Throttle Lock (GTLOCK):** This bit secures the (G)MCH throttling control registers GTEW, GTC and TSWDT. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits are read-only.
30	RO	0b	**Reserved**
29	R/W/L	0b	**Reserved**
28:25	RO	0h	**Reserved**
24:22	R/W/L	000b	**Reserved**
21	R/W/L	0b	**(G)MCH Bandwidth Based Throttling Enable:** 0: Bandwidth Threshold (WAB) is not used for throttling. 1: Bandwidth Threshold (WAB) is used for throttling. If both bandwidth based and thermal sensor based throttling modes are on and the thermal sensor trips, the thermal threshold is used for throttling.
20	R/W/L	0b	**(G)MCH Thermal Sensor Trip Enable:** 0: (G)MCH throttling is not initiated when the (G)MCH thermal sensor trips. 1: (G)MCH throttling is initiated when the (G)MCH thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19	RO	0b	**Reserved**
18:16	R/W/L	000b	**Reserved**
15:8	R/W/L	00h	**WAB:** Threshold allowed per clock for bandwidth based throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	**WAT:** Threshold allowed per clock during thermal sensor enabled throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.

19.7.18 C0DTPEW - Channel 0 DRAM Rank Throttling Passive Event

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1278-127Fh
Default Value: 0000000000000000h
Access: RO; R/W/L
Size: 64 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks. (G)MCH implements 4 independent filters, one per rank. All bits in this register can be locked by the DTLOCK bit in the C0DTC register.

Bit	Access	Default Value	Description
63:48	RO	0000h	**Reserved**
47:40	R/W/L	00h	**Additive Weight for ODT:** This value is added to the total weight of a Rank if ODT on that rank is asserted. Note that this value should reflect whether the DRAMs have been programmed for 75- or 150-Ω termination.
39:32	R/W/L	00h	**Weight for Any Open Page during Active (WAOPDA):** This value is input to the filter if, during the present clock, the corresponding rank has any pages open and is not in power down. The value programmed here is IDD3N from the JEDEC.
31:24	R/W/L	00h	**All Banks Precharge Active (ABPA):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged but is not in power down. The value programmed here is IDD2N from the JEDEC spec.
23:16	R/W/L	00h	**Weight for Any Open Page during Power Down (WAOPDPD):** This value is input to the filter if, during the present clock, the corresponding rank is in power down with pages open. The value programmed here is IDD3P from the JEDEC.
15:8	R/W/L	00h	**All Banks Precharge Power Down (ABPPD):** This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged and is powered down. The value programmed here is IDD2P from the JEDEC spec.
7:0	R/W/L	00h	**Self Refresh:** This value is input to the filter if in a clock the corresponding rank is in self refresh.

19.7.19 C0DTAEW - Channel 0 DRAM Rank Throttling Active Event

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1280-1287h
Default Value: 0000000000000000h
Access: RO; R/W/L
Size: 64 bits

This register contains programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length, 1N/2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks. (G)MCH implements 4 independent filters, one per rank. In the clock (G)MCH asserts a command to the DRAM (via CS# assertion) based on the command type the one of the weights specified in this register is added to the weight specified in the previous register and input to the filter.

Bit	Access	Default Value	Description
63:56	RO	00h	**Read with AP**
55:48	RO	00h	**Write with AP**
47:40	R/W/L	00h	**Read**
39:32	R/W/L	00h	**Write**
31:24	R/W/L	00h	**Precharge – All**
23:16	R/W/L	00h	**Precharge**
15:8	R/W/L	00h	**Activate**
7:0	R/W/L	00h	**Refresh**

19.7.20 C0DTC - Channel 0 DRAM Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1288-128Bh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

This register is for programmable Event weights that are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The Bios must account for burst length, 1N/2N rule considerations. It is also possible for bios to take into account type loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	Description
31	R/W/L	0b	**DRAM Throttle Lock (DTLOCK):** This bit secures the DRAM throttling control registers DT*EW and DTC. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits are read-only.
30	RO	0b	**Reserved**
29	R/W/L	0b	**Reserved**
28:25	RO	0h	**Reserved**
24:22	R/W/L	000b	**Reserved**
21	R/W/L	0b	**(G)MCH Bandwidth Based Throttling Enable:** 0: Bandwidth Threshold (WAB) is not used for throttling. 1: Bandwidth Threshold (WAB) is used for throttling. If both bandwidth based and thermal sensor based throttling modes are on and the thermal sensor trips, the thermal threshold is used for throttling.
20	R/W/L	0b	**(G)MCH Thermal Sensor Trip Enable:** 0: (G)MCH throttling is not initiated when the (G)MCH thermal sensor trips. 1: (G)MCH throttling is initiated when the (G)MCH thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19	RO	0b	**Reserved**
18:16	R/W/L	000b	**Time Constant:** 000: 2^28 Clocks 001: 2^29 Clocks 010: 2^30 Clocks 011: 2^31 Clocks 1XX: Reserved

Bit	Access	Default Value	Description
15:8	R/W/L	00h	**WAB:** Threshold allowed per clock for bandwidth based throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	**WAT:** Threshold allowed per clock during for thermal sensor enabled throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.

19.7.21 C1DRB01 - Channel 1 DRAM Rank Boundary 0/1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1300-1303h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRB01.

19.7.22 C1DRB23 - Channel 1 DRAM Rank Boundary 2/3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1304-1307h
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00h	**Reserved**

19.7.23 C1DRA - Channel 1 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1308-130Bh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRA.

19.7.24 C1DCLKDIS - Channel 1 DRAM Clock Disable

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 130C-130Fh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DCLKDIS.

19.7.25 C1DRT0 - Channel 1 DRAM Timing Register 0

B/D/F/Type: 0/0/0/MCHBAR Chipset
Address Offset: 1310-1313h
Default Value: 34B10461h
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRT0.

19.7.26 C1DRT1 - Channel 1 DRAM Timing Register 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1314-1317h
Default Value: 11E08463h
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRT1.

19.7.27 C1DRT2 - Channel 1 DRAM Timing Register 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1318-131Bh
Default Value: 2200105Fh
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRT2.

19.7.28 C1DRT3 - Channel 1 DRAM Timing Register 3

B/D/F/Type: 0/0/0/MCHBAR Chipset
Address Offset: 131C-131Fh
Default Value: 01056101h
Access: RO; R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRT3.

19.7.29 C1DRT4 - Channel 1 DRAM Timing Register 4

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1320-1323h
Default Value:	29503C32h
Access:	RO; R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT4.

19.7.30 C1DRT5 - Channel 1 DRAM timing register 5

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1324-1327h
Default Value:	62C32020h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT5.

19.7.31 C1DRC0 - Channel 1 DRAM Controller Mode 0

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1330-1333h
Default Value:	40000002h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC0.

19.7.32 C1DRC1 - Channel 1 DRAM Controller Mode 1

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1334-1337h
Default Value:	00000000h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC1.

19.7.33 C1DRC2 - Channel 1 DRAM Controller Mode 2

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1338-133Bh
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC2.

19.7.34 C1AIT - Channel 1 Adaptive Idle Timer Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1350-1357h
Default Value:	0000000000000000h
Access:	R/W; RO
Size:	64 bits

This register controls Characteristics of Adaptive Idle Timer Mechanism. The operation of this register is detailed in the description for register C0AIT.

19.7.35 C1DTEW1 - Channel 1 (G)MCH Throttling Event Weight 1

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	136C-136Fh
Default Value:	00000000h
Access:	R/W; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0DTEW1.

19.7.36 C1GTEW - Channel 1 (G)MCH Throttling Event Weight

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1370-1373h
Default Value:	00000000h
Access:	R/W/L
Size:	32 bits

The operation of this register is detailed in the description for register C0GTEW.

19.7.37 C1GTC - Channel 1 (G)MCH Throttling Control

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1374-1377h
Default Value:	00000000h
Access:	R/W/L; RO
Size:	32 bits

The operation of this register is detailed in the description for register C0GTC.

19.7.38 C1DTPEW - Channel 1 DRAM Rank Throttling Passive Event

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1378-137Fh
Default Value:	0000000000000000h
Access:	RO; R/W/L
Size:	64 bits

The operation of this register is detailed in the description for register C0DTPEW.

19.7.39 C1DTAEW - Channel 1 DRAM Rank Throttling Active Event

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1380-1387h
Default Value: 0000000000000000h
Access: RO; R/W/L
Size: 64 bits

The operation of this register is detailed in the description for register C0DTAEW.

19.7.40 C1DTC - Channel 1 DRAM Throttling Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 1388-138Bh
Default Value: 00000000h
Access: R/W/L; RO
Size: 32 bits

The operation of this register is detailed in the description for register C0DTC.

19.8 DMI RCRB

This section describes the mapped register for DMI. The DMIBAR register, described in Section 18.1.17 provides the base address or these registers.

This Root Complex Register Block (RCRB) controls (G)MCH –ICH8M serial interconnect. An RCRB is required for configuration and control of element that are located internal to root complex that are not directly associated with a PCI Express device. The base address of this space is programmed in DMIBAR in Device 0 config space.

Note: All RCRB register spaces needs to remain organized as they are here. The Virtual Channel capabilities (or at least the first PCI Express Extended Capability) must begin at the 0h offset of the 4-K area pointed to by the associated BAR. This is a PCI Express 1.0 specification requirement.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DMI Virtual Channel Enhanced Capability	DMIVCECH	0	3	04010002h	RO
DMI Port VC Capability Register 1	DMIPVCCAP1	4	7	00000001h	RO; R/WO
DMI Port VC Capability Register 2	DMIPVCCAP2	8	B	00000001h	RO
DMI Port VC Control	DMIPVCCTL	C	D	0000h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		E	F		
DMI VC0 Resource Capability	DMIVC0RCAP	10	13	00000001h	RO
DMI VC0 Resource Control	DMIVC0RCTL0	14	17	800000FFh	RO; R/W
Reserved		18	19		
DMI VC0 Resource Status	DMIVC0RSTS	1A	1B	0002h	RO
DMI VC1 Resource Capability	DMIVC1RCAP	1C	1F	00008001h	RO
DMI VC1 Resource Control	DMIVC1RCTL1	20	23	01000000h	RO; R/W
Reserved		24	25		
DMI VC1 Resource Status	DMIVC1RSTS	26	27	0002h	RO
Reserved		28	3F		
DMI Root Complex Link Declaration	DMIRCLDECH	40	43	08010005h	RO
DMI Element Self Description	DMIESD	44	47	01000202h	RO; R/WO
Reserved		48	4F		
DMI Link Entry 1 Description	DMILE1D	50	53	00000000h	R/WO; RO
Reserved		54	57		
DMI Link Entry 1 Address	DMILE1A	58	5F	0000000000000000h	RO; R/WO
DMI Link Entry 2 Description	DMILE2D	60	63	00000000h	RO; R/WO
Reserved		64	67		
DMI Link Entry 2 Address	DMILE2A	68	6F	0000000000000000h	RO; R/WO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		70	83		
DMI Link Capabilities	DMILCAP	84	87	00012C41h	RO; R/WO
DMI Link Control	DMILCTL	88	89	0000h	RO; R/W
DMI Link Status	DMILSTS	8A	8B	0001h	RO

19.8.1 DMIVCECH - DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 0-3h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access	Default Value	Description
31:20	RO	040h	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

19.8.2 DMIPVCCAP1 - DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 4-7h
Default Value: 00000001h
Access: RO; R/WO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	**Reserved**
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	**Reserved**
2:0	R/WO	001b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.

19.8.3 DMIPVCCAP2 - DMI Port VC Capability Register 2

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8-Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23:8	RO	0000h	**Reserved**
7:0	RO	01h	**VC Arbitration Capability (VCAC):** Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority.

19.8.4 DMIPVCCTL - DMI Port VC Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: C-Dh
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	**Reserved**
3:1	R/W	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000: Hardware fixed arbitration scheme, for example, Round Robin. Others: Reserved See the PCI express specification for more details.
0	RO	0b	**Reserved**

19.8.5 DMIVC0RCAP - DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 10-13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23	RO	0b	**Reserved**
22:16	RO	00h	**Reserved**
15	RO	0b	**Reject Snoop Transactions (REJSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

19.8.6 DMIVC0RCTL0 - DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 14-17h
Default Value: 800000FFh
Access: RO; R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**Virtual Channel 0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	**Reserved**
26:24	RO	000b	**Virtual Channel 0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	**Reserved**
19:17	R/W	000b	**Port Arbitration Select (PAS):** Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted.
16:8	RO	000h	**Reserved**
7:1	R/W	7Fh	**Traffic Class / Virtual Channel 0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	**Traffic Class 0 / Virtual Channel 0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

19.8.7 DMIVC0RSTS - DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1A-1Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	1b	**Virtual Channel 0 Negotiation Pending (VC0NP):** 0:The VC negotiation is complete. 1:The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	**Reserved**

19.8.8 DMIVC1RCAP - DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1C-1Fh
Default Value: 00008001h
Access: RO;
Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	**Reserved**
23	RO	0b	**Reserved**
22:16	RO	00h	**Reserved**
15	RO	1b	**Reject Snoop Transactions (REJSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

19.8.9 DMIVC1RCTL1 - DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 20-23h
Default Value: 01000000h
Access: R/W; RO
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access	Default Value	Description
31	R/W	0b	**Virtual Channel 1 Enable (VC1E):** 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27	RO	0h	**Reserved**
26:24	R/W	001b	**Virtual Channel 1 ID (VC1ID):** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO	0h	**Reserved**
19:17	R/W	000b	**Port Arbitration Select (PAS):** Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO	000h	**Reserved**

Bit	Access	Default Value	Description
7:1	R/W	00h	**Traffic Class / Virtual Channel 1 Map (TCVC1M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	0b	**Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

19.8.10 DMIVC1RSTS - DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 26-27h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	1b	**Virtual Channel 1 Negotiation Pending (VC1NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	**Reserved**

19.8.11 DMIRCLDECH - DMI Root Complex Link Declaration

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 40-43h
Default Value: 08010005h
Access: RO
Size: 32 bits

This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component.

Bit	Access	Default Value	Description
31:20	RO	080h	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Internal Link Control Capability).
19:16	RO	1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO	0005h	**Extended Capability ID (ECID):** Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

19.8.12 DMIESD - DMI Element Self Description

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 44-47h
Default Value: 01000202h
Access: RO; R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	01h	**Port Number (PORTNUM):** Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO	00h	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:8	RO	02h	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 2 (one for (G)MCH egress port to main memory and one to egress port belonging to ICH on other side of internal link).
7:4	RO	0h	**Reserved**
3:0	RO	2h	**Element Type (ETYP):** Indicates the type of the Root Complex Element. Value of 2 h represents an Internal Root Complex Link (DMI).

19.8.13 DMILE1D - DMI Link Entry 1 Description

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 50-53h
Default Value: 00000000h
Access: R/WO; RO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	R/WO	00h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (egress port of ICH). The target port number is with respect to the component that contains this element as specified by the target component ID. This can be programmed by BIOS, but the default value will likely be correct because the DMI RCRB in the ICH will likely be associated with the default egress port for the ICH meaning it will be assigned port number 0.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RO	0000h	**Reserved**
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

19.8.14 DMILE1A - DMI Link Entry 1 Address

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 58-5Fh
Default Value: 0000000000000000h
Access: RO; R/WO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (egress port of ICH) for this link entry.
11:0	RO	000h	**Reserved**

19.8.15 DMILE2D - DMI Link Entry 2 Description

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 60-63h
Default Value: 00000000h
Access: RO; R/WO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RO	0000h	**Reserved**
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

19.8.16 DMILE2A - DMI Link Entry 2 Address

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 68-6Fh
Default Value: 0000000000000000h
Access: RO; R/WO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	**Reserved**

19.8.17 DMILCAP - DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 84-87h
Default Value: 00012C41h
Access: RO; R/WO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access	Default Value	Description
31:18	RO	0000h	**Reserved**
17:15	R/WO	010b	**L1 Exit Latency (L1SELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. 000: Less than 1 µs 00: 1 µs to less than 2 µs 010: 2 µs to less than 4 µs 011: 4 µs to less than 8 µs 100: 8 µs to less than 16 µs 101: 16 µs to less than 32 µs 110: 32 µs-64 µs 111: More than 64 µs Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	R/WO	010b	**L0s Exit Latency (L0SELAT):** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 µs 101: 1 µs to less than 2 µs 110: 2 µs-4 µs 111: More than 4 µs
11:10	RO	11b	**Active State Link PM Support (ASLPMS):** L0s & L1 entry supported.
9:4	RO	04h	**Max Link Width (MLW):** Indicates the maximum number of lanes supported for this link.
3:0	RO	1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

19.8.18 DMILCTL - DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 88-89h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register allows control of DMI.

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	R/W	0b	**Extended Synch (EXTSYNC):** 0: Standard Fast Training Sequence (FTS). 1: Forces extended transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP Ordered Set prior to entering L0, and the transmission of 1024 TS1 ordered sets in the RecoveryRcvrLock state prior to entering the RecoveryRcvrCfg state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6:3	RO	0000b	**Reserved**
2	R/W	0b	**Reserved**
1:0	R/W	00b	**Active State Power Management Support (ASPMS):** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Entry Supported

19.8.19 DMILSTS - DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8A-8Bh
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access	Default Value	Description
15:10	RO	00h	**Reserved**
9:4	RO	00h	**Negotiated Width (NWID):** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 0h: Reserved 1h: X1 2h: X2 4h: X4 All other encodings are Reserved
3:0	RO	1h	**Negotiated Speed (NSPD):** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are Reserved

19.9 Egress Port (EP) RCRB

This Root Complex Register Block (RCRB) controls the port arbitration that is based on the PCI Express 1.0 specification. Port arbitration is done for all PCI Express based isochronous requests (always on Virtual Channel 1) before being submitted to the main memory arbiter. The base address of this space is programmed in the EPBAR in Device 0 config space.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		0	3		
EP Port VC Capability Register 1	EPPVCCAP1	4	7	00000401h	RO; R/WO
EP Port VC Capability Register 2	EPPVCCAP2	8	B	00000001h	RO
Reserved		C	F		
EP VC 0 Resource Capability	EPVC0RCAP	10	13	00000001h	RO
EP VC 0 Resource Control	EPVC0RCTL	14	17	800000FFh	RO; R/W
Reserved		18	19		
EP VC 0 Resource Status	EPVC0RSTS	1A	1B	0000h	RO
EP VC 1 Resource Capability	EPVC1RCAP	1C	1F	10008010h	RO; R/WO
EP VC 1 Resource Control	EPVC1RCTL	20	23	01080000h	R/W; RO; R/W/S
Reserved		24	25		
EP VC 1 Resource Status	EPVC1RSTS	26	27	0000h	RO
EP VC 1 Maximum Number of Time Slots	EPVC1MTS	28	2B	04050609h	R/W
EP VC 1 Isoch Timing Control	EPVC1ITC	2C	2F	00000000h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved	EPVC1IWT	30	37	00000000000 00000h	R/W
EP VC 1 Isoch Slot Time	EPVC1IST	38	3F	00000000000 00000h	R/W
Reserved		40	43		
EP Element Self Description	EPESD	44	47	00000201h	RO; R/WO
Reserved		48	4F		
EP Link Entry 1 Description	EPLE1D	50	53	01000000h	RO; R/WO
Reserved		54	57		
EP Link Entry 1 Address	EPLE1A	58	5F	00000000000 00000h	RO; R/WO
EP Link Entry 2 Description	EPLE2D	60	63	02000002h	RO; R/WO
EP Link Entry 2 Address	EPLE2A	68	6F	00000000000 08000h	RO
Reserved		70	9F		
Port Arbitration Table	PORTARB	100	11F	00000000000 00000000000 00000000000 00000000000 00000000000 000000000h	R/W

19.9.1 EPPVCCAP1 - EP Port VC Capability Register 1

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 4-7h
Default Value: 00000401h
Access: RO; R/WO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:12	RO	00000h	**Reserved**
11:8	RO	04h	**Reserved**
7:3	RO	0h	**Reserved**
2:0	R/WO	001b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

19.9.2 EPPVCCAP2 - EP Port VC Capability Register 2

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 8-Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port. This register bit field shall contain default value unless otherwise indicated in the BIOS Specification.

19.9.3 EPVC0RCAP - EP VC 0 Resource Capability

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 10-13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15	RO	0b	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	01h	**Port Arbitration Capability (PAC):** Indicates types of Port Arbitration supported by this VC 0 resource.

19.9.4 EPVC0RCTL - EP VC 0 Resource Control

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 14-17h
Default Value: 800000FFh
Access: RO; R/W;
Size: 32 bits

Controls the resources associated with Egress Port Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**VC0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	**Reserved**
26:24	RO	000b	**VC0 ID (VC0ID):** For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	**Reserved**
19:17	RO	000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service.
16:8	RO	000h	**Reserved**
7:1	R/W	7Fh	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource.
0	RO	1b	**Reserved**

19.9.5 EPVC0RSTS - EP VC 0 Resource Status

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 1A-1Bh
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	0b	**VC0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	**Reserved**

19.9.6 EPVC1RCAP - EP VC 1 Resource Capability

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 1C-1Fh
Default Value: 10008010h
Access: RO; R/WO
Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	10h	**Reserved**
23	RO	0b	**Reserved**
22:16	R/WO	00h	**Reserved**
15	RO	1b	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	**Reserved**
7:0	RO	10h	**Port Arbitration Capability (PAC):** Indicates types of Port Arbitration supported by this VC1 resource.

19.9.7 EPVC1RCTL - EP VC 1 Resource Control

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 20-23h
Default Value: 01080000h
Access: R/W; RO; R/W/S
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access	Default Value	Description
31	R/W	0b	**VC1 Enable (VC1E):** Upon Read after negotiation 0: Virtual Channel is disabled. 1: Virtual Channel is enabled.
30:27	RO	0h	**Reserved**
26:24	R/W	001b	**VC1 ID (VC1ID):** Assigns a VC ID to the VC resource. Assigned value must be non-zero.
23:20	RO	0h	**Reserved**
19:17	R/W	100b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service.
16	R/W/S	0b	**Reserved**
15:8	RO	00h	**Reserved**
7:1	R/W	00h	**TC/VC1 Map (TCVC1M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource.
0	RO	0b	**TC0/VC1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

19.9.8 EPVC1RSTS - EP VC 1 Resource Status

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 26-27h
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	0b	**VC1 Negotiation Pending (VC1NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	**Reserved**

19.9.9 EPVC1MTS - EP VC 1 Maximum Number of Time Slots

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 28-2Bh
Default Value: 04050609h
Access: R/W
Size: 32 bits

The fields in this register reflect the maximum number of time slots supported by the (G)MCH for various configurations. This register bit field shall contain the default value unless otherwise indicated in BIOS specification.

19.9.10 EPVC1ITC - EP VC 1 Isoch Timing Control

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 2C-2Fh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

This register reflects the number of common host clocks (Hclks) per time slot. This register bit field shall contain the default value unless otherwise indicated in BIOS specification.

19.9.11 EPVC1IST - EP VC 1 Isoch Slot Time

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 38-3Fh
Default Value: 0000000000000000h
Access: R/W
Size: 64 bits

This register reflects the number of common host clocks per time slot. This register bit field shall contain the default value unless otherwise indicated in BIOS specification.

19.9.12 EPESD - EP Element Self Description

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 44-47h
Default Value: 00000201h
Access: RO; R/WO
Size: 32 bits

This register provides information about the root complex element containing this link declaration capability.

Bit	Access	Default Value	Description
31:24	RO	00h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00h indicates to configuration software that this is the default egress port.
23:16	R/WO	00h	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element.
15:8	RO	02h	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCIe and DMI).
7:4	RO	0h	**Reserved**
3:0	RO	1h	**Element Type (ET):** Indicates the type of the Root Complex Element. Value of 1h represents a port to system memory.

19.9.13 EPLE1D - EP Link Entry 1 Description

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 50-53h
Default Value: 01000000h
Access: RO; R/WO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	01h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry.
15:2	RO	0000h	**Reserved**
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB (Root Complex Register Block)
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

19.9.14 EPLE1A - EP Link Entry 1 Address

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 58-5Fh
Default Value: 0000000000000000h
Access: RO; R/WO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0	RO	000h	**Reserved**

19.9.15 EPLE2D - EP Link Entry 2 Description

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 60-63h
Default Value: 02000002h
Access: RO; R/WO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	02h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component.
15:2	RO	0000h	**Reserved**
1	RO	1b	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port. The link address specifies the configuration address (Segment, Bus, Device, Function) of the target root port.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

19.9.16 EPLE2A - EP Link Entry 2 Address

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 68-6Fh
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:28	RO	000000000h	**Reserved**
27:20	RO	00h	**Bus Number (BUSN)**
19:15	RO	00001b	**Device Number (DEVN):** Target for this link is PCI Express x16 port (Device 1).
14:12	RO	000b	**Function Number (FUNN)**
11:0	RO	000h	**Reserved**

19.9.17 PORTARB - Port Arbitration Table

B/D/F/Type: 0/0/0/EPBAR
Address Offset: 100-11Fh
Default Value:
00000000000000000000000000000000000000000000000000000000000000000000000000000000h
Access: R/W
Size: 256 bits

The Port Arbitration Table register is a read-write register array used to store the arbitration table for Port Arbitration of the Egress Port VC resource. The register bit field shall contain the default values otherwise indicated in BIOS Specification.

§

20 PCI Express* Graphics Device 1 Configuration Registers (D1:F0)

Device 1 contains the controls associated with the x16 root port that is the intended attach point for external graphics. It is typically referred to as PEG (PCI Express Graphics) port. It also functions as the virtual PCI-to-PCI Bridge that was previously associated with AGP.

Warning: When reading the PCI Express "conceptual" registers such as these, you may not get a valid value unless the register value is stable.

The PCI Express Specification defines two types of reserved bits:

- Reserved and Preserved: Reserved for future RW implementations; software must preserve value read for writes to these bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to these bits.

Unless explicitly documented as Reserved and Zero, all bits marked as Reserved are part of the Reserved and Preserved type which has historically been the typical definition for Reserved.

Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first disable the link, then program the registers, then re-enable the link (which will cause a full-retrain with the new settings).

20.1 PEG Device 1 Function 0 Configuration Registers Summary

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID1	0	1	8086h	RO
Device Identification	DID1	2	3	2A01h[1] 2A11h[2]	RO
PCI Command	PCICMD1	4	5	0000h	RO; R/W
PCI Status	PCISTS1	6	7	0010h	RO; R/WC
Revision Identification	RID1	8	8	00h	RO
Class Code	CC1	9	B	060400h	RO
Cache Line Size	CL1	C	C	00h	R/W
Header Type	HDR1	E	E	01h	RO
Reserved		F	17		
Primary Bus Number	PBUSN1	18	18	00h	RO
Secondary Bus Number	SBUSN1	19	19	00h	R/W
Subordinate Bus Number	SUBUSN1	1A	1A	00h	R/W
Reserved		1B	1B		
I/O Base Address	IOBASE1	1C	1C	F0h	RO; R/W
I/O Limit Address	IOLIMIT1	1D	1D	00h	RO; R/W
Secondary Status	SSTS1	1E	1F	0000h	R/WC; RO
Memory Base Address	MBASE1	20	21	FFF0h	RO; R/W
Memory Limit Address	MLIMIT1	22	23	0000h	RO; R/W
Prefetchable Memory Base Address	PMBASE1	24	25	FFF1h	RO; R/W
Prefetchable Memory Limit Address	PMLIMIT1	26	27	0001h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Prefetchable Memory Base Address	PMBASEU1	28	2B	0000000Fh	R/W
Prefetchable Memory Limit Address	PMLIMITU1	2C	2F	00000000h	R/W
Reserved		30	33		
Capabilities Pointer	CAPPTR1	34	34	88h	RO
Reserved		35	3B		
Interrupt Line	INTRLINE1	3C	3C	00h	R/W
Interrupt Pin	INTRPIN1	3D	3D	01h	RO
Bridge Control	BCTRL1	3E	3F	0000h	RO; R/W
Reserved		40	7F		
Power Management Capabilities	PM_CAPID1	80	83	C8039001h	RO
Power Management Control/Status	PM_CS1	84	87	00000000h	RO; R/W/S; R/W
Subsystem ID and Vendor ID Capabilities	SS_CAPID	88	8B	0000800Dh	RO
Subsystem ID and Subsystem Vendor ID	SS	8C	8F	00008086h	R/WO
Message Signaled Interrupts Capability ID	MSI_CAPID	90	91	A005h	RO
Message Control	MC	92	93	0000h	RO; R/W
Message Address	MA	94	97	00000000h	RO; R/W
Message Data	MD	98	99	0000h	R/W
Reserved		9A	9F		
PCI Express-G Capability List	PEG_CAPL	A0	A1	0010h	RO
PCI Express-G Capabilities	PEG_CAP	A2	A3	0141h	RO; R/WO
Device Capabilities	DCAP	A4	A7	00008000h	RO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Device Control	DCTL	A8	A9	0000h	RO; R/W
Device Status	DSTS	AA	AB	0000h	RO; R/WC
Link Capabilities	LCAP	AC	AF	02014D01h	RO; R/WO
Link Control	LCTL	B0	B1	0040h	RO; R/W
Link Status	LSTS	B2	B3	1001h	RO
Slot Capabilities	SLOTCAP	B4	B7	00040000h	R/WO; RO
Slot Control	SLOTCTL	B8	B9	01C0h	RO; R/W
Slot Status	SLOTSTS	BA	BB	0000h	RO; R/WC
Root Control	RCTL	BC	BD	0000h	RO; R/W
Reserved		BE	BF		
Root Status	RSTS	C0	C3	00000000h	RO; R/WC
Reserved		C4	EB		
PCI Express-G Legacy Control	PEGLC	EC	EF	00000000h	RO; R/W
Reserved		F0	FF		

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965, GLE960 and GL960 Express Chipsets.
2. Valid for the Mobile Intel GME965 Express Chipset only.

20.1.1 VID1 - Vendor Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register to uniquely identify any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

20.1.2 DID1 - Device Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 2-3h
Default Value: 2A01h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	2A01h[1] 2A11h[2]	**Device Identification Number (DID1):** Identifier assigned to the (G)MCH Device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port).

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965, GLE960, and GL960 Express Chipsets.
2. Valid for the Mobile Intel GME965 Chipset only.

20.1.3 PCICMD1 - PCI Command

B/D/F/Type: 0/1/0/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; R/W;
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	R/W	0b	**INTA Assertion Disable (INTAAD):** 0: This device is permitted to generate INTA interrupt messages. 1: This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be deasserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and deassert messages.
9	RO	0b	**Fast Back-to-Back Enable (FB2B):** Hardwired to 0.
8	R/W	0b	**SERR Message Enable (SERRE1):** Controls Device 1 SERR messaging. The (G)MCH communicates the SERRB condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control Register 0: The SERR message is generated by the (G)MCH for Device 1 only under conditions enabled individually through the Device Control Register. 1: The (G)MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO	0b	**Reserved**
6	R/W	0b	**Parity Error Enable (PERRE):** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0: Master Data Parity Error bit in PCI Status register can NOT be set. 1: Master Data Parity Error bit in PCI Status register CAN be set.
5	RO	0b	**VGA Palette Snoop (VGAPS):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access	Default Value	Description
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not Applicable or Implemented. Hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Not Applicable or Implemented. Hardwired to 0.
2	R/W	0b	**Bus Master Enable (BME):** Controls the ability of the PEG port to forward Memory and IO Read/Write Requests in the upstream direction. 0: This device is prevented from making memory or IO requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address 0 with byte enables deasserted. Reads will be forwarded to memory address 0 and will return Unsupported Request status (or Master abort) in its completion packet. 1: This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.
1	R/W	0b	**Memory Access Enable (MAE):** 0: All of Device 1's memory space is disabled. 1: Enable the Memory and Prefetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W	0b	**IO Access Enable (IOAE):** 0: All of Device 1's I/O space is disabled. 1: Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

20.1.4 PCISTS1 - PCI Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 6-7h
Default Value: 0010h
Access: RO; R/WC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the (G)MCH.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (we don't do error forwarding).
14	R/WC	0b	**Signaled System Error (SSE):** This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO	0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO	0b	**Received Target Abort Status (RTAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO	0b	**Signaled Target Abort Status (STAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	00b	**DEVSELB Timing (DEVT):** This device is not the subtractively decoded device on Bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO	0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PEG's virtual PCI-to-PCI bridge is integrated with the (G)MCH functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as an R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access	Default Value	Description
6	RO	0b	**Reserved**
5	RO	0b	**66-/60-MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4	RO	1b	**Capabilities List (CAPL):** Indicates that a capabilities list is present. Hardwired to 1.
3	RO	0b	**INTA Status (INTAS):** Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and deassert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit. Note that INTA emulation interrupts received across the link are not reflected in this bit.
2:0	RO	000b	**Reserved**

20.1.5 RID1 - Revision Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device 1. These bits are read only and writes to this register have no effect.

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID1):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch

20.1.6 CC1 - Class Code

B/D/F/Type: 0/1/0/PCI
Address Offset: 9-Bh
Default Value: 060400h
Access: RO;
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register- specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO	04h	**Sub-Class Code (SUBCC):** Indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO	00h	**Programming Interface (PI):** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

20.1.7 CL1 - Cache Line Size

B/D/F/Type: 0/1/0/PCI
Address Offset: Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access	Default Value	Description
7:0	R/W	00h	**Cache Line Size (Scratch Pad):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

20.1.8 HDR1 - Header Type

B/D/F/Type: 0/1/0/PCI
Address Offset: Eh
Default Value: 01h
Access: RO;
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	Description
7:0	RO	01h	**Header Type Register (HDR):** Returns 01 to indicate that this is a single function device with bridge header layout.

20.1.9 PBUSN1 - Primary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this "virtual" Host-PCI Express Bridge is connected to PCI Bus 0.

Bit	Access	Default Value	Description
7:0	RO	00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

20.1.10 SBUSN1 - Secondary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge i.e., to PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access	Default Value	Description
7:0	R/W	00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express-G.

20.1.11 SUBUSN1 - Subordinate Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access	Default Value	Description
7:0	R/W	00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device 1 bridge. When only a single PCI device resides on the PCI Express-G segment, this register will contain the same value as the SBUSN1 register.

20.1.12 IOBASE1 - I/O Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ch
Default Value: F0h
Access: R/W; RO
Size: 8 bits

This register controls the CPU to PCI Express-G I/O access routing based on the following formula:
IO_BASE=< address =<IO_LIMIT
Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Access	Default Value	Description
7:4	R/W	Fh	**I/O Address Base (IOBASE):** Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express-G. BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0	RO	0h	**Reserved**

20.1.13 IOLIMIT1 - I/O Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Dh
Default Value: 00h
Access: R/W; RO
Size: 8 bits

This register controls the CPU to PCI Express-G I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Access	Default Value	Description
7:4	R/W	0h	**I/O Address Limit (IOLIMIT):** Corresponds to A[15:12] of the I/O address limit of Device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO	0h	**Reserved**

20.1.14 SSTS1 - Secondary Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 1E-1Fh
Default Value: 0000h
Access: R/WC; RO
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express-G side) of the "virtual" PCI-PCI bridge embedded within (G)MCH.

Bit	Access	Default Value	Description
15	R/WC	0b	**Detected Parity Error (DPE):** When set indicates that the (G)MCH received across the link (upstream) a Posted Write Data Poisoned TLP (EP=1).
14	R/WC	0b	**Received System Error (RSE):** This bit is set when the secondary side receives an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.

Bit	Access	Default Value	Description
13	R/WC	0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	R/WC	0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO	0b	**Signaled Target Abort (STA):** Not Applicable or Implemented. Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).
10:9	RO	00b	**DEVSELB Timing (DEVT):** Not Applicable or Implemented. Hardwired to 0.
8	R/WC	0b	**Master Data Parity Error (SMDPE):** When set indicates that the (G)MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	**Reserved**
5	RO	0b	**66-/60-MHz Capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4:0	RO	00h	**Reserved**

20.1.15 MBASE1 - Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 20-21h
Default Value: FFF0h
Access: R/W; RO
Size: 16 bits

This register controls the CPU to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
15:4	R/W	FFFh	**Memory Address Base (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express-G.
3:0	RO	0h	**Reserved**

20.1.16 MLIMIT1 - Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 22-23h
Default Value: 0000h
Access: R/W; RO
Size: 16 bits

This register controls the CPU to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express-G address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be

performed in a true plug-and-play manner to the prefetchable address range for improved CPU- PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e., prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access	Default Value	Description
15:4	R/W	000h	**Memory Address Limit (MLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express-G.
3:0	RO	0h	**Reserved**

20.1.17 PMBASE1 - Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 24-25h
Default Value: FFF1h
Access: R/W; RO
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
15:4	R/W	FFFh	**Prefetchable Memory Base Address (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express-G.
3:0	RO	1h	**64-bit Address Support:** Indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.

20.1.18 PMLIMIT1 - Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 26-27h
Default Value: 0001h
Access: R/W; RO
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Bit	Access	Default Value	Description
15:4	R/W	000h	**Prefetchable Memory Address Limit (PMLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express-G.
3:0	RO	1h	**64-Bit Address Support):** Indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch

20.1.19 PMBASEU1 - Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 28-2Bh
Default Value: 0000000Fh
Access: R/W
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation.
This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
31:4	R/W	0000000h	**Reserved (MBASEU1):** These registers are R/W for compliance purposes only. They should never be programmed to anything other than zeros.
3:0	R/W	Fh	**Prefetchable Memory Base Address (MBASEU):** Corresponds to A[35:32] of the lower limit of the prefetchable memory range that will be passed to PCI Express-G.

20.1.20 PMLIMITU1 - Prefetchable Memory Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	2C-2Fh
Default Value:	00000000h
Access:	R/W
Size:	32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40- bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh.

Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Bit	Access	Default Value	Description
31:4	R/W	0000000h	**Reserved (MLIMITU1):** These registers are R/W for compliance purposes only. They should never be programmed to anything other than zeros.
3:0	R/W	0h	**Prefetchable Memory Address Limit (MLIMITU):** Corresponds to A[35:32] of the upper limit of the prefetchable Memory range that will be passed to PCI Express-G.

20.1.21 CAPPTR1 - Capabilities Pointer

B/D/F/Type: 0/1/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access	Default Value	Description
7:0	RO	88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

20.1.22 INTRLINE1 - Interrupt Line

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access	Default Value	Description
7:0	R/W	00h	**Interrupt Connection (INTCON):** Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected.

20.1.23 INTRPIN1 - Interrupt Pin

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access	Default Value	Description
7:0	RO	01h	**Interrupt Pin (INTPIN):** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

20.1.24 BCTRL1 - Bridge Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 3E-3Fh
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express-G) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within (G)MCH, e.g., VGA compatible address ranges mapping.

Bit	Access	Default Value	Description
15:12	RO	0h	**Reserved**
11	RO	0b	**Discard Timer SERR Enable (DTSERRE):** Not Applicable or Implemented. Hardwired to 0.
10	RO	0b	**Discard Timer Status (DTSTS):** Not Applicable or Implemented. Hardwired to 0.
9	RO	0b	**Secondary Discard Timer (SDT):** Not Applicable or Implemented. Hardwired to 0.
8	RO	0b	**Primary Discard Timer (PDT):** Not Applicable or Implemented. Hardwired to 0.
7	RO	0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	R/W	0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.

Bit	Access	Default Value	Description
5	RO	0b	**Master Abort Mode (MAMODE):** When acting as a master, unclaimed reads that experience a master abort returns all 1's and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4	R/W	0b	**VGA 16-bit Decode (VGA16D):** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0: Execute 10-bit address decodes on VGA I/O accesses 1: Execute 16-bit address decodes on VGA I/O accesses.
3	R/W	0b	**VGA Enable (VGAEN):** Controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in Device 0, offset 97h[0].
2	R/W	0b	**ISA Enable (ISAEN):** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the (G)MCH to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0: All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to PCI Express-G. 1: (G)MCH will not forward to PCI Express-G any I/O transactions addressing the last 768 bytes in each 1-KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express-G these cycles will be forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W	0b	**SERR Enable (SERREN):** 0: No forwarding of error messages from secondary side to primary side that could result in an SERR. 1: ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	R/W	0b	**Parity Error Response Enable (PEREN):** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the (G)MCH receives across the link (upstream) a Read Data Completion Poisoned TLP 0: Master Data Parity Error bit in Secondary Status register **cannot** be set. 1: Master Data Parity Error bit in Secondary Status register **can** be set.

20.1.25 PM_CAPID1 - Power Management Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 80-83h
Default Value: C8039001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:27	RO	19h	**PME Support (PMES):** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot and D3cold. This device is not required to do anything to support D3hot and D3cold, it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO	0b	**D2 Power State Support (D2PSS):** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO	0b	**D1 Power State Support (D1PSS):** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO	000b	**Auxiliary Current (AUXC):** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO	0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is **not** required before generic class device driver is to use it.
20	RO	0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO	0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO	011b	**PCI PM CAP Version (PCIPMCV):** Version: - A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	RO	90h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO	01h	**Capability ID (CID):** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

20.1.26 PM_CS1 - Power Management Control/Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 84-87h
Default Value: 00000000h
Access: RO; R/W/S; R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved** Not Applicable or Implemented. Hardwired to 0.
15	RO	0b	**PME Status (PMESTS):** Indicates that this device does not support PMEB generation from D3cold.
14:13	RO	00b	**Data Scale (DSCALE):** Indicates that this device does not support the power management data register.
12:9	RO	0h	**Data Select (DSEL):** Indicates that this device does not support the power management data register.
8	R/W/S	0b	**PME Enable (PMEE):** Indicates that this device does not generate PMEB assertion from any D-state. 0: PMEB generation not possible from any D State 1: PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2	RO	00h	**Reserved**

Bit	Access	Default Value	Description
1:0	R/W	00b	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of type 0 config cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the (G)MCH logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

20.1.27 SS_CAPID - Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 88-8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:8	RO	80h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO	0Dh	**Capability ID (CID):** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

20.1.28 SS - Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 8C-8Fh
Default Value: 00008086h
Access: R/WO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Bit	Access	Default Value	Description
31:16	R/WO	0000h	**Subsystem ID (SSID):** Identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO	8086h	**Subsystem Vendor ID (SSVID):** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

20.1.29 MSI_CAPID - Message Signaled Interrupts Capability ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 90-91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case walking this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Bit	Access	Default Value	Description
15:8	RO	A0h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO	05h	**Capability ID (CID):** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

20.1.30 MC - Message Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 92-93h
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	0b	**64-Bit Address Capable (64AC):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32-bit/4-GB limit.
6:4	R/W	000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. Value: Number of Messages Requested 000: 1 All of the following are reserved in this implementation: 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
0	R/W	0b	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs. 0: MSI will not be generated. 1: MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

20.1.31 MA - Message Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 94-97h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:2	R/W	00000000h	**Message Address (MA):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	**Force Dword Align (FDWA):** Hardwired to 0 so that addresses assigned by system software are always aligned on a Dword address boundary.

20.1.32 MD - Message Data

B/D/F/Type: 0/1/0/PCI
Address Offset: 98-99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	**Message Data (MD):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

20.1.33 PEG_CAPL - PCI Express-G Capability List

B/D/F/Type: 0/1/0/PCI
Address Offset: A0-A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access	Default Value	Description
15:8	RO	00h	**Pointer to Next Capability (PNC):** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO	10h	**Capability ID (CID):** Identifies this linked list item (capability structure) as being for PCI Express registers.

20.1.34 PEG_CAP - PCI Express-G Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A2-A3h
Default Value: 0141h
Access: RO; R/WO
Size: 16 bits

This register indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
15:14	RO	00b	**Reserved**
13:9	RO	00h	**Interrupt Message Number (IMN):** Not Applicable or Implemented. Hardwired to 0.
8	R/WO	1b	**Slot Implemented (SI):** 0: The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1: The PCI Express Link associated with this port is connected to a slot. BIOS Requirement: This field must be initialized appropriately if a slot connection is not implemented.
7:4	RO	4h	**Device/Port Type (DPT):** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO	1h	**PCI Express Capability Version (PCIECV):** Hardwired to 1 as it is the first version.

20.1.35 DCAP - Device Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A4-A7h
Default Value: 00008000h
Access: RO
Size: 32 bits

This register indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
31: 6	RO	0000h	**Reserved**
5	RO	0b	**Extended Tag Field Supported (ETFS):** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Not Applicable or Implemented. Hardwired to 0.
2:0	RO	000b	**Max Payload Size (MPS):** Hardwired to indicate 128-B max supported payload for Transaction Layer Packets (TLP).

20.1.36 DCTL - Device Control

B/D/F/Type: 0/1/0/PCI
Address Offset: A8-A9h
Default Value: 0000h
Access: RO; R/W;
Size: 16 bits

Provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access	Default Value	Description
15:12	RO	0h	**Reserved**
11	RO	0b	**Reserved**
10:8	RO	000b	**Reserved**
7:5	R/W	000b	**Max Payload Size (MPS):** 000: 128-B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO	0b	**Reserved**
3	R/W	0b	**Unsupported Request Reporting Enable (URRE):** When set, Unsupported Requests will be reported. Note that reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W	0b	**Fatal Error Reporting Enable (FERE):** When set fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W	0b	**Non-Fatal Error Reporting Enable (NFERE):** When set non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W	0b	**Correctable Error Reporting Enable (CERE):** When set correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

20.1.37 DSTS - Device Status

B/D/F/Type: 0/1/0/PCI
Address Offset: AA-ABh
Default Value: 0000h
Access: RO; R/WC
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access	Default Value	Description
15:6	RO	000h	**Reserved**
5	RO	0b	**Transactions Pending (TP):** 0: All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1: Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO	0b	**Reserved**
3	R/WC	0b	**Unsupported Request Detected (URD):** When set this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.
2	R/WC	0b	**Fatal Error Detected (FED):** When set this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	R/WC	0b	**Non-Fatal Error Detected (NFED):** When set this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.

Bit	Access	Default Value	Description
0	R/WC	0b	**Correctable Error Detected (CED):** When set this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

20.1.38 LCAP - Link Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: AC-AFh
Default Value: 02014D01h
Access: RO; R/WO
Size: 32 bits

This register indicates PCI Express device specific capabilities.

Bit	Access	Default Value	Description
31:24	RO	02h	**Port Number (PN):** Indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description [31:24].
23:18	RO	000b	**Reserved**
17:15	R/WO	010b	**L1 Exit Latency (L1ELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs BIOS Requirement: If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RO	100b	**L0s Exit Latency (L0SELAT):** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 µs 101: 1 µs to less than 2 µs 110: 2 µs - 4 µs 111: More than 4 µs The actual value of this field depends on the common Clock Configuration bit (LCTL[6]).

Bit	Access	Default Value	Description
11:10	R/WO	11b	**Active State Link PM Support (ASLPMS)**
9:4	RO	10h	**Max Link Width (MLW):** Indicates the maximum number of lanes supported for this link.
3:0	RO	1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

20.1.39 LCTL - Link Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B0-B1h
Default Value: 0040h
Access: RO; R/W;
Size: 16 bits

This register allows control of PCI Express Link.

Bit	Access	Default Value	Description
15:9	RO	0000000b	**Reserved**
8	RO	0b	**Enable Clock Power Management (ECPM):** Applicable only for form factors that support a "Clock Request" (CLKREQ#) mechanism, this enable functions as follows 0b: Clock power management is disabled and device must hold CLKREQ# signal low (Default). 1b: When this bit is set to 1 the device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification. Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.
7	R/W	0b	**Extended Synch (ES):** 0: Standard Fast Training Sequence (FTS). 1: Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	R/W	1b	**Common Clock Configuration (CCC):** 0: Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1: Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training.
5	R/W	0b	**Retrain Link (RL):** 0: Normal operation. 1: Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).

Bit	Access	Default Value	Description
4	R/W	0b	**Link Disable (LD):** 0: Normal operation 1: Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO	0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2	R/W	0b	**Far-End Digital Loopback (FEDLB):**
1:0	R/W	00b	**Active State PM (ASPM):** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Entry Supported

20.1.40 LSTS - Link Status

B/D/F/Type: 0/1/0/PCI
Address Offset: B2-B3h
Default Value: 1001h
Access: RO
Size: 16 bits

Indicates PCI Express Link status.

Bit	Access	Default Value	Description
15:13	RO	00b	**Reserved**
12	RO	1b	**Slot Clock Configuration (SCC):** 0: The device uses an independent clock irrespective of the presence of a reference on the connector. 1: The device uses the same physical reference clock that the platform provides on the connector.
11	RO	0b	**Link Training (LTRN):** Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO	0b	**Reserved**
9:4	RO	00h	**Negotiated Width (NW):** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed) 00h: Reserved 01h: X1 02h: X2 04h: X4 08h: X8 10h: X16 All other encodings are reserved.
3:0	RO	1h	**Negotiated Speed (NS):** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are reserved.

20.1.41 SLOTCAP - Slot Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: B4-B7h
Default Value: 00040000h
Access: R/WO; RO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description
31:19	R/WO	0000h	**Physical Slot Number (PSN):** Indicates the physical slot number attached to this Port. BIOS Requirement: This field must be initialized by BIOS to a value that assigns a slots number that is globally unique within the chassis.
18	R/WO	1b	**No Command Completed Support (NCCS):** When set to 1b, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set to 1b if the hotplug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
17	RO	0b	**Reserved**
16:15	R/WO	00b	**Slot Power Limit Scale (SPLS):** Specifies the scale used for the Slot Power Limit Value. 00: 1.0x 01: 0.1x 10: 0.01x 11: 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO	00h	**Slot Power Limit Value (SPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	RO	0b	**Reserved for Hot-plug Capable (HPC):** Indicates that this slot is capable of supporting hot-lug operations.
5	RO	0b	**Reserved for Hot-plug Surprise (HPS):** Indicates that a device in this slot might be removed from the system without any prior notification.

Bit	Access	Default Value	Description
4	RO	0b	**Power Indicator Present (PIP):** Indicates that a Power Indicator is electrically controlled by the chassis for this slot.
3	RO	0b	**Attention Indicator Present (AIP):** Indicates that an Attention Indicator is implemented on the chassis for this slot
2	RO	0b	**Reserved**
1	RO	0b	**Reserved**
0	RO	0b	**Reserved for Attention Button Present (ABP):** Indicates that an Attention Indicator is implemented on the chassis for this slot

20.1.42 SLOTCTL - Slot Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B8-B9h
Default Value: 01C0h
Access: RO; R/W
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description
15:10	RO	000b	**Reserved**
9:8	RO	01b	**Power Indicator Control (PIC):** Reads to this field reflects the state of current power indicator. Writes to this field set the Power indicator and cause the port to send the appropriate Power_Indicator _* messages 00: Reserved 01: On 10: Blink 11: Off
7:6	RO	11b	**Reserved for Attention Indicator Control (AIC):** Reads to this field reflects the state of current power indicator. Writes to this field set the Power indicator and cause the port to send the appropriate Power_Indicator _* messages 00: Reserved 01: On 10: Blink 11: Off
5	RO	0b	**Reserved for Hot-plug Interrupt Enable (HPIE):** When set , this bit enables generation of an interrupt on enabled hot-plug events
4	RO	0b	**Command Completed Interrupt Enable (CCI):** When set enables software notification when a hot-plug command is completed by the Hot-Plug Controller.
3	R/W	0b	**Presence Detect Changed Enable (PDCE):** When set to 1b, this bit enables software notification on a presence detect changed event.
2	RO	0b	**Reserved**
1	RO	0b	**Reserved**
0	RO	0b	**Attention Button Pressed Enable (ABPE):** When set enables software notification on an attention button pressed event.

20.1.43 SLOTSTS - Slot Status

B/D/F/Type: 0/1/0/PCI
Address Offset: BA-BBh
Default Value: 0000h
Access: RO; R/WC
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description
15:7	RO	000h	**Reserved**
6	RO	0b	**Presence Detect State (PDS):** Indicates the presence of an adapter in the slot, 0b Slot Empty 1b Card Present in slot
5	RO	0b	**Reserved**
4	RO	0b	**Reserved**
3	R/WC	0b	**Presence Detect Changed (PDC):** This bit is set when the value reported in Presence Detect State is changed.
2	RO	0b	**Reserved**
1	RO	0b	**Reserved for Power Fault Detected (PFD):** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. **Note** that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
0	RO	0b	**Reserved**

20.1.44 RCTL - Root Control

B/D/F/Type: 0/1/0/PCI
Address Offset: BC-BDh
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access	Default Value	Description
15:4	RO	000h	**Reserved**
3	R/W	0b	**PME Interrupt Enable (PMEIE):** 0: No interrupts are generated as a result of receiving PME messages. 1: Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W	0b	**System Error on Fatal Error Enable (SEFEE):** Controls the Root Complex's response to fatal errors. 0: No SERR generated on receipt of fatal error. 1: Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W	0b	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):** Controls the Root Complex's response to non-fatal errors. 0: No SERR generated on receipt of non-fatal error. 1: Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W	0b	**System Error on Correctable Error Enable (SECEE):** Controls the Root Complex's response to correctable errors. 0: No SERR generated on receipt of correctable error. 1: Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

20.1.45 RSTS - Root Status

B/D/F/Type: 0/1/0/PCI
Address Offset: C0-C3h
Default Value: 00000000h
Access: RO; R/WC
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access	Default Value	Description
31:18	RO	0000h	**Reserved**
17	RO	0b	**PME Pending (PMEP):** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/WC	0b	**PME Status (PMES):** Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO	0000h	**PME Requestor ID (PMERID):** Indicates the PCI requestor ID of the last PME requestor.

20.1.46 PEGLC - PCI Express-G Legacy Control

B/D/F/Type: 0/1/0/PCI
Address Offset: EC-EFh
Default Value: 00000000h
Access: RO; R/W
Size: 32 bits

Controls functionality that is needed by legacy (non-PCI Express aware) OS's during run time.

Bit	Access	Default Value	Description
31:3	RO	00000000h	**Reserved**
2	R/W	0b	**PME GPE Enable (PMEGPE):** 0: Do not generate GPE PME message when PME is received. 1: Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the (G)MCH to support PMEs on the PEG port under legacy operating systems.
1	R/W	0b	**Hot-Plug GPE Enable (HPGPE):** 0: Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1: Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the (G)MCH to support Hot-Plug on the PEG port under legacy operating systems.
0	R/W	0b	**General Message GPE Enable (GENGPE):** 0: Do not forward received GPE assert/deassert messages 1: Forward received GPE assert/deassert messages. These general GPE message can be received via the PEG port from an external Intel device (i.e., PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, PxH might send this message if a PCI Express device is hot plugged into a PxH downstream port.

20.2 PEG Device 1 Function 0 Extended Configuration Registers

Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definition than standard PCI capability structures.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Virtual Channel Enhanced Capability Header	VCECH	100	103	14010002h	RO
Port VC Capability Register 1	PVCCAP1	104	107	00000000h	RO
Port VC Capability Register 2	PVCCAP2	108	10B	00000001h	RO
Port VC Control	PVCCTL	10C	10D	0000h	RO; R/W
Reserved		10E	10F		
VC0 Resource Capability	VC0RCAP	110	113	00000000h	RO
VC0 Resource Control	VC0RCTL	114	117	800000FFh	RO; R/W
Reserved		118	119		
VC0 Resource Status	VC0RSTS	11A	11B	0002h	RO
VC1 Resource Capability	VC1RCAP	11C	11F	00000000h	RO
VC1 Resource Control	VC1RCTL	120	123	00000000h	RO
Reserved		124	125		
VC1 Resource Status	VC1RSTS	126	127	0000h	RO
Reserved		128	13F		
Root Complex Link Declaration Enhanced	RCLDECH	140	143	00010005h	RO
Element Self Description	ESD	144	147	02000100h	RO; R/WO
Reserved		148	14F		
Link Entry 1 Description	LE1D	150	153	00000000h	RO; R/WO
Reserved		154	157		

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Link Entry 1 Address	LE1A	158	15F	0000000000000000h	RO; R/WO

20.2.1 VCECH - Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/1/0/MM
Address Offset: 100-103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access	Default Value	Description
31:20	RO	140h	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

20.2.2 PVCCAP1 - Port VC Capability Register 1

B/D/F/Type: 0/1/0/MM
Address Offset: 104-107h
Default Value: 00000000h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	**Reserved**
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	**Reserved**
2:0	RO	000b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

20.2.3 PVCCAP2 - Port VC Capability Register 2

B/D/F/Type: 0/1/0/MM
Address Offset: 108-10Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8	RO	0000h	**Reserved**
7:0	RO	01h	**VC Arbitration Capability (VCAC):** Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority. VC0 is the lowest priority.

20.2.4 PVCCTL - Port VC Control

B/D/F/Type: 0/1/0/MM
Address Offset: 10C-10Dh
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	**Reserved**
3:1	R/W	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 001b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0	RO	0b	**Reserved**

20.2.5 VC0RCAP - VC0 Resource Capability

B/D/F/Type: 0/1/0/MM
Address Offset: 110-113h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	00h	**Reserved**
15	RO	0b	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0	RO	0000h	**Reserved**

20.2.6 VC0RCTL - VC0 Resource Control

B/D/F/Type: 0/1/0/MM
Address Offset: 114-117h
Default Value: 800000FFh
Access: RO; R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**VC0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	**Reserved**
26:24	RO	000b	**VC0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8	RO	0000h	**Reserved**
7:1	R/W	7Fh	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

20.2.7 VC0RSTS - VC0 Resource Status

B/D/F/Type: 0/1/0/MM
Address Offset: 11A-11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	**Reserved**
1	RO	1b	**VC0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	**Reserved**

20.2.8 VC1RCAP - VC1 Resource Capability

B/D/F/Type: 0/1/0/MM
Address Offset: 11C-11Fh
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00000000h	**Reserved**

20.2.9 VC1RCTL - VC1 Resource Control

B/D/F/Type: 0/1/0/MM
Address Offset: 120-123h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00000000h	**Reserved**

20.2.10 VC1RSTS - VC1 Resource Status

B/D/F/Type: 0/1/0/MM
Address Offset: 126-127h
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	**Reserved**

20.2.11 RCLDECH - Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MM
Address Offset: 140-143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PEG) to other elements of the root complex component to which it belongs. See PCI Express specification for link/topology declaration requirements.

Bit	Access	Default Value	Description
31:20	RO	000h	**Pointer to Next Capability (PNC):** This is the last capability in the PCI Express extended capabilities list
19:16	RO	1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO	0005h	**Extended Capability ID (ECID):** Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability. See corresponding Egress Port Link Declaration Capability registers for diagram of Link Declaration Topology.

20.2.12 ESD - Element Self Description

B/D/F/Type: 0/1/0/MM
Address Offset: 144-147h
Default Value: 02000100h
Access: RO; R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	02h	**Port Number (PN):** Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO	00h	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:8	RO	01h	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO	0h	**Reserved**
3:0	RO	0h	**Element Type (ET):** Indicates the type of the Root Complex Element. Value of 0 h represents a root port.

20.2.13 LE1D - Link Entry 1 Description

B/D/F/Type: 0/1/0/MM
Address Offset: 150-153h
Default Value: 00000000h
Access: RO; R/WO
Size: 32 bits

This register is the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).
15:2	RO	0000h	**Reserved**
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

20.2.14 LE1A - Link Entry 1 Address

B/D/F/Type: 0/1/0/MM
Address Offset: 158-15Fh
Default Value: 0000000000000000h
Access: RO; R/WO
Size: 64 bits

This register is the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	**Reserved**
31:12	R/WO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	**Reserved**

§

21 Internal Graphics Device 2 Configuration Register (D2:F0-F1)

Device 2 contains registers for the internal graphics functions. The table below lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not, this selected through bit 1 of GGC register (Device 0, offset 52h).

The following sections describe Device 2 PCI configuration registers only.

21.1 Internal Graphics Device 2 Configuration Register Details (D2:F0)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO
Device Identification	DID2	2	3	2A02h[1] 2A12h[2]	RO
PCI Command	PCICMD2	4	5	0000h	RO; R/W
PCI Status	PCISTS2	6	7	0090h	RO
Revision Identification	RID2	8	8	00h	RO
Class Code	CC	9	B	030000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT2	D	D	00h	RO
Header Type	HDR2	E	E	80h	RO
Reserved		F	F		
Graphics Translation Table Range Address	GTTMMADR	10	17	0000000000000004h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Graphics Memory Range Address	GMADR	18	1F	00000000000 0000Ch	R/W; RO; R/W/L
I/O Base Address	IOBAR	20	23	00000001h	RO; R/W
Reserved		24	2B		
Subsystem Vendor Identification	SVID2	2C	2D	0000h	R/WO
Subsystem Identification	SID2	2E	2F	0000h	R/WO
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO
Capabilities Pointer	CAPPOINT	34	34	90h	RO
Reserved		25	3B		
Interrupt Line	INTRLINE	3C	3C	00h	R/W
Interrupt Pin	INTRPIN	3D	3D	01h	RO
Minimum Grant	MINGNT	3E	3E	00h	RO
Maximum Latency	MAXLAT	3F	3F	00h	RO
Reserved		40	43		
Capabilities Pointer (to Mirror of Dev0 CAPID)	MCAPPTR	44	44	48h	RO
Reserved		45	51		
Mirror of Dev0 (G)MCH Graphics Control	MGGC	52	53	0030h	RO
Mirror of Dev0 DEVEN	MDEVENdev0 F0	54	57	0000001Bh	RO
Reserved		58	5B		
Base of Stolen Memory	BSM	5C	63	00000000000 00000h	RO
Reserved		64	65		
Multi Size Aperture Control	MSAC	66	66	02h	RO; R/W; R/W/L

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		67	8F		
Message Signaled Interrupts Capability ID	MSI_CAPID	90	91	D005h	RO
Message Control	MC	92	93	0000h	RO; R/W
Message Address	MA	94	97	00000000h	R/W; RO
Message Data	MD	98	99	0000h	R/W
Reserved		9A	BF		
Graphics Debug Reset	GDRST	C0	C0	00h	R/W; RO
Reserved		C1	CF		
Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RO
Power Management Capabilities	PMCAP	D2	D3	0023h	RO
Power Management Control/Status	PMCS	D4	D5	0000h	RO; R/W
Reserved		D6	E3		
System Display Event Register	ASLE	E4	E7	00000000h	R/W
Reserved		E8	F0		
Graphics Clock Frequency and Gating Control	GCFGC	F0	F1	0201h	R/W; RO
Reserved		F2	F3		
Legacy Backlight Brightness	LBB	F4	F7	00000000h	R/W
Reserved		F8	FB		
ASL Storage	ASLS	FC	FF	00000000h	R/W

NOTES:

1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

21.1.1 VID2 - Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

21.1.2 DID2 - Device Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2-3h
Default Value: 2A02h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	2A02h[1] 2A12h[2]	**Device Identification Number (DID):** Identifier assigned to the (G)MCH core/primary PCI device.

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

21.1.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/0/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	R/W	0b	**Interrupt Disable:** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO	0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO	0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO	0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W	0b	**Bus Master Enable (BME):** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.

Bit	Access	Default Value	Description
1	R/W	0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	R/W	0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

21.1.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/0/PCI
Address Offset: 6-7h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to 00.
8	RO	0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.

Bit	Access	Default Value	Description
7	RO	1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO	0b	**66-MHz PCI Capable (66C):** N/A - Hardwired to 0.
4	RO	1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	**Interrupt Status:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2:0	RO	000b	**Reserved**

21.1.5 RID2 - Revision Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1.

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch.

21.1.6 CC - Class Code

B/D/F/Type: 0/2/0/PCI
Address Offset: 9-Bh
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	Description
23:16	RO	03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO	00h	**Sub-Class Code (SUBCC):** Based on Device 0 GGC-GMS bits and GGC-IVD bits. 00h: VGA compatible 80h: Non VGA (GMS = "000" or IVD = 1)
7:0	RO	00h	**Programming Interface (PI):** 00h: Hardwired as a Display controller.

21.1.7 CLS - Cache Line Size

B/D/F/Type: 0/2/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** This field is hardwired to 0's. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

21.1.8 MLT2 - Master Latency Timer

B/D/F/Type: 0/2/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer Count Value**

21.1.9 HDR2 - Header Type

B/D/F/Type: 0/2/0/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	Description
7	RO	1b	**Multi Function Status (MFunc):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the Mfunc bit is also set.
6:0	RO	00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

21.1.10 GTTMMADR - Graphics Translation Table Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 10-17h
Default Value: 0000000000000004h
Access: RO; R/W
Size: 64 bits

The base address of Global GTT is located in the Memory Base Address + 512 KB

The allocation is for 1024 KB and the base address is defined by bits [35:20].

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:20	R/W	0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [35:20]. 1 MB combined for MMIO and Global GTT table aperture (512K each).
19:4	RO	0000h	**Reserved**
3	RO	0b	**Prefetchable Memory**
2	RO	1b	**Memory Type:** 0 : To indicate 32-bit base address 1 : To indicate 64-bit base address
1	RO	0b	**Reserved**
0	RO	0b	**Memory / IO Space**

21.1.11 GMADR - Graphics Memory Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 18-1Fh
Default Value: 000000000000000Ch
Access: R/W; RO; R/W/L
Size: 64 bits

IGD graphics memory base address is specified in this register.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:29	R/W	00h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [35:29].
28	R/W/L	0b	**Reserved**
27	R/W/L	0b	**256-MB Address Mask:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Dev 2, Func 0, offset 66h) for details.
26:4	RO	000000h	**Reserved**
3	RO	1b	**Prefetchable Memory:** Hardwired to 1 to enable prefetching.
2	RO	1b	**Memory Type:** 0 : To indicate 32-bit base address 1 : To indicate 64-bit base address
1	RO	0b	**Reserved**
0	RO	0b	**Memory/IO Space:** Hardwired to 0 to indicate memory space.

21.1.12 IOBAR - I/O Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 20-23h
Default Value: 00000001h
Access: RO; R/W
Size: 32 bits

This register provides the Base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

If accesses to this IO bar is allowed then the (G)MCH claims all 8-, 16- or 32- bit IO cycles from the CPU that falls within the 8B claimed.

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:3	R/W	0000h	**IO Base Address:** Set by the OS, these bits correspond to address signals [15:3].
2:1	RO	00b	**Memory Type:** Hardwired to 0's to indicate 32-bit address.
0	RO	1b	**Memory / IO Space:** Hardwired to 1 to indicate IO space.

21.1.13 SVID2 - Subsystem Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2C-2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.

21.1.14 SID2 - Subsystem Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2E-2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

21.1.15 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 30-33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Access	Default Value	Description
31:18	RO	0000h	**ROM Base Address:** Hardwired to 0's.
17:11	RO	00h	**Address Mask:** Hardwired to 0's to indicate 256-KB address range.
10:1	RO	000h	**Reserved** Hardwired to 0's.
0	RO	0b	**ROM BIOS Enable:** 0 = ROM not accessible.

21.1.16 CAPPOINT - Capabilities Pointer

B/D/F/Type: 0/2/0/PCI
Address Offset: 34h
Default Value: 90h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	90h	**Capabilities Pointer Value:** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List which is the MSI Capabilities ID register at address 90h or the Power Management Capabilities ID registers at address D0h.The value is determined by CAPL[0].

21.1.17 INTRLINE - Interrupt Line

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access	Default Value	Description
7:0	R/W	00h	**Interrupt Connection:** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

21.1.18 INTRPIN - Interrupt Pin

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	01h	**Interrupt Pin:** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h: INTA#.

21.1.19 MINGNT - Minimum Grant

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Minimum Grant Value:** The IGD does not burst as a PCI compliant master.

21.1.20 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

21.1.21 MCAPPTR - Capabilities Pointer (to Mirror of Dev0 CAPID)

B/D/F/Type: 0/2/0/PCI
Address Offset: 44h
Default Value: 48h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	48h	**Capabilities Pointer Value:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

21.1.22 MGGC - Mirror of Dev0 (G)MCH Graphics Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 52-53h
Default Value: 0030h
Access: RO
Size: 16 bits

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Bit	Access	Default Value	Description
15:7	RO	000000000b	**Reserved**
6:4	RO	011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Stolen Memory Bases is located between (TOLUD - SMSize) to TOUD. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0. Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. 101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. 110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. 111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. **NOTE:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.
3:2	RO	00b	**Reserved**
1	RO	0b	**IGD VGA Disable (IVD):** 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80. 0: Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.
0	RO	0b	**Reserved**

21.1.23 MDEVENdev0F0 - Mirror of Dev0 DEVEN

B/D/F/Type: 0/2/0/PCI
Address Offset: 54-57h
Default Value: 0000001Bh
Access: RO
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the (G)MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	Description
31:8	RO	000000h	**Reserved**
7	RO	0b	**Reserved**
6:5	RO	00b	**Reserved**
4	RO	1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden. 1: Bus 0 Device 2 Function 1 is enabled and visible. If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.
3	RO	1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden. 1: Bus 0 Device 2 Function 0 is enabled and visible. If this (G)MCH does not have internal graphics capability (CAPID0[33] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2	RO	0b	**Reserved**
1	RO	1b	**PCI Express Graphics Port Enable. (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden. Also gates PCI Express internal clock (lgclk) and asserts PCI Express internal reset (lgrstB). 1: Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities (CAPID0[37] and CAPID0[35]), SDVO presence HW strap and SDVO/PCIe concurrent HW strap.
0	RO	1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

21.1.24 BSM - Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI
Address Offset: 5C-63h
Default Value: 0000000000000000h
Access: RO
Size: 64 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, (G)MCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

Bit	Access	Default Value	Description
63:36	RO	0000000h	**Reserved**
35:32	RO	0h	**Base of Stolen Memory:**
31:20	RO	000h	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO	00000h	**Reserved**

21.1.25 MSAC - Multi Size Aperture Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 66h
Default Value: 02h
Access: RO; R/W; R/W/L
Size: 8 bits

This register determines the size of the graphics memory aperture in Function 0 and only in the untrusted space. By default the aperture size is 256 MB. Only the system BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Bit	Access	Default Value	Description
7:4	R/W	0h	**Scratch Bits Only:**
3	RO	0b	**Reserved**
2:1	R/W/L	01b	**Untrusted Aperture Size (LHSAS):** 11: bits [28:27] of GMADR register are made Read only and forced to zero, allowing only 512 MB of GMADR 01 : Illegal programming 00 : Illegal programming 10 : Illegal programming.
0	RO	0b	**Reserved**

21.1.26 MSI_CAPID - Message Signaled Interrupts Capability ID

B/D/F/Type: 0/2/0/PCI
Address Offset: 90-91h
Default Value: D005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address. The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0[@ 7Fh). In that case walking this linked list will skip this capability and instead go directly to the PCI PM capability.

Bit	Access	Default Value	Description
15:8	RO	D0h	**Pointer to Next Capability:** This contains a pointer to the next item in the capabilities list which is the Power Management Capability.
7:0	RO	05h	**Capability ID:** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

21.1.27 MC - Message Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 92-93h
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	0b	**64-bit Address Capable:** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32-bit/4-GB limit.
6:4	R/W	000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. Value: Number of Messages Requested. 000: 1 All of the following are reserved in this implementation: 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
0	R/W	0b	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs.

21.1.28 MA - Message Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 94-97h
Default Value: 00000000h
Access: R/W; RO
Size: 32 bits

A read from this register produces undefined results.

Bit	Access	Default Value	Description
31:2	R/W	00000000h	**Message Address:** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	**Force Dword Align:** Hardwired to 0 so that addresses assigned by system software are always aligned on a Dword address boundary.

21.1.29 MD - Message Data

B/D/F/Type: 0/2/0/PCI
Address Offset: 98-99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	**Message Data:** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

21.1.30 GDRST - Graphics Debug Reset

B/D/F/Type: 0/2/0/PCI
Address Offset: C0h
Default Value: 00h
Access: R/W; RO
Size: 8 bits

Bit	Access	Default Value	Description
7:2	RO	00b	**Reserved**
1	RO	0b	**Graphics Reset Status:** 0: Graphics subsystem not in Reset. 1: Graphics Subsystem in Reset as a result of Graphics Debug Reset. This bit gets is set to a 1 and the Graphics hardware has completed the debug reset sequence and all Graphics assets are in reset. This bit is cleared when Graphics Debug Reset bit is set to a 0.
0	R/W	0b	**Graphics Debug Reset:** 0: Deassert display and render domain reset 1: Assert display and render domain reset Render and Display clock domain resets should be asserted for at least 20 µs. Once this bit is set to a 1 all GFX core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state, Display and overlay engines are halted (garbage on screen). VGA memory is not available, Store Dwords, interrupts are not ensured to be completed. Device 2 IO registers are not available. Device 2 Config registers are available when Graphics debug reset is asserted.

21.1.31 PMCAPID - Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI
Address Offset: D0-D1h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**NEXT_PTR:** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO	01h	**CAP_ID :** SIG defines this ID is 01h for power management.

21.1.32 PMCAP - Power Management Capabilities

B/D/F/Type: 0/2/0/PCI
Address Offset: D2-D3h
Default Value: 0023h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	**D2:** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	**Reserved**
5	RO	1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	**Auxiliary Power Source:** Hardwired to 0.
3	RO	0b	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.

Bit	Access	Default Value	Description
2:0	RO	011b	**Version:** A value of 011b indicates that this function complies with revision 1.2 of the *PCI Power Management Interface Specification*

21.1.33 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/0/PCI
Address Offset: D4-D5h
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO	00b	**Reserved**
12:9	RO	0h	**Reserved**
8	RO	0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO	00h	**Reserved**
1:0	R/W	00b	**Power State:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Bits[1:0] Power state 00 D0 Default 01 D1 Not Supported 10 D2 Not Supported 11 D3

21.1.34 ASLE - System Display Event Register

B/D/F/Type: 0/2/0/PCI
Address Offset: E4-E7h
Default Value: 00000000h
Access: R/W
Size: 32 bits

The exact use of these bytes including whether they are addressed as bytes, words, or as a Dword, is not pre-determined but subject to change by driver and System BIOS teams (acting in unison).

Bit	Access	Default Value	Description
31:24	R/W	00h	**ASLE Scratch Trigger3:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W	00h	**ASLE Scratch Trigger2**: When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W	00h	**ASLE Scratch Trigger 1:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W	00h	**ASLE Scratch Trigger 0:** When written, this scratch byte triggers an interrupt when IEF bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

21.1.35 GCFGC - Graphics Clock Frequency and Gating Control

B/D/F/Type: 0/2/0/PCI
Address Offset: F0-F1h
Default Value: 0201h
Access: R/W; RO
Size: 16 bits

Bit	Access	Default Value	Description
15	R/W	0b	**Reserved**
14	R/W	0b	Gate Core Display Clock (GCRC) (GCRC): Gate Core Display Clock (GCRC): 0: cdclk is running1:cdclk is gated
13	R/W	0b	Reserved (RSVD):
12:8	R/W	00010b	**Graphics Core Display Clock Select**: Software programs this register. 00010 => 320/333 MHz Others => Reserved
7	RO	0b	**Reserved**
6:5	R/W	00b	**Reserved**.
4	R/W	0b	**Gate Core Render and Sampler Clock (GateCRCLK):** Gate Core Render and Sampler Clock (GCRC): 0: crclk, crb2clk and csclk are running 1: crclk, crb2clk and csclk are gated
3:0	R/W	0001b	**Graphics Core Render Clock Select (CRCLKFREQ):** Software programs this register to set the crclk and csclk frequencies. 0010= ~ 250/267 MHz 0011 = ~ 320/333 MHz 0100 = ~ 400/444 MHz 0101= ~ 500/533 MHz Others = Reserved

21.1.36 LBB - Legacy Backlight Brightness

B/D/F/Type: 0/2/0/PCI
Address Offset: F4-F7h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access	Default Value	Description
31:24	R/W	00h	**LBPC Scratch Trigger3:** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W	00h	**LBPC Scratch Trigger2:** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W	00h	**LBPC Scratch Trigger1:** When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W	00h	**Legacy Backlight Brightness (LBES):** The value of zero is the lowest brightness setting and 255 is the brightest. A write to this register will cause a flag to be set (LBES) in the PIPEBSTATUS register and cause an interrupt if Backlight event in the PIPEBSTATUS register and cause an Interrupt if Backlight Event (LBEE) and Display B Event is enabled by software.

21.1.37 ASLS - ASL Storage

B/D/F/Type: 0/2/0/PCI
Address Offset: FC-FFh
Default Value: 00000000h
Access: R/W;
Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	Description
31:0	R/W	00000000h	RW according to a software controlled usage to support device switching

21.2 Device 2 Function 1 PCI configuration Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO
Device Identification	DID2	2	3	2A03h[1] 2A13h[2]	RO
PCI Command	PCICMD2	4	5	0000h	RO; R/W
PCI Status	PCISTS2	6	7	0090h	RO
Revision Identification	RID2	8	8	00h	RO
Class Code Register	CC	9	B	038000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT2	D	D	00h	RO
Header Type	HDR2	E	E	80h	RO
Reserved		F	F		
Memory Mapped Range Address	MMADR	10	17	0000000000000004h	RO; R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Subsystem Vendor Identification	SVID2	2C	2D	0000h	RO
Subsystem Identification	SID2	2E	2F	0000h	RO
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO
Capabilities Pointer	CAPPOINT	34	34	D0h	RO
Minimum Grant	MINGNT	3E	3E	00h	RO
Maximum Latency	MAXLAT	3F	3F	00h	RO
Mirror of Dev0 Capability Pointer	MCAPPTR	44	44	48h	RO
Reserved		48	51		
Mirror of Dev0 (G)MCH Graphics Control	MGGC	52	53	0030h	RO
Mirror of Dev0 DEVEN	MDEVENdev 0F0	54	57	0000001Bh	RO
Reserved		58	5B		
Base of Stolen Memory	BSM	5C	63	0000000000 000000h	RO
Reserved		64	65		
Multi Size Aperture Control	MSAC	66	66	02h	RO

NOTES:

1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

21.2.1 VID2 - Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 0-1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

21.2.2 DID2 - Device Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2-3h
Default Value: 2A03h
Access: RO
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID's is necessary for allowing distinct Plug and Play enumeration of Function 1 when both Function 0 and Function 1 have the same class code.

Bit	Access	Default Value	Description
15:0	RO	2A03h[1] 2A13h[2]	**Device Identification Number (DID):** This is a 16-bit value assigned to the (G)MCH Graphic device Function 1.

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

21.2.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/1/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	RO	0b	**Reserved**
9	RO	0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO	0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO	0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	**VGA Palette Snoop Enable (VGASNOOP):** This bit is hardwired to 0 to disable snooping.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W	0b	**Bus Master Enable (BME):** Set to 1 to enable the IGD to function as a PCI compliant master. Set to 0 to disable IGD bus mastering.
1	R/W	0b	**Memory Access Enable (MAE):** This bit controls the IGD responds to memory space accesses. 0: Disable. 1: Enable.

Bit	Access	Default Value	Description
0	R/W	0b	**I/O Access Enable (IOAE):** This bit controls the IGD responds to I/O space accesses. 0: Disable. 1: Enable.

21.2.4 PCISTS2 - PCI Status

B/D/F/Type: 0/2/1/PCI
Address Offset: 6-7h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	**Received Target Abort Status (RTAS:** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	**DEVSEL Timing (DEVT):** These bits are hardwired to 00.
8	RO	0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	**User-Defined Format (UDF):** Hardwired to 0.

Bit	Access	Default Value	Description
5	RO	0b	**66-MHz PCI Capable (66C):** Hardwired to 0.
4	RO	1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	**Interrupt Status:** Hardwired to 0.
2:0	RO	0h	**Reserved**

21.2.5 RID2 - Revision Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1.

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch.

21.2.6 CC - Class Code Register

B/D/F/Type: 0/2/1/PCI
Address Offset: 9-Bh
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	Description
23:16	RO	03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO	80h	**Sub-Class Code (SUBCC):** 80h: Non VGA
7:0	RO	00h	**Programming Interface (PI):** 00h: Hardwired as a Display controller.

21.2.7 CLS - Cache Line Size

B/D/F/Type: 0/2/1/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

Note: The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** This field is hardwired to 0's. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

21.2.8 MLT2 - Master Latency Timer

B/D/F/Type: 0/2/1/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Note: The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer Count Value:** Hardwired to 0's.

21.2.9 HDR2 - Header Type

B/D/F/Type: 0/2/1/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	Description
7	RO	1b	**Multi Function Status (MFunc):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the Mfunc bit is also set.
6:0	RO	00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

21.2.10 MMADR - Memory Mapped Range Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 10-17h
Default Value: 0000000000000004h
Access: RO; R/W
Size: 64 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [35:20].

Bit	Access	Default Value	Description
63:36	R/W	0000000h	**Reserved**
35:20	R/W	0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [35:20].
19:4	RO	0000h	**Address Mask:** Hardwired to 0's to indicate 512-KB address range (aligned to 1-M boundary).
3	RO	0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2	RO	1b	**Memory Type:** 0: To indicate 32 bit base address. 1: To indicate 64 bit base address.
1	RO	0b	**Reserved**
0	RO	0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

21.2.11 SVID2 - Subsystem Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2C-2Dh
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

21.2.12 SID2 - Subsystem Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2E-2Fh
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

21.2.13 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 30-33h
Default Value: 00000000h
Access: RO
Size: 32 bits

Note: The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Access	Default Value	Description
31:18	RO	0000h	**ROM Base Address:** Hardwired to 0's.
17:11	RO	00h	**Address Mask:** Hardwired to 0's to indicate 256-KB address range.
10:1	RO	000h	**Reserved:** Hardwired to 0's.
0	RO	0b	**ROM BIOS Enable:** 0 = ROM not accessible.

21.2.14 CAPPOINT - Capabilities Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	D0h	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List which is the Power Management Capabilities ID registers at address D0h.

21.2.15 MINGNT - Minimum Grant

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Minimum Grant Value:** The IGD does not burst as a PCI compliant master.

21.2.16 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

21.2.17 MCAPPTR - Mirror of Dev0 Capability Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 44h
Default Value: 48h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	48h	**Capabilities Pointer Value:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

21.2.18 MGGC - Mirror of Dev0 (G)MCH Graphics Control

B/D/F/Type: 0/2/1/PCI
Address Offset: 52-53h
Default Value: 0030h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:7	RO	000000000b	**Reserved**

Bit	Access	Default Value	Description
6:4	RO	011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Stolen Memory Bases is located between (TOLUD - SMSize) to TOUD. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0. Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. 101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. 110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. 111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.
3:2	RO	00b	**Reserved**
1	RO	0b	**IGD VGA Disable (IVD):** 0: Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80.
0	RO	0b	**Reserved**

21.2.19 MDEVENdev0F0 - Mirror of Dev0 DEVEN

B/D/F/Type: 0/2/1/PCI
Address Offset: 54-57h
Default Value: 0000001Bh
Access: RO
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the (G)MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	Description
31:8	RO	000000h	**Reserved**
7	RO	0b	**Reserved**
6:5	RO	00b	**Reserved**
4	RO	1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.
3	RO	1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible If this (G)MCH does not have internal graphics capability (CAPID0[33] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2	RO	0b	**Reserved**
1	RO	1b	**PCI Express Graphics Port Enable. (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities, SDVO presence HW strap and SDVO/PCIe concurrent HW strap. Device 1 is Disabled on Reset if {the SDVO present strap is sampled high and the SDVO/PCIe concurrent strap is sampled low}.
0	RO	1b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

21.2.20 BSM - Base of Stolen Memory

B/D/F/Type: 0/2/1/PCI
Address Offset: 5C-63h
Default Value: 0000000000000000h
Access: RO
Size: 64 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, (G)MCH claims 1 to 64MBs of DRAM for internal graphics if enabled.

Bit	Access	Default Value	Description
63:36	RO	0000000h	**Reserved**
35:32	RO	0h	**Base of Stolen Memory**
31:20	RO	000h	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO	00000h	**Reserved**

21.2.21 MSAC - Multi Size Aperture Control

B/D/F/Type: 0/2/1/PCI
Address Offset: 66h
Default Value: 02h
Access: RO
Size: 8 bits

This register determines the size of the graphics memory aperture in Function 0 and only in the untrusted space. By default, the aperture size is 256 MB. Only the system BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. **System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.**

Bit	Access	Default Value	Description
7:4	RO	0h	**Scratch Bits Only:** Have no physical effect on hardware.
3	RO	0b	**Reserved**
2:1	RO	01b	**Untrusted Aperture Size (LHSAS):** 11: bits [28:27] of GMADR register are made Read only and forced to zero, allowing only 512 MB of GMADR 01: bit [28] of GMADR is made R/W and bit [27] of GMADR is forced to zero allowing 256 MB of GMADR 00: bits [28:27] of GMADR register are made R/W allowing 128 MB of GMADR 10: Illegal programming.
0	RO	0b	**Reserved**

21.3 Device 2 Function 0 –PCI I/O Registers

The following are not PCI config registers. They are I/O registers. This mechanism allows access to internal graphics MMIO registers must not be used to access VGA I/O registers which are mapped through the MMIO space. VGA registers must be access directly through the dedicated VGA IO ports.

21.3.1 Device 2 Function 0 IO Configuration Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
MMIO Address Register	Index	0	3	00000000h	R/W
MMIO Data Register	Data	4	7	00000000h	R/W

21.3.2 Index - MMIO Address Register

B/D/F/Type: 0/2/0/PCI IO
Address Offset: 0-3h
Default Value: 00000000h
Access: R/W
Size: 32 bits

MMIO_INDEX: A 32 bit IO write to this port loads the offset of the MMIO register that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed by the (G)MCH but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Bit	Access	Default Value	Description
31:2	R/W	00000000h	**Reserved**
1:0	R/W	00b	**Target:** 00: MMIO Registers. Others: Reserved

21.3.3 Data - MMIO Data Register

B/D/F/Type: 0/2/0/PCI IO
Address Offset: 4-7h
Default Value: 00000000h
Access: R/W
Size: 32 bits

MMIO_DATA: A 32 bit IO write to this port is re-directed to the MMIO register/GTT location pointed to by the MMIO-index register. A 32 bit IO read to this port is re-directed to the MMIO register address pointed to by the MMIO-index register regardless of the target selection in MMIO_INDEX (1:0). 8 or 16 bit IO writes are completed by the (G)MCH and may have un-intended side effects, hence must not be used to access the data port. 8 or 16 bit IO reads are completed normally.

Note: If the target field in MMIO Index selects "GTT", reads to MMIO data return 0's and not the value programmed in the GTT memory corresponding to the offset programmed in MMIO index.

Bit	Access	Default Value	Description
31:0	R/W	00000000h	**MMIO Data Window (DATA)**

22 Intel® Management Engine Subsystem PCI Device 3

22.1 MEI1 PCI Device 3 Function 0

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identifiers	ID	0	3	2A04h[1] 2A14h[2]	RO
Command	CMD	4	5	0000h	RO; RW
Device Status	STS	6	7	0010h	RO
Revision ID	RID	8	8	00h	RO
Class Code	CC	9	B	000000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	80h	RO
Reserved		F	F		
MEI MMIO Base Address	MEI_MBAR	10	17	0000000000000004h	RO; RW
Reserved		18	2B		
Sub System Identifiers	SS	2C	2F	00000000h	RWO
Reserved		30	33		
Capabilities Pointer	CAP	34	34	50h	RO
Reserved		35	3B		
Interrupt Information	INTR	3C	3D	0100h	RO; RW
Minimum Grant	MGNT	3E	3E	00h	RO
Maximum Latency	MLAT	3F	3F	00h	RO
Host Firmware Status	HFS	40	43	00000000h	RO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		44	4F		
PCI Power Management Capability ID	PID	50	51	8C01h	RO
PCI Power Management Capabilities	PC	52	53	C803h	RO
PCI Power Management Control and Status	PMCS	54	55	0008h	RWC; RO; RW
Reserved		56	8B		
Message Signaled Interrupt Identifiers	MID	8C	8D	0005h	RO
Message Signaled Interrupt Message Control	MC	8E	8F	0080h	RO; RW
Message Signaled Interrupt Message Address	MA	90	93	00000000h	RW; RO
Reserved		94	97		
Message Signaled Interrupt Message Data	MD	98	99	0000h	RW
Intel® MEI Interrupt Delivery Mode	HIDM	A0	A0	00h	RW

NOTES:

1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

22.1.1 ID - Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 0-3h
Default Value: 29748086h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	2A04h[1] 2A14h[2]	**Device ID (DID):** Indicates what device number assigned for the Intel® Management Engine subsystem.
15:0	RO	8086h	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

22.1.2 CMD - Command

B/D/F/Type: 0/3/0/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00000b	**Reserved**
10	RW	0b	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	RO	0b	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	RO	0b	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	RO	0b	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	RO	0b	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	RO	0b	**VGA Palette Snooping Enable (VGA):** Not implemented, hardwired to 0

Bit	Access	Default Value	Description
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	RW	0b	**Bus Master Enable (BME):** Controls the Intel® MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel® Management Engine MSI. When this bit is 0, Intel MEI is blocked from generating MSI to the host CPU.
1	RW	0b	**Memory Space Enable (MSE):** Controls access to the Intel MEI host controller's memory mapped register space.
0	RO	0b	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

22.1.3 STS - Device Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 6-7h
Default Value: 0010h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	RO	0b	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	RO	0b	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	RO	0b	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	RO	0b	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	RO	00b	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.

Bit	Access	Default Value	Description
8	RO	0b	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	RO	0b	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	RO	0b	**Reserved**
5	RO	0b	**66-MHz Capable (C66):** Not implemented, hardwired to 0.
4	RO	1b	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	RO	0b	**Interrupt Status (IS):** Indicates the interrupt status of the device (1 = asserted).
2:0	RO	000b	**Reserved**

22.1.4 RID - Revision ID

B/D/F/Type: 0/3/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision ID (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch.

22.1.5 CC - Class Code

B/D/F/Type: 0/3/0/PCI
Address Offset: 9-Bh
Default Value: 000000h
Access: RO
Size: 24 bits

Bit	Access	Default Value	Description
23:16	RO	00h	**Base Class Code (BCC):** Indicates the base class code of the Intel® MEI host controller device.
15:8	RO	00h	**Sub Class Code (SCC):** Indicates the sub class code of the Intel MEI host controller device.
7:0	RO	00h	**Programming Interface (PI):** Indicates the programming interface of the Intel MEI host controller device.

22.1.6 CLS - Cache Line Size

B/D/F/Type: 0/3/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

22.1.7 MLT - Master Latency Timer

B/D/F/Type: 0/3/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

22.1.8 HTYPE - Header Type

B/D/F/Type: 0/3/0/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7	RO	1b	**Multi-Function Device (MFD):** Indicates the Intel® MEI host controller is part of a multi-function device.
6:0	RO	0000000b	**Header Layout (HL):** Indicates that the Intel MEI host controller uses a target device layout.

22.1.9 MEI_MBAR - MEI MMIO Base Address

B/D/F/Type: 0/3/0/PCI
Address Offset: 10-17h
Default Value: 0000000000000004h
Access: RO; RW
Size: 64 bits

Bit	Access	Default Value	Description
63:4	RW	00000000 0000000h	**Base Address (BA):** Base address of register memory space.
3	RO	0b	**Prefetchable (PF):** Indicates that this range is not prefetchable
2:1	RO	10b	**Type (TP):** Indicates that this range can be mapped anywhere in 64-bit address space.
0	RO	0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

22.1.10 SS - Sub System Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 2C-2Fh
Default Value: 00000000h
Access: RWO;
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RWO	0000h	**Subsystem ID (SSID):** Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	RWO	0000h	**Subsystem Vendor ID (SSVID):** Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.

22.1.11 CAP - Capabilities Pointer

B/D/F/Type: 0/3/0/PCI
Address Offset: 34h
Default Value: 50h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	50h	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

22.1.12 INTR - Interrupt Information

B/D/F/Type: 0/3/0/PCI
Address Offset: 3C-3Dh
Default Value: 0100h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	01h	**Interrupt Pin (IPIN):** This indicates the interrupt pin the Intel® MEI host controller uses. The value of 01h selects INTA# interrupt pin. **NOTE:** As Intel MEI is an internal device in the GMCH, the INTA# pin is implemented as an INTA# message to the ICH.
7:0	RW	00h	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to.

22.1.13 MGNT - Minimum Grant

B/D/F/Type: 0/3/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Grant (GNT):** Not implemented, hardwired to 0.

22.1.14 MLAT - Maximum Latency

B/D/F/Type: 0/3/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Latency (LAT):** Not implemented, hardwired to 0.

22.1.15 HFS - Host Firmware Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 40-43h
Default Value: 00000000h
Access: RO;
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00000000h	**Firmware Status Host Access (FS_HA):** Reserved.

22.1.16 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/0/PCI
Address Offset: 50-51h
Default Value: 8C01h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	8Ch	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO	01h	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

22.1.17 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/0/PCI
Address Offset: 52-53h
Default Value: C803h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	11001b	**PME_Support (PSUP):** Indicates the states that can generate PME#. Intel® Management Engine Interface can assert PME# from any D-state except D1 or D2 which are not supported by Intel MEI.
10	RO	0b	**D2_Support (D2S):** The D2 state is not supported for the Intel MEI host controller.
9	RO	0b	**D1_Support (D1S):** The D1 state is not supported for the Intel MEI host controller.
8:6	RO	000b	**Reserved**
5	RO	0b	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	RO	0b	**Reserved**
3	RO	0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

22.1.18 PMCS - PCI Power Management Control and Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 54-55h
Default Value: 0008h
Access: RWC; RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15	RWC	0b	**PME Status (PMES):** The PME Status bit in Intel® MEI space can be set to 1 by FW performing a write into AUX register to set PMES. This bit is cleared by host CPU writing a 1 to it. FW cannot clear this bit. Host CPU writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#
14:9	RO	000000b	Reserved
8	RW	0b	**PME Enable (PMEE):** This bit is read/write, under control of host SW. It does not directly have an effect on PME events. This bit is reset to 0 by MRST#
7:4	RO	0000b	**Reserved**
3	RO	1b	**No_Soft_Reset (NSR):** This bit indicates that when the Intel MEI host controller is transitioning from D3hot to D0 due to power state command, it does not perform an internal reset.
2	RO	0b	**Reserved**
1:0	RW	00b	**Power State (PS):** This field is used both to determine the current power state of the Intel MEI host controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state

22.1.19 MID - Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 8C-8Dh
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Next Pointer (NEXT):** Indicates the next item in the list. This can be other capability pointers (such as PCI-Express) or it can be the last item in the list.
7:0	RO	05h	**Capability ID (CID):** Capabilities ID indicates MSI.

22.1.20 MC - Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/0/PCI
Address Offset: 8E-8Fh
Default Value: 0080h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	1b	**64-Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages.
6:4	RO	000b	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	RO	000b	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	RW	0b	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

22.1.21 MA - Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/0/PCI
Address Offset: 90-93h
Default Value: 00000000h
Access: RW; RO
Size: 32 bits

Bit	Access	Default Value	Description
31:2	RW	00000000h	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW-aligned.
1:0	RO	00b	**Reserved**

22.1.22 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/0/PCI
Address Offset: 98-99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RW	0000h	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

22.1.23 HIDM - MEI Interrupt Delivery Mode

B/D/F/Type: 0/3/0/PCI
Address Offset: A0h
Default Value: 00h
Access: RW
Size: 8 bits
BIOS Optimal Default 00h

Bit	Access	Default Value	Description
7:2	RO	0h	**Reserved**
1:0	RW	00b	**MEI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the Intel® MEI will send: 00: Generate Legacy or MSI interrupt 01: Generate SCI 10: Generate SMI

22.2 MEI2 PCI Device 3 Function 1

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identifiers	ID	0	3	2A05h[1] 2A15h[2]	RO
Command	CMD	4	5	0000h	RO; RW
Device Status	STS	6	7	0010h	RO
Revision ID	RID	8	8	00h	RO
Class Code	CC	9	B	000000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	80h	RO
Reserved		F	F		
MEI MMIO Base Address	MEI_MBAR	10	17	000000000000 0004h	RO; RW
Reserved		18	2B		
Sub System Identifiers	SS	2C	2F	00000000h	RWO
Reserved		30	33		
Capabilities Pointer	CAP	34	34	50h	RO
Reserved		35	3B		
Interrupt Information	INTR	3C	3D	0100h	RW; RO
Minimum Grant	MGNT	3E	3E	00h	RO
Maximum Latency	MLAT	3F	3F	00h	RO
Host Firmware Status	HFS	40	43	00000000h	RO
Reserved		44	4F		
PCI Power Management Capability ID	PID	50	51	8C01h	RO
PCI Power Management Capabilities	PC	52	53	C803h	RO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
PCI Power Management Control and Status	PMCS	54	55	0008h	RW; RWC; RO
Reserved		56	8B		
Message Signaled Interrupt Identifiers	MID	8C	8D	0005h	RO
Message Signaled Interrupt Message Control	MC	8E	8F	0080h	RO, RW
Message Signaled Interrupt Message Address	MA	90	93	00000000h	RO, RW
Reserved		94	97		
Message Signaled Interrupt Message Data	MD	98	99	0000h	RW
MEI Interrupt Delivery Mode	HIDM	A0	A0	00h	RW

NOTES:

1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

22.2.1 ID - Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 0-3h
Default Value: 29058086h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	2A05h[1] 2A15h[2]	**Device ID (DID):** Indicates what device number assigned by Intel.
15:0	RO	8086h	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

22.2.2 CMD - Command

B/D/F/Type: 0/3/1/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00000b	**Reserved**
10	RW	0b	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	RO	0b	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	RO	0b	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	RO	0b	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	RO	0b	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	RO	0b	**VGA Palette Snooping Enable (VGA):** Not implemented, hardwired to 0
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	RW	0b	**Bus Master Enable (BME):** Controls the Intel® MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel® Management Engine ME MSI. When this bit is 0, Intel MEI is blocked from generating MSI to the host CPU.
1	RW	0b	**Memory Space Enable (MSE):** Controls access to the Intel MEI host controller's memory mapped register space.
0	RO	0b	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

22.2.3 STS - Device Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 6-7h
Default Value: 0010h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	RO	0b	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	RO	0b	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	RO	0b	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	RO	0b	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	RO	00b	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	RO	0b	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	RO	0b	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	RO	0b	**Reserved**
5	RO	0b	**66-MHz Capable (C66):** Not implemented, hardwired to 0.
4	RO	1b	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	RO	0b	**Interrupt Status (IS):** Indicates the interrupt status of the device (1 = asserted).
2:0	RO	000b	**Reserved**

22.2.4 RID - Revision ID

B/D/F/Type: 0/3/1/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision ID (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch..

22.2.5 CC - Class Code

B/D/F/Type: 0/3/1/PCI
Address Offset: 9-Bh
Default Value: 000000h
Access: RO
Size: 24 bits

Bit	Access	Default Value	Description
23:16	RO	00h	**Base Class Code (BCC):** Indicates the base class code of the Intel® MEI host controller device.
15:8	RO	00h	**Sub Class Code (SCC):** Indicates the sub class code of the Intel MEI host controller device.
7:0	RO	00h	**Programming Interface (PI):** Indicates the programming interface of the Intel MEI host controller device.

22.2.6 CLS - Cache Line Size

B/D/F/Type: 0/3/1/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

22.2.7 MLT - Master Latency Timer

B/D/F/Type: 0/3/1/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

22.2.8 HTYPE - Header Type

B/D/F/Type: 0/3/1/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7	RO	1b	**Multi-Function Device (MFD):** Indicates the Intel® MEI host controller is part of a multi-function device.
6:0	RO	0000000b	**Header Layout (HL):** Indicates that the Intel MEI host controller uses a target device layout.

22.2.9 MEI_MBAR - MEI MMIO Base Address

B/D/F/Type: 0/3/1/PCI
Address Offset: 10-17h
Default Value: 0000000000000004h
Access: RO; RW
Size: 64 bits

Bit	Access	Default Value	Description
63:4	RW	00000000 0000000h	**Base Address (BA):** Base address of register memory space.
3	RO	0b	**Prefetchable (PF):** Indicates that this range is not prefetchable
2:1	RO	10b	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space
0	RO	0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

22.2.10 SS - Sub System Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 2C-2Fh
Default Value: 00000000h
Access: RWO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RWO	0000h	**Subsystem ID (SSID):** Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	RWO	0000h	**Subsystem Vendor ID (SSVID):** Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.

22.2.11 CAP - Capabilities Pointer

B/D/F/Type: 0/3/1/PCI
Address Offset: 34h
Default Value: 50h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	50h	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

22.2.12 INTR - Interrupt Information

B/D/F/Type: 0/3/1/PCI
Address Offset: 3C-3Dh
Default Value: 0100h
Access: RW; RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	01h	**Interrupt Pin (IPIN):** This indicates the interrupt pin the Intel® MEI host controller uses. The value of 01h selects INTA# interrupt pin. **NOTE:** As Intel MEI is an internal device in the GMCH, the INTA# pin is implemented as an INTA# message to the ICH.
7:0	RW	00h	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

22.2.13 MGNT - Minimum Grant

B/D/F/Type: 0/3/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Grant (GNT):** Not implemented, hardwired to 0.

22.2.14 MLAT - Maximum Latency

B/D/F/Type: 0/3/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Latency (LAT):** Not implemented, hardwired to 0.

22.2.15 HFS - Host Firmware Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 40-43h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00000000h	**Firmware Status Host Access (FS_HA):** Indicates current status of the firmware for the Intel® MEI controller.

22.2.16 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/1/PCI
Address Offset: 50-51h
Default Value: 8C01h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	8Ch	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO	01h	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

22.2.17 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/1/PCI
Address Offset: 52-53h
Default Value: C803h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	11001b	**PME_Support (PSUP):** Indicates the states that can generate PME#. Intel® MEI can assert PME# from any D-state except D1 or D2 which are not supported by Intel MEI.
10	RO	0b	**D2_Support (D2S):** The D2 state is not supported for the Intel MEI host controller.
9	RO	0b	**D1_Support (D1S):** The D1 state is not supported for the Intel MEI host controller.
8:6	RO	000b	**Reserved**
5	RO	0b	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	RO	0b	**Reserved**
3	RO	0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

22.2.18 PMCS - PCI Power Management Control and Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 54-55h
Default Value: 0008h
Access: RW; RWC; RO
Size: 16 bits

Bit	Access	Default Value	Description
15	RWC	0b	**PME Status (PMES):** The PME Status bit in Intel® MEI space can be set to 1 by ARC FW performing a write into AUX register to set PMES. This bit is cleared by host CPU writing a 1 to it. ARC cannot clear this bit. Host CPU writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#
14:9	RO	000000b	**Reserved**
8	RW	0b	**PME Enable (PMEE):** This bit is read/write, under control of host SW. It does not directly have an effect on PME events. However, this bit is shadowed into AUX space so ARC FW can monitor it. The ARC FW is responsible for ensuring that FW does not cause the PME-S bit to transition to 1 while the PMEE bit is 0, indicating that host SW had disabled PME. This bit is reset to 0 by MRST#
7:4	RO	0000b	**Reserved**
3	RO	1b	**No_Soft_Reset (NSR):** This bit indicates that when the Intel MEI host controller is transitioning from D3hot to D0 due to power state command, it does not perform and internal reset. Configuration context is pRSVD (RSVD): Reserved
2	RO	0b	**Reserved**
1:0	RW	00b	**Power State (PS):** This field is used both to determine the current power state of the Intel MEI host controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state

22.2.19 MID - Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 8C-8Dh
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Next Pointer (NEXT):** Indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI-Express) or it can be the last item in the list.
7:0	RO	05h	**Capability ID (CID):** Capabilities ID indicates MSI.

22.2.20 MC - Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/1/PCI
Address Offset: 8E-8Fh
Default Value: 0080h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	1b	**64-Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages.
6:4	RO	000b	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	RO	000b	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	RW	0b	**MSI Enable (MSIE):** I f set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

22.2.21 MA - Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/1/PCI
Address Offset: 90-93h
Default Value: 00000000h
Access: RO; RW;
Size: 32 bits

Bit	Access	Default Value	Description
31:2	RW	00000000h	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	RO	00b	**Reserved**

22.2.22 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/1/PCI
Address Offset: 98-99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RW	0000h	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

22.2.23 HIDM - MEI Interrupt Delivery Mode

B/D/F/Type: 0/3/1/PCI
Address Offset: A0h
Default Value: 00h
Access: RW
Size: 8 bits
BIOS Optimal Default 00h

Bit	Access	Default Value	Description
7:2	RO	0h	**Reserved**
1:0	RW	00b	**MEI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the Intel® MEI will send when ARC writes to set the M_IG bit in AUX space. They are interpreted as follows: 00: Generate Legacy or MSI interrupt 01: Generate SCI 10: Generate SMI

22.3 AMT IDER PCI Device 3 Function 2

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identification	ID	0	3	2A06h[1] 2A16h[2]	RO
Command Register	CMD	4	5	0000b	RO;RW
Device Status	STS	6	7	00B0h	RO
Revision ID	RID	8	8	00h	RO
Class Codes	CC	9	B	010185h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	< Not Defined >	< Not Defined >
Reserved		F	F		
Primary Command Block IO Bar	PCMDBA	10	13	00000001h	RO; RW
Primary Control Block Base Address	PCTLBA	14	17	00000001h	RO; RW

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Secondary Command Block Base Address	SCMDBA	18	1B	00000001h	RO; RW
Secondary Control Block base Address	SCTLBA	1C	1F	00000001h	RO; RW
Legacy Bus Master Base Address	LBAR	20	23	00000001h	RO; RW
Reserved	RSVD	24	27		
Reserved		28	2B		
Sub System Identifiers	SS	2C	2F	00008086h	RWO
Expansion ROM Base Address	EROM	30	33	00000000h	RO
Capabilities Pointer	CAP	34	34	C8h	RO
Reserved		35	3B		
Interrupt Information	INTR	3C	3D	0300h	RO; RW
Minimum Grant	MGNT	3E	3E	00h	RO
Maximum Latency	MLAT	3F	3F	00h	RO
Reserved		40	C7		
PCI Power Management Capability ID	PID	C8	C9	D001h	RO
PCI Power Management Capabilities	PC	CA	CB	0023h	RO
PCI Power Management Control and Status	PMCS	CC	CF	00000000h	RO; RW; RWC
Message Signaled Interrupt Capability ID	MID	D0	D1	0005h	RO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Message Signaled Interrupt Message Control	MC	D2	D3	0080h	RO; RW
Message Signaled Interrupt Message Address	MA	D4	D7	00000000h	RO; RW
Message Signaled Interrupt Message Upper Address	MAU	D8	DB	00000000h	RO; RW
Message Signaled Interrupt Message Data	MD	DC	DD	0000h	RW

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

22.3.1 ID - Identification

B/D/F/Type: 0/3/2/PCI
Address Offset: 0-3h
Default Value: 29768086h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	2A06h[1] 2A16h[2]	**Device ID (DID):** Assigned by Manufacturer, identifies the type of Device.
15:0	RO	8086h	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

22.3.2 CMD - Command Register

B/D/F/Type: 0/3/2/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

.

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	RW	0b	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt and MSI is not enabled.
9:3	RO	0b	**Reserved**
2	RW	0b	**Bus Master Enable (BME):** Controls the Intel® Active Management Technology (Intel® AMT) function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	RO	0b	**Memory Space Enable (MSE):** Intel AMT function does not contain target memory space.
0	RW	0b	**I/O Space Enable (IOSE):** Controls access to the Intel AMT function's target I/O space.

22.3.3 STS - Device Status

B/D/F/Type: 0/3/2/PCI
Address Offset: 6-7h
Default Value: 00B0h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** No parity error on its interface.
14	RO	0b	**Signaled System Error (SSE):** The Intel® AMT function will never generate a SERR#.
13	RO	0b	**Reserved**
12	RO	0b	**Reserved**
11	RO	0b	**Reserved**
10:9	RO	00b	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the Intel AMT function's PCI interface.
8	RO	0b	**Master Data Parity Error Detected) (DPD):** Intel AMT function (IDER), as a master, does not detect a parity error. Other Intel AMT function is not a master and hence this bit is reserved also.
7:5	RO	1b	**Reserved**
4	RO	1b	**Capabilities List (CL):** Indicates that there is a capabilities pointer implemented in the device.
3	RO	0b	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTC interrupt asserted to the Host
2:0	RO	000b	**Reserved**

22.3.4 RID - Revision ID

B/D/F/Type: 0/3/2/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision ID (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch.

22.3.5 CC - Class Codes

B/D/F/Type: 0/3/2/PCI
Address Offset: 9-Bh
Default Value: 010185h
Access: RO
Size: 24 bits

Bit	Access	Default Value	Description
23:0	RO	010185h	**Programming Interface BCC SCC (PI BCC SCC)**

22.3.6 CLS - Cache Line Size

B/D/F/Type: 0/3/2/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** All writes to system memory are Memory Writes.

22.3.7 MLT - Master Latency Timer

B/D/F/Type: 0/3/2/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer (MLT):** Not implemented since the function is in (G)MCH

22.3.8 HTYPE - Header Type

B/D/F/Type: 0/3/2/PCI
Address Offset: Eh
Default Value: < Not Defined >
Access: < Not Defined >
Size: 8 bits

Register is **not** implemented.

22.3.9 PCMDBA - Primary Command Block IO Bar

B/D/F/Type: 0/3/2/PCI
Address Offset: 10-13h
Default Value: 00000001h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:3	RW	0000h	**Base Address (BAR):** Base Address of the BAR0 I/O space (8 consecutive I/O locations)
2:1	RO	00b	**Reserved**
0	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

22.3.10 PCTLBA - Primary Control Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 14-17h
Default Value: 00000001h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:2	RW	0000h	**Base Address (BAR):** Base Address of the BAR1 I/O space (4 consecutive I/O locations)
1	RO	0b	**Reserved**
0	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

22.3.11 SCMDBA - Secondary Command Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 18-1Bh
Default Value: 00000001h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:3	RW	0000h	**Base Address (BAR):** Base Address of the I/O space (8 consecutive I/O locations)
2:1	RO	00b	**Reserved**
0	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

22.3.12 SCTLBA - Secondary Control Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 1C-1Fh
Default Value: 00000001h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:2	RW	0000h	**Base Address (BAR):** Base Address of the I/O space (4 consecutive I/O locations)
1	RO	0b	**Reserved**
0	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

22.3.13 LBAR - Legacy Bus Master Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 20-23h
Default Value: 00000001h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:4	RW	000h	**Base Address (BA):** Base Address of the I/O space (16 consecutive I/O locations)
3:1	RO	000b	**Reserved**
0	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

22.3.14 SS - Sub System Identifiers

B/D/F/Type: 0/3/2/PCI
Address Offset: 2C-2Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RWO	0000h	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value
15:0	RWO	8086h	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value

22.3.15 EROM - Expansion ROM Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 30-33h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:11	RO	000000h	**Expansion ROM Base Address (ERBAR)**
10:1	RO	000h	**Reserved**
0	RO	0b	**Enable (EN):** Enable expansion ROM Access

22.3.16 CAP - Capabilities Pointer

B/D/F/Type: 0/3/2/PCI
Address Offset: 34h
Default Value: C8h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	c8h	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset c8h (the power management capability)

22.3.17 INTR - Interrupt Information

B/D/F/Type: 0/3/2/PCI
Address Offset: 3C-3Dh
Default Value: 0300h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	03h	**Interrupt Pin (IPIN):** A value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively Function Value INTx (2 IDE) 03h INTC
7:0	RW	00h	**Interrupt Line (ILINE):** The value written in this register tells which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the HW

22.3.18 MGNT - Minimum Grant

B/D/F/Type: 0/3/2/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Reserved**

22.3.19 MLAT - Maximum Latency

B/D/F/Type: 0/3/2/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Reserved**

22.3.20 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/2/PCI
Address Offset: C8-C9h
Default Value: D001h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	D0h	**Next Capability (NEXT):** Its value of 0xD0 points to the MSI capability
7:0	RO	01h	**Cap ID (CID):** Indicates that this pointer is a PCI power management

22.3.21 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/2/PCI
Address Offset: CA-CBh
Default Value: 0023h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00000b	**PME Support (PME):** Indicates no PME# in the Intel® AMT function
10	RO	0b	**D2 Support (D2S):** The D2 state is not Supported
9	RO	0b	**D1 Support (D1S):** The D1 state is not supported
8:6	RO	000b	**Reserved**
5	RO	1b	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	RO	0b	**Reserved**
3	RO	0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#
2:0	RO	011b	**Version (VS):** Indicates support for revision 1.2 of the PCI power management specification

22.3.22 PMCS - PCI Power Management Control and Status

B/D/F/Type: 0/3/2/PCI
Address Offset: CC-CFh
Default Value: 00000000h
Access: RO; RW; RWC
Size: 32 bits
BIOS Optimal Default 0000h

Bit	Access	Default Value	Description
31:16	RO	0h	**Reserved**
15	RO	0b	**PME Status (PMES):** This bit is set when a PME event is to be requested. Not supported
14:9	RO	00h	**Reserved**
8	RO	0b	**PME Enable (PMEE):** Not Supported
7:4	RO	0000b	**Reserved**
3	RWC	0b	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized.
2	RO	0b	**Reserved**
1:0	RW	00b	**Power State (PS):** This field is used both to determine the current power state of the Intel® AMT function and to set a new power state. The values are: 00 – D0 state 11 – D3HOT state

22.3.23 MID - Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/2/PCI
Address Offset: D0-D1h
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Next Pointer (NEXT):** Value indicates this is the last item in the capabilities list.
7:0	RO	05h	**Capability ID (CID):** Capabilities ID value indicates device is capable of generating an MSI

22.3.24 MC - Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/2/PCI
Address Offset: D2-D3h
Default Value: 0080h
Access: RO; RW
Size: 16 bits

.

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	1b	**64-Bit Address Capable (C64):** Capable of generating 64-bit and 32-bit messages
6:4	RW	000b	**Multiple Message Enable (MME):** These bits are R/W for software compatibility, but only one message is ever sent by the Intel® AMT function
3:1	RO	000b	**Multiple Message Capable (MMC):** Only one message is required
0	RW	0b	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts

22.3.25 MA - Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/2/PCI
Address Offset: D4-D7h
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:2	RW	00000000h	**Address (ADDR):** Lower 32 bits of the system specified message address, always Dword aligned
1:0	RO	00b	**Reserved**

22.3.26 MAU - Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/2/PCI
Address Offset: D8-DBh
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:4	RO	0000000h	**Reserved**
3:0	RW	0000b	**Address (ADDR):** Upper 4 bits of the system specified message address

22.3.27 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/2/PCI
Address Offset: DC-DDh
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RW	0000h	**Data (DATA):** This content is driven onto the lower word of the data bus of the MSI memory write transaction

22.4 (KT) Redirection PCI Device 3 Function 3

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identification	ID	0	3	2A07h[1] 2A17h[2]	RO
Command Register	CMD	4	5	0000h	RO; RW
Device Status	STS	6	7	00B0h	RO
Revision ID	RID	8	8	00h	RO
Class Codes	CC	9	B	010185h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	< Not Defined >	< Not Defined >
Reserved		F	F		
KT IO Block Base Address	KTIBA	10	13	00000001h	RO; RW
KT Mem Block Base Address	KTMBA	14	17	00000000h	RO; RW
Reserved		18	28		
Sub System Identifiers	SS	2C	2F	00008086h	RWO
Expansion ROM Base Address	EROM	30	33	00000000h	RO
Capabilities Pointer	CAP	34	34	C8h	RO
Reserved		35	3B		
Interrupt Information	INTR	3C	3D	0200h	RO; RW
Minimum Grant	MGNT	3E	3E	00h	RO
Maximum Latency	MLAT	3F	3F	00h	RO
Reserved		40	C7		
PCI Power Management Capability ID	PID	C8	C9	D001h	RO

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
PCI Power Management Capabilities	PC	CA	CB	0023h	RO
PCI Power Management Control and Status	PMCS	CC	CF	00000000h	RO; RW; RWC
Message Signaled Interrupt Capability ID	MID	D0	D1	0005h	RO
Message Signaled Interrupt Message Control	MC	D2	D3	0080h	RO; RW
Message Signaled Interrupt Message Address	MA	D4	D7	00000000h	RO; RW
Message Signaled Interrupt Message Upper Address	MAU	D8	DB	00000000h	RO; RW
Message Signaled Interrupt Message Data	MD	DC	DD	0000h	RW

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only

22.4.1 ID - Identification

B/D/F/Type: 0/3/3/PCI
Address Offset: 0-3h
Default Value: 29878086h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	2A07h1 2A17h2	**Device ID (DID):** Assigned by manufacturer, identifies the device.
15:0	RO	8086h	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

NOTES:
1. Valid for all Mobile Intel 965 Express Chipsets except for the Mobile Intel GME965 and GLE960 Express Chipsets.
2. Valid for the Mobile Intel GME965 and GLE960 Express Chipsets only.

22.4.2 CMD - Command Register

B/D/F/Type: 0/3/3/PCI
Address Offset: 4-5h
Default Value: 0000h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	**Reserved**
10	RW	0b	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt and MSI is not enabled.
9:3	RO	0b	**Fast Back-to-Back Enable (FBE):** Reserved
2	RW	0b	**Bus Master Enable (BME):** Controls the KT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. For KT, the only bus mastering activity is MSI generation.
1	RW	0b	**Memory Space Enable (MSE):** Controls Access to the Intel® AMT function's target memory space.
0	RW	0b	**I/O Space Enable (IOSE):** Controls access to the Intel AMT function's target I/O space.

22.4.3 STS - Device Status

B/D/F/Type: 0/3/3/PCI
Address Offset: 6-7h
Default Value: 00B0h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** No parity error on its interface
14	RO	0b	**Signaled System Error (SSE):** The Intel® AMT function will never generate an SERR#
13	RO	0b	**Reserved**
12	RO	0b	**Reserved**
11	RO	0b	**Reserved**
10:9	RO	00b	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the Intel AMT function's PCI interface
8	RO	0b	**Master Data Parity Error Detected) (DPD):** AMT function (IDER), as a master, does not detect a parity error. Other AMT function is not a master and hence this bit is reserved also.
7	RO	1b	**Reserved**
6	RO	0b	**Reserved**
5	RO	1b	**Reserved**
4	RO	1b	**Capabilities List (CL):** Indicates that there is a capabilities pointer implemented in the device.
3	RO	0b	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTB interrupt asserted to the Host
2:0	RO	000b	**Reserved**

22.4.4 RID - Revision ID

B/D/F/Type: 0/3/3/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Revision ID (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH. A register swapping mechanism behind RID register is used to select between a single SRID, or a single CRID to be reflected in the RID register. For the C0 stepping SRID= 03h, CRID= 0Ch.

22.4.5 CC - Class Codes

B/D/F/Type: 0/3/3/PCI
Address Offset: 9-Bh
Default Value: 010185h
Access: RO
Size: 24 bits

Bit	Access	Default Value	Description
23:0	RO	010185h	**Programming Interface BCC SCC (PI BCC SCC)**

22.4.6 CLS - Cache Line Size

B/D/F/Type: 0/3/3/PCI
Address Offset: Ch
Default Value: 00h
Access: RO;
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Cache Line Size (CLS):** All writes to system memory are Memory Writes.

22.4.7 MLT - Master Latency Timer

B/D/F/Type: 0/3/3/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

.

Bit	Access	Default Value	Description
7:0	RO	00h	**Master Latency Timer (MLT):** Not implemented since the function is in (G)MCH.

22.4.8 HTYPE - Header Type

B/D/F/Type: 0/3/3/PCI
Address Offset: Eh
Default Value: < Not Defined >
Access: < Not Defined >
Size: 8 bits

Register is **not** implemented. Reads return 0.

22.4.9 KTIBA - KT IO Block Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 10-13h
Default Value: 00000001h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	**Reserved**
15:3	RW	0000h	**Base Address (BAR):** Base Address of the I/O space (8 consecutive I/O locations).
2:1	RO	00b	**Reserved**
0	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space.

22.4.10 KTMBA - KT Mem Block Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 14-17h
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:12	RW	00000h	**Base Address (BAR):** Memory Mapped IO BAR.
11:4	RO	00h	**Reserved**
3	RO	0b	**Prefetchable (PF):** Indicates that this range is not prefetchable.
2:1	RO	00b	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	RO	0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

22.4.11 SS - Sub System Identifiers

B/D/F/Type: 0/3/3/PCI
Address Offset: 2C-2Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RWO	0000h	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	RWO	8086h	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

22.4.12 EROM - Expansion ROM Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 30-33h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:11	RO	000000h	**Expansion ROM Base Address (ERBAR)**
10:1	RO	000h	**Reserved**
0	RO	0b	**Enable (EN):** Enable expansion ROM Access.

22.4.13 CAP - Capabilities Pointer

B/D/F/Type: 0/3/3/PCI
Address Offset: 34h
Default Value: C8h
Access: RO
Size: 8 bits

.

Bit	Access	Default Value	Description
7:0	RO	c8h	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset c8h (the power management capability)

22.4.14 INTR - Interrupt Information

B/D/F/Type: 0/3/3/PCI
Address Offset: 3C-3Dh
Default Value: 0200h
Access: RW; RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	02h	**Interrupt Pin (IPIN):** A value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. Function / Value / INTx (3 KT/Serial Port) / 02h / INTB
7:0	RW	00h	**Interrupt Line (ILINE):** The value written in this register tells which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the hardware.

22.4.15 MGNT - Minimum Grant

B/D/F/Type: 0/3/3/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Reserved**

22.4.16 MLAT - Maximum Latency

B/D/F/Type: 0/3/3/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	**Reserved**

22.4.17 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/3/PCI
Address Offset: C8-C9h
Default Value: D001h
Access: RO
Size: 16 bits

it	Access	Default Value	Description
15:8	RO	D0h	**Next Capability (NEXT):** Its value of 0xD0 points to the MSI capability.
7:0	RO	01h	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

22.4.18 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/3/PCI
Address Offset: CA-CBh
Default Value: 0023h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00000b	**PME Support (PME):** Indicates no PME# in the Intel® AMT function.
10	RO	0b	**D2 Support (D2S):** The D2 state is not supported.
9	RO	0b	**D1 Support (D1S):** The D1 state is not supported.
8:6	RO	000b	**Aux Current (AUXC):** PME# from D3 (cold) state is not supported, therefore this field is 000b.
5	RO	1b	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	RO	0b	**Reserved**
3	RO	0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	**Version (VS):** Indicates support for revision 1.2 of the PCI power management specification.

22.4.19 PMCS - PCI Power Management Control and Status

B/D/F/Type: 0/3/3/PCI
Address Offset: CC-CFh
Default Value: 00000000h
Access: RO; RW; RWC
Size: 32 bits
BIOS Optimal Default 0000h

Bit	Access	Default Value	Description
31:16	RO	0h	**Reserved**
15	RO	0b	**PME Status (PMES):** This bit is set when a PME event is to be requested. Not supported.
14:9	RO	00h	**Reserved**
8	RO	0b	**PME Enable (PMEE):** Not Supported.
7:4	RO	0h	**Reserved**
3	RWC	0b	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized.
2	RO	0b	**Reserved**
1:0	RW	00b	**Power State (PS):** This field is used both to determine the current power state of the Intel® AMT function and to set a new power state. The values are: 00 – D0 state 11 – D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

22.4.20 MID - Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/3/PCI
Address Offset: D0-D1h
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Next Pointer (NEXT):** Value Indicates this is the last item in the list.
7:0	RO	05h	**Capability ID (CID):** Value of Capabilities ID indicates device is capable of generating MSI.

22.4.21 MC - Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/3/PCI
Address Offset: D2-D3h
Default Value: 0080h
Access: RO; RW
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	**Reserved**
7	RO	1b	**64-Bit Address Capable (C64):** Capable of generating 64-bit and 32-bit messages.
6:4	RW	000b	**Multiple Message Enable (MME):** These bits are R/W for software compatibility, but only one message is ever sent by the Intel® AMT function.
3:1	RO	000b	**Multiple Message Capable (MMC):** Only one message is required.
0	RW	0b	**MSI Enable (MSIE):** If set MSI is enabled and traditional interrupt pins are not used to generate interrupts.

22.4.22 MA - Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/3/PCI
Address Offset: D4-D7h
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:2	RW	00000000h	**Address (ADDR):** Lower 32 bits of the system specified message address, always Dworded.
1:0	RO	00b	**Reserved**

22.4.23 MAU - Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/3/PCI
Address Offset: D8-DBh
Default Value: 00000000h
Access: RO; RW
Size: 32 bits

Bit	Access	Default Value	Description
31:4	RO	0000000h	**Reserved**
3:0	RW	0000b	**Address (ADDR):** Upper 4 bits of the system specified message address.

22.4.24 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/3/PCI
Address Offset: DC-DDh
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RW	0000h	**Data (DATA):** This MSI data is driven onto the lower word of the data bus of the MSI memory write transaction.

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