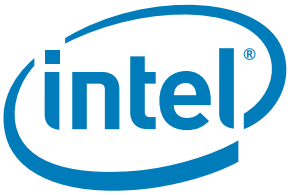
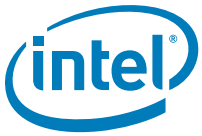


Intel® System Controller Hub (Intel® SCH)

Datasheet Addendum for US15WP and US15WPT

Febuary 2009



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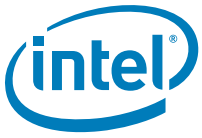
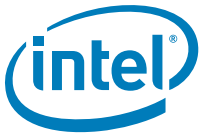
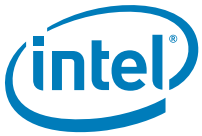


Tables



Revision History

Revision Number	Description	Revision Date
-001	•Initial release for Large Package Intel® SCH	Febuary 2009



1 Introduction

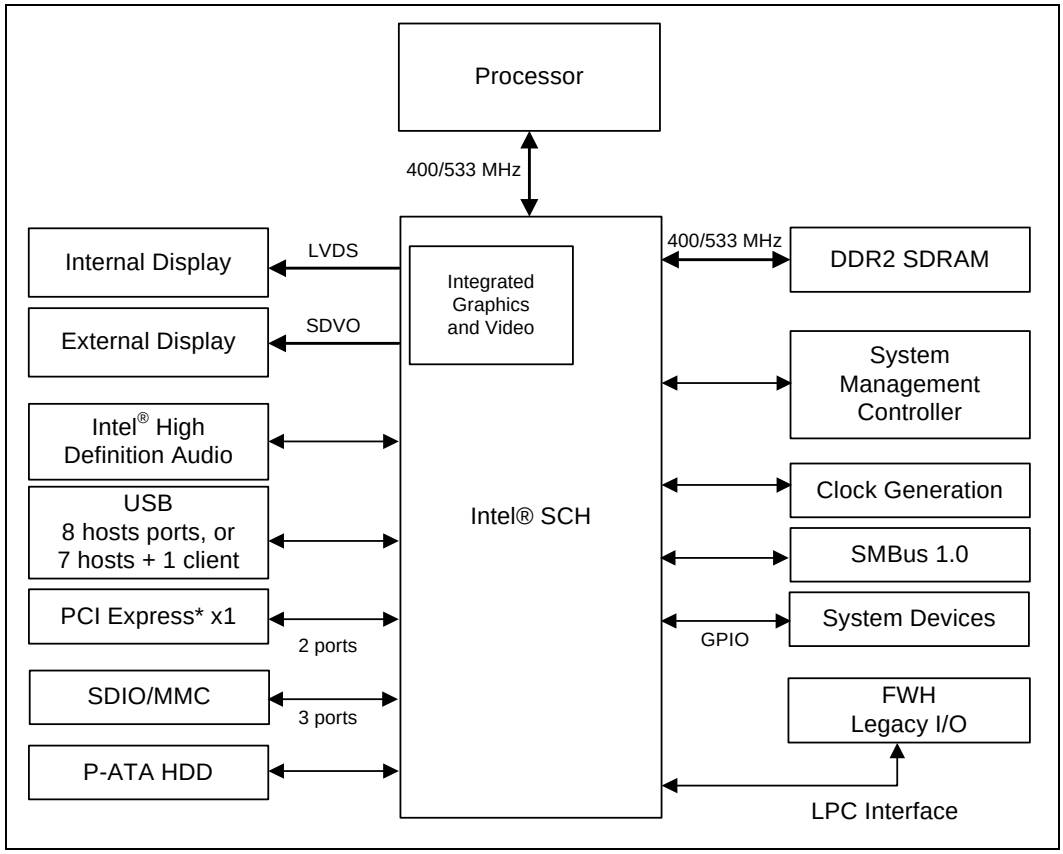
The Intel® System Controller Hub (Intel® SCH) chipset was designed to be used in conjunction with the Intel® Atom™ Z5xx series processor. The chipset combines functionality normally found in separate GMCH (integrated graphics, processor interface, memory controller) and ICH (on-board and end-user I/O expansion) components into a single component consuming less than 2.3 W of thermal design power. The System Controller Hub provides functionality necessary for traditional operating systems (such as Microsoft Windows XP*, Windows XPe*, Win CE* or Linux*) as well as functionality normally associated with handheld devices (such as SDIO/MMC and USB client). Figure 1 shows an example system block diagram. Section 1.3 provides an overview of the major features of the Intel® SCH.

This document is the datasheet addendum for the Intel® System Controller Hub (Intel® SCH) for SKUs US15WP and US15WPT. These SKUs provide the same functionality found in the smaller package SCH, but with a larger package that is easier to deal with. The “P” extension to the part number denotes that the part has a larger package then it’s small form factor counterpart, and the “T” extension to the part number denotes that the part supports the Industrial Temperature range. These larger package SCH SKUs were designed to be used in conjunction with the Intel® Atom™ Z5xxPx series processors. This addendum and datasheet contain signal description, system memory map, register descriptions, a description of the SCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

Caution: The datasheet addendum provides supplemental information to the *Intel® System Controller Hub (Intel® SCH) Datasheet* for the small form factor (SFF) package.

Warning: This document contains information on new products. The specifications are subject to change without notice. Please refer to the *Intel® System Controller Hub (SCH) Specification Update* for updates and verify with your local Intel Sales office that you have the latest document before finalizing a design.

Figure 1. System Block Diagram Example



1.1 Terminology

Table 1. Terminology

Term	Description
ACPI	Advanced Control Programmable Interface
ADD2	Advanced Digital Display 2. An interface specification that accepts serial DVO inputs and translates them into different display outputs such as DVO, TV-OUT, and LVDS.
Core	The internal base logic in the system controller hub.
Cold Reset	Full reset is when PWROK is deasserted and all system rails except VCCRTC are powered down
CRT	Cathode Ray Tube
CT	Commercial Temperature - 0 to 70°C
DBI	Dynamic Bus Inversion
DDR2	A second generation Double Data Rate SDRAM memory technology
DVI	Digital Video Interface. DVI is a specification that defines the connector and interface for digital displays.

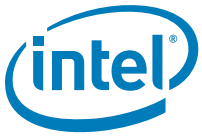


Table 1. Terminology

Term	Description
EHCI	Enhanced Host Controller Interface. A controller interface that, on Intel® SCH, supports up to eight USB 2.0 high-speed root ports, two of which are to be used internally only.
FSB	Front Side Bus. FSB is synonymous with host bus or processor bus
FWH	Firmware Hub
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. HDMI transmits all ATSC HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available through: http://www.hdmi.org/)
Host	This term is used synonymously with processor.
IGD	Internal Graphics Device. Generic name for a graphics accelerator that performs decoding of digital video signals.
Intel® GMA 500	Intel® Graphics Media Accelerator 500. A hardware accelerator for 2D and 3D graphics.
INTx	An interrupt request signal where “x” stands for interrupts A, B, C, and D
IT	Industrial Temperature - AEC-Q100 Grade 3: -40 to 85° C ambient
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling. LVDS is a high speed, low power data transmission standard used for display connections to LCD panels.
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express*	PCI Express* is a high-speed serial interface. The PCI Express* configuration is software compatible with the existing PCI specifications.
Processor	Intel® Atom™ processor
Rank	A unit of DRAM corresponding to number of SDRAM devices in parallel such that a full 64-bit data bus is formed.
Intel® SCH	Intel® System Controller Hub: a single-chip component that contains the processor interface, DDR2 SDRAM controller, Intel® GMA 500, various display interfaces, USB, SDIO, PCI Express*, PATA, LPC, and other I/O capabilities.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SD/SDIO	Secure Digital / Secure Digital Input Output Cards
SDVO	Serial Digital Video Out (SDVO). SDVO is a digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out).
SMC	Embedded Controller, or External Controller. Refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks.
SDVO Device	Third party codec that use SDVO as an input may have a variety of output formats, including DVI, LVDS, HDMI, TV-Out, etc.
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.

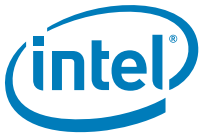


Table 1. Terminology

Term	Description
SMI	System Management Interrupt. SMI is used to indicate any of several system conditions (such as, thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface from Silicon Image* that is used in DVI and HDMI. TMDS is based on low-voltage differential signaling and converts an 8-bit signal into a 10-bit transition-minimized and DC-balanced signal (equal number of 0s and 1s) in order to reduce EMI generation and improve reliability.
TOLM	Top Of Low Memory. The highest address below 4 GB where a processor-initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.
UHCI	Universal Host Controller Interface. A controller interface that supports two USB 1.1 ports. The Intel® SCH contains three UHCI controllers.
UMA	Unified Memory Architecture. UMA describes an IGD using system memory for its frame buffers.
VCO	Voltage Controlled Oscillator
Warm Reset	Warm reset is when both RESET# and PWROK are asserted.

1.2 Reference Documents

Table 2. Reference documents

Document	Document number / Location
Intel® Atom™ Processor Z5xx Series Datasheet	319535
Intel® Atom™ Processor Z5xx Series Specification Update	319536
Intel® Atom™ Processor Z5xx Series Datasheet Addendum and Specification Update Addendum	321423
Intel® System Controller Hub (Intel® SCH) Datasheet	319537
Intel® System Controller Hub (SCH) Specification Update	319538
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
System Management Bus Specification, Version 1.0 (SMBus)	http://www.smbus.org/specs/
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Power Management Specification, Revision 1.1	http://www.pcisig.com/specifications
Advanced Configuration and Power Interface, Version 3.0 (ACPI)	http://www.acpi.info/
Universal Host Controller Interface, Revision 1.1 (UHCI)	http://download.intel.com/technology/usb/UHCI11D.pdf

Document	Document number/ Location
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Universal Serial Bus Specification (USB), Revision 2.0	http://www.usb.org/developers/docs
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0	http://www.intel.com/hardwaredesign/hpetspec_1.pdf

1.3 Overview

The Intel® SCH is designed for use with Intel® Atom™ processor-based platforms. The System Controller Hub connects to the processor as shown in Figure 1.

The Intel® SCH incorporates a variety of PCI functions as listed in Table 3.

Table 3. PCI Devices and Functions

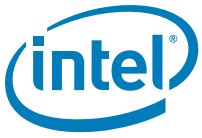
Device	Function	Function Description
0	0	Host Bridge
2	0	Integrated Graphics and Video Device
26	0	USB Client
27	0	Intel® High Definition Audio (Intel® HD Audio) Controller
28	0	PCI Express* Port 1
	1	PCI Express* Port 2
29	0	USB Classic UHCI Controller 1
	1	USB Classic UHCI Controller 2
	2	USB Classic UHCI Controller 3
	7	USB2 EHCI Controller
30	0	SDIO/MMC Port 0
	1	SDIO/MMC Port 1
	2	SDIO/MMC Port 2
31	0	LPC Interface
	1	PATA Controller

NOTE: All devices are on PCI Bus 0.

1.3.1 Processor Interface

The Intel® SCH supports the Intel® Atom™ processor Z5xxP series subset of the Enhanced Mode Scalable Bus Protocol, and implements a low-power CMOS bus. The System Controller Hub supports a single bus agent with FSB data rates of 400 MT/s and 533 MT/s. The Intel® SCH features include:

- Intel® Atom™ processor Z5xxPx series support
- CMOS frontside bus signaling for reduced power
- 400 MT/s or 533 MT/s data rate operation



- 64-Byte cache-line size
- 64-bit data bus, 32-bit address bus
- Supports one physical processor attachment with up to two logical processors
- 16 deep IOQ
- 1 deep defer queue
- FSB interrupt delivery
- Power-saving sideband control (DPWR#) for enabling/disabling processor data input sense amplifiers
- 1.05-V V_{TT} operation

1.3.2 System Memory Controller

The Intel® SCH integrates a DDR2 memory controller with a single 64-bit wide interface. Only DDR2 memory is supported. The memory controller interface is fully configurable through a set of control registers. Features of the Intel® SCH memory controller include:

- Supports 1.8 V DDR2 SDRAM, up to 2 ranks
- Supports 400 MT/s and 533 MT/s data rates
- Single 64-bit wide channel
- Single command per clock (1-N) operation
- Support for a maximum of 2GB of DRAM
- One or two rank operation
- Device density support for 512 Mb, 1024Mb, and 2084 Mb devices
- Device widths of x16
- Aggressive power management to reduce idle power consumption
- Page closing policies to proactively close pages after idle periods
- No on-die termination (ODT) support
- Supports non-terminated and board-terminated bus topologies

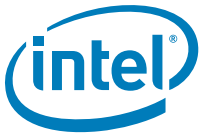
1.3.3 USB Host

The Intel® SCH contains three Universal Host Controller Interface (UHCI) USB 1.1 controllers and an Enhanced Host Controller Interface (EHCI) USB 2.0 controller. Port-routing logic on the system controller hub determines which USB controller is used to operate a given USB port.

A total of eight USB ports are supported. All eight of these ports are capable of high-speed data transfers up to 480MB/s, and six of the ports are also capable of full-speed and low-speed signaling. The two high-speed-only USB ports may only be used internally within the system platform.

1.3.4 USB Client

The Intel® SCH supports USB client functionality on port 2 of the USB interface. This permits the platform to attach to a separate USB host as a peripheral mass storage volume or RNDIS device.



1.3.5 PCI Express*

The Intel® SCH has two PCI Express* root ports supporting the *PCI Express Base Specification, Revision 1.0a*. PCI Express* root ports 1–2 can be statically configured as two x1 lanes. Each root port supports 2.5 Gb/s bandwidth in each direction.

An external graphics device can be used via one of the x1 PCI Express* lanes/ports.

1.3.6 LPC Interface

The Intel® SCH implements an LPC interface as described in the *LPC 1.1 Specification*. The LPC bridge function of the system controller hub resides in PCI Device 31: Function 0.

The LPC interface has three PCI-based clock outputs that may be provided to different I/O devices, such as Firmware Hub flash memory or a legacy I/O chip. The LPC_CLKOUT signals run at one-fourth the H_CLKINP/N frequency and support a total of six loads (two loads per clock pair) with no external buffering.

1.3.7 Parallel ATA (PATA)

The PATA Host Controller supports three types of data transfers:

- Programmed I/O (PIO): Processor is in control of the data transfer.
- Multi-word DMA (ATA-5): DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 66MB/s.
- Ultra DMA: Synchronous DMA protocol that redefines signals on the PATA cable to allow both host and target throttling of data and transfer rates up to 100MB/s. Ultra DMA 100/66/33 are supported.

The frequency of the PATA clock is one-fourth the host bus clock (H_CLKINP/N).

1.3.8 Intel® Graphics Media Accelerator 500

The Intel® SCH provides integrated graphics (2D and 3D) and high-definition video decode capabilities with minimal power consumption.

1.3.8.1 Graphics

The highly compact IGD contains an advanced shader architecture (model 3.0+) that performs pixel shading and vertex shading within a single hardware accelerator. The processing of pixels is deferred until they are determined to be visible, which minimizes access to memory and improves render performance.

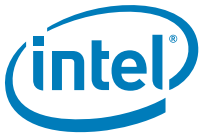
1.3.8.2 Video

The Intel® SCH supports full hardware acceleration of video decode standards such as H.264, MPEG2, MPEG4, VC1, and WMV9.

1.3.9 Display Interfaces

The IGD includes LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays, depending on SKU.

If external graphics is used instead of the internal graphics device, LVDS and SDVO ports will not function.



1.3.9.1 LVDS

The Intel® SCH supports a Low-Voltage Differential Signaling interface that allows the IGD to communicate directly to an on-board flat-panel display. The LVDS interface supports pixel color depths of 18 and 24 bits.

1.3.9.2 Serial DVO (SDVO) Display

The Intel® SCH has a digital display channel capable of driving SDVO adapters that provide interfaces to a variety of external display technologies (e.g., DVI, TV-Out, analog CRT).

SDVO lane reversal is not supported.

1.3.10 Secure Digital I/O (SDIO) / Multimedia Card (MMC) Controller

The Intel® SCH contains three SDIO/MMC expansion ports used to communicate with a variety of internal or external SDIO and MMC devices. Each port supports SDIO Revision 1.1 and MMC Revision 4.0 and is backward-compatible with previous interface specifications.

1.3.11 SMBus Host Controller

The Intel® SCH contains an SMBus host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices.

The system controller hub SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). See the *System Management Bus (SMBus) Specification,* Version 1.0.

1.3.12 Intel® High Definition Audio (Intel® HD Audio) Controller

The *Intel® High Definition Audio Specification* defines a digital interface that can be used to attach different types of codecs (such as audio and modem codecs). The Intel HD Audio controller supports up to four audio streams, two in and two out.

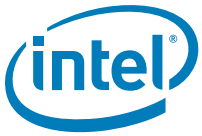
With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the Intel High Definition Audio (Intel HD Audio) controller provides audio quality that can deliver consumer electronic (CE) levels of audio experience. On the input side, the Intel® SCH adds support for an array of microphones.

The Intel HD Audio controller uses a set of DMA engines to effectively manage the link bandwidth and support simultaneous independent streams on the link. The capability enables new exciting usage models with Intel HD Audio (e.g., listening to music while playing a multi-player game on the Internet.) The Intel HD Audio controller also supports isochronous data transfers allowing glitch-free audio to the system.

1.3.13 General Purpose I/O (GPIO)

The Intel® SCH contains a total of 14 GPIO pins. Ten GPIOs are powered by the core power rail and are turned off during sleep modes (S3 and higher). The remaining four GPIOs are powered by the system controller hub suspend well power supply. These GPIOs and remain active during S3. The suspend well GPIOs can be used to wake the system from the Suspend-to-RAM state.

The GPIOs are not 5V tolerant.



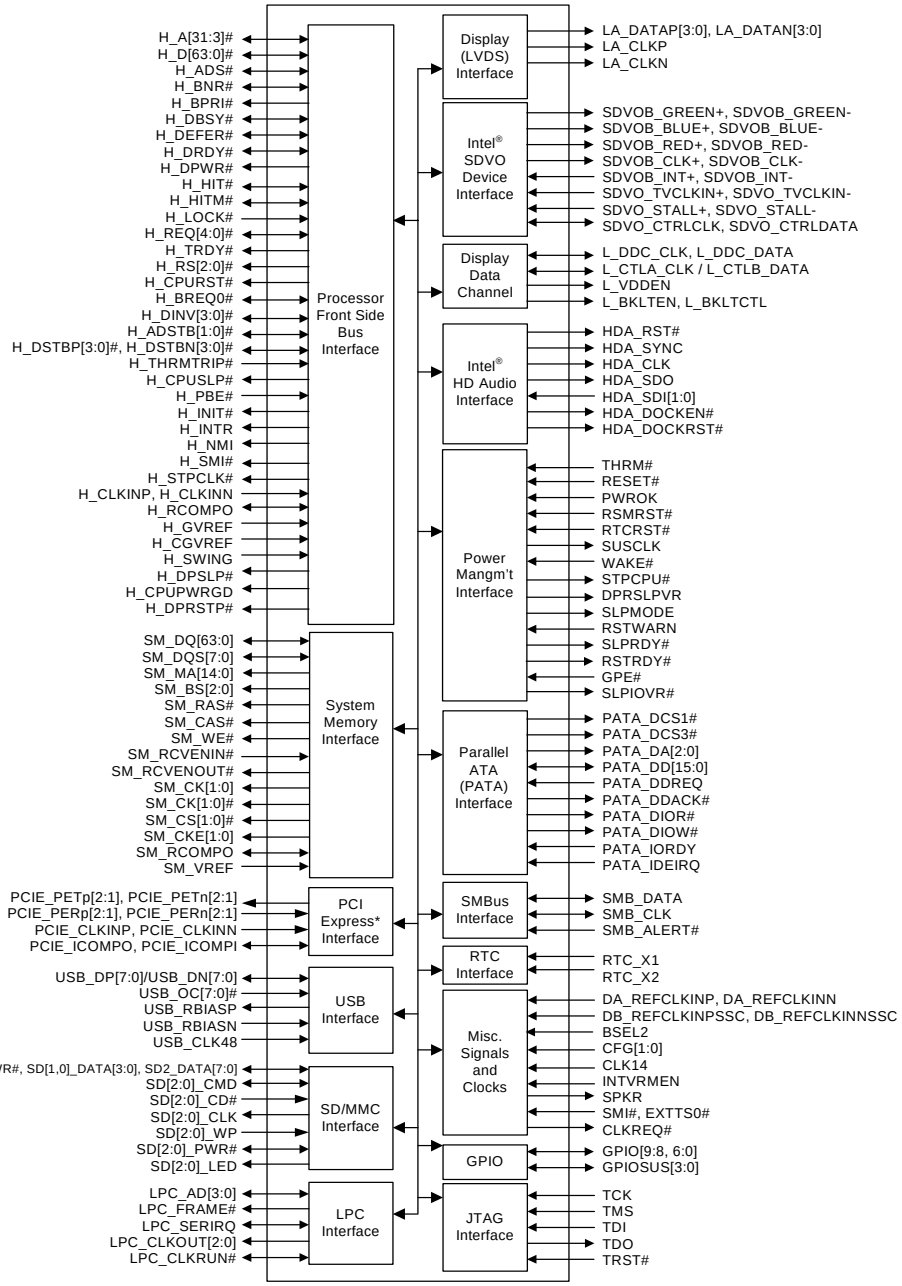
1.3.14 Power Management

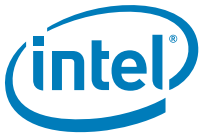
The Intel® SCH contains a mechanism to allow flexible configuration of various device maintenance routines as well as power management functions such as enhanced clock control and low-power state transitions (e.g., Suspend-to-RAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The system controller hub contains full support for the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 3.0.

2 Signal Description

This chapter provides a detailed description of the Intel® SCH signals and boot strap definitions. The signals are arranged in functional groups according to their associated interface (see Figure 2).

Figure 2. Signal Information Diagram





2.1 Host Interface Signals

Each signal description table has the following headings:

- **Signal**: The name of the signal/pin.
- **Type**: The buffer direction and type. Buffer direction can be either input, output, or I/O (bidirectional). See Table 4 for definitions of the different buffer types.
- **Power Well**: The power plane used to supply power to that signal. Choices are Core, DDR, Suspend, and RTC.
- **Description**: A brief explanation of the signal's function.

Table 4. Intel® SCH Signal Description (Sheet 1 of 4)

Signal	Type	Power Well	Description
H_ADS#	I/O AGTL+	Core	**Address Strobe:** The host bus owner asserts H_ADS# to indicate the first of two cycles of a request phase.
H_BNR#	I/O CMOS	Core	**Block Next Request:** This signal is used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
H_BPRI#	O CMOS	Core	**Priority Agent Bus Request:** The Intel® SCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the H_LOCK# signal was asserted.
H_BREQ0#	I/O CMOS	Core	**Bus Request 0#:** The Intel® SCH pulls the processor bus H_BREQ0# signal low during H_CPURST#. The signal is sampled by the processor on the active-to-inactive transition of H_CPURST#. H_BREQ0# should be tri-stated after the hold time requirement has been satisfied.
H_CPURST#	O CMOS	Core	**CPU Reset:** H_CPURST# allows the processor to begin execution in a known state. The Intel® SCH asserts H_CPURST# and deasserts H_CPUPWRGD upon exit from its reset. H_CPURST# is deasserted 2–10 ms after H_CPUPWRGD is asserted.
H_DBSY#	I/O AGTL+	Core	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
H_DEFER#	I/O CMOS	Core	**Defer:** The Intel® SCH will generate a deferred response as defined by the rules of the dynamic defer policy. The Intel® SCH will also use the H_DEFER# signal to indicate a processor retry response.

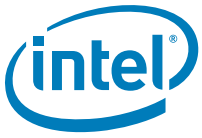


Table 4. Intel® SCH Signal Description (Sheet 2 of 4)

Signal	Type	Power Well	Description
H_DINV[3:0]#	I/O CMOS	Core	**Dynamic Bus Inversion:** These signals are driven along with the H_D[63:0]# signals. They indicate if the associated data bus signals are inverted or not. H_DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **H_DINV[x]# Data Bits** H_DINV3#H_D[63:48] H_DINV2#H_D[47:32] H_DINV1#H_D[31:16] H_DINV0#H_D[15:0]
H_DPWR#	O CMOS	Core	**Data Power:** Used by Intel® SCH to indicate that a data return cycle is pending within 2 host clock cycles or more. The processor uses this signal during a read-cycle to activate the data input buffers in preparation for H_DRDY# and the related data.
H_DRDY#	I/O AGTL+	Core	**Data Ready:** This signal is asserted for each cycle that data is transferred.
H_A[31:3]#	I/O CMOS	Core	**Host Address Bus:** H_A[31:3]# connect to the processor address bus. During processor cycles, H_A[31:3]# are inputs.
H_ADSTB[1:0]#	I/O AGTL+	Core	**Host Address Strobe:** The source synchronous strobes are used to transfer H_A[31:3]# and H_REQ[4:0]# at the 2x transfer rate. H_ADSTB0# maps to H_A[16:3]#, H_REQ[4:0]# H_ADSTB1# maps to H_A[31:17]#
H_D[63:0]#	I/O CMOS	Core	**Host Data:** These signals are connected to the processor data bus.
H_DSTBP[3:0]# H_DSTBN[3:0]#	I/O AGTL+	Core	**Host Data Strobes:** The source synchronous strobes used to transfer H_D[63:0]# and H_DINV[3:0]# at the 4x transfer rate. **Strobe Data Bits** H_DSTB[P/N]3#H_D[63:48]#, H_DINV3# H_DSTB[P/N]2# H_D[47:32]#, H_DINV2# H_DSTB[P/N]1# H_D[31:16]#, H_DINV1# H_DSTB[P/N]0# H_D[15:0]#, H_DINV0#
H_HIT#	I/O CMOS	Core	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with H_HITM# by the target to extend the snoop window.
H_HITM#	I/O CMOS	Core	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. This signal is also driven in conjunction with H_HIT# to extend the snoop window.
H_LOCK#	I CMOS	Core	**Host Lock:** All processor bus cycles sampled with the assertion of H_LOCK# and H_ADS#, until the negation of H_LOCK# must be atomic.

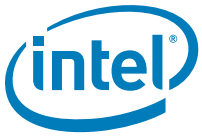


Table 4. Intel® SCH Signal Description (Sheet 3 of 4)

Signal	Type	Power Well	Description
H_REQ[4:0]#	I/O CMOS	Core	**Host Request Command:** These signals are asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
H_TRDY#	O CMOS	Core	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
H_RS[2:0]#	O CMOS	Core	**Response Signals:** These signals indicate the type of response as shown below: 000 = Idle State 001 = Retry Response 010 = Deferred Response 011 = Reserved (not driven by Intel® SCH) 100 = Hard Failure (not driven by Intel® SCH) 101 = No data response 110 = Implicit Writeback 111 = Normal data response
H_THRMTRIP#	I CMOS	Core	**Thermal Trip:** When low, this signal indicates that a thermal trip event from the processor occurred, and corrective action will be taken.
H_CPUSLP#	O CMOS	Core	**CPU SLP:** This signal puts the processor into a state that saves power vs. the Stop-Grant state. However, during that time, no snoops occur. The signal will go active for all other sleep states.
H_PBE#	I CMOS	Core	**Pending Break Event:** This signal can be used in some states for notification by the processor of pending interrupt events.
H_INIT#	O CMOS_OD	Core	**Initialization:** The Intel® SCH can be configured to support a special meaning to the CPU during H_CPURST# deassertion. H_INIT# functionality for resetting the CPU is not supported. This signal requires a board-level pull-up.
H_INTR	O CMOS	Core	**Processor Interrupt:** H_INTR is asserted by the Intel® SCH to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output normally driven low.
H_NMI	O CMOS	Core	**Non-Maskable Interrupt:** H_NMI is used to force a non-maskable interrupt to the processor. The processor detects the rising edge of H_NMI. A non-maskable interrupt is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register.
H_SMI#	O CMOS	Core	**System Management Interrupt:** H_SMI# is an active low output synchronous to LPC clock that is asserted by the Intel® SCH in response to one of many enabled hardware or software events.

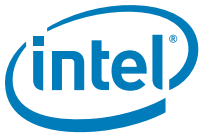
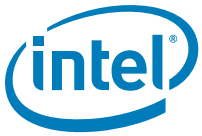


Table 4. Intel® SCH Signal Description (Sheet 4 of 4)

Signal	Type	Power Well	Description
H_STPCLK#	O CMOS	Core	**Stop Clock Request:** H_STPCLK# is an active-low output synchronous to LPC clock that is asserted by Intel® SCH in response to one of many hardware or software events. When the processor samples H_STPCLK# asserted, it responds by stopping its internal clock.
H_DPSLP#	O CMOS	Core	**Deep Sleep:** This signal is asserted by the Intel® SCH to the processor and system controller hub. When the signal is low, the processor enters the Deep Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deep Sleep state. This signal and the H_STPCLK# pin shut the clock in the processor and at the clock generator, respectively. The H_DPSLP# assertion time is wider than the H_STPCLK# assertion time in order for the processor to receive an active clock input whenever H_DPSLP# is deasserted.
H_DPRSTP#	O CMOS	Core	**Deeper Sleep:** When asserted on the platform, this signal causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. To return to the deep sleep state, H_DPRSTP# must be deasserted.
H_CPUPWRGD	O CMOS	Core	**CPU Power Good:** This signal is used for Enhanced Intel SpeedStep® technology support. H_CPUPWRGD goes to the processor. It is kept high during the Intel SpeedStep® technology state transition to prevent loss of processor context.
Host Interface Reference and Compensation			
H_CLKINP H_CLKINN	I CMOS 0.8	Core	**Differential clock Input for the Host PLL:** This low-voltage differential signal pair is used for FSB transactions. The clock input also supplies a signal to the internal core and memory interface clocks.
H_RCOMPO	I/O A	Core	**Host Resistor Compensation:** This is connected to a reference resistor to dynamically calibrate the driver strengths.
H_SWING	I A	Core	**Voltage Swing Calibration**
H_GVREF H_CGVREF	I A	Core	**Voltage Reference:** These pins are for the input buffer differential amplifier to determine a high versus a low input voltage.



2.2 System Memory Signals

Table 5. System Memory Signals (Sheet 1 of 2)

Signal	Type	Power Well	Description
SM_DQ[63:0]	I/O CMOS1.8	DDR	**Data Lines:** The SM_DQ[63:0] signals interface to the DRAM data bus.
SM_DQS[7:0]	I/O CMOS1.8	DDR	**Data Strobes:** These signals are the data strobes used for capturing data. Each strobe signal corresponds to 8 data bits. During writes, SM_DQSx is centered in data. During reads, SM_DQSx is edge aligned with data.
SM_MA[14:0]	O CMOS1.8	DDR	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SM_BS[2:0]	O CMOS1.8	DDR	**Bank Select (Bank Address):** These signals define which banks are selected within each SDRAM row. Bank select and memory address signals combine to address every possible location within an SDRAM device.
SM_RAS#	O CMOS1.8	DDR	**Row Address Strobe:** SM_RAS# is used to signify the presence of the row address on SM_MA[14:0] to the DRAM device being selected.
SM_CAS#	O CMOS1.8	DDR	**Column Address Strobe:** SM_CAS# is used to signify the presence of the column row address on SM_MA to the DRAM device being selected.
SM_WE#	O CMOS1.8	DDR	**Write Enable:** SM_WE# tells the DRAM memory that it is performing a write operation on the bus.
SM_RCVENIN#	I CMOS1.8	DDR	**Receive Enable In:** This signal connects to SM_SRCVENOUT# internally. This input (driven from SM_SRCVENOUT#) enables the DQS input buffers during reads.
SM_RCVENOUT#	O CMOS1.8	DDR	**Receive Enable Out:** This signal connects to SM_SRCVENIN# internally. It is part of the feedback used to enable the DQS input buffers during reads.
SM_CK[1:0] SM_CK[1:0]#	O CMOS1.8	DDR	**Differential DDR Clock:** SM_CKx and SM_CKx# pairs are differential clock outputs. The crossing of the positive edge of SM_CKx and the negative edge of SM_CKx# is used to sample the address and control signals on the DRAM.
SM_CS[1:0]#	O CMOS1.8	DDR	**Chip Select:** These signals select particular DRAM components during the active state. There is one SM_CSx# for each DRAM rank, toggled on the positive edge of SM_CKx

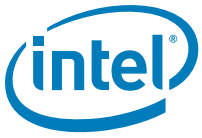


Table 5. System Memory Signals (Sheet 2 of 2)

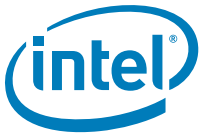
Signal	Type	Power Well	Description
SM_CKE[1:0]	O CMOS1.8	DDR	**Clock Enable:** SM_CKEx is used to initialize DRAM during power-up and to place all DRAM rows into and out of self-refresh during the S3 Suspend-to-RAM low power state. SM_CKEx is also used to dynamically power down inactive DRAM rows. There is one SM_CKEx per SDRAM row, toggled on the positive edge of SM_CKx.
SM_VREF	I A	DDR	**Input Buffer VREF:** This signal is for the input buffer differential amplifier to determine a high versus a low input voltage.
SM_RCOMPO	I/O A	DDR	**Resistor Compensation Output Pin:** This pin is connected to a reference resistor to calibrate the dynamically calibrate the driver strengths.

2.3 Integrated Display Interfaces

2.3.1 LVDS Signals

Table 6. LVDS Signals

Signal	Type	Power Well	Description
LA_DATAP[3:0] LA_DATAN[3:0]	O LVDS	Core	**Channel A Differential Data Output:** Differential signal pair.
LA_CLKP LA_CLKN	O LVDS	Core	**Channel A Differential Clock Output:** Differential signal pair.



2.3.2 Serial Digital Video Output (SDVO) Signals

Table 7. Serial Digital Video Output (SDVO) Signals

Signal Name	Type	Power Well	Description
SDVOB_RED+ SDVOB_RED-	O PCIe	Core	**Serial Digital Video Channel B Red:** SDVOB_RED[±] is a differential data pair that provides red pixel data for the SDVOB channel during Active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK[±] signal pair.
SDVOB_GREEN+ SDVOB_GREEN-	O PCIe	Core	**Serial Digital Video Channel B Green:** SDVOB_GREEN[±] is a differential data pair that provides green pixel data for the SDVOB channel during Active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK[±] signal pair.
SDVOB_BLUE+ SDVOB_BLUE-	O PCIe	Core	**Serial Digital Video Channel B Blue:** SDVOB_BLUE[±] is a differential data pair that provides blue pixel data for the SDVOB channel during Active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK[±] signal pair.
SDVOB_CLK+ SDVOB_CLK-	O PCIe	Core	**Serial Digital Video Channel B Clock:** This differential clock signal pair is generated by the Intel® SCH internal PLL and runs between 100 MHz and 200 MHz. If TV-out mode is used, the SDVO_TVCLKIN[±] clock input is used as the frequency reference for the PLL. The SDVOB_CLK[±] output pair is then driven back to the SDVO device.
SDVOB_INT+ SDVOB_INT-	I PCIe	Core	**Serial Digital Video Input Interrupt:** Differential input pair that may be used as an interrupt notification from the SDVO device to the Intel® SCH. This signal pair can be used to monitor hot plug attach/detach notifications for a monitor driven by an SDVO device.
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I PCIe	Core	**Serial Digital Video TV-OUT Synchronization Clock:** Differential clock pair that is driven by the SDVO device to the Intel® SCH. If SDVO_TVCLKIN[±] is used, it becomes the frequency reference for the system controller hub dot clock PLL, but will be driven back to the SDVO device through the SDVOB_CLK[±] differential pair. This signal pair has an operating range of 100–200 MHz, so if the desired display frequency is less than 100 MHz, the SDVO device must apply a multiplier to get the SDVO_TVCLKIN[±] frequency into the 100- to 200-MHz range.

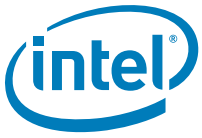


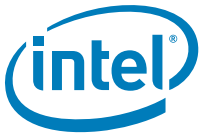
Table 7. Serial Digital Video Output (SDVO) Signals

Signal Name	Type	Power Well	Description
SDVO_STALL+ SDVO_STALL-	I PCIe	Core	**Serial Digital Video Field Stall:** Differential input pair that allows a scaling SDVO device to stall the Intel® SCH pixel pipeline.
SDVO_CTRLCLK	I/O CMOS3.3 _OD	Core	**SDVO Control Clock:** Single-ended control clock line from the Intel® SCH to the SDVO device. Similar to I^2C clock functionality, but may run at faster frequencies. SDVO_CTRLCLK is used in conjunction with SDVO_CTRLDATA to transfer device configuration, PROM, and monitor DDC information. This interface directly connects the system controller hub to the SDVO device.
SDVO_CTRLDATA	I/O CMOS3.3 _OD	Core	**SDVO Control Data:** SDVO_CTRLDATA is used in conjunction with SDVO_CTRLCLK to transfer device configuration, PROM, and monitor DDC information. This interface directly connects the Intel® SCH to the SDVO device.

2.3.3 Display Data Channel (DDC) and GMBUS Support

Table 8. Display Data Channel (DDC) and GMBUS Support

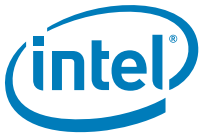
Signal Name	Type	Power Well	Description
L_DDC_CLK	I/O CMOS3.3 _OD	Core	**Display Data Channel Clock:** I^2C-based control signal (Clock) for EDID control
L_DDC_DATA	I/O CMOS3.3 _OD	Core	**Display Data Channel Data:** I^2C-based control signal (Data) for EDID control
L_CTLA_CLK	I/O CMOS3.3 _OD	Core	**Control A Clock**: This signal can be used to control external clock chip for SSC - optional
L_CTLB_DATA	I/O CMOS3.3 _OD	Core	**Control B Data**: This signal can be used to control external clock chip for SSC - optional
L_VDDEN	O CMOS3.3	Core	**LCD Power Enable:** This signal permits panel power enable control.
L_BKLTEN	O CMOS3.3	Core	**LCD Backlight Enable**: This signal permits panel backlight enable control.
L_BKLTCTL	O CMOS3.3	Core	**LCD Backlight Control:** This signal allows control of LCD brightness.



2.4 Universal Serial Bus (USB) Signals

Table 9. Universal Serial Bus (USB) Signals

Signal Name	Type	Power Well	Description
USB_DP[5:0]/ USB_DN[5:0]	I/O USB	Sus	**USB Port 5:0 Differentials: Bus Data/Address/ Command Bus:** These differential pairs are used to transmit data/address/command signals for ports 0 through 5. These ports can be routed to either the EHCI controller or one of the three UHCI controllers and are capable of running at either high, full, or low speed.
USB_DP[7:6]/ USB_DN[7:6]	I/O USB	Sus	**USB Port 7:6 Differentials: Bus Data/Address/ Command Bus:** These differential pairs are used to transmit data/address/command signals for ports 6 and 7. These ports are routed only to the EHCI controller and should be used ONLY for in-system USB 2.0 devices.
USB_RBIASP	O A	Sus	**Resistor Bias P:** This pin is an analog connection point for an external resistor. This signal is used to set transmit currents and internal load resistors.
USB_RBIASN	I A	Sus	**Resistor Bias N:** This pin is an analog connection point for an external resistor. This signal is used to set transmit currents and internal load resistors.
USB_CLK48	I USB	Sus	**48-MHz Clock:** This optional clock is used to run the USB controller. By default, the Intel® SCH uses DA_REFCLKIN to clock the USB logic.
USB_OC[7:0]#	I CMOS3.3	Sus	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. USB_OC[7:0]# are not 5-V tolerant.
USBCC/ GPIOSUS3	I/O CMOS3.3	Sus	**USB Client Connect:** This signal, on GPIOSUS3, may be used in systems where USB port 2 is configured for client mode. This indicates connection to an external USB host has been established. **NOTE:** If USB Client support is enabled, then this signal is dedicated for USB Client Connect.



2.5 PCI Express* Signals

Table 10. PCI Express* Signals

Signal Name	Type	Power Well	Description
PCIE_PETp[2:1] PCIE_PETn[2:1]	O PCIe	Core	**PCI Express* Transmit:** PCIE_PETp[2:1] are PCI Express ports 2:1 transmit pair (P and N) signals.
PCIE_PERp[2:1] PCIE_PERn[2:1]	I PCIe	Core	**PCI Express Receive:** PCIE_PERp[2:1] PCI Express ports 2:1 receive pair (P and N) signals.
PCIE_CLKINP PCIE_CLKINN	I PCIe	Core	**PCI Express Input Clock:** 100 MHz differential clock signals.
PCIE_ICOMPO	I/O A	Core	**PCI Express Compensation Pin:** Output compensation for both current and resistance. Also provides buffer compensation for the LVDS and SDVO buffers.
PCIE_ICOMPI	I/O A	Core	**PCI Express Compensation Pin:** Input compensation for current. Also provides buffer compensation for the LVDS and SDVO buffers.

2.6 Secure Digital I/O (SDIO)/MultiMedia Card (MMC) Signals

Table 11. Secure Digital I/O (SDIO)/MultiMedia Card (MMC) Signals (Sheet 1 of 2)

Signal Name	Type	Power Well	Description
SD0_DATA[3:0] SD1_DATA[3:0] SD2_DATA[7:0]	I/O CMOS3.3	Core	**SDIO Controller 0/1/2 Data:** These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SDn_DATA0 is used for data transfer. Wider data bus widths can be configured for data transfer. **NOTE:** Port 0 and 1 are 4 bits wide while ports 2 is 8 bits wide.
SD0_CMD SD1_CMD SD2_CMD	I/O CMOS3.3	Core	**SDIO Controller 0/1/2 Command:** This signal is used for card initialization and transfer of commands. It has two operating modes: open-drain for initialization mode, and push-pull for fast command transfer.
SD0_CLK SD1_CLK SD2_CLK	O CMOS3.3	Core	**SDIO Controller 0/1/2 Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal is generated by Intel® SCH at a maximum frequency of: 24 Mhz for SD and SDIO. 48 Mhz for MMC.
SD0_WP SD1_WP SD2_WP	I CMOS3.3	Core	**SDIO Controller 0/1/2 Write Protect**: These signals denote the state of the write-protect tab on SD cards.

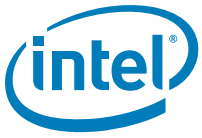


Table 11. Secure Digital I/O (SDIO)/MultiMedia Card (MMC) Signals (Sheet 2 of 2)

Signal Name	Type	Power Well	Description
SD0_CD# SD1_CD# SD2_CD#	I CMOS3.3	Core	**SDIO Controller 0/1/2 Card Detect:** This signal indicates when a card is present in an external slot.
SD0_LED SD1_LED SD2_LED	O CMOS3.3	Core	**SDIO Controller 0/1/2 LED:** This signal can be used to drive an external LED and indicate when transfers are occurring on the bus.
SD0_PWR# SD1_PWR# SD2_PWR#	I/O CMOS3.3	Core	**SDIO/MMC Power Enable:** These pins can be used to enable the power being supplied to an SDIO/MMC device.

2.7 Parallel ATA (PATA) Signals

Table 12. Parallel ATA (PATA) Signals (Sheet 1 of 2)

Signal Name	Type	Power Well	Description
PATA_DD[15:0]	I/O CMOS3.3-5	Core	**Device Data:** These signals drive the corresponding signals on the PATA connector. There is an internal 13.3-kΩ pull-down on PATA_DD7.
PATA_DA[2:0]	O CMOS3.3-5	Core	**Device Address:** These output signals are connected to the corresponding signals on the PATA connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.
PATA_DIOR#	O CMOS3.3-5	Core	**Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the PATA device that it may drive data onto the DD lines. Data is latched by the Intel® SCH on the deassertion edge of PATA_DIOR#. The PATA device is selected either by the ATA register file chip selects (PATA_DCS1# or PATA_DCS3#) and the PATA_DA lines, or the PATA DMA acknowledge (PATA_DDAK#).
PATA_DIOW#	O CMOS3.3-5	Core	**Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the PATA device that it may latch data from the PATA_DD lines. Data is latched by the PATA device on the deassertion edge of PATA_DIOW#. The PATA device is selected either by the ATA register file chip selects (PATA_DCS1# or PATA_DCS3#) and the PATA_DA lines, or the PATA DMA acknowledge (PATA_DDAK#).
PATA_DDACK#	O CMOS3.3-5	Core	**Device DMA Acknowledge:** This signal directly drives the DAK# signals on the PATA connectors. Each is asserted by the Intel® SCH to indicate to PATA DMA slave devices that a given data transfer cycle (assertion of PATA_DIOR# or PATA_DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master PATA function and are not associated with any AT-compatible DMA channel.

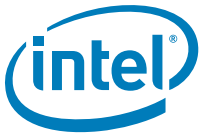


Table 12. Parallel ATA (PATA) Signals (Sheet 2 of 2)

Signal Name	Type	Power Well	Description
PATA_DCS3#	O CMOS3.3-5	Core	**Device Chip Select for 300 Range:** This chip select is for the ATA control register block. This is connected to the corresponding signal on the connector.
PATA_DCS1#	O CMOS3.3-5	Core	**Device Chip Selects for 100 Range:** This chip select is for the ATA command register block. This is connected to the corresponding signal on the PATA connector.
PATA_DDREQ	I CMOS3.3-5	Core	**Device DMA Request:** This input signal is directly driven from the DRQ signals on the PATA connector. It is asserted by the PATA device to request a data transfer, and used in conjunction with the PCI bus master PATA function and are not associated with any AT compatible DMA channel. There is an internal 13.3 kΩ pull-down on this pin.
PATA_IORDY	I CMOS3.3-5	Core	**I/O Channel Ready (PIO):** This signal will keep the strobe active (PATA_DIOR# on reads, PATA_DIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers.
PATA_IDEIRQ	I CMOS3.3-5	Core	**IDE Interrupt**: Input from the PATA device indicating request for an interrupt. Tied internally to IRQ14.

2.8 Intel® High Definition Audio (Intel® HD Audio) Interface

Table 13. Intel® High Definition Audio (Intel® HD Audio) Interface (Sheet 1 of 2)

Signal Name	Type	Power Well	Description
HDA_RST#	O CMOS_HDA	Core	**Intel HD Audio Reset:** This signal is the reset to external codec(s)
HDA_SYNC	O CMOS_HDA	Core	**Intel HD Audio Sync:** This signal is an 48-kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.
HDA_CLK	O CMOS_HDA	Core	**Intel HD Audio Clock (Output):** This signal is a 24.000-MHz serial data clock generated by the Intel High Definition Audio (Intel HD Audio) controller. This signal contains an integrated pull-down resistor so that it does not float when an Intel HD Audio codec (or no codec) is connected.
HDA_SDO	O CMOS_HDA	Core	**Intel HD Audio Serial Data Out:** This signal is a serial TDM data output to the codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio.

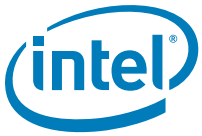


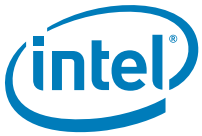
Table 13. Intel® High Definition Audio (Intel® HD Audio) Interface (Sheet 2 of 2)

Signal Name	Type	Power Well	Description
HDA_SDI[1:0]	I CMOS_HDA	Core	**Intel® HD Audio Serial Data In:** These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.
HDA_DOCKEN#	O CMOS_HDA	Core	**Intel HD Audio Dock Enable:** This active low signal controls the external Intel HD Audio docking isolation logic. When deasserted, the external docking switch is in isolate mode. When asserted, the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Intel® SCH signals.
HDA_DOCKRST#	O CMOS_HDA	Core	**Intel HD Audio Dock Reset:** This signal is a dedicated reset signal for the codec(s) in the docking station. It works similar to, but independent of, the normal HDA_RST# signal.

2.9 LPC Interface

Table 14. LPC Interface

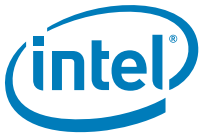
Signal Name	Type	Power Well	Description
LPC_AD[3:0]	I/O CMOS3.3	Core	**LPC Address/Data:** Multiplexed Command, Address, Data
LPC_FRAME#	O CMOS3.3	Core	**LPC Frame:** This signal indicates the start of an LPC/FHW cycle.
LPC_SERIRQ	I/O CMOS3.3	Core	**Serial Interrupt Request:** This signal conveys the serial interrupt protocol.
LPC_CLKRUN#	I/O CMOS3.3	Core	**Clock Run:** This signal gates the operation of the LPC_CLKOUTx. Once an interrupt sequence has started, LPC_CLKRUN# should remain asserted to allow the LPC_CLKOUTx to run.
LPC_CLKOUT[2:0]	O CMOS3.3	Core	**LPC Clock:** These signals are the clocks driven by the Intel® SCH to LPC devices. Each clock can support up to two loads. **Note:** Primary boot device such (behind SMC) should be connected to LPC_CLKOUT[0]



2.10 SMBus Interface

Table 15. SMBus Interface

Signal Name	Type	Power Well	Description
SMB_DATA	I/O CMOS3.3 _OD	Core	**SMBus Data:** This signal is the SMBus data pin. An external pull-up resistor is required.
SMB_CLK	I/O CMOS3.3 _OD	Core	**SMBus Clock:** This signal is the SMBus clock pin. An external pull-up resistor is required.
SMB_ALERT#	I CMOS3.3 _OD	Core	**SMBus Alert:** This signal can be used to wake the system, generate an interrupt, or generate an SMI#.



2.11 Power Management Interface

Table 16. Power Management Interface (Sheet 1 of 2)

Signal Name	Type	Power Well	Description
THRM#	I CMOS3.3	Core	**Thermal Alarm:** This signal is an active low signal generated by external hardware to generate an SMI or SCI.
RESET#	I CMOS3.3	DDR	**System Reset:** This signal forces a reset after being de-bounced. This signal is powered by V_{CCSM}.
PWROK	I CMOS3.3	RTC	**Power OK:** When asserted, PWROK is an indication to the Intel® SCH that core power is stable. PWROK can be driven asynchronously.
RSMRST#	I CMOS3.3	RTC	**Resume Well Reset:** This signal is used for resetting the resume well. An external RC circuit is required to ensure that the resume well power is valid prior to RSMRST# going high.
RTCRST#	I CMOS3.3	RTC	**RTC Well Reset:** This signal is normally held high (to VCC_RTC), but can be driven low on the motherboard to test the RTC power well and reset some bits in the RTC well registers that are otherwise not reset by SLPMODE or RSMRST#. An external RC circuit on the RTCRST# signal creates a time delay such that RTCRST# will go high some time after the battery voltage is valid. This allows the Intel® SCH to detect when a new battery has been installed. The RTCRST# input must always be high when other non-RTC power planes are on. This signal is in the RTC power well.
SUSCLK	O CMOS3.3	Sus	**Suspend Clock:** This signal is an output of the RTC generator circuit (32.768 kHz). SUSCLK can have a duty cycle from 30% to 70%.
WAKE#	I CMOS3.3	Sus	**PCI Express* Wake Event:** This signal indicates a PCI Express port wants to wake the system.
STPCPU#	O CMOS3.3	Core	**Stop the CPU Clock:** This signal is used to support the C3 state. Asserting this signal halts the clocks to the processor by controlling the enable clock chip.
DPRSLPVR	O CMOS3.3	Core	**Deeper Sleep Voltage Regulator:** This signal is asserted by the Intel® SCH to the processor's voltage regulator. When the signal is high, the voltage regulator outputs the lower "Deeper Sleep" voltage. When the signal is low (default), the voltage regulator outputs the higher "Normal" voltage. This signal is in the core I/O plane and has a standard CMOS output (not open drain).
SLPIOVR#	O CMOS3.3	Core	**Sleep I/O Voltage Regulator Disable:** The SLPIOVR# can be connected to an external VR and be used to control power supplied to the processor's I/O rail during the C6 state.

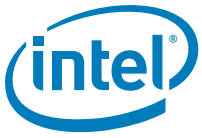


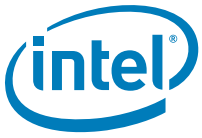
Table 16. Power Management Interface (Sheet 2 of 2)

Signal Name	Type	Power Well	Description
SLPMODE	O CMOS3.3	Sus	**Sleep Mode:** SLPMODE determines which sleep state is entered. When SLPMODE is high, S3 will be chosen. When SLPMODE is low, S4/S5 will be the selected sleep mode.
RSTWARN	I CMOS3.3	Sus	**Reset Warning**: Asserting the RSTWARN signal forces the Intel® SCH to enter a sleep state or begin to power down. A system management controller might do so after an external event, such as pressing of the power button or occurrence of a thermal event.
SLPRDY#	O CMOS3.3	Sus	**Sleep Ready**: The Intel® SCH will drive the SLPRDY# signal low to indicate to the system management controller that the system controller hub is awake and able to placed into a sleep state. Deassertion of this signal indicates that a wake is being requested from a system device.
RSTRDY#	O CMOS3.3	Sus	**Reset Ready**: Assertion of the RSTRDY# signal indicates to the system management controller that it is ready to be placed into a low power state. During a transition from S0 to S3/4/5 sleep states, the Intel® SCH asserts RSTRDY# and CPURST# after detecting assertion of the RSTWARN signal from the external system management controller.
GPE#	I CMOS3.3 _OD	Sus	**General Purpose Event**: GPE# is asserted by an external device (typically, the system management controller) to log an event in the Intel® SCH ACPI space and cause an SCI (if enabled).

2.12 Real Time Clock Interface

Table 17. Real Time Clock Interface

Signal Name	Type	Power Well	Description
RTC_X1	Special A	RTC	**Crystal Input 1:** This signal is connected to the 32.768-kHz crystal. If no external crystal is used, then RTC_X1 can be driven with the desired clock rate.
RTC_X2	Special A	RTC	**Crystal Output 2:** This signal is connected to the 32.768-kHz crystal. If no external crystal is used, then RTC_X2 should be left floating.



2.13 JTAG Interface

The JTAG interface is accessible only after PWROK is asserted.

Table 18. JTAG Interface

Signal Name	Type	Power Well	Description
TCK	I CMOS	Sus	**JTAG Test Clock:** TCK is a clock input used to drive Test Access Port (TAP) state machine during test and debugging. This input may change asynchronous to the host clock.
TDI	I CMOS	Sus	**JTAG Test Data In:** TDI is used to serially shift data and instructions into the TAP.
TDO	O CMOS_OD	Sus	**JTAG Test Data Out:** TDO is used to serially shift data out of the device.
TMS	I CMOS	Sus	**Test Mode Select:** This signal is used to control the state of the TAP controller.
TRST#	I CMOS	Sus	**Test Reset:** This signal resets the controller logic. It should be pulled down unless TCK is active.

2.14 Miscellaneous Signals and Clocks

Table 19. Miscellaneous Signals and Clocks (Sheet 1 of 2)

Signal Name	Type	Power Well	Description
DA_REFCLKINP/ DA_REFCLKINN	I	Core	**Display PLLA CLK Differential Pair:** 96 MHz, no SSC support.
DB_REFCLKINPSSC/ DB_REFCLKINNSSC	I	Core	**Display PLLB CLK Differential Pair:** display PLL differential clock pair for SSC support.
CLKREQ#	O CMOS3.3 _OD	Core	**Clock Required**: The SCH will not assert CLKREQ# to enable a power management mode to the clock chip.
CLK14	I CMOS3.3	Core	**Oscillator Clock:** This signal is used for 8254 timers and HPETs. It runs at 14.31818 MHz. This clock stops (and should be low) during S3, S4, and S5 states. CLK14 must be accurate to within 500 ppm over 100 µs (and longer periods) to meet HPET accuracy requirements.
INTVRMEN	I CMOS3.3	RTC	**Internal VRM Enable:** This signal is used to enable or disable the integrated 1.5-V Voltage Regulators for the Suspend and Auxiliary wells on the Intel® SCH. When connected to V_{SS}, the VRMs are disabled; when connected to the RTC power well, the VRMs are enabled. This signal is in the RTC well. It is not latched and must remain valid for the VRMs to behave properly.

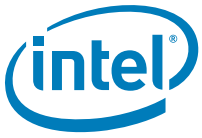


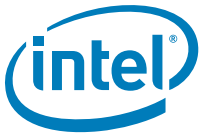
Table 19. Miscellaneous Signals and Clocks (Sheet 2 of 2)

Signal Name	Type	Power Well	Description
SPKR	O CMOS3.3	Core	**Speaker:** The SPKR signal is the output of counter 2 and is internally ANDed with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon SLPMODE, its output state is 0.
SMI#	I CMOS3.3	Core	**System Management Interrupt:** This signal is generated by the external system management controller.
EXTTS0#	I CMOS3.3	Core	**External Thermal Sensor 0 Event:**
EXTTS1#/GPIO9	I CMOS3.3	Core	**External Thermal Sensor 1 Event:** EXTTS1# is multiplexed with GPIO9.
BSEL2	I CMOS	Core	**Host Bus Speed Select:** At the deassertion of RESET#, the value sampled on BSEL2 determines the expected frequency of the bus. Refer to Table 22 for more details.
CFG[1:0]	I CMOS	Core	**Configuration:** Strap pins used to configure the graphics/display clock frequency. Refer to Table 22 for more details.

2.15 General Purpose I/O

Table 20. General Purpose I/O

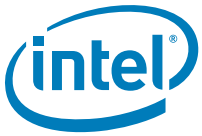
Signal Name	Type	Power Well	Description
GPIO9/EXTTS1#	I/O CMOS3.3	Core	**General Purpose I/O #9 / External Thermal Sensor 1:** This GPIO can function as a second external thermal sensor input.
GPIO8/ PROCHOT#	I/O CMOS3.3 / OD	Core	**General Purpose I/O #8 / Processor Hot:** Defaults to a GPIO. As PROCHOT#, this signal can function as an Open-Drain output to the CPU or SMC to signify a processor thermal event.
GPIO[6:0]	I/O CMOS3.3	Core	**General Purpose I/O:** These signals are powered off of the core well power plane within the Intel® SCH.
GPIOSUS3/ USBCC	I/O CMOS3.3	Sus	**Resume Well General Purpose I/O #3/USB Client Connect:** This GPIO can function as an input signifying connection to an external USB host. **Note:** If a USB Client is enabled in the system, then GPIOSUS3 cannot be used as a general purpose I/O.
GPIOSUS[2:0]	I/O CMOS3.3	Sus	**General Purpose I/O:** These signals are powered from the suspend well power plane within the Intel® SCH. They are accessible during the S3 sleep state.



2.16 Power and Ground Signals

Table 21. Power and Ground Signals

Interface	Ball Name	Nominal Voltage	Description
Common	VCC	1.05	Core supply
	VSS	0	Ground
Host	VTT	1.05	Used for FSB input and output devices
	VCCAHPLL	1.5	Analog Power Supply
	VCCDHPLL	1.5	Digital Power Supply
DDR2	VCCSM	1.8 1.5	Driver and Receiver supply Configurable for 1.8-V/1.5-V operation
SDVO/ PCIe/ LVDS	VCCLVDS	1.5	Dedicated LVDS supply (must be supplied regardless of LVDS usage).
	VCCSDVO	1.5	Dedicated SDVO supply (must be supplied regardless of SDVO usage).
	VCCPCIE	1.5	Dedicated PCIe analog/digital supply.
	VCCAPCIEPLL	1.5	PCIe PLL.
	VCCAPCIEBG	3.3	Band Gap (needs to be enabled for PCIe, SDVO or LVDS).
	VSSAPCIEBG	0	PCIe Band Gap VSS.
Display PLL	VCCADPLLA	1.5	Display PLL A power supply (digital and analog) Must be powered even if DPLLA isn't used.
	VCCADPLLB	1.5	Display PLL B power supply (digital and analog) Must be powered even if DPLLB isn't used.
Intel® High Definition Audio	VCC15	1.5	Used for I/O digital logic
	VCCHDA	3.3/1.5	Configurable for 3.3-V or 1.5-V operation
	VCC33	3.3	Used for some internal 3.3-V circuits
SDIO/MMC/ CMOS/LPC/ PATA	VCC15	1.5	Used for I/O digital logic
	VCC33	3.3	Used for I/O analog driver
	VCC5REF	5	Used for 5-V tolerance on core group inputs
USB	VCCAUSBPLL	1.5	USB PLL Supply. Must be powered even if USB is not used
	VCC15USB	1.5	Power for USB Logic and Analogs.
	VCCP33USBSUS	3.3	USB 3.3-V Supply
	VCCAUSBBGSUS	3.3	USB Band Gap
	VSSAUSBBGSUS	0	USB Band Gap VSS
	VCC5REFSUS	5	5-V supply in suspend power well
CMOS Suspend	VCC33SUS	3.3	3.3-V suspend Power Supply
	VCC33RTC	3.3	Used for Real Time Clock

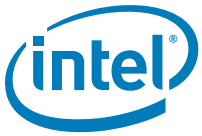


2.17 Functional Straps

The following signals are used to configure certain Intel® SCH features. All strap signals are in the core power well. They are sampled at the rising edge of PWROK and then revert later to their normal usage. Straps should be driven to the desired state at least four LPC (PCI) clocks prior to the rising edge of PWROK.

Table 22. Functional Strap Definitions

<table>
<tr><th>Signal Name</th><th>Strap Function</th><th>Comments</th></tr>
<tr><td>BSEL2 and CFG[1:0]</td><td>FSB/DDR Frequency Select
Graphics Frequency Select</td><td>BSEL2: Selects the frequency of the host interface and DDR interface. Normal system configuration will have this signal connected to the processor's BSEL2 signal and will not require external pull-up/pull-down resistors.
CFG[1:0]: Selects the frequency of the internal graphics device.
<table><tr><th>BSEL2</th><th>CFG1</th><th>CFG0</th><th>FSB Freq</th><th>GFX Freq</th></tr><tr><td>1</td><td>0</td><td>0</td><td>100 MHz</td><td>200 MHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>133 MHz</td><td>200 MHz</td></tr></table>All other combinations are reserved</td></tr>
<tr><td>GPIO3
GPIO0</td><td>CMC (Chipset Microcode) Base Address</td><td>Selects the starting address that the CMC will use to start fetching code (GPIO3 is the most significant).
<table><tr><th>GPIO3</th><th>GPIO0</th><th>CMC Base Address</th></tr><tr><td>0</td><td>0</td><td>FFFB0000h</td></tr><tr><td>0</td><td>1</td><td>FFFC0000h</td></tr><tr><td>1</td><td>0</td><td>FFFD0000h (default)</td></tr><tr><td>1</td><td>1</td><td>FFFE0000h</td></tr></table></td></tr>
<tr><td>RESERVED1</td><td>LPC_CLKOUT[0] Buffer Strength</td><td>Selects the drive strength of the LPC_CLKOUT0 clock.
0 = 1 Load driver strength
1 = 2 Load driver strength</td></tr>
<tr><td>XOR_TEST</td><td>XOR Chain Enable</td><td>Enables XOR chain mode
0 = XOR mode enable
1 = XOR mode disable (default)</td></tr>
</table>



3 Pin States

This chapter describes the states of each Intel® SCH signal in and around reset. It also documents what signals have internal pull-up/pull-down/series termination resistors and their values.

3.1 Pin Reset States

Table 23. Reset State Definitions

Signal State	Description
High-Z	The Intel® SCH places this output in a high-impedance state. For I/O's, external drivers are not expected.
Don't Care	The state of the input (driven or tri-stated) does not effect the Intel® SCH. For I/O it is assumed the output buffer is in a high-impedance state.
VOH	The Intel® SCH drives this signal high
VOL	The Intel® SCH drives this signal low
VOX-known	The Intel® SCH drives this signal to a level defined by internal function configuration
VOX-unknown	The Intel® SCH drives this signal, but to an indeterminate value
VIH	The Intel® SCH expects/requires the signal to be driven high
VIL	The Intel® SCH expects/requires the signal to be driven low
pull-up	This signal is pulled high by a pull-up resistor (internal or external)
pull-down	This signal is pulled low by a pull-down resistor (internal or external)
VIX-unknown	The Intel® SCH expects the signal to be driven by an external source, but the exact electrical level of that input is unknown.
Running	The clock is toggling or signal is transitioning because the function has not stopped.
Off	The power plane for this signal is powered down. The Intel® SCH does not drive outputs and inputs should not be driven to the Intel® SCH.

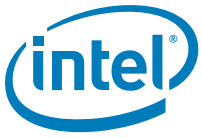


Table 24. Intel® SCH Reset State (Sheet 1 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
Host Interface					
H_A[31:3]#	I/O	VOH	pull-up	Off	Off
H_D[63:0]#	I/O	VOH	pull-up	Off	Off
H_ADS#	I/O	VOH	pull-up	Off	Off
H_BNR#	I/O	VOH	pull-up	Off	Off
H_BPRI#	O	VOH	pull-up	Off	Off
H_DBSY#	I/O	VOH	pull-up	Off	Off
H_DEFER#	I/O	VOH	pull-up	Off	Off
H_DRDY#	I/O	VOH	pull-up	Off	Off
H_DPWR#	O	VOH	VOL	Off	Off
H_HIT#	I/O	VOH	pull-up	Off	Off
H_HITM#	I/O	VOH	pull-up	Off	Off
H_LOCK#	I	VIH	pull-up	Off	Off
H_REQ[4:0]#	I/O	VOH	pull-up	Off	Off
H_CPUSLP#	O	VOH	VOH	Off	Off
H_TRDY#	O	VOH	pull-up	Off	Off
H_RS[2:0]#	O	VOH	pull-up	Off	Off
H_CPURST#	O	VOL	pull-up	Off	Off
H_BREQ0#	I/O	VIL	pull-up	Off	Off
H_DINV[3:0]#	I/O	VOH	pull-up	Off	Off
H_ADSTB[1:0]#	I/O	VOH	pull-up	Off	Off
H_DSTBP[3:0]#, H_DSTBN[3:0]#	I/O	VOH	pull-up	Off	Off
H_THERMTRIP	I	VIX-unknown	pull-up	Off	Off
H_PBE#	I	VIH	pull-up	Off	Off
H_INIT#	O	VOX-unknown	pull-up	Off	Off
H_INTR	O	VOL	VOL	Off	Off
H_NMI	O	VOL	VOL	Off	Off
H_SMI#	O	VOH	VOH	Off	Off
H_STPCLK#	O	VOH	VOH	Off	Off
H_CLKINP, H_CLKINN	I	Running	Running	Off	Off
H_RCOMPO	I/O-A	High-Z	High-Z	Off	Off
H_GVREF	I-A	VIX-unknown	VIX-unknown	Off	Off
H_GCVREF	I-A	VIX-unknown	VIX-unknown	Off	Off
H_SWING	I-A	VIX-unknown	VIX-unknown	Off	Off
H_DPSLP#	O	VOH	VOH	Off	Off
H_CPUPWRGD	O	VOL	VOL	Off	Off

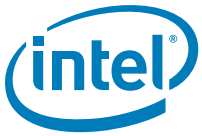


Table 24. Intel® SCH Reset State (Sheet 2 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
H_DPRSTP#	O	VOH	VOH	Off	Off
System Memory Interface					
SM_DQ[63:0]	I/O	High-Z	High-Z	Off	Off
SM_DQS[7:0]	I/O	High-Z	High-Z	Off	Off
SM_MA[14:0]	O	High-Z	VOL	Off	Off
SM_BS[2:0]	O	High-Z	VOL	Off	Off
SM_RAS#	O	High-Z	VOH	Off	Off
SM_CAS#	O	High-Z	VOH	Off	Off
SM_WE#	O	High-Z	VOH	Off	Off
SM_RCEVENIN#	I	High-Z	High-Z	Off	Off
SM_RCVENOUT#	O	High-Z	High-Z	Off	Off
SM_CK[1:0]	O	High-Z	VOH	Off	Off
SM_CK[1:0]#	O	High-Z	VOL	Off	Off
SM_CS[1:0]#	O	High-Z	VOH	Off	Off
SM_CKE[1:0]	O	VOL	VOL	VOL	Off
SM_VREF	I-A	VIX-unknown	VIX-unknown	Don't Care	Off
SM_RCOMP	I-A	High-Z	High-Z	High-Z	Off
LVDS					
LA_DATAP[3:0], LA_DATAN[3:0]	O	High-Z	High-Z	Off	Off
LA_CLKP/N	O	High-Z	High-Z	Off	Off
SDVO					
SDVOB_GREEN+, SDVOB_GREEN-	O	pull-up	High-Z	Off	Off
SDVOB_BLUE+, SDVOB_BLUE-	O	pull-up	High-Z	Off	Off
SDVOB_RED+, SDVOB_RED-	O	pull-up	High-Z	Off	Off
SDVOB_CLK+, SDVOB_CLK-	O	pull-up	High-Z	Off	Off
SDVOB_TVCLKIN+, SDVOB_TVCLKIN-	I	Don't care	Don't care	Off	Off
SDVO_INT+, SDVO_INT-	I	Don't care	Don't care	Off	Off
SDVO_STALL+, SDVO_STALL-	I	Don't care	Don't care	Off	Off
SDVO_CTRLCLK	I/O	pull-up	High-Z	Off	Off
SDVO_CTRLDATA	I/O	pull-up	High-Z	Off	Off

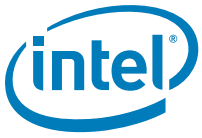


Table 24. Intel® SCH Reset State (Sheet 3 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
DDC					
L_DDC_CLK	I/O	pull-up	High-Z	Off	Off
L_DDC_DATA	I/O	pull-up	High-Z	Off	Off
L_CTLCLKA / B	I/O	pull-up	High-Z	Off	Off
L_VDDEN	O	High-Z	High-Z	Off	Off
L_BKLTEN	O	High-Z	High-Z	Off	Off
L_BKLTCTL	O	High-Z	High-Z	Off	Off
USB					
USB_DP[7:0] USB_DN[7:0]	I/O	VOL	VOL	VOX-unknown	Off
USB_OC[7:0]#	I	VIX-unknown	VIX-unknown	VIX-unknown	Off
USB_RBIASP	I-A	High-Z	High-Z	High-Z	Off
USB_RBIASN	I-A	High-Z	High-Z	High-Z	Off
USB_CLK48	I	Don't care	don't care	Off	Off
PCI Express*					
CLKREQ#	O	VOX	VOX	Off	Off
PCIE_PETp[2:1]	O	pull-up	VOL	Off	Off
PCIE_PETn[2:1]	O	VOH	VOH	Off	Off
PCIE_PERp[2:1]	I	Don't care	Don't care	Off	Off
PCIE_PERn[2:1]	I	Don't care	Don't care	Off	Off
PCIE_CLKINP, PCIE_CLKINN	I	Don't care	Don't care	Off	Off
PCIE_ICOMPO, PCIE_ICOMPI	I/O	High-Z	High-Z	Off	Off
SDIO/MMC					
SD0_DATA[3:0]	I/O	pull-up	High-Z	Off	Off
SD1_DATA[3:0]	I/O	pull-up	High-Z	Off	Off
SD2_DATA[7:0]	I/O	pull-up	High-Z	Off	Off
SD[2:0]_CMD	I/O	pull-up	High-Z	Off	Off
SD[2:0]_CLK	O	VOL	VOL	Off	Off
SD[2:0]_WP	I/O	Don't care	Don't care	Off	Off
SD[2:0]_CD#	I/O	Don't care	Don't care	Off	Off
SD[2:0]_LED	O	VOL	High-Z	Off	Off
SD[2:0]_PWR#	O	VOL	High-Z	Off	Off

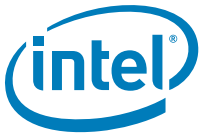


Table 24. Intel® SCH Reset State (Sheet 4 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
PATA					
PATA_DCS1#	O	VOH	VOH	Off	Off
PATA_DCS3#	O	VOH	VOH	Off	Off
PATA_DA[2:0]	O	VOX-unknown	VOX-unknown	Off	Off
PATA_DD[15:0]	I/O	High-Z	High-Z	Off	Off
PATA_DDREQ	I	VIL	VIL	Off	Off
PATA_DDACK#	O	VOH	VOH	Off	Off
PATA_DIOR#	O	VOH	VOH	Off	Off
PATA_DIOW#	O	VOH	VOH	Off	Off
PATA_IORDY	I	VIH	VIH	Off	Off
PATA_IDEIRQ	I	VIL	VIL	Off	Off
Intel® High Definition Audio					
HDA_RST#	O	VOL	VOL	Off	Off
HDA_SYNC	O	High-Z	High-Z	Off	Off
HDA_CLK	O	High-Z	VOL	Off	Off
HDA_SDO	O	High-Z	High-Z	Off	Off
HDA_SDI[1:0]	I	Don't care	Don't care	Off	Off
HDA_DOCKEN#	O	VOH	VOH	Off	Off
HDA_DOCKRST#	O	VOH	VOH	Off	Off
LPC					
LPC_LAD[3:0]	I/O	High-Z	High-Z	Off	Off
LPC_FRAME#	O	VOH	VOH	VOH	Off
LPC_SERIRQ	I/O	High-Z	High-Z	Off	Off
LPC_CLKOUT[2:0]	O	VOL	VOL	VOL	Off
LPC_CLKRUN#	I/O	VOH	VOH	VOH	Off
SMBus					
SMB_DATA	I/O	High-Z	High-Z	Off	Off
SMB_CLK	I/O	High-Z	High-Z	Off	Off
SMB_ALERT#	I	High-Z	High-Z	Off	Off
Power Management					
THRM#	I	VIX-unknown	VIX-unknown	Off	Off
RESET#	I	VIL	VIH	VIL	Off
PWROK	I	VIX-unknown	VIL	VIL	VIL
RSMRST#	I	VIX-unknown	VIH	VIH	VIH
RTCRST#	I	VIX-unknown	VIH	VIH	VIH
SUSCLK	O	Running	Running	Running	Off

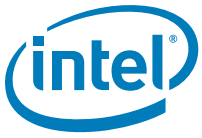
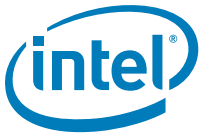


Table 24. Intel® SCH Reset State (Sheet 5 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
WAKE#	I	VIX-unknown	VIX-unknown	VIX-unknown	Off
STPCPU#	O	VOH	VOH	Off	Off
DPRSLPVR	O	VOL	VOL	Off	Off
SLPMODE	O	VOL	VOL	VOH	Off
RSTWARN	I	VIH	VIH	VIH	Off
SLPRDY#	O	VOH	VOH	VOL	Off
RSTRDY#	O	VOH	VOH	VOL	Off
GPE#	I	VIX-unknown	VIX-unknown	VIX-unknown	Off
SLPIOVR#	I/O	High-Z	High-Z	Off	Off
Real Time Clock					
RTC_X1	I-A	Running	Running	Running	Running
RTC_X2	I-A	Running	Running	Running	Running
JTAG					
TCK	I	pull-up	pull-up	Off	Off
TMS	I	pull-up	pull-up	Off	Off
TDI	I	pull-up	pull-up	Off	Off
TDO	O	High-Z	High-Z	Off	Off
TRST#	I	pull-up	pull-up	Off	Off
Miscellaneous					
BSEL2	I	VIX-unknown	VIX-unknown	Off	Off
CFG[1:0]	I	VIX-unknown	VIX-unknown	Off	Off
CLK14	I	Running	Running	Off	Off
INTVRMEN	I	VIH	VIH	VIH	VIH
SPKR	O	VOL	VOL	VOL	Off
SMI#	I	VIX-unknown	VIX-unknown	Off	Off
EXTTS	I	X	X	Off	Off
GPIO					
GPIO[6:0], GPIO[9:8]	I/O	High-Z	High-Z	Off	Off
GPIOSUS[3:0]	I/O	High-Z	High-Z	VIX-unknown	Off



3.2 Integrated Termination Resistors

Table 25. Intel® SCH Integrated Termination Resistors (Sheet 1 of 2)

Signal	Resistor Type	Nominal Value	Tolerance
GPIO3	pull-up	22 kΩ	±20%
GPIO0	pull-down	22 kΩ	±20%
HDA_CLK	pull-down	22 kΩ	±20%
HDA_DOCKRST#	pull-down	20 kΩ	±20%
HDA_RST#	pull-down	22 kΩ	±20%
HDA_SDI[1:0]	pull-down	22 kΩ	±20%
HDA_SDO	pull-down	22 kΩ	±20%
HDA_SYNC	pull-down	22 kΩ	±20%
LA_CLKN, LA_CLK_P	pull-up	50 Ω	±20%
LA_DATAN[3:0], LA_DATAP[3:0]	pull-up	50 Ω	±20%
LPC_LAD[3:0]	pull-up	50 kΩ	±20%
PATA_DA[2:0]	Series	33 Ω	±20%
PATA_DCS1#	Series	33 Ω	±20%
PATA_DCS3#	Series	33 Ω	±20%
PATA_DD[16:0]	Series	33 Ω	±20%
PATA_DD7	pull-down	13.3 kΩ	±20%
PATA_DDACK#	Series	33 Ω	±20%
PATA_DDREQ	Series	33 Ω	±20%
PATA_DDREQ	pull-down	13.3 kΩ	±20%
PATA_DIOR#	Series	33 Ω	±20%
PATA_DIOW#	Series	33 Ω	±20%
PATA_IDEIRQ	Series	33 Ω	±20%
PATA_IORDY	Series	33 Ω	±20%
PCIE_PERn[2:1], PCIE_PERp[2:1]	pull-down	50 Ω	±20%
PCIE_PETn[2:1], PCIE_PETp[2:1]	pull-up	50 Ω	±20%
RESERVED1	pull-up	300 kΩ	±20%
RESET#[1]	pull-down	50 kΩ	±20%
SD[2:0]_PWR#	pull-up	60 kΩ	±20%
SD2_DATA[7:0] SD[1,0]_DATA[3:0]	pull-up	75 kΩ	±30%
SDVOB_RED, SDVOB_RED#	pull-up	50 Ω	±20%
SDVOB_BLUE, SDVOB_BLUE#	pull-up	50 Ω	±20%
SDVOB_GREEN, SDVOB_GREEN#	pull-up	50 Ω	±20%
SDVOB_CLK, SDVOB_CLK#	pull-up	50 Ω	±20%
SDVOB_CLK#	pull-up	50 Ω	±20%

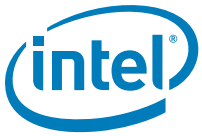


Table 25. Intel® SCH Integrated Termination Resistors (Sheet 2 of 2)

Signal	Resistor Type	Nominal Value	Tolerance
SDVOB_INT, SDVOB_INT#	pull-down	50 Ω	±20%
SDVOB_STALL, SDVOB_STALL#	pull-down	50 Ω	±20%
SDVOB_TVCLKIN, SDVOB_TVCLKIN#	pull-down	50 Ω	±20%
STPCPU#	pull-down	20 kΩ	±20%
TRST#[2]	pull-up	5 kΩ	±40%
TCK[2]	pull-up	5 kΩ	±40%
TMS[2]	pull-up	5 kΩ	±40%
TDI[2]	pull-up	5 kΩ	±40%
USB_DN[7:0]. USB_DP[7:0]	pull-down	15 kΩ	±20%
USB_DN2, USB_DP2 (Client mode)	pull-up	1.5 kΩ	±20%

NOTES:
1. The Intel® SCH power-on is a very controlled sequence with several intermediate transitional states before the true reset is reached (this is a reset state from PWROK asserted high to RESET# deasserted high). Pin values are not ensured to be at the specified reset state until all power supplies and input clocks are stable. The 3.3 V I/O pins may glitch, toggle or float.
2. Refer to the Intel® System Controller Hub (Intel® SCH) Debug Port Design Guide (DPDG) External Version Revision 1.0 for more information on pull-up/pull-down requirements.

4 Absolute Maximums and Operating Conditions

4.1 Absolute Maximums

Table 26 lists the Intel® SCH maximum environmental stress ratings. Functional operation at the absolute maximum and minimum parameters is neither implied nor guaranteed.

The voltage on a specific pin shall be denoted as "V" followed by the subscripted name of that pin. For example:

- V_{TT} refers to the voltage applied to the V_{TT} signal (In the case of power supply signal names, the second V is not repeated in the subscripted portion.)
- V_{H_SWING} refers to the voltage level of the H_SWING signal.

Caution: *At conditions outside functional operation limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits. If the component is exposed to conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded. Although the device contains protective circuitry to resist damage from electro-static discharge, precautions should always be taken to avoid high static voltages or electric fields.*

Table 26. Intel® SCH Absolute Maximum Ratings (Sheet 1 of 2)

Parameter	Description / Signal Names	Min	Max	Unit
$T_{storage\ (short\text{-}term)}$ $T_{storage\ (sustained\ exposure)}$	Storage Temperature[1] Storage Temperature[1]	-55 -5	125 40	°C
Voltage on any 3.3-V Pin with respect to Ground		-0.5	V_{CC33} + 0.5	V
Voltage on any 5-V Tolerant Pin with respect to Ground (V_{CC5REF} = 5 V)		-0.5	V_{CC5REF} + 0.5	V
1.05-V Supply Voltage with respect to V_{SS}	VCC, VTT, VCCSUSBYP, VCCSUSUSBBYP	-0.5	2.1	V
1.5 V Supply Voltage with respect to V_{SS}	VCCAHPLL, VCCDHPLL, VCCLVDS, VCCSDVO, VCCPCIE, VCCAPCIEPLL, VCCADPLLA, VCCADPLLB, VCC15, VCC15USB, VCC15USBSUSBYP, VCCAUSBPLL, VCC15SUS, VCCRTCBYP, VCCHDA[2]	-0.5	2.1	V

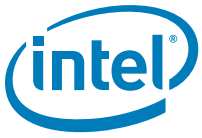


Table 26. Intel® SCH Absolute Maximum Ratings (Sheet 2 of 2)

Parameter	Description / Signal Names	Min	Max	Unit
1.8 V Supply Voltage with respect to V_{SS}	VCCSM	-0.3	2.3	V
3.3 V Supply Voltage with respect to V_{SS}	VCCAPCIEBG, VCC33, VCC33, VCCP33USBSUS, VCCAUSBBGSUS, VCC33SUS, VCC33RTC, VCCHDA[2]	-0.5	4.6	V
5.0 V Supply Voltage with respect to V_{SS}	VCC5REF, VCC5REFSUS	-0.5	5.5	V

NOTES:
1. Refer to Section 6 for more information.
2. VCCHDA is configurable for 1.5-V or 3.3-V operation. Use the appropriate Maximum Limits for the selected configuration.

4.2 Thermal Characteristics

The Intel® SCH is designed for operation at junction temperatures between 0 °C and 105 °C for commercial temperature parts, and -40 °C and 110 °C for industrial temperature rated parts. The thermal resistance of the package is given in Table 27. Package thermal resistance is the measure of the package's heat dissipation capability from die active surface (junction) to a specified reference point (case, board, ambient, etc.).

Table 27. Intel® SCH Thermal Characteristics

Signal Name	Parameter	Min	Nom	Max	Units	Notes
Ψ_{jt}	Characterization Juntion-to-top	-	0.8	-	ºC/Watt	1
T_{die}	Die Junction Operating Temperature for CT	0	-	105	ºC	2, 3
T_{die}	Die Junction Operating Temperature for IT	-40	-	110	ºC	2, 3

NOTES:
1. Determined by analyzes under IVI Boundary test conditions.
2. Measured at top center of the package.
3. Functionality is not guaranteed for parts that exceed T_{die} temperature above 105 ºC. Full performance may be affected if the on-die thermal sensor is enabled.

4.3 General Operating Conditions

The voltage on a specific pin shall be denoted as “V” followed by the subscripted name of that pin. For example:

- V_{TT} refers to the voltage applied to the V_{TT} signal. (In the case of power supply signal names, the second V is not repeated in the subscripted portion.)
- V_{H_SWING} refers to the voltage level of the H_SWING signal.
- Refer to Table 35 for PLL noise rejection specifications.

Table 28. Intel® SCH Maximum Power Consumption

Power Plane	Maximum Power Consumption			Unit	Notes
Symbol	S0	S3	S4/S5		
	Table 31	50m	100u	W	1

NOTES:
1. This specification applies for worst case scenario per rail. In this context, a cumulative use of these values will represent a non realistic application.

5 DC Characteristics

5.1 Signal Groups

The signal description includes the type of buffer used for the particular signal.

Table 29. Intel® SCH Buffer Types

Buffer Type	Description
AGTL+	Assisted Gunning Transceiver Logic Plus. Open Drain interface signals that require termination. Refer to the AGTL+ I/O Specification for complete details.
CMOS, CMOS Open Drain	1.05-V CMOS buffer
CMOS_HDA	CMOS buffers for Intel® HD Audio interface that can be configured for either 1.5-V or 3.3-V operation.
CMOS1.8	1.8-V CMOS buffer. These buffers can be configured as Stub Series Termination Logic (SSTL1.8)
CMOS3.3, CMOS3.3 Open Drain	3.3-V CMOS buffer
CMOS3.3-5	3.3-V CMOS buffer, 5-V tolerant
USB	Compliant with USB1.1 and USB2.0 specifications.
PCIE	PCI Express* interface signals. These signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 V_{max}. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
SDVO	Serial-DVO differential output buffers. These signals are AC coupled.
LVDS	Low Voltage Differential Signal buffers. These signals should drive across a 100-Ohm resistor at the receiver when driving.
Analog	Analog reference or output. Can be used as a threshold voltage or for buffer compensation.

Table 30. Intel® SCH Signal Group Definitions (Sheet 1 of 2)

Signal Group	Signals	Notes
AGTL+	H_ADS#, H_A[31:3]#, H_ADSTB[1:0]#, H_BNR#, H_BREQ0#, H_D[63:0]#, H_DBSY#, H_DEFER#, H_DINV[3:0]#, H_DRDY#, H_DSTBN[3:0]#, H_DSTBP[3:0]#, H_HIT#, H_HITM#, H_REQ[4:0]#, H_BPRI#, H_CPURST#, H_TRDY#, H_RS[2:0]#, H_DPWR#, H_LOCK#	
CMOS	H_THRMTRIP#, H_CPUSLP#, H_PBE#, H_INTR, H_NMI, H_SMI#, TDI, TMS, TRST#, H_STPCLK#, H_DPSLP#, H_DPRSTP#, H_CPUPWRGD, BSEL2, CFG[1:0], TCK	1
CMOS Open Drain	H_INIT#	
CMOS_HDA	HDA_RST#, HDA_SYNC, HDA_SDO, HDA_SDI[1:0], HDA_DOCKEN#, HDA_DOCKRST#	2

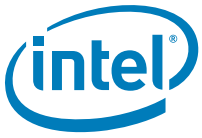


Table 30. Intel® SCH Signal Group Definitions (Sheet 2 of 2)

Signal Group	Signals	Notes
CMOS1.8	SM_DQ[63:0], SM_DQS[7:0], SM_MA[14:0], SM_BS[2:0], SM_RAS#, SM_CAS#, SM_WE#, SM_RCVENIN, SM_RCVENOUT, SM_CS[1:0]#, SM_CKE[1:0]	
CMOS3.3	LPC_AD[3:0], LPC_FRAME#, LPC_SERIRQ, LPC_CLKRUN# SD[0:2]_DATA[7:0], SD[0:2]_CMD, SD[0:2]_WP, SD[0:2]_CD#, SD[0:2]_LED, INTVRMEN, SPKR, SMI#, EXTTS, THRM#, RESET#, PWROK, RSMRST#, RTCRST#, SUSCLK, WAKE#, STPCPU#, DPRSLPVR, SLPMODE, RSTWARN, SLPRDY#, RSTRDY#, L_VDDEN, L_BKLTEN, L_BKLTCTL, USB_OC[7:0]#, GPIO[9:8], SLPIOVR#, GPIO[6:0], GPIOSUS[3:0]	
CMOSS3.3 Open Drain	CLKREQ#, GPE#, TDO, L_DDC_CLK, L_DDC_DATA, L_CTLA_CLK, L_CTLB_CLK, SDVO_CTRLCLK, SDVO_CTRLDATA, SMB_DATA, SMB_ALERT#	
CMOS3.3-5	PATA_DD[15:0], PATA_DA[2:0], PATA_DIOR#, PATA_DIOW#, PATA_DDACK#, PATA_DCS3#, PATA_DCS1#, PATA_DDREQ, PATA_IORDY, PATA_IDEIRQ	
PCIE	PCIE_PETp[2:1], PCIE_PETn[2:1], PCIE_PERp[2:1], PCIE_PERn[2:1]	
SDVO	SDVOB_RED+, SDVOB_RED-, SDVOB_GREEN+, SDVOB_GREEN-, SDVOB_BLUE+, SDVOB_BLUE-, SDVOB_CLK+, SDVOB_CLK- SDVOB_INT+, SDVOB_INT-, SDVO_TVCLKIN+, SDVO_TVCLKIN-, SDVO_STALL+, SDVO_STALL-	
LVDS	LA_DATAP[3:0], LA_DATAN[3:0], LA_CLKP, LA_CLKN	
USB	USB_DP[7:0], USB_DN[7:0]	
Analog, Reference	H_RCOMPO, H_SWING, H_GVREF, H_CGVREF, PCIE_ICOMPO, SM_VREF, SM_RCOMPO, PCIE_ICOMPI, RTC_X1, RTC_X2, USB_RBIASP, USB_RBIASN	
Clocks	H_CLKINP, H_CLKINN, PCIE_CLKINP, PCIE_CLKINN, USB_CLK48, SMB_CLK, LPC_CLKOUT[1:0], DA_REFCLKINP, DA_REFCLKINN, DB_REFCLKINPSCC, DB_REFCLKINNSCC, HDA_CLK, SUSCLK, SD[2:0]_CLK, SM_CK[1:0], SM_CK[1:0]#, CLK14, RTC_X1, RTC_X2	

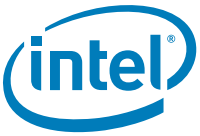
NOTES:
1. These are 1.05-V buffers powered by VTT (except BSEL and TCK which are powered by VCC).
2. The Intel® HD Audio interface signals can operate in either 1.5-V or 3.3-V ranges. 3.3 V operation is the default. The HDA interface can be configured to use the low voltage range by setting the Low Voltage Mode Enable bit of the HDCTL PCI configuration register (D27:F0, offset 40h, bit 0).

5.2 Power and Current Characteristics

Table 31. Thermal Design Power

Symbol	Parameter	Max	Unit	Notes
TDP	Thermal Design Power (at 1.05-V Core Voltage)	2.3	W	1

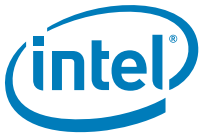
NOTES:
1. This spec is the Thermal Design Power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to concoct higher power synthetic workloads that write



but never read. Under realistic read/write conditions, this higher power workload can only be transient and is accounted in the AC (max) spec.

Table 32. DC Current Characteristics

Symbol	Parameter	Signal Names	Max[1,2]	Unit	Notes
I_{VTT}	1.05-V VTT Supply Current	VTT	739	mA	3
I_{VCC_105}	1.05-V Core Supply Current	VCC	1800	mA	4,5
I_{VCC_15}	1.5-V Core Supply Current	VCC15	10	mA	
$I_{VCCPCIE}$	1.5-V PCI Express* Supply Current	VCCPCIE, VCCPCIEPLL	250	mA	6,7
$I_{VCCLVDS}$	1.5-V LVDS Supply Current	VCCLVDS	62	mA	
$I_{VCCSDVO}$	1.5-V SDVO Supply Current	VCCSDVO	73	mA	
$I_{VCCPCIEBG}$	3.3-V PCI Express Band Gap	VCCPCIEBG	5	mA	
I_{VCC33}	3.3-V HV CMOS Supply Current	VCC33	100	mA	
$I_{VCCHPLL}$	1.5-V Host PLL Supply Current	VCCAHPLL, VCCDHPLL	15 42	mA mA	
$I_{VCCADPLLA,B}$	1.5-V Display PLLA and PLLB Supply Current	VCCADPLLA, VCCADPLLB	48 48	mA mA	
$I_{VCCUSB15}$	1.5-V USB Core Current	VCCUSBCORE	322	mA	
$I_{VCCUSBSUS}$	3.3-V USB Suspend Current	VCC33USBSUS	32	mA	
$I_{VCCUSBSUSBG}$	3.3-V USB Suspend Bandgap Current	VCC33USBBGSUS	5	mA	
$I_{VCCUSBPLL}$	1.5-V USB PLL Current	VCCAUSBPLL	11	mA	
$I_{VCCSUS33}$	3.3-V Suspend Current	VCC33SUS	5	mA	
DDR2 Interface[8]					
I_{VCCSM}	DDR2 System Memory: (1.8-V, 533 MTs) (1.5-V, 533 MTs)	VCCSM	 568 473	mA	
I_{SUS_VCCSM}	DDR2 System Memory Interface (1.8-V) Standby Supply Current	VCCSM	~5	mA	10
I_{SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current		10	µA	
I_{SUS_SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current		10	µA	10
I_{TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current	VCCSM	20	mA	
I_{SUS_TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current	VCCSM	15	µA	10



NOTES:
1. These are pre-silicon estimates, subject to change without notice.
2. I_{CCMAX} is determined on a per-interface basis, and all cannot happen simultaneously.
3. Can vary from CPU. This estimate does not include sense Amps, as they are on a separate rail, or CPU-specific signals.
4. Estimate is only for max current coming through the chipset's supply balls.
5. Includes maximum leakage.
6. Rail includes PLL current.
7. I_{CCMAX} number includes max current for all signal names listed in the table.
8. Determined with 2x Intel® SCH DDR2 buffer strength settings into a 50 Ohms to ½ VCCSM (DDR/DDR2) test load.
9. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express* specification and measured over any 250 consecutive TX UI's. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements
10. Standby refers to system memory in Self Refresh during S3 (STR).

5.3 General DC Characteristics

The voltage on a specific pin shall be denoted as "V" followed by the subscripted name of that pin. For example:

- V_{TT} refers to the voltage applied to the VTT signal. (In the case of power supply signal names, the second V is not repeated in the subscripted portion.)
- V_{H_SWING} refers to the voltage level of the H_SWING signal

Table 33. Operating Condition Power Supply and Reference DC Characteristics

Signal Name	Parameter	Min	Nom	Max	Unit
Power Supply Voltages					
VCC	1.05 V Intel® SCH Core Supply Voltage	0.9975	1.05	1.1025	V
VTT	1.05 V Host AGTL+ Termination Voltage	0.9975	1.05	1.1025	V
VCC15 VCCPCIE VCCSDVO VCCLVDS VCC15USB	1.5 V Supply Voltage	1.425	1.50	1.575	V
VCCAHPLL VCCDHPLL VCCAPCIEPLL VCCADPLLA VCCADPLLB VCCAUSBPLL	Various 1.5 V PLL Supply Voltages	1.425	1.5	1.575	V
VCCSM	1.8 V DDR2 I/O Supply Voltage 1.5 V DDR2 I/O Supply Voltage	1.7 1.425	1.8 1.5	1.9 1.575	V
VCC33 VCCPCIEBG	3.3 V Power Supply Voltage	3.135	3.3	3.465	V
VCCHDA	1.5/3.3 V Supply for Intel® High Definition Audio	1.425 3.135	1.5 3.3	1.575 3.465	V
VCC33SUS VCCP33USBSUS VCCAUSBBGSUS	3.3 V Suspend-Well Power Supplies	3.135	3.3	3.465	V

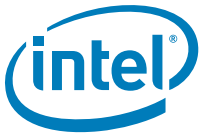


Table 33. Operating Condition Power Supply and Reference DC Characteristics

Signal Name	Parameter	Min	Nom	Max	Unit
VCC5REF VCC5REFSUS	5 V Reference Voltages	4.75	5.0	5.25	V
VCC33RTC	Battery Voltage	2.0	3.3	3.6	V
Reference Signals					
H_SWING	Host Compensation Reference Voltage	0.3125 x V_{TT} – 1%	0.3125 x V_{TT}	0.3125 x V_{TT} + 1%	V
H_GVREF	Host AGTL+ Reference Voltage	2/3 x V_{TT} – 1%	2/3 x V_{TT}	2/3 x V_{TT} + 1%	V
H_CGVREF	Host CMOS Reference Voltage	1/2 x V_{TT} – 1%	1/2 x V_{TT}	1/2 x V_{TT} + 1%	V
SM_VREF	DDR2 Reference Voltage	0.49 x V_{CCSM}	0.50 x V_{CCSM}	0.51 x V_{CCSM}	
H_RCOMPO SM_RCOMPO PCIE_ICOMPO PCIE_ICOMPI USB_RBIASP USB_RBIASN					

Table 34. Active Signal DC Characteristics (Sheet 1 of 4)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
AGTL+						
V_{IL}	Input Low Voltage	–0.1	0.0	$^2/_3$ V_{TT} – 0.1	V	
V_{IH}	Input High Voltage	$^2/_3$ V_{TT} + 0.1	VTT	V_{TT} + 0.1	V	
V_{OL}	Output Low Voltage			$^1/_3$ V_{TT} + 0.1	V	
V_{OH}	Output High Voltage	V_{TT} – 0.1		VTT	V	
I_{OL}	Output Low Current			V_{TTMAX} ÷ (1.5 R_{ttmin})	mA	1
I_{LEAK}	Input Leakage Current			20	µA	2
C_{IN}	Input Capacitance	2		3.5	pF	
CMOS, CMOS Open Drain						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{TT} – 0.1	V	4
V_{IH}	Input High Voltage	½ V_{TT} + 0.7	VTT	V_{TT} + 0.1	V	4
V_{OL}	Output Low Voltage			0.1 x VTT	V	4
V_{OH}	Output High Voltage	0.9 x V_{TT}		VTT	V	4
I_{LEAK}	Input Leakage Current			20	µA	2, 3
C_{IN}	Input Capacitance	1		3.5	pF	

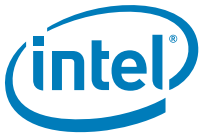


Table 34. Active Signal DC Characteristics (Sheet 2 of 4)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
CMOS_HDA						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{CCHDA} – 1	V	
V_{IH}	Input High Voltage	½ V_{CCHDA} + 0.7	V_{CCHDA}	V_{CCHDA} + 0.1	V	
V_{OL}	Output Low Voltage			0.1 V_{CCHDA}	V	
V_{OH}	Output High Voltage	0.9 V_{CCHDA}			V	
I_{LEAK}	Input Leakage Current			20	µA	
C_{IN}	Input Capacitance	2		3.5	pF	
CMOS1.8						
V_{IL}	Input Low Voltage			V_{SM_VREF} – 0.250	V	
V_{IH}	Input High Voltage	V_{SM_VREF} + 0.250			V	
V_{OL}	Output Low Voltage			V_{SM_VREF} – 0.250	V	
V_{OH}	Output High Voltage	V_{SM_VREF} + 0.250			V	
I_{OL}	Output Low Current			0.3	mA	
I_{LEAK}	Input Leakage Current			1.4	µA	5
C_{IN}	Input Capacitance	2.0		3.4	pF	
CMOS3.3, CMOS3.3 Open Drain						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V – 1	V	
V_{IH}	Input High Voltage	½ V_{CC33} + 0.7	V_{CC33}	V_{CC33} + 0.1	V	
V_{OL}	Output Low Voltage			0.1 V_{CC33}	V	3
V_{OH}	Output High Voltage	0.9 V_{CC33}			V	3
IOL	Output Low Current			1.5	mA	
I_{OH}	Output High Current			-0.5 mA	mA	
I_{LEAK}	Input Leakage Current			20	µA	3
C_{IN}	Input Capacitance	1		3.5	pF	
CMOS3.3–5						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{CC33} – 0.1	V	
V_{IH}	Input High Voltage	½ V_{CC33} + 0.7	V_{CC33}	V_{CC33} + 0.1	V	
V_{OL}	Output Low Voltage			0.1 V_{CC33}	V	
V_{OH}	Output High Voltage	0.9 V_{CC33}			V	
I_{LEAK}	Input Leakage Current			20	µA	
C_{IN}	Input Capacitance	1		3.5	pF	
USB						

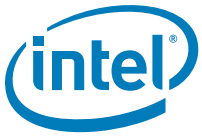


Table 34. Active Signal DC Characteristics (Sheet 3 of 4)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
Refer to the *Universal Serial Bus (USB) Base Specification*, Rev. 2.0.						
PCIE						
$V_{TX-DIFF\ P-P}$	Differential Peak to Peak Output Voltage	0.400		0.6	V	6
V_{TX_CM-ACp}	AC Peak Common Mode Output Voltage			20	mV	6
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX-DIFF\ p-p}$	Differential Input Peak to Peak Voltage	0.175		1.2	V	6
V_{RX_CM-ACp}	AC peak Common Mode Input Voltage			150	mV	
SDVO						
$V_{TX-DIFF\ P-P}$	Differential Peak to Peak Output Voltage	0.400		0.6	V	6
V_{TX_CM-ACp}	AC Peak Common Mode Output Voltage			20	mV	6
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX-DIFF\ p-p}$	Differential Input Peak to Peak Voltage	0.175		1.2	V	6
V_{RX_CM-ACp}	AC peak Common Mode Input Voltage			150	mV	
LVDS						
V_{OD}	Differential Output Voltage	250	350	450	mV	
ΔV_{OD}	Change in V_{OD} between Complementary Output States	0.8		50	mV	
V_{OS}	Offset Voltage		1.25	1.375	V	
ΔV_{OS}	Change in V_{OS} between Complementary Output States			50		
I_{Os}	Output Short Circuit Current		-3.5	-10		
I_{OZ}	Output Tristate Current		±1	±10		
Differential Clocks						
V_{SWING}	Input swing	300			mV	7, 8
V_{CROSS}	Crossing point	300		550	mV	7, 9, 10, 11

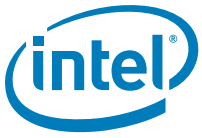


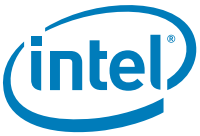
Table 34. Active Signal DC Characteristics (Sheet 4 of 4)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{CROSS_VAR}	V_{CROSS} Variance			140	mV	7, 9, 10, 12
V_{IH}	Maximum input voltage			1.15	V	7, 9, 13
V_{IL}	Minimum input voltage	-0.3			V	7, 9, 14

NOTES:
1. R_{ttmin} = 50 Ohm
2. $V_{OL} < V_{PAD} < V_{TT}$
3. For CMOS Open Drain signals defined in Table 34, V_{OH}, V_{OL}, and I_{LEAK} DC specs are not applicable due to the pull-up/pull-down resister that is required on the board.
4. BSEL2, CFG[1:0] and TCK signals reference VCC, not VTT.
5. At VCCSM = 1.7 V.
6. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express* specification and measured over any 250 consecutive TX UI's. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements.
7. Applicable to the following signals: H_CLKINN/P, PCIE_CLKINN/P, DB_DREFCLKIN[N,P]SCC, DA_DREFCLKINN/P
8. Measurement taken from differential waveform.
9. Measurement taken from single ended waveform.
10. V_{CROSS} is defined as the voltage where Clock = Clock#.
11. Only applies to the differential rising edge (i.e., Clock rising and Clock# falling)
12. The total variation of all V_{CROSS} measurements in any particular system. This is a subset of V_{CROSS}MIN /V_{CROSS}max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting V_{CROSS_VAR} to be smaller than V_{CROSS} absolute.
13. The max voltage including overshoot.
14. The min voltage including undershoot.

Table 35. PLL Noise Rejection Specifications

PLL	Noise Rejection Specification	Notes
VCCAHPLL	34 dB(A) attenuation of power supply noise in 1-MHz (f1) to 66-MHz (f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mV	
VCCDHPLL	peak to peak noise should be limited to < 120 mV	
VCCAPCIE	< 0 dB(A) in 0 to 1MHz, 20 dB(A) attenuation of power supply noise in 1 MHz(f1) to 1.25 GHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 40 mV	
VCCADPLLA	20 dB(A) attenuation of power supply noise in 10-kHz(f1) to 2.5-MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV	
VCCADPLLB	20 dB(A) attenuation of power supply noise in 10-kHz(f1) to 2.5-MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV	
VCCAUSBPLL	USB PLL	



6 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits which the device is exposed to while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes below guideline on post board attach limits).

Table 36 specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality & reliability may be affected.

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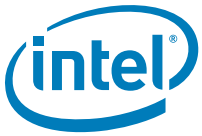
Table 36. Intel® SCH Absolute Maximum Ratings

Parameter	Description / Signal Names	Min	Max	Unit
$T_{storage\ (short\text{-}term)}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.[1,2,3,4,5]	-55	125	ºC
$T_{storage\ (sustained\ exposure)}$	The minimum/maximum device storage temperature for a sustained period of time.[1,2,3,4,5]	-5	40	ºC
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.[1,2,3,4,5]	-	60% @24ºC	
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with sustained storage conditions.[1,2,3,4,5]	-	6	months

NOTES:

1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications
2. These ratings apply to the Intel component and do not include the tray or packaging
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel® does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel® board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28C)
5. Device storage temperature qualification methods follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards.



7 Ballout and Package Information

The Intel® SCH comes in an Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 1295 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters. Key package attributes are listed below:

Dimensions:

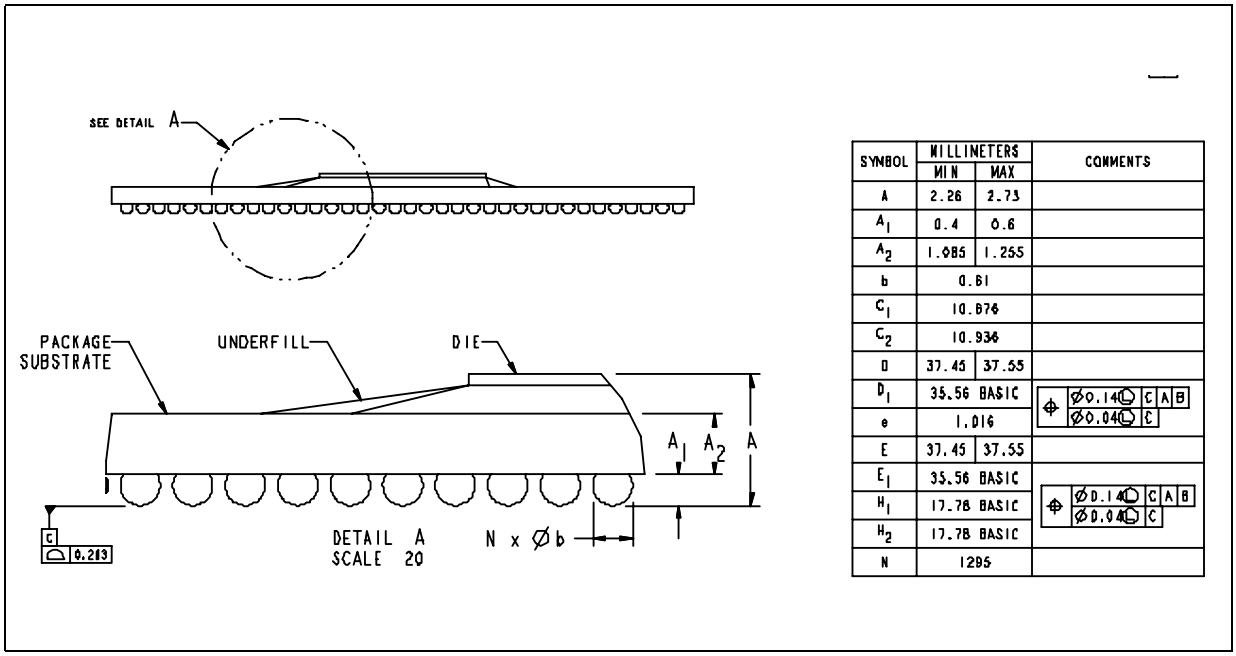
- Silicon Process: P861, 6 metal
- Physical Die Size: 10.725 mm x 10.985 mm
- Package parameters: 37.5 mm x 37.5 mm
- Ball Count: 1295
- Package Land/Pitch: 1.016 mm
- Land metal diameter: 375 microns
- Solder resist opening: 321 microns

Tolerances:

- .X - ± 0.1
- .XX - ± 0.05
- Angles - ± 1.0 degrees

7.1 Package Diagrams

Figure 3. Intel® SCH (Side View)



SYMBOL	MILLIMETERS		COMMENTS
	MIN	MAX	
A	2.26	2.73	
A_1	0.4	0.6	
A_2	1.085	1.255	
b	0.61		
C_1	10.876		
C_2	10.936		
D	37.45	37.55	
D_1	35.56 BASIC		Ø0.14 C A B Ø0.04 C
e	1.016		
E	37.45	37.55	
E_1	35.56 BASIC		
H_1	17.78 BASIC		Ø0.14 C A B Ø0.04 C
H_2	17.78 BASIC		
N	1295		

Figure 4. Intel® SCH Package (Solder Resist Opening)

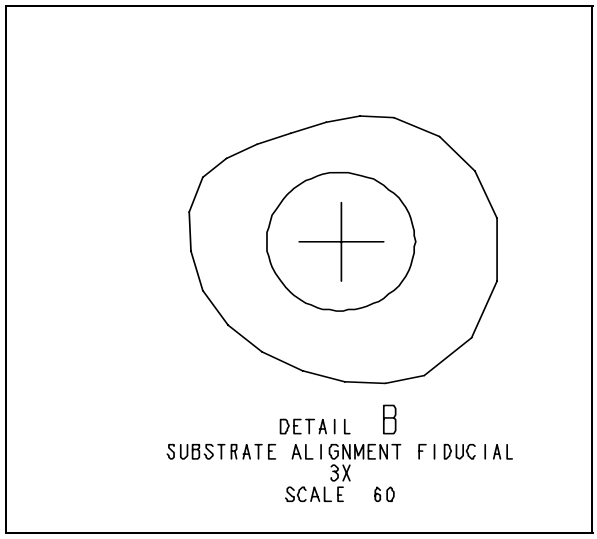
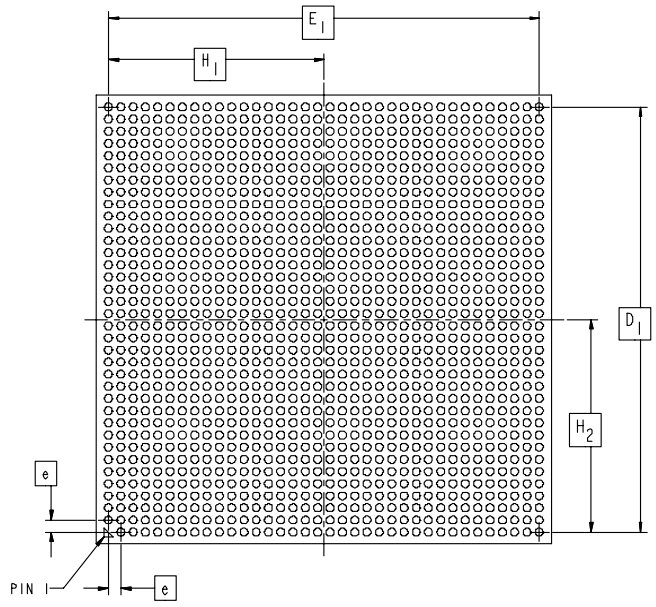
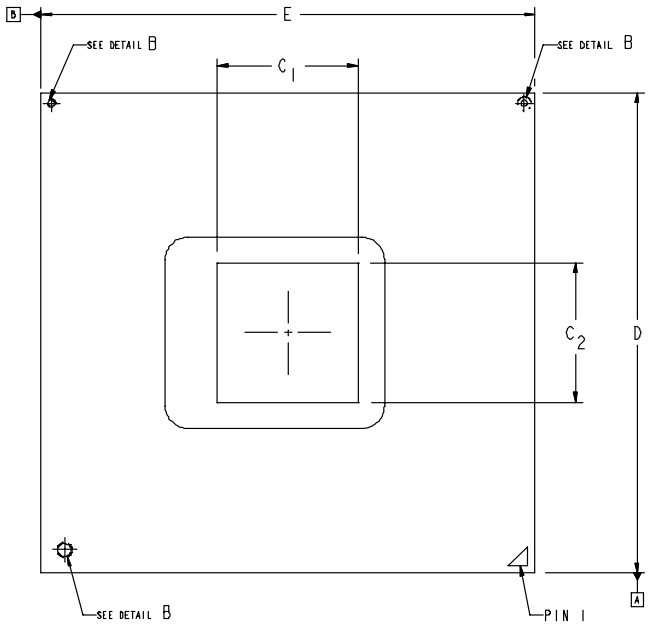


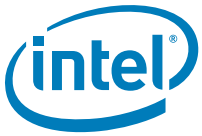
Figure 5. Intel® SCH (Bottom View)



NOTE: Maximum outgoing package coplanarity not to exceed 8 mils.

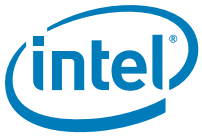
Figure 6. Intel® SCH (Top View)



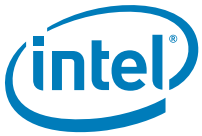


7.2 Reverse Ballout Definition and Signal Location

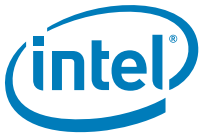
	AT	AR	AP	AN	AM	AL	AK	AJ
1	VSS	VSS	VSS	VSS	H_D31#	H_DSTBP1#	H_D21#	H_D22#
2	VSS	VSS	VSS	H_D26#	VSS	H_DSTBN1#	VSS	H_D29#
3	VSS	VSS	VSS	H_D30#	VSS	H_D16#	VSS	H_D17#
4	VSS	H_DPWR#	H_D28#	H_D19#	VSS	H_D24#	VSS	H_D20#
5	H_D50#	VSS	VSS	VSS	VSS	H_D18#	VSS	H_D1#
6	H_D53#	H_DSTBN3#	H_DSTBP3#	H_D49#	H_D27#	H_D25#	H_D23#	H_D14#
7	H_D48#	VSS	VSS	VSS	VSS	H_D57#	VSS	H_D8#
8	H_D60#	H_D61#	H_D55#	H_D63#	H_D51#	H_D52#	H_DINV1#	H_D15#
9	H_D54#	VSS	VSS	VSS	VSS	H_DINV3#	VSS	VSS
10	H_D39#	H_D34#	H_D42#	H_D56#	H_D58#	H_D59#	H_D62#	VSS
11	H_D36#	VSS	VSS	VSS	VSS	H_D32#	VSS	VSS
12	H_D43#	H_DINV2#	H_D44#	H_D35#	H_D37#	H_D33#	H_D45#	VSS
13	H_D47#	VSS	VSS	VSS	VSS	H_D40#	VSS	VSS
14	H_DSTBP2#	H_DSTBN2#	H_D46#	H_D41#	H_D38#	RESERVED5	RESERVED4	VSS
15	VSS	H_TESTIN#	VSS	H_DPRSTP#	VSS	H_THRMTRIP#	VSS	VSS
16	SM_DQ63	VSS	SM_DQ59	VSS	SM_DQ58	VSS	SM_DQ62	VSS
17	SM_DQS7	SM_DQ61	VSS	SM_DQ57	VSS	SM_DQ56	VSS	VSS
18	SM_DQ60	VSS	SM_DQ51	VSS	SM_DQ50	VSS	SM_DQ55	SM_CK1#
19	SM_DQS6	SM_DQ54	VSS	SM_DQ53	VSS	SM_DQ49	VSS	SM_CK1
20	SM_DQ48	VSS	SM_DQ52	VSS	SM_DQ43	VSS	SM_DQ42	VSS
21	SM_DQ47	SM_DQ46	VSS	SM_DQS5	VSS	SM_DQ45	VSS	RESERVED2
22	SM_DQ41	VSS	SM_DQ40	VSS	SM_DQ44	VSS	SM_DQ35	VSS
23	SM_DQ34	SM_DQ39	VSS	SM_DQS4	VSS	SM_DQ38	VSS	SM_CAS#
24	SM_DQ37	VSS	SM_DQ33	VSS	SM_DQ32	VSS	SM_DQ36	VSS
25	SM_DQ31	SM_DQ27	VSS	SM_DQ26	VSS	SM_DQ30	VSS	SM_BS0
26	SM_DQS3	VSS	SM_DQ29	VSS	SM_DQ28	VSS	SM_DQ25	VSS
27	SM_DQ24	SM_DQ23	VSS	SM_DQ19	VSS	SM_DQ18	VSS	SM_MA3
28	SM_DQ22	VSS	SM_DQS2	VSS	SM_DQ21	VSS	SM_DQ20	VSS
29	SM_DQ17	SM_DQ16	VSS	SM_DQ11	VSS	SM_DQ10	VSS	SM_MA8
30	SM_DQ15	VSS	SM_DQS1	VSS	SM_DQ14	VSS	SM_DQ13	VSS
31	SM_DQ9	SM_DQ8	VSS	SM_DQ12	VSS	SM_DQ3	VSS	SM_MA7
32	SM_DQ2	VSS	SM_DQ7	VSS	SM_DQS0	VSS	SM_DQ5	VSS
33	VSS	SM_DQ6	VSS	SM_DQ1	VSS	SM_CKE0	VSS	SM_CKE1
34	VSS	VSS	SM_DQ0	VSS	SM_CK0#	VSS	VSS	VSS
35	VSS	VSS	VSS	SM_DQ4	SM_CK0	VSS	SM_VREF	VSS
36	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SM_RCVENIN



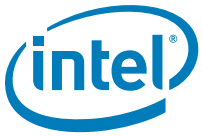
	AH	AG	AF	AE	AD	AC	AB
1	H_D4#	H_D11#	H_DSTBN0#	H_DSTBP0#	H_DBSY#	H_TRDY#	H_HITM#
2	VSS	H_D13#	VSS	H_D6#	VSS	H_BNR#	VSS
3	VSS	H_D3#	VSS	H_D10#	VSS	H_RS0#	VSS
4	VSS	H_D9#	VSS	H_RS1#	VSS	H_ADS#	VSS
5	VSS	H_D2#	VSS	H_INIT#	VSS	H_LOCK#	VSS
6	VSS	H_D0#	VSS	H_INTR	VSS	H_RS2#	VSS
7	H_D7#	H_D5#	H_DINV0#	H_STPCLK#	H_HIT#	H_BPRI#	H_DPSLP#
8	VSS	H_D12#	VSS	H_NMI	VSS	H_CPUSLP#	VSS
9	VSS	VSS	VTT	VSS	VTT	VSS	VTT
10	VTT	VTT	VTT	VTT	VTT	VTT	VTT
11	VSS	VSS	VSS	VSS	VCCDHPLL	VCCAHPLL	VTT
12	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VSS	VSS
13	VCCSM	VCCSM	VSS	VCCSM	VCCSM	VSS	VCC
14	VCCSM	VSS	VSS	VCCSM	VCCSM	VSS	VCC
15	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VSS	VCC
16	VCCSM	VSS	VSS	VCCSM	VCCSM	VSS	VCC
17	VCCSM	VSS	VSS	VCCSM	VCCSM	VSS	VCC
18	VSS	VCCSM	VCCSM	VCCSM	VCCSM	VSS	VCC
19	VSS	VCCSM	VCCSM	VCCSM	VCCSM	VSS	VCC
20	VSS	VSS	VSS	VCCSM	VCCSM	VSS	VCC
21	VSS	RESERVED3	VSS	VCCSM	VCCSM	VSS	VCC
22	SM_CS0#	SM_MA13	VSS	VCCSM	VCCSM	VSS	VCC
23	VSS	SM_CS1#	VSS	VCCSM	VCCSM	VSS	VCC
24	SM_BS1	SM_RAS#	VSS	VSS	VCCSM	VSS	VSS
25	VSS	SM_WE#	VSS	VCCPCIE	VSS	VCCSDVO	VCCSDVO
26	SM_MA0	SM_MA10	VSS	VCCPCIE	VCCPCIE	VSS	VCCSDVO
27	VSS	SM_MA1	VSS	VCCPCIE	VCCPCIE	VSS	VCCSDVO
28	SM_MA2	SM_MA5	VSS	VCCPCIE	VCCPCIE	VCCPCIE	VSS
29	VSS	SM_MA4	VSS	VCCPCIE	VCCPCIE	VSS	PCIE_PERn2
30	SM_MA12	SM_MA9	VSS	VCCPCIE	VSS	PCIE_PERp2	VSS
31	VSS	SM_MA6	VSS	VSS	PCIE_PETn2	VSS	VCCAPCIEBG
32	SM_MA11	SM_BS2	VSS	PCIE_PETp2	VSS	VSSAPCIEBG	VSS
33	VSS	SM_MA14	VSS	VSS	PCIE_PETp1	VSS	PCIE_PERp1
34	VSS	VSS	VSS	PCIE_PETn1	VSS	PCIE_PERn1	VSS
35	SM_RCVENOUT	VSS	RESET#	VSS	PCIE_ICOMPI	VSS	PCIE_CLKINN
36	VSS	SM_RCOMPO	VSS	PCIE_ICOMPO	VSS	PCIE_CLKINP	VSS



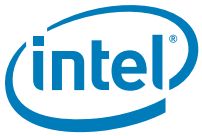
	AA	Y	W	V	U	T
1	H_BREQ0#	H_REQ0#	H_A16#	H_A15#	H_A4#	H_A17#
2	H_DEFER#	VSS	H_A13#	VSS	H_A9#	VSS
3	H_DRDY#	VSS	H_A10#	VSS	H_REQ2#	VSS
4	H_A3#	VSS	H_A12#	VSS	H_A21#	VSS
5	H_A8#	VSS	H_A14#	VSS	H_A26#	VSS
6	H_REQ3#	VSS	H_ADSTB0#	VSS	H_A19#	VSS
7	H_A6#	H_A5#	H_A7#	H_A11#	H_A25#	H_A24#
8	H_REQ4#	VSS	H_REQ1#	VSS	H_A18#	VSS
9	VSS	VTT	VSS	VTT	VSS	VTT
10	VTT	VTT	VTT	VTT	VTT	VTT
11	VSS	VTT	VSS	VTT	VSS	VTT
12	VCC	VSS	VCC	VSS	VCC	VSS
13	VCC	VCC	VCC	VCC	VCC	VCC
14	VSS	VSS	VSS	VSS	VSS	VSS
15	VCC	VCC	VCC	VCC	VCC	VCC
16	VSS	VSS	VSS	VSS	VSS	VSS
17	VCC	VCC	VCC	VCC	VCC	VCC
18	VSS	VSS	VSS	VSS	VSS	VSS
19	VCC	VCC	VCC	VCC	VCC	VCC
20	VSS	VSS	VSS	VSS	VSS	VSS
21	VCC	VCC	VCC	VCC	VCC	VCC
22	VSS	VSS	VSS	VSS	VSS	VSS
23	VCC	VCC	VCC15USB	VCC15USB	VCC15USB	RESERVED15
24	VCC	VSS	VCC15USB	VCC15USB	VCC15USB	VSS
25	VCCSDVO	VSS	VSS	VCCLVDS	RESERVED17	RESERVED16
26	VCCSDVO	VCCADPLLB	VCCLVDS	VCCADPLLA	VCCAUSBBGSUS	VSSAUSBBGSUS
27	VSS	VCCLVDS	VCCAUSBPLL	VCCLVDS	VCC5REFSUS	RESERVED13
28	VCCAPCIEPLL	VSS	VCCLVDS	VSS	RESERVED11	VSS
29	VSS	SDVOB_INT#	VSS	RESERVED7	VSS	LA_DATAN2
30	SDVOB_INT	VSS	RESERVED6	VSS	LA_DATAP2	VSS
31	VSS	SDVOB_GREEN#	VSS	SDVOB_CLK#	VSS	DA_REFCLKINP
32	SDVOB_GREEN	VSS	SDVOB_CLK	VSS	DA_REFCLKINN	VSS
33	VSS	SDVOB_RED#	VSS	SDVOB_STALL#	VSS	LA_DATAP0
34	SDVOB_RED	VSS	SDVOB_STALL	VSS	LA_DATAN0	VSS
35	VSS	SDVOB_TVCLKIN#	VSS	SDVOB_BLUE#	VSS	LA_DATAN1
36	SDVOB_TVCLKIN	VSS	SDVOB_BLUE	VSS	LA_DATAP1	VSS



	R	P	N	M	L	K	J
1	H_A27#	H_A20#	H_SMI#	VSS	H_CLKINP	H_CLKINN	VSS
2	H_ADSTB1#	VSS	H_CPURST#	VSS	VSS	VSS	VSS
3	H_A23#	VSS	H_RCOMPO	VSS	VSS	VCC33	VSS
4	H_A30#	VSS	H_CGVREF	VSS	VCC33	VSS	VCC33
5	H_A29#	VSS	H_GVREF	VSS	VSS	VCC33	VSS
6	H_A31#	VSS	H_SWING	VSS	VCC33	VSS	VCC33
7	H_A28#	H_PBE#	H_CPUPWRGD	VSS	VSS	VCC33	VSS
8	H_A22#	VSS	VSS	VSS	VCC33	VSS	VCC33
9	VSS	VTT	VSS	VTT	VSS	VCC33	VSS
10	VTT	VTT	VTT	VSS	VCC33	VSS	VCC33
11	VSS	VTT	VSS	VSS	VSS	VCC33	VSS
12	VCC	VSS	VCCHDA	VCCHDA	VSS	VSS	VCC15
13	VCC	VCC	VCC	VCC	VSS	VCC15	VCC15
14	VSS	VSS	VSS	VCC	VSS	VCC15	VCC15
15	VCC	VCC	VCC	VCC	VSS	VCC15	VCC15
16	VSS	VSS	VSS	VSS	VSS	VCC15	VCC15
17	VCC	VCC	VCC	VCC	VSS	VCC15	VCC15
18	VSS	VSS	VSS	VCC	VSS	VCC15	VCC15
19	VCC	VCC	VCC	VCC	VSS	VCC15	VCC15
20	VSS	VSS	VSS	VSS	VSS	VCC15	VCC15
21	VCC	VCC	VCC	VCC	VSS	VCC15	VCC15
22	VSS	VSS	VSS	VCC	VSS	VCC15	VCC15
23	VCC	VCC	VCC	VCC	VSS	VCC15	VCC15
24	RESERVED14	VSS	VSS	VSS	VSS	VSS	VCC15
25	VCCP33USBSUS	VCCP33USBSUS	VSS	VCC33SUS	VCC5REF	VSS	VSS
26	RESERVED12	VSS	VCCP33USBSUS	VCC33SUS	VCC33SUS	VSS	RESERVED10
27	VSS	VCC33SUS	VSS	VCC33SUS	VSS	VSS	VSS
28	VSS	VSS	VSS	VSS	VSS	VSS	GPIOSUS3
29	VSS	USB_OC6#	VSS	USB_OC3#	VSS	USB_OC0#	VSS
30	USB_OC1#	VSS	USB_OC7#	VSS	USB_OC2#	VSS	USB_OC4#
31	VSS	LA_CLKN	VSS	USB_DP0	VSS	USB_DP3	VSS
32	LA_CLKP	VSS	USB_DN0	VSS	USB_DN3	VSS	DB_REFCLKINPSSC
33	VSS	LA_DATAN3	VSS	USB_DP1	VSS	USB_DN5	VSS
34	LA_DATAP3	VSS	USB_DN1	VSS	USB_DP5	VSS	USB_DP7
35	VSS	USB_RBIASP	VSS	USB_DP2	VSS	USB_DP4	VSS
36	USB_RBIASN	VSS	USB_DN2	VSS	USB_DN4	VSS	USB_DP6



	H	G	F	E	D	C	B	A
1	VSS	VSS	VSS	HDA_CLK	VSS	VSS	VSS	
2	VSS	VSS	VSS	HDA_SYNC	VSS	VSS	VSS	VSS
3	VCC33	VSS	HDA_DOCKEN#	VSS	HDA_DOCKRST#	VSS	VSS	VSS
4	VSS	HDA_SDO	VSS	HDA_SDI1	VSS	SD0_DATA1	SD0_CLK	VSS
5	VCC33	VSS	HDA_SDI0	VSS	HDA_RST#	VSS	VSS	SD2_PWR#
6	VSS	XOR_TEST	VSS	SD0_DATA3	SD0_CD#	SD1_PWR#	SD1_WP	SD1_CMD
7	VCC33	VSS	RESERVED19	VSS	VSS	VSS	VSS	SD1_CD#
8	VSS	SD2_LED	SD0_WP	SD1_LED	SD0_LED	SD1_DATA3	SD1_DATA0	SD2_WP
9	VSS	SD2_DATA3	VSS	VSS	VSS	VSS	VSS	SD2_DATA4
10	VSS	SD1_DATA1	SD2_CLK	SD0_DATA0	SD2_CMD	VSS	SD2_DATA7	SD2_DATA1
11	VSS	SD2_DATA0	VSS	VSS	VSS	VSS	VSS	SD2_DATA5
12	VSS	SD2_CD#	SD2_DATA6	SD0_CMD	RESERVED20	SD0_PWR#	RESERVED18	SD2_DATA2
13	VSS	L_CTLB_DATA	VSS	VSS	VSS	VSS	VSS	SD0_DATA2
14	VSS	GPIO9	CFG0	L_DDCDATA	BSEL2	SD1_CLK	RESERVED21	SD1_DATA2
15	VSS	L_DDCCLK	VSS	VSS	VSS	VSS	VSS	L_CTLA_CLK
16	VSS	STPCPU#	GPIO0	SDVO_CTRLCLK	L_VDDEN	SMI#	SDVO_CTRLDATA	CLKREQ#
17	VSS	L_BKLTEN	VSS	VSS	VSS	VSS	VSS	GPIO1
18	VSS	L_BKLTCTL	SMB_ALERT#	SLPIOVR#	CLK14	THRM#	EXTTS	RESERVED1
19	VSS	LPC_AD2	VSS	GPIO8	GPIO3	GPIO2	DPRSLPVR	CFG1
20	VSS	LPC_CLKRUN#	VSS	VSS	VSS	VSS	VSS	LPC_CLKOUT1
21	VSS	SMB_CLK	SMB_DATA	LPC_SERIRQ	GPIO4	SPKR	GPIO5	GPIO6
22	VSS	LPC_CLKOUT0	VSS	VSS	VSS	VSS	VSS	LPC_CLKOUT2
23	VSS	LPC_AD0	PATA_DD4	PATA_DD5	PATA_DD9	PATA_DD7	PATA_DD8	PATA_DD6
24	VSS	LPC_AD1	VSS	VSS	VSS	VSS	VSS	PATA_DD10
25	VSS	LPC_FRAME#	PATA_DD11	PATA_DD14	PATA_DD1	PATA_DD2	PATA_DD12	PATA_DD3
26	VSS	LPC_AD3	VSS	VSS	VSS	VSS	VSS	PATA_DD13
27	RESERVED9	VSS	PATA_DA0	PATA_IORDY	PATA_DIOR#	PATA_DDREQ	PATA_DD15	PATA_DD0
28	VSS	INTVRMEN	RSMRST#	VSS	VSS	VSS	VSS	PATA_DIOW#
29	USB_OC5#	VSS	PATA_DCS3#	PATA_DCS1#	PATA_DA2	PATA_DA1	PATA_IDEIRQ	PATA_DDACK#
30	VSS	RTCRST#	RESERVED0	VSS	VSS	VSS	VSS	VCC33RTC
31	DB_REFCLKINNSSC	VSS	GPIOSUS2	SLPMODE	PWROK	WAKE#	SUSCLK	RTC_X2
32	VSS	TMS	VSS	GPIOSUS1	VSS	VSS	VSS	RTC_X1
33	USB_DN7	VSS	TRST#	VSS	TDI	SLPRDY#	RSTRDY#	VSS
34	VSS	TDO	VSS	TCK	VSS	RSTWARN	VSS	VSS
35	USB_DN6	VSS	VSS	VSS	GPE#	VSS	VSS	VSS
36	VSS	GPIOSUS0	VSS	USB_CLK48	VSS	VSS	VSS	VSS



7.3 Pin List by Ball Name

Ball Name	Ball Number
BSEL2	D14
CFG0	F14
CFG1	A19
CLK14	D18
CLKREQ#	A16
DA_REFCLKINN	U32
DA_REFCLKINP	T31
DB_REFCLKINNSSC	H31
DB_REFCLKINPSSC	J32
DPRSLPVR	B19
EXTTS	B18
GPE#	D35
GPIO0	F16
GPIO1	A17
GPIO2	C19
GPIO3	D19
GPIO4	D21
GPIO5	B21
GPIO6	A21
SLPIOVR#	E18
GPIO8	E19
GPIO9	G14
GPIOSUS0	G36
GPIOSUS1	E32
GPIOSUS2	F31
GPIOSUS3	J28
H_A10#	W3
H_A11#	V7
H_A12#	W4
H_A13#	W2
H_A14#	W5
H_A15#	V1
H_A16#	W1
H_A17#	T1
H_A18#	U8
H_A19#	U6

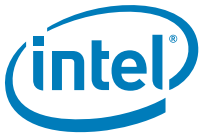
Ball Name	Ball Number
H_A20#	P1
H_A21#	U4
H_A22#	R8
H_A23#	R3
H_A24#	T7
H_A25#	U7
H_A26#	U5
H_A27#	R1
H_A28#	R7
H_A29#	R5
H_A3#	AA4
H_A30#	R4
H_A31#	R6
H_A4#	U1
H_A5#	Y7
H_A6#	AA7
H_A7#	W7
H_A8#	AA5
H_A9#	U2
H_ADS#	AC4
H_ADSTB0#	W6
H_ADSTB1#	R2
H_BNR#	AC2
H_BPRI#	AC7
H_BREQ0#	AA1
H_CGVREF	N4
H_CLKINN	K1
H_CLKINP	L1
H_CPUPWRGD	N7
H_CPURST#	N2
H_CPUSLP#	AC8
H_D0#	AG6
H_D1#	AJ5
H_D10#	AE3
H_D11#	AG1
H_D12#	AG8
H_D13#	AG2

Ball Name	Ball Number
H_D14#	AJ6
H_D15#	AJ8
H_D16#	AL3
H_D17#	AJ3
H_D18#	AL5
H_D19#	AN4
H_D2#	AG5
H_D20#	AJ4
H_D21#	AK1
H_D22#	AJ1
H_D23#	AK6
H_D24#	AL4
H_D25#	AL6
H_D26#	AN2
H_D27#	AM6
H_D28#	AP4
H_D29#	AJ2
H_D3#	AG3
H_D30#	AN3
H_D31#	AM1
H_D32#	AL11
H_D33#	AL12
H_D34#	AR10
H_D35#	AN12
H_D36#	AT11
H_D37#	AM12
H_D38#	AM14
H_D39#	AT10
H_D4#	AH1
H_D40#	AL13
H_D41#	AN14
H_D42#	AP10
H_D43#	AT12
H_D44#	AP12
H_D45#	AK12
H_D46#	AP14
H_D47#	AT13

Ball Name	Ball Number
H_D48#	AT7
H_D49#	AN6
H_D5#	AG7
H_D50#	AT5
H_D51#	AM8
H_D52#	AL8
H_D53#	AT6
H_D54#	AT9
H_D55#	AP8
H_D56#	AN10
H_D57#	AL7
H_D58#	AM10
H_D59#	AL10
H_D6#	AE2
H_D60#	AT8
H_D61#	AR8
H_D62#	AK10
H_D63#	AN8
H_D7#	AH7
H_D8#	AJ7
H_D9#	AG4
H_DBSY#	AD1
H_DEFER#	AA2
H_DINV0#	AF7
H_DINV1#	AK8
H_DINV2#	AR12
H_DINV3#	AL9
H_DPRSTP#	AN15
H_DPSLP#	AB7
H_DPWR#	AR4
H_DRDY#	AA3
H_DSTBN0#	AF1
H_DSTBN1#	AL2
H_DSTBN2#	AR14
H_DSTBN3#	AR6
H_DSTBP0#	AE1
H_DSTBP1#	AL1
H_DSTBP2#	AT14
H_DSTBP3#	AP6

Ball Name	Ball Number
H_GVREF	N5
H_HIT#	AD7
H_HITM#	AB1
H_INIT#	AE5
H_INTR	AE6
H_LOCK#	AC5
H_NMI	AE8
H_PBE#	P7
H_RCOMPO	N3
H_REQ0#	Y1
H_REQ1#	W8
H_REQ2#	U3
H_REQ3#	AA6
H_REQ4#	AA8
H_RS0#	AC3
H_RS1#	AE4
H_RS2#	AC6
H_SMI#	N1
H_STPCLK#	AE7
H_SWING	N6
H_TESTIN#	AR15
H_THRMTRIP#	AL15
H_TRDY#	AC1
HDA_CLK	E1
HDA_DOCKEN#	F3
HDA_DOCKRST#	D3
HDA_RST#	D5
HDA_SDI0	F5
HDA_SDI1	E4
HDA_SDO	G4
HDA_SYNC	E2
INTVRMEN	G28
L_BKLTCTL	G18
L_BKLTEN	G17
L_CTLA_CLK	A15
L_CTLB_DATA	G13
L_DDCCLK	G15
L_DDCDATA	E14
L_VDDEN	D16

Ball Name	Ball Number
LA_CLKN	P31
LA_CLKP	R32
LA_DATAN0	U34
LA_DATAN1	T35
LA_DATAN2	T29
LA_DATAN3	P33
LA_DATAP0	T33
LA_DATAP1	U36
LA_DATAP2	U30
LA_DATAP3	R34
LPC_AD0	G23
LPC_AD1	G24
LPC_AD2	G19
LPC_AD3	G26
LPC_CLKOUT0	G22
LPC_CLKOUT1	A20
LPC_CLKOUT2	A22
LPC_CLKRUN#	G20
LPC_FRAME#	G25
LPC_SERIRQ	E21
PATA_DA0	F27
PATA_DA1	C29
PATA_DA2	D29
PATA_DCS1#	E29
PATA_DCS3#	F29
PATA_DD0	A27
PATA_DD1	D25
PATA_DD10	A24
PATA_DD11	F25
PATA_DD12	B25
PATA_DD13	A26
PATA_DD14	E25
PATA_DD15	B27
PATA_DD2	C25
PATA_DD3	A25
PATA_DD4	F23
PATA_DD5	E23
PATA_DD6	A23
PATA_DD7	C23



Ball Name	Ball Number
PATA_DD8	B23
PATA_DD9	D23
PATA_DDACK#	A29
PATA_DDREQ	C27
PATA_DIOR#	D27
PATA_DIOW#	A28
PATA_IDEIRQ	B29
PATA_IORDY	E27
PCIE_CLKINN	AB35
PCIE_CLKINP	AC36
PCIE_ICOMPI	AD35
PCIE_ICOMPO	AE36
PCIE_PERn1	AC34
PCIE_PERn2	AB29
PCIE_PERp1	AB33
PCIE_PERp2	AC30
PCIE_PETn1	AE34
PCIE_PETn2	AD31
PCIE_PETp1	AD33
PCIE_PETp2	AE32
PWROK	D31
RESERVED0	F30
RESERVED1	A18
RESERVED10	J26
RESERVED11	U28
RESERVED12	R26
RESERVED13	T27
RESERVED14	R24
RESERVED15	T23
RESERVED16	T25
RESERVED17	U25
RESERVED18	B12
RESERVED19	F7
RESERVED2	AJ21
RESERVED20	D12
RESERVED21	B14
RESERVED3	AG21
RESERVED4	AK14
RESERVED5	AL14

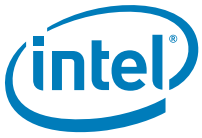
Ball Name	Ball Number
RESERVED6	W30
RESERVED7	V29
RESERVED9	H27
RESET#	AF35
RSMRST#	F28
RSTRDY#	B33
RSTWARN	C34
RTC_X1	A32
RTC_X2	A31
RTCRST#	G30
SD0_CD#	D6
SD0_CLK	B4
SD0_CMD	E12
SD0_DATA0	E10
SD0_DATA1	C4
SD0_DATA2	A13
SD0_DATA3	E6
SD0_LED	D8
SD0_PWR#	C12
SD0_WP	F8
SD1_CD#	A7
SD1_CLK	C14
SD1_CMD	A6
SD1_DATA0	B8
SD1_DATA1	G10
SD1_DATA2	A14
SD1_DATA3	C8
SD1_LED	E8
SD1_PWR#	C6
SD1_WP	B6
SD2_CD#	G12
SD2_CLK	F10
SD2_CMD	D10
SD2_DATA0	G11
SD2_DATA1	A10
SD2_DATA2	A12
SD2_DATA3	G9
SD2_DATA4	A9
SD2_DATA5	A11

Ball Name	Ball Number
SD2_DATA6	F12
SD2_DATA7	B10
SD2_LED	G8
SD2_PWR#	A5
SD2_WP	A8
SDVO_CTRLCLK	E16
SDVO_CTRLDATA	B16
SDVOB_BLUE	W36
SDVOB_BLUE#	V35
SDVOB_CLK	W32
SDVOB_CLK#	V31
SDVOB_GREEN	AA32
SDVOB_GREEN#	Y31
SDVOB_INT	AA30
SDVOB_INT#	Y29
SDVOB_RED	AA34
SDVOB_RED#	Y33
SDVOB_STALL	W34
SDVOB_STALL#	V33
SDVOB_TVCLKIN	AA36
SDVOB_TVCLKIN#	Y35
SLPMODE	E31
SLPRDY#	C33
SM_BS0	AJ25
SM_BS1	AH24
SM_BS2	AG32
SM_CAS#	AJ23
SM_CK0	AM35
SM_CK0#	AM34
SM_CK1	AJ19
SM_CK1#	AJ18
SM_CKE0	AL33
SM_CKE1	AJ33
SM_CS0#	AH22
SM_CS1#	AG23
SM_DQ0	AP34
SM_DQ1	AN33
SM_DQ10	AL29
SM_DQ11	AN29

Ball Name	Ball Number
SM_DQ12	AN31
SM_DQ13	AK30
SM_DQ14	AM30
SM_DQ15	AT30
SM_DQ16	AR29
SM_DQ17	AT29
SM_DQ18	AL27
SM_DQ19	AN27
SM_DQ2	AT32
SM_DQ20	AK28
SM_DQ21	AM28
SM_DQ22	AT28
SM_DQ23	AR27
SM_DQ24	AT27
SM_DQ25	AK26
SM_DQ26	AN25
SM_DQ27	AR25
SM_DQ28	AM26
SM_DQ29	AP26
SM_DQ3	AL31
SM_DQ30	AL25
SM_DQ31	AT25
SM_DQ32	AM24
SM_DQ33	AP24
SM_DQ34	AT23
SM_DQ35	AK22
SM_DQ36	AK24
SM_DQ37	AT24
SM_DQ38	AL23
SM_DQ39	AR23
SM_DQ4	AN35
SM_DQ40	AP22
SM_DQ41	AT22
SM_DQ42	AK20
SM_DQ43	AM20
SM_DQ44	AM22
SM_DQ45	AL21
SM_DQ46	AR21
SM_DQ47	AT21

Ball Name	Ball Number
SM_DQ48	AT20
SM_DQ49	AL19
SM_DQ5	AK32
SM_DQ50	AM18
SM_DQ51	AP18
SM_DQ52	AP20
SM_DQ53	AN19
SM_DQ54	AR19
SM_DQ55	AK18
SM_DQ56	AL17
SM_DQ57	AN17
SM_DQ58	AM16
SM_DQ59	AP16
SM_DQ6	AR33
SM_DQ60	AT18
SM_DQ61	AR17
SM_DQ62	AK16
SM_DQ63	AT16
SM_DQ7	AP32
SM_DQ8	AR31
SM_DQ9	AT31
SM_DQS0	AM32
SM_DQS1	AP30
SM_DQS2	AP28
SM_DQS3	AT26
SM_DQS4	AN23
SM_DQS5	AN21
SM_DQS6	AT19
SM_DQS7	AT17
SM_MA0	AH26
SM_MA1	AG27
SM_MA10	AG26
SM_MA11	AH32
SM_MA12	AH30
SM_MA13	AG22
SM_MA14	AG33
SM_MA2	AH28
SM_MA3	AJ27
SM_MA4	AG29

Ball Name	Ball Number
SM_MA5	AG28
SM_MA6	AG31
SM_MA7	AJ31
SM_MA8	AJ29
SM_MA9	AG30
SM_RAS#	AG24
SM_RCOMPO	AG36
SM_RCVENIN	AJ36
SM_RCVENOUT	AH35
SM_VREF	AK35
SM_WE#	AG25
SMB_ALERT#	F18
SMB_CLK	G21
SMB_DATA	F21
SMI#	C16
SPKR	C21
STPCPU#	G16
SUSCLK	B31
TCK	E34
TDI	D33
TDO	G34
THRM#	C18
TMS	G32
TRST#	F33
USB_CLK48	E36
USB_DN0	N32
USB_DN1	N34
USB_DN2	N36
USB_DN3	L32
USB_DN4	L36
USB_DN5	K33
USB_DN6	H35
USB_DN7	H33
USB_DP0	M31
USB_DP1	M33
USB_DP2	M35
USB_DP3	K31
USB_DP4	K35
USB_DP5	L34



Ball Name	Ball Number
USB_DP6	J36
USB_DP7	J34
USB_OC0#	K29
USB_OC1#	R30
USB_OC2#	L30
USB_OC3#	M29
USB_OC4#	J30
USB_OC5#	H29
USB_OC6#	P29
USB_OC7#	N30
USB_RBIASN	R36
USB_RBIASP	P35
VCC	AA12
VCC	AA13
VCC	AA15
VCC	AA17
VCC	AA19
VCC	AA21
VCC	AA23
VCC	AA24
VCC	AB13
VCC	AB14
VCC	AB15
VCC	AB16
VCC	AB17
VCC	AB18
VCC	AB19
VCC	AB20
VCC	AB21
VCC	AB22
VCC	AB23
VCC	M13
VCC	M14
VCC	M15
VCC	M17
VCC	M18
VCC	M19
VCC	M21
VCC	M22

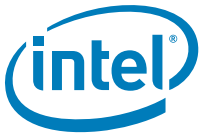
Ball Name	Ball Number
VCC	M23
VCC	N13
VCC	N15
VCC	N17
VCC	N19
VCC	N21
VCC	N23
VCC	P13
VCC	P15
VCC	P17
VCC	P19
VCC	P21
VCC	P23
VCC	R12
VCC	R13
VCC	R15
VCC	R17
VCC	R19
VCC	R21
VCC	R23
VCC	T13
VCC	T15
VCC	T17
VCC	T19
VCC	T21
VCC	U12
VCC	U13
VCC	U15
VCC	U17
VCC	U19
VCC	U21
VCC	V13
VCC	V15
VCC	V17
VCC	V19
VCC	V21
VCC	W12
VCC	W13
VCC	W15

Ball Name	Ball Number
VCC	W17
VCC	W19
VCC	W21
VCC	Y13
VCC	Y15
VCC	Y17
VCC	Y19
VCC	Y21
VCC	Y23
VCC15	J12
VCC15	J13
VCC15	J14
VCC15	J15
VCC15	J16
VCC15	J17
VCC15	J18
VCC15	J19
VCC15	J20
VCC15	J21
VCC15	J22
VCC15	J23
VCC15	J24
VCC15	K13
VCC15	K14
VCC15	K15
VCC15	K16
VCC15	K17
VCC15	K18
VCC15	K19
VCC15	K20
VCC15	K21
VCC15	K22
VCC15	K23
VCC15USB	U23
VCC15USB	U24
VCC15USB	V23
VCC15USB	V24
VCC15USB	W23
VCC15USB	W24

Ball Name	Ball Number
VCC33	H3
VCC33	H5
VCC33	H7
VCC33	J4
VCC33	J6
VCC33	J8
VCC33	J10
VCC33	K3
VCC33	K5
VCC33	K7
VCC33	K9
VCC33	K11
VCC33	L4
VCC33	L6
VCC33	L8
VCC33	L10
VCC33RTC	A30
VCC33SUS	L26
VCC33SUS	M25
VCC33SUS	M26
VCC33SUS	M27
VCC33SUS	P27
VCC5REF	L25
VCC5REFSUS	U27
VCCADPLLA	V26
VCCADPLLB	Y26
VCCAHPLL	AC11
VCCAPCIEBG	AB31
VCCAPCIEPLL	AA28
VCCAUSBBGSUS	U26
VCCAUSBPLL	W27
VCCDHPLL	AD11
VCCHDA	M12
VCCHDA	N12
VCCLVDS	V25
VCCLVDS	V27
VCCLVDS	W26
VCCLVDS	W28
VCCLVDS	Y27

Ball Name	Ball Number
VCCP33USBSUS	N26
VCCP33USBSUS	P25
VCCP33USBSUS	R25
VCCPCIE	AC28
VCCPCIE	AD26
VCCPCIE	AD27
VCCPCIE	AD28
VCCPCIE	AD29
VCCPCIE	AE25
VCCPCIE	AE26
VCCPCIE	AE27
VCCPCIE	AE28
VCCPCIE	AE29
VCCPCIE	AE30
VCCSDVO	AA25
VCCSDVO	AA26
VCCSDVO	AB25
VCCSDVO	AB26
VCCSDVO	AB27
VCCSDVO	AC25
VCCSM	AD12
VCCSM	AD13
VCCSM	AD14
VCCSM	AD15
VCCSM	AD16
VCCSM	AD17
VCCSM	AD18
VCCSM	AD19
VCCSM	AD20
VCCSM	AD21
VCCSM	AD22
VCCSM	AD23
VCCSM	AD24
VCCSM	AE12
VCCSM	AE13
VCCSM	AE14
VCCSM	AE15
VCCSM	AE16
VCCSM	AE17

Ball Name	Ball Number
VCCSM	AE18
VCCSM	AE19
VCCSM	AE20
VCCSM	AE21
VCCSM	AE22
VCCSM	AE23
VCCSM	AF12
VCCSM	AF15
VCCSM	AF18
VCCSM	AF19
VCCSM	AG12
VCCSM	AG13
VCCSM	AG15
VCCSM	AG18
VCCSM	AG19
VCCSM	AH12
VCCSM	AH13
VCCSM	AH14
VCCSM	AH15
VCCSM	AH16
VCCSM	AH17
VSS	A2
VSS	A3
VSS	A4
VSS	A33
VSS	A34
VSS	A35
VSS	A36
VSS	AA9
VSS	AA11
VSS	AA14
VSS	AA16
VSS	AA18
VSS	AA20
VSS	AA22
VSS	AA27
VSS	AA29
VSS	AA31
VSS	AA33



Ball Name	Ball Number
VSS	AA35
VSS	AB2
VSS	AB3
VSS	AB4
VSS	AB5
VSS	AB6
VSS	AB8
VSS	AB12
VSS	AB24
VSS	AB28
VSS	AB30
VSS	AB32
VSS	AB34
VSS	AB36
VSS	AC9
VSS	AC12
VSS	AC13
VSS	AC14
VSS	AC15
VSS	AC16
VSS	AC17
VSS	AC18
VSS	AC19
VSS	AC20
VSS	AC21
VSS	AC22
VSS	AC23
VSS	AC24
VSS	AC26
VSS	AC27
VSS	AC29
VSS	AC31
VSS	AC33
VSS	AC35
VSS	AD2
VSS	AD3
VSS	AD4
VSS	AD5
VSS	AD6

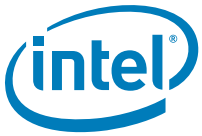
Ball Name	Ball Number
VSS	AD8
VSS	AD25
VSS	AD30
VSS	AD32
VSS	AD34
VSS	AD36
VSS	AE9
VSS	AE11
VSS	AE24
VSS	AE31
VSS	AE33
VSS	AE35
VSS	AF2
VSS	AF3
VSS	AF4
VSS	AF5
VSS	AF6
VSS	AF8
VSS	AF11
VSS	AF13
VSS	AF14
VSS	AF16
VSS	AF17
VSS	AF20
VSS	AF21
VSS	AF22
VSS	AF23
VSS	AF24
VSS	AF25
VSS	AF26
VSS	AF27
VSS	AF28
VSS	AF29
VSS	AF30
VSS	AF31
VSS	AF32
VSS	AF33
VSS	AF34
VSS	AF36

Ball Name	Ball Number
VSS	AG9
VSS	AG11
VSS	AG14
VSS	AG16
VSS	AG17
VSS	AG20
VSS	AG34
VSS	AG35
VSS	AH2
VSS	AH3
VSS	AH4
VSS	AH5
VSS	AH6
VSS	AH8
VSS	AH9
VSS	AH11
VSS	AH18
VSS	AH19
VSS	AH20
VSS	AH21
VSS	AH23
VSS	AH25
VSS	AH27
VSS	AH29
VSS	AH31
VSS	AH33
VSS	AH34
VSS	AH36
VSS	AJ9
VSS	AJ10
VSS	AJ11
VSS	AJ12
VSS	AJ13
VSS	AJ14
VSS	AJ15
VSS	AJ16
VSS	AJ17
VSS	AJ20
VSS	AJ22

Ball Name	Ball Number
VSS	AJ24
VSS	AJ26
VSS	AJ28
VSS	AJ30
VSS	AJ32
VSS	AJ34
VSS	AJ35
VSS	AK2
VSS	AK3
VSS	AK4
VSS	AK5
VSS	AK7
VSS	AK9
VSS	AK11
VSS	AK13
VSS	AK15
VSS	AK17
VSS	AK19
VSS	AK21
VSS	AK23
VSS	AK25
VSS	AK27
VSS	AK29
VSS	AK31
VSS	AK33
VSS	AK34
VSS	AK36
VSS	AL16
VSS	AL18
VSS	AL20
VSS	AL22
VSS	AL24
VSS	AL26
VSS	AL28
VSS	AL30
VSS	AL32
VSS	AL34
VSS	AL35
VSS	AL36

Ball Name	Ball Number
VSS	AM2
VSS	AM3
VSS	AM4
VSS	AM5
VSS	AM7
VSS	AM9
VSS	AM11
VSS	AM13
VSS	AM15
VSS	AM17
VSS	AM19
VSS	AM21
VSS	AM23
VSS	AM25
VSS	AM27
VSS	AM29
VSS	AM31
VSS	AM33
VSS	AM36
VSS	AN1
VSS	AN5
VSS	AN7
VSS	AN9
VSS	AN11
VSS	AN13
VSS	AN16
VSS	AN18
VSS	AN20
VSS	AN22
VSS	AN24
VSS	AN26
VSS	AN28
VSS	AN30
VSS	AN32
VSS	AN34
VSS	AN36
VSS	AP1
VSS	AP2
VSS	AP3

Ball Name	Ball Number
VSS	AP5
VSS	AP7
VSS	AP9
VSS	AP11
VSS	AP13
VSS	AP15
VSS	AP17
VSS	AP19
VSS	AP21
VSS	AP23
VSS	AP25
VSS	AP27
VSS	AP29
VSS	AP31
VSS	AP33
VSS	AP35
VSS	AP36
VSS	AR1
VSS	AR2
VSS	AR3
VSS	AR5
VSS	AR7
VSS	AR9
VSS	AR11
VSS	AR13
VSS	AR16
VSS	AR18
VSS	AR20
VSS	AR22
VSS	AR24
VSS	AR26
VSS	AR28
VSS	AR30
VSS	AR32
VSS	AR34
VSS	AR35
VSS	AR36
VSS	AT1
VSS	AT2



Ball Name	Ball Number
VSS	AT3
VSS	AT4
VSS	AT15
VSS	AT33
VSS	AT34
VSS	AT35
VSS	AT36
VSS	B1
VSS	B2
VSS	B3
VSS	B5
VSS	B7
VSS	B9
VSS	B11
VSS	B13
VSS	B15
VSS	B17
VSS	B20
VSS	B22
VSS	B24
VSS	B26
VSS	B28
VSS	B30
VSS	B32
VSS	B34
VSS	B35
VSS	B36
VSS	C1
VSS	C2
VSS	C3
VSS	C5
VSS	C7
VSS	C9
VSS	C10
VSS	C11
VSS	C13
VSS	C15
VSS	C17
VSS	C20

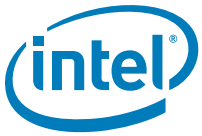
Ball Name	Ball Number
VSS	C22
VSS	C24
VSS	C26
VSS	C28
VSS	C30
VSS	C32
VSS	C35
VSS	C36
VSS	D1
VSS	D2
VSS	D4
VSS	D7
VSS	D9
VSS	D11
VSS	D13
VSS	D15
VSS	D17
VSS	D20
VSS	D22
VSS	D24
VSS	D26
VSS	D28
VSS	D30
VSS	D32
VSS	D34
VSS	D36
VSS	E3
VSS	E5
VSS	E7
VSS	E9
VSS	E11
VSS	E13
VSS	E15
VSS	E17
VSS	E20
VSS	E22
VSS	E24
VSS	E26
VSS	E28

Ball Name	Ball Number
VSS	E30
VSS	E33
VSS	E35
VSS	F1
VSS	F2
VSS	F4
VSS	F6
VSS	F9
VSS	F11
VSS	F13
VSS	F15
VSS	F17
VSS	F19
VSS	F20
VSS	F22
VSS	F24
VSS	F26
VSS	F32
VSS	F34
VSS	F35
VSS	F36
VSS	G1
VSS	G2
VSS	G3
VSS	G5
VSS	G7
VSS	G27
VSS	G29
VSS	G31
VSS	G33
VSS	G35
VSS	H1
VSS	H2
VSS	H4
VSS	H6
VSS	H8
VSS	H9
VSS	H10
VSS	H11

Ball Name	Ball Number
VSS	H12
VSS	H13
VSS	H14
VSS	H15
VSS	H16
VSS	H17
VSS	H18
VSS	H19
VSS	H20
VSS	H21
VSS	H22
VSS	H23
VSS	H24
VSS	H25
VSS	H26
VSS	H28
VSS	H30
VSS	H32
VSS	H34
VSS	H36
VSS	J1
VSS	J2
VSS	J3
VSS	J5
VSS	J7
VSS	J9
VSS	J11
VSS	J25
VSS	J27
VSS	J29
VSS	J31
VSS	J33
VSS	J35
VSS	K2
VSS	K4
VSS	K6
VSS	K8
VSS	K10
VSS	K12

Ball Name	Ball Number
VSS	K24
VSS	K25
VSS	K26
VSS	K27
VSS	K28
VSS	K30
VSS	K32
VSS	K34
VSS	K36
VSS	L2
VSS	L3
VSS	L5
VSS	L7
VSS	L9
VSS	L11
VSS	L12
VSS	L13
VSS	L14
VSS	L15
VSS	L16
VSS	L17
VSS	L18
VSS	L19
VSS	L20
VSS	L21
VSS	L22
VSS	L23
VSS	L24
VSS	L27
VSS	L28
VSS	L29
VSS	L31
VSS	L33
VSS	L35
VSS	M1
VSS	M2
VSS	M3
VSS	M4
VSS	M5

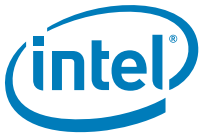
Ball Name	Ball Number
VSS	M6
VSS	M7
VSS	M8
VSS	M10
VSS	M11
VSS	M16
VSS	M20
VSS	M24
VSS	M28
VSS	M30
VSS	M32
VSS	M34
VSS	M36
VSS	N8
VSS	N9
VSS	N11
VSS	N14
VSS	N16
VSS	N18
VSS	N20
VSS	N22
VSS	N24
VSS	N25
VSS	N27
VSS	N28
VSS	N29
VSS	N31
VSS	N33
VSS	N35
VSS	P2
VSS	P3
VSS	P4
VSS	P5
VSS	P6
VSS	P8
VSS	P12
VSS	P14
VSS	P16
VSS	P18



Ball Name	Ball Number
VSS	P20
VSS	P22
VSS	P24
VSS	P26
VSS	P28
VSS	P30
VSS	P32
VSS	P34
VSS	P36
VSS	R9
VSS	R11
VSS	R14
VSS	R16
VSS	R18
VSS	R20
VSS	R22
VSS	R27
VSS	R28
VSS	R29
VSS	R31
VSS	R33
VSS	R35
VSS	T2
VSS	T3
VSS	T4
VSS	T5
VSS	T6
VSS	T8
VSS	T12
VSS	T14
VSS	T16
VSS	T18
VSS	T20
VSS	T22
VSS	T24
VSS	T28
VSS	T30
VSS	T32
VSS	T34

Ball Name	Ball Number
VSS	T36
VSS	U9
VSS	U11
VSS	U14
VSS	U16
VSS	U18
VSS	U20
VSS	U22
VSS	U29
VSS	U31
VSS	U33
VSS	U35
VSS	V2
VSS	V3
VSS	V4
VSS	V5
VSS	V6
VSS	V8
VSS	V12
VSS	V14
VSS	V16
VSS	V18
VSS	V20
VSS	V22
VSS	V28
VSS	V30
VSS	V32
VSS	V34
VSS	V36
VSS	W9
VSS	W11
VSS	W14
VSS	W16
VSS	W18
VSS	W20
VSS	W22
VSS	W25
VSS	W29
VSS	W31

Ball Name	Ball Number
VSS	W33
VSS	W35
VSS	Y2
VSS	Y3
VSS	Y4
VSS	Y5
VSS	Y6
VSS	Y8
VSS	Y12
VSS	Y14
VSS	Y16
VSS	Y18
VSS	Y20
VSS	Y22
VSS	Y24
VSS	Y25
VSS	Y28
VSS	Y30
VSS	Y32
VSS	Y34
VSS	Y36
VSSAPCIEBG	AC32
VSSAUSBBGSUS	T26
VTT	AA10
VTT	AB9
VTT	AB10
VTT	AB11
VTT	AC10
VTT	AD9
VTT	AD10
VTT	AE10
VTT	AF9
VTT	AF10
VTT	AG10
VTT	AH10
VTT	M9
VTT	N10
VTT	P9
VTT	P10



Ball Name	Ball Number
VTT	P11
VTT	R10
VTT	T9
VTT	T10
VTT	T11
VTT	U10
VTT	V9
VTT	V10
VTT	V11
VTT	W10
VTT	Y9
VTT	Y10
VTT	Y11
WAKE#	C31
XOR_TEST	G6

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