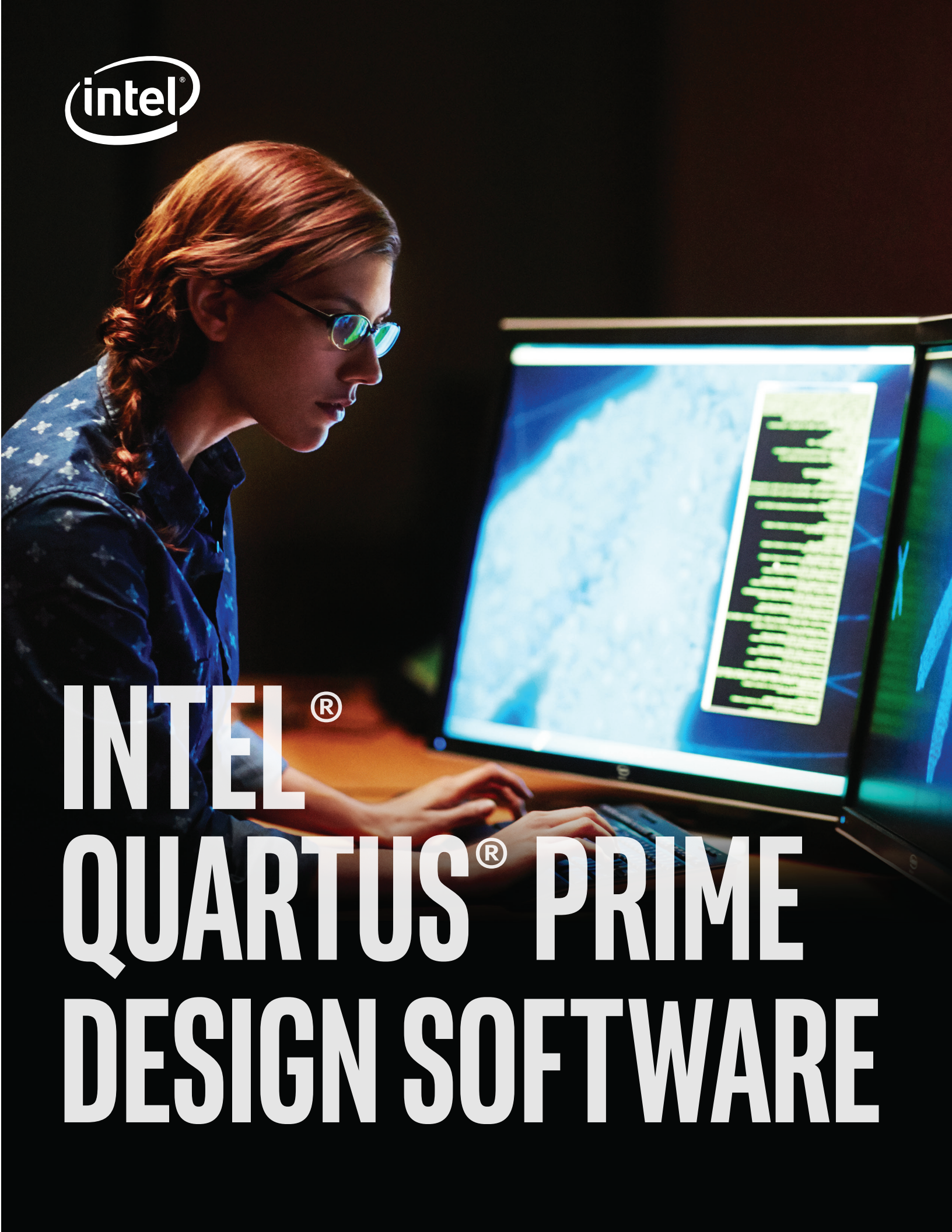


INTEL® QUARTUS® PRIME DESIGN SOFTWARE

A FAST PATH TO YOUR DESIGN

The Intel® Quartus® Prime software is revolutionary in performance and productivity for FPGA, CPLD, and SoC designs, providing a fast path to convert your concept into reality. The Intel Quartus Prime software can easily adapt to your specific needs in all phases of FPGA, CPLD, and SoC design in different platforms.

The Intel Quartus Prime software provides everything you need to design with Intel FPGAs. Key tools and features include:

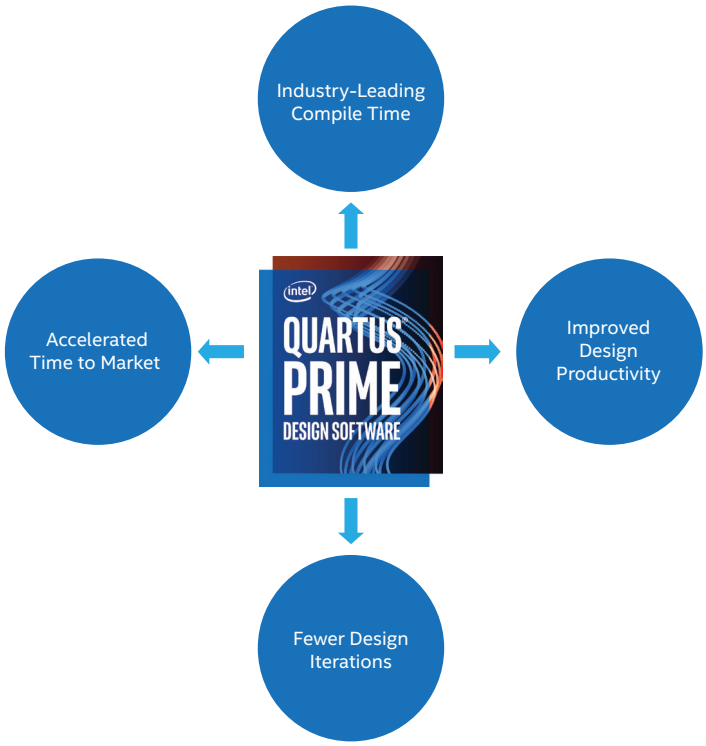
- Platform Designer
- Interface Planner
- Intel HLS Compiler
- Power Analyzer
- Timing Analyzer
- DSP Builder for Intel FPGAs
- ModelSim-Intel FPGA

INTEL QUARTUS PRIME SOFTWARE EDITIONS

The Intel Quartus Prime software is available in three editions based on your design requirements: Pro, Standard, and Lite Edition.

- **Intel Quartus Prime Pro Editon**–The Intel Quartus Prime Pro Edition software is optimized to support the advanced features in Intel's next-generation FPGAs and SoCs with the Intel Agilex™, Intel Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 GX device family.
- **Intel Quartus Prime Standard Edition**–The Intel Quartus Prime Standard Edition software includes extensive support for earlier device families in addition to the Intel Cyclone 10 LP and Intel MAX® 10 device family.
- **Intel Quartus Prime Lite Edition**–The Intel Quartus Prime Lite Edition software provides an ideal entry point to Intel's high-volume device families and is available as a free download with no license file required.

Intel Quartus Prime Software Key Benefits



FEATURES

Partial Reconfiguration

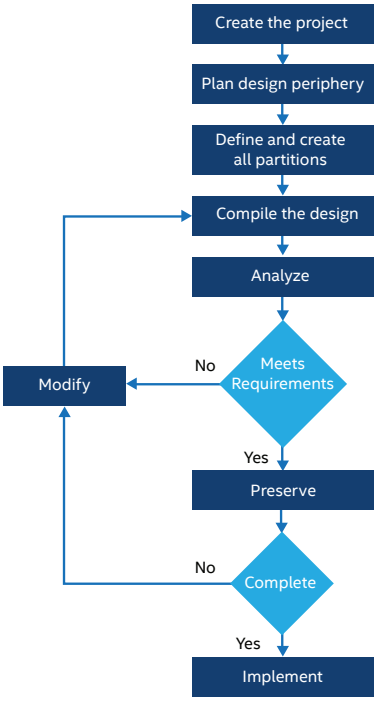
Partial reconfiguration of the FPGA offers several benefits and enables new applications. The Intel Quartus Prime Pro Edition software features an intuitive flow with graphical user interface support for partial reconfiguration of Intel Arria 10 FPGAs and SoCs. Designers can visually optimize the floorplan of the dynamic region that needs to be reconfigured in the chip planner. Constraints can be easily assigned using the Logic Lock Region feature in the Intel Quartus Prime Pro Edition software.

The key benefits of partial reconfiguration are:

- Lower cost
- Smaller board footprint
- Lower power

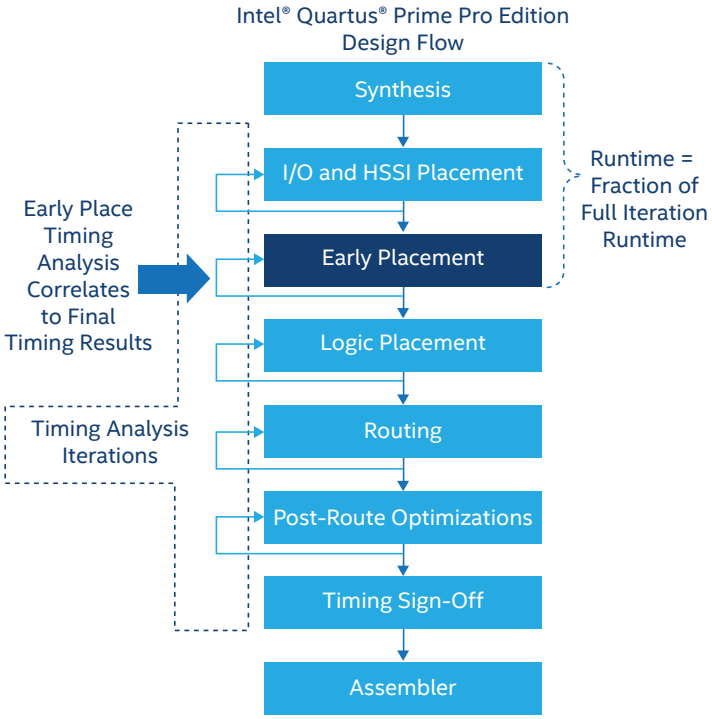
Block-Based Design

The Intel Quartus Prime Pro Edition design software offers block-based design flows. They are of two types- the Incremental Block-Based Compilation and Design Block Reuse flows, which allow your geographically diverse development team to collaborate on a design.



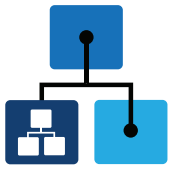
Incremental Optimization Reduces Full Design Iterations

The incremental capability optimizations in the Intel Quartus Prime Pro Edition software offers a faster methodology to converge to design sign-off. The Intel Quartus Prime Pro Edition software boosts the incremental optimization capability with an early placement stage. This stage, in addition to the I/O and HSSI placement, logic placement, routing, and post-route optimizations offers a more granular convergence to design closure.



PLATFORM DESIGNER (FORMERLY QSYS)

Platform Designer (Pro Edition) is the next-generation system integration tool in the Intel Quartus Prime Pro Edition software and builds on the capabilities of Platform Designer (Standard Edition), which is supported in the Intel Quartus Prime Standard Edition software. Both the Platform Designer (Standard and Pro Editions) save significant time and effort in the FPGA design process by automatically generating interconnect logic to connect intellectual property (IP) functions and subsystems. The new Platform Designer (Pro Edition) tool also supports a variety of design entry methods, such as register transfer level (RTL), block-based design entry, to schematic entry, and black boxes.



Hierarchical Framework

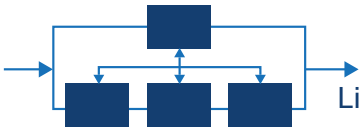
Platform Designer (formerly Qsys) Pro Edition

STANDARD INTERCONNECTS	
AMBA® Interconnect Standards from ARM	AXI, AHB, APB
Intel® FPGA	Avalon® Interfaces
IP-XACT	Design Descriptors

DESIGN REUSE

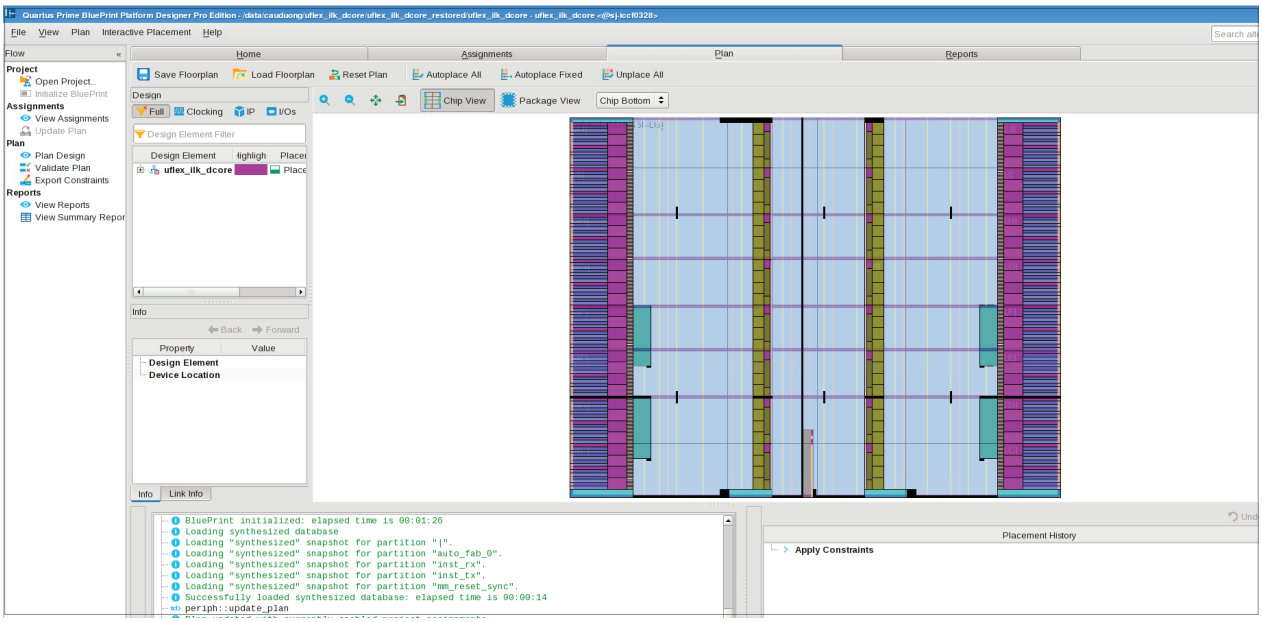
Multiple Sources

RTL
"Black Box"
OpenCL™ Kernel
DSP Builder for Intel FPGAs Subsystem



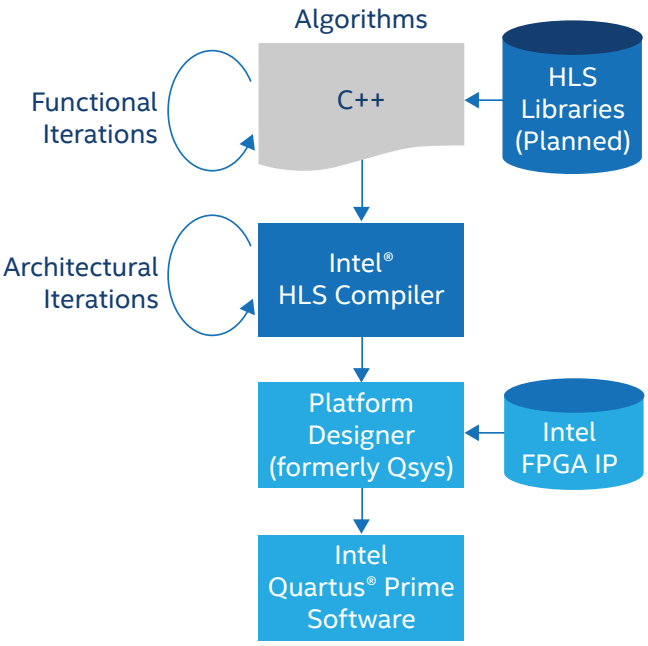
INTERFACE PLANNER

The Interface Planner explores a device's peripheral architecture and efficiently assigns interfaces. The Interface Planner prevents illegal pin assignments by performing fitter and legal checks in real time. This flow eliminates complex error messages and the need to wait for a full compile, thereby speeding up your I/O design by 10X. †



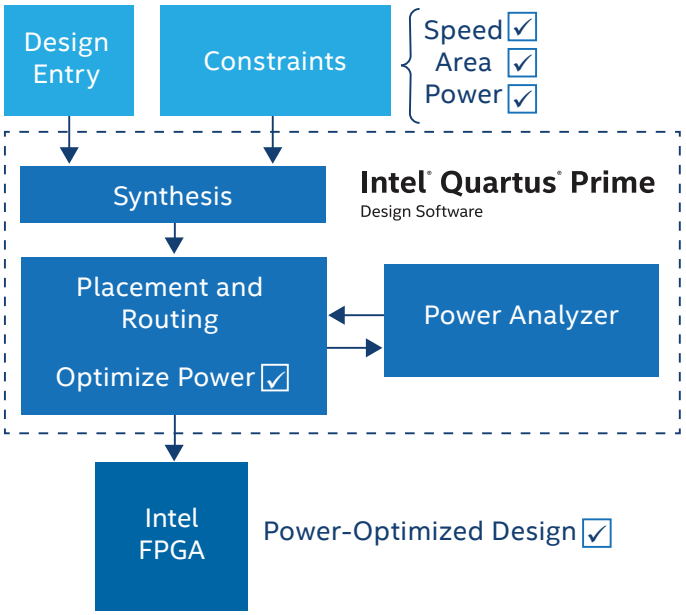
INTEL HLS COMPILER

Intel HLS Compiler is a high-level synthesis (HLS) tool that takes in untimed C++ as input and generates production-quality register transfer level (RTL) that is optimized for Intel FPGAs. The figure below shows the Intel HLS Compiler tool flow, which enables an accelerated time for development that rivals hand-coded RTL. Creating FPGA accelerators can be cumbersome if customers wish to stick to traditional RTL flows. Therefore, we developed the Intel HLS Compiler tool. It is great for those who have already mastered the back-end flow, from high-level design to bit stream to run on the FPGA. Our high-level synthesis compiler allows you to generate RTL code that can be loaded into the Platform Designer (formerly Qsys) using C++.



POWER ANALYZER

Power analysis technology features the new Power and Thermal Calculator (PTC) for Intel Stratix 10 and Intel Agilex devices, the Excel-based early power estimator (EPE), and the power analyzer tool in the Intel Quartus Prime software. These power analysis tools give you the ability to estimate power consumption from early design concept through design implementation.



TIMING ANALYZER

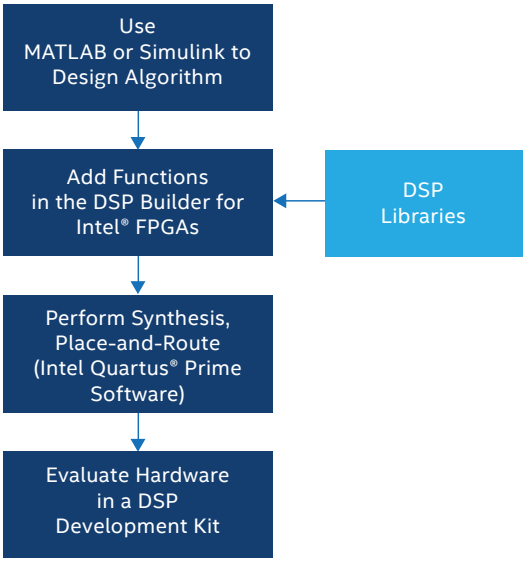
This is the second generation, easy-to-use timing analyzer that leverages industry-standard Synopsys Design Constraints (SDC) support to achieve accurate timing, resulting in faster timing closure.

DSP BUILDER FOR INTEL FPGAS

The DSP Builder for Intel FPGAs software generates HDL for digital signal processing (DSP) algorithms in model-based design flow. The DSP Builder for Intel FPGAs software integrates the algorithm development, simulation, and verification capabilities of MathWorks MATLAB and Simulink system-level design tools with the Intel Quartus Prime design software. You can shorten DSP design cycles by creating the hardware representation of a DSP design in an algorithm-friendly development environment. The DSP Builder for Intel FPGAs software consists of Standard Blockset and Advanced Blockset. The Advanced Blockset version is recommended for new designs.

Features:

- Provides superior fixed-point and IEEE 754 single-precision, floating-point DSP implementation with vector processing
- Offers bit-accurate and cycle-accurate simulation models
- Performs automatic generation of VHDL test benches
- Facilitates integration of complex DSP functions



MODELSIM-INTEL FPGA EDITION SOFTWARE

The ModelSim-Intel FPGA Edition software is a version of the ModelSim software licensed from Mentor Graphics targeted for Intel devices. The software supports Intel FPGA gate-level simulation libraries and includes behavioral simulation, HDL testbenches, and Tcl scripting. The ModelSim-Intel FPGA Edition software supports dual-language simulation. This includes designs that are written in a combination of Verilog, SystemVerilog, and VHDL languages, also known as mixed HDL.

Both the ModelSim-Intel FPGA Edition software and ModelSim-Intel FPGA Starter Edition software are available for all versions of the Intel Quartus Prime software. The ModelSim-Intel FPGA Starter Edition software is the same as the ModelSim-Intel FPGA Edition software except for the following areas:

- The ModelSim-Intel FPGA Edition software is licensed
- The ModelSim-Intel FPGA Starter Edition software simulation performance is lower than that of ModelSim-Intel FPGA Edition, and has a line limit of 10,000 executable lines compared to an unlimited number of lines allowed in the ModelSim-Intel FPGA Edition software

INTEL QUARTUS PRIME DESIGN SOFTWARE

www.intel.com/quartus

The Intel Quartus Prime software is revolutionary in performance and productivity for FPGA, CPLD, and SoC designs, providing a fast path to convert your concept into reality. The Intel Quartus Prime software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

INTEL QUARTUS PRIME DESIGN SOFTWARE			AVAILABILITY		
			PRO EDITION ($)	STANDARD EDITION ($)	LITE EDITION (FREE)
Device Support	Intel Agilex series		✓		
	Intel Stratix series	IV, V		✓	
		10	✓		
	Intel Arria series	II			✓[1]
		II, V		✓	
		10	✓	✓	
	Intel Cyclone series	IV, V		✓	✓
		10 LP		✓	✓
		10 GX	✓[2]		
	Intel MAX series	II, V, 10		✓	✓
Design Flow	Partial reconfiguration		✓	✓[3]	
	Rapid recompile		✓	✓[4]	
	Block-based design		✓		
	Incremental optimization		✓		
Design Entry/Planning	IP Base Suite		✓	✓	Available for purchase
	Intel HLS Compiler		✓	✓	✓
	Platform Designer (Standard)			✓	✓
	Platform Designer (Pro)		✓		
	Design Partition Planner		✓	✓	
	Chip Planner		✓	✓	✓
	Interface Planner		✓		
	Logic Lock regions		✓	✓	
	VHDL		✓	✓	✓
	Verilog		✓	✓	✓
	SystemVerilog		✓	✓[5]	✓[5]
	VHDL-2008		✓	✓[5]	
Functional Simulation	ModelSim-Intel FPGA Starter Edition software		✓	✓	✓
	ModelSim-Intel FPGA Edition software		✓[7]	✓[6]	✓[6]
Compilation (Synthesis & Place and Route)	Fitter (Place and Route)		✓	✓	✓
	Early placement		✓		
	Register retiming		✓	✓	
	Fractal synthesis		✓		
	Multiprocessor support		✓	✓	
Timing and Power Verification	Timing Analyzer		✓	✓	✓
	Design Space Explorer II		✓	✓	✓
	Power Analyzer		✓	✓	✓
In-System Debug	Signal Tap Logic Analyzer		✓	✓	✓
	Transceiver toolkit		✓	✓	
	Intel Advanced Link Analyzer		✓	✓	
Operating System (OS) Support	Windows/Linux 64 bit support		✓	✓	✓
Price			Buy Fixed - $3,995 Float - $4,995	Buy Fixed - $2,995 Float - $3,995	Free
Download			Download Now	Download Now	Download Now

Notes:
1. The only Arria II FPGA supported is the EP2AGX45 device.
2. The Intel Cyclone 10 GX device support is available for free in the Pro Edition software.
3. Available for Cyclone V and Stratix V devices only and requires a partial reconfiguration license.
4. Available for Stratix V, Arria V, and Cyclone V devices.
5. Limited language support.
6. Requires an additional license.

ADDITIONAL DEVELOPMENT TOOLS

TOOLS	DESCRIPTION
Intel FPGA SDK for OpenCL™	• No additional licenses are required. • Supported with the Intel Quartus Prime Pro/Standard Edition software. • The software installation file includes the Intel Quartus Prime Pro/Standard Edition software and the OpenCL software.
Intel HLS Compiler	• No additional license required. • Now available as a separate download. • Supported with all editions of the Intel Quartus Prime software.
DSP Builder for Intel FPGAs	• Additional licenses are required. • DSP Builder for Intel FPGAs (Advanced Blockset only) is supported with the Intel Quartus Prime Pro Edition software for Intel Agilex, Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices. • DSP Builder for Intel FPGAs (Standard Blockset and Advanced Blockset) is supported with the Intel Quartus Prime Standard Edition software for Intel Arria 10, Intel Cyclone 10 LP, Intel MAX 10, Stratix V, Arria V, and Cyclone V devices.
Nios® II Embedded Design Suite	• No additional licenses are required. • Supported with all editions of the Intel Quartus Prime software. • Includes Nios II software development tools and libraries.
Intel SoC FPGA Embedded Development Suite (SoC EDS)	• Requires additional licenses for Arm Development Studio (DS) Intel SoC FPGA Edition. • The SoC EDS Standard Edition is supported with the Intel Quartus Prime Lite/Standard Edition software and the SoC EDS Pro Edition is supported with the Intel Quartus Prime Pro Edition software.

INTEL QUARTUS PRIME DESIGN SOFTWARE FEATURES SUMMARY

Interface Planner	Enables you to quickly create your I/O design using real time legality checks.
Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
Platform Designer	Accelerates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect based on a network-on-a-chip architecture.
Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Intel and from Intel's third-party IP partners.
Synthesis	Provides expanded language support for System Verilog and VHDL 2008.
Scripting support	Supports command-line operation and Tcl scripting.
Rapid recompile	Maximizes your productivity by reducing your compilation time for small design after a full compile. Improves design timing preservation.
Incremental optimization	Offers a faster methodology to converge to design sign-off. The traditional fitter stage is divided into finer stages for more control over the design flow.
Partial reconfiguration	Creates a physical region on the FPGA that can be reconfigured to execute different functions. Synthesize, place, route, close timing, and generate configuration bitstreams for the functions implemented in the region.
Block-based design flows	Provides flexibility of reusing timing-closed modules or design blocks across projects and teams.
Intel Hyperflex FPGA Architecture	Provides increased core performance and power efficiency for Intel Agilex and Intel Stratix 10 devices.
Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Intel Quartus Prime software settings to find optimal results.
Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
Chip planner	Reduces verification time while maintaining timing closure by enabling small, post-placement and routing design changes to be implemented in minutes.
Timing Analyzer	Provides native Synopsys Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
Signal Tap logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
Power Analyzer	Enables you to analyze and optimize both dynamic and static power consumption accurately.
Design Assistant	A design rules checking tool that allows you to get to design closure faster by reducing the number of iterations needed and by enabling faster iterations with targeted guidance provided by the tool at various stages of compilation.
Fractal synthesis	Enables the Intel Quartus Prime software to efficiently pack arithmetic operations in FPGA's logic resources resulting in significantly improved performance.
EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit www.intel.com/fpgaedapartners.

Getting Started Steps

Step 1: Download the free Intel Quartus Prime Lite Edition software
www.intel.com/quartus

Step 2: Get oriented with the Intel Quartus Prime software interactive tutorial
After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training
www.intel.com/fpgatraining

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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