
intel
Intel®
FPGA
Product
Catalog
Version 21.3

Contents

Intel FPGA and Custom Logic Solutions Portfolio

Intel delivers a broad portfolio of custom logic solutions — FPGAs, SoCs, structured ASICs, and CPLDs—together with software tools, intellectual property (IP), embedded processors, customer support, and technical training. Intel's product leadership, excellent value, and superior quality of service give you a measurable advantage. Bring your great ideas to life faster, better, and more cost effectively.

FPGAs, Structured ASICs, and CPLDs

Intel FPGAs and CPLDs give you the flexibility to innovate, differentiate, and stay ahead in the market. We have five classes of FPGAs to meet your market needs, from the industry's highest density and performance to the most cost effective.

Intel Agilex FPGAs

The Intel Agilex FPGA family, built on 10 nm SuperFin technology, enables customized acceleration and connectivity for a wide range of compute and bandwidth intensive applications, while providing an improvement in performance and reduction in power.

Intel Cyclone Series

The Intel Cyclone FPGA series is built to meet your low-power, cost-sensitive design needs, enabling you to get to market faster.

Intel Stratix Series

The Intel Stratix FPGA and SoC family enables you to deliver high-performance, state-of-the-art products to market faster with lower risk and higher productivity.

Intel MAX Series

The Intel MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single-chip small form.

Intel Arria Series

The Intel Arria device family delivers performance and power efficiency in the midrange.

Intel eASIC Devices

Intel eASIC structured ASIC devices complete the gap between FPGA and ASIC by delivering lower power and lower unit price versus FPGAs and lower non-recurring engineering (NRE) and faster time to market versus standard cell ASICs.

Power Solutions

Power your systems with Intel Enpirion Power Solutions. Our integrated power management products provide a combination of small footprint, low-noise performance, and high efficiency. Intel Enpirion power system-on-chip (PowerSoC) products provide a qualified and reliable solution that enables you to complete your design faster.

Acceleration Platform or Card Solutions

Intel FPGA-based acceleration platforms or cards enable a scalable volume deployment of various workloads in edge, network, cloud, enterprise, and other types of data center environment through Intel FPGA Programmable Acceleration Cards and development software, such as the Intel Acceleration Stack for Intel Xeon CPU with FPGAs and the OpenVINO™ toolkit.

Productivity-Enhancing Design Software, Embedded Processing, IP, Development Kits, and Training

With Intel, you get a complete design environment and a wide choice of design tools—all built to work together so your designs are up and running fast. You can try one of our training classes to get a jump-start on your designs. Choose Intel and see how we enhance your productivity and make a difference to your bottom line.

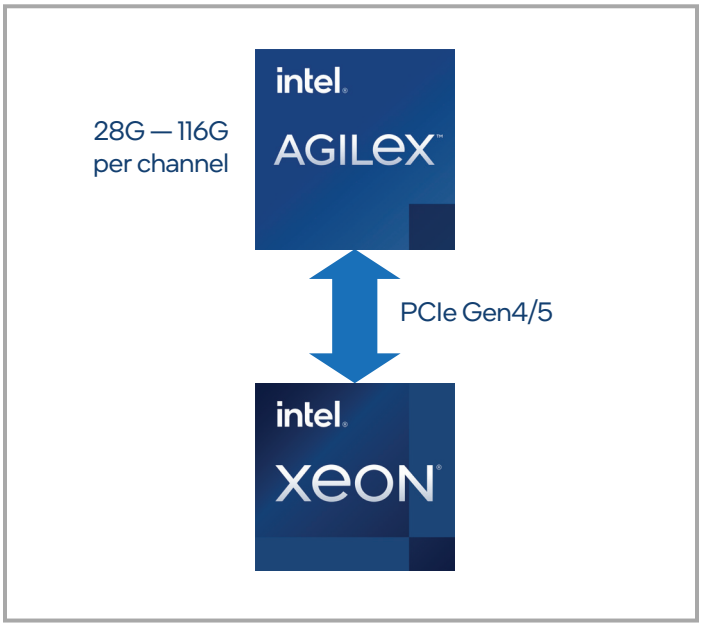
Intel Agilex FPGA and SoC Overview

www.intel.com/agilex

The Intel Agilex FPGA family leverages heterogeneous 3D system-in-package (SiP) technology to integrate Intel's first FPGA fabric built on 10 nm SuperFin technology and the second-generation Intel® Hyperflex™ FPGA Architecture to deliver up to 45% higher performance (geometric mean vs. Intel® Stratix® 10 FPGA)[1] or up to 40% lower power[1] for data center, networking, and edge applications. Intel Agilex SoC FPGAs also integrate the quad-core Arm Cortex-A53 processor to provide high system integration.

INTEL AGILEX F-SERIES FPGAs AND SoCs	INTEL AGILEX I-SERIES SoC FPGAs	INTEL AGILEX M-SERIES SoC FPGAs
Intel Agilex F-Series FPGAs and SoC FPGAs bring together transceiver support up to 58 Gbps, increased digital signal processing (DSP) capabilities, hardened high performance cryptographic blocks, high system integration, and second-generation Intel Hyperflex FPGA architecture for a wide range of data center, networking, and edge applications. The Intel Agilex F-Series FPGA and SoC family also provides the option to integrate the quad-core Arm Cortex-A53 processor to provide high system integration.	Intel Agilex I-Series SoC FPGAs are optimized for high-performance processor interface and bandwidth-intensive applications. Cache and memory coherent attach to Intel Xeon® processors with Compute Express Link (CXL), hardened PCI Express (PCIe) Gen5 support, and transceiver support up to 116 Gbps make the Intel Agilex I-Series SoC FPGAs a compelling choice for applications that demand massive interface bandwidth and high performance.	Intel Agilex M-Series SoC FPGAs are optimized for compute and memory intensive applications. With cache and memory coherent attach to Intel Xeon processors, high-bandwidth memory integration, hardened DDR5 controller, and Intel Optane™ persistent memory support, the Intel Agilex M-Series SoC FPGAs are optimized for data-intensive applications that need massive memory in addition to high bandwidth. Coming soon.

Efficient Network Transformation



Datapath Acceleration

VNF Performance Optimization

- Load balancing
- Data integrity
- Network translation

Significant Improvements

- Throughput
- Jitter
- Latency

Infrastructure Offload

Optimized Architecture

- SmartNIC
- vRouter
- Security

Small Form Factor and Low Power

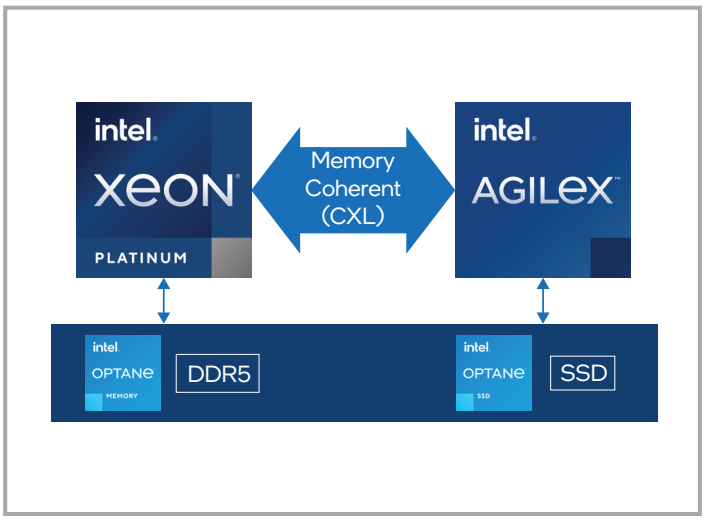
- Wide range of servers

Product and Performance Information:

[1] This comparison is based on the Intel Agilex FPGA and SoC family vs. Intel Stratix 10 FPGA family using simulation results and is subject to change. This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications, and roadmaps.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer. No computer system can be absolutely secure. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

Converged Workload Acceleration for the Data Center

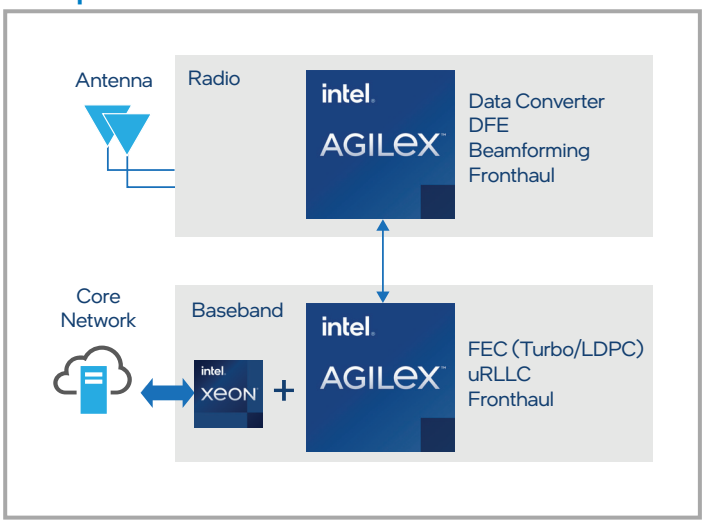


Infrastructure Acceleration
- Network
- Security
- Remote memory access

Application Acceleration
- Artificial intelligence (AI)
- Search
- Video transcode
- Database
- 40 TFLOPs of DSP performance[1]

Storage Acceleration
- Compression
- Decompression
- Encryption
- Memory hierarchy management

Agility and Flexibility for All Stages of 5G Implementation



Custom Logic Continuum

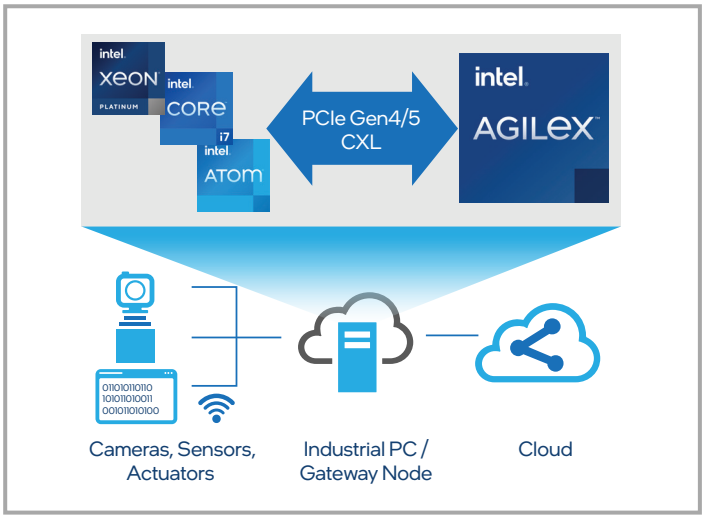
FPGA Flexibility
- High flexibility
- Short time to market

Rapid Intel eASIC Device Optimization
- Power and cost optimization

Full Custom ASIC Optimization
- Best power[1]
- Best performance[1]
- Best cost[1]

Application-Specific Tile Options
- Data converter
- Vector engine
- Custom compute

Smart, Safe, and Secure Factory Acceleration



Acceleration and Analytics
- In-line protocol acceleration
- Look-aside application acceleration

Safety and Security
- Secure boot
- Encryption
- Authentication

Customized Connectivity
- Time-sensitive networks
- Flexible I/O

Product and Performance Information:
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Intel Agilex FPGA and SoC Features - F Series

View device ordering codes on page 50.

PRODUCT LINE		AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 022	AGF 023	AGF 027
Resources	Logic elements (LEs)	573,480	764,640	1,178,525	1,437,240	1,918,975	2,208,075	2,308,080	2,692,760
	Adaptive logic modules (ALMs)	194,400	259,200	399,500	487,200	650,500	748,500	782,400	912,800
	ALM registers	777,600	1,036,800	1,598,000	1,948,800	2,602,000	2,994,000	3,129,600	3,651,200
	High-performance crypto blocks	0	0	0	0	2	0	2	0
	eSRAM memory blocks	0	0	2	2	1	0	1	0
	eSRAM memory size (Mb)	0	0	36	36	18	0	18	0
	M20K memory blocks	2,844	3,792	5,900	7,110	8,500	10,900	10,464	13,272
	M20K memory size (Mb)	56	74	115	139	166	212	204	259
	MLAB memory count	9,720	12,960	19,975	24,360	32,525	37,425	39,120	45,640
	MLAB memory size (Mb)	6	8	12	15	20	23	24	28
	I/O PLL	12	12	16	16	10	16	10	16
	Variable-precision digital signal processing (DSP) blocks	1,640	2,296	3,743	4,510	1,354	6,250	1,640	8,528
	18 x 19 multipliers	3,280	4,592	7,486	9,020	2,708	12,500	3,280	17,056
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.5 / 5.0	3.5 / 6.9	6.0 / 12.0	6.8 / 13.6	2.0 / 4.0	9.4 / 18.8	2.5 / 5.0	12.8 / 25.6
	Maximum EMIF x72	2	2	4	4	2	4	2	4
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	192	288	384	384	240	384	240	384
	AIB interfaces	2	2	2	2	4	4	4	4
	Memory devices supported	DDR4, QDR IV							
	Secure data manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection							
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4							
Tile Resources	F-Tile	PCI Express (PCIe) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbps FEC/PCS) 300G Interlaken IEEE 1588 v2 support PMA direct							
	E-Tile	Transceiver channel count : Up to 24 channels at 28.9 Gbps (NRZ) / 12 channels at 58 Gbps (PAM4) - RS & KP FEC[1] Networking support : - 400GbE (4 x 100GbE hard IP blocks (10/25 GbE FEC/PCS/MAC)) IEEE 1588 v2 support PMA direct							
	P-Tile	PCIe hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) SR-IOV 8PF / 2kVF VirtIO support Scalable IOV							

PRODUCT LINE	AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 022	AGF 023	AGF 027
F- Tile - Package Options and I/O Pins					**GPIO (LVDS) / F-Tile 32G NRZ (58G PAM4)**			
1546A (F-Tile x2) (37.5 mm x 34 mm, 0.92 mm Hex)	384(192)/ 32(24)	384(192)/ 32(24)						
2340A (F-Tile x2) (45 mm x 42 mm, 0.92 mm Hex)	576 (288)/ 32(24)	576 (288)/ 32(24)	744(372)/ 32(24)	744(372)/ 32(24)	480(240)/ 32(24)	744(372)/ 32(24)	480(240)/ 32(24)	744(372)/ 32(24)
3184C (F-Tile x4) (56 mm x 45 mm, 0.92 mm Hex)					480(240)/ 64(48)	720(360)/ 64(48)	480(240)/ 64(48)	720(360)/ 64(48)
E-Tile and P-Tile - Package Options and I/O Pins					**GPIO (LVDS) / E-Tile 28.9G NRZ (57.8G PAM4) / P-Tile 16G PCIe**			
2486A (E-Tile x1 & P-Tile x1) (55 mm x 42.5 mm, 1.0 mm Hex)			768(384)/ 16(8)/16	768(384)/ 16(8)/16				
2581A (E-Tile x1 & P-Tile x2) (50 mm x 40.5 mm, 0.92/0.94 mm Hex)[2]					480(240)/ 24(12)/32	624(312)/ 24(12)/32	480(240)/ 24(12)/32	624(312)/ 24(12)/32

Notes:
1. Only 4 instances of KP-FEC are supported when using 100GE MAC.
2. Conditional migration path from AGF 019/023 to AGF 022/027 devices.

Intel Agilex SoC FPGA Features - I Series

View device ordering codes on page 50.

PRODUCT LINE		AGI 019	AGI 022	AGI 023	AGI 027
Resources	Logic elements (LEs)	1,918,975	2,208,075	2,308,080	2,692,760
	Adaptive logic modules (ALMs)	650,500	748,500	782,400	912,800
	ALM registers	2,602,000	2,994,000	3,129,600	3,651,200
	High-performance crypto blocks	2	0	2	0
	eSRAM memory blocks	1	0	1	0
	eSRAM memory size (Mb)	18	0	18	0
	M20K memory blocks	8,500	10,900	10,464	13,272
	M20K memory size (Mb)	166	212	204	259
	MLAB memory count	32,525	37,425	39,120	45,640
	MLAB memory size (Mb)	20	23	24	28
	I/O PLL	10	16	10	16
	Variable-precision digital signal processing (DSP) blocks	1,354	6,250	1,640	8,528
	18 x 19 multipliers	2,708	12,500	3,280	17,056
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.4 /4.9	9.4 / 18.8	2.4 / 4.9	12.8/25.6
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	240	360	240	360
	AIB interaces	4	4	4	4
	Memory devices supported	DDR4 and QDR IV			
	Secure data manager	AES-256/SHA-256 bitstream encryption or authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection			
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache , NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4			
Tile Resources	F-Tile	PCI Express (PCIe) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) 300G Interlaken IEEE 1588 support PMA direct			
	R-Tile	Compute Express Interface (CXL) - Link width x16 lanes, x8 lanes PCIe hard IP block (Gen5 x16) or Bifurcateable 2x PCIe Gen5 x8 (EP) or 4x Gen5 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO support Precise time management PIPE direct			

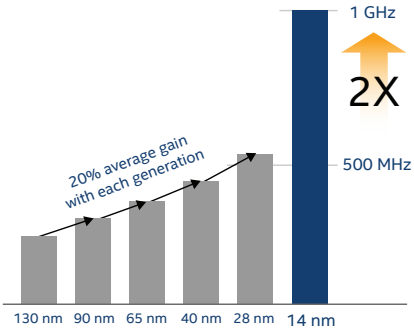
PRODUCT LINE	AGI 019	AGI 022	AGI 023	AGI 027
F- Tile - Package Options and I/O Pins	**GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) Channels**			
3184B (F-Tile x4) (56 mm x 45 mm, 0.92 mm Hex)		720(360) / 64(48) / 8(8)	480(240) / 64(48) / 8(8)	720(360) / 64(48) / 8(8)
F-Tile and R-Tile - Package Options and I/O Pins	**GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ(116G PAM4) Channels / R- Tile 32G PCIe (CXL) lanes**			
2957A (F-Tile x1 & R-Tile x 3) (56 mm x 45 mm, 1.0 / 0.92 mm Hex)		720(360)/16(12)/4(4)/ 48(32)		720(360)/16(12)/4(4)/ 48(32)
3184A (F-Tile x3 & R-Tile x1) (56 mm x 45 mm, 0.92 mm Hex)		720(360)/48(36)/8(8)/ 16(16)		720(360)/48(36)/8(8)/ 16(16)
1935A (F-Tile x1 & R-Tile x 1) (42.5mm x 42.5mm, 1.025 mm Hex)	480(240)/16(12)/0(0)/ 16(16)		480(240)/16(12)/0(0)/ 16(16)	

Generation 10 FPGAs and SoCs

Intel's Generation 10 FPGAs and SoCs are optimized based on process technology and architecture to deliver the industry's highest performance and highest levels of system integration at the lowest power. Generation 10 device families include Intel Stratix 10 FPGAs and SoCs, Intel Arria 10 FPGAs and SoCs, Intel Cyclone 10 FPGAs, and Intel MAX 10 FPGAs.

Intel® Stratix® 10

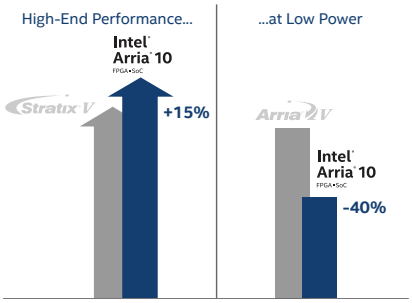
FPGA ▪ SoC



- 2X core performance with revolutionary Intel Hyperflex FPGA architecture†
- Up to 70% power savings†
- Highest density FPGA with up to 10.2 M logic elements (LEs)
- 64 bit quad-core Arm Cortex-A53 processor system
- Up to 10 tera floating point operations per second (TFLOPS) single-precision floating-point throughput
- Built on Intel's 14 nm Tri-Gate process technology

Intel® Arria® 10

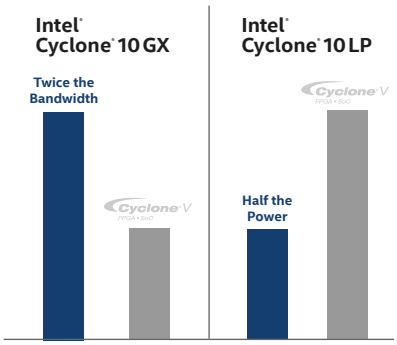
FPGA ▪ SoC



- 15% higher performance than the previous high-end devices†
- 40% lower midrange power†
- 1.5 GHz dual-core Arm Cortex-A9 processor
- IP core support, including 100G Ethernet, 150G/300G Interlaken, and PCI Express Gen3
- Built on TSMC's 20 nm process technology

Intel® Cyclone® 10

FPGA



Intel Cyclone 10 GX

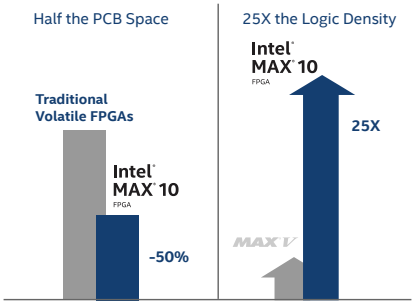
- Optimized for high-bandwidth, high-performance applications
- The industry's first low-cost FPGA with 12.5 Gbps transceiver I/O support
- High-performance 1,866 Mbps external memory interface
- 1.434 Gbps LVDS I/Os
- The industry's first low-cost FPGA with IEEE 754 compliant hard floating-point DSP blocks

Intel Cyclone 10 LP

- Optimized for cost and power-sensitive applications
- Chip-to-chip bridging
- I/O expansion
- Control applications

Intel® MAX® 10

FPGA



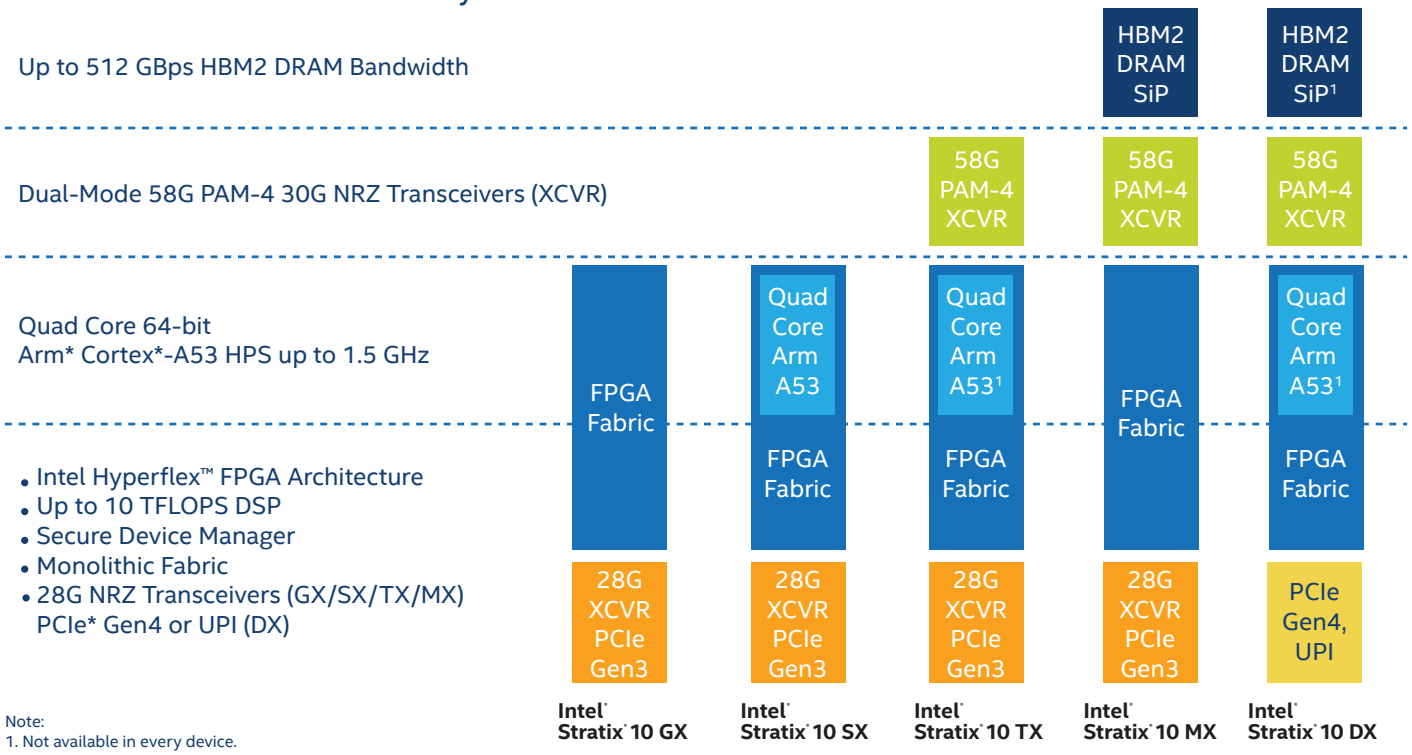
- Single-chip, dual-configuration non-volatile FPGA
- Optimal system component integration for half the PCB space of traditional volatile FPGAs
- Broad range of IP including analog-to-digital converters (ADCs), DSP, and the Nios II embedded soft processor

Intel Stratix 10 FPGA and SoC Overview

www.intel.com/stratix10

Intel FPGAs and SoCs deliver breakthrough advantages in performance, power efficiency, density, and system integration that are unmatched in the industry. Featuring the revolutionary Intel Hyperflex FPGA Architecture and built on the Intel 14 nm Tri-Gate process, Intel Stratix 10 devices deliver 2X core performance gains over previous-generation, high-performance FPGAs with up to 70% lower power†.

Intel® Stratix® 10 Device Family Variants



Note:
1. Not available in every device.

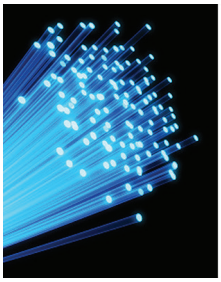
The figure above shows the core performance benchmarks achieved by early access customers using the Intel Stratix 10 Hyperflex FPGA architecture. With the 2X performance increase, customers in multiple end markets can achieve significant improvements in both throughput and area utilization, with up to 70% lower power†.

Intel Stratix 10 FPGA and SoC system integration breakthroughs include:

- Heterogeneous 3D system in package (SiP) integration
- The highest density FPGA fabric with up to 10.2 million LEs
- Up to 10 TFLOPS of IEEE 754 compliant single-precision floating-point DSP throughput
- Secure Device Manager (SDM) with the most comprehensive security capabilities
- Integrated quad-core 64 bit Arm Cortex-A53 hard processor system up to 1.5 GHz
- Complementary optimized and validated Intel Enpirion power solutions
- Dual-mode 28.9 Gbps non-return-to-zero (NRZ) and 57.8 Gbps PAM-4 transceivers
- HBM2 DRAM SiP delivering up to 512 GBps of memory bandwidth

These unprecedented capabilities make Intel Stratix 10 devices uniquely positioned to address the design challenges in next-generation, high-performance systems in virtually all end markets including wireline and wireless communications, computing, storage, military, broadcast, medical, and test and measurement.

Communications



- 400G/500G/1T optical transmission
- 200G/400G bridging and aggregation
- 982 MHz remote radio head
- Mobile backhaul
- 5G wireless communications

Computing and Storage



- Data center server acceleration
- High-performance computing (HPC)
- Oil and gas exploration
- Bioscience

Defense



- Next-generation radar
- Secure communications
- Avionics and guidance systems

Broadcast



- High-end broadcast studio
- High-end broadcast distribution
- Headend encoder or EdgeQAM or converged multiservice access platform (CMAP)

Devices: Generation 10 Device Portfolio

Intel Stratix 10 GX FPGA Features

View device ordering codes on page 50.

	PRODUCT LINE	GX 400	GX 650	GX 850	GX 1100	GX 1650	GX 2100	GX 2500	GX 2800	GX 1660	GX 2110	GX 10M
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,325,000	1,624,000	2,005,000	2,422,000	2,753,000	1,679,000	2,073,000	10,200,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	449,280	550,540	679,680	821,150	933,120	569,200	702,720	3,466,080
	ALM registers	512,640	829,440	1,139,840	1,797,120	2,202,160	2,718,720	3,284,600	3,732,480	2,276,800	2,810,880	13,864,320
	Hyper-Registers from Intel Hyperflex FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric										
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees										
	M20K memory blocks	1,537	2,489	3,477	5,461	5,851	6,501	9,963	11,721	6,162	6,847	12,950
	M20K memory size (Mb)	30	49	68	107	114	127	195	229	120	134	253
	MLAB memory size (Mb)	2	3	4	7	8	11	13	15	9	11	55
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,592	3,145	3,744	5,011	5,760	3,326	3,960	3,456
	18 x 19 multipliers	1,296	2,304	4,032	5,184	6,290	7,488	10,022	11,520	6,652	7,920	6,912
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.4	12.6	15.0	20.0	23.0	13.3	15.8	13.8
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.1	5.0	6.0	8.0	9.2	5.3	6.3	5.5
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection										–
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4								–	–	–
	Maximum user I/O pins	374	392	688	688	704	704	1160	1160	688	688	2,304
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	120	192	336	336	336	336	576	576	336	336	1152[5]
	Total full duplex transceiver count	24	24	48	48	96	96	96	96	48	48	48
	GXT full duplex transceiver count (up to 28.3 Gbps)	16	16	32	32	64	64	64	64	32	32	–
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	32	32	16	16	48
	PCI Express hard intellectual property (IP) blocks (Gen3 x16)	1	1	2	2	4	4	4	4	2	2	4[6]
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys										
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[7, 8]												
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)		374,56,120,24	392,8,192,24	–	–	–	–	–	–	–	–	
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		–	–	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	–	–	
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	1160,8,576,24	1160,8,576,24	–	–	
F4938 pin (70 mm x 74 mm, 1.0 mm pitch)												2304, 32, 1152, 48

Notes:
1. LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system only available in Stratix 10 SX SoCs.
5. 1.4 Gbps LVDS maximum rate for GX 10M.
6. PCIe Gen3 x 8 support for GX 10M.
7. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
8. All data is preliminary and subject to change without prior notice.

392,8,192,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration path.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Stratix 10 TX Features

View device ordering codes on page 50.

	PRODUCT LINE	TX 400	TX 850	TX 850	TX 1100	TX 1100	TX 1650	TX 2100	TX 2500	TX 2500	TX 2800	TX 2800
Resources	Logic elements (LEs)[1]	378,000	841,000	841,000	1,325,000	1,325,000	1,679,000	2,073,000	2,422,000	2,422,000	2,753,000	2,753,000
	Adaptive logic modules (ALMs)	128,160	284,960	284,960	449,280	449,280	569,200	702,720	821,150	821,150	933,120	933,120
	ALM registers	512,640	1,139,840	1,139,840	1,797,120	1,797,120	2,276,800	2,810,880	3,284,600	3,284,600	3,732,480	3,732,480
	Hyper-Registers from Intel Hyperflex FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric										
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees										
	eSRAM memory blocks	–	–	–	–	–	2	2	–	–	–	–
	eSRAM memory size (Mb)	–	–	–	–	–	94.5	94.5	–	–	–	–
	M20K memory blocks	1,537	3,477	3,477	5,461	5,461	6,162	6,847	9,963	9,963	11,721	11,721
	M20K memory size (Mb)	30	68	68	107	107	120	134	195	195	229	229
	MLAB memory size (Mb)	2	4	4	7	7	9	11	13	13	15	15
	Variable-precision digital signal processing (DSP) blocks	648	2,016	2,016	2,592	2,592	3,326	3,960	5,011	5,011	5,760	5,760
	18 x 19 multipliers	1,296	4,032	4,032	5,184	5,184	6,652	7,920	10,022	10,022	11,520	11,520
	Peak fixed-point performance (TMACS)[2]	2.6	8.1	8.1	10.4	10.4	13.3	15.8	20.0	20.0	23.0	23.0
	Peak floating-point performance (TFLOPS)[3]	1.0	3.2	3.2	4.1	4.1	5.3	6.3	8.0	8.0	9.2	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection										
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4										
		Yes	Yes	Yes	Yes	Yes	–	–	Yes	Yes	Yes	Yes
	Maximum user I/O pins	384	440	440	440	440	440	440	440	296	440	296
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	144	216	216	216	216	216	216	216	144	216	144
	Total full duplex transceiver count	24	48	72	48	72	96	96	96	144	96	144
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	12 PAM-4 24 NRZ	12 PAM-4 24 NRZ	24 PAM-4 48 NRZ	12 PAM-4 24 NRZ	24 PAM-4 48 NRZ	36 PAM-4 72 NRZ	36 PAM-4 72 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	0	16	16	16	16	16	16	16	16	16	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	0	8	8	8	8	8	8	8	8	8	8
	PCI Express hard intellectual property (IP) blocks (Gen3 x16)	0	1	1	1	1	1	1	1	1	1	1
	100G Ethernet MAC (no FEC) hard IP blocks	0	1	1	1	1	1	1	1	1	1	1
	100G Ethernet MAC + FEC hard IP blocks	4	4	8	4	8	12	12	12	20	12	20
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys										
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, E-Tile Transceiver Count and H-Tile Transceiver Count[5, 6]												
F1152 pin (35mm x 35mm, 1.0mm pitch)		384,0,144,24,0										
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)			440,8,216,24,24	–	440,8,216,24,24	–	–	–	–	–	–	–
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	440,8,216,48,24	–	440,8,216,48,24	440,8,216,72,24	440,8,216,72,24	440,8,216,72,24	–	440,8,216,72,24	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	296,8,144,120,24	–	296,8,144,120,24

Notes:
1. LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system present in select Intel Stratix 10 TX devices.
5. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
6. All data is preliminary and subject to change without prior notice.

296,8,144,120,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, GXE (E-Tile) transceiver count, and GXT+GX (H-Tile) transceiver count

Indicates pin migration path.

PRODUCT LINE	HARD PROCESSOR SYSTEM (HPS)
Processor	Quad-core 64 bit Arm Cortex-A53 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • Arm NEON media engine • Arm CoreSight debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4 and DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA
USB on-the-go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I²C controller	5X I²C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	4X
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs
HPS DDR Shared I/Os	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitstream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection

Notes:
1. With overdrive feature.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Stratix 10 MX Features

View device ordering codes on page 51.

	PRODUCT LINE	MX 1650	MX 1650	MX 1650	MX 2100	MX 2100	MX 2100	MX 2100
Resources	Logic elements (LEs)[1]	1,679,000	1,679,000	1,679,000	2,073,000	2,073,000	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	569,200	569,200	569,200	702,720	702,720	702,720	702,720
	ALM registers	2,276,800	2,276,800	2,276,800	2,810,880	2,810,880	2,810,880	2,810,880
	Hyper-Registers from Intel Hyperflex FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric						
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees						
	HBM2 high-bandwidth DRAM memory (GB)	8	16	8	8	8	16	8
	eSRAM memory blocks	2	2	2	2	2	2	2
	eSRAM memory size (Mb)	94.5	94.5	94.5	94.5	94.5	94.5	94.5
	M20K memory blocks	6,162	6,162	6,162	6,847	6,847	6,847	6,847
	M20K memory size (Mb)	120	120	120	134	134	134	134
	MLAB memory size (Mb)	9	9	9	11	11	11	11
	Variable-precision digital signal processing (DSP) blocks	3,326	3,326	3,326	3,960	3,960	3,960	3,960
	18 x 19 multipliers	6,652	6,652	6,652	7,920	7,920	7,920	7,920
	Peak fixed-point performance (TMACS)[2]	13.3	13.3	13.3	15.8	15.8	15.8	15.8
	Peak floating-point performance (TFLOPS)[3]	5.3	5.3	5.3	6.3	6.3	6.3	6.3
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection						
	Hard processor system[4]	–	–	–	–	–	–	–
	Maximum user I/O pins	656	656	584	640	656	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	312	312	288	312	312	312	288
	Total full duplex transceiver count	96	96	96	48	96	96	96
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	0	0	36 PAM-4 72 NRZ	0	0	0	36 PAM-4 72 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	64	64	16	32	64	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	32	32	8	16	32	32	8
	PCI Express hard intellectual property (IP) blocks (Gen3 x16)	4	4	1	2	4	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	4	4	1	2	4	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	0	12	0	0	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys						
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, E-Tile Transceiver Count and H-Tile Transceiver Count[5, 6]								
F2597 pin (52.5 mm x 52.5 mm, 1.0mm pitch)		656, 32, 312, 0, 96	656, 32, 312, 0, 96	–	640, 16, 312, 0, 48	656, 32, 312, 0, 96	656, 32, 312, 0, 96	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	584, 8, 288, 72, 24	–	–	–	584, 8, 288, 72, 24

Notes:
1. LE counts valid in comparing across Altera devices, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system not available in Intel Stratix 10 MX devices.
5. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
6. All data is preliminary and subject to change without prior notice.

656,32,312,0,96 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, E-Tile transceiver count and H-Tile transceiver count.

Indicates pin migration path.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Stratix 10 DX Features

View device ordering codes on page 51.

	PRODUCT LINE	DX 1100	DX 2100	DX 2800
Resources	Logic elements (LEs)[1]	1,325,000	2,073,000	2,753,000
	Adaptive logic modules (ALMs)	449,280	702,720	933,120
	ALM registers	1,797,120	2,810,880	3,732,480
	Hyper-Registers from Intel Hyperflex FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric		
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees		
	HBM2 High-bandwidth DRAM memory stacks	–	2	–
	HBM2 High-bandwidth DRAM memory size (GB)	–	8	–
	eSRAM memory blocks	–	2	–
	eSRAM memory size (Mb)	–	94.5	–
	M20K memory blocks	5,461	6,847	11,721
	M20K memory size (Mb)	107	134	229
	MLAB memory size (Mb)	7	11	15
	Variable-precision digital signal processing (DSP) blocks	2,592	3,960	5,760
	18 x 19 multipliers	5,184	7,920	11,520
	Peak fixed-point performance (TMACS)[2]	10.4	15.8	23.0
	Peak floating-point performance (TFLOPS)[3]	4.1	6.3	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection		
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4		
		Yes	–	–
	Maximum user I/O pins	528	612	816
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	264	306	408
	Total full duplex transceiver count - non return to zero (NRZ)	32	84	84
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	8 PAM-4, or 16 NRZ	12 PAM-4, or 24 NRZ	4 PAM-4, or 8 NRZ
	GXP transceiver count - NRZ (up to 16 Gbps)	16	60	76
	UPI/PCI Express Gen4 x16 hard intellectual property (IP) blocks (configurable for UPI or PCIe operation)	-	3	3
	PCI Express Gen4 x16 hard IP blocks (supports PCIe only)	1	-	1
	100G Ethernet media access control (MAC) + forward error correction (FEC) hard IP blocks	4	4	2
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3		
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, P-Tile Transceiver Count and E-Tile Transceiver Count				
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		528,0,264,16,16	–	–
F2597 pin (52.5 mm x 52.5 mm, 1.0 mm pitch)		–	612,0,306,60,24	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	816,0,408,76,8

Notes:
1. LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system present in select Intel Stratix 10 DX devices.
5. All data is preliminary and subject to change without prior notice.

816,0,408,76,8 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, P-Tile transceiver count, E-Tile transceiver count.

PRODUCT LINE	HARD PROCESSOR SYSTEM (HPS)
Processor	Quad-core 64 bit Arm Cortex-A53 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • Arm NEON media engine • Arm CoreSight debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4, DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA
USB on-the-go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	4X
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs
HPS DDR Shared I/Os	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitstream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection

Notes:
1. With overdrive feature.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Stratix 10 SoC Features

View device ordering codes on page 50.

	PRODUCT LINE	SX 400	SX 650	SX 850	SX 1100	SX 1650	SX 2100	SX 2500	SX 2800
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,325,000	1,624,000	2,005,000	2,422,000	2,753,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	449,280	550,540	679,680	821,150	933,120
	ALM registers	512,640	829,440	1,139,840	1,797,120	2,202,160	2,718,720	3,284,600	3,732,480
	Hyper-Registers from Intel Hyperflex FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric							
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees							
	M20K memory blocks	1,537	2,489	3,477	5,461	5,851	6,501	9,963	11,721
	M20K memory size (Mb)	30	49	68	107	114	127	195	229
	MLAB memory size (Mb)	2	3	4	7	8	11	13	15
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,592	3,145	3,744	5,011	5,760
	18 x 19 multipliers	1,296	2,304	4,032	5,184	6,290	7,488	10,022	11,520
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.4	12.6	15.0	20.0	23.0
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.1	5.0	6.0	8.0	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection							
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4							
	Maximum user I/O pins	374	392	688	688	704	704	1160	1160
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	120	192	336	336	336	336	576	576
	Total full duplex transceiver count	24	24	48	48	96	96	96	96
	GXT full duplex transceiver count (up to 28.3 Gbps)	16	16	32	32	64	64	64	64
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	32	32
	PCI Express hard intellectual property (IP) blocks (Gen3 x16)	1	1	2	2	4	4	4	4
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys							
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5, 6]									
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)		374,56,120,24	392,8,192,24	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		–	–	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	1160,8,576,24	1160,8,576,24

Notes:
1. LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system only available in Intel Stratix 10 SX SoCs.
5. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
6. All data is preliminary and subject to change without prior notice.

392,8,192,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration path.

PRODUCT LINE	HARD PROCESSOR SYSTEM (HPS)
Processor	Quad-core 64 bit Arm Cortex-A53 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • Arm NEON media engine • Arm CoreSight debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4 and DDR3 (Up to 64 bit with ECC)
Direct memory access (DMA) controller	8 channels
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA
USB on-the-go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	4X
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs
HPS DDR Shared I/O	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitsream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection

Notes:
1. With overdrive feature.

Intel FPGA Product Catalog

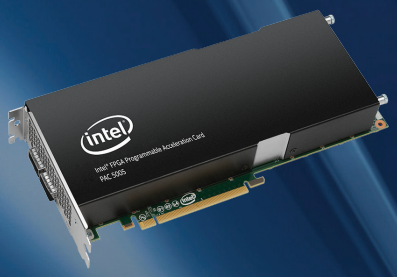
intel

Accelerator Cards That Fit Your Performance Needs

Intel® FPGA-based acceleration solutions make it possible to move, process, and store data faster and more efficiently. Intel and partner Programmable Acceleration Cards (PACs), Infrastructure Processing Units (IPUs), and SmartNICs offer hardware programmability on production-qualified cards, which enable the quick design and deployment of workloads in networking, wireless, cloud, and data center applications.

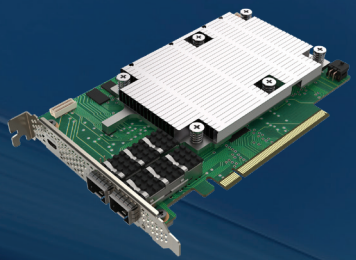
Intel FPGA PAC
N3000

Intel PAC with
Intel Arria® 10 GX FPGA



Intel FPGA PAC
D5005

Silicom FPGA
SmartNIC N5010



Inventec FPGA
IPU C5020X

For more information, please visit:
www.intel.com/fpgaaccelerationhub

Intel Arria 10 FPGA and SoC Overview

www.intel.com/arria10

Intel Arria 10 FPGAs and SoCs deliver the highest performance at 20 nm, offering a one speed-grade performance advantage over competing devices. Intel Arria 10 FPGAs and SoCs are up to 40% lower power than previous generation FPGAs and SoCs, and feature the industry's only hard floating-point DSP blocks with speeds up to 1,500 giga floating-point operations per second (GFLOPS)†. The Intel Arria 10 FPGAs and SoCs are ideal for the following end market applications.

Wireless

Applications

- Remote radio head
- Mobile backhaul
- Active antenna
- Base station
- 4G/Long Term Evolution (LTE) macro eNB
- Wideband Code Division Multiple Access (W-CDMA)

Cloud Service and Storage

Applications

- Flash cache
- Cloud
- Server
- Financial
- Bioscience
- Oil and gas
- Data center server acceleration

Broadcast

Applications

- Switcher
- Server
- Encoder/decoder
- Capture cards
- Editing
- Monitors
- Multiviewers

Devices: Generation 10 Device Portfolio

Intel Arria 10 FPGA Features

View device ordering codes on page 52.

PRODUCT LINE		GX 160	GX 220	GX 270	GX 320	GX 480	GX 570	GX 660	GX 900	GX 1150	GT 900	GT 1150
Resources	Part number reference	10AX016	10AX022	10AX027	10AX032	10AX048	10AX057	10AX066	10AX090	10AX115	10AT090	10AT115
	LEs (K)	160	220	270	320	480	570	660	900	1,150	900	1,150
	System logic elements (K)	210	288	354	419	629	747	865	1,180	1,506	1,180	1,506
	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200	339,620	427,200
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53	47	53
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7	9.2	12.7
	Hardened single-precision floating-point multipliers/ adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688	1,518/1,518	1,518/1,518	1,518/1,518	1,518/1,518
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376	3,036	3,036	3,036	3,036
	Peak fixed-point performance (GMACS)[1]	343	420	1,826	2,167	3,010	3,351	3,714	3,340	3,340	3,340	3,340
	Peak floating-point performance (GFLOPS)	140	172	747	887	1,231	1,371	1,519	1,366	1,366	1,366	1,366
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16	16	16	16	16
	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0										
	I/O standards supported	3 V I/O pins only: 3 V LVTTL, 2.5 V CMOS DDR and LVDS I/O pins: POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL All I/Os: 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-135, SSTL-125, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-135, Differential SSTL-125, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12										
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	324	270	384	384	312	312
	Maximum user I/O pins	288	288	384	384	492	696	696	768	768	624	624
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48	96	96	72	72
	Transceiver count (25.78 Gbps)	–	–	–	–	–	–	–	–	–	6	6
	PCI Express hardened IP blocks (Gen3 x8)	1	1	2	2	2	2	2	4	4	4	4
	Maximum 3 V I/O pins	48	48	48	48	48	48	48	–	–	–	–
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC										
Package Options[2] and I/O Pins[3]: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs[4], and Transceiver Count												
U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72,6	–	–	–	–	–	–	–	–	–
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	–	–	–	–	–	–	–
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12	–	–	–	–	–	–
F34	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24	504, 0, 252, 24	504, 0, 252, 24	–	–
F35	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	396, 48, 174, 36	396, 48, 174, 36	396, 48, 174, 36	–	–	–	–
KF40	F1517 pin (40 mm)	–	–	–	–	–	696, 96, 324, 36	696, 96, 324, 36	–	–	–	–
NF40	F1517 pin (40 mm)	–	–	–	–	–	588, 48, 270, 48	588, 48, 270, 48	600, 0, 300, 48	600, 0, 300, 48	–	–
RF40	F1517 pin (40 mm)	–	–	–	–	–	–	–	342, 0, 154, 66	342, 0, 154, 66	–	–
NF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	768, 0, 384, 48	768, 0, 384, 48	–	–
SF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	624, 0, 312, 72	624, 0, 312, 72	624, 0, 312, 72	624, 0, 312, 72
UF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	480, 0, 240, 96	480, 0, 240, 96	–	–

Notes:
1. Fixed-point performance assumes the use of pre-adders.
2. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
3. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
4. Each LVDS pair can be configured as either a differential input or a differential output.
5. Certain packages might not bond out all PCI Express hard IP blocks.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

192, 48, 72, 6 — Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

— Indicates pin migration.

Intel FPGA Product Catalog 24

Devices: Generation 10 Device Portfolio

Intel Arria 10 SoC Features

View device ordering codes on page 52.

PRODUCT LINE		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Resources	Part number reference	10AS016	10AS022	10AS027	10AS032	10AS048	10AS057	10AS066
	LEs (K)	160	220	270	320	480	570	660
	System Logic Elements (K)	210	288	354	419	629	747	865
	ALMs	61,510	83,730	101,620	118,730	181,790	217,080	250,540
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133
	M20K memory (Mb)	9	11	15	17	28	35	42
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7
	Hardened single-precision floating-point multipliers/ adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376
	Peak fixed-point performance (GMACS)[1]	343	420	1,826	2,167	3,010	3,351	3,714
	Peak floating-point performance (GFLOPS)	140	172	747	887	1,231	1,371	1,519
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16
	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0						
	I/O standards supported	3 V I/O pins only: 3 V LVTTL, 2.5 V CMOS DDR and LVDS I/O pins: POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL All I/Os: 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-135, SSTL-125, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-135, Differential SSTL-125, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	270	270
	Maximum user I/O pins	288	288	384	384	492	696	696
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48
	Transceiver count (25.78 Gbps)	–	–	–	–	–	–	–
	PCI Express hardened IP blocks (Gen3 x8)	1	1	2	2	2	2	2
	Maximum 3 V I/O pins	48	48	48	48	48	48	48
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC						
Package Options[2] and I/O Pins[3]: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs[4], and Transceiver Count								
U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72,6	–	–	–	–	–
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	–	–	–
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12	–	–
F34	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24
F35	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	396, 48, 174, 36	396, 48, 174, 36	396, 48, 174, 36
KF40	F1517 pin (40 mm)	–	–	–	–	–	696, 96, 324, 36	696, 96, 324, 36
NF40	F1517 pin (40 mm)	–	–	–	–	–	588, 48, 270, 48	588, 48, 270, 48

Notes:
1. Fixed-point performance assumes the use of pre-adders.
2. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
3. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
4. Each LVDS pair can be configured as either a differential input or a differential output.
5. Certain packages might not bond out all PCI Express hard IP blocks.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

192, 48, 72, 6 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration.

PRODUCT LINE	HARD PROCESSOR SYSTEM (HPS)
Processor	Dual-core Arm Cortex-A9 MPCore processor
Maximum processor frequency	1.2 -1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) • Level 2 cache (512 KB) shared • FPU single and double precision • Arm Neon media engine • Arm CoreSight debug and trace technology • Snoop control unit (SCU) • Acceleration coherency port (ACP)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4 and DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 EMAC with integrated DMA
USB OTG controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
SPI controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	7X
Software-programmable GPIOs	Maximum 54 GPIOs
Direct shared I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure boot, AES, and secure hash algorithm

Notes:
1. With overdrive feature.

Intel FPGA Product Catalog

Intel Cyclone 10 FPGA Overview

www.intel.com/cyclone10

Intel Cyclone 10 FPGAs deliver cost and power savings over previous generations of Intel Cyclone FPGAs. Intel Cyclone 10 GX FPGAs provide high bandwidth via 12.5G transceiver-based functions, 1.4 Gbps LVDS, and 1,866 Mbps DDR3 SDRAM, and feature a hard floating-point DSP block in a low-cost FPGA. Intel Cyclone 10 LP devices offer low static power, cost-optimized functions.

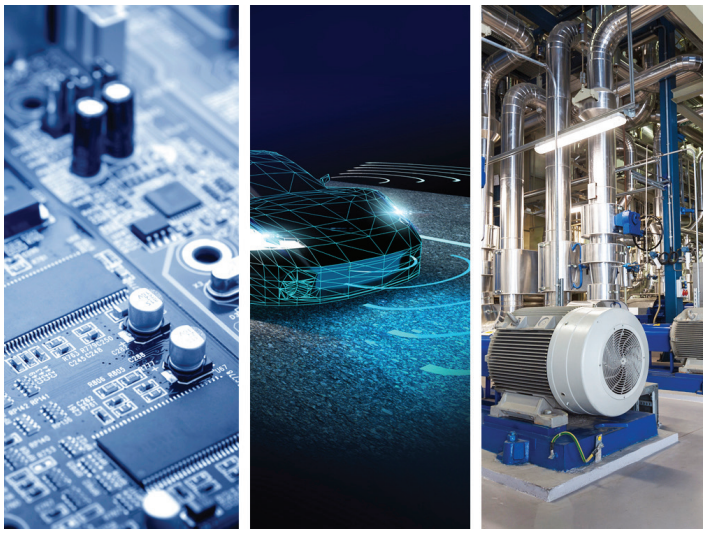
- Intel Cyclone 10 GX FPGAs are optimized for high bandwidth‡
- Intel Cyclone 10 LP FPGAs are optimized for power and cost-sensitive applications

Intel Cyclone 10 GX FPGA

- Low-cost 12.5 Gbps transceivers
- 1,866 Mbps 72 bit DDR3 SDRAM interface
- 1.4 Gbps LVDS
- The industry's first low-cost FPGA with hard floating-point blocks

GX Applications

- Embedded vision cameras
- Industrial robotics
- Machine vision
- Programmable logic controllers
- Pro-AV systems



Intel Cyclone 10 LP FPGA

- Designed for power-sensitive applications
- Simplified core power supply requirements
- High I/O count to package density ratio
- Embedded Nios II soft processor support

LP Applications

- I/O expansion
- Interfacing
- Chip-to-chip bridging
- Sensor fusion
- Industrial motor control

‡ Compared to previous generation Cyclone FPGAs, cost comparisons are based on list price. Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

Intel Cyclone 10 GX FPGA Features

View device ordering codes on page 52.

	PRODUCT LINE	10CX085	10CX105	10CX150	10CX220
Resources	Logic elements (LEs)[1]	85,000	104,000	150,000	220,000
	Adaptive logic modules (ALMs)	31,000	38,000	54,770	80,330
	ALM registers	124,000	152,000	219,080	321,320
	M20K memory blocks	291	382	475	587
	M20K memory size (Kb)	5,820	7,640	9,500	11,740
	MLAB memory size (Kb)	653	799	1,152	1,690
	Variable-precision digital signal processing (DSP) blocks	84	125	156	192
	18 x 19 multipliers	168	250	312	384
	Peak fixed-point peformance (GMACS)[2]	151	225	281	346
	Peak floating-point performance (GFLOPS)[3]	59	88	109	134
I/O and Architectural Features	Global clock networks	32	32	32	32
	Regional clocks	8	8	8	8
	Maximum user I/O pins	192	284	284	284
	Maximum LVDS pairs 1.4 Gbps (RX or TX)	72	118	118	118
	Maximum transceiver count (12.5 Gbps)	6	12	12	12
	Maximum 3V I/O pins	48	48	48	48
	PCI Express hard IP blocks (Gen2 x4)[4]	1	1	1	1
	Memory devices supported	DDR3, DDR3L, LPDDR3			
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, 3V I/O Count, LVDS Pairs, Total Transceiver count[5]					
	U484 pin (19 mm x 19 mm, 0.8 mm pitch)	188, 48, 70, 6	188, 48, 70, 6	188, 48, 70, 6	188, 48, 70, 6
	F672 pin (27 mm x 27 mm, 1.0 mm pitch)	192, 48, 72, 6	236, 48, 94, 10	236, 48, 94, 10	236, 48, 94, 10
	F780 pin (29 mm x 29 mm, 1.0 mm pitch)		284, 48, 118, 12	284, 48, 118, 12	284, 48, 118, 12

Notes:
1. LE counts valid in comparing across Intel devices, and are conservative versus competing FPGAs.
2. Fixed-point performance assumes the use of pre-adders.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Hard PCI Express IP core x2 in U484 package
5. Each LVDS pair can be configured as either a differential input or differential output.
6. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
7. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

284,48,118,12 Numbers indicate GPIO count, 3V I/O count, LVDS pairs, total transceiver count.

Indicates pin migration path.

Devices: Generation 10 Device Portfolio

Intel Cyclone 10 LP FPGA Features

View device ordering codes on page 52.

PRODUCT LINE		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
Resources	Logic elements (LEs)[1]	6,000	10,000	16,000	25,000	40,000	55,000	80,000	120,000
	M9K memory blocks	30	46	56	66	126	260	305	432
	M9K memory size (Kb)	270	414	504	594	1,134	2,340	2,745	3,888
	DSP blocks (18 x 18 multipliers)	15	23	56	66	126	156	244	288
	Phase-locked loops (PLL)	2	2	4	4	4	4	4	4
I/O and Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	Maximum user I/O pins	176	176	340	150	325	321	423	525
	Maximum LVDS channels	65	65	137	52	124	132	178	230
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, LVDS Pairs[2]									
M164 pin (8 mm x 8 mm, 0.5 mm pitch)			101,26	87, 22					
U256 pin (14 mm x 14 mm, 0.8 mm pitch)		176, 65	176, 65	162, 53	150, 52				
U484 pin (19 mm x 19 mm, 0.8 mm pitch)				340, 137		325, 124	321, 132	289, 110	
E144 pin (22 mm x 22mm, 0.5 mm pitch)		88, 22	88, 22	78, 19	76, 18				
F484 pin (23 mm x 23 mm, 1.0 mm pitch)				340, 137		325, 124	321, 132	289, 110	277, 103
F780 pin (29 mm x 29 mm, 1.0 mm pitch)								423, 178	525, 230

Notes:
1. LE counts valid in comparing across Intel devices, and are conservative versus competing FPGAs.
2. This includes both dedicated and emulated LVDS pairs
3. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit **www.intel.com/fpga**.

71, 22 Numbers indicate GPIO count, LVDS pairs.

Indicates pin migration path.

Intel FPGA Product Catalog

Intel MAX 10 FPGA Overview

www.intel.com/max10

Intel MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor, programmable logic device.

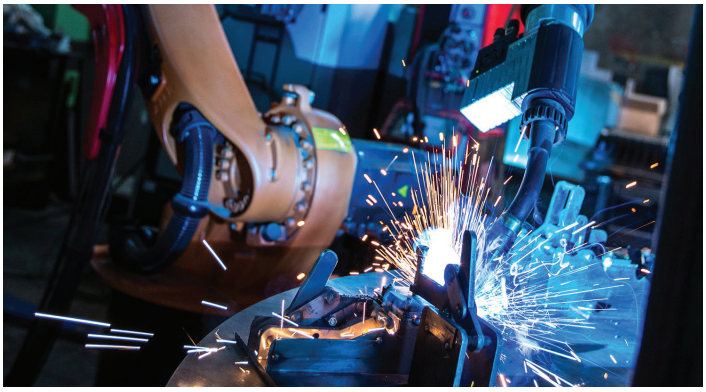
Intel MAX 10 FPGAs are built on TSMC's 55 nm flash technology, enabling instant-on configuration so you can quickly control the power-up or initialization of other components in the system. The devices also include full-featured FPGA capabilities, such as DSP, analog functionality, Nios II Gen2 embedded soft processor support, and memory controllers.

With a robust set of FPGA capabilities, Intel MAX 10 FPGAs are optimized for a wide range of high-volume, cost-sensitive applications, including:

Automotive

- Built on TSMC's 55 nm high-volume flash process tailored for the automotive industry's rigorous safety and quality requirements
- Integrated flash provides instant-on behavior for applications requiring fast boot times such as rear-view cameras in advanced driver assistance systems (ADAS) and infotainment displays
- FPGA-class signal processing acceleration for electric vehicle (EV) applications, such as motor control, battery management, and power conversion

Industrial



- Reduced footprint, increased design security and reliability, and lower system cost
- Accurate environmental condition sensing and efficient real-time controls for motor control, I/O modules, and Internet of Things (IoT) applications
- Single-chip support for multiple industrial Ethernet protocols and machine-to-machine (M2M) communication

Communications

- Analog functionality for sensing board environment allows integration of power-up sequencing and system-monitoring circuitry in a single device
- High I/O count and software-based system management using the Nios II soft processor enable board management integration in an advanced, reliable, single-chip system controller

Intel MAX 10 FPGA Features

View device ordering codes on page 53.

PRODUCT LINE		10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)		2	4	8	16	25	40	50
Block memory (Kb)		108	189	378	549	675	1,260	1,638
User flash memory[1] (KB)		12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers		16	20	24	45	55	125	144
PLLs[2]		1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration		Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD)[3]		-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)		Yes[4]	Yes[4]	Yes[4]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver								
V36 (D)[6]	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/7	–	–	–	–	–	–
V81 (D)[7]	WLCSP (4 mm, 0.4 mm pitch)	–	–	C/F, 56, 7/17	–	–	–	–
F256 (D)	FBGA (17 mm, 1.0 mm pitch)	–	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54
U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/47	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	–	–	–
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	–	–	C/A, 250, 15/83	C/A, 320, 22/116	C/A, 360, 24/136	C/A, 360, 24/136	C/A, 360, 24/136
F672 (D)	FBGA (27 mm, 1.0 mm pitch)	–	–	–	–	–	C/A, 500, 30/192	C/A, 500, 30/192
E144 (S)[6]	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/28	C/A, 101, 10/28
M153 (S)	MBGA (8 mm, 0.5 mm pitch)[8]	C, 112, 9/29	C/A, 112, 9/29	C/A, 112, 9/29	–	–	–	–
U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	–	–	–
U324 (S)	UBGA (15 mm, 0.8 mm pitch)	C, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81			

Notes:
1. Additional user flash may be available, depending on configuration options.
2. The number of PLLs available is dependent on the package option.
3. Availability of the ADC or TSD varies by package type. Smaller pin-count packages do not have access to the ADC hard IP.
4. SRAM only.
5. SRAM, DDR3 SDRAM, DDR2 SDRAM, or LPDDR2.
6. "D" = Dual power supply (1.2 V/2.5 V), "S" = Single power supply (3.3 V or 3.0 V).
7. V81 package does not support analog feature set. 10M08 V81 F devices support dual image with RSU.
8. "Easy PCB" utilizes 0.8 mm PCB design rules.
9. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

C, 27, 3/7 — Indicates feature set options, GPIO count, and LVDS transmitter or receiver count. Feature set options: C = Compact (single image), F = Flash (dual image with RSU), A = Analog (analog features block). Each has added premiums.

Indicates pin migration.

Intel eASIC Devices Overview

www.intel.com/easic

Intel eASIC devices are structured ASICs, an intermediary technology between FPGAs and standard-cell ASICs, that provide lower unit cost and lower power compared to FPGAs. These devices provide faster time to market and lower non-recurring engineering cost compared to standard-cell ASICs. The new Intel eASIC N5X devices, previously code-named Diamond Mesa, include a hard processor system and secure device managers that are compatible with Intel FPGAs to extend Intel's logic portfolio offerings.

Intel eASIC N5X Devices

- 16 nm process
- Up to 80M equivalent ASIC gates
- 250 Mb of true dual port memory
- 32.44 Gbps high-speed transceivers
- Quad-core Arm Cortex-A53 hard processor system

Intel eASIC N3XS Devices

- 28 nm process
- Up to 52 million equivalent ASIC gates
- 124 Mb of true dual port memory
- 28 Gbps high-speed transceivers

Intel eASIC N3X Devices

- 28 nm
- Up to 5 million equivalent logic gates
- Up to 15.049 Kb of true dual port memory
- Up to 18 12.5 Gbps high-speed transceivers

Intel eASIC N5X Device Features

PRODUCT LINE	N5X007	N5X015	N5X024	N5X047	N5X088
eCells (M)[1]	0.70	1.47	2.38	4.65	8.83
Equivalent ASIC gates (M)	7	1.5	2.4	4.7	8.8
M10K Memory	1752	3,684	6,004	11,780	22,372
M10K Memory (Mb)	17.94	37.72	61.48	120.63	229.09
128b register file	12,488	26,180	42,560	82,992	157,640
128b register file (Mb)	1.6	3.35	5.45	10.62	20.18
Secure device manager	Secure data manager AES-256/SHA-256 bitstream encryption/authentication, ECDSA 256/384 boot code authentication, side channel attack protection; three independent user root keys— vendor authenticated boot (VAB), secured data object storage (SDOS), time-and-priority-based key revocation				
Hard Processor System	Quad-core 64 bit Arm Cortex-A53 up to 1.5 GHz with 32 KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers for DDR4/LPDDR4/LPDDR4x, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4				
SoC I/O EMIF / Pin Mux / Dedicated	140 / 48 / 24	140 / 48 / 24	140 / 48 / 24	140 / 48 / 24	140 / 48 / 24
Maximum GPIO	416	560	682	682	1114
Transceiver 32	16	24	32	64	80
Package Examples – Packages Can be Customized Per Application Requirements					
FC676, FC1085 (27x27 mm)	Yes	–	–	–	–
FC780, FC1221 (29x29 mm)	Yes	Yes	–	–	–
FC896, FC1440 (31x31 mm)	Yes	Yes	Yes	–	–
FC1152 (35x35 mm)	Yes	Yes	Yes	–	–
FC1517 (40x40 mm)	–	Yes	Yes	Yes	Yes
FC1760 (42.5x42.5 mm)	–	–	Yes	Yes	Yes
FC1932 (45x45 mm)	–	–	–	–	Yes
FC2205 (47.5x47.5 mm)	–	–	–	–	Yes
FC2397 (50x50 mm)	–	–	–	–	Yes

Notes:
1. eCell can be configured as logic, adders, and/or registers and are roughly equivalent to a 4-input logic element capacity.

Intel eASIC N3XS Device Features

PRODUCT LINE	N3XSTe3	N3XSTe5	N3XSTe9	N3XSTe11	N3XSTe15
Equivalent eCells (K)	410	1,040	1,558	3,863	5,262
Equivalent ASIC gates (M)	4	10	16	39	52
LCells	556,800	1,412,880	2,115,840	5,247,840	7,147,920
ACells	172,800	438,480	656,640	1,628,640	2,218,320
eDFFs	230,400	584,640	875,520	2,171,520	2,957,760
bRAM18K blocks (18 Kbit size)	456	1,176	1,776	4,446	6,084
bRAM18K (Kbits)	8,405	21,676	32,735	81,949	112,140
Regfile2K blocks (2 Kbit size)	450	1,161	1,751	4,431	5,977
Regfile2K (Kbits)	922	2,378	3,607	9,075	12,241
Total Memory (Kbits)	9,327	24,054	36,342	91,023	124,381
PLLs	6	12	14	20	24
MGIO 16 (16.3 Gbps)	8	12	32	24	32
MGIO 28 (28 Gbps)	0	0	0	24	32
Legacy I/O	62	62	62	62	62
High-Speed I/O	232	372	522	738	882
Package Examples – Packages Can be Customized Per Application Requirements					
CS484	Yes	–	–	–	–
FC484	Yes	Yes	–	–	–
FC529	–	Yes	Yes	–	–
FC572	Yes	Yes	Yes	–	–
FC676	Yes	Yes	Yes	Yes	–
FC780	–	Yes	Yes	Yes	Yes
FC1152	–	–	Yes	Yes	Yes
FC1517	–	–	–	–	Yes

Intel eASIC N3X Device Features

PRODUCT LINE	N3XT500
eCells	503,424
eDFFs	346,104
Full Adders	503,424
bRAM Kbits	15,409
bRAM blocks	1,672
PLL	16
DLL	42
MGIO-T	18 (12.5 Gbps)
Package Examples – Packages Can be Customized Per Application Requirements	
CS160 (7x11 mm)	4/30
FC484 (23 mm)	8/316
FC672 (27 mm)	8/316
FC780 (29 mm)	14/336
FC896 (31 mm)	18/336
FC1152 (35 mm)	18/392

Devices: 28 nm Device Portfolio

Stratix V FPGA Features

View device ordering codes on page 53.

PRODUCT LINE		STRATIX V GS FPGAs[1]					STRATIX V GX FPGAs[1]										STRATIX V E FPGAs[1]	
		5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6	5SGXB9	5SGXBB	5SEE9	5SEEB
Resources	LEs (K)	236	360	457	583	695	340	420	490	622	840	952	490	597	840	952	840	952
	ALMs	89,000	135,840	172,600	220,000	262,400	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400	317,000	359,200	317,000	359,200
	Registers	356,000	543,360	690,400	880,000	1,049,600	513,200	634,000	740,000	938,880	1,268,000	1,436,800	740,000	901,600	1,268,000	1,436,800	1,268,000	1,436,800
	M20K memory blocks	688	957	2,014	2,320	2,567	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660	2,640	2,640	2,640	2,640
	M20K memory (Mb)	13	19	39	45	50	19	37	45	50	52	52	41	52	52	52	52	52
	MLAB memory (Mb)	2.72	4.15	5.27	6.71	8.01	3.92	4.84	5.65	7.16	9.67	10.96	5.65	6.88	9.67	10.96	9.67	10.96
	Variable-precision DSP blocks	600	1,044	1,590	1,775	1,963	256	256	256	256	352	352	399	399	352	352	352	352
	18 x 18 multipliers	1,200	2,088	3,180	3,550	3,926	512	512	512	512	704	704	798	798	704	704	704	704
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	Regional clocks	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]																
	I/O standards supported	LVTTL, LVCMOS, PCI· PCI-X, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																
	Maximum LVDS pairs, 1.4 Gbps (receive/transmit)	108/108	174/174	174/174	210/210	210/210	174/174	174/174	210/210	210/210	210/210	210/210	150/150	150/150	150/150	150/150	210/210	210/210
	Transceiver count (14.1 Gbps)	24	36	36	48	48	36	36	48	48	48	48	66	66	66	66	–	–
	Transceiver count (28.05 Gbps)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	PCI Express hardened IP blocks (Gen3 x8)	1	1	1	4	4	2	2	4	4	4	4	4	4	4	4	–	–
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3																
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, Full-Duplex LVDS, and Transceiver Count																		
F780 pin (29 mm, 1.0 mm pitch)		360, 90, 12[3]	360, 90, 12[3]	–	–	–	360, 90, 12[3]	–	–	–	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		432, 108, 24	432, 108, 24	552, 138, 24	–	–	432, 108, 24	552, 138, 24	552, 138, 24	552, 138, 24	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		–	–	–	–	–	432, 108, 36	432, 108, 36	432, 108, 36	432, 108, 36	–	–	–	–	–	–	–	–
F1517 pin (40 mm, 1.0 mm pitch)		–	696, 174, 36	696, 174, 36	696, 174 ,36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36[4]	696, 174, 36[4]	432, 108, 66	432, 108, 66	–	–	696, 174, 0[4]	696, 174, 0[4]
F1517 pin (40 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	600,150,48	600,150,48	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	–	–	–	600, 150, 66	600, 150, 66	600, 150, 66[4]	600, 150, 66[4]	–	–
F1932 pin (45 mm, 1.0 mm pitch)		–	–	–	840,210,48	840,210,48	–	–	840, 210, 48	840, 210, 48	840, 210, 48	840, 210, 48	–	–	–	–	840, 210, 0	840, 210, 0

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. 3.3 V compliant, requires a 3.0 V power supply.
3. Hybrid package (flip chip) FBGA: 33 x 33 (mm) 1.0-mm pitch.
4. Hybrid package (flip chip) FBGA: 45 x 45 (mm) 1.0-mm pitch.
5. 360, 90, 12 Numbers indicate GPIO count, LVDS count, and transceiver count.
6. Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.
7. Stratix series devices are offered for commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered for industrial temperatures (0 ˚C to 100 ˚C).

Intel FPGA Product Catalog

Devices: 28 nm Device Portfolio

Arria V FPGA and SoC Features

View device ordering codes on page 54.

PRODUCT LINE		ARRIA V GX FPGAs[1]								ARRIA V GT FPGAs[1]				ARRIA V GZ FPGAs[1]				ARRIA V SX SoCs[1]		ARRIA V ST SoCs[1]	
		5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7	5AGTC3	5AGTC7	5AGTD3	5AGTD7	5AGZE1	5AGZE3	5AGZE5	5AGZE7	5ASXB3	5ASXB5	5ASTD3	5ASTD5
Resources	LEs (K)	75	156	190	242	300	362	420	504	156	242	362	504	220	360	400	450	350	462	350	462
	ALMs	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240	58,900	91,680	136,880	190,240	83,020	135,840	150,960	169,800	132,075	174,340	132,075	174,340
	Registers	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960	235,600	366,720	547,520	760,960	332,080	543,360	603,840	679,200	528,300	697,360	528,300	697,360
	M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414	1,051	1,366	1,726	2,414	–	–	–	–	1,729	2,282	1,729	2,282
	M20K memory blocks	–	–	–	–	–	–	–	–	–	–	–	–	585	957	1,440	1,700	–	–	–	–
	M10K memory (Kb)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140	10,510	13,660	17,260	24,140	–	–	–	–	17,290	22,820	17,290	22,820
	M20K memory (Kb)	–	–	–	–	–	–	–	–	–	–	–	–	11,700	19,140	28,800	34,000	–	–	–	–
	MLAB memory (Kb)	463	961	1,173	1,448	1,852	2,098	2,532	2,906	961	1,448	2,098	2,906	2,594	4,245	4,718	5,306	2,014	2,658	2,014	2,658
	Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,156	396	800	1,045	1,156	800	1,044	1,092	1,139	809	1,090	809	1,090
	18 x 18 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,312	792	1,600	2,090	2,312	1,600	2,088	2,184	2,278	1,618	2,180	1,618	2,180
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (Arm Cortex-A9)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (GHz)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1.05[2]	1.05[2]	1.05[2]	1.05[2]
	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[3] (FPGA)	10	10	12	12	12	12	16	16	10	12	12	16	20	20	24	24	14	14	14	14
	PLLs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	3	3	3
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[4]																			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																			
	Maximum LVDS pairs (receiver/transmitter)	80/67	80/67	136/120	136/120	176/160	176/160	176/160	176/160	80/70	136/120	176/160	176/160	108/99	108/99	168/166	168/166	136/120	136/120	136/120	136/120
	Transceiver count (6.5536 Gbps)	9	9	24	24	24	24	36	36	3	6	6	6	–	–	–	–	30	30	30	30
	Transceiver count (10.3125 Gbps)[5]	–	–	–	–	–	–	–	–	4	12	12	20	–	–	–	–	–	–	16	16
	Transceiver count (12.5 Gbps)	–	–	–	–	–	–	–	–	–	–	–	–	24	24	36	36	–	–	–	–
	PCI Express hardened IP blocks (Gen2 x4)	1	1	2	2	2	2	2	2	1	2	2	2	–	–	–	–	2	2	2	2
	PCI Express hardened IP blocks (Gen2 x8, Gen3)	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1	–	–	–	–
	GPIOs (FPGA)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	540	540	540	540
	GPIOs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	208	208	208	208
	Hard memory controllers[6] (FPGA)	2	2	4	4	4	4	4	4	2	4	4	4	–	–	–	–	3	3	3	3
	Hard memory controllers (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1
	Memory devices supported	DDR3, DDR2, DDR II+[7], QDR II, QDR II+, RLDRAM II, RLDRAM 3[8], LPDDR[7], LPDDR2[7]																			
Package Options and I/O Pins: GPIO Count, and Transceiver Count																					
F672 pin (27 mm, 1.0 mm pitch)		336 9,0	336 9,0	336 9,0	336 9,0	–	–	–	–	336 3,4	–	–	–	–	–	–	–	–	–	–	–
H780 pin (29 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	–	–	–	–	342 12	342 12	–	–	–	–		–
F896 pin (31 mm, 1.0 mm pitch)		416 9,0	416 9,0	384 18,0	384 18,0	384 18,0	384 18,0	–	–	416 3,4	384 6,8	384 6,8	–	–	–	–	–	250, 208 12+0	250, 208 12+0	250, 208 12+6	250, 208 12+6
F896 pin (31 mm, 1.0 mm pitch)		320 9,0	320 9,0	320 9,0	320 9,0	320 9,0	–	–	–	320 3,4	320 3,4	320 3,4	–	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		–	–	544 24,0	544 24,0	544 24,0	544 24,0	544 24,0	544 24,0	–	544 6,12	544 6,12	544 6,12	414 24	414 24	534 24	534 24	385, 208 18+0	385, 208 18+0	385, 208 18+8	385, 208 18+8
F1517 pin (40 mm, 1.0 mm pitch)		–	–	–	–	704 24,0	704 24,0	704 36,0	704 36,0	–	–	704 6,12	704 6,20	–	–	674 36	674 36	540, 208 30+0	540, 208 30+0	540, 208 30+16	540, 208 30+16

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. 1.15 V operation.
3. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
4. For Arria V GZ devices, the I/O voltage of 3.3 V compliant, requires a 3.0 V power supply.
5. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels.
6. With 16 and 32 bit ECC support.
7. These memory interfaces are not available as Intel FPGA IP.
8. This memory interface is only available for Arria V GZ devices.

336 / 9,0 — For Arria V GX and GT devices, values on top indicate available user I/O pins and values at the bottom indicate the 6.5536 Gbps and 10.3125 Gbps transceiver count. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels. For Arria V GZ devices, values on top indicate available user I/O pins and values at the bottom indicate the 12.5 Gbps transceiver count.

250, 208 / 12+0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 6.5536 Gbps plus 10.3125 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

Pin migration is only possible if you use up to 320 I/O pins, up to nine 6.5536 Gbps transceiver count (for Arria V GX devices), and up to four 10.3125 Gbps transceiver count (for Arria V GT devices).

Devices: 28 nm Device Portfolio

Cyclone V FPGA Features

View device ordering codes on page 55.

	PRODUCT LINE	CYCLONE V E FPGAS[1]					CYCLONE V GX FPGAS[1]					CYCLONE V GT FPGAS[1]		
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
Resources	LEs (K)	25	49	77	149.5	301	35.5	50	77	149.5	301	77	149.5	301
	ALMs	9,434	18,480	29,080	56,480	113,560	13,460	18,868	29,080	56,480	113,560	29,080	56,480	113,560
	Registers	37,736	73,920	116,320	225,920	454,240	53,840	75,472	116,320	225,920	454,240	116,320	225,920	454,240
	M10K memory blocks	176	308	446	686	1,220	135	250	446	686	1,220	446	686	1,220
	M10K memory (Kb)	1,760	3,080	4,460	6,860	12,200	1,350	2,500	4,460	6,860	12,200	4,460	6,860	12,200
	MLAB memory (Kb)	196	303	424	836	1,717	291	295	424	836	1,717	424	836	1,717
	Variable-precision DSP blocks	25	66	150	156	342	57	70	150	156	342	150	156	342
	18 x 18 multipliers	50	132	300	312	684	114	140	300	312	684	300	312	684
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	4	4	6	7	8	4	6	6	7	8	6	7	8
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3												
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2					LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS					
	Maximum LVDS pairs (receiver/transmitter)	56/56	56/56	60/60	120/120	120/120	52/52	84/84	84/84	120/120	140/140	84/84	120/120	140/140
	Transceiver count (3.125 Gbps)	–	–	–	–	–	3	6	6	9	12	–	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	–	–	6[4]	9[4]	12[4]
	PCI Express hardened IP blocks (Gen1)[5]	–	–	–	–	–	1	2	2	2	2	–	–	–
	PCI Express hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	–	–	2	2	2
	Hard memory controllers[6] (FPGA)	1	1	2	2	2	1	2	2	2	2	2	2	2
	Memory devices supported	DDR3, DDR2, LPDDR2												

Package Options and I/O Pins: GPIO Count, and Transceiver Count

M301 pin (11 mm, 0.5 mm pitch)							129 4	129 4				129 4		
M383 pin (13 mm, 0.5 mm pitch)	223 223		175				175 6	175 6				175 6		
M484 pin (15 mm, 0.5 mm pitch)				240					240 3				240 3	
U324 pin (15 mm, 0.8 mm pitch)	176 176					144 3								
U484 pin (19 mm, 0.8 mm pitch)	224 224	224	224	240	240	208 3	224 6	224 6	240 6	240 5		224 6	240 6	240 5
F256 pin (17 mm, 1.0 mm pitch)	128 128													
F484 pin (23 mm, 1.0 mm pitch)	224 224	240	240	240	224	208 3	240 6	240 6	240 6	224 6		240 6	240 6	224 6
F672 pin (27 mm, 1.0 mm pitch)				336	336		336 6	336 6	336 9	336 9		336 6	336 9	336 9
F896 pin (31 mm, 1.0 mm pitch)				480	480				480 9	480 12			480 9	480 12
F1152 pin (35 mm, 1.0 mm pitch)										560 12				560 12

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. Transceiver counts shown are for ≤ 5 Gbps. The 6 Gbps channel count support depends on package and channel usage. Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
5. Only one PCIe hard IP block supported in M301, M484, and U324 packages.
6. Includes 16 and 32 bit error correction code ECC support.

129
4 Values on top indicate available user I/O pins; values at the bottom indicate the 3.125 Gbps, 5 Gbps, or 6.144 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For FPGAs: Pin migration is only possible if you use only up to 175 GPIOs.

Devices: 28 nm Device Portfolio

Cyclone V SoC Features

View device ordering codes on page 55.

	PRODUCT LINE	CYCLONE V SE SoCs[1]				CYCLONE V SX SoCs[1]				CYCLONE V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K)	25	40	85	110	25	40	85	110	85	110
	ALMs	9,434	15,094	32,075	41,509	9,434	15,094	32,075	41,509	32,075	41,509
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (Arm Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual	Dual	Dual	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (MHz)	925	925	925	925	925	925	925	925	925	925
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	5	5	6	6	5	5	6	6	6	6
	PLLs (HPS)	3	3	3	3	3	3	3	3	3	3
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS									
	Maximum LVDS pairs (receiver/transmitter)	37/32	37/32	72/72	72/72	37/32	37/32	72/72	72/72	72/72	72/72
	Transceiver count (3.125 Gbps)	–	–	–	–	6	6	9	9	–	–
	Transceiver count (6.144 Gbps)	–	–	–	–	–	–	–	–	9[3]	9[3]
	PCI Express hardened IP blocks (Gen1)	–	–	–	–	2	2	2[4]	2[4]	–	–
	PCI Express hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	2	2
	GPIOs (FPGA)	145	145	288	288	145	145	288	288	288	288
	GPIOs (HPS)	181	181	181	181	181	181	181	181	181	181
	Hard memory controllers[5] (FPGA)	1	1	1	1	1	1	1	1	1	1
	Hard memory controllers[5] (HPS)	1	1	1	1	1	1	1	1	1	1
	Memory devices supported	DDR3, DDR2, LPDDR2									

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, and Transceiver Count

U484 pin (19 mm, 0.8 mm pitch)	66, 151 0	66, 151 0	66, 151 0	66, 151 0						
U672 pin (23 mm, 0.8 mm pitch)	145, 181 0	145, 181 0	145, 181 0	145, 181 0	145, 181 6	145, 181 6	145, 181 6	145, 181 6		
F896 pin (31 mm, 1.0 mm pitch			288, 181 0	288, 181 0			288, 181 9	288, 181 9	288, 181 9	288, 181 9

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Transceiver counts shown are for ≤ 5 Gbps. The 6 Gbps channel count support depends on package and channel usage. Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
4. One PCI Express hard IP block in U672 package.
5. With 16 and 32 bit ECC support.

66, 151 / 0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For SoCs: Pin migration is only possible if you use only up to 138 GPIOs.

Devices: 60 nm Device Portfolio

Cyclone IV FPGA Features

View device ordering codes on page 56.

	PRODUCT LINE	CYCLONE IV GX FPGAS[1]							CYCLONE IV E FPGAS[1]								
		EP4CGX15	EP4CGX22	EP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Resources	LEs (K)	14	21	29	50	74	109	150	6	10	15	22	29	40	56	75	114
	M9K memory blocks	60	84	120	278	462	666	720	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480	270	414	504	594	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	0	40	80	140	198	280	360	15	23	56	66	66	116	154	200	266
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	20	20	20	30	30	30	30	10	10	20	20	20	20	20	20	20
	PLLs	3	4	4	8	8	8	8	2	2	4	4	4	4	4	4	4
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3															
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12															
	Emulated LVDS channels	9	40	40	73	73	139	139	66	66	137	52	224	224	160	178	230
	Maximum LVDS pairs, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59	–	–	–	–	–	–	–	–	–
	Transceiver count[2] (2.5 Gbps/3.124 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4[3]	0, 8	0, 8	0, 8	0, 8	–	–	–	–	–	–	–	–	–
	PCI Express hardened IP blocks (Base specification, Rev 1.1, 2.0, and so on)	1	1	1	1	1	1	1	–	–	–	–	–	–	–	–	–
	Memory devices supported	DDR2, DDR, SDR															
	Package Options and I/O Pins: General-Purpose I/O (GPIO) Count and Transceiver Count																
	E144 pin[4] (22 mm, 0.5 mm pitch)	–	–	–	–	–	–	–	91	91	81	79	–	–	–	–	–
	M164 pin (8 mm, 0.5 mm pitch)	–	–	–	–	–	–	–	–	–	90	–	–	–	–	–	–
	M256 pin (9 mm, 0.5 mm pitch)	–	–	–	–	–	–	–	–	–	166	–	–	–	–	–	–
	U256 pin (14 mm, 0.8 mm pitch)	–	–	–	–	–	–	–	179	179	165	153	–	–	–	–	–
	U484 pin (19 mm, 0.8 mm pitch)	–	–	–	–	–	–	–	–	–	–	–	328	328	324	292	–
	F169 pin (14 mm, 1.0 mm pitch)	72 2	72 2	72 2	–	–	–	–	–	–	–	–	–	–	–	–	–
	F256 pin (17 mm, 1.0 mm pitch)	–	–	–	–	–	–	–	179	179	165	153	–	–	–	–	–
	F324 pin (19 mm, 1.0 mm pitch)	–	150 4	150 4	–	–	–	–	–	–	–	–	193	193	–	–	–
	F484 pin (23 mm, 1.0 mm pitch)			290 4	290 4	290 4	270 4	270 4	–	–	343	–	328	328	324	292	280
	F672 pin (27 mm, 1.0 mm pitch)	–	–	–	310 8	310 8	393 8	393 8	–	–	–	–	–	–	–	–	–
	F780 pin (29 mm, 1.0 mm pitch)	–	–	–	–	–	–	–	–	–	–	–	532	532	374	426	528
	F896 pin (31 mm, 1.0 mm pitch)	–	–	–	–	–	475 8	475 8	–	–	–	–	–	–	–	–	–

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. Transceiver performance varies by product line and package offering.
3. EP4CGX30 supports 3.125 Gbps transceivers only in F484 package option.
4. Enhanced thin quad flat pack (EQFP).

72 2 Values on top indicate available user I/O pins; values at the bottom indicate the 2.5 Gbps or 3.125 Gbps transceiver count.

Pin migration (same Vcc, GND, ISP, and input pins). User I/Os may be less than labelled for pin migration.

MAX CPLD Series

MAX V CPLD Features

View device ordering codes on page 57.

	PRODUCT LINE	MAX V CPLDS[1]						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Resources	LEs	40	80	160	240	570	1,270	2,210
	Equivalent macrocells[2]	32	64	128	192	440	980	1,700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8	8	8	8	8	8	8
	Logic convertible to memory[3]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Clocks, Maximum I/O Pins, and Architectural Features	Internal oscillator	✓	✓	✓	✓	✓	✓	✓
	Fast power-on reset	✓	✓	✓	✓	✓	✓	✓
	Boundary-scan JTAG	✓	✓	✓	✓	✓	✓	✓
	JTAG ISP	✓	✓	✓	✓	✓	✓	✓
	Fast input registers	✓	✓	✓	✓	✓	✓	✓
	Programmable register power-up	✓	✓	✓	✓	✓	✓	✓
	JTAG translator	✓	✓	✓	✓	✓	✓	✓
	Real-time ISP	✓	✓	✓	✓	✓	✓	✓
	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	54	79	114	159	271	271
	LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓
	LVDS outputs	✓	✓	✓	✓	✓	✓	✓
	32 bit, 66 MHz PCI compliant	–	–	–	–	–	✓[4]	✓[4]
	Schmitt triggers	✓	✓	✓	✓	✓	✓	✓
	Programmable slew rate	✓	✓	✓	✓	✓	✓	✓
	Programmable pull-up resistors	✓	✓	✓	✓	✓	✓	✓
	Programmable GND pins	✓	✓	✓	✓	✓	✓	✓
	Open-drain outputs	✓	✓	✓	✓	✓	✓	✓
	Bus hold	✓	✓	✓	✓	✓	✓	✓
Package Options and I/O Pins[5]								
E64 pin (9 mm, 0.4 mm pitch)		54	54	54	–	–	–	–
T100 pin[6] (16 mm, 0.5 mm pitch)		–	79	79	79	74	–	–
T144 pin[6] (22 mm, 0.5 mm pitch)		–	–	–	114	114	114	–
M64 pin (4.5 mm, 0.5 mm pitch)		30	30	–	–	–	–	–
M68 pin (5 mm, 0.5 mm pitch)		–	52	52	52	–	–	–
M100 pin (6 mm, 0.5 mm pitch)		–	–	79	79	74	–	–
M144 pin (7 mm, 0.5 mm pitch)		–	–	–	–	–	–	–
M256 pin (11 mm, 0.5 mm pitch)		–	–	–	–	–	–	–
U256 pin (14 mm, 0.8 mm pitch)		–	–	–	–	–	–	–
F100 pin (11 mm, 1.0 mm pitch)		–	–	–	–	–	–	–
F256 pin (17 mm, 1.0 mm pitch)		–	–	–	–	159	211	204
F324 pin (19 mm, 1.0 mm pitch)		–	–	–	–	–	271	271

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. Typical equivalent macrocells.
3. Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.
4. An external resistor must be used for 5.0 V tolerance.
5. For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Intel's online selector guide.
6. Thin quad flat pack (TQFP).

54 Number indicates available user I/O pins.

Pin migration (same Vcc, GND, ISP, and input pins). User I/Os may be less than labelled for pin migration.

Configuration Devices

View device ordering codes on page 57.

www.intel.com/fpgaconfiguration

The following information is an overview of our configuration devices. To determine the right configuration device for your FPGA, refer to the device datasheets and pin-out files available on the Documentation: Configuration Devices page.

Intel FPGA serial configuration devices store the configuration file for our SRAM-based FPGAs. We designed our serial configuration devices to minimize board space while providing a dedicated FPGA configuration solution. Serial configuration devices are recommended for new designs. For information on additional configuration devices supporting older products, refer to the device datasheets and pin-out files, available on the Documentation: Configuration Devices page.

EPCQ-A SERIAL CONFIGURATION DEVICES FOR 28 NM AND PRIOR FPGAs (3.0–3.3 V)

	SOIC	
	8 pin 4.9 x 6.0 (mm)	16 pin 10.3 x 10.3 (mm)
EPCQ4A	4	
EPCQ16A	16	
EPCQ32A	32	
EPCQ64A		64
EPCQ128A		128

Notes:

512 Number indicates memory size in megabits (Mb).

Vertical migration (same V_{cc}, GND, ISP, and input pins).

Transceiver Technology

www.intel.com/transceiverprotocols

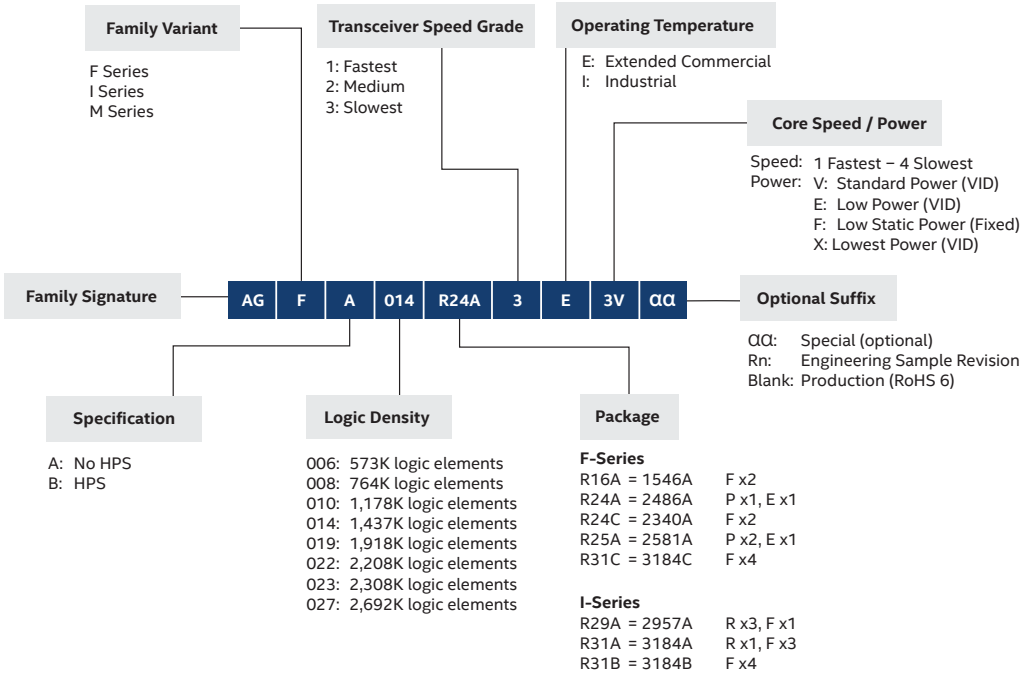
Intel FPGAs with integrated transceivers offer a range of data rates to suit all applications from 600 Mbps to 30 Gbps non-return-to-zero (NRZ) and up to 58 Gbps PAM4 Gbps.

For a list of supported transceiver protocols, visit **www.intel.com/transceiverprotocols**.

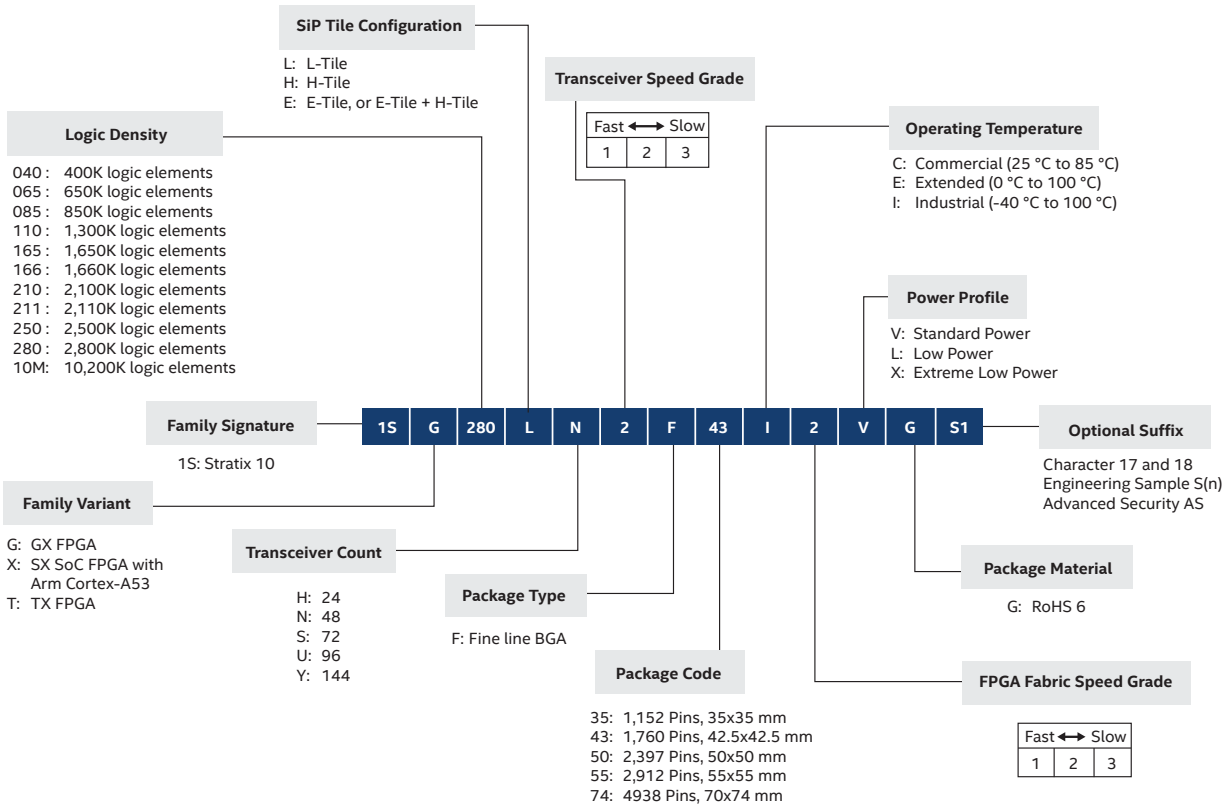
To learn more about Intel transceivers, visit the **Transceivers** page.

Ordering Codes

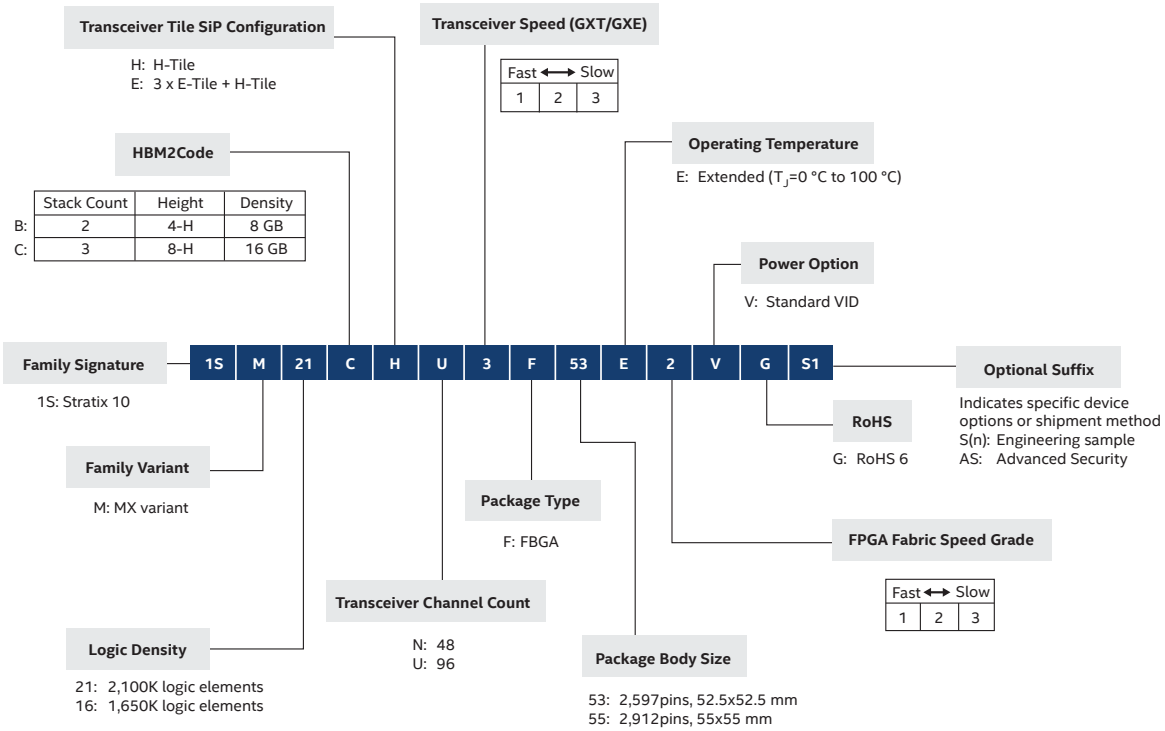
Ordering Information for Intel Agilex (F and I) Series



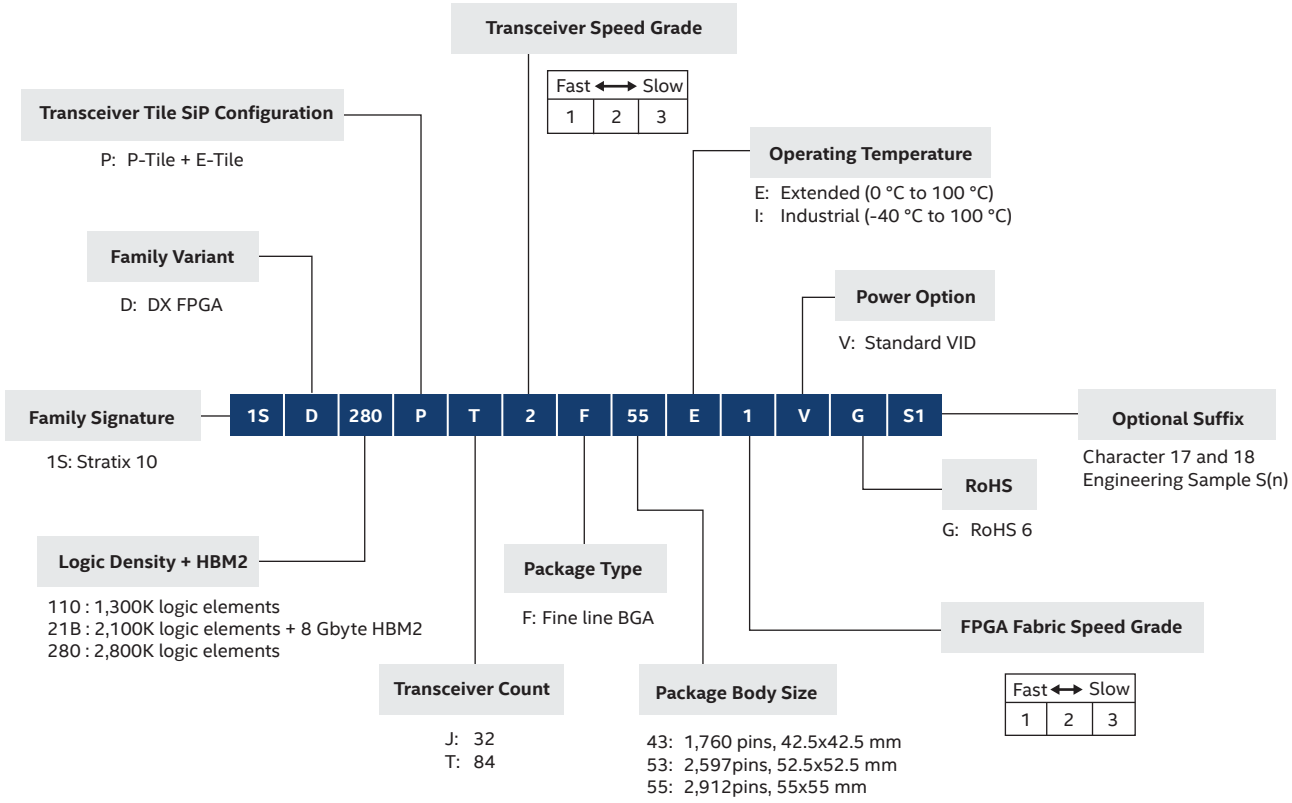
Ordering Information for Intel Stratix 10 (GX, SX, TX) Devices



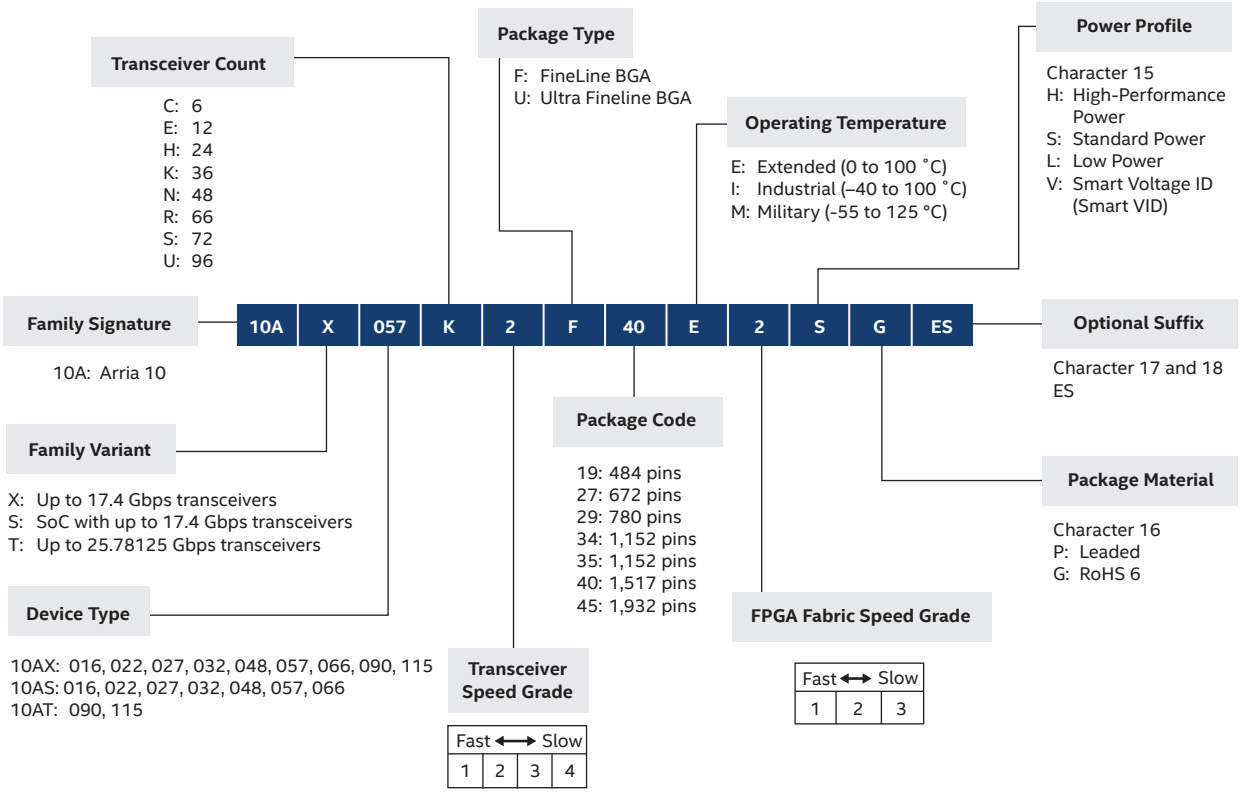
Ordering Information for Intel Stratix 10 (MX) Devices



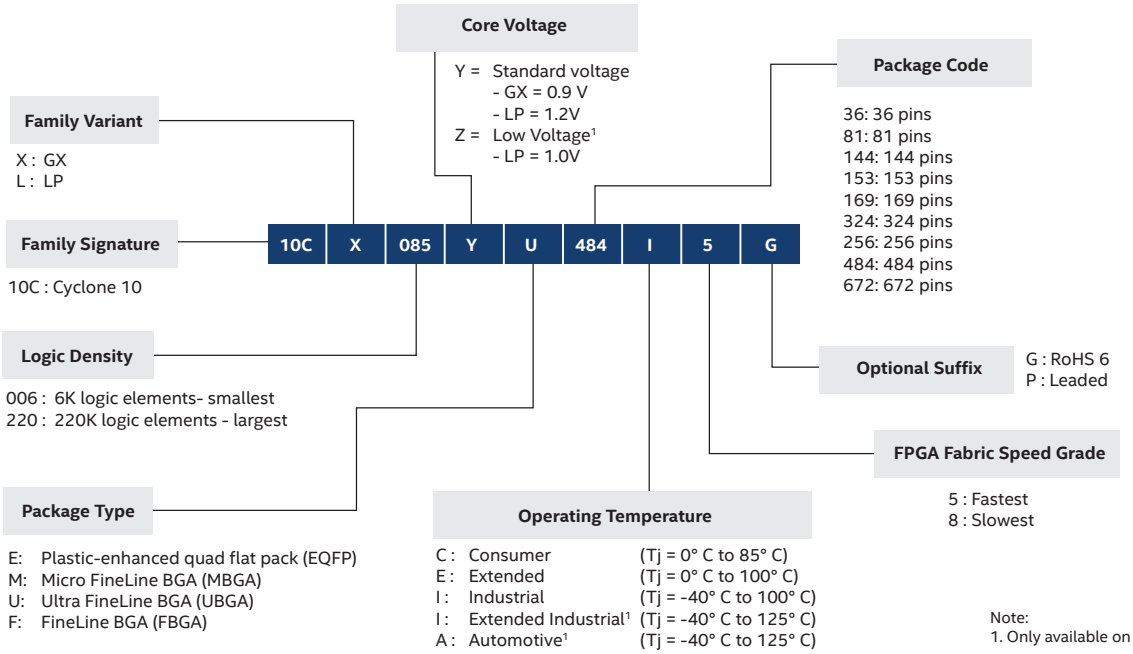
Ordering Information for Intel Stratix 10 (DX) Devices



Ordering Information for Intel Arria 10 (GX, SX, GT) Devices

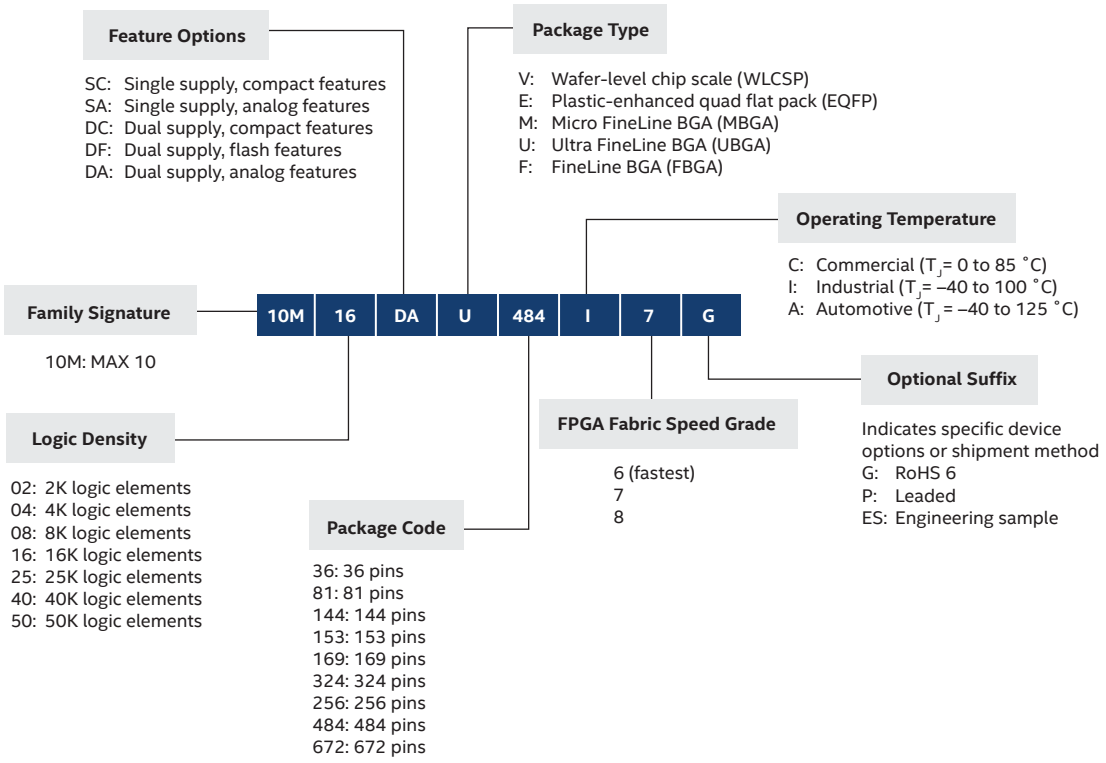


Ordering Information for Intel Cyclone 10 Devices

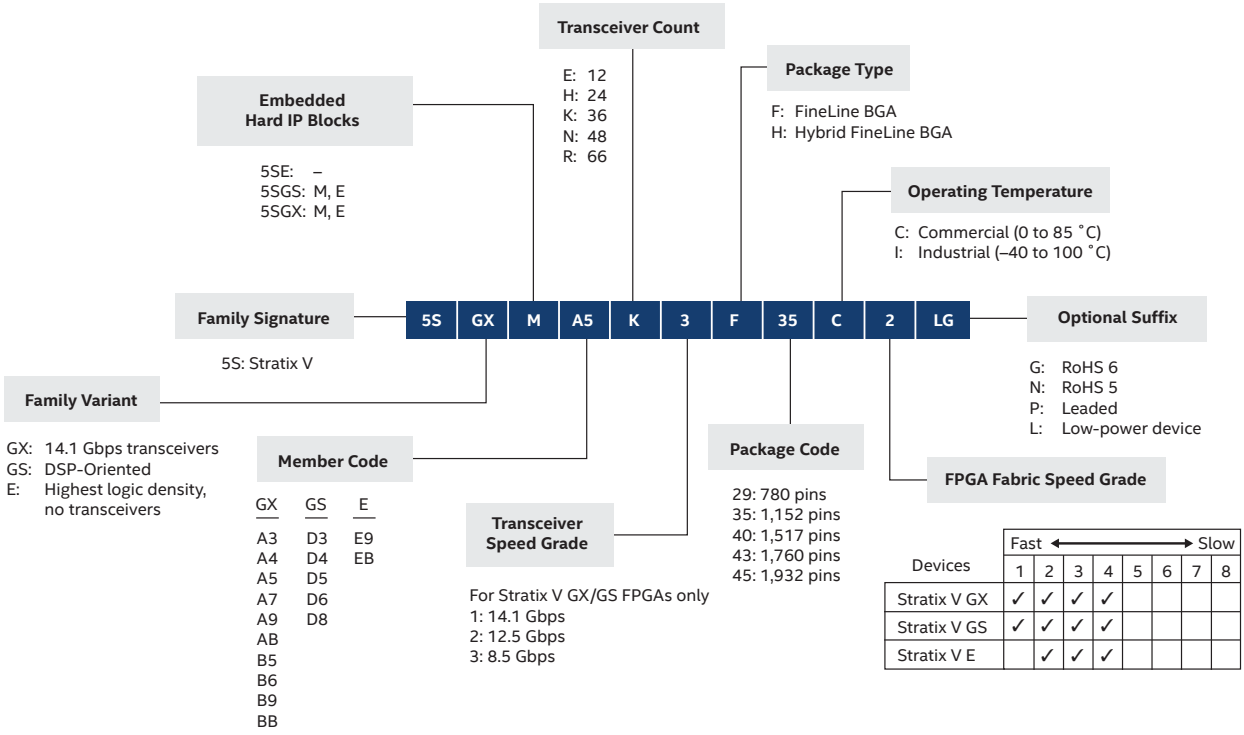


Note:
1. Only available on Intel Cyclone 10 LP

Ordering Information for Intel MAX 10 Devices

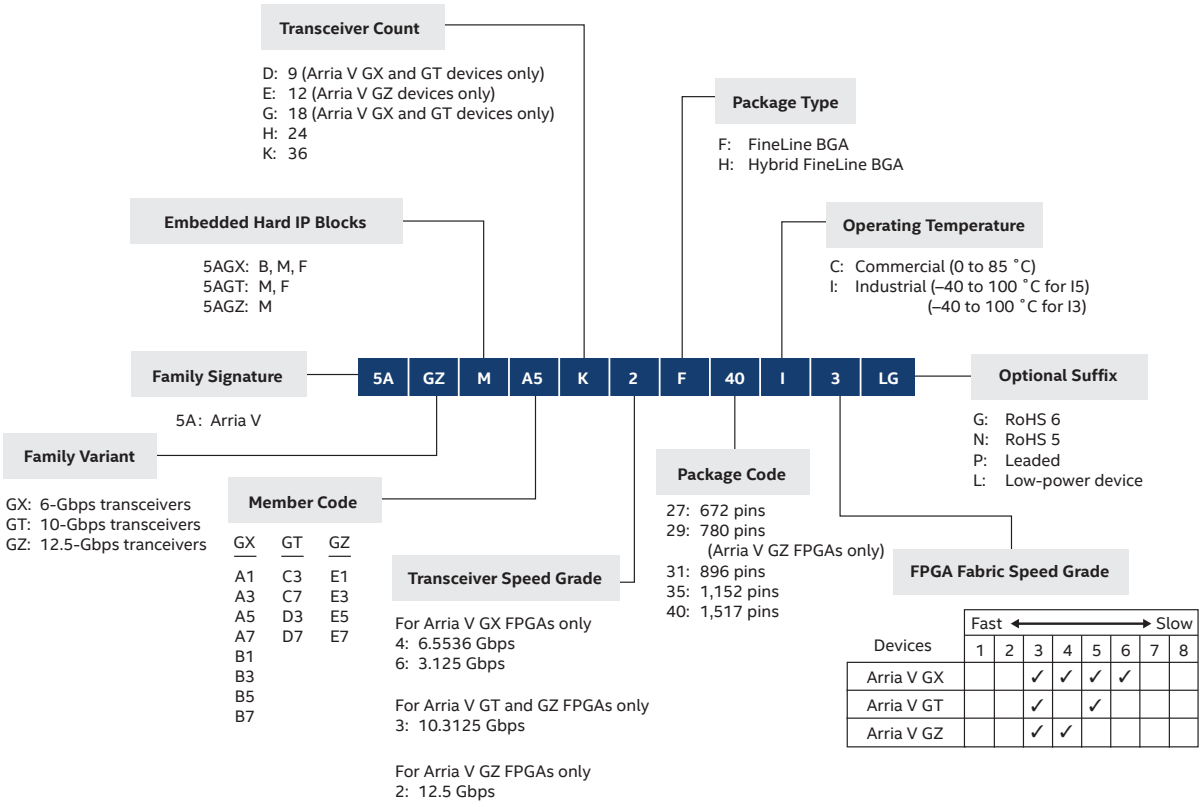


Ordering Information for Stratix V (GX, GS, E) Devices

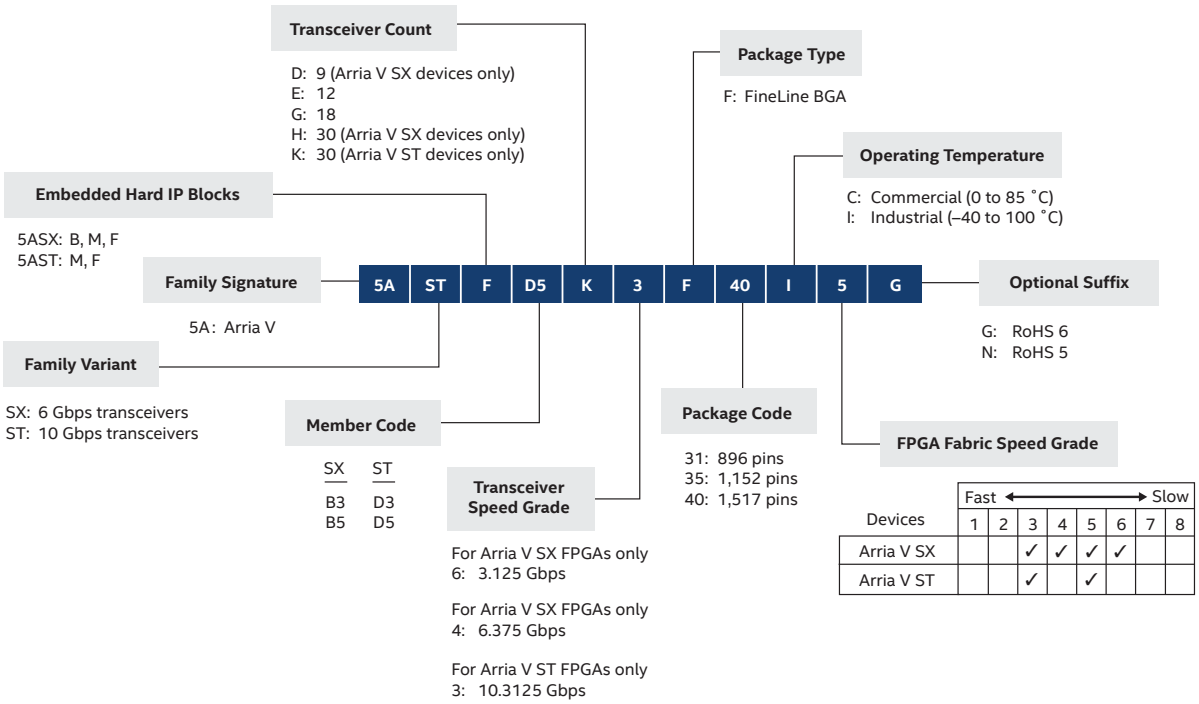


Devices	Fast ← → Slow							
	1	2	3	4	5	6	7	8
Stratix V GX	✓	✓	✓	✓				
Stratix V GS	✓	✓	✓	✓				
Stratix V E		✓	✓	✓				

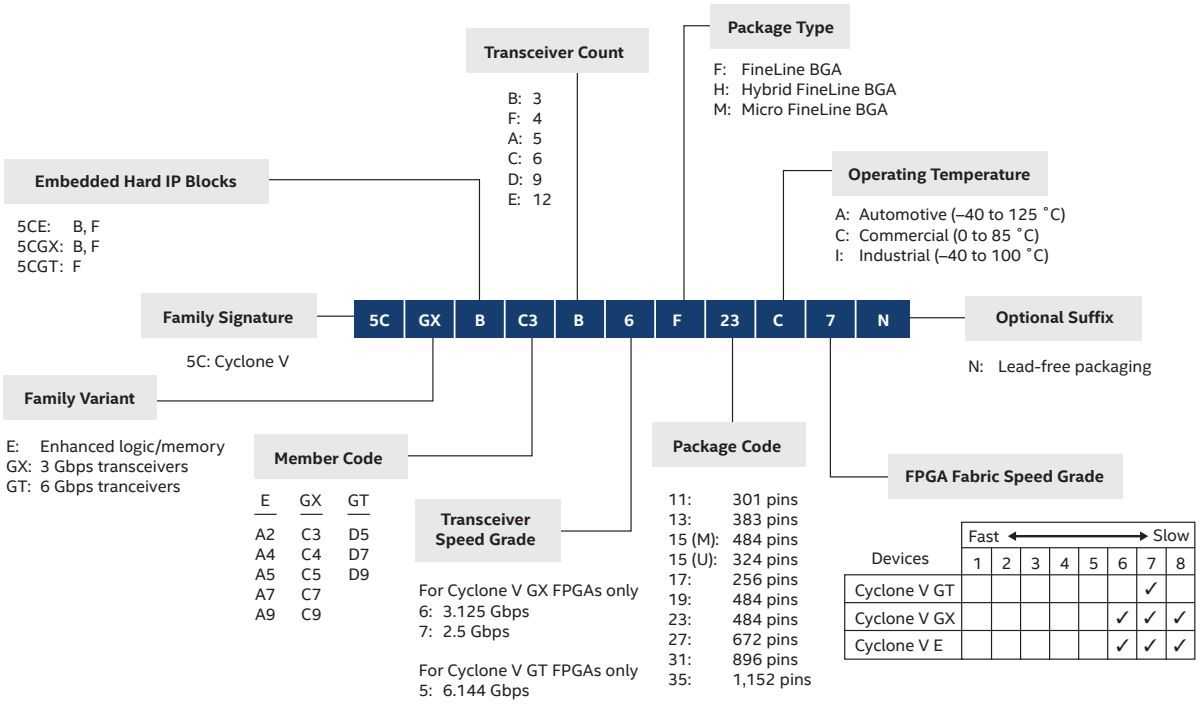
Ordering Information for Arria V (GT, GX, GZ) Devices



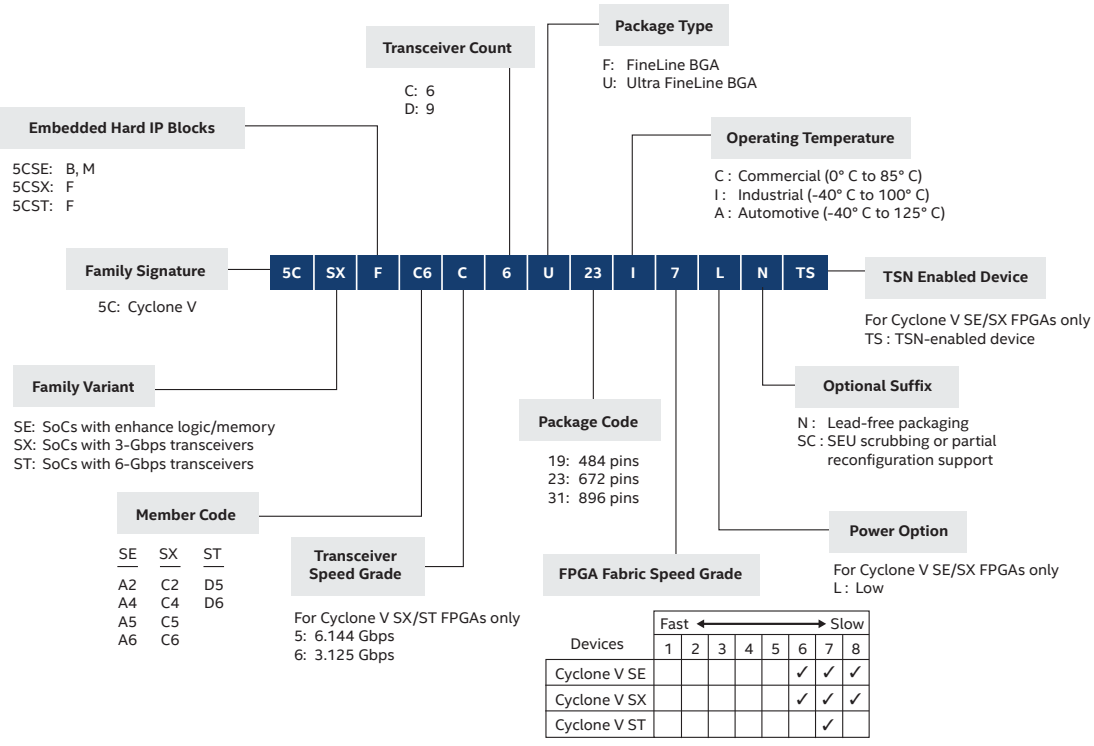
Ordering Information for Arria V (SX, ST) SoCs



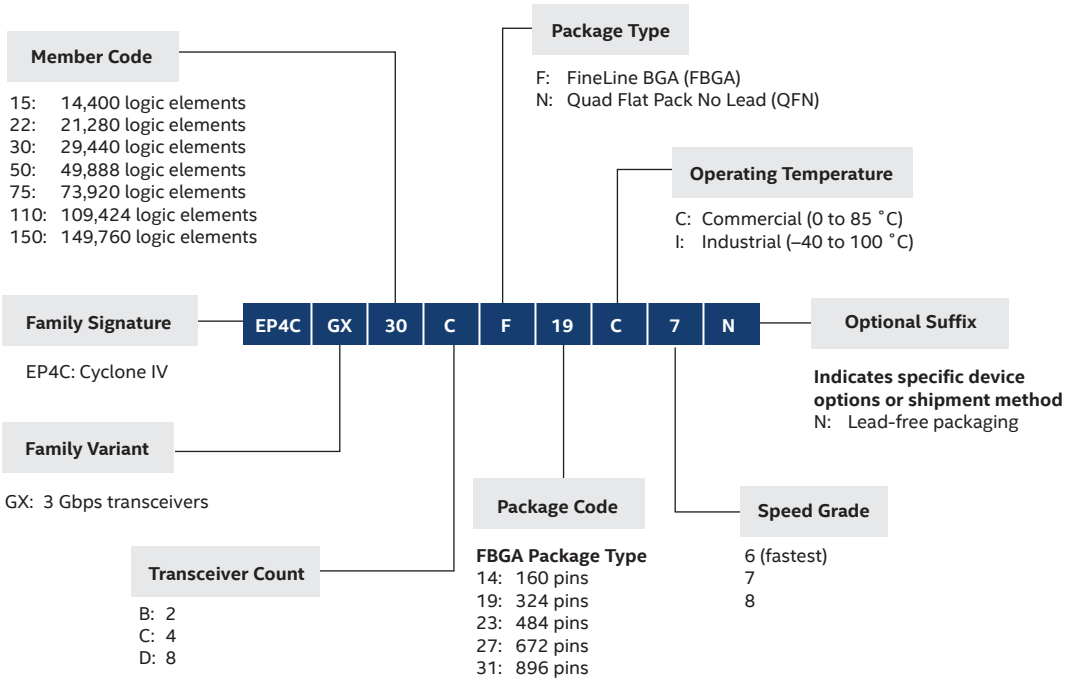
Ordering Information for Cyclone V (E, GX, GT) Devices



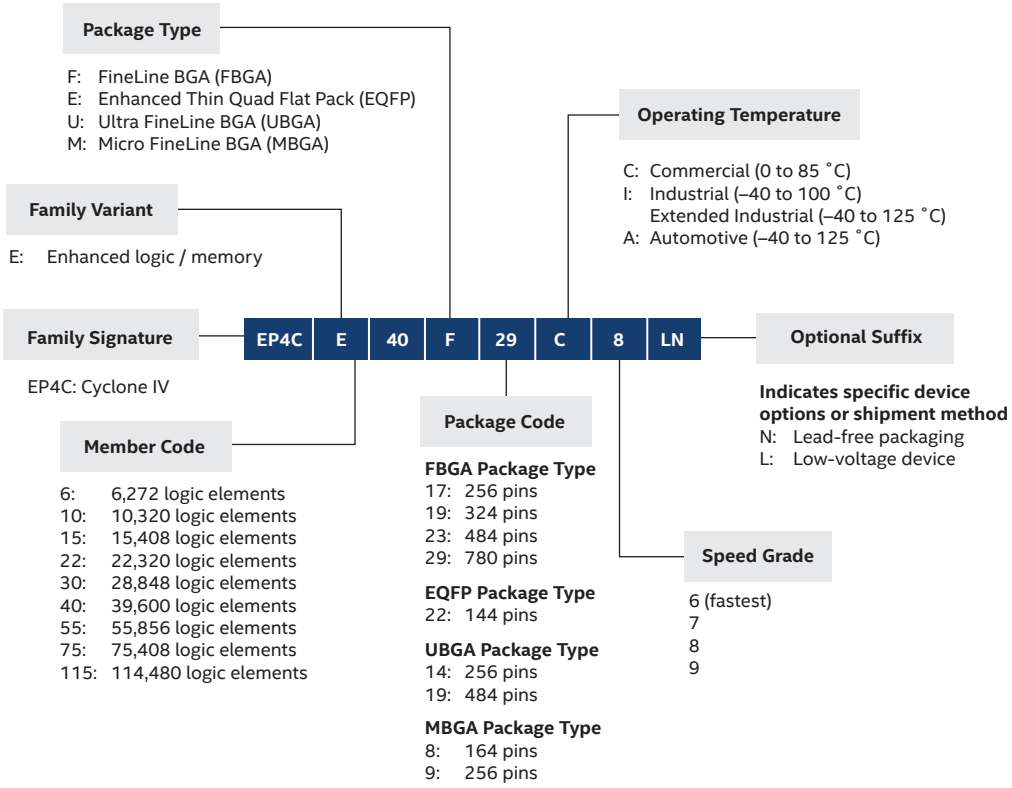
Ordering Information for Cyclone V (SE, SX, ST) SoCs



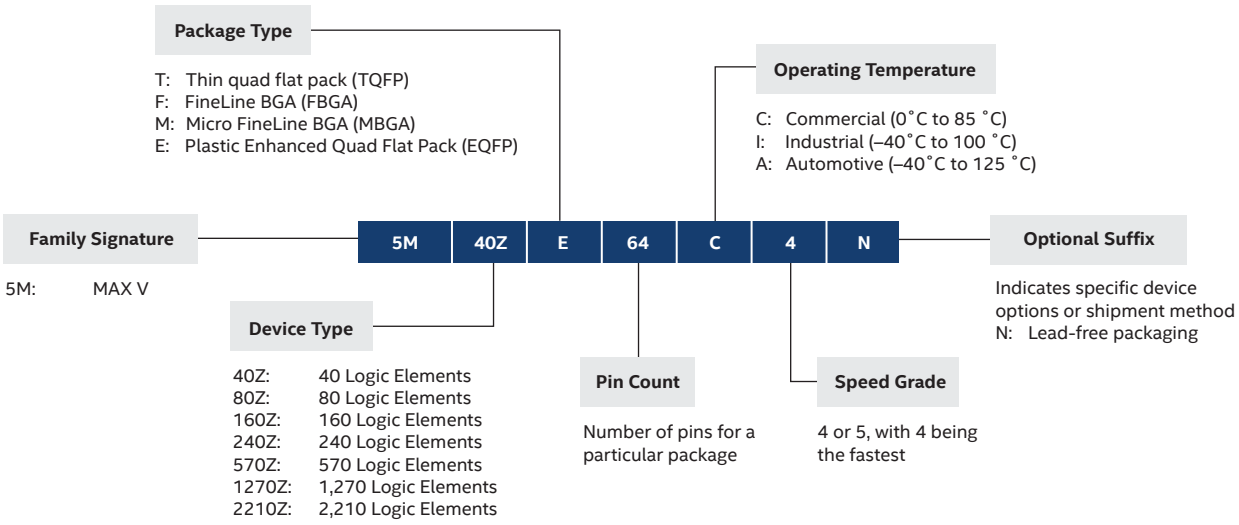
Ordering Information for Cyclone IV GX Devices



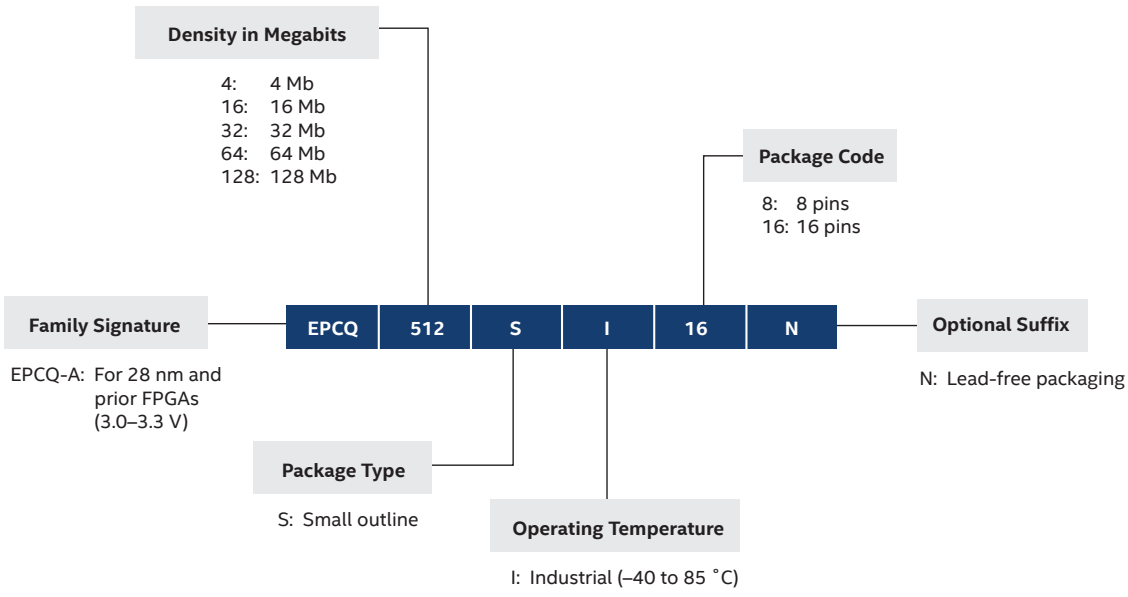
Ordering Information for Cyclone IV E Devices



Ordering Information for MAX V Devices



Ordering Information for Serial Configuration Devices



Intel FPGA Programmable Acceleration Overview

Accelerate your data center, cloud, and network infrastructure with a portfolio of Intel and partner Programmable Acceleration Cards (PACs), Infrastructure Processing Units (IPUs), and SmartNICs enabled by Intel's latest FPGA technology, designed and qualified for large volume deployments. Existing Intel® PAC platforms like the N3000 are supported by platform software such as the Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs, while the Intel® Open FPGA Stack (Intel® OFS) supports new Intel, third-party, or proprietary cards like the Silicom SmartNIC N5010. Intel's wide portfolio of platforms, cards, and software solutions enables your workloads to be efficiently developed, scaled, and deployed.

Intel SmartNICs and Programmable Acceleration Cards

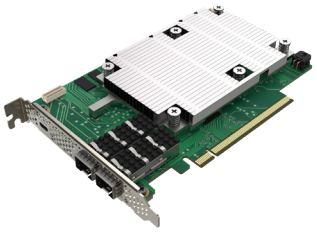
Intel® FPGA PAC N3000 accelerates network traffic for up to 100 Gbps to support low-latency, high-bandwidth 5G applications. This SmartNIC allows you to create custom-tailored solutions for core network workloads and Virtualized Radio Access Network (vRAN) to achieve faster time to market with the support of industry-standard orchestration and open source tools.

Intel® PAC with Intel® Arria® 10 GX FPGA provides FPGA acceleration in a low-power, low-profile form factor and inline acceleration for speeds of up to 40 Gbps. Its performance and versatility allow you to implement various solutions in data center and enterprise application acceleration.

Intel® FPGA PAC D5005 offers a high-density Intel Stratix 10 FPGA with a high-speed interface up to 100 Gbps for both look aside and inline acceleration of various data center and enterprise application—data analytics, AI, packet monitoring, and more.

Partner SmartNIC and IPU Acceleration Platforms

Silicom FPGA SmartNIC N5010 is the first hardware programmable 4X 100GE FPGA SmartNIC that enables next-generation IA-based servers to meet the performance needs of the 4/5G Core User Plane Function/Access Gateway Function (UPF/AGF). Its re-programmability can support Virtual Broadband Network Gateway (vBNG), Virtualized Evolved Packet Core (vEPC), Internet Protocol Security (IPSec), vFirewall, Segment Routing Version (SRv6), and Vector Packet Processing (VPP) workload capability.



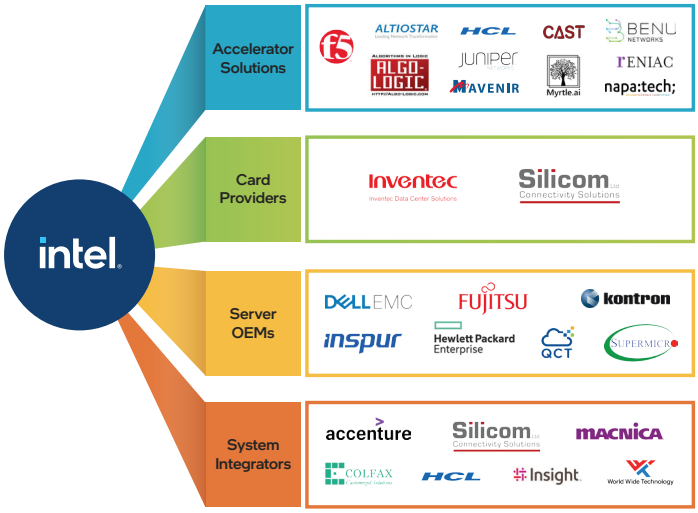
Cards based on the Intel FPGA IPU C5000X Platform

Silicom FPGA IPU C5010X and Inventec FPGA IPU C5020X adapters are Intel® Xeon® D processor, SoC + FPGA cards, offering a hardware programmable data path with 50G connectivity. With these IPUs, cloud service providers can improve server core utilization by offloading vSwitch and storage using the IA-optimized Data Plane Development Kit (DPDK) and Storage Performance Development Kit (SPDK).

Product Descriptions and Datasheets for Partner SmartNIC and IPU Acceleration Platforms can be found at the **Silicom** and **Inventec** websites, and are not located in this catalog.

Accelerated Workload Solutions with Intel Partners

Intel has engaged with leading providers of virtual appliances and accelerator functions best suited for FPGA acceleration. These partners build pre-designed accelerator functions that integrate seamlessly into common libraries, software frameworks, and your custom software application to minimize development investment and accelerate time to market. Our partners specialize in applications from 5G, network functions virtualization (NFV), data center, and more. All you need to do is select a card, identify a workload you want to accelerate, and let our partners take the effort out of your design. As a result, you get complete solutions and design services to minimize your development investment and accelerate your time to market.



Partners listed in the figure are examples and not all partners are represented.

Platform Software

You now have the choice to use the Intel Acceleration Stack for Intel Xeon CPU with FPGAs for existing Intel FPGA PACs, or to adopt the Intel OFS for new Intel, third-party, or proprietary cards or platforms.

The Intel Acceleration Stack for Intel Xeon CPU with FPGAs is a robust collection of software, firmware, and tools designed and distributed by Intel to make it easier to develop and deploy Intel FPGAs for workload optimization in the data center. Benefits to design engineers include saving design time, enabling code-reuse, and enabling the first common developer interface.

Intel OFS is a scalable, source-accessible hardware and software infrastructure delivered via git repositories that enables you to customize your own unique acceleration platform or card solutions. This second-generation hardware and software infrastructure is being used by Intel and selected third-party SmartNICs.

Why Choose Intel FPGAs for Acceleration Applications?

Ease of Deployment

Find validated and qualified Intel® FPGA Programmable Acceleration Cards (Intel® FPGA PACs) through several leading original equipment manufacturers (OEMs).

Standardization

Help eliminate complexity and enable application portability by leveraging the standard hardware and software interfaces provided by the Intel platform or card software.

Wide-range of Solutions

Discover what FPGAs can do for your business with the broad portfolio of acceleration solutions from technology experts.

Customization

Create customer platform or card solutions using source-accessible Intel® OFS hardware and software code.

Faster Time to Deployment

Experience faster time to deployment with native support for Intel OFS by leading open-source software distribution vendors.

Portability

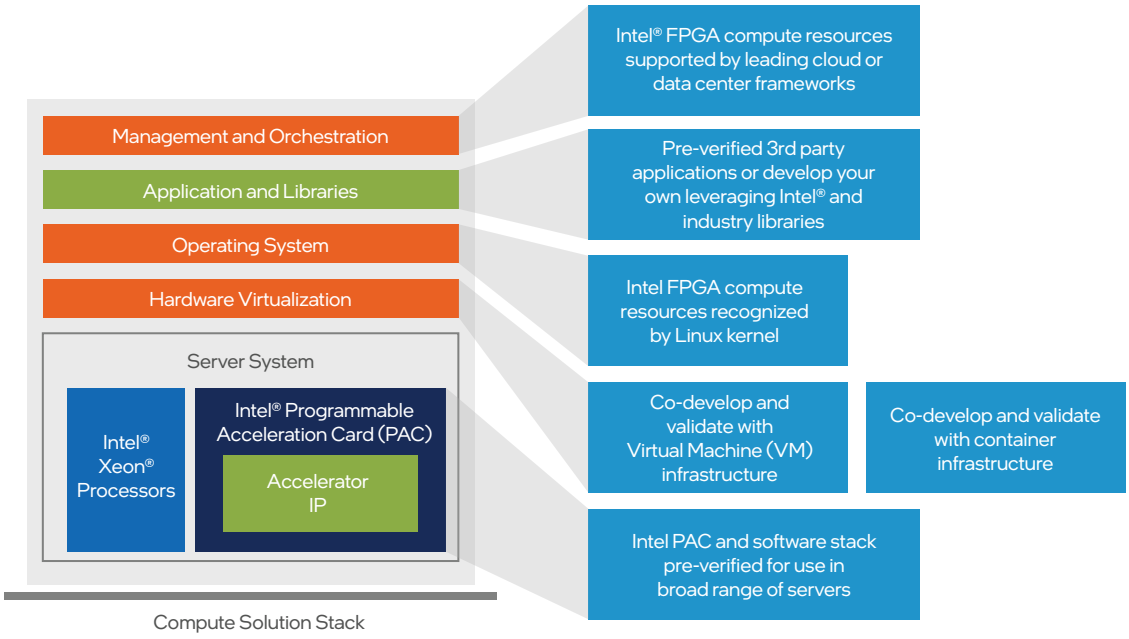
Achieve greater design portability through industry-standard interface support and reusable OFS Standard APIs.

Intel Acceleration Stack for Intel Xeon CPU with FPGAs

The Intel Acceleration Stack for Intel Xeon CPU with FPGAs is a robust collection of software, firmware, and tools designed and distributed by Intel to make it easier to develop and deploy Intel® FPGAs for workload optimization in the data center. The Intel Acceleration Stack for Intel Xeon CPU with FPGAs provides multiple benefits such as saving time, enabling code reuse, and providing the first common developer interface.

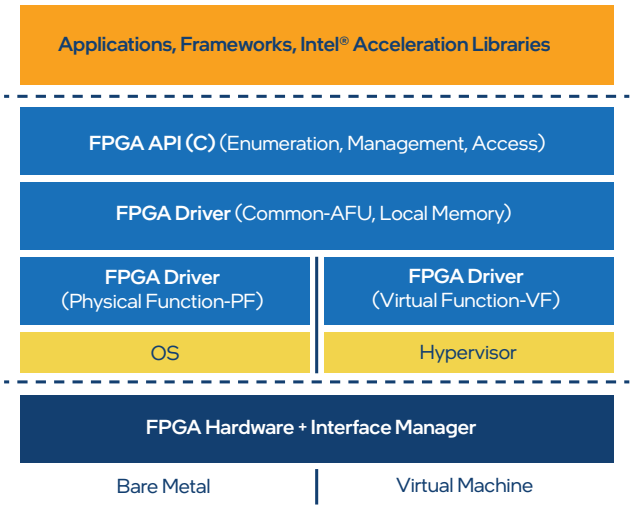
The Intel Acceleration Stack for Intel Xeon CPU with FPGAs provides multiple benefits to design engineers:

- Saves developer time to focus on unique value-add of their solution
- Enables code-reuse across multiple Intel FPGA form-factor products
- Establishes the world's first common developer interface for Intel FPGA data center products
- Offers optimized and simplified hardware and software APIs provided by Intel
- Enables growing adoption of Intel PACs by Intel partner ecosystem, further broadening appeal and simplifying use



Platform or Card Software

Open Programmable Acceleration Engine (OPAE) technology is a software programming layer that provides a consistent API across FPGA product generations and platforms. It is designed for minimal software overhead and latency, while providing an abstraction for hardware-specific FPGA resource details. To foster an open ecosystem and encourage the use of FPGA acceleration for data center workloads, Intel has open sourced the technology for the industry and developer community.



Intel Open FPGA Stack

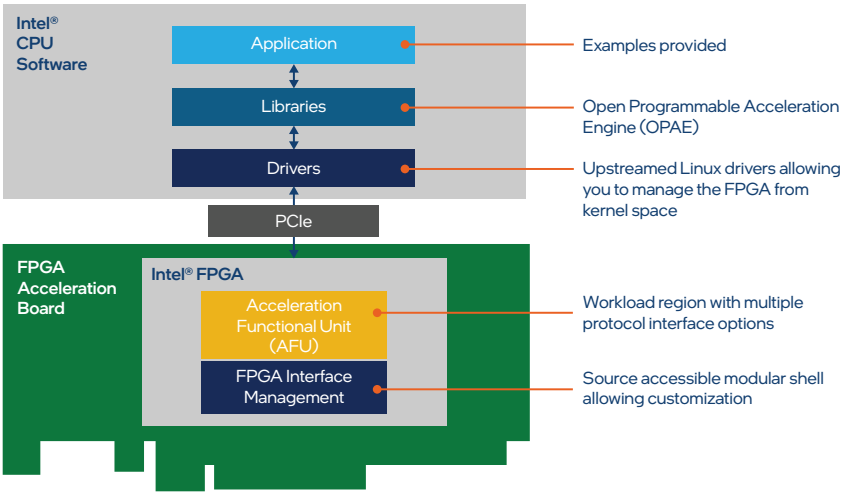
Intel Open FPGA Stack (Intel® OFS) is a scalable, source-accessible hardware and software infrastructure delivered through git repositories that enables you to customize your own unique acceleration platform or card solutions. Intel OFS provides open access to a source-accessible infrastructure, developed using an open source methodology, with standard interfaces and APIs. Developers are already using Intel OFS to develop on Intel and third-party platforms or cards featuring Intel Stratix 10 and Intel Agilex FPGA solutions.

Intel OFS provides multiple benefits to hardware, software, and application design engineers:

INTEL® OFS FEATURE	BOARD DEVELOPER	SOFTWARE DEVELOPER	APPLICATION DEVELOPER
Inherit an ecosystem of Intel® Open FPGA Stack-based boards, workloads, and OS distributors	✓	✓	✓
Accelerate software development by leveraging software drivers upstreamed to the Linux kernel and Open Programmable Acceleration Engine (OPAE) software and libraries		✓	✓
Accelerate workload development with industry-standard Arm AMBA AXI and Avalon compliant bus interfaces, workload examples, and simulation	✓		✓
Accelerate your verification and validation with automated build scripts, a United Verification Methodology (UVM) environment, and a suite of unit test cases	✓		
Customize your FPGA design (FIM) with modular and composable source code	✓		

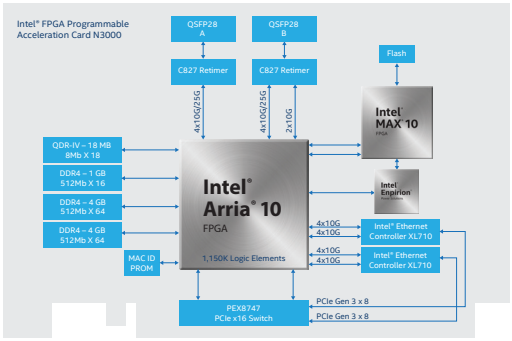
Early Access Program for Intel OFS

The Early Access Program (EAP) for Intel OFS runs through most of 2021. Intel OFS EAP members benefit from early access to Intel OFS code, documentation, and direct support from Intel. Those interested in trying Intel OFS for their next project or interested in details on the Intel OFS EAP should reach out to an Intel sales representative or visit **www.intel.com/ofs** to get started.



Intel FPGA Programmable Acceleration Card N3000

Intel FPGA Programmable Acceleration Card (Intel FPGA PAC) N3000 is a highly customizable card, which enables high-throughput, lower latency, and high-bandwidth applications. It allows the optimization of data plane performance to achieve lower costs while maintaining a high degree of flexibility. End-to-end industry-standard and open-source tool support allow you to quickly adapt to evolving workloads and industry standards. Intel is accelerating 5G and NFV adoption for ecosystem partners, such as telecommunications equipment manufacturers (TEMs), virtual network functions (VNF) vendors, system integrators, and telecommunications companies to bring scalable and high-performance solutions to market. This product includes a variant that is designed to be Network Equipment Building System (NEBS)-friendly and features a Root-of-Trust device that helps protect systems from FPGA hosted security exploits.



Targeted Workloads

- Fronthaul Gateway (FHGW)
- Open Virtual Switch (OvS)
- Contrail, tungsten fabric
- Segment routing for IPv6 (SRv6) VPP
- vRAN
- Distributed Denial of Service (DDoS), Virtual Firewall (vFW),and Virtual Broadband Network Gateway (vBNG) for H-QoS, classification, policing, scheduling, and shaping
- vEPC, 4G/5G UPF
- IPSec

Hardware

Intel Arria 10 GT FPGA
- High-performance, multi-gigabit SERDES transceivers up to 25.78 Gbps
- 1,150K logic elements
- 65.7 Mb on-chip memory
- 3,036 DSP blocks

Onboard Memory
- 9 GB DDR4
- 144 Mb QDR-IV

Interfaces
- PCIe Gen3 x16
- Dual Intel Ethernet Converged Network Adapter (Intel Ethernet CNA) XL710
- 2X QSFP with 10 Gbps and 25 Gbps support (up to 100GbE configuration)

Form Factor
- 1/2 length, full height; single slot

Board Management
- Intel MAX 10 FPGA BMC
  - Temperature and voltage readout
  - PLDM
- Remote update capabilities for FPGA flash memory and BMC

Power Management
- Intel Enpirion Power Solutions: Intelligent system power management with real-time telemetry and system health monitoring.

Software

- Data Plane Development Kit (DPDK)
- OPAE
- Acceleration Stack for Intel Xeon CPU with FPGAs
- FPGA Interface Manager

Design Entry Tools

- Intel Quartus Prime Pro Edition Software
- Intel FPGA SDK for OpenCL

Ordering Information

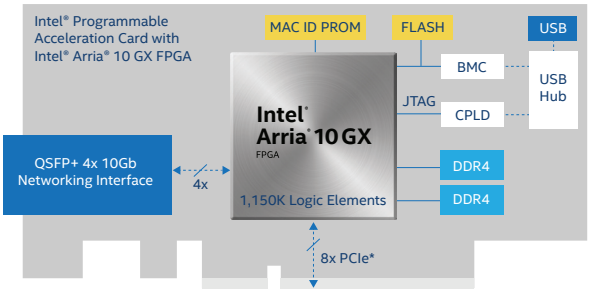
PART NUMBER	ETHERNET CONFIGURATION
BD-NFV-N3000-1	8x10G
BD-NVV-N3000-2	2x2x25G
BD-NVV-N3000-3	2x2/4x25G (NEBS[1] optimized)

[1] NEBS: Optimized for Network Equipment Building System (NEBS) applications

Contact an **Intel sales representative** for volume production orders.

Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

This PCIe-based FPGA acceleration card for data centers offers both inline and lookaside acceleration. It provides the performance and versatility of FPGA acceleration and is one of several cards or platforms supported by the Acceleration Stack for Intel Xeon CPUs with FPGAs. This acceleration stack provides a common developer interface for both application and accelerator function developers, and includes drivers, APIs, and an FPGA interface manager. Together with acceleration libraries and development tools, the acceleration stack saves developer time and enables code re-use across multiple Intel FPGA cards or platforms. The card can be deployed in a variety of servers with its small form factor, low-power dissipation, and passive heat sink.



Targeted Workloads

- Big data analytics
- Artificial intelligence
- Image transcoding
- Financial technology (FinTech)
- Packet Monitoring & Cyber security
- High-performance computing (HPC), such as genomics and oil and gas

Hardware

Intel Arria 10 GX FPGA

- High-performance, multi-gigabit serializer/deserializer (SERDES) transceivers up to 15 Gbps
- 1,150K logic elements available
- 65.7 Mb of on-chip memory
- 3,036 DSP blocks

On-Board Memory

- 8 GB DDR4 memory (4 GB x 2 banks)
- 1 Gb (128 MB) flash

Interfaces

- PCIe x8 Gen3 electrical, x16 mechanical
- USB 2.0 interface for debug and programming of FPGA and flash memory
- 1X QSFP+ with 4X 10GbE or 40GbE support

Form Factor

- ½ length, standard height; single slot with half height option
- 66 W thermal design power (TDP)

Board Management

- Temperature and voltage readout
- Platform Level Data Model (PLDM)

Software

- Acceleration Stack for Intel Xeon CPU with FPGAs
- FPGA Interface Manager installed
- OPAE

Design Entry Tools

- Intel Quartus Prime Pro Edition Software
- Acceleration Stack for Intel Xeon CPU with FPGAs
- Intel FPGA SDK for OpenCL

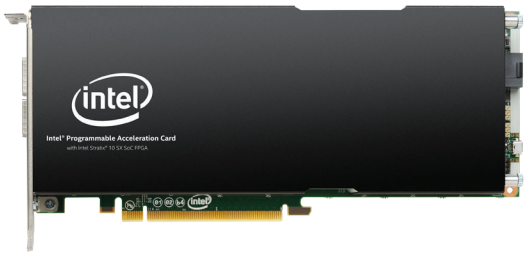
Ordering Information

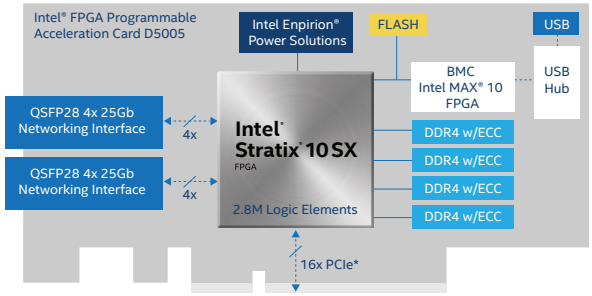
Buy now from:

- **Qualified server OEMs** listed on the Intel PAC with Intel Arria 10 GX FPGA website
- Authorized Intel Programmable Solutions **distributors** in your region
- **Arrow**, **Mouser**, **Digikey**, and **Colfax** (online purchase)
- Or, contact an **Intel sales representative**

Intel FPGA Programmable Acceleration Card D5005

This high-performance FPGA acceleration card for data centers offers both inline and lookaside acceleration. Expanding upon the Intel PAC portfolio, it offers inline high-speed interfaces up to 100 Gbps. The Intel FPGA PAC D5005 additional processing capability makes it ideal for FinTech and streaming analytics applications. It provides the performance and versatility of FPGA acceleration and is one of several cards or platforms supported by the Acceleration Stack for Intel Xeon CPU with FPGAs. This acceleration stack provides a common developer interface for both application and accelerator function developers, and includes drivers, APIs, and an FPGA interface manager. Together with acceleration libraries and development tools, the acceleration stack saves developer time and enables code re-use across multiple Intel FPGA cards or platforms.





Targeted Workloads

- FinTech
- Artificial intelligence
- Streaming analytics
- Video transcoding
- Genomics
- Packet Monitoring & Cyber security
- High-performance computing (HPC), such as genomics and oil and gas

Hardware

Intel Stratix 10 SX FPGA
- High-performance, multigigabit SERDES transceivers up to 26.3 Gbps
- 2,800K logic elements and 244 Mb on-chip memory
- 11,520 DSP blocks

Onboard Memory
- 32 GB DDR4 memory with error correction code
- 2 GB QSPI flash memory

Interfaces
- PCIe Gen3 x16
- USB 2.0 interface for debug and programming of FPGA and flash memory
- 2X QSFP+ with up to 100 Gbps support

Form Factor
- 3/4 length, full height; dual slot
- 215 W TDP

Board Management
- Intel MAX 10 FPGA Baseboard Management Controller (BMC)
  - Temperature and voltage readout
  - PLDM
  - Intelligent Platform Management Interface (IPMI 2.0)
- Remote Update capabilities for FPGA flash memory and BMC

Power Management
- Intel Enpirion Power Solutions: Intelligent system power management with real-time telemetry and system health monitoring.

Software

- Acceleration Stack for Intel Xeon CPU with FPGAs
- FPGA Interface Manager
- OPAE

Design Entry Tools

- Intel Quartus Prime Pro Edition Software
- Intel FPGA SDK for OpenCL

Ordering Information

Engineering sample: BD-ACD-1SX280H2DES

Production: BD-ACD-D5005

Development sample:
- **Qualified server OEMs** listed on the Intel FPGA PAC D5005 website
- Authorized Intel Programmable Solutions **distributors** in your region
- **Arrow** and **Mouser** (online purchase)
- Or, contact an **Intel sales representative**

Intel FPGA Acceleration Card Comparison

	FEATURES	INTEL PAC WITH INTEL ARRIA 10 GX FPGA	INTEL FPGA PAC D5005	INTEL FPGA PAC N3000	SILICOM FPGA SMARTNIC N5010	INVENTEC FPGA IPU C5020X ADAPTER
Product Category	Target Market	Cloud and Enterprise	Cloud and Enterprise	SmartNIC for Communications	SmartNIC for Communications	IPU for CSP
	Type	Intel FPGA PAC	Intel FPGA PAC	Intel FPGA PAC	Partner card	Partner card
FPGA Resources	FPGA	Intel Arria 10 GX	Intel Stratix 10 SX	Intel Arria 10 GT	Intel Stratix 10 DX	Intel Stratix 10 DX
	Logic Elements	1,150K	2,800K	1,150K	2,073K	1,325K
	On-chip Memory	65.7 Mb	244 Mb	65.7 Mb	240 Mb + 8 GB (HBM2)	114 Mb
	DSP Blocks	3,036	11,520	3,036	7,920	5,184
Processor	Type	-	-	-	-	Intel Xeon D-1612 Processor
Memory	DDR4	8 GB (4 GB x 2 banks)	32 GB (8 GB x 4 banks)	9 GB (4 GB x 2 banks + 1 GB)	32 GB	20 GB
	SRAM	-	-	144 Mb QDR IV	144 Mb QDR IV	-
	HBM	-	-	-	8 GB (2 x 4 GB)	-
	Flash	1 Gb	2 Gb	2 Gb	2 GB	1.25 Gb
Interfaces and Modules	PCI Express	Gen3 x8 (electrical) Gen3 x16 (mechanical)	Gen3 x16	Gen3 x16	Gen4 x16 edge connector Gen4 x16 over cable (N5000)	Gen3 x8, Gen4 x8 (Option)
	Network Interface	10 Gbps, 40 Gbps (up to 40 GbE)	10 Gbps, 25 Gbps, 40 Gbps, 100 Gbps	10 Gbps, 25 Gbps (up to 100 GbE) with Dual Intel Ethernet Controller XL710	4 x100 Gbps Dual Intel Ethernet Controller E810 (N5000)	2 x25 Gbps
	Intel MAX 10 FPGA Baseboard Management Controller (BMC)	-	Yes	Yes	Yes	Option
	FPGA Interface Manager	Yes	Yes	Yes	Yes	-
Mechanical, Thermal, and Power	Form Factor	½ length, full height ½ length, ½ height	¾ length, full height	½ length, full height	2/3 length, full height Full length, full height (N5000)	½ length, full height
	Width	Single slot	Dual slot	Single slot	Single slot (active cooling)	
	Maximum Power Consumption (TDP)	66 W	215 W	100 W	194 W	36 W (FPGA) + 22/30 W (Xeon-D 4C/8C)
Tools Support	Intel Acceleration Stack for Intel Xeon CPU with FPGAs	Yes	Yes	Yes	Yes	-
	Intel Quartus Prime Software	Yes	Yes	Yes	Yes	Yes
	Intel OneAPI Toolkits	Beta	Beta	-	TBD	-
	Data Plane Developer Kit (DPDK)	-	-	Yes	Yes	Yes
	Intel Distribution of OpenVINO™ Toolkit	Yes	-	-	-	-
How to buy	Contact to	Intel, OEMs, Distributors	Intel, OEMs, Distributors	Intel, OEMs, Distributors	Silicom	Inventec, Silicom

Accelerated Workload Solutions

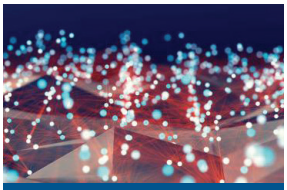
Intel's broad ecosystem enables leading providers to offer a variety of accelerator functions best suited for FPGA acceleration. A number of these providers have complete solutions enabled for Intel FPGA-based PACs, IPUs, and SmartNICs, ranging from NFV, network security and monitoring, data analytics, AI, and more.

VNF and NFV Infrastructure Acceleration Workloads

- Open vSwitch (OvS)
- Contrail
- Distributed Denial-of-Service (DDoS) and Virtual Firewall (vFW)
- Segment Routing Version (SRv6)
- Network Slicing

Wireless Application Workloads

Virtualized Radio Access Network (VRAN)



Fronthaul Gateway (FHGW)

Turbo/LDPC

Application Workloads for Enterprise and Cloud

Data Analytics

Artificial Intelligence

Packet Monitoring and Cyber Security

Media Processing

Genomics

Financial Services (FSI)

Visit the following website for the various partner acceleration solutions: www.intel.com/content/www/us/en/programmable/solutions/acceleration-hub/solutions.html

Intel Quartus Prime Design Software

www.intel.com/quartus

The Intel Quartus Prime Software is revolutionary in performance and productivity for FPGA, CPLD, and SoC designs, providing a fast path to convert your concept into reality. The Intel Quartus Prime Software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

INTEL QUARTUS PRIME DESIGN SOFTWARE			AVAILABILITY		
			PRO EDITION ($)	STANDARD EDITION ($)	LITE EDITION (FREE)
Device Support	Intel Agilex series		✓		
	Intel Stratix series	IV, V		✓	
		10	✓		
	Intel Arria series	II			✓[1]
		II, V		✓	
		10	✓	✓	
	Intel Cyclone series	IV, V		✓	✓
		10 LP		✓	✓
		10 GX	✓[2]		
	Intel MAX series			✓	✓
Design Flow	Partial reconfiguration		✓	✓[3]	
	Block-based design		✓		
	Incremental optimization		✓		
Design Entry/Planning	IP Base Suite		✓	✓	Available for purchase
	Intel® HLS Compiler		✓	✓	✓
	Platform Designer (Standard)			✓	✓
	Platform Designer (Pro)		✓		
	Design Partition Planner		✓	✓	
	Chip Planner		✓	✓	✓
	Interface Planner		✓		
	Logic Lock regions		✓	✓	
	VHDL		✓	✓	✓
	Verilog		✓	✓	✓
	SystemVerilog		✓	✓[4]	✓[4]
	VHDL-2008		✓	✓[4]	
Functional Simulation	Questa*-Intel® FPGA Starter Edition software		✓	✓	✓
	Questa-Intel FPGA Edition software		✓[5]	✓[5]	✓[5]
Compilation (Synthesis & Place and Route)	Fitter (Place and Route)		✓	✓	✓
	Register retiming		✓	✓	
	Fractal synthesis		✓		
	Multiprocessor support		✓	✓	
Timing and Power Verification	Timing Analyzer		✓	✓	✓
	Design Space Explorer II		✓	✓	✓
	Power Analyzer		✓	✓	✓
	Power and Thermal Calculator		✓[6]		
In-System Debug	Signal Tap Logic Analyzer		✓	✓	✓
	Transceiver toolkit		✓	✓	
	Intel Advanced Link Analyzer		✓	✓	
Operating System (OS) Support	Windows/Linux 64 bit support		✓	✓	✓

Notes:
1. The only Arria II FPGA supported is the EP2AGX45 device.
2. The Intel Cyclone 10 GX device support is available for free in the Pro Edition software.
3. Available for Cyclone V and Stratix V devices only and requires a partial reconfiguration license.
4. For language support, refer to the **Verilog and SystemVerilog Synthesis Support** section of the Intel Quartus Prime Standard Edition User Guide.
5. Requires an additional license.
6. Integrated in the Intel Quartus Prime Software and available as a standalone tool. Only supports Intel Agilex and Intel Stratix 10 devices.

ADDITIONAL DEVELOPMENT TOOLS

TOOLS	DESCRIPTION
Intel FPGA SDK for OpenCL	• No additional licenses are required. • Supported with the Intel Quartus Prime Pro/Standard Edition Software. • The software installation file includes the Intel Quartus Prime Pro/Standard Edition Software and the OpenCL software.
Intel HLS Compiler	• No additional license required. • Now available as a separate download. • Supported with the Intel Quartus Prime Pro Edition Software.
DSP Builder for Intel FPGAs	• Additional licenses are required. • DSP Builder for Intel FPGAs (Advanced Blockset only) is supported with the Intel Quartus Prime Pro Edition Software for Intel Agilex, Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices.
Nios II Embedded Design Suite	• No additional licenses are required. • Supported with all editions of the Intel Quartus Prime Software. • Includes Nios II software development tools and libraries.
Intel SoC FPGA Embedded Development Suite (SoC EDS)	• Requires additional licenses for Arm* Development Studio for Intel® SoC FPGA (Arm* DS for Intel® SoC FPGA). • The SoC EDS Standard Edition is supported with the Intel Quartus Prime Lite/Standard Edition Software and the SoC EDS Pro Edition is supported with the Intel Quartus Prime Pro Edition Software.

INTEL QUARTUS PRIME DESIGN SOFTWARE FEATURES SUMMARY

Interface Planner	Enables you to quickly create your I/O design using real time legality checks.
Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
Platform Designer	Accelerates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect based on a network-on-a-chip architecture.
Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Intel and from Intel's third-party IP partners.
Synthesis	Provides expanded language support for System Verilog and VHDL 2008.
Scripting support	Supports command-line operation and Tcl scripting.
Incremental optimization	Offers a faster methodology to converge to design sign-off. The traditional fitter stage is divided into finer stages for more control over the design flow.
Partial reconfiguration	Creates a physical region on the FPGA that can be reconfigured to execute different functions. Synthesize, place, route, close timing, and generate configuration bitstreams for the functions implemented in the region.
Block-based design flows	Provides flexibility of reusing timing-closed modules or design blocks across projects and teams.
Intel Hyperflex FPGA Architecture	Provides increased core performance and power efficiency for Intel Stratix 10 devices.
Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Intel Quartus Prime Software settings to find optimal results.
Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
Chip planner	Reduces verification time while maintaining timing closure by enabling small, post-placement and routing design changes to be implemented in minutes.
Timing Analyzer	Provides native Synopsys Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
Signal Tap logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
Power Analyzer	Enables you to analyze and optimize both dynamic and static power consumption accurately.
Design Assistant	A design rules checking tool that allows you to get to design closure faster by reducing the number of iterations needed and by enabling faster iterations with targeted guidance provided by the tool at various stages of compilation.
Fractal synthesis	Enables the Intel Quartus Prime Software to efficiently pack arithmetic operations in the FPGA's logic resources resulting in significantly improved performance.
EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit www.intel.com/fpgaedapartners.

Getting Started Steps

Step 1: Download the free Intel Quartus Prime Lite Edition Software
www.intel.com/quartus

Step 2: Get oriented with the Intel Quartus Prime Software interactive tutorial.
After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training
www.intel.com/fpgatraining

Purchase the Intel Quartus Prime Software and increase your productivity today.

INTEL QUARTUS PRIME SOFTWARE
Intel Quartus Prime Software (Standard and Pro Edition) and Questa*-Intel® FPGA Edition software are bundled together into one single ordering part number effective October 15, 2021.
SW-ONE-QUARTUS Price: $3,645
The purchase can be applied for Fixed or Floating or Renewal licenses. Refer to the following product advisories for more information: • ADV 2127 Single Ordering Part Number for Intel Quartus Prime Software

QUESTA-INTEL FPGA EDITION SOFTWARE	QUESTA-INTEL FPGA STARTER EDITION SOFTWARE
SW-QUESTA-PLUS	SW-QUESTA
$1,995	Free
Questa-Intel FPGA Edition software is available for $1,995	Questa-Intel FPGA Starter Edition is available for free, but requires a license that can be generated at the Self-Service Licensing Center. It is 40% the performance of the Questa-Intel FPGA Edition software.
Refer to the following product advisories for more information: • ADV 2122 Replacement of ModelSim*-Intel® FPGA Edition Software	

DSP Builder for Intel FPGAs

www.intel.com/dspbuilder

The DSP Builder for Intel FPGAs is a DSP development tool that allows push-button HDL generation of DSP algorithms directly from the MathWorks Simulink environment. This tool adds additional libraries alongside existing Simulink libraries with the DSP Builder for Intel FPGAs (Advanced Blockset) and DSP Builder for Intel FPGAs (Standard Blockset). Intel recommends using the DSP Builder for Intel FPGAs (Advanced Blockset) for new designs. The DSP Builder for Intel FPGAs (Standard Blockset) is not recommended for new designs except as a wrapper for the DSP Builder for Intel FPGAs (Advanced Blockset).

DSP BUILDER FOR INTEL FPGAs FEATURES

The DSP Builder for Intel FPGAs (Advanced Blockset) offers the following features:

- Arithmetic logic unit (ALU) folding to build custom ALU processor architectures from a flat data-rate design
- High-level synthesis optimizations, auto-pipeline insertion and balancing, and targeted hardware mapping
- High-performance fixed- and floating-point DSP with vector processing
- Auto memory mapping
- Single system clock datapath
- Flexible 'white-box' fast Fourier transform (FFT) toolkit with an open hierarchy of libraries and blocks for users to build custom FFTs

Generate resource utilization tables for all designs without the Intel Quartus Prime Software compile.

Automatically generate projects or scripts for the Intel Quartus Prime Software, the Questa*-Intel FPGA software, Timing Analyzer, and Platform Designer.

FEATURES	DSP BUILDER FOR INTEL FPGAS (STANDARD BLOCKSET)	DSP BUILDER FOR INTEL FPGAS (ADVANCED BLOCKSET)
High-level optimization		✓
Auto pipeline insertion		✓
Floating-point blocks		✓
Resource sharing		✓
IP-level blocks	✓	✓
Low-level blocks	✓	✓
System integration	✓	✓
Hardware co-simulation	✓	✓

Purchase the DSP Builder for Intel FPGAs to meet high-performance DSP design needs today.

PRICING	OPERATING SYSTEM
$1,995 Primary $1,995 Renewal Subscription for one year	Windows/ Linux

Getting Started with the DSP Builder for Intel FPGAs

Step 1: Download the Intel Quartus Prime Pro or Standard Edition Software (www.intel.com/quartus):
- Pro Edition to target the latest Intel Agilex, Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices.
- Standard Edition to target Intel Arria 10, Intel Cyclone 10 LP, Intel MAX 10, Stratix V, and Cyclone V devices.

Step 2: Purchase additional DSP Builder for Intel FPGAs and MATLAB software licenses:
- DSP Builder for Intel FPGAs software license
- MATLAB software license

Step 3: Follow the following required order of installation:
a. Intel Quartus Prime Software
b. MathWorks MATLAB software
c. DSP Builder for Intel FPGAs

Step 4: To view the DSP Builder for Intel FPGAs version history and software requirements, visit the DSP Builder for Intel FPGAs Version History and Software Requirements web page.

Step 5 : To learn how to add your DSP Builder for Intel FPGAs license to your MATLAB installation, refer to the Installing and Licensing DSP Builder for Intel FPGAs web page.

Intel FPGA SDK for OpenCL

www.intel.com/opencl

Intel FPGA SDK for OpenCL[1] allows you to accelerate applications on FPGAs by abstracting away the complexities of FPGA design. Software programmers can write hardware-accelerated kernel functions in OpenCL that is an ANSI C-based language with additional OpenCL constructs to extract parallelism and program heterogeneous platforms. FPGAs are the accelerator of choice for heterogeneous systems, providing low latency, performance, and power efficiency versus GPUs and CPUs.

INTEL FPGA SDK FOR OPENCL SOFTWARE FEATURES SUMMARY	
Offline Compiler	• GCC-based model compiler of OpenCL kernel code
OpenCL Utility	• Diagnostics for board installation • Flash or program FPGA image • Install board drivers (typically PCI Express)
Intel Code Builder for OpenCL API	• Edit, build, and debug OpenCL kernels • Collect runtime performance • View generated reports
Operating System	• Microsoft Windows 10 • Red Hat Enterprise Linux 6 • Read Hat Enterprise Linux 7 • SUSE SLE 12 • Ubuntu 14.04 LTS • Ubuntu 16.04 LTS • Ubuntu 18.04 LTS
Memory Requirements	• Computer equipped with at least 32 GB RAM

Notes:
1. Product is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

Getting Started with the Intel FPGA SDK for OpenCL

Step 1: Download the Intel Quartus Prime Pro Edition Software to target the latest Intel Agilex, Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 devices.

Note: The software installation file includes the OpenCL software and Intel Quartus Prime Pro Edition Software. The Intel Quartus Prime Software requires a license purchase but no additional licenses are required for the Intel FPGA SDK for OpenCL.

Step 2: Download the Intel Board Support Package (BSP) that is needed to run your OpenCL application. You can also purchase a partner provided BSP, or create a custom BSP.

Step 3: For more information, read the Intel FPGA SDK for OpenCL Getting Started Guide.

Embedded Software and Tools for Intel SoC FPGA

www.intel.com/soceds

The Intel SoC FPGA Embedded Development Suite (SoC EDS) is a comprehensive tool suite for embedded software development on Intel SoC FPGAs. It comprises development tools, utility programs, and design examples to jump-start firmware and application software development. The SoC EDS is available in Standard and Pro Editions. The Standard Edition includes extensive support for 28 nm SoC FPGA families, whereas the Pro Edition is optimized to support the advanced features in the next-generation SoC FPGA families. In addition, the SoC EDS works in conjunction with the Arm Development Studio for Intel SoC FPGA (Arm DS for Intel SoC FPGA). This toolkit enables embedded developers to code, build, debug, and optimize in a single Eclipse-based IDE. The Arm DS for Intel SoC FPGA licenses are available in two options: a 30-day evaluation license and a paid Arm DS for Intel SoC FPGA license. The Arm DS for Intel SoC FPGA license is included at no cost with Intel SoC FPGA Development Kits.

INTEL SoC FPGA EMBEDDED DEVELOPMENT SUITE

	KEY FEATURES	AVAILABILITY			
		STANDARD		PRO	
		EVALUATION LICENSE	PAID LICENSE	EVALUATION LICENSE	PAID LICENSE
Supported Device Families	Cyclone V SoC	✓	✓		
	Arria V SoC	✓	✓		
	Intel Arria 10 SoC	✓	✓	✓	✓
	Intel Stratix 10 SoC			✓	✓
	Intel Agilex SoC			✓	✓
Compiler Tools	Linaro Compiler[1]	✓	✓	✓	✓
	Arm Compiler 5 (included in the Arm DS for Intel SoC FPGA)		✓		
	Arm Compiler 6 (included in the Arm DS for Intel SoC FPGA)		✓		✓
Libraries	Hardware Libraries (HWLIBs)	✓	✓	✓	✓
Other Tools	Quartus Prime Programmer	✓	✓	✓	✓
	Signal Tap Logic Analyzer	✓	✓	✓	✓
	Intel FPGA Boot Disk Utility	✓	✓	✓	✓
	Device Tree Generator	✓	✓	✓	✓
Design Examples	Golden Hardware Reference Design (GHRD) for SoC development kits	✓	✓	✓	✓
	Triple-Speed Ethernet (TSE) with Modular Scatter-Gather Direct Memory Access (mSG-DMA)[2]	✓	✓	✓	✓
	PCI Express Root Port with Message Signal Interrupts (MSI)[2]	✓	✓	✓	✓
	Partial Reconfiguration design example[3]			✓	✓
Host OS Support	Windows 7 64 bit	✓	✓	✓	✓
	Windows 10 64 bit	✓	✓	✓	✓
	Red Hat Linux 6 64 bit	32 bit libraries are required	32 bit libraries are required	32 bit libraries are required	32 bit libraries are required
Ubuntu 18		✓	✓	✓	✓

ARM DEVELOPMENT STUDIO FOR INTEL SOC FPGA

Arm DS for Intel SoC FPGA	Linux application debugging over Ethernet	✓	✓	✓	✓
	Debugging over Intel FPGA Download Cable II · Board bring-up · Device driver development · Operating system (OS) porting · Bare-metal programming · Arm CoreSight trace support		✓		✓
	Debugging over DSTREAM · Board bring-up · Device driver development · OS porting · Bare-metal programming · Arm CoreSight trace support		✓		✓
	FPGA-adaptive debugging · Auto peripheral register discovery · Cross-triggering between CPU and FPGA domains · Arm CoreSight trace support · Access to System Trace Module (STM) events		✓		✓
	Streamline Performance Analyzer support	Limited	✓	Limited	✓

Notes:
1. You have to download the Linaro Compiler.
2. These design examples are only available through Rocketboards.org.
3. For Intel Arria 10 SoC only.
4. Individual components of SoC EDS can now be downloaded from Github
5. Intel has migrated to Arm DS for Intel SoC FPGA. Arm DS for Intel SoC FPGA is no longer a part of SoC EDS and is a separate download from www.intel.com.

SoC FPGA Operating System Support

Intel and our ecosystem partners offer comprehensive operating system support for Intel SoC FPGA development boards that support the Arm Cortex-A9 processor.

OPERATING SYSTEM	COMPANY
Abassi	Code Time Technologies
Android	MRA Digital
AUTOSAR MCAL	Intel
Bare-Metal/Hardware Libraries	Intel
Carrier Grade Edition 7 (CGE7)	MontaVista
DEOS	DDC-I
eCosPro	eCosCentric
eT-Kernel	eSOL
FreeRTOS	FreeRTOS.org
INTEGRITY RTOS	Green Hills Software
Linux	Open Source (www.rocketboards.org)
Nucleus	Mentor Graphics
OSE	Enea
PikeOS	Sysgo
QNX Neutrino	QNX
RTEMS	RTEMS.org
RTXC	Quadros System
ThreadX	Express Logic
uC/OS-II, uC/OS-III	Micrium
uC3 (Japanese)	eForce
VxWorks	Wind River
Wind River Linux	Wind River
Windows Embedded Compact 7	Microsoft (Witekio)

More Information

For the latest on OS support for Intel SoCs, visit www.intel.com/socecosystem

Nios® V Processor

The Nios® V processor is the next generation of soft processor for Intel FPGAs based on the open-source industry standard RISC-V Instruction Set Architecture. This processor is available in the Intel Quartus Prime Pro Edition Software starting with version 21.3. The first core in the Nios V processor series is the the Nios V/m microcontroller. Additional cores in future releases will be Nios V/g general-purpose processor, an application-class processor, and a Linux-capable processor.

You can use the Nios V processor together with the Arm processor in Intel SoCs to create effective multi-processor systems.

With the Nios V processor you can:

- Lower overall system cost and complexity by integrating external processors into the FPGA.
- Target the Intel Agilex, Intel Stratix 10, Intel Arria 10, Intel Cyclone 10 devices, or the FPGA portion of the Intel Agilex, Intel Stratix 10, and Intel Arria 10 SoC. Support on Intel Quartus software standard devices coming soon.
- Leverage the community-maintained ecosystem to get your designs to market faster by choosing from the most up-to-date and modern toolchains, debuggers, and real-time operating system (RTOS) for your software development
- Take advantage of the free license for the Nios V/m microcontroller core to get started today

Hardware development

- Intel Quartus Prime Pro Edition Software
- Platform Designer
- Signal Tap logic analyzer
- System Console for low-level debugging of Platform Designer systems

Software development

- Initial development is supported using the open-source ecosystem starting with Intel Quartus Prime Pro Edition Software v21.3
- Unified debugger for homogeneous and heterogeneous debug capabilities coming in 2022

Licensing

A license is required for Nios V processors. Nios V/m embedded processor license is available at no cost in the Self-Service Licensing Center.

Getting started

To learn more about the Nios V processor, visit www.intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html.

Nios® II Processor

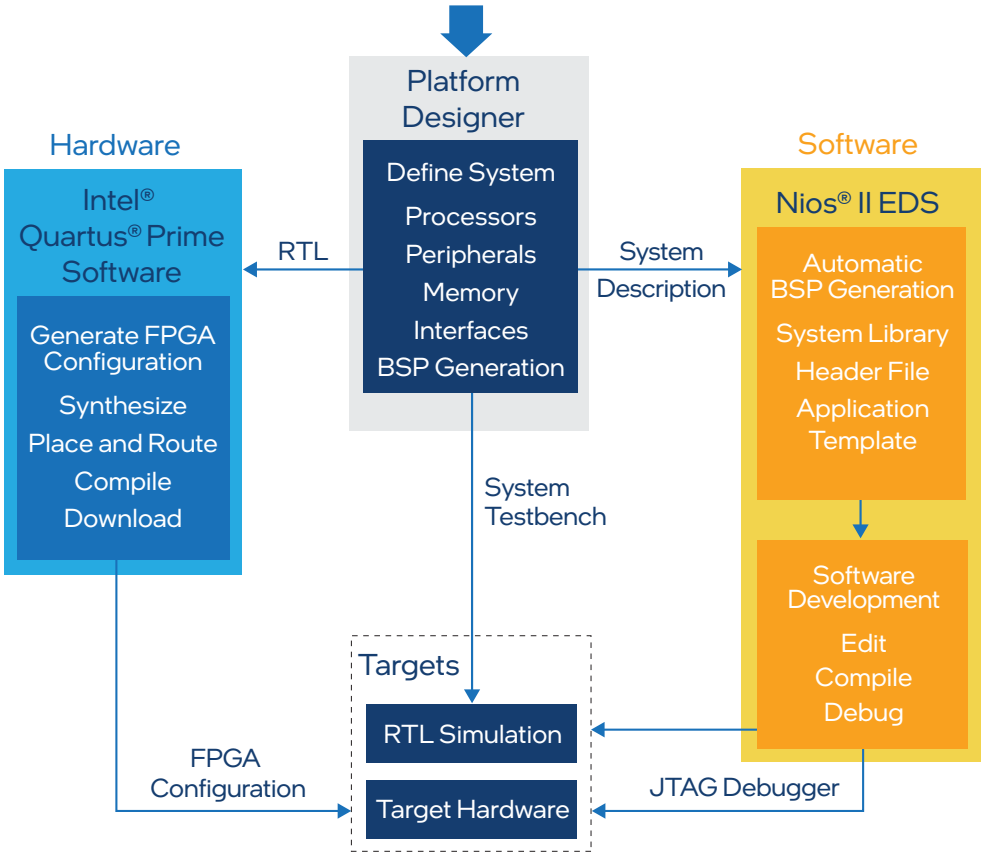
In any Intel FPGA, the Nios® II processor offers a custom system solution that has the flexibility of software and the performance of hardware. Through its innovative design, the Nios II processor leverages the logic resources of the device to provide unprecedented hard and soft real-time capabilities.

You can also use the Nios II processor together with the Arm processor in Intel SoCs to create effective multi-processor systems.

With the Nios II processor you can:

- Lower overall system cost and complexity by integrating external processors into the FPGA.
- Scale performance with multiple processors, custom instructions (hardware acceleration of a software function), or co-processor modules (hardware accelerator next to the soft processor).
- Target the Intel Agilex, Intel Stratix, Intel Arria, Intel Cyclone, or Intel MAX 10 FPGA, or the FPGA portion of the Intel Agilex, Intel Stratix 10, Intel Arria 10, Arria V, or Cyclone V SoC.
- Eliminate the risk of processor and ASSP device obsolescence.
- Take advantage of the free Nios II economy core, and the free Nios II Embedded Design Suite (EDS), to get started today.

Nios II Processor Development Flow



Nios II Processor Embedded Design Suite

The Nios II processor, the world's most versatile processor according to Gartner Research, is the most widely used soft processor in the FPGA industry. This soft processor delivers unprecedented flexibility for your cost-sensitive, real-time, safety-critical (DO-254), and applications processing needs. All Intel FPGA families support the Nios II processor.

NIOS II EDS CONTENTS
Nios II Software Build Tools for Eclipse (Nios II SBT for Eclipse) for software development · Based on Eclipse IDE · New project wizards · Software templates · Source navigator and editor
Compiler for C and C++ (GNU)
Software Debugger/Profiler
Flash Programmer
Embedded Software · Hardware Abstraction Layer (HAL) · MicroC/OS-II RTOS (full evaluation version) · Newlib ANSI-C standard library · Simple file system
Other Intel Command-Line Tools and Utilities
Design Examples

Hardware Development Tools

- Intel Quartus Prime Standard and Pro Edition Software
- Platform Designer
- Signal Tap logic analyzer plug-in for the Nios II processor
- System Console for low-level debugging of Platform Designer systems

Licensing

Getting started with the Nios II processor is now easier than ever. Not only is the Nios II EDS free, but the Nios II economy core IP is also free.

Licenses for the Nios II fast core IP are available stand-alone (IP-NIOS) or as part of the Embedded IP Suite (IPS-EMBEDDED). The Embedded IP Suite is a value bundle that contains licenses for the Nios II processor IP core, DDR1/2/3 Memory Controller IP cores, Triple-Speed Ethernet MAC IP core and 16550 - compatible UART IP core. These licenses support both Nios II Classic and Gen2 processors. These royalty-free licenses never expire and allow you to target your processor design to any Intel FPGA.

Nios II EDS: What You Get for Free!

The Nios II Embedded Design Suite (EDS) provides all the tools and software you need to develop code for the Nios II processor.
With the Nios II EDS you can:

- **Develop software with Nios II SBT for Eclipse:** Based on industry-standard Eclipse, the Nios II SBT is an integrated development environment for editing, compiling, debugging software code, and flash programming.
- **Manage board support packages (BSPs):** The Nios II EDS makes managing your BSP easier than ever. The Nios II EDS automatically adds device drivers for Intel FPGA-provided IP to your BSP, and the BSP Editor provides full control over your build options.
- **Evaluate a RTOS:** The Nios II EDS contains an evaluation version of the popular Micrium MicroC/OS-II RTOS. Product licenses can be purchased directly from Micrium.

Join the Nios II Processor Community!

Be one of many Nios II processor developers who visit the Intel FPGA Wiki, Intel FPGA Community, and the Rocketboards.org website. Intel FPGA Wiki and the Rocketboards.org website have hundreds of design examples and design tips from Nios II processor developers all over the world. Join ongoing discussions on the Nios II processor section of the Intel FPGA Community to learn more about Linux, hardware, and software development for the Nios II processor.

Visit the following websites:
community.intel.com
forums.intel.com
rocketboards.org
fpgacloud.intel.com

Development Kits

Go to page 82 for information about embedded development kits.

Nios II Processor Operating System Support

Intel and our ecosystem partners offer comprehensive operating system support for the Nios II processor.

OS	AVAILABILITY
ChibiOS/RT	Now through www.emb4fun.com
eCos	Now through www.ecoscentric.com
eCos (Zylin)	Now through www.opensource.zylin.com
embOS	Now through www.segger.com
EUROS	Now through www.euros-embedded.com
FreeRTOS	Now through www.freertos.org
Linux	Now through www.windriver.com
Linux	Now through www.rocketboards.org
oSCAN	Now through www.vector.com
TargetOS	Now through www. blunkmicro.com
ThreadX	Now through www.threadx.com
Toppers	Now through www.toppers.jp
µC/OS-II, µC/OS-III	Now through www.micrium.com
Zephyr	Now through https://www.zephyrproject.org/

SUMMARY OF SOFT PROCESSORS

CATEGORY	PROCESSOR	VENDOR	DESCRIPTION
Performance-optimized processing	Nios V microcontroller core	Intel	Based on RISC-V: RV32IA. Nios V processors give you the ultimate flexibility to achieve the exact performance required for your embedded design, without overpaying for high clock frequency, power-hungry off-the-shelf processors. Due to architectural improvements, the Nios V processor has performance benefits over the Nios II processor.
Power- and cost-optimized processing	Nios II economy core	Intel	With unique, real-time hardware features such as custom instructions, ability to use FPGA hardware to accelerate a function, vectored interrupt controller, and tightly coupled memory, as well as support for industry-leading RTOSs, the Nios II processor meets both your hard and soft real-time requirements, and offers a versatile solution for real-time processing.
Real-time processing	Nios II fast core[1]	Intel	
Applications processing	Nios II fast core	Intel	A simple configuration option adds a memory management unit to the Nios II fast processor core to support embedded Linux. Both open-source and commercially supported versions of Linux for Nios II processors are available.
Safety-critical processing	Nios II SC	HCELL	Certify your design for DO-254 compliance by using the Nios II Safety Critical core along with the DO-254 compliance design services offered by HCELL.
Lockstep Solution	Nios II Lockstep dual core	Intel	Provides high diagnostic coverage, self-checking and advanced diagnostic features in full compliance with functional safety standards IEC 61508 and ISO 26262.
Safety qualification kit (Qkit)	Nios II fast, standard and economy cores	Validas AG	Enables software designers to qualify the use of Nios II Toolchain in their safety application, fulfilling the requirements of IEC 61508 up to SIL 4 and ISO 26262 up to ASIL D.

Notes:

1. With the Nios II Gen2 product the standard core is not available as a pre-configured option, however the Gen2 fast core can be configured in the Platform Designer to have the same feature set as the standard core.
2. Starting with Nios II EDS v19.1, the Nios II EDS requires the Eclipse IDE component to be manually installed. Details on installing Eclipse IDE can be found in the Nios II Software Developer Handbook.

Getting Started

To learn more about Intel's portfolio of customizable processors and how you can get started, visit www.intel.com/niosii.

Customizable Processor Portfolio Overview

PERFORMANCE AND FEATURE SET SUMMARY OF KEY PROCESSORS SUPPORTED ON INTEL FPGAS

CATEGORY	PERFORMANCE-OPTIMIZED CORE	COST-AND POWER-SENSITIVE PROCESSORS	REAL-TIME PROCESSOR	APPLICATIONS PROCESSORS		
Features	**Nios V/m Microcontroller**	**Nios II Economy**	**Nios II Fast**	**28 nm[1] Dual-Core Arm Cortex-A9**	**20 nm[2] Dual-Core Arm Cortex-A9**	**14 nm[2] Quad-Core Arm Cortex-A53**
Maximum frequency (MHz)[3]	~ 566 MHz (Intel Agilex FPGA)[4]	400 (Stratix V)	330 (Stratix V)	925 MHz (Cyclone V SoC) 1.05 GHz (Arria V SoC)	1.5 GHz (Intel Arria 10 -1 speed grade)	1.5 GHz (Intel Stratix and Intel Agilex series)
Maximum performance (MIPS at MHz) Intel Agilex device series	268 (at 566 MHz)	–	–	–	–	–
Maximum performance (MIPS[5] at MHz) Intel Stratix series	167 (at 360 MHz)	52 (at 400 MHz)	363 (at 330 MHz)	–		–
Maximum performance (MIPS[5] at MHz) Intel Arria series	141 (at 305 MHz)	44 (at 340 MHz)	319 (at 290 MHz)	2,625 MIPS per core at 1.05 GHz	3,750 MIPS per core at 1.5 GHz	–
Maximum performance (MIPS[5] at MHz) Intel Cyclone series	–	30 (at 230 MHz)	187 (at 170 MHz)	2,313 MIPS per core at 925 MHz	–	–
Maximum performance efficiency (MIPS[5] per MHz)	0.464	0.13	1.1	2.5	2.5	2.3
16/32/64 bit instruction set support	32	32	32	16 and 32	16 and 32	16/32/64
Level 1 instruction cache	–	–	Configurable	32 KB	32 KB	32 KB
Level 1 data cache	–	–	Configurable	32 KB	32 KB	32 KB
Level 2 cache	–	–	–	512 KB	512 KB	1 MB
Memory management unit	–	–	Configurable	✓	✓	✓(+System MMU)
Floating-point unit	–	–	FPH[6]	Dual precision	Dual precision	Dual precision
Vectored interrupt controller	–	–	Optional	–	–	–
Tightly coupled memory	–	–	Configurable	–	–	–
Custom instruction interface	–	Up to 256	Up to 256	–	–	–
Equivalent ALMs	1,500	600	1,800 – 3,200	HPS	HPS	HPS

Notes:
1. 28 nm SoCs comprise Cyclone V SoCs and Arria V SoCs.
2. 20 nm SoCs comprise Intel Arria 10 SoCs.
3. Maximum performance measurements measured on Stratix V FPGAs.
4. Nios V processor Fmax is based on the highest speed grade device.
5. Dhrystone 2.1 benchmark. Note that performance will vary with system and software configuration.
6. Floating-point hardware – Nios II processor custom instructions.

Intel and Intel Partner Alliance IP Functions

www.intel.com/fpgaip

For a complete list of IP functions from Intel and Intel Partner Alliance, please visit www.intel.com/fpgaip.

	PRODUCT NAME	VENDOR NAME
DSP	**ARITHMETIC**	
	Floating Point Megafunctions	Intel
	Floating Point Arithmetic Co-Processor	Digital Core Design
	Floating Point Arithmetic Unit	Digital Core Design
	ERROR DETECTION/CORRECTION	
	Reed-Solomon Encoder/Decoder II	Intel
	Viterbi Compiler, High-Speed Parallel Decoder	Intel
	Viterbi Compiler, Low-Speed/ Hybrid Serial Decoder	Intel
	Turbo Encoder/Decoder	Intel
	High-Speed Reed Solomon Encoder/ Decoder	Intel
	BCH Encoder/Decoder	Intel
	Low-Density Parity Check Encoder/ Decoder	Intel
	Zip-Accel-C: GZIP/ZLIB/Deflate Data Compression Core	CAST, Inc.
	Zip-Accel-D: GUNZIP/ZLIP/Inflate Data Decompression Core	CAST, Inc.
	FILTERS AND TRANSFORMS	
	Fast Fourier Transform (FFT)/ Inverse FFT (IFFT)	Intel
	Cascaded Integrator Comb (CIC) Compiler	Intel
	Finite Impulse Response (FIR) Compiler II	Intel
	SHA-1	CAST, Inc.
	SHA-256	CAST, Inc.
	AES CODECs	CAST, Inc.
	MODULATION/DEMODULATION	
	Numerically Controlled Oscillator Compiler	Intel
	ATSC and Multi-Channel ATSC 8-VSB Modulators	Commsonic
	DVB-T Modulator	Commsonic
	DVB-S2 Modulator	Commsonic
	VIDEO AND IMAGE PROCESSING	
	Video and Image Processing Suite	Intel
	Stereo Vision IP Suite	Fujisoft Incorporated
	Infinivision	Gidel
	HD JPEG 2000 Encoders/Decoders	IntoPIX
	TICO Lightweight Video Compression	IntoPIX
	Multi-Channel JPEG 2000 Encoder and Decoder Cores	Silex Insight
	VC-2 High Quality Video Decoder	Silex Insight
	VC-2 High Quality Video Encoder	Silex Insight

	PRODUCT NAME	VENDOR NAME
DSP (CONTINUED)	**VIDEO AND IMAGE PROCESSING (CONTINUED)**	
	JPEG Encoders	CAST, Inc.
	Ultra-fast, 4K-compatible, AVC/ H.264 Baseline Profile Encoder	CAST, Inc.
	Low-Power AVC / H.264 Baseline Profile Encoder	CAST, Inc.
	H.265 Main Profile Video Decoder	CAST, Inc.
PROCESSORS AND PERIPHERALS	**HARD/SOFT PROCESSORS**	
	Nios II Embedded Processors	Intel
	Arm Cortex-A9 MPCore Processor in Intel SoC	Intel
	Arm Cortex-A53 MPCore Processor in Intel SoC	Intel
INTERFACE AND PROTOCOLS	**COMMUNICATION**	
	Optical Transport Network (OTN) Framers/Deframers	Intel
	SFI-5.1	Intel
	ETHERNET	
	Low-Latency 10 Gbps Ethernet Media Access Controller (MAC) with 1588	Intel
	Triple-Speed Ethernet (10/100/1000 Mbps) MAC and PHY with 1588 Option	Intel
	1 / 2.5 / 5 / 10G Multi-Rate PHY and Backplane Options	Intel
	10G Base-X (XAUI) PHY	Intel
	25G MAC and PHY with RS-FEC option	Intel
	40G Ethernet MAC and PHY with 1588 and Backplane Options	Intel
	50G MAC and PHY	Intel
	100G Ethernet MAC and PHY with 1588 and RS-FEC options	Intel
	1G/10Gb Ethernet PHY	Intel
	High-Performance Gigabit Ethernet MAC	IFI
	HIGH SPEED	
	JESD204B	Intel
	JESD204C	Intel
	Common Public Radio Interface (CPRI)	Intel
	Interlaken	Intel
	Interlaken Look-Aside	Intel
	SerialLite II/III/IV	Intel
	SATA 1.0/SATA 2.0	Intelliprop, Inc.
	RapidIO Gen3	Mobiveil
	QDR Infiniband Target Channel Adapter	Polybus

	PRODUCT NAME	VENDOR NAME
INTERFACE AND PROTOCOLS (CONTINUED)	**PCI EXPRESS / PCI**	
	PCI Express Hard-IP Controller Gen3, Gen2, Gen1 x1 x2 x4 x8 x16 Controller with SRIOV on Intel Stratix 10 GX FPGA	Intel
	PCI Express Hard-IP Controller Gen4, Gen3, Gen2, Gen1 x16 x8, x4 x2 x1 Controller with SRIOV on Intel Stratix 10 DX FPGA	Intel
	PCI Express Hard-IP Controller Gen5, Gen4,Gen3, Gen2, Gen1 x16 x8, x4 x2 x1 Controller with SRIOV on Intel Agilex FPGA	Intel
	PCI Express Memory-mapped bridge/ DMA IP on Intel Stratix 10 GX, DX, Intel Agilex FPGA	Intel
	PCI Express Gen4, Gen3, Gen2, Gen1 Scalable Switch IP with 1 UP port and up to 32 DN ports for Intel Stratix 10 and Intel Agilex FPGAs	Intel
	Multichannel DMA IP for Intel Stratix 10 GX, Intel Stratix 10 DX, and Intel Agilex FPGAs	Intel
	Expresso 3.0 PCI Express Core (Gen 1 - 4)	Rambus (Northwest Logic)
	XpressRICH3 PCI Express Gen1, Gen2, Gen3, and Gen4	PLDA
	CXL	
	XpressLINK-SOC Controller IP for CXL Gen3, Gen4, Gen5 Endpoint & Rootport for Intel Agilex devices	PLDA
	SERIAL	
	Generic QUAD SPI Controller	Intel
	Avalon® I²C (Master)	Intel
	I²C Slave to Avalon-MM Master Bridge	Intel
	Serial Peripheral Interface (SPI)/Avalon Master Bridge	Intel
	UART	Intel
	JTAG UART	Intel
	16550 UART	Intel
	JTAG/Avalon Master Bridge	Intel
	CAN 2.0/FD	CAST, Inc.
	Local Interconnect Network (LIN) Controller	CAST, Inc.
	H16550S UART	CAST, Inc.
	MD5 Message-Digest	CAST, Inc.
	Smart Card Reader	CAST, Inc.
	DI2CM I²C Bus Interface-Master	Digital Core Design
	DI2CSB I²C Bus Interface-Slave	Digital Core Design
	D16550 UART with 16-Byte FIFO	Digital Core Design
	DSPI Serial Peripheral Interface Master/ Slave	Digital Core Design
	Secure Digital (SD)/MMC SPI	El Camino GmbH
	Secure Digital I/O (SDIO)/SD Memory/ Slave Controller	Eureka Technology, Inc.
	SDIO/SD Memory/ MMC Host Controller	Eureka Technology, Inc.
	Nios II Advanced CAN	IFI
	I²C Master/Slave/PIO Controller	Microtronix, Inc.
	I²C Master and Slave	SLS

	PRODUCT NAME	VENDOR NAME
INTERFACE AND PROTOCOLS (CONTINUED)	**SERIAL (CONTINUED)**	
	USB High-Speed Function Controller	SLS
	USB Full-/Low-Speed Function Controller	SLS
	Embedded USB 3.0 / 3.1 Gen 1 Host and Device Controllers	SLS
	USB 3.0 SuperSpeed Device Controller	SLS
	AUDIO AND VIDEO	
	Character LCD	Intel
	Pixel Converter (BGR0 to BGR)	Intel
	Video Sync Generator	Intel
	SD/HD/3G-HD Serial Digital Interface (SDI)	Intel
	DisplayPort 1.1 and 1.2	Intel
	HDMI 1.4 and 2.0	Intel
	Bitec HDMI 2.0a IP core	Bitec
	DisplayPort 1.3 IP Core	Bitec
	HDCP IP Core	Bitec
	MIPI CSI-2 Controller Core	Rambus (Northwest Logic)
	MIPI DSI-2 Controller Core	Rambus (Northwest Logic)
	AC'97 Controller	SLS
MEMORIES AND MEMORY CONTROLLERS	**DMA**	
	DMA Controllers	Eureka Technology, Inc.
	Lancero Scatter-Gather DMA Engine for PCI Express	Microtronix, Inc.
	AXI DMA back-End Core	Rambus (Northwest Logic)
	Expresso DMA Bridge Core	Rambus (Northwest Logic)
	Express DMA Core	Rambus (Northwest Logic)
	FLASH	
	CompactFlash (True IDE)	Intel
	EPCS Serial Flash Controller	Intel
	Flash Memory	Intel
	NAND Flash Controller	Eureka Technology, Inc.
	Universal NVM Express Controller (UNEX)	Mobiveil, Inc.
	ONFI Controller	SLS
	Enhanced ClearNAND Controller	SLS
	SDRAM	
	DDR/DDR2 and DDR3/DDR4 SDRAM Controllers	Intel
	LPDDR2 SDRAM Controller	Intel
	RLDRAM 2 Controller	Intel
	Streaming Multi-Port SDRAM Memory Controller	Microtronix, Inc.
	HyperDrive Multi-Port DDR2 Memory Controller	Microtronix, Inc.
	Avalon Multi-Port SDRAM Memory Controller	Microtronix, Inc.
	SRAM	
	SSRAM (Cypress CY7C1380C)	Intel
	QDR II/II+/II+Xtreme/IV SRAM Controller	Intel

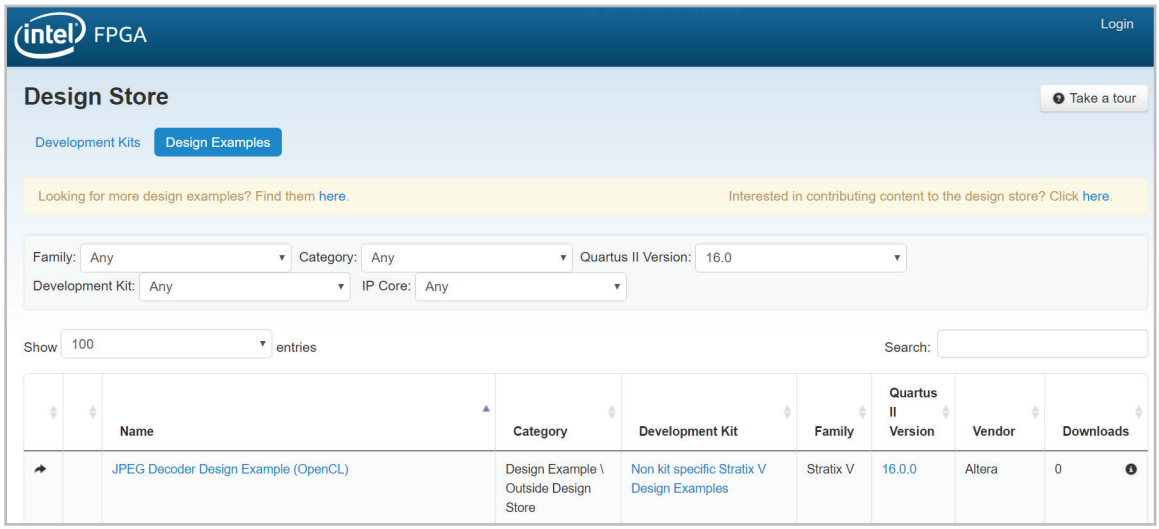
Design Store

fpgacloud.intel.com/devstore

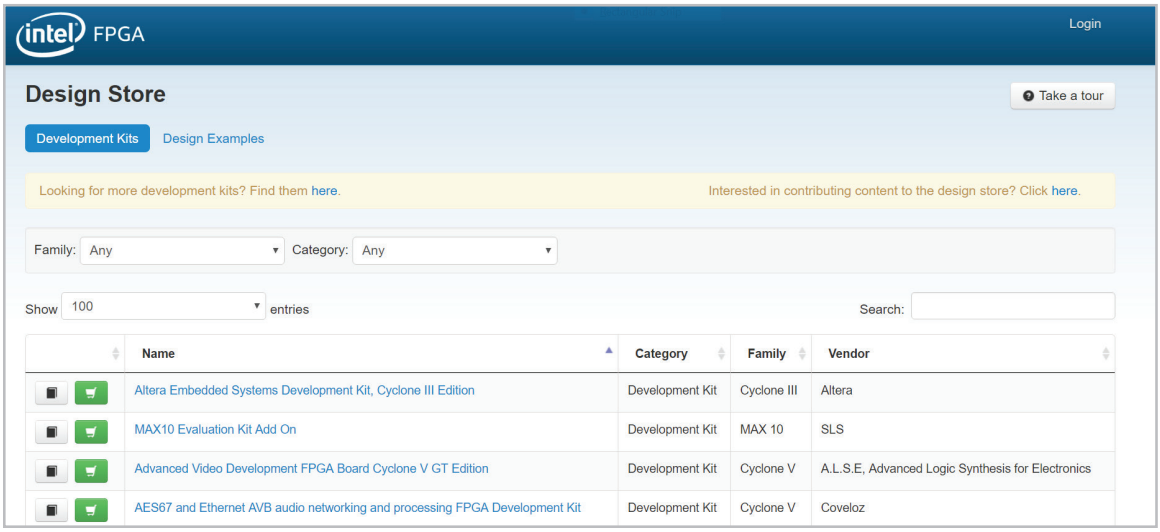
The Design Store contains Intel and partner FPGA design examples to assist you in designing with Intel FPGAs and associated development tools. Design examples are cataloged by development kit, Intel Quartus software versions, and IP for easy search. These design examples showcase a wide range of interface IP, core function IP, configuration, embedded, and end applications. New content is continuously added and updated for all product families. Adjunct sites containing Intel FPGA content such as the rocketboards.org embedded Linux site are also cataloged through the Design Store.

Check out the Design Store now: fpgacloud.intel.com/devstore

Design Example Search



Development Kit Search



Intel FPGA and Partner Development Kits

www.intel.com/fpgaboards

Intel FPGA development kits provide a complete, high-quality design environment for engineers. These kits help simplify the design process and reduce time to market. Development kits include software, reference designs, cables, and programming hardware. Intel FPGA and partner development kits are listed below. For more details about these development kits or other older development kits that are available, check out our online development kits page at www.intel.com/fpgaboards.

PRODUCT AND VENDOR NAME	DESCRIPTION
INTEL AGILEX FPGA KITS	
Intel Agilex F-Series FPGA Development Kit **Intel**	This kit allows you to design and develop your Intel Agilex F-Series FPGA design, and includes all hardware and software needed to take advantage of the performance and capabilities of the Intel Agilex F-Series FPGA with E-Tile and P-Tile. This PCIe form factor board can be used to develop and test PCI Express 4.0 designs, and external memory subsystems consisting of DDR4 and QDR IV memories. The kit also includes two QSFPDD connectors supporting both optical and electrical interfaces.
INTEL STRATIX 10 FPGA KITS	
Intel Stratix 10 GX FPGA Development Kit **Intel**	This kit provides a complete design environment including all hardware and software needed to take advantage of the performance and capabilities of the Intel Stratix 10 GX FPGA. This kit can be used to develop and test PCI Express 3.0 designs, memory subsystem consisting of DDR4, DDR3, QDR IV, and RLDRAM III memories, and develop modular and scalable designs using FPGA mezzanine card (FMC) connectors.
Intel Stratix 10 GX Transceiver Signal Integrity Development Kit **Intel**	This kit provides a complete design environment including all hardware and software needed to take advantage of the performance and capabilities of the Intel Stratix 10 GX FPGA. This kit can be used to evaluate transceiver channel performance, generate and verify pseudo-random binary sequence (PRBS), and dynamically change the channel's differential output voltage (VoD), pre-emphasis, and equalization settings.
Intel Stratix 10 SX SoC Development Kit **Intel**	The kit offers a quick and simple approach for developing custom Arm processor-based SoC designs. It offers memory options, such as HiLo DDR4 and DDR4 SODIMM. There are also two FMC+ low-pin-count connectors and two quad small form factor pluggable (QSFP) connectors for transceiver channel performance. More notably, the kit offers two HPS peripheral daughtercards to expand the capabilities.
Intel Stratix 10 TX Signal Integrity Development Kit **Intel**	This kit offers a complete design environment for developing on the Intel Stratix 10 TX FPGA. It can evaluate E-Tile transceiver channel performance up to 58 Gbps PAM4 and 30 Gbps NRZ. The board has different QSFP-DD, FMC+, MXP, and SMA connectors for networking applications. It can also be used for jitter analysis and to verify physical medium attachment (PMA) compliance for 10/25/50G/100G/200G/400G Ethernet and other major standards.
Intel Stratix 10 MX FPGA Development Kit **Intel**	This kit can be used to test and develop designs using the Intel Stratix 10 MX FPGA, which features High-Bandwidth Memory (HBM). PCIe 3.0 designs can be developed as the board contains a PCIe end point connector and a PCIe root port connector. The board also contains a DIMM socket and HiLO connector for expanded memory capability.
S10VG4 **BittWare Inc.**	This PCI Express card is based on the Intel Stratix 10 FPGA and is ideal for high-density data center applications. BittWare's Viper platform offers support for large FPGA loads, up to 32 GB of DDR4 SDRAM, and 4x100 Gbps Ethernet. The card is enabled for high-speed networking with four front panel QSFP+ cages, each supporting 40/100GbE or four 10/25GbE channels. Serial expansion is available through two UltraPort SlimSAS connectors. A 1GbE interface, a pulse-per-second (PPS) input, and a USB interface are available for debug and support. The board's flexible memory configuration includes four DIMM sites that support DDR4 SDRAM and QDR.
Nallatech 520 **Nallatech**	This is a PCI Express accelerator card based on the Intel Stratix 10 FPGA designed to address a range of compute-intensive and latency-critical applications including machine learning, gene sequencing, oil and gas, and real-time network analytics. This introduces the ground-breaking single precision floating-point performance of up to 10 TFLOPS per device.

PRODUCT AND VENDOR NAME	DESCRIPTION
INTEL MAX 10 FPGA KITS	
Intel MAX 10 FPGA Nios II Embedded Evaluation Kit (NEEK) **Terasic**	This kit is a full featured embedded evaluation kit based on the Intel MAX 10 device family. The kit delivers an integrated platform that includes hardware, design tools, IP, and reference designs for developing a wide range of applications. This kit allows developers to rapidly customize their processor and IP to suit their specific needs, rather than constraining their software around the fixed feature set of the processor. The kit features a capacitive LCD multimedia color touch panel, which natively supports multi-touch gestures. An eight megapixel digital image sensor, ambient light sensor, and three-axis accelerometer make up this rich feature set, along with a variety of interfaces connecting the kit to the outside for Internet of Things (IoT) applications across markets.
Intel MAX 10 FPGA Development Kit **Intel**	This kit offers a comprehensive general-purpose development platform for many markets and applications, such as industrial and automotive. This fully featured development kit includes a 10M50DAF484C6G device, DDR3 memory, 2X 1 GbE, high-speed mezzanine card (HSMC) connector, quad serial peripheral interface, 16 bit digital-to-analog converter (DAC), flash memory, and 2X Digilent Pmod Compatible headers.
Intel MAX 10 FPGA Evaluation Kit **Intel**	The 10M08 evaluation board provides a cost-effective entry point to Intel MAX 10 FPGA design. The card comes complete with an Arduino header socket, which lets you connect a wide variety of daughtercards. Other features include an Intel MAX 10 10M08SAE144C8G device, Arduino shield expansion, access to 80 I/O through-holes, and a prototyping area.
DECA Intel MAX 10 FPGA Evaluation Kit **Arrow**	DECA is a full-featured evaluation kit featuring a 10M50DAF484C6G device. The kit includes a BeagleBone-compatible header for further I/O expansion, a variety of sensors (gesture/humidity/ temperature/CMOS), MIPI CSI-2 camera interface, LEDs, pushbuttons, and an on-board Intel FPGA Download Cable II.
Mpression Odyssey Intel MAX 10 FPGA IoT Evaluation Kit **Macnica**	The Macnica Intel MAX 10 FPGA evaluation kit connects and controls your FPGA design via Bluetooth using the Mpression Odyssey Smartphone application. This kit also includes a10M08U169C8G device, SDRAM, Arduino shield expansion capability, and Bluetooth SMART connectivity module.
STRATIX V FPGA KITS	
Stratix V Advanced Systems Development Kit **Intel**	This kit is a complete systems design environment that includes both the hardware and software needed to begin architecture development and system design using Stratix V FPGAs. The PCI Express-based form factor utilizes a x16 edge connector, and includes high memory bandwidth to DDR3, QDR II+, and serial memory. Multiple high-speed protocols are accessible through FMC and HSMC connections. A one year license for the Intel Quartus Prime Software is available with this kit.
Stratix V GX FPGA Development Kit **Intel**	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix V GX FPGA. This kit includes the PCI Express x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, and SDI interfaces. Memory includes one x72 DDR3 SDRAM, one RLDRAM II x18 QDR II+ SRAM, and flash memory. This kit also includes two SMA connectors for a differential transceiver output. Several programmable oscillators are available and other user interfaces include three user pushbuttons, one 8-position DIP switch, 16 user LEDs, an LCD display, and power and temperature measurement circuitry.
Transceiver Signal Integrity Development Kit, Stratix V GX Edition **Intel**	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include seven full-duplex transceiver channels with SMA connectors, two 14G backplane connectors (from Amphenol and Molex), four programmable clock oscillators, four user pushbuttons, one 8-position DIP switch, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, an embedded Intel FPGA Download Cable, and JTAG interfaces.
Transceiver Signal Integrity Development Kit, Stratix V GT Edition **Intel**	The Stratix V GT Transceiver Signal Integrity Development Kit provides a platform for electrical compliance testing and interoperability analysis. The accessibility to multiple channels allows for real-world analysis as implemented in the system with transceiver channels available through SMA and popular backplane connectors. This development kit can be used for evaluation of transceiver link performance up to 25.7 Gbps, generation and checking pseudo-random binary sequence (PRBS) patterns via an easy-to-use GUI that does not require the Intel Quartus Prime Software, access advanced equalization to fine-tune link settings for optimal bit error ratio (BER), jitter analysis, and verifying physical media attachment (PMA) interoperability with Stratix V GT FPGAs for targeted protocols, such as CEI-25/28G, CEI-11G, PCI Express Gen 3.0, 10GBASE-KR, 10 Gigabit Ethernet, XAUI, CEI-6G, Serial RapidIO, HD-SDI, and others. You can use the built-in high speed backplane connectors to evaluate custom backplane performance and evaluate link BER.
100G Development Kit, Stratix V GX Edition **Intel**	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through one x18 QDR II and six x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 12.5 Gbps, and verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCI Express (Gen1, Gen2, and Gen3), and other major standards. This kit can also validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP.
DSP Development Kit, Stratix V Edition **Intel**	The DSP Development Kit, Stratix V Edition provides a complete design environment that includes all the hardware and software you need to begin developing DSP intensive FPGA designs immediately. The development kit is RoHS-compliant. You can use this development kit to develop and test PCI Express designs at data rates up to Gen3, develop and test memory subsystems for DDR3 SDRAM or QDR II SRAM memories, and use the HSMC connectors to interface to one of over 35 different HSMCs provided by Intel partners, supporting protocols such as Serial RapidIO, 10 Gbps Ethernet, SONET, CPRI, OBSAI, and others.

PRODUCT AND VENDOR NAME	DESCRIPTION
INTEL ARRIA 10 FPGA KITS	
Intel Arria 10 FPGA Development Kit **Intel**	This kit provides a complete design environment including hardware and software for prototyping and testing high-speed serial interfaces to an Intel Arria 10 GX FPGA. This kit includes the PCI Express x8 form factor, two FMC connectors for expandability, Ethernet, USB, and SDIs. The board includes one HiLo connector for plugging in DRAM and SRAM daughtercards. Supported daughtercard formats include DDR4 x72 SDRAM, DDR3 x72 SDRAM, RLDRAM 3 x36, and QDR IV x36 SRAM. The board includes SMA connectors for transceiver output, clock output, and clock input. Several programmable oscillators are available and other user interfaces include user push buttons, dual in-line package (DIP) switches, bi-color user LEDs, an LCD display, power, and temperature measurement circuitry. This development kit comes with a one-year license for the Intel Quartus Prime Software.
Intel Arria 10 FPGA Signal Integrity Kit **Intel**	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include six full-duplex transceiver channels with 2.4 mm SMA connectors, four full-duplex transceiver channels to Amphenol Xcede+ backplane connector, four full-duplex transceiver channels to C form factor pluggable (CFP2) optical interface, four full-duplex transceiver channel to QSFP+ optical interface, one transceiver channel to SFP+ optical interface, and ten full-duplex transceiver channels to Samtec BullsEye high-density connector. This board also includes several programmable clock oscillators, user pushbuttons, DIP switches, user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, Ethernet, an embedded Intel FPGA Download Cable II, and JTAG interfaces. This development kit comes with a one-year license for the Intel Quartus Prime Software.
Intel Arria 10 SoC Development Kit **Intel**	This kit offers a quick and simple approach for developing custom Arm processor-based SoC designs. The Intel Arria 10 SoCs offers full software compatibility with previous generation SoCs, a broad ecosystem of Arm software and tools, and an enhanced FPGA and DSP hardware design flow. This kit includes an Intel Arria 10 10AS066N3F40I2SG SoC, PCI Express Gen3 protocol support, a dual FMC expansion headers, two 10/100/1000 SGMII Ethernet ports, one 10/100/1000 RGMII Ethernet port, two 10GbE small form factor pluggable (SFP) cages, two 1GB DDR4 HPS HiLo memory card, DDR4 SDRAM, NAND, quad SPI, SD/MICRO boot flash cards, character LCD, display port, and SDI port.
Attila Instant-Development Kit Intel Arria 10 FPGA FMC IDK **REFLEX**	This kit provides out-of-the-box experience, combining compact hardware platform and an efficient intuitive software environment. This kit is designed for high-performance serial transceiver applications using Intel Arria 10 GX 1150 KLEs. Hardware, software design tools, IP, and pre-verified reference designs included. Its unique installation and GUI allows an immediate start, and its reference designs enable fast turn-around designs, shortening and securing the developments.
Alaric Instant-Development Kit Intel Arria 10 SoC FMC IDK **REFLEX**	This kit provides out-of-the-box experience, combining compact hardware platform and an efficient intuitive software environment. This kit is designed for high-performance serial transceiver applications using an Intel Arria 10 SoC with 660 KLEs and an Arm dual-core Cortex-A9 MPCore. Its unique installation and GUI allows an immediate start, and its reference designs enable fast turn-around designs, shortening and securing the developments.
Nallatech 510T **Nallatech**	Nallatech 510T is an FPGA co-processor that is designed to deliver ultimate performance per watt for compute-intensive data center applications. The 510T is a GPU-sized 16-lane PCI Express Gen3 card featuring two of Intel's new floating-point enabled Intel Arria 10 FPGAs delivering up to 16 times the performance of the previous generation†. Applications can achieve a total sustained performance of up to 3 TFLOPS.
INTEL CYCLONE 10 FPGA KITS	
Intel Cyclone 10 LP Evaluation Kit **Intel**	This kit provides an easy-to-use platform for evaluating Intel Cyclone 10 LP FPGA technology and Intel Enpirion regulators. This evaluation board enables you to develop designs for Intel Cyclone 10 LP FPGAs via Arduino UNO R3 shields, Digilent Pmod Compatible cards, GPIOs, or Ethernet connector. This kit also measures key Intel Cyclone 10 LP FPGA power supplies and reuse the kit's PCB schematic as a model for your design.
Intel Cyclone 10 GX FPGA Development Kit **Intel**	This kit is an ideal starting point for developing applications, such as embedded vision, factory automation, and surveillance. With this development kit, you can develop Intel Cyclone 10 GX FPGA-based designs with expansion through PCIe Gen2, USB 3.1, SFP+, and RJ-45.

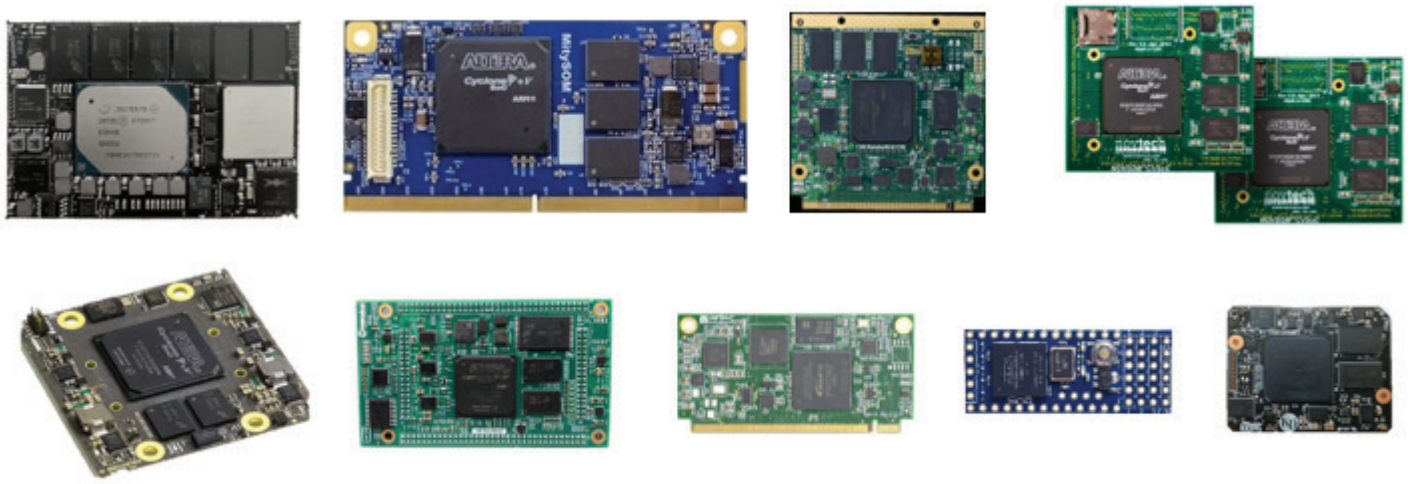
PRODUCT AND VENDOR NAME	DESCRIPTION
ARRIA V FPGA AND SoC KITS	
Arria V GX Starter Kit, Arria V GX Edition **Intel**	This kit provides a low-cost platform for developing transceiver I/O-based Arria V GX FPGA designs. This kit includes the PCI Express x8 form factor, one HSMC connector, a 32 bit DDR3 SDRAM device, one-channel high-speed transceiver input and output connected to SMAs, HDMI output, SDI input and output, 16x2 LCD display, and flash memory.
Arria V SoC Development Kit and SoC Embedded Design Suite **Intel**	The Arria V SoC Development Kit offers a quick and simple approach to develop custom Arm processor-based SoC designs. Intel's midrange, transceiver-based Arria V FPGA fabric provides the highest bandwidth with the lowest total power for midrange applications such as remote radio units, 10G/40G line cards, medical imaging, broadcast studio equipment, and the acceleration of image- and video-processing applications. This development kit includes the SoC Embedded Design Suite software development tools. The development board has PCI Express Gen2 x4 lanes (endpoint or rootport), two FMC expansion headers, dual Ethernet PHYs, and various DRAM and flash memories.
CYCLONE V FPGA AND SoC KITS	
Cyclone V E FPGA Development Kits **Intel**	The Cyclone V E Development Kit offers a comprehensive general-purpose development platform for many markets and applications, including industrial, networking, military, and medical applications. The kit features an Intel Cyclone V device and a multitude of onboard resources including multiple banks of DDR3 and LPDDR2 memory, LCD character display, LEDs, user switches, USB, and RJ-45 connectors. The Cyclone V E FPGA Development Kit gives industrial equipment designers greater flexibility in implementing real-time Ethernet communications with industrial Ethernet IP cores.
Cyclone V GT FPGA Development Kit **Intel**	This kit can be used to prototype Cyclone V GT FPGA or Cyclone V GX FPGA applications. It offers a quick and simple way to develop low-cost and low-power system-level designs and achieve rapid results. This kit supports a myriad of functionalities, such as FPGA prototyping, FPGA power measurement, transceiver I/O performance up to 5 Gbps, PCI Express Gen2 x4 (at 5 Gbps per lane), endpoint or rootport support.
Cyclone V SoC Development Kit **Intel**	The Cyclone V SoC Development Kit offers a quick and simple approach to develop custom Arm processor-based SoC designs accompanied by Intel's low-power, low-cost Cyclone V FPGA fabric. This kit supports a wide range of functions, such as processor and FPGA prototyping and power measurement, industrial networking protocols, motor control applications, acceleration of image- and video-processing applications, PCI Express x4 lane with ~1,000 MBps transfer rate (endpoint or rootport).
Cyclone V GX Starter Kit **Terasic Technologies**	The Cyclone V GX Starter Kit offers a robust hardware design platform based on Cyclone V GX FPGA. This kit is optimized for the lowest cost and power requirement for transceiver applications with industry-leading programmable logic for ultimate design flexibility. The Cyclone V Starter Kit development board includes hardware, such as Arduino Header, on-board Intel FPGA Download Cable circuit, audio and video capabilities, and an on-board HSMC connector with high-speed transceivers that allows for an even greater array of hardware setups.
DE0-Nano-SoC Kit **Terasic Technologies**	The DE0-Nano-SoC Kit combines a robust, Cyclone V SoC-based development board and interative reference designs into a powerful development platform. This low-cost kit is an interactive, web-based guided tour that lets you quickly learn the basics of SoC development and provides an excellent platform on which to develop your own design. The board includes a Gigabit Ethernet port, USB 2.0 OTG port, SD card flash, 1 GB DDR3 SDRAM, an Arduino header, two 40-pin expansion headers, on-board Intel FPGA Download Cable circuit, 8-channel A/D converter, accelerometer, and much more.
MAX V CPLD KITS	
MAX V CPLD Development Kit **Intel**	This low-cost platform will help you quickly begin developing low-cost, low-power CPLD designs. Use this kit as a stand-alone board or combined with a wide variety of daughtercards that are available from third parties. With this platform, you can develop designs for the 5M570Z CPLD and build upon example designs provided.
STRATIX IV FPGA KITS	
100G Development Kit, Stratix IV GT Edition **Intel**	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCI Express (Gen1, Gen2, and Gen3), and other major standards. This kit can also validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP.

PRODUCT AND VENDOR NAME	DESCRIPTION
CYCLONE IV FPGA KITS	
Cyclone IV GX FPGA Development Kit **Intel**	This kit provides a comprehensive design environment that allows you to quickly develop low-cost and low-power FPGA system-level designs. This kit includes the PCI Express short card form factor, two HSMC connectors, and a 10/100/1000 Mbps Ethernet interface. Onboard memory includes 128 MB DDR2 SDRAM, 64 MB flash, and 4 MB SSRAM. This kit also includes SMA connectors, and 50 MHz, 100 MHz, and 125 MHz clock oscillators, as well as user interfaces including pushbuttons, LEDs, and a 7-segment LCD display.
DEO-Nano Development Board **Terasic Technologies**	The DE0-Nano Development Board is a compact-sized FPGA development platform suited for prototyping circuit designs such as robots and "portable" projects. The board is designed to be used in the simplest possible implementation targeting the Cyclone IV device up to 22,320 LEs. This kit allows you to extend designs beyond the DE0-Nano board with two external general-purpose I/O (GPIO) headers and allows you to handle larger data storage and frame buffering with on-board memory devices including SDRAM and EEPROM. This kit is lightweight, reconfigurable, and suitable for mobile designs without excessive hardware. This kit provides enhanced user peripheral with LEDs and push buttons and three power scheme options including a USB Mini-AB port, 2-pin external power header, and two DC 5-V pins.
Industrial Networking Kit **Terasic Technologies**	The Industrial Networking Kit (INK) offers a comprehensive development platform for industrial automation and applications. The kit consists of the DE2-115 board featuring the Cyclone IV device and dual 10/100/1000-Mbps Ethernet, 128 MB SDRAM, 8 MB flash memory, 2 MB SRAM, HSMC and GPIO connectors, USB 2.0, an SD card slot, switches and buttons, LEDs, 16x2 display, audio and video, and VGA-out. The kit also includes an Industrial Communications Board (ICB-HSMC) that supports RS-485, RS-232, CAN, and additional I/O expansion.
DE2-115 Development and Education Board **Terasic Technologies**	This board is part of the DE2 educational development board series and features the Cyclone IV E EP4CE115 FPGA. The DE2-115 offers an optimal balance of low cost, low power, and a rich supply of logic, memory and DSP capabilities, as well as interfaces to support mainstream protocols including GbE. A HSMC connector is provided to support additional functionality and connectivity via HSMC daughtercards and cables.
MAX II CPLD Kits	
MAX II/MAX IIZ Development Kit **System Level Solutions**	This board provides a hardware platform for designing and developing simple and low-end systems based on MAX II or MAX IIZ devices. The board features a MAX II or MAX IIZ EPM240T100Cx or EPM240ZM100Cx device with 240 LEs and 8,192 bits of user flash memory (UFM). The board also supports vertical migration into EPM570T100Cx devices with 570 LEs and 8,192 bits of UFM.

Intel FPGA-Based SoM Partner Ecosystem

www.intel.com/fpgasoms

System on modules (SoMs) provide a compact, pre-configured solution with FPGA, memory, and software which is perfect for prototyping, proof-of-concept, and initial system development and production. SoMs enable you to focus on development of your IP, algorithms, and human/mechanical interfaces rather than spending time on the fundamentals of the processor and electrical system and software bring-up. In many cases, SoMs can also make sense for full system production.



Customer Benefits

- Faster time to market by off-loading complex board design
- Production-ready hardware for immediate deployment
- Versatile product design and application fit from various partners
- Minimize component supplier management

Target Application

- General embedded applications
- Industrial PC, factory automation, and control applications
- Machine vision, surveillance camera, and retail applications
- Networking and security applications
- Test and measurement equipment

The following Intel SoC-based SoMs are available now from Intel FPGA partners:

Partner	Partner Tier	SoM Product Name	Intel Device	Processor	FPGA Logic Elements	Target Application	Size (mm)
Exor International	Titanium	microSOM us02	Cyclone® V SoC (SE)	Dual-core Arm Cortex-A9 MPCore processor	25K/110K LEs	Industrial, 5G, AI	48x35
		GigaSOM gS01	Intel® Cyclone® 10 GX + Intel Atom® E39xx	Intel Atom x5-E3930 / x5-E3940 / x7-E3950	220K LEs		
Mantaro / HITEK systems	Ttianium	Agilex HPC SOM	Intel® Agilex™	Quad-core 64-bit Arm Cortex-A53	1,437K LEs	HPC	174x138
Reflex CES	Titanium	COMXpress Stratix® 10 SoC	Intel® Stratix® 10 SX	Quad-core 64-bit Arm Cortex-A53	2,753K LEs	HPC, Video & Vision	125x95
		Achilles Arria® 10 SoM	Intel® Arria® 10 SoC	Dual-core Arm Cortex-A9 MPCore processor	270K/660K LEs	Industrial, Video & Vision, Radar Systems	85x95
Terasic	Titanium	Apollo Agilex SoM	Intel Agilex	Quad-core 64-bit Arm Cortex-A53	1,437K LEs	AI Edge, HPC	145x133
		Apollo S10 SoM	Intel Stratix 10 SX	Quad-core 64-bit Arm Cortex-A53	2,753K LEs	General purpose	151x185
Alorium Technology	Gold	Sno	Intel® MAX® 10		16K LEs	MCU replace	18x43
		Evo M51	Intel MAX 10	Atmel SAMD51 32-bit Arm Cortex-M4 processor	25K LEs	Motor Control	23x56

Partner	Partner Tier	SoM Product Name	Intel Device	Processor	FPGA Logic Elements	Target Application	Size (mm)
Critical Link	Gold	MitySOM-A10S	Intel Arria 10 SoC	Dual-core Arm Cortex-A9 MPCore processor	270K LEs	General purpose	82x39
		MitySOM-5CSX	Cyclone V SoC (SX)		Up to 110K LEs		
Enclustra	Gold	Mercury+ AA1	Intel Arria 10 SoC	Dual-core Arm Cortex-A9 MPCore processor	270K/480K LEs	Industrial	TBD
		Mercury SA1	Cyclone V SoC (SX)		110K LEs		56x54
		Mercury+ SA2	Cyclone V SoC (ST)		110K LEs		74x54
		Mercury CA1	Cyclone® IV		75K/115K LEs	General purpose	56x54
GEB Enterprise	Gold	PICO SOM CARD MAX10	Intel MAX 10		Up to 50K LEs	Industrial	TBD
iWave System Technologies	Gold	iW-Rainbow-G24M	Intel Arria 10 SoC / GX	Dual-core Arm Cortex-A9 MPCore processor	660K LEs / 1150K LEs	ASIC proto, General Purpose	95x75
		iW-RainboW-G17M	Cyclone V SoC (SX)		Up to 110K LEs		70x70
Kondo Electronics	Gold	KEIm-08	Intel MAX 10		8K LEs	MCU replacement	70x35
		KEIm-25	Intel MAX 10		25K LEs	General purpose	
		KEIm-CVSoC	Cyclone V SoC (SX)	Dual-core Arm Cortex-A9 MPCore processor	85K LEs	Video & Vision, AI, Industrial	
MRA Digital	Gold	C5SOC-SOM-PROCESSOR	Cyclone V SoC (SX)	Dual-core Arm Cortex-A9 MPCore processor	110K LEs	Video & Vision, Industrial	66x56
NDR	Gold	N-EMB-100/110	Cyclone V SoC (SX)	Dual-core Arm Cortex-A9 MPCore processor	110K LEs	Industrial networking	TBD
		N-EMB-120	Intel MAX 10		50K LEs	Industrial networking	TBD
Novtech	Gold	NOVSOM CVL	Cyclone V SoC (SE)	Dual-core Arm Cortex-A9 MPCore processor	Up to 110K LEs	General purpose	68x35
		NOVSOM CV	Cyclone V SoC (SE, SX, ST)		Up to 110K LEs		73x64
Aries	Member	MAX	Intel Arria 10 SoC	Dual-core Arm Cortex-A9 MPCore processor	480K/660K LEs	General purpose	60x110
		MCXL	Intel Cyclone 10 LP		16K/40K/ 55K LEs		37x90
		MCV	Cyclone V SoC (SE, SX)	Dual-core Arm Cortex-A9 MPCore processor	25K/40K/85K/ 110K LEs		74x42
		MX10	Intel MAX 10		4K/8K/16K/ 50KLE		70x35
		SpiderSOM	Intel MAX 10		2K/8K LEs		70x35
Macnica	Distributor	Borax SOM	Cyclone V SoC (SE)	Dual-core Arm Cortex-A9 MPCore processor	Up to 110K LEs	General purpose	95x55

Intel Partner Alliance

www.intel.com/partneralliance

The Intel® Partner Alliance is a program designed to enhance the value, relevance and the experience we deliver to our partners. The unification of former Intel partner programs such as the Design Solutions Network and the FPGA Partner Program, to name a few, will allow Intel and its partners to continue driving the industry to innovate solutions with powerful technology. These investments will help enable disruption and accelerate new market opportunities in an increasingly data-centric world. From leading edge technologies to sophisticated sales enablement and powerful partner networking, the Intel Partner Alliance will connect partners to a world of innovation.

Visit the Intel® Solutions Marketplace to connect with thousands of partners, opening the door to matchmaking opportunities to grow your business and innovate. Access the vast catalog of Intel Solutions Marketplace offerings and Partner Directory – the fastest way to find products, solutions, and Intel Partner Alliance partners that meet your business needs.

Learn more and join the Intel Partner Alliance today.

Training Overview

www.intel.com/fpgatraining

We offer an extensive curriculum of classes to deepen your expertise. Our classes are beneficial whether you're new to FPGA, CPLD, and SoC design, or are an advanced user wanting an update on the latest tools, tips, and tricks. Our training paths are delivered in four ways:

ONLINE AND SELF-PACED TRAINING	INSTRUCTOR-LED VIRTUAL / ONLINE CLASSROOM	ON-SITE INSTRUCTOR-LED TRAINING	QUICK VIDEO
Pre-recorded presentations and demonstrations, generally 30 minutes long. Online classes are free and available at any time, from any computer with Internet access with non-restrictive firewall. You can find some of these online training courses on the Intel FPGA Technical Training YouTube Channel.	Instructor-taught training supplemented with hands-on exercises. Taught virtually using a WebEx connection and Internet access with non-restrictive firewall. Allows you to benefit from the interactivity with an instructor from the comfort of your home or office. Classes are taught in 4.5-hour sessions across consecutive days.	In-person instruction with hands-on lab exercises, typically lasting one or more days. Labs are conducted on development boards either onsite or via remote connection through Webex. Classes are conducted by an Intel or Intel partner subject matter expert. Fees vary.	These short how-to YouTube videos teach specific skills and help solve your issues. Refer to the Engineer-to-engineer YouTube Channel.

Learn more about our training program or sign up for classes at www.intel.com/fpgatraining. Start sharpening your competitive edge today!

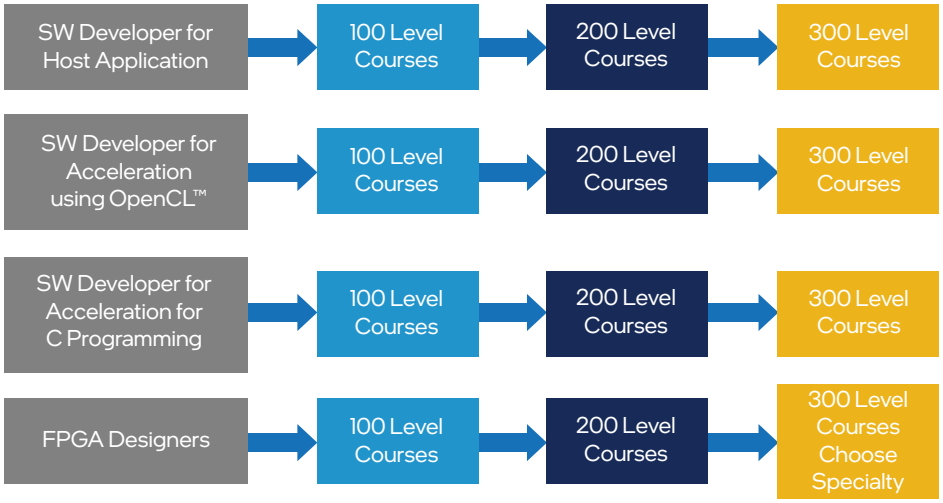
To help you decide which courses might be most useful to you, we've grouped classes into specific curricula levels. Select the persona that your work most closely aligns with to view your recommended training curriculum:

- Software Developer for Host Application
- Software Developer for Acceleration using OpenCL Standard
- Software Developer for C Programming
- FPGA Designer: What's New – Intel Agilex FPGAs

The courses are categorized into levels to help you select the best course that aligns with your existing knowledge and your training goals.

The training material is broken up into the following three levels:

- 100 level courses are introductory courses that offer a high-level overview on a topic.
- 200 level courses expect a basic understandings of material covered in the 100 level courses and provides the next level of instruction.
- 300 level courses are more technically advanced and/or are specific to an area of expertise.



Training

www.intel.com/fpgatraining

Instructor-Led and Virtual Classes

VIRTUAL CLASSROOM COURSES DENOTED WITH A■
(ALL COURSES ARE ONE DAY IN LENGTH UNLESS OTHERWISE NOTED)

Note: To view the course details, click on the course titles.

COURSE CATEGORY	GENERAL DESCRIPTION	COURSE TITLES
High-Level Design	Accelerate algorithm performance with Open Computing Language (OpenCL) by offloading to an FPGA.	• Introduction to OpenCL Programs for Intel FPGA■ • Optimizing OpenCL Programs for Intel FPGAs■ • Introduction to High-Level Synthesis with Intel FPGAs■ • High-Level Synthesis Advanced Optimization Techniques■
Design Languages	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic.	• Introduction to VHDL■ • Advanced VHDL Design Techniques■ • Introduction to Verilog HDL■ • Advanced Verilog HDL Design Techniques■
Intel Quartus Prime Software	Acquire design entry, compilation, programming, verification, and optimization skills by learning how to use both basic and advanced features of the Intel Quartus Prime Software.	• The Intel Quartus Prime Software: Foundation■ • The Intel Quartus Prime Software: Foundation for Xilinx Vivado Design Suite Users■ • Intel Quartus Prime Software Debug Tools■ • Intel Quartus Prime Pro Software Timing Analysis■ • Timing Closure with the Quartus II Software■ • Partial Reconfiguration with Intel FPGAs■
Design Optimization Techniques	Learn design techniques and Intel Quartus Prime Software features to improve design performance. Note: While the focus of this course is the Intel Stratix 10 device family, many of the techniques you will learn can be used to improve performance in other device architectures.	• Performance Optimization with Intel Stratix 10 FPGA Hyperflex Architecture■ • Advanced Optimization with Intel Stratix 10 FPGA Hyperflex Architecture■ • The Intel Hyperflex FPGA Optimization Workshop■
System Integration	Build hierarchical systems by integrating IP and custom logic.	• Introduction to the Platform Designer System Integration Tool■
Embedded System Design	Learn to design an Arm-based processor system in an Intel FPGA	• Using Intel SoC FPGAs■ • Using Intel Stratix 10 and Agilex SoC FPGAs■
System Design	Solve DSP and video system design challenges using Intel technology.	• Designing with DSP Builder for Intel FPGAs■
Connectivity Design	Build high-speed, gigabit interfaces using embedded transceivers found in leading-edge FPGA families.	• Building Interfaces with Arria 10 High-Speed Transceivers■

Online Training

FREE ONLINE TRAINING COURSES (COURSES ARE APPROXIMATELY 30 MINUTES LONG)

COURSE CATEGORY	COURSE TITLES	LANGUAGES
Getting Started	Read Me First!	English, Chinese, and Japanese
	Basics of Programmable Logic: FPGA Architecture	English, Chinese, and Japanese
	Basics of Programmable Logic: History of Digital Logic Design	English, Chinese, and Japanese
	How to Begin a Simple FPGA Design	English, Chinese, and Japanese
	University Self-Guided Lab: Become an FPGA Designer in 4 Hours	English only
	FPGA Business Fundamentals	English and Japanese
Acceleration	Introduction to the Acceleration Stack for Intel Xeon CPU with FPGAs	English, Chinese, and Japanese
	Introduction to Intel FPGAs for Software Developers	English only
	Performance Tuning Architectures with the Intel FPGA Deep Learning Acceleration Suite	English only
	OpenCL Development with the Acceleration Stack for Intel Xeon CPU with FPGA	English, Chinese, and Japanese
	Building RTL Workloads for the Acceleration Stack for Intel Xeon CPU with FPGAs	English, Chinese, and Japanese
	Application Development on the Acceleration Stack for Intel Xeon CPU with FPGAs	English, Chinese, and Japanese
	Introduction to Apache Hadoop	English only
	Introduction to Apache Spark	English only
	Introduction to Kafka	English only
	Introduction to High Performance Computing (HPC)	English and Japanese
	Intel Programmable Acceleration Card (PAC) Getting Started	English and Japanese
	Building an Accelerator Functional Unit for the Intel FPGA Programmable Acceleration Card N3000	English only
	Introduction to Intel FPGA Programmable Acceleration Card N3000	English only
	Getting Started with the Intel FPGA Programmable Acceleration Card N3000	English only
	Intel FPGA Programmable Acceleration Card N3000 Board Management Controller	English only
	Intel FPGA Programmable Acceleration Card N3000 Security	English only
	Open Programmable Acceleration Engine (OPAE) In Depth	English only
Deep Learning	Getting Started with the Intel Distribution of OpenVINO™ toolkit with FPGAs	English only
	Introduction to Deep Learning	English only
	Programmers' Introduction to the Intel FPGA Deep Learning Acceleration Suite	English, Japanese and Chinese
	Deploying Intel FPGAs for Deep Learning Inferencing with OpenVINO Toolkit	English only
OpenCL	Introduction to Parallel Computing with OpenCL Programs on FPGAs	English, Japanese, and Chinese
	Writing OpenCL Programs for Intel FPGAs	English, Japanese, and Chinese
	Running OpenCL Programs on Intel FPGAs	English, Japanese, and Chinese
	Using Channels and Pipes with OpenCL on Intel FPGAs	English only
	OpenCL: Single-Threaded versus Multi-Threaded Kernels	English and Japanese
	OpenCL Optimization Techniques: Image Processing Algorithm Example	English only
	OpenCL Optimization Techniques: Secure Hash Algorithm Example	English only
	Memory Optimization for OpenCL on Intel FPGAs	English only
	OpenCL Coding Optimizations for Intel Stratix 10 Devices	English only
	Building Custom Platforms for Intel FPGA SDK for OpenCL: BSP Basics	English only
	Building Custom Platforms for Intel FPGA SDK for OpenCL: Modifying a Reference Platform	English only

FREE ONLINE TRAINING COURSES (COURSES ARE APPROXIMATELY ONE HOUR LONG)

COURSE CATEGORY	COURSE TITLES	LANGUAGES
High-Level Synthesis	Introduction to High-Level Synthesis (Part 1 of 7)	English and Japanese
	HLS Interfaces (Part 2 of 7)	English only
	HLS Loop Optimizations (Part 3 of 7)	English only
	HLS Data Types (Part 4 of 7)	English only
	HLS Local Memory Optimizations (Part 5 of 7)	English only
	HLS Performance Optimization (Part 6 of 7)	English only
	HLS Optimization Example: Matrix Decomposition (Part 7 of 7)	English only
	HLS Coding Optimizations for Intel Stratix 10 Devices	English only
Design Languages	VHDL Basics	English, Chinese, and Japanese
	Verilog HDL Basics	English, Chinese, and Japanese
	SystemVerilog with the Intel Quartus Software	English and Chinese
	Best HDL Design Practices for Timing Closure	English
Software Overview and Design Entry	Intel Quartus Prime Tools Ask an Expert	English only
	Using the Intel Quartus Prime Standard Edition Software: An Introduction	English and Chinese
	The Intel Quartus Prime Software: Foundation (Pro Edition)	English and Chinese
	The Intel Quartus Prime Software: Foundation (Standard Edition)	English only
	Using the Intel Quartus Prime Pro Edition Synthesis Engine	English and Japanese
	Introduction to Incremental Compilation in the Intel Quartus Prime Standard Edition Software	English and Chinese
	Incremental Block-Based Compilation in the Intel Quartus Prime Pro Software: Design Partitioning	English and Japanese
	Incremental Block-Based Compilation in the Intel Quartus Prime Pro Software: Introduction	English and Japanese
	Incremental Block-Based Compilation in the Intel Quartus Prime Pro Software: Timing Closure & Tips	English and Japanese
	Design Block Reuse in the Intel Quartus Prime Pro Software	English only
	Fast & Easy I/O System Design with Interface Planner	English and Chinese
	SERDES Channel Simulation with IBIS-AMI Models	English and Japanese
	Partial Reconfiguration for Intel FPGA Devices: Introduction & Project Assignments	English only
	Partial Reconfiguration for Intel FPGA Devices: Design Guidelines & Host Requirements	English only
	Partial Reconfiguration for Intel FPGA Devices: PR Host IP & Implementations	English only
	Partial Reconfiguration for Intel FPGA Devices: Output Files & Demonstration	English only
Verification and Debugging	Debugging with Signal Tap for Intel FPGAs Office Hours	English only
	Signal Tap Logic Analyzer: Introduction & Getting Started	English and Chinese
	SignalTap II Logic Analyzer: Triggering Options, Compilation, & Device Programming	English only
	SignalTap II Logic Analyzer: Data Acquisition & Additional Features	English only
	SignalTap Logic Analyzer: Basic Configuration & Trigger Conditions	English only
	Using Intel Quartus Prime Pro Software: Chip Planner	English and Japanese
	System Console	English only
	Debugging JTAG Chain Integrity	English only
	Power Analysis & Optimization for Intel Arria 10 & Stratix 10 Devices: Intro & Early Power Estimator	English only
	Power Analysis & Optimization for Intel Arria 10 & Stratix 10 Devices: Power Analyzer	English only
	Power Analysis & Optimization for Intel Arria 10 & Stratix 10 Devices: Optimization	English only
	Power Analysis & Optimization for Intel Arria 10 & Stratix 10 Devices: SmartVoltage ID	English only
	Power Analysis	English only
	Power Optimization	English only
	Intel FPGA Power and Thermal Calculator for Intel FPGA Devices	English and Japanese

FREE ONLINE TRAINING COURSES (COURSES ARE APPROXIMATELY ONE HOUR LONG)

COURSE CATEGORY	COURSE TITLES	LANGUAGES
Timing Analysis and Closure	Understanding Timing Analysis in FPGAs	English only
	Intel Quartus Prime Pro Software Timing Analysis – Part 1: Timing Analyzer	English only
	Intel Quartus Prime Pro Software Timing Analysis – Part 2: SDC Collections	English only
	Intel Quartus Prime Pro Software Timing Analysis – Part 3: Clock Constraints	English only
	Intel Quartus Prime Pro Software Timing Analysis – Part 4: I/O Interfaces	English only
	Intel Quartus Prime Pro Software Timing Analysis – Part 5: Timing Exceptions	English only
	Using Design Space Explorer	English and Japanese
	Timing Closure Using TimeQuest Custom Reporting	English only
	Design Evaluation for Timing Closure	English only
	Good High-Speed Design Practices	English only
	Clock Domain Crossing Considerations	English only
	Constraining Source Synchronous Interfaces	English, Chinese, and Japanese
	Constraining Double Data Rate Source Synchronous Interfaces	English, Chinese, and Japanese
	Stratix 10 Hyperflex FPGA Architecture Overview	English, Chinese, and Japanese
	Intel Quartus Prime Software Hyper-Aware Design Flow	English and Japanese
	Intel Hyperflex Architecture Overview for Intel Agilex Devices	English and Japanese
	Using Fast Forward Compile for the Intel Hyperflex FPGA Architecture	English and Japanese
	Introduction to Hyper-Retiming	English, Chinese, and Japanese
	Eliminating Barriers to Hyper-Retiming	English and Japanese
	Introduction to Hyper-Pipelining	English and Japanese
	Intel Hyperflex FPGA Architecture Design: Analyzing Critical Chains	English only
	Intel Stratix 10 FPGA Optimization: Loop Analysis and Solutions	English only
	Hyper-Optimization Techniques 2: Pre-Computation	English only
	Hyper-Optimization Techniques 3: Shannon's Decomposition	English only
	Creating High-Performance Designs in Intel Stratix 10 FPGAs	English only
	Creating High-Performance Designs in 20 nm Intel FPGAs	English and Japanese
Memory Interfaces	Verifying Memory Interfaces in Intel Agilex Devices	English and Japanese
	On-Chip Debugging of Memory Interfaces in Intel Agilex Devices	English only
	Introduction to Memory Interfaces in Intel Agilex Devices	English and Japanese
	Integration of Memory Interfaces in Intel Agilex Devices	English and Japanese
	Using High Performance Memory Interfaces in Altera 28 nm and 40 nm FPGAs	English and Chinese
	Introduction to Hybrid Memory Cubes with Altera FPGAs	English only
	Implementing the Hybrid Memory Cube Controller IP in an Altera FPGA	English only
	High Bandwidth Memory (HBM2) Interfaces in Intel Stratix 10 MX Devices: Introduction, Architecture	English only
	High Bandwidth Memory (HBM2) Interfaces in Intel Stratix 10 MX Devices: HBMC Features	English only
	High Bandwidth Memory (HBM2) Interfaces in Intel Stratix 10 MX Devices: Implementation	English only
	Introduction to Memory Interfaces IP in Intel FPGA Devices	English and Chinese
	Integrating Memory Interfaces IP in Intel FPGA Devices	English only
	On-Chip Debugging of Memory Interfaces IP in Intel FPGA Devices	English only
	Verifying Memory Interfaces IP in Intel FPGA Devices	English and Chinese

FREE ONLINE TRAINING COURSES (COURSES ARE APPROXIMATELY ONE HOUR LONG)

COURSE CATEGORY	COURSE TITLES	LANGUAGES
Connectivity Design	Debugging with the Ethernet Toolkit	English only
	Configuring the Intel FPGA E-Tile Hard IP for Ethernet	English and Japanese
	Intel FPGA E-Tile Transceiver Basics	English and Japanese
	Intel Stratix 10 FPGA L- and H-Tile Transceiver Basics	English, Chinese, and Japanese
	Intel FPGA E-Tile Clocking	English and Japanese
	Transceiver Basics for 20 nm and 28 nm Devices	English, Chinese and Japanese
	Transceiver Toolkit for 28-nm Devices	English and Chinese
	Transceiver Toolkit for Intel Stratix 10 Devices	English only
	Transceiver Toolkit for Intel Arria 10 and Cyclone 10 GX Devices	English only
	Generation 10 Transceiver Clocking	English only
	Building a Generation 10 Transceiver PHY Layer	English only
	Building an Intel Stratix 10 FPGA Transceiver PHY Layer	English only
	Advanced Signal Conditioning for Arria 10 FPGA Transceivers	English only
	Introduction to the Arria 10 Hard IP for PCI Express	English only
	Customizing Intel Stratix 10, Intel Arria 10 & Intel Cyclone 10 GX FPGA Hard IP for PCI Express	English only
	Connecting to the Arria 10 Hard IP for PCI Express	English only
	Designing with Intel Stratix 10, Intel Arria 10 & Intel Cyclone 10 GX Hard IP for PCI Express	English only
	Introduction to the 28 nm Hard IP for PCI Express	English only
	Customizing the 28 nm Hard IP for PCI Express	English only
	Connecting to the 28 nm Hard IP for PCI Express	English only
	Designing with the 28 nm Hard IP for PCI Express	English only
	Introduction to the Triple-Speed Ethernet MegaCore Function	English and Chinese
	Implementing the Triple-Speed Ethernet MegaCore Function	English only
	Introduction to the 10Gb Ethernet PHY Intel FPGA IP Cores	English only
	Introduction to the Low Latency 10Gb Ethernet MAC Intel FPGA IP Core	English only
	Using the 10Gb Ethernet Design Examples	English only
	Designing Boards with Intel Agilex FPGAs	English only
System Design	Platform Designer Standard Interfaces	English only
	Introduction to Platform Designer	English, Chinese, and Japanese
	Creating a System Design with Platform Designer: Getting Started	English, Chinese, and Japanese
	Creating a System Design with Platform Designer: Finish the System	English and Chinese
	Platform Designer in the Intel Quartus Prime Pro Edition Software	English only
	Advanced System Design Using Platform Designer: Component & System Simulation	English only
	Advanced System Design Using Platform Designer: System Optimization	English only
	Advanced System Design Using Platform Designer: System Verification with System Console	English only
	Advanced System Design Using Platform Designer: Utilizing Hierarchy	English only
	Custom IP Development Using Avalon and Arm AMBA AXI Interfaces	English, Chinese, and Japanese
	DSP Builder Advanced Blockset: Getting Started	English only
	DSP Builder Advanced Blockset: Interfaces and IP Libraries	English only
	DSP Builder Advanced Blockset: Using Primitives	English only
	Variable-Precision DSP Blocks in Altera 20 nm FPGAs	English only
	High Performance Floating Point Processing with FPGAs	English only
	Building Video Systems	English only
	Creating Reusable Design Blocks: Introduction to IP Reuse with the Intel Quartus Prime Software	English only
	Creating Reusable Design Blocks: IP Design & Implementation with the Intel Quartus Prime Software	English and Japanese
	Creating Reusable Design Blocks: IP Integration with the Intel Quartus Prime Software	English and Japanese
	Avalon Verification Suite	English and Chinese
	Low-Density Parity-Check (LDPC) Codes Intel FPGA IP for 5G Systems	English only

FREE ONLINE TRAINING COURSES (COURSES ARE APPROXIMATELY ONE HOUR LONG)

COURSE CATEGORY	COURSE TITLES	LANGUAGES
Embedded System Design	Intel Stratix 10 SoC FPGA Technical Overview	English only
	Hardware Design Flow for an Arm-based Intel SoC FPGA	English, Chinese, and Japanese
	Software Design Flow for an Arm-based Intel SoC FPGA	English, Chinese, and Japanese
	Initial Design Review for Arria 10 SoC FPGA Designs	English only
	Using Linux on Intel SoC FPGAs Ask an Expert	English only
	Getting Started with Linux OS for Intel SoC FPGAs	English and Japanese
	SoC Hardware Overview: Interconnect and Memory	English and Chinese
	SoC Hardware Overview: System Management, Debug, and General Purpose Peripherals	English, Chinese and Japanese
	SoC Hardware Overview: the Microprocessor Unit	English, Chinese and Japanese
	Profiling Intel SoC FPGAs with Arm Streamline	English only
	Creating Second Stage Bootloader for Altera SoCs	English only
	Secure Boot with Arria 10 SoC FPGAs	English only
	The Nios II Processor: Booting	English only
	Designing with the Nios II Processor and Qsys - Day 1	Japanese only
	Using the Nios II Processor	Chinese only
	Using the Nios II Processor: Custom Components and Instructions	English only
	Using the Nios II Processor: Hardware Development	English only
	Using the Nios II Processor: Software Development	English only
	The Nios II Processor: Hardware Abstraction Layer	English only
Device-Specific Training	Intel Agilex FPGA Configuration	English and Japanese
	Introduction to Configuring Intel FPGAs	English and Chinese
	Configuration Schemes for Intel FPGAs	English and Chinese
	Configuration for Stratix 10 Devices	English and Chinese
	Integrating an Analog to Digital Converter in Intel MAX 10 Devices	English only
	Introduction to Analog to Digital Conversion in Intel MAX 10 Devices	English only
	Using the ADC Toolkit in Intel MAX 10 Devices	English only
	Using the MAX 10 User Flash Memory	English only
	Using the MAX 10 User Flash Memory with the Nios II Processor	English only
	Using the Generic Serial Flash Interface	English only
	Reducing Compile Time with Fast Preservation	English and Japanese
	Remote System Upgrade in Intel MAX 10 Devices	English, Chinese, and Japanese
	Remote System Upgrade in MAX 10 Devices: Design Flow & Demonstration	Chinese and Japanese
	Mitigating Single Event Upsets in Intel Arria 10 and Intel Cyclone 10 GX Devices	English and Japanese
	SEU Mitigation in Arria 10 Devices: Hierarchy Tagging	English only
	SEU Mitigation in Intel FPGA Devices: Fault Injection	English only
	Thermal Management in Intel Stratix 10 Devices	English and Chinese
Scripting	Command-Line Scripting	English only
	Introduction to Tcl	English and Chinese
	Intel Quartus Prime Software Tcl Scripting	English and Chinese

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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