

2N6451, 2N6452 N-Channel JFET

Features

- InterFET [N0132L Geometry](#)
- Low Noise: 1.0 nV/√Hz Typical
- High Gain: 15mS Minimum
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

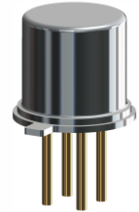
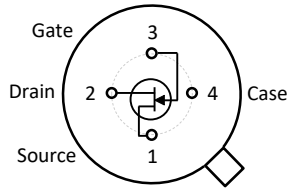
Applications

- Audio Amplifiers
- Low-Noise, High Gain Amplifiers
- Low-Noise Preamplifiers

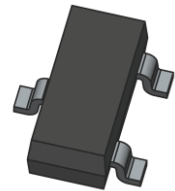
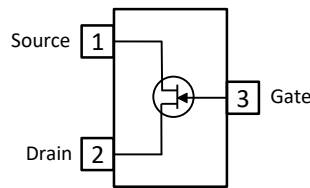
Description

The -25V InterFET 2N6451 and 2N6452 are targeted for sensitive amplifier stages for mid-frequencies designs. Gate leakages are typically less than 50pA at room temperatures. The TO-72 package is hermetically sealed and suitable for military applications.

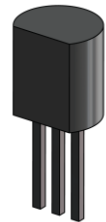
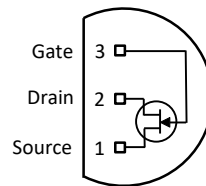
TO-72 Bottom View



SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters	2N6451 Min	2N6452 Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	-20	-25	V
I_{DSS} Drain to Source Saturation Current	5	5	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.5	-0.5	V
G_{FS} Forward Transconductance	15	15	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N6451; 2N6452	Through-Hole	TO-72	Bulk
PN6451; PN6452	Through-Hole	TO-92	Bulk
SMP6451; SMP6452	Surface Mount	SOT23	Bulk
SMP6451TR; SMP6452TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N6451COT; 2N6452COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N6451CFT; 2N6452CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-25	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	300	mW
P Power Derating	2	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

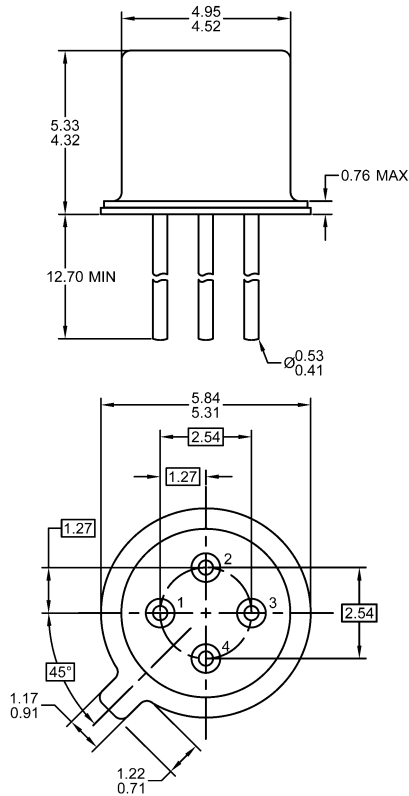
Parameters	Conditions	2N6451		2N6452		Unit
		Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-20		-25		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -10V, V_{DS} = 0V, T_A = 25^\circ\text{C}$		-0.1			nA
	$V_{GS} = -15V, V_{DS} = 0V, T_A = 25^\circ\text{C}$				-0.5	nA
	$V_{GS} = -10V, V_{DS} = 0V, T_A = 125^\circ\text{C}$		-0.2			μA
	$V_{GS} = -15V, V_{DS} = 0V, T_A = 125^\circ\text{C}$				-1	μA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 0.5\text{nA}$	-0.5	-3.5	-0.5	-3.5	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	5	20	5	20	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N6451		2N6452		Unit
		Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{kHz}$	15	30	15	30	mS
G_{OS} Output Conductance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{kHz}$		50		50	μS
C_{iss} Input Capacitance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{MHz}$		25		25	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{MHz}$		5		5	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 10V, I_D = 5\text{mA}, f = 10\text{Hz}$		5		10	nV/ $\sqrt{\text{Hz}}$
	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{kHz}$		3		8	
NF Noise Figure	$V_{DS} = 10V, I_D = 5\text{mA}, f = 10\text{Hz}$ $R_G = 10\text{k}\Omega$		1.5		2.5	dB

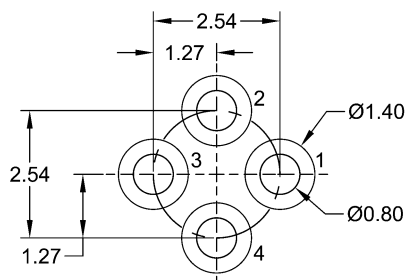
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

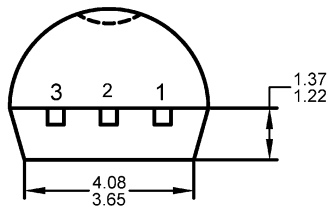
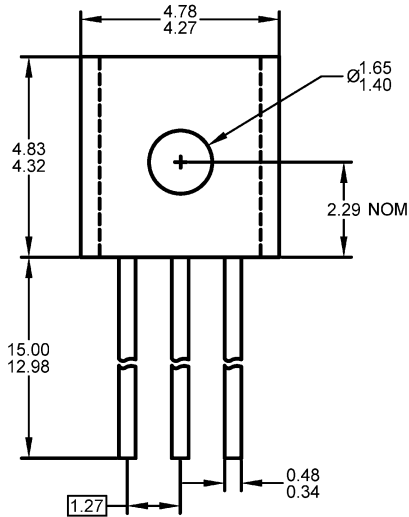
Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

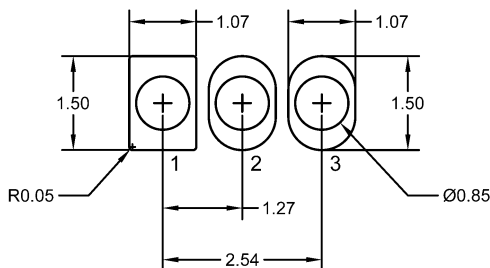
TO-92 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

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