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Technical
Support

## IF1322, IF1322A Dual Matched N-Channel JFET

## Features

- InterFET N0132L Geometry
- Low Noise: $1.0 \mathrm{nV} / \mathrm{VHz}$ Typical
- High Gain: 20mS Typical
- Low Cutoff Voltage: 1.5V Maximum
- RoHS Compliant
- SMT, TH, and Bare Die Package options.


## Applications

- Low Noise High Gain Amplifier
- Differential Amplifiers
- Instrumentation Amplifiers
- Acoustic and Vibration Sensors


## Description

The -20V InterFET IF1322 matched pair JFET is targeted for low noise high gain differential amplifier designs. The IF1322 has a cutoff voltage of less than 1.5 V ideal for low-level power supplies. The TO-71 package is hermetically sealed and suitable for military uses. Custom specifications, matching, and packaging options are available.


SOIC8 Top View


## Product Summary

| Parameters |  | IF1322 Min | IF1322A Min | Unit |
| :--- | :--- | :---: | :---: | :---: |
| BV | GSS | Gate to Source Breakdown Voltage | -20 | -20 |
| IDSS | Drain to Source Saturation Current | 8 | 8 | V |
| $\mathrm{~V}_{\text {GS(off) }}$ | Gate to Source Cutoff Voltage | -0.8 | -0.8 | mA |
| $\mathrm{G}_{\text {FS }}$ | Forward Transconductance | 10 | 10 | V |

Ordering Information Custom Part and Binning Options Available E

| Part Number | Description | Case | Packaging |
| :--- | :--- | :---: | :---: |
| IF1322T71; IF1322AT71 | Through-Hole | TO-71 | Bulk |
| IF1322S08; IF1322AS08 | Surface Mount | SOIC8 | Bulk |
|  | 7" Tape and Reel: Max 500 Pieces <br> IF1322S08TR; IF1322AS08TR | 13" Tape and Reel: Max 2,500 Pieces | SOIC8 |$\quad$| Minimum 500 Pieces |
| :---: |
| Tape and Reel |
| IF1322COT; IF1322ACOT |
| IF1322CFT; IF1322ACFT * |
| Chip Orientated Tray (COT Waffle Pack) |

* Bare die packaged options are designed for matched specifications but not $100 \%$ tested

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IF1322-A

## Electrical Characteristics

Maximum Ratings (@ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Unless otherwise specified)

| Parameters | Value | Unit |  |
| :--- | :--- | :---: | :---: |
| $\mathrm{V}_{\text {RGS }}$ | Reverse Gate Source and Gate Drain Voltage | -20 | V |
| $\mathrm{I}_{\mathrm{FG}}$ | Continuous Forward Gate Current | 50 | mA |
| $\mathrm{P}_{\mathrm{D}}$ | Continuous Device Power Dissipation | 400 | mW |
| P | Power Derating | 2.3 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Operating Junction Temperature | -55 to 125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {STG }}$ | Storage Temperature | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |

Static Characteristics (@TA $=25^{\circ} \mathrm{C}$, Unless otherwise specified)

| Parameters |  | Conditions | IF1322 |  | IF1322A |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |
| $\mathrm{V}_{\text {(BR) }}$ GSS | Gate to Source Breakdown Voltage |  | $\begin{gathered} \text { GSS1: } I_{G}=-25 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DS}}=0 \mathrm{~V} \\ \mathrm{GSS} 2: \mathrm{I}_{\mathrm{G}}=-3 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DS}}=0 \mathrm{~V} \\ \mathrm{GSS}: \mathrm{I}_{\mathrm{G}}=-1 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DS}}=0 \mathrm{~V} \end{gathered}$ | -20 |  | -20 |  | V |
| Igss | Gate to Source Reverse Current | $\mathrm{V}_{\text {dS }}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=-10 \mathrm{~V}$ |  | -0.1 |  | -0.1 | nA |
| VGS(OfF) | Gate to Source Cutoff Voltage | $V_{\text {DS }}=10 \mathrm{~V}, \mathrm{ld}=1 \mu \mathrm{~A}$ | -0.8 | -1.5 | -0.8 | -1.5 | V |
| $V_{\text {GS(F) }}$ | Gate to Source Forward Voltage | $\begin{aligned} & V_{D S}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{G}}=-1 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{DS}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{G}}=-1 \mu \mathrm{~A} \end{aligned}$ | 0.3 | 1.0 | 0.3 | 1.0 | V |
| loss | Drain to Source Saturation Current | $\begin{gathered} \mathrm{V}_{\mathrm{DS}}=10 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V} \\ \text { (Pulsed) } \end{gathered}$ | 8 | 25 | 8 | 25 | mA |

Dynamic Characteristics (@ TA $=25^{\circ} \mathrm{C}$, Unless otherwise specified)

| Parameters |  | Conditions | IF1322 |  | IF1322A |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |
| Gfs | Forward Transconductance |  | $\mathrm{V}_{\mathrm{DS}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}$ | 10 |  | 10 |  | mS |
| $\left\|\mathrm{V}_{\mathrm{GS} 1}-\mathrm{V}_{\mathrm{GS} 2}\right\|$ | Differential Gate Source Voltage | $\mathrm{V}_{\mathrm{DS}}=5 \mathrm{~V}, \mathrm{ld}=3 \mathrm{~mA}$ |  | 30 |  | 40 | mV |
| $\mathrm{e}_{\mathrm{n}}$ | Equivalent Circuit Input Noise Voltage | $\begin{gathered} V_{D S}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=3 \mathrm{~mA}, \mathrm{f}=1 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{DS}}=5 \mathrm{~V}, \mathrm{ID}_{\mathrm{D}}=3 \mathrm{~mA}, \mathrm{f}=100 \mathrm{~Hz} \end{gathered}$ |  | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ |  | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ | $\mathrm{nV} / \sqrt{ } \mathrm{Hz}$ |
| In | Equivalent Circuit Input Noise Current | $\mathrm{V}_{\mathrm{DS}}=5 \mathrm{~V}, \mathrm{ld}=3 \mathrm{~mA}, \mathrm{f}=1 \mathrm{kHz}$ |  | 0.05 |  | 0.05 | $\mathrm{pA} / \sqrt{ } \mathrm{Hz}$ |

## Typical IF1322, IF1322A Characteristics



Typical IF1322, IF1322A Characteristics (Continued)



## SOIC8 Mechanical and Layout Data

## Package Outline Data




1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-O rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

## Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.


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## T0-71 Mechanical and Layout Data

## Package Outline Data



## Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.
7. All linear dimensions are in millimeters.
8. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
9. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

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