

# IFN5564, IFN5565, IFN5566 Dual Matched N-Channel JFET

## Features

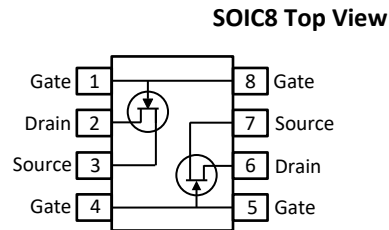
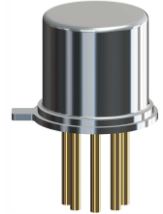
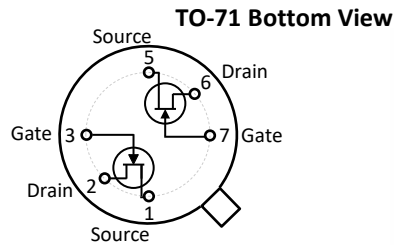
- InterFET [N0072S Geometry](#)
- Low Noise: 2.5 nV/√Hz Typical
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 6.5 pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

## Applications

- Wide Band Differential Amplifier
- Commutators

## Description

The -40V InterFET IFN5564, IFN5565, and IFN5566 JFET's are targeted for wide bandwidth differential amplifiers and commutators. Gate leakages are less than 10pA at room temperatures. The IFN5564 is matched down to 5mV. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



## Product Summary

Parameters	IFN5564 Min	IFN5565 Min	IFN5566 Min	Unit
$BV_{GSS}$ Gate to Source Breakdown Voltage	-40	-40	-40	V
$I_{DSS}$ Drain to Source Saturation Current	5	5	5	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.5	-0.5	-0.5	V
$G_{FS}$ Forward Transconductance	7000	7000	7000	$\mu S$

## Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN5564; IFN5565; IFN5566	Through-Hole	TO-71	Bulk
SMP5564; SMP5565; SMP5566	Through-Hole	SOIC8	Bulk
SMP5564TR; SMP5565TR; SMP5566TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFN5564COT; IFN5565COT; IFN5566COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFN5564CFT; IFN5565CFT; IFN5566CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

\* Bare die packaged options are designed for matched specifications but not 100% tested



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V <sub>RGS</sub> Reverse Gate Source and Gate Drain Voltage	-40	V
I <sub>FG</sub> Continuous Forward Gate Current	50	mA
P <sub>D</sub> Continuous Device Power Dissipation	650	mW
P Power Derating	3.3	mW/°C
T <sub>J</sub> Operating Junction Temperature	-55 to 150	°C
T <sub>STG</sub> Storage Temperature	-65 to 200	°C

### Static Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

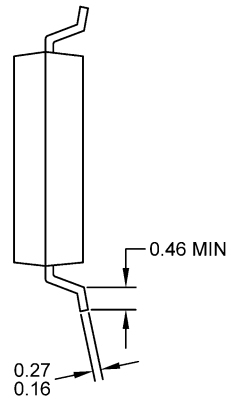
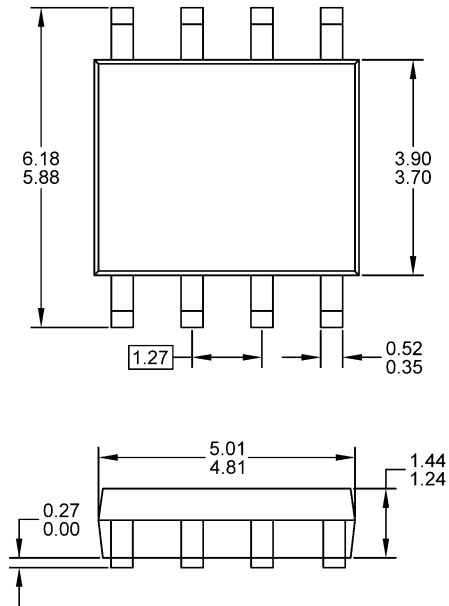
Parameters	Conditions	IFN5564, IFN5565, IFN5566		Unit
		Min	Max	
V <sub>(BR)GSS</sub> Gate to Source Breakdown Voltage	I <sub>G</sub> = -1μA, V <sub>DS</sub> = 0V	-40		V
I <sub>GSS</sub> Gate to Source Reverse Current	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0V, T <sub>A</sub> = 25°C V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0V, T <sub>A</sub> = 150°C		-100 -200	pA nA
V <sub>GS(OFF)</sub> Gate to Source Cutoff Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1nA	-0.5	-3	V
V <sub>GS(F)</sub> Gate Source Forward Voltage	V <sub>DS</sub> = 0V, I <sub>G</sub> = 2mA		1	V
I <sub>DSS</sub> Drain to Source Saturation Current	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V (Pulsed)	5	30	mA
R <sub>DS(ON)</sub> Static Drain to Source ON Resistance	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA		100	Ω

### Dynamic Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Conditions	IFN5564, IFN5565, IFN5566		Unit
		Min	Max	
G <sub>FS</sub> Forward Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 1kHz V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 100MHz	7000 7000	12500	μhmo
G <sub>OS</sub> Output Conductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 1kHz		45	μhmo
C <sub>iss</sub> Input Capacitance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 1MHz		12	pF
C <sub>rss</sub> Reverse Capacitance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 1MHz		3	pF
NF Noise Figure	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 10Hz, R <sub>G</sub> = 1MΩ		1	dB
e <sub>n</sub> Equivalent Circuit Input Noise Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA, f = 10Hz		50	nV/√Hz
I <sub>DSS1</sub> /I <sub>DSS2</sub> Saturation Drain Current Ratio	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V (Pulsed)	0.95	1	-
V <sub>GS1</sub> - V <sub>GS2</sub>   Differential Gate Source Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA	IFN5564 IFN5565 IFN5566	5 10 20	mV
$\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ Differential Gate Source Voltage with Temperature	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA T <sub>A</sub> = 25°C to -55°C [0.8,2,4] T <sub>A</sub> = 25°C to 125°C [1,2.5,5]	IFN5564 IFN5565 IFN5566	0.8 2 4 1 2.5 5	mV/°C
g <sub>fs1</sub> /g <sub>fs2</sub> Transconductance Ratio	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA	IFN5564 IFN5565 IFN5566	0.95 0.9 0.9	1 1 1 -

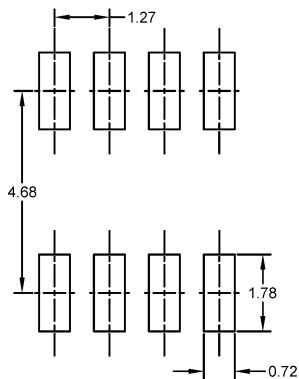
## SOIC8 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

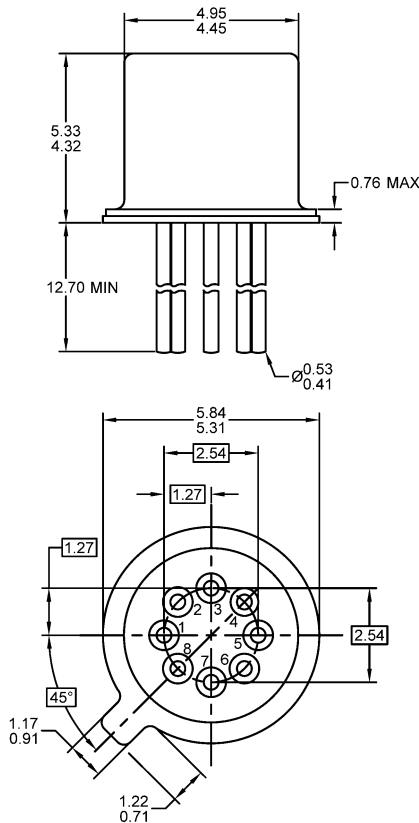
### Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

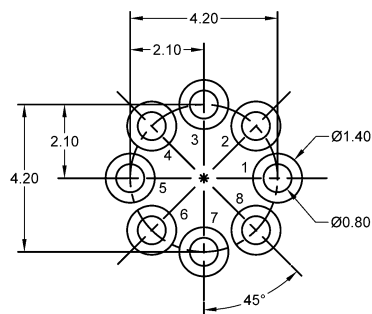
## TO-71 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

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