

Micropower Single Supply Rail-to-Rail Input-Output Op Amp

The EL8186 is a micropower operational amplifier optimized for single supply operation at 5V and can operate down to 2.4V.

The EL8186 draws minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micropower supply current. Offset current, voltage and current noise, slew rate, and gain-bandwidth product are all two to ten times better than on previous micropower op amps.

The EL8186 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Ordering Information

PART NUMBER (BRAND)	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL8186IW-T7	BBJA	7" (3K pcs)	6-Pin SOT-23	MDP0038
EL8186IW-T7A	BBJA	7" (250 pcs)	6-Pin SOT-23	MDP0038
EL8186IWZ-T7 (Note)	BBRA	7" (3K pcs)	6-Pin SOT-23 (Pb-free)	MDP0038
EL8186IWZ-T7A (Note)	BBRA	7" (250 pcs)	6-Pin SOT-23 (Pb-free)	MDP0038
EL8186ISZ (Note)	8186ISZ	-	8-Pin SO (Pb-free)	MDP0027
EL8186ISZ-T7 (Note)	8186ISZ	7"	8-Pin SO (Pb-free)	MDP0027
EL8186ISZ-T13 (Note)	8186ISZ	13"	8-Pin SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

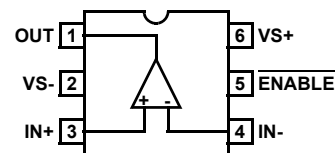
- 55µA supply current
- 400µV typical offset voltage
- 500pA input bias current
- 400kHz gain-bandwidth product
- 1MHz -3dB bandwidth
- 0.13V/µs slew rate
- Single supply operation down to 2.4V
- Rail-to-rail input and output
- Output sources and sinks 26mA load current
- Pb-Free plus anneal available (RoHS compliant)

Applications

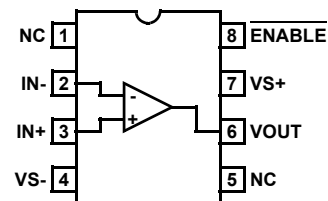
- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre amps
- pH probe amplifiers

Pinouts

**EL8186
(6-PIN SOT-23)
TOP VIEW**



**EL8186
(8-PIN SO)
TOP VIEW**



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	5.5V	Output Short-Circuit Duration	Indefinite
Differential Input Current	5mA	Ambient Operating Temperature Range	-40°C to +85°C
Input Voltage	-0.5V to $V_S + 0.5V$	Storage Temperature Range	-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage			0.4	1	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			1		$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current			0.4	2	nA
I_B	Input Bias Current			0.5	3	nA
e_N	Input Noise Voltage Peak-to-Peak	$f = 0.1\text{Hz to } 10\text{Hz}$		1		μV_{PP}
	Input Noise Voltage Density	$f_O = 1\text{kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$
i_N	Input Noise Current Density	$f_O = 1\text{kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V \text{ to } 5V$	90	110		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.4V \text{ to } 5V$	90	110		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.5V \text{ to } 4.5V, R_L = 100\text{k}\Omega$	200	500		V/mV
		$V_O = 0.5V \text{ to } 4.5V, R_L = 1\text{k}\Omega$		25		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, $R_L = 100\text{k}\Omega$		3	6	mV
		Output low, $R_L = 1\text{k}\Omega$		130	200	mV
		Output high, $R_L = 100\text{k}\Omega$	4.994	4.997		V
		Output high, $R_L = 1\text{k}\Omega$	4.8	4.88		V
SR	Slew Rate		0.09	0.13	0.17	$\text{V}/\mu\text{s}$
GBW	Gain Bandwidth Product	$f_O = 100\text{kHz}$		400		kHz
BW	-3dB Bandwidth	Unity gain, $C_{LOAD} = 27\text{pF}, R_F = 100$		1		MHz
$I_{S,ON}$	Supply Current, Enabled		40	55	75	μA
$I_{S,OFF}$	Supply Current, Disabled			3	10	μA
I_{O+}	Short Circuit Output Current	$R_L = 10\Omega$	18	31		mA
I_{O-}	Short Circuit Output Current	$R_L = 10\Omega$	17	26		mA
V_S	Minimum Supply Voltage			2.2	2.4	V
V_{INH}	Enable Pin High Level				2	V
V_{INL}	Enable Pin Low Level		0.8			V
I_{ENH}	Enable Pin Input Current	$V_{EN} = 5V$	0.25	0.7	2	μA
I_{ENL}	Enable Pin Input Current	$V_{EN} = 0V$	-0.5	0	+0.5	μA

Typical Performance Curves

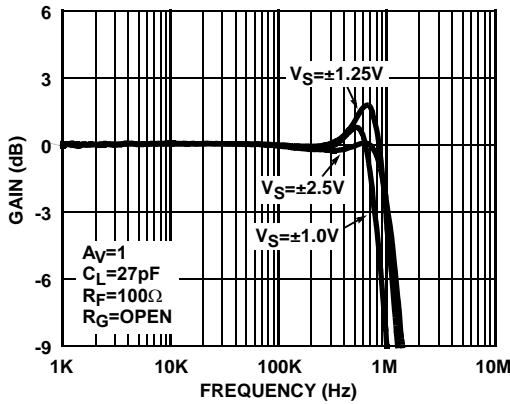


FIGURE 1. UNITY GAIN FREQUENCY RESPONSE vs SUPPLY VOLTAGE

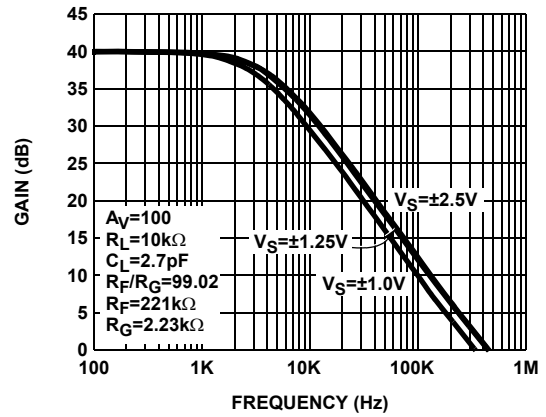


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

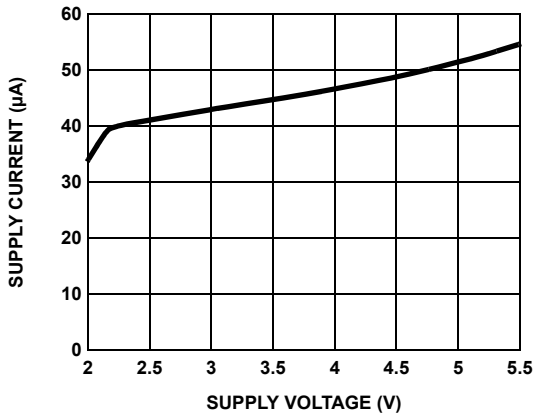


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

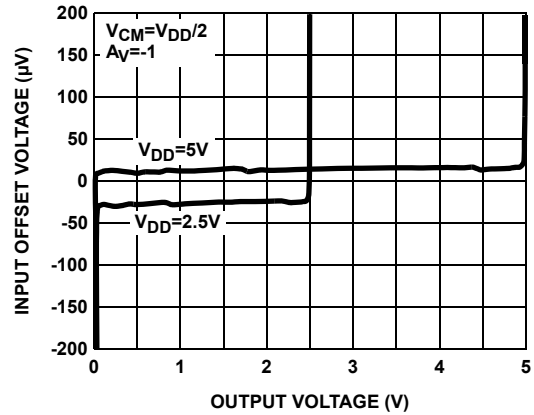


FIGURE 4. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

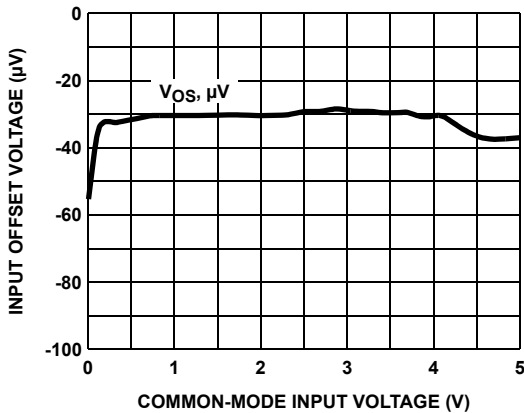


FIGURE 5. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

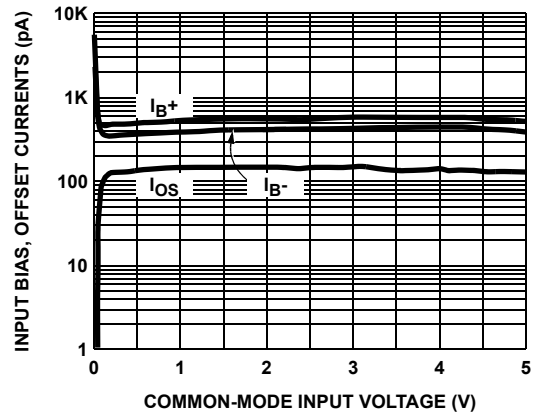


FIGURE 6. INPUT BIAS + OFFSET CURRENTS vs COMMON-MODE INPUT VOLTAGE

Typical Performance Curves (Continued)

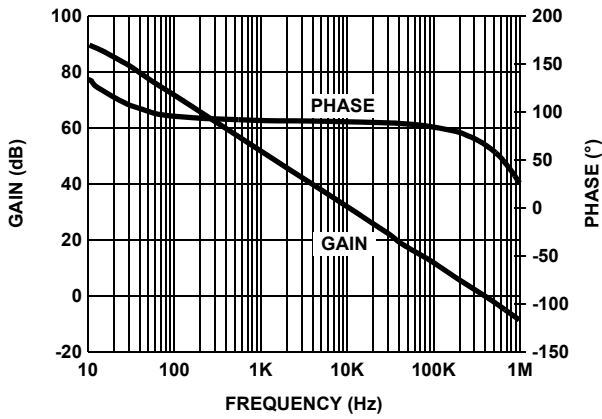


FIGURE 7. A_{VOL} vs FREQUENCY @ 1k Ω LOAD

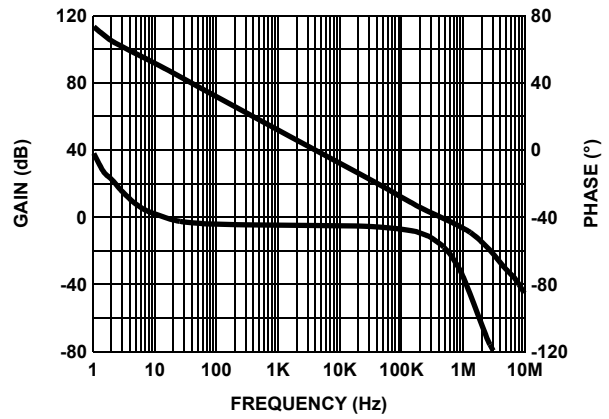


FIGURE 8. A_{VOL} vs FREQUENCY @ 100k Ω LOAD

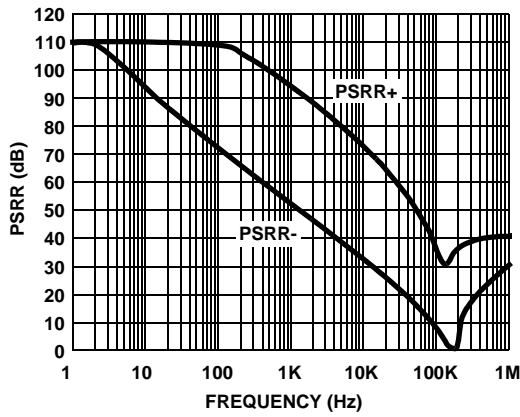


FIGURE 9. PSRR vs FREQUENCY

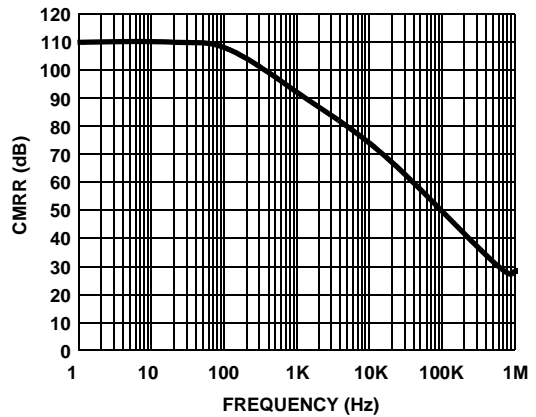


FIGURE 10. CMRR vs FREQUENCY

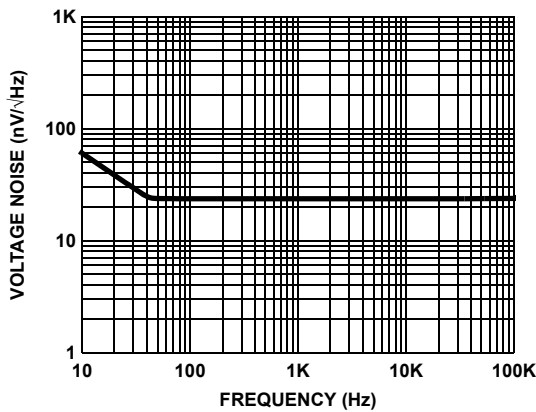


FIGURE 11. VOLTAGE NOISE vs FREQUENCY

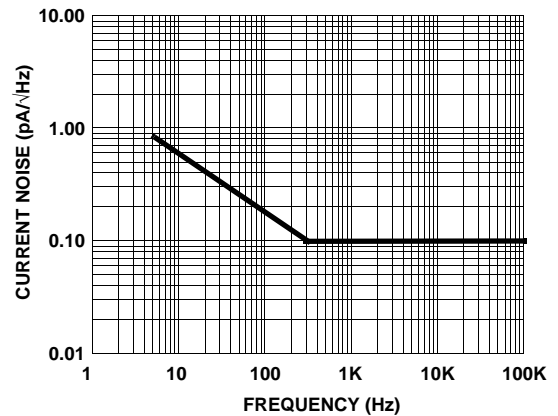


FIGURE 12. CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

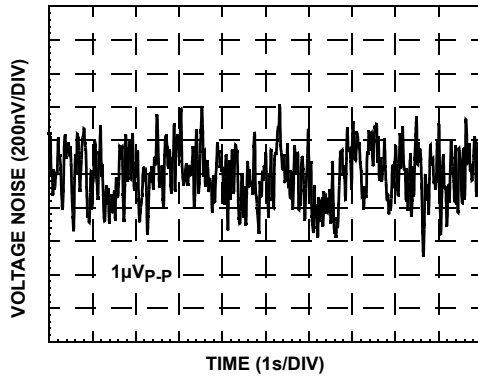


FIGURE 13. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

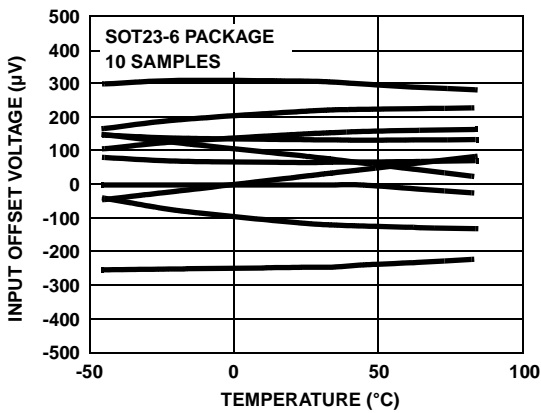


FIGURE 14. V_{OS} vs TEMPERATURE

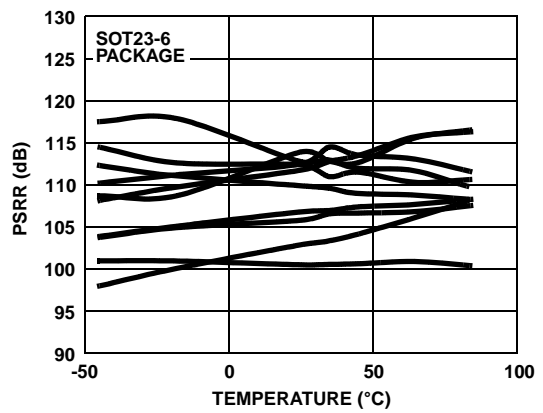


FIGURE 15. PSRR vs TEMPERATURE

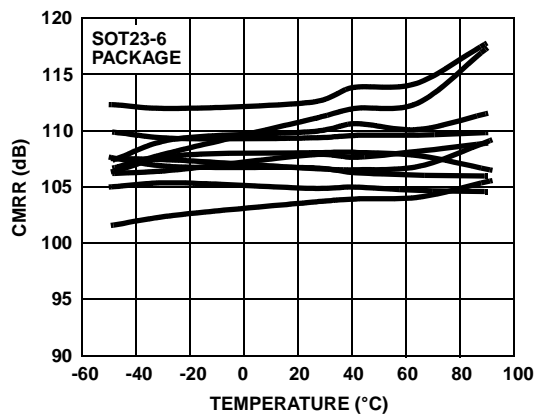


FIGURE 16. CMRR vs TEMPERATURE

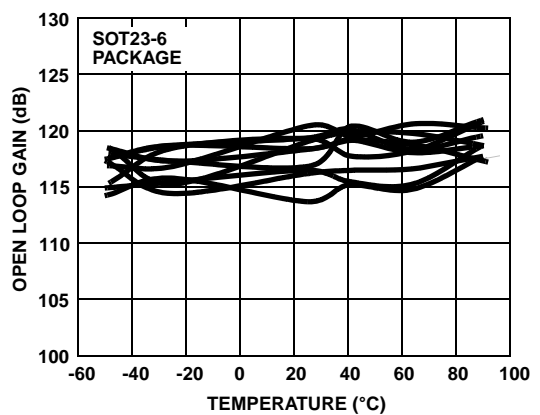


FIGURE 17. A_{VOL} vs TEMPERATURE

Typical Performance Curves (Continued)

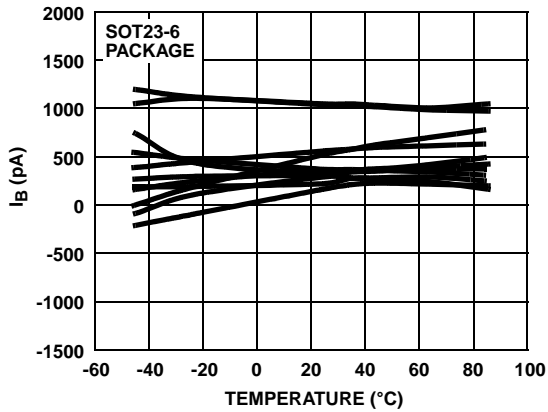


FIGURE 18. I_B vs TEMPERATURE

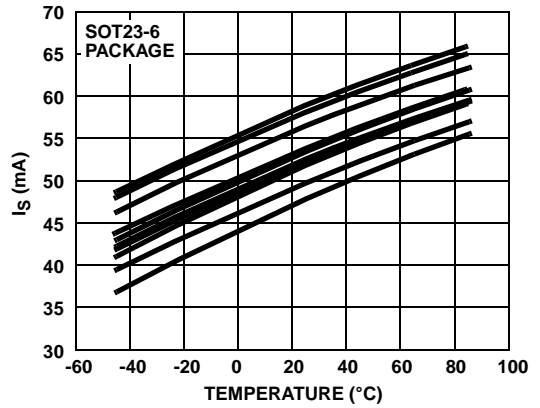


FIGURE 19. I_S vs TEMPERATURE

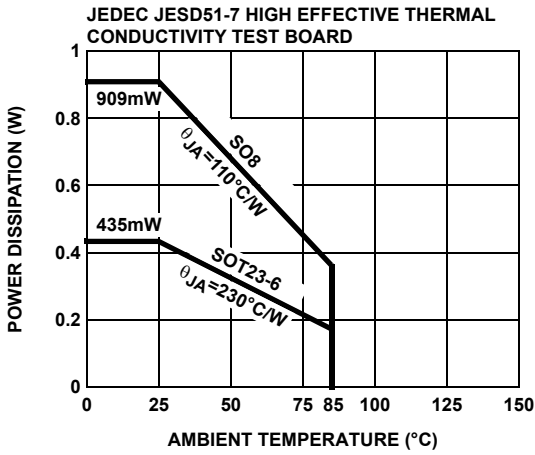


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

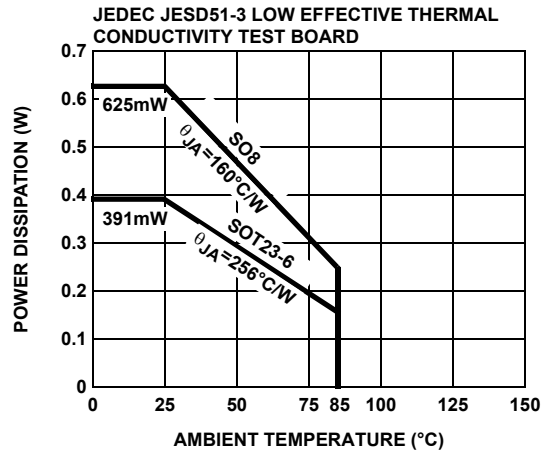


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Introduction

The EL8186 is a rail-to-rail input and output micro-power single supply operational amplifier with an enable feature. The device achieves rail-to-rail input and output operation and eliminates the concerns introduced by a conventional rail-to-rail input and output operational amplifier.

Rail-to-Rail Input

The input common-mode voltage range of the EL8186 goes from negative supply to positive supply without introducing offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The EL8186 achieves input rail-to-rail performance without sacrificing important precision specifications and without degrading distortion performance. The EL8186's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range for the EL8186 gives consistent behavior from typically 10mV above the negative rail all the way up to the positive rail.

Input Bias Current Compensation

The input bias currents of the EL8186 are reduced to a typical 500pA while maintaining excellent bandwidth for a micro-power operational amplifier. Inside the EL8186 is an input bias cancelling circuit. The input stage transistors are still biased with an adequate amount of current for speed but the cancelling circuit sinks most of the base current, leaving a small fraction as input bias current. The input bias current compensation/cancellation operates from typically 10mV above the negative rail to the positive supply rail.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The EL8186 with a 100k Ω load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The EL8186 offers an EN pin. The active low enable pin disables the device when pulled up to at least 2.2V. Upon disable the part consumes typically 3 μ A, while the output is in a high impedance state. The EN also has an internal pull down. If left open, the EN pin will pull to negative rail and the device will be enabled by default. The high impedance at output during disable allows multiple EL8186s to be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the EN pin.

Typical Applications

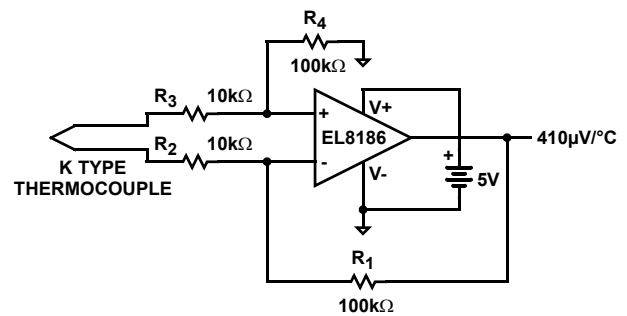
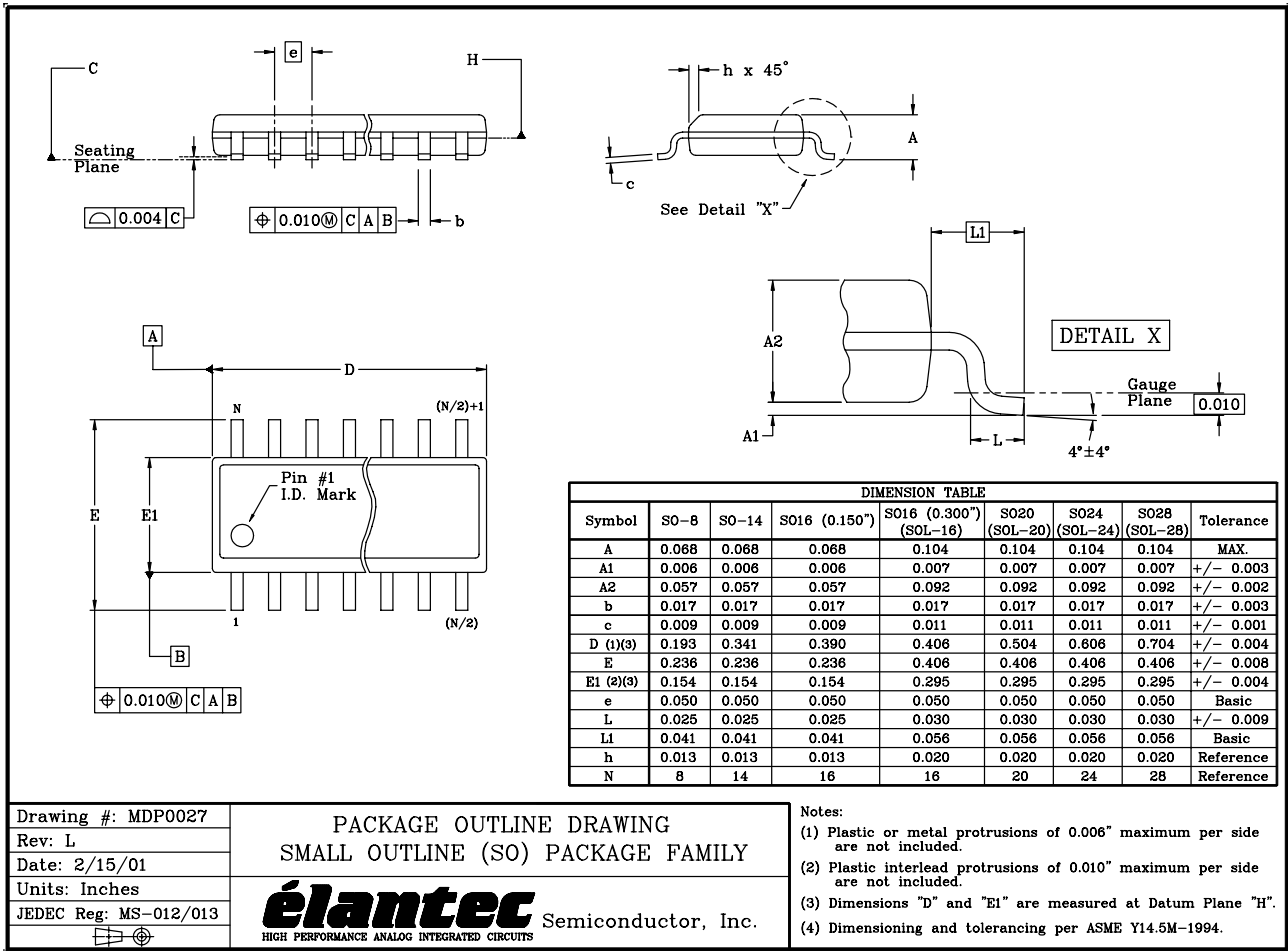


FIGURE 22. THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The EL8186 is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The EL8186's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

SO Package Outline Drawing

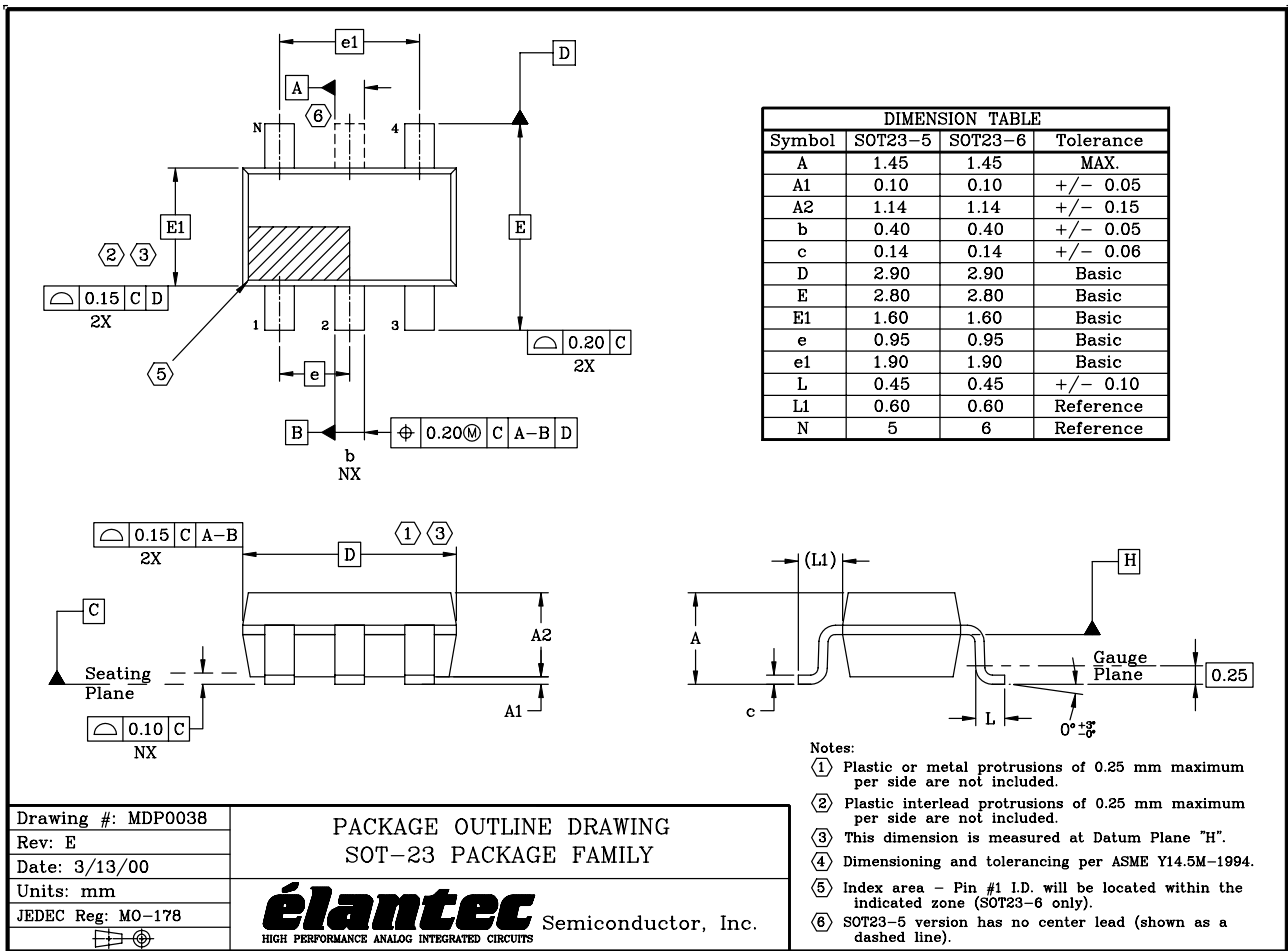


Drawing #: MDP0027
 Rev: L
 Date: 2/15/01
 Units: Inches
 JEDEC Reg: MS-012/013

PACKAGE OUTLINE DRAWING
 SMALL OUTLINE (SO) PACKAGE FAMILY

élantec Semiconductor, Inc.
 HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

SOT-23 Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

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