HA-2520, HA-2522, HA-2525

20MHz, High Slew Rate, Uncompensated, High Input Impedance, Operational Amplifiers

FN2894
Rev 10.00
June 13, 2014

HA-2520, HA-2522, HA-2525 comprise a series of operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

120V/µs slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for RF and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520, HA-2522, HA-2525's superior dynamic specifications are complemented by 10nA offset current, 100MΩ input impedance and offset trim capability.

Features

- High slew rate 120V/µs
- Fast settling 200ns
- Full power bandwidth 2MHz
- Gain bandwidth ($A_V \geq 3$). 20MHz
- High input impedance 100MΩ
- Low offset current. 10nA
- Compensation pin for unity gain capability
- Pb-free PDIP available (RoHS compliant)

Applications

- Data acquisition systems
- RF amplifiers
- Video amplifiers
- Signal generators

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA2-2520-2	HA2- 2520-2	-55 to +125	8 Ld Metal Can	T8.C
HA7-2520-2	HA7- 2520-2	-55 to +125	8 Ld CerDIP	F8.3A
HA2-2522-2	HA2- 2522-2	-55 to +125	8 Ld Metal Can	T8.C
HA3-2525-5Z (Notes 1, 2)	HA3- 2525-5Z	0 to +75	8 Ld PDIP	E8.3

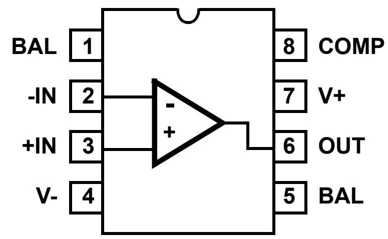
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Pb-Free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

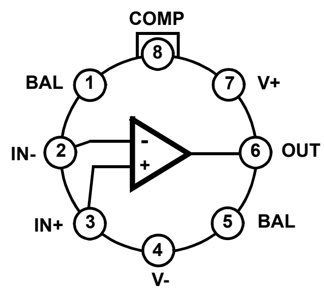
HA-2520, HA-2522, HA-2525

Pinouts

HA-2520, HA-2525
(8 LD CERDIP, 8 LD PDIP)
TOP VIEW



HA-2520, HA-2522
(8 LD METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 40V
Differential Input Voltage 15V
Output Current 50mA

Operating Conditions

Temperature Range
HA-2520/2522-2 . . . . -55°C to +125°C
HA-2525-5 . . . . 0°C to +75°C

Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
PDIP Package*	96	N/A
CERDIP Package	135	50

Maximum Junction Temperature (Hermetic Packages) . . . . . +175°C
Maximum Junction Temperature (Plastic Package) . . . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
4. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications V_{SUPPLY} = ±15V

PARAMETER	TEMP (°C)	HA-2520-2 MIN (Note 16)	HA-2520-2 TYP	HA-2520-2 MAX (Note 16)	HA-2522-2 MIN (Note 16)	HA-2522-2 TYP	HA-2522-2 MAX (Note 16)	HA-2525-5 MIN (Note 16)	HA-2525-5 TYP	HA-2525-5 MAX (Note 16)	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	25		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Drift	Full		20			25			30		µV/°C
Bias Current	25		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	25		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 5)	25	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10			±10			±10			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 6, 9)	25	10	15		7.5	15		7.5	15		kV/V
	Full	7.5			5			5			kV/V
Common Mode Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB
Gain Bandwidth (Notes 5, 8)	25	10	20		10	20		10	20		MHz
Minimum Stable Gain	25	3			3			3			V/V
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 6)	Full	±10	±12		±10	±12		±10	±12		V
Output Current (Note 9)	25	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Notes 9, 14)	25	1.5	2.0		1.2	2.0		1.2	2.0		MHz

Electrical Specifications V_{SUPPLY} = ±15V **(Continued)**

PARAMETER	TEMP (°C)	HA-2520-2			HA-2522-2			HA-2525-5			UNITS
		MIN (Note 16)	TYP	MAX (Note 16)	MIN (Note 16)	TYP	MAX (Note 16)	MIN (Note 16)	TYP	MAX (Note 16)	
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 6, 10, 11, 13)	25		25	50		25	50		25	50	ns
Overshoot (Notes 6, 10, 11, 13)	25		25	40		25	50		25	50	%
Slew Rate (Notes 6, 10, 17, 15)	25	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 6, 10, 17, 15)	25		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	25		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 12)	Full	80	90		74	90		74	90		dB

NOTES:

5. This parameter value is based on design calculations.
6. R_L = 2kΩ
7. V_{CM} = ±10V.
8. A_V > 10.
9. V_O = ±10V.
10. C_L = 50pF.
11. V_O = ±200mV.
12. ΔV = ±5V.
13. See "Transient Response" Test Circuits and Waveforms.
14. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
15. V_{OUT} = ±5V.
16. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
17. See " Slew Rate and Settling Time" Test Circuits and Waveforms.

Test Circuits and Waveforms

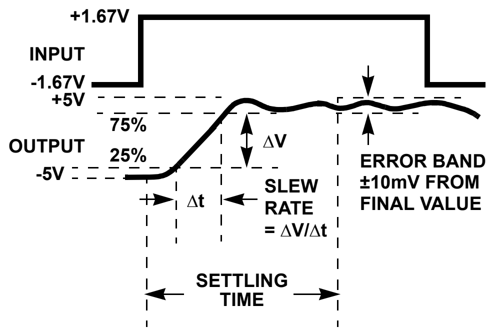
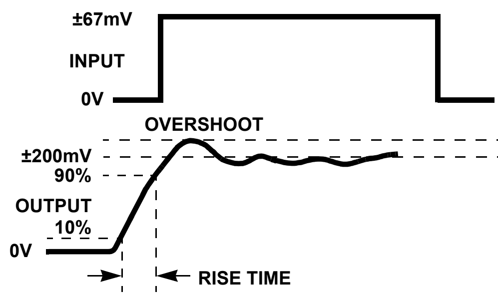


FIGURE 1. SLEW RATE AND SETTLING TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

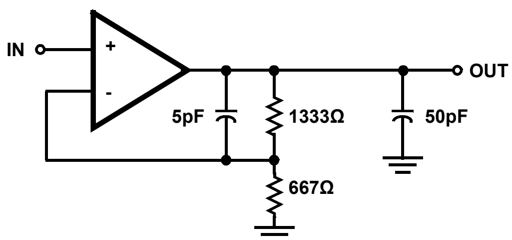
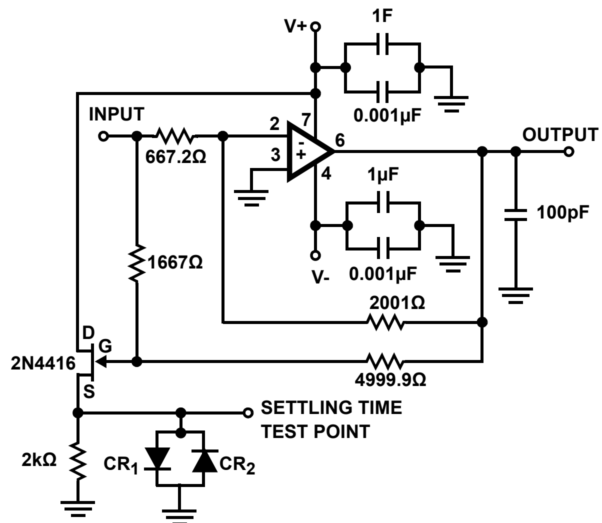


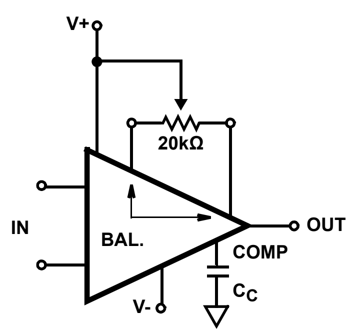
FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE



NOTES:

18. A_V = -3.
19. Feedback and summing resistor ratios should be 0.1% matched.
20. Clipping diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

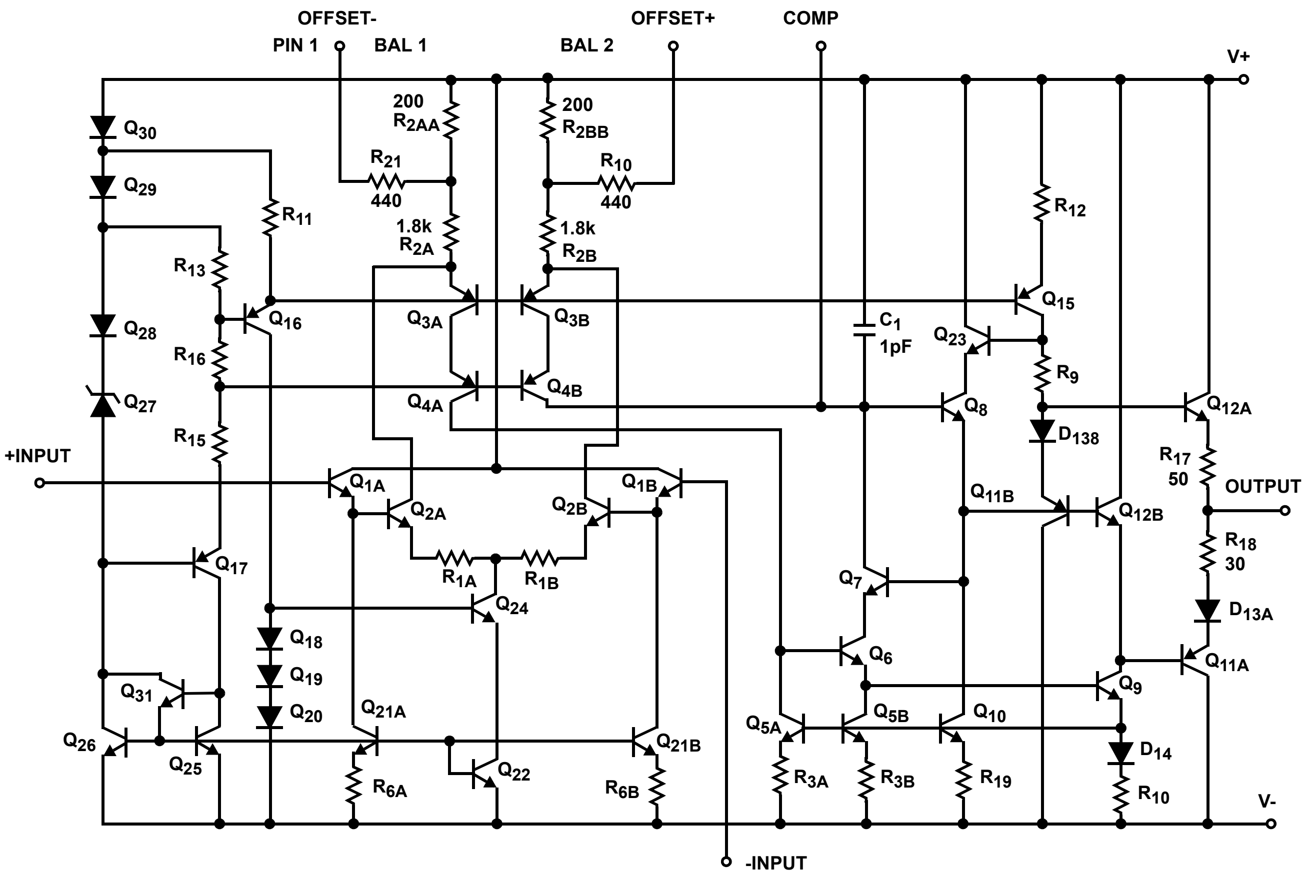
FIGURE 4. SETTLING TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is $|V_{OS}$ + 1mV$|$ minimum referred to output. Typical ranges are ±20mV with R_T = 20kΩ.

FIGURE 5. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

Schematic Diagram



Typical Application

Inverting Unity Gain Circuit

Figure 6 shows a Compensation Circuit for an inverting unity gain amplifier. The circuit was tested for functionality with supply voltages from ±4V to ±15V, and the performance as tested was: Slew Rate ≈ 120V/μs; Bandwidth ≈ 10MHz; and Settling Time (0.1%) ≈ 500ns. Figure 7 illustrates the amplifier's frequency response, and it is important to note that capacitance at pin 8 must be minimized for maximum bandwidth.

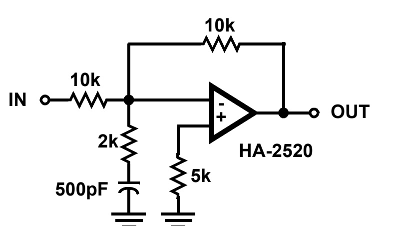


FIGURE 6. INVERTING UNITY GAIN CIRCUIT

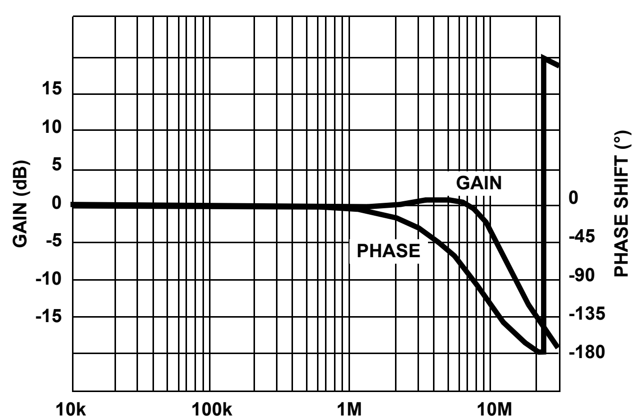


FIGURE 7. FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT

Typical Performance Curves V_S = ±15V, T_A = +25°C, Unless Otherwise Specified

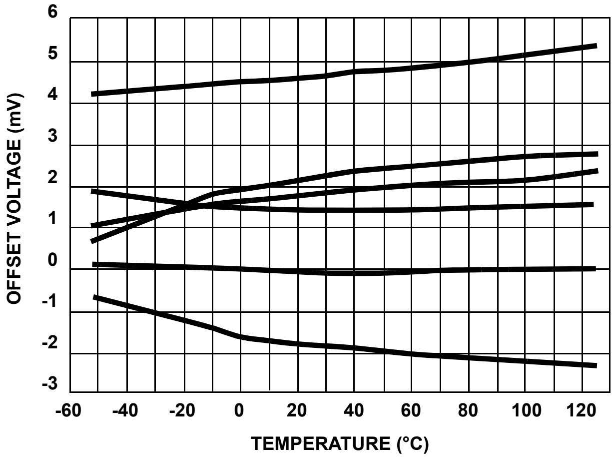


FIGURE 8. OFFSET VOLTAGE vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

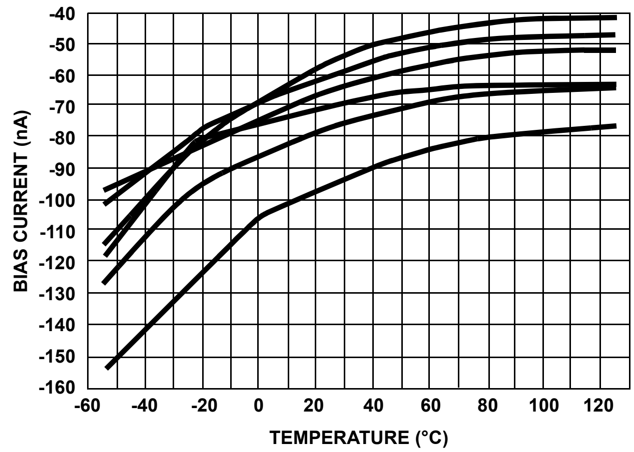


FIGURE 9. BIAS CURRENT vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

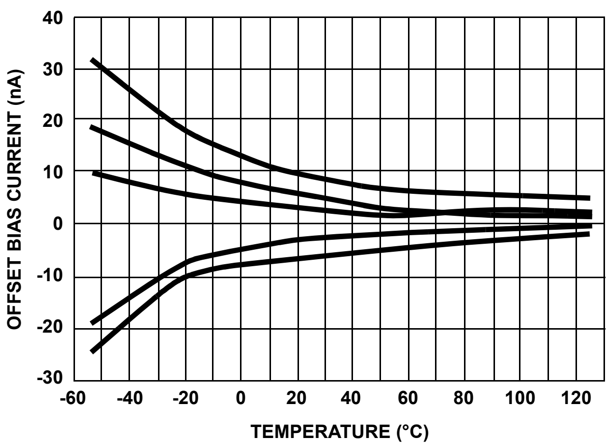


FIGURE 10. OFFSET CURRENT vs TEMPERATURE (5 TYPICAL UNITS FROM 3 LOTS)

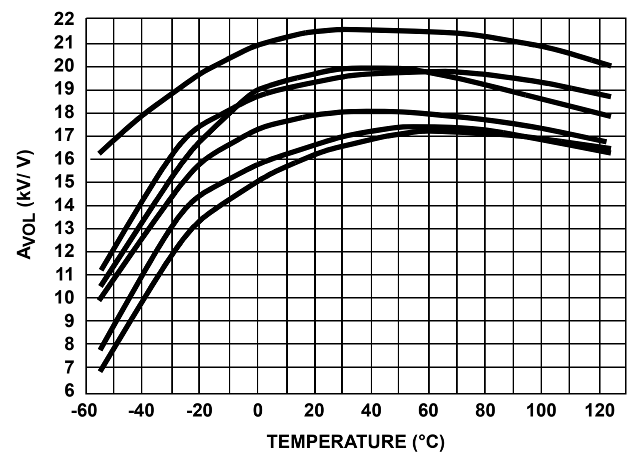


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

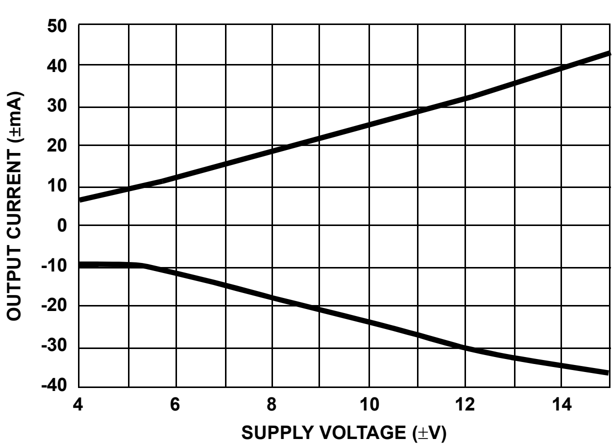


FIGURE 12. OUTPUT CURRENT vs SUPPLY VOLTAGE

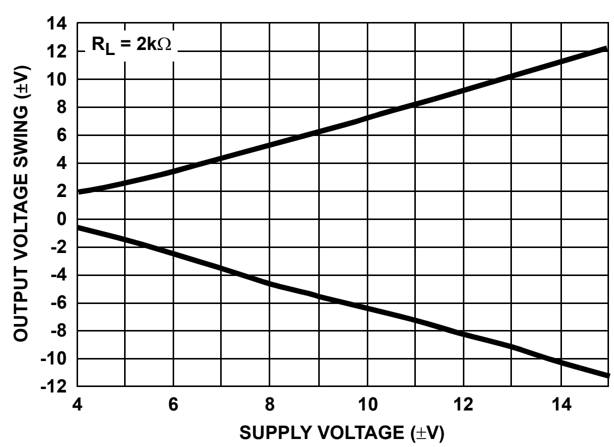


FIGURE 13. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

HA-2520, HA-2522, HA-2525

Typical Performance Curves V_S = ±15V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

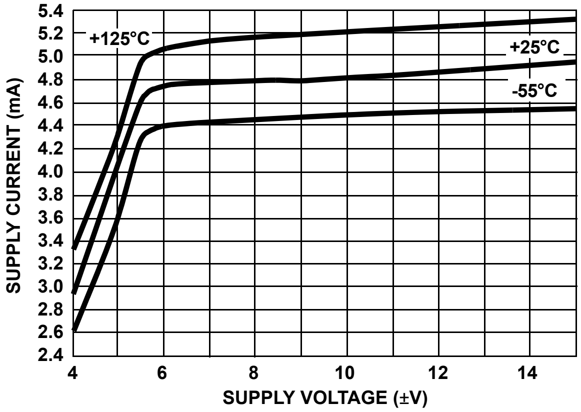


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

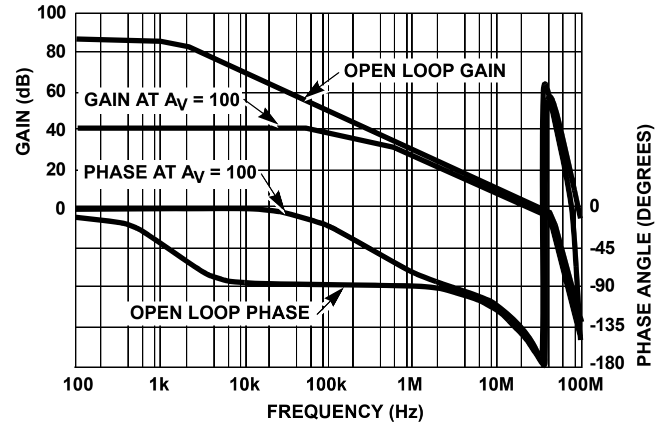


FIGURE 15. FREQUENCY RESPONSE

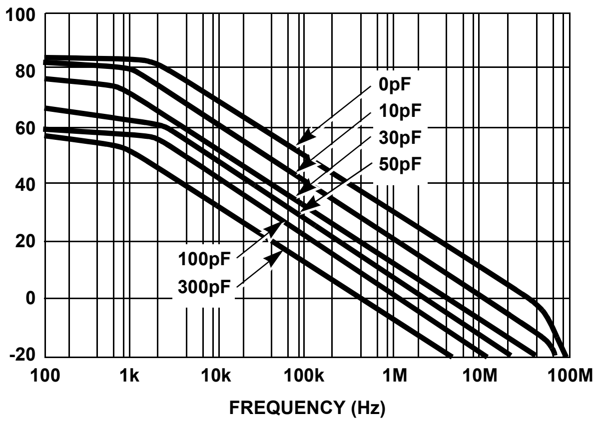


FIGURE 16. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP PIN TO GROUND

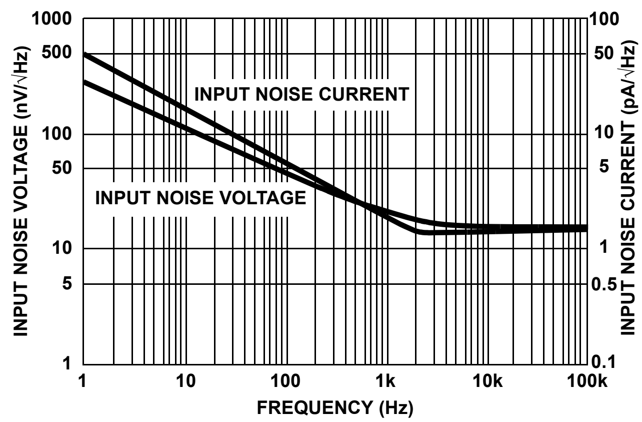


FIGURE 17. INPUT NOISE CHARACTERISTICS

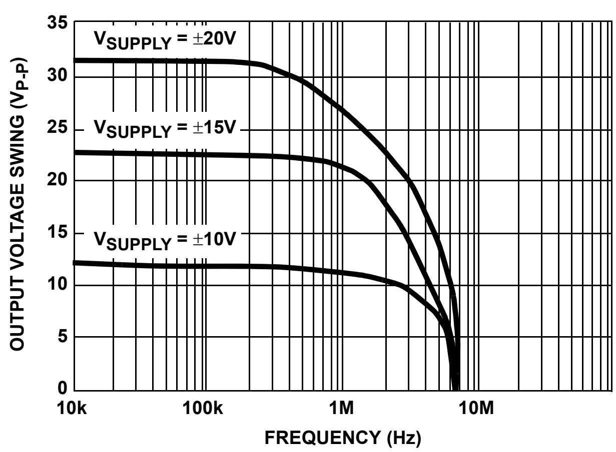


FIGURE 18. OUTPUT VOLTAGE SWING vs FREQUENCY

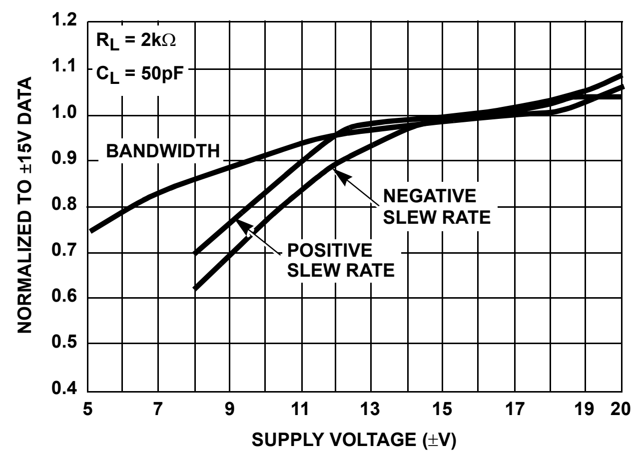


FIGURE 19. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

HA-2520, HA-2522, HA-2525

Die Characteristics

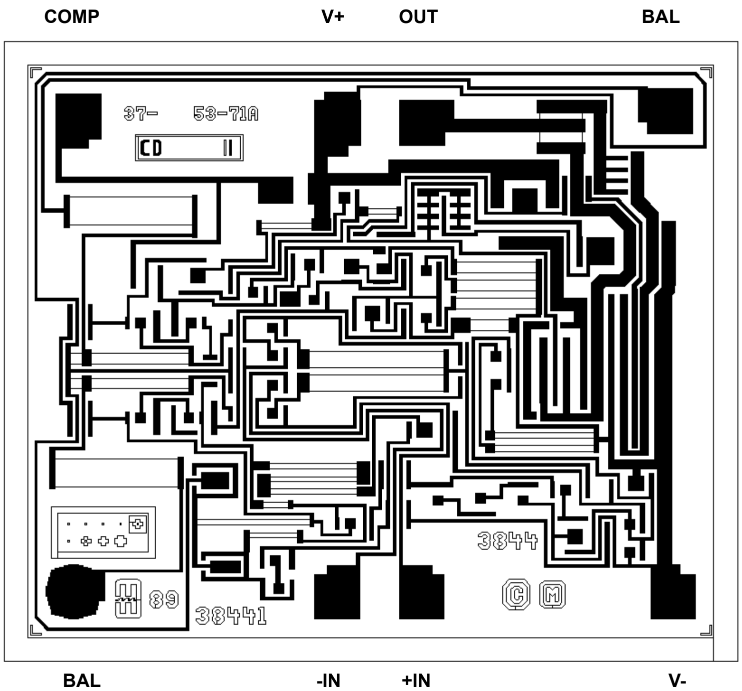
SUBSTRATE POTENTIAL:
Unbiased

TRANSISTOR COUNT:
40

PROCESS:
Bipolar Dielectric Isolation

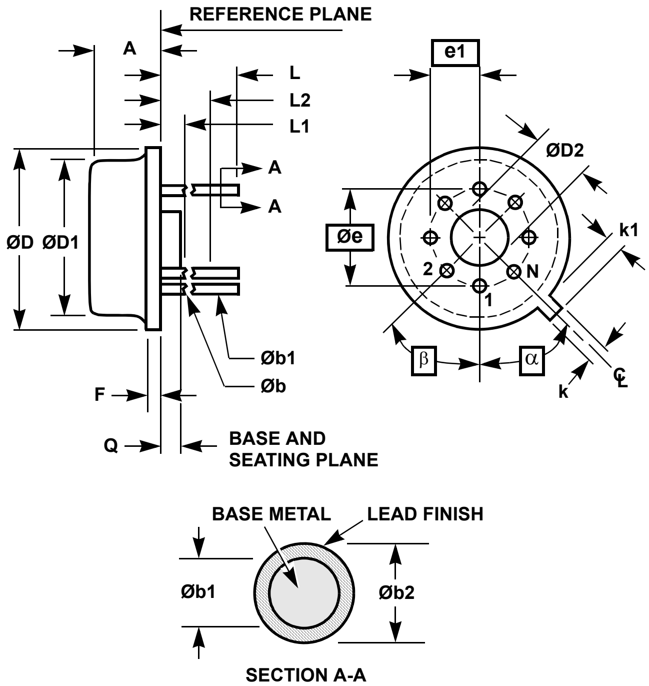
Metallization Mask Layout

HA-2520, HA-2522, HA-2525



HA-2520, HA-2522, HA-2525

Metal Can Packages (Can)



T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
a	45° BSC		45° BSC		3
b	45° BSC		45° BSC		3
N	8		8		4

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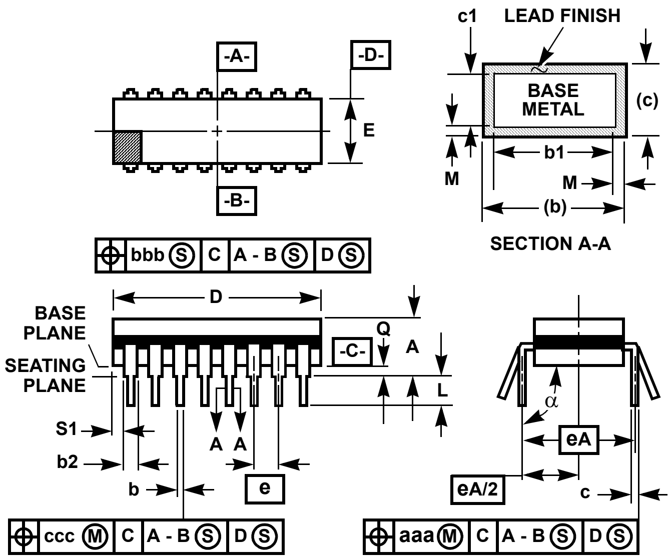
NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. a is the basic spacing from the centerline of the tab to terminal 1 and b is the basic spacing of each lead or lead position (N -1 places) from a, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

HA-2520, HA-2522, HA-2525

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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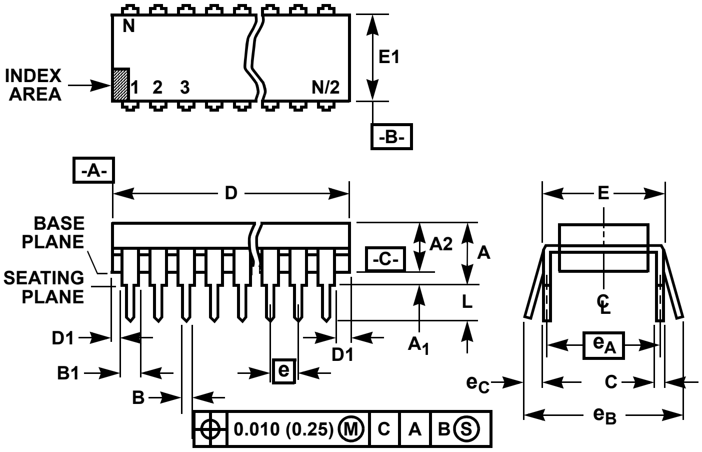
HA-2520, HA-2522, HA-2525

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).