

HD-15530

CMOS Manchester Encoder-Decoder

FN2960  
Rev 1.00  
March 1997

Features

- Support of MIL-STD-1553
- Data Rate . . . . . 1.25 MBit/s
- Sync Identification and Lock-In
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power . . . . .50mW at 5V

Ordering Information

PACKAGE	TEMP. RANGE	1.25 MEGABIT/s	PKG. NO.
CERDIP	-40°C to +85°C	HD1-15530-9	F24.6
	-55°C to +125°C	HD1-15530-8	
		7802901JA	
CLCC	-40°C to +85°C	HD4-15530-9	J28.A
	-55°C to +125°C	HD4-15530-8	
		78029013A	
PDIP	-40°C to +85°C	HD3-15530-9	E24.6

Description

The Intersil HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

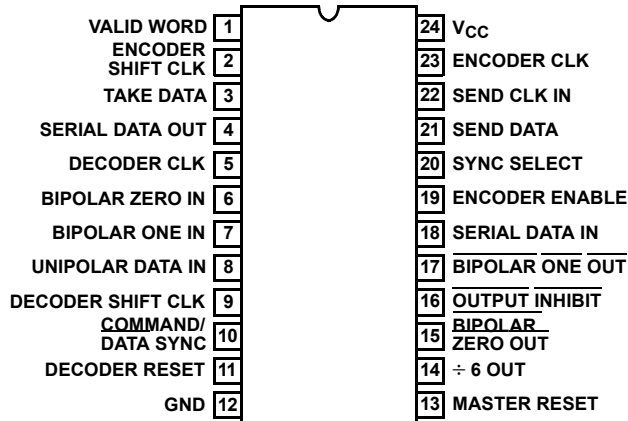
This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5V supply.

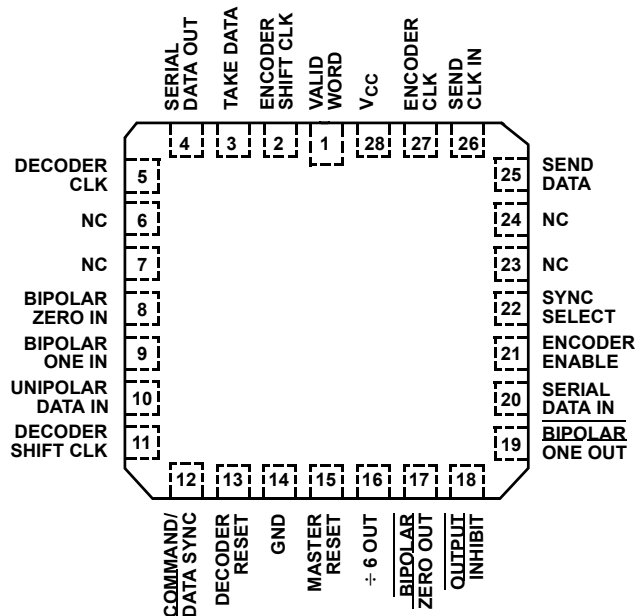
The HD-15530 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.

Pinouts

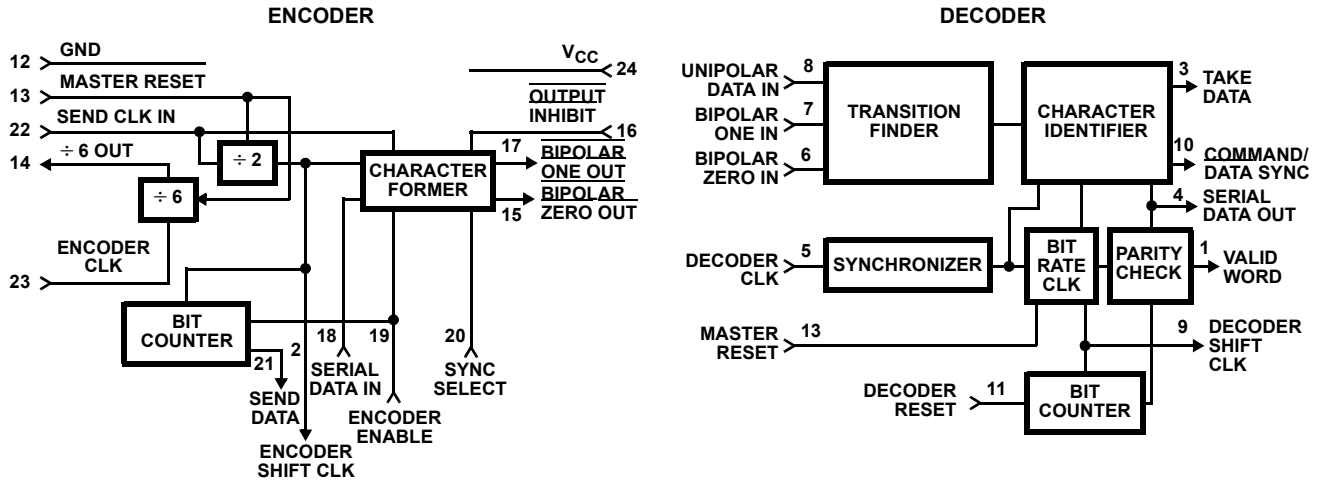
HD-15530 (CERDIP, PDIP)  
TOP VIEW



HD-15530 (CLCC)  
TOP VIEW



**Block Diagrams**



**Pin Description**

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNLPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	BIPOLAR ZERO OUT	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	OUTPUT INHIBIT	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	BIPOLAR ONE OUT	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.

**Pin Description** (Continued)

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	V <sub>CC</sub>	Both	V <sub>CC</sub> is the +5V power supply pin. A 0.1µF decoupling capacitor from V <sub>CC</sub> (pin 24) to GROUND (pin 12) is recommended.

I = Input    O = Output

**Encoder Operation**

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA

input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low- to-high transition (3) - (4). After the sync and Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

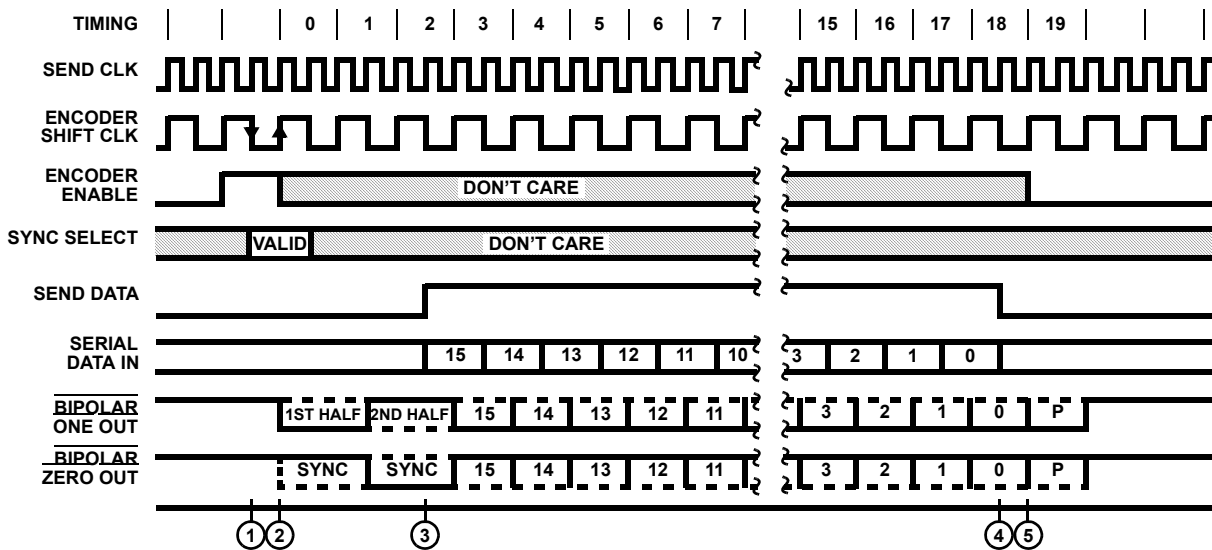


FIGURE 1.

## Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/DATA SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT

is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

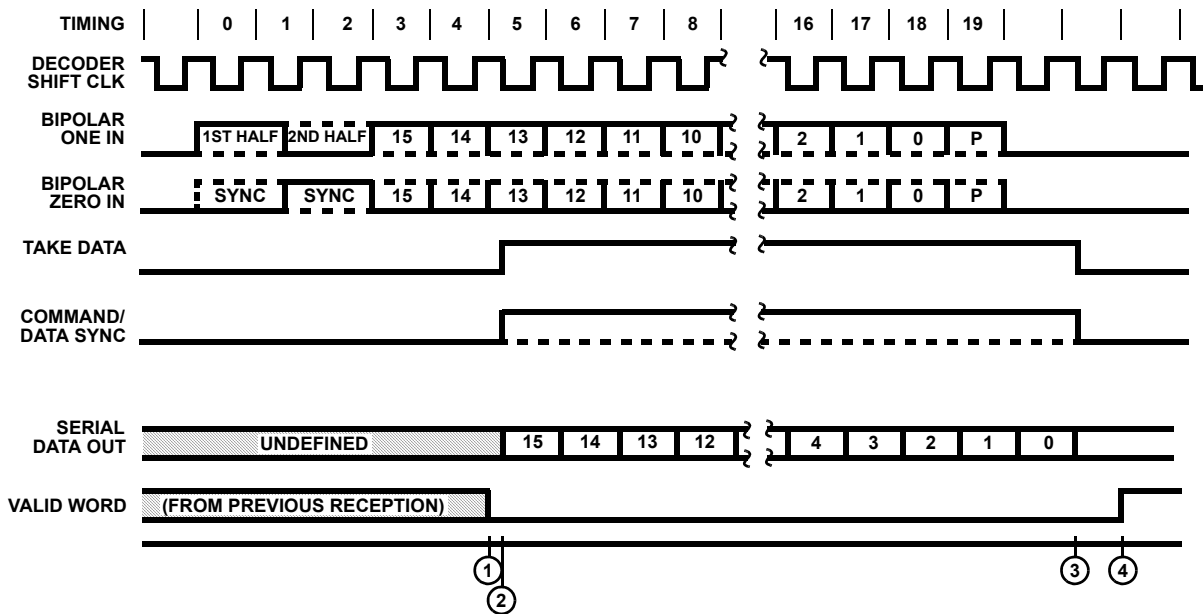


FIGURE 2.

### How to Make Our MTU Look Like a Manchester Encoded UART

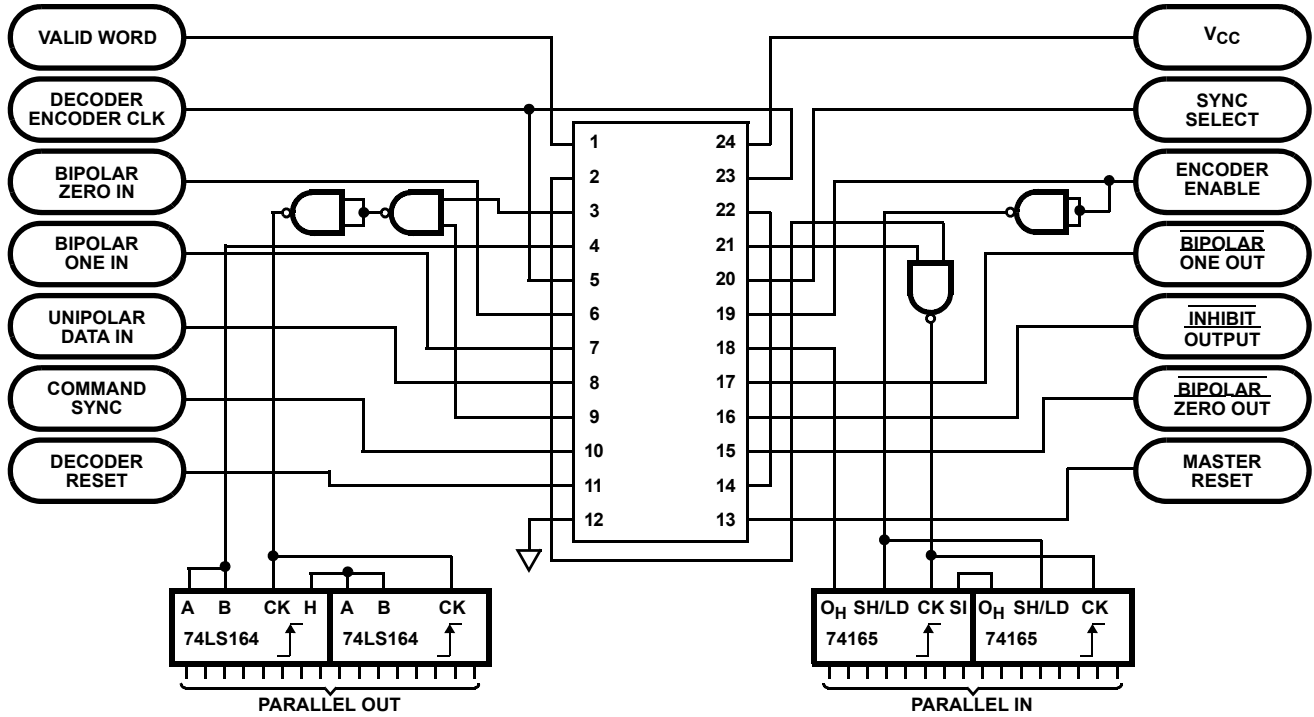


FIGURE 3.

### Typical Timing Diagrams for a Manchester Encoded UART

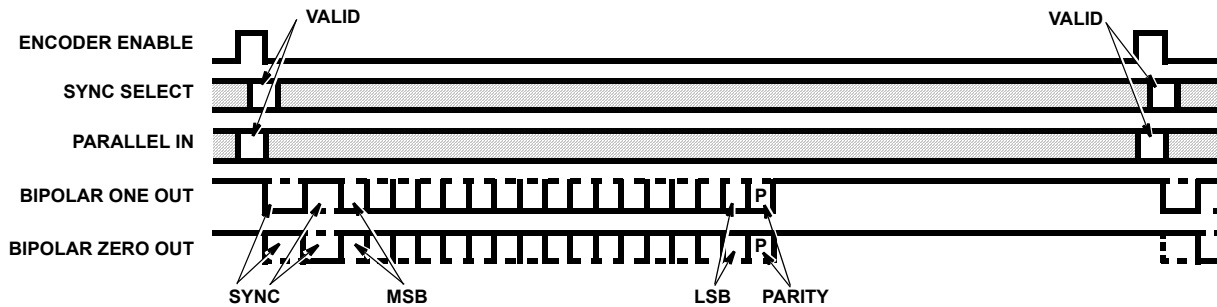


FIGURE 4. ENCODER TIMING

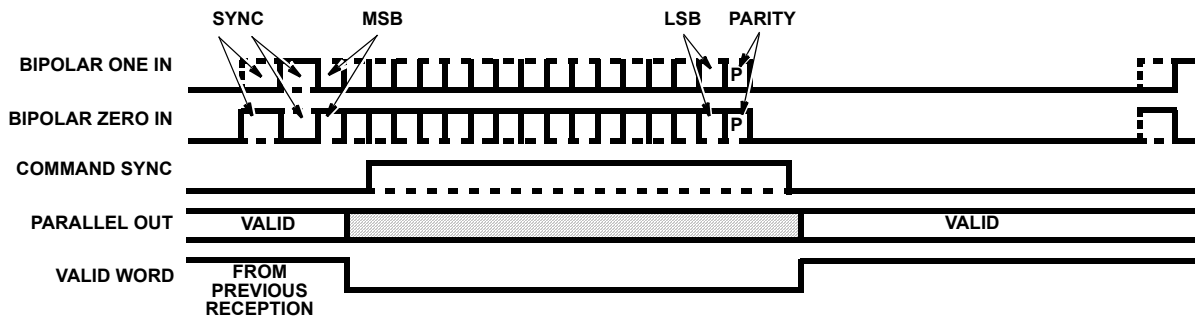


FIGURE 5. DECODER TIMING

### MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15530 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded

by a synchronizing pulse, and followed by parity bit, occupying a total of 20µs. The word formats are shown in Figure 4. The special abbreviations are as follows:

- P Parity, which is defined to be odd, taken across all 17 bits.
- R/T Receive on logical zero, transmit on ONE.
- ME Message Error if logical 1.
- TF Terminal Flat, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

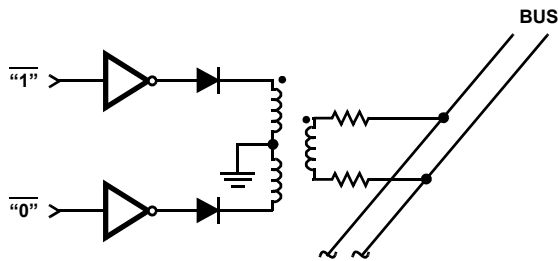


FIGURE 6. SIMPLIFIED MIL-STD-1553 DRIVER

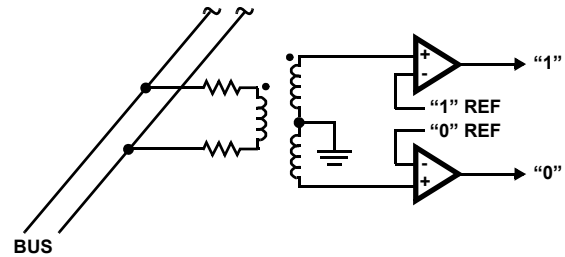


FIGURE 7. SIMPLIFIED MIL-STD-1553 RECEIVER

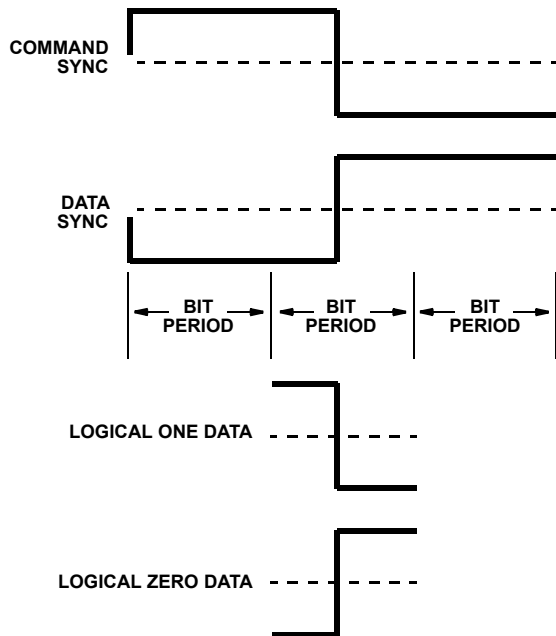


FIGURE 8. MIL-STD-1553 CHARACTER FORMATS

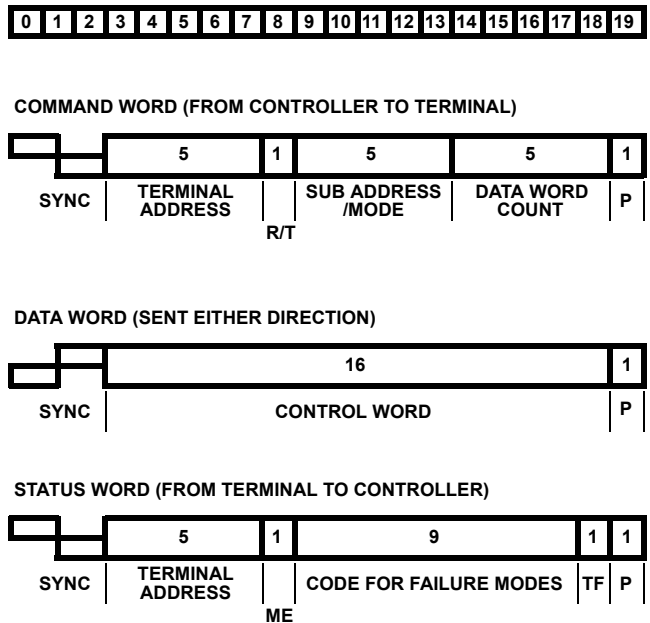


FIGURE 9. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15530.

**Absolute Maximum Ratings**

Supply Voltage ..... +7.0V  
 Input, Output or I/O Voltage ..... GND-0.3V to V<sub>CC</sub> +0.3V  
 ESD Classification ..... Class 1

**Operating Conditions**

Supply Voltage ..... +4.5V to +5.5V  
 Temperature Range (T<sub>A</sub>)  
     HD-15530-9 ..... -40°C to +85°C  
     HD-15530-8 ..... -55°C to +125°C  
 Encoder/Decoder Clock Rise Time ..... 8ns Max  
 Encoder/Decoder Clock Fall Time ..... 8ns Max  
 Sync Transition Span (TD2) ..... 18 TDC Typ (Note 1)  
 Short Data Transition Span (TD4) ..... 6 TDC Typ (Note 1)  
 Long Data Transition Span (TD5) ..... 12 TDC Typ (Note 1)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**Thermal Information**

Thermal Resistance (Typical)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)
CERDIP Package	55	12
CLCC Package	65	14
Plastic DIP Package	60	N/A
Maximum Junction Temperature		
Ceramic Package		+175°C
Plastic Package		150°C
Maximum Storage Temperature Range		-65°C to +150°C
Maximum Lead Temperature (Soldering 10s)		+300°C

**Die Characteristics**

Gate Count ..... 456 Gates

**DC Electrical Specifications** V<sub>CC</sub> = 5V ±10%, T<sub>A</sub> = -40°C to +85°C (HD-15530-9)  
 T<sub>A</sub> = -55°C to +125°C (HD-15530-8)

PARAMETER	SYMBOL	LIMITS		TEST CONDITIONS	UNITS
		MIN	MAX		
Input LOW Voltage	V <sub>IL</sub>	-	0.2 V <sub>CC</sub>	V <sub>CC</sub> = 4.5V and 5.5V	V
Input HIGH Voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>	-	V <sub>CC</sub> = 4.5V and 5.5V	V
Input LOW Clock Voltage	V <sub>ILC</sub>	-	GND +0.5	V <sub>CC</sub> = 4.5V and 5.5V	V
Input HIGH Clock Voltage	V <sub>IHC</sub>	V <sub>CC</sub> -0.5	-	V <sub>CC</sub> = 4.5V and 5.5V	V
Output LOW Voltage	V <sub>OL</sub>	-	0.4	I <sub>OL</sub> = 1.8mA (Note 2), V <sub>CC</sub> = 4.5V	V
Output HIGH Voltage	V <sub>OH</sub>	2.4	-	I <sub>OH</sub> = -3mA (Note 2), V <sub>CC</sub> = 4.5V	V
Input Leakage Current	I <sub>I</sub>	-1.0	+1.0	V <sub>I</sub> = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V	µA
Standby Supply Current	I <sub>CCSB</sub>	-	2	V <sub>IN</sub> = V <sub>CC</sub> = 5.5V Output Open	mA
Operating Power Supply Current	I <sub>CCOP</sub>	-	10	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = V <sub>CC</sub> , f = 15MHz, Outputs Open	mA
Function Test	F <sub>T</sub>	-	-	(Note 3)	-

NOTES:

1. TDC = Decoder clock period = 1/FDC
2. Interchanging of force and sense conditions is permitted.
3. Tested as follows: f = 15MHz, V<sub>IH</sub> = 70% V<sub>CC</sub>, V<sub>IL</sub> = 20% V<sub>CC</sub>, C<sub>L</sub> = 50pF, V<sub>OH</sub> ≥ 1.5V and V<sub>OL</sub> ≤ 1.5V.

**Capacitance** T<sub>A</sub> = +25°C; Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C <sub>IN</sub>	Input Capacitance	15	pF	All measurements are referenced to device GND
C <sub>O</sub>	Output Capacitance	15	pF	

**AC Electrical Specifications**  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  (HD-15530-9)  
 $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  (HD-15530-8)

PARAMETER	SYMBOL	(NOTE 2) TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
<b>ENCODER TIMING</b>					
Encoder Clock Frequency	FEC	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	15	MHz
Send Clock Frequency	FESC	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	2.5	MHz
Encoder Data Rate	FED	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	1.25	MHz
Master Reset Pulse Width	TMR	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	150	-	ns
Shift Clock Delay	TE1	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	125	ns
Serial Data Setup	TE2	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	75	-	ns
Serial Data Hold	TE3	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	75	-	ns
Enable Setup	TE4	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	90	-	ns
Enable Pulse Width	TE5	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	100	-	ns
Sync Setup	TE6	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	55	-	ns
Sync Pulse Width	TE7	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	150	-	ns
Send Data Delay	TE8	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	0	50	ns
Bipolar Output Delay	TE9	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	130	ns
Enable Hold	TE10	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	10	-	ns
Sync Hold	TE11	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	95	-	ns
<b>DECODER TIMING</b>					
Decoder Clock Frequency	FDC	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	15	MHz
Decoder Data Rate	FDD	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	1.25	MHz
Decoder Reset Pulse Width	TDR	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	150	-	ns
Decoder Reset Setup Time	TDRS	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	75	-	ns
Decoder Reset Hold Time	TDRH	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	10	-	ns
Master Reset Pulse	TMR	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	150	-	ns
Bipolar Data Pulse Width	TD1	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	TDC + 10 (Note 1)	-	ns
One Zero Overlap	TD3	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	TDC - 10 (Note 1)	ns
Sync Delay (ON)	TD6	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-20	110	ns
Take Data Delay (ON)	TD7	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	0	110	ns
Serial Data Out Delay	TD8	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	-	80	ns
Sync Delay (OFF)	TD9	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	0	110	ns
Take Data Delay (OFF)	TD10	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	0	110	ns
Valid Word Delay	TD11	$V_{CC} = 4.5V$ and $5.5V$ , $C_L = 50pF$	0	110	ns

## NOTES:

1. TDC = Decoder clock period =  $1/FDC$
2. AC Testing as follows: Input levels:  $V_{IH} = 70\% V_{CC}$ ,  $V_{IL} = 20\% V_{CC}$ ; Input rise/fall times driven at  $1ns/V$ ; Timing Reference levels:  $1.5V$ ; Output load:  $C_L = 50pF$ .



### Timing Waveforms

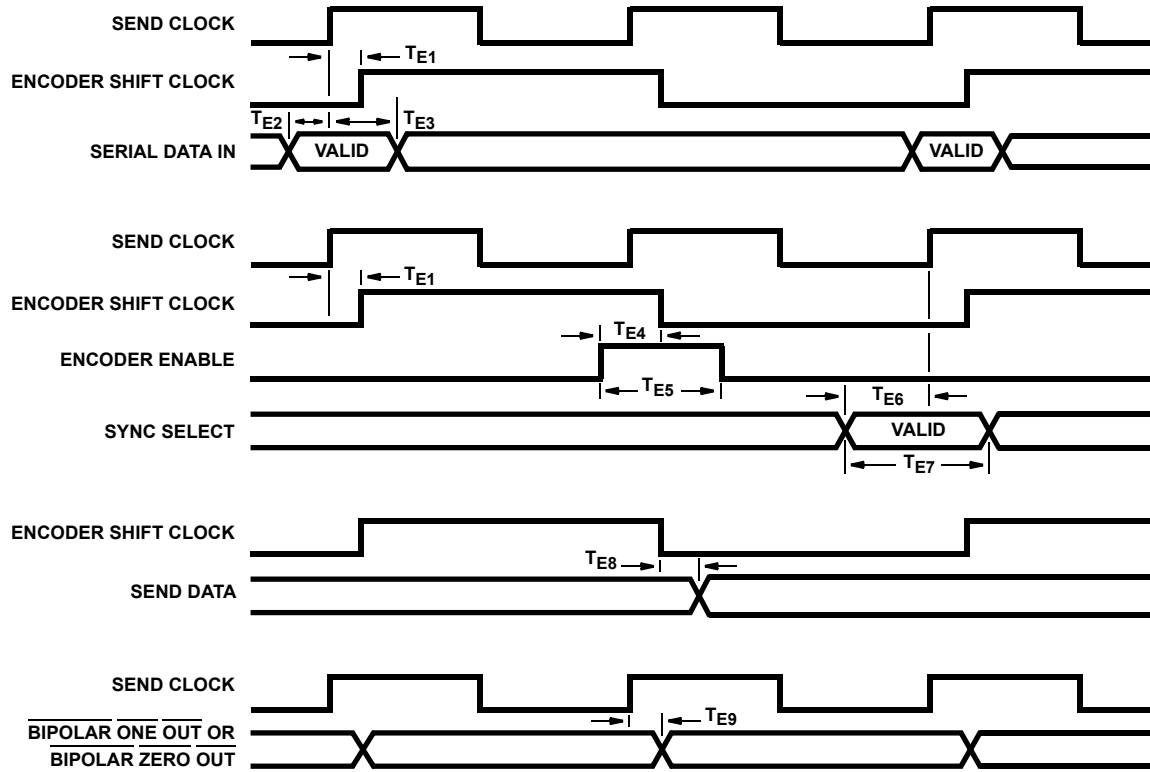


FIGURE 10. ENCODER TIMING

**Timing Waveforms** (Continued)

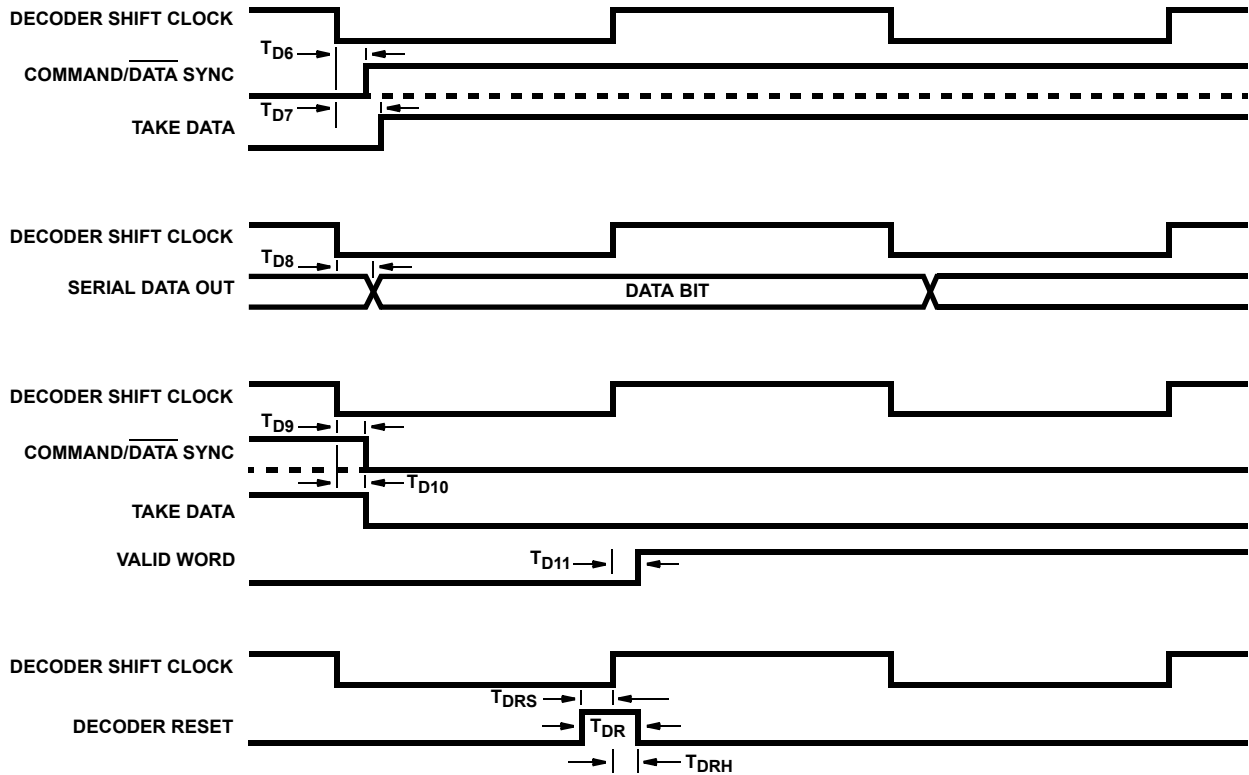


FIGURE 11. DECODER TIMING

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**Timing Waveforms** (Continued)

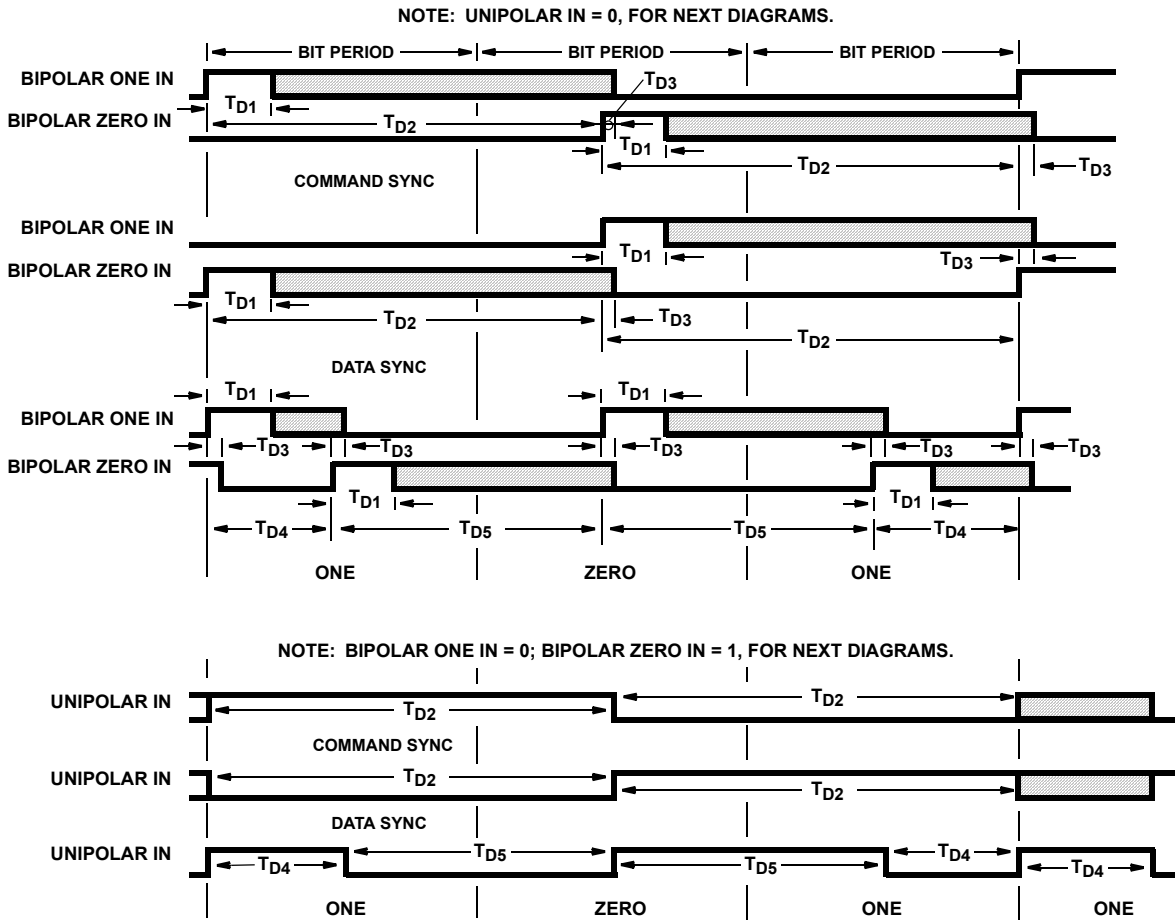
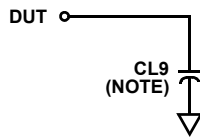


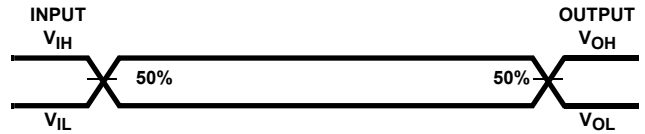
FIGURE 12. DECODER TIMING

**Test Load Circuit**



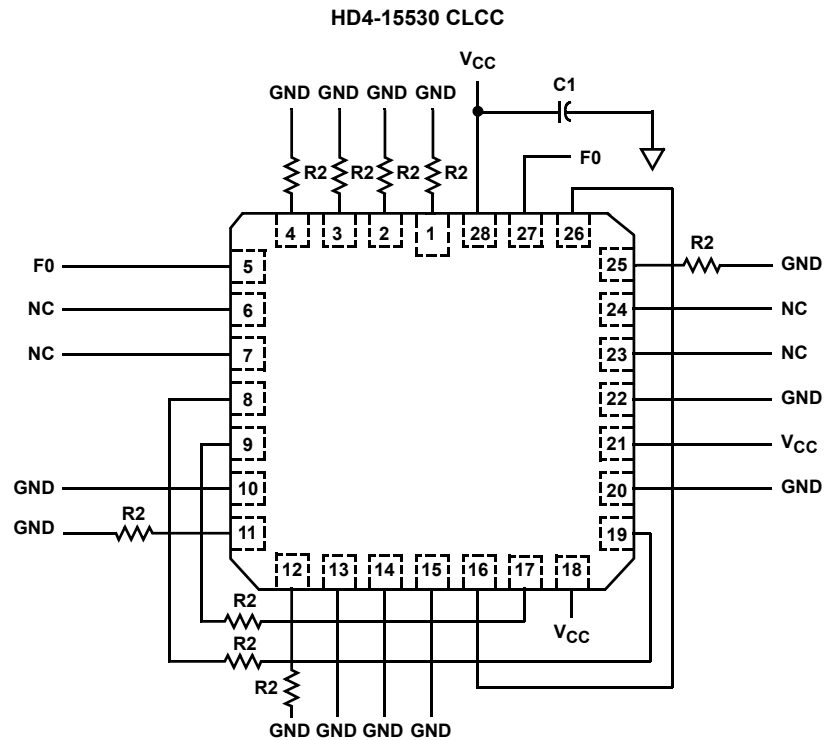
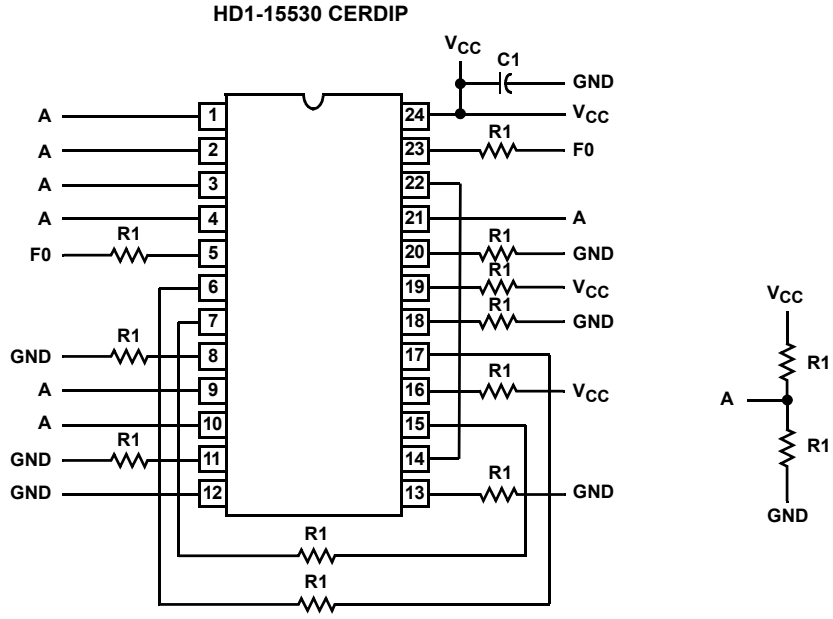
NOTE: Includes stray and jig capacitance.

**AC Testing Input, Output Waveform**



AC Testing: All input signals must switch between  $V_{IL}$  and  $V_{IH}$ . Input rise and fall times are driven at 1ns per volt.

**Burn-In Circuits**



- NOTES:
1.  $V_{CC} = 5.5V \pm 0.5V$
  2.  $V_{IH} = 4.5V \pm 10\%$
  3.  $V_{IL} = -0.2V + 0.4V$
  4.  $R1 = 47K\Omega \pm 5\%$
  5.  $R2 = 1.8K\Omega \pm 5\%$
  6.  $F0 = 100KHz \pm 10\%$
  7.  $C1 = 0.01\mu F$  Min.

## Die Characteristics

**DIE DIMENSIONS:**

155 x 195 x 19mils

**METALLIZATION:**

Type: Si-Al

Thickness: 11kÅ ±2kÅ

**GLASSIVATION:**

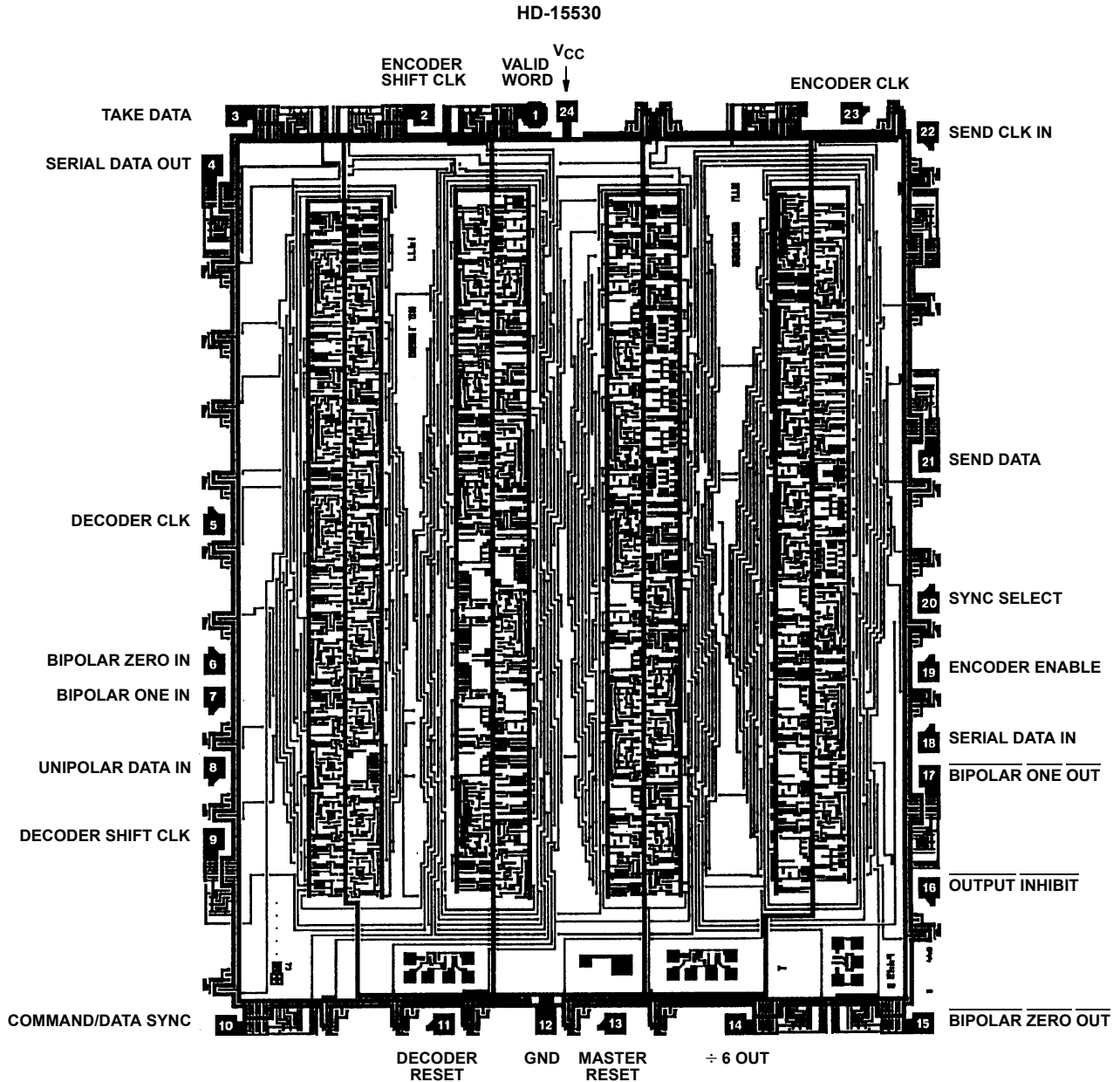
Type: SiO<sub>2</sub>

Thickness: 8kÅ ±1kÅ

**WORST CASE CURRENT DENSITY:**

1.8 x 10<sup>5</sup> A/cm<sup>2</sup>

## Metallization Mask Layout



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