IV1Q12080T4Z – 1200V 80mΩ Automotive SiC MOSFET

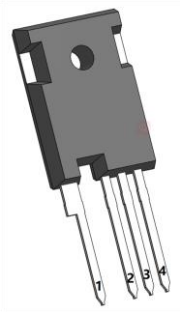
Features

- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin gate input easing driver circuit design
- AEC-Q101 qualified

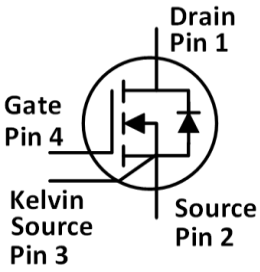
Applications

- On-board chargers
- Automotive compressor inverters
- Automotive DC/DC
- Solar inverters
- Switch mode power supplies

Outline:



TO247-4



RoHS COMPLIANT

HF

Marking Diagram:

1Q12080T4Z
YYWWZ
XXXX

1Q12080T4Z= Specific Device Code
YY = Year
WW = Work Week
Z = Assembly Location
XXXX = Lot Traceability

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	1200	V	V_{GS}=0V, I_D=100μA	
V_{GSmax} (DC)	Maximum DC voltage	-5 to 22	V	Static (DC)	
V_{GSmax} (Spike)	Maximum spike voltage	-10 to 25	V	<1% duty cycle, and pulse width<200ns	
V_{GSon}	Recommended turn-on voltage	20±0.5	V		
V_{GSoff}	Recommended turn-off voltage	-3.5 to -2	V		
I_D	Drain current (continuous)	42	A	V_{GS}=20V, T_C=25°C	Fig. 21
		31	A	V_{GS}=20V, T_C=100°C	
I_{DM}	Drain current (pulsed)	70	A	Pulse width limited by SOA	Fig. 24
P_{TOT}	Total power dissipation	300	W	T_C=25°C	Fig. 22
T_{stg}	Storage temperature range	-55 to 175	°C		
T_J	Operating junction temperature	-55 to 175	°C		
T_L	Solder Temperature	260	°C	wave soldering only allowed at leads, 1.6mm from case for 10 s	

Thermal Data

Symbol	Parameter	Value	Unit	Note
$R_{\theta(J-C)}$	Thermal Resistance from Junction to Case	0.5	°C/W	Fig. 23

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		5	100	μA	V_{DS}=1200V, V_{GS}=0V	
I_{GSS}	Gate leakage current			±100	nA	V_{DS}=0V, V_{GS}=-5~20V	
V_{TH}	Gate threshold voltage	1.8	3.6	5	V	V_{GS}=V_{DS}, I_D=3.8mA	Fig. 8, 9
			2.7		V	V_{GS}=V_{DS}, I_D=3.8mA @ T_C=175°C	
R_{ON}	Static drain-source on-resistance		80	100	mΩ	V_{GS}=20V, I_D=10A @T_J=25°C	Fig. 4, 5, 6, 7
			130		mΩ	V_{GS}=20V, I_D=10A @T_J=175°C	
C_{iss}	Input capacitance		1680		pF	V_{DS}=800V, V_{GS}=0V, f=1MHz, V_{AC}=25mV	Fig. 16
C_{oss}	Output capacitance		69		pF		
C_{rss}	Reverse transfer capacitance		6.7		pF		
E_{oss}	C_{oss} stored energy		27		μJ		Fig. 17
Q_g	Total gate charge		76		nC	V_{DS}=800V, I_D=20A, V_{GS}=-5 to 20V	Fig. 18
Q_{gs}	Gate-source charge		29		nC		
Q_{gd}	Gate-drain charge		34		nC		
R_g	Gate input resistance		4.2		Ω	f=1MHz	
E_{ON}	Turn-on switching energy		154		μJ	V_{DS}=800V, I_D=20A, V_{GS}=-3.5 to 20V, $R_{G(ext)}$=2.0Ω, L=290μH	Fig. 19, 20
E_{OFF}	Turn-off switching energy		80		μJ		
$t_{d(on)}$	Turn-on delay time		8.9		ns		
t_r	Rise time		19.9				
$t_{d(off)}$	Turn-off delay time		14.7				
t_f	Fall time		9.5				

Reverse Diode Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		4.7		V	I_{SD}=10A, V_{GS}=0V	Fig. 10, 11, 12
			4.2		V	I_{SD}=10A, V_{GS}=0V, T_J=175°C	
t_{rr}	Reverse recovery time		10.2		ns	V_{GS}=0V, I_{SD}=20A, V_R=800V, di/dt=1100A/μs	
Q_{rr}	Reverse recovery charge		64		nC		
I_{RRM}	Peak reverse recovery current		11.3		A		

Typical Performance (curves)

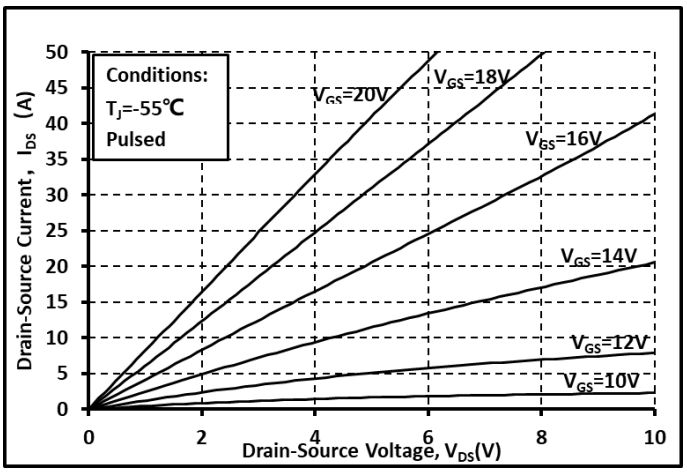


Fig. 1 Output Curve @ T_J=-55℃

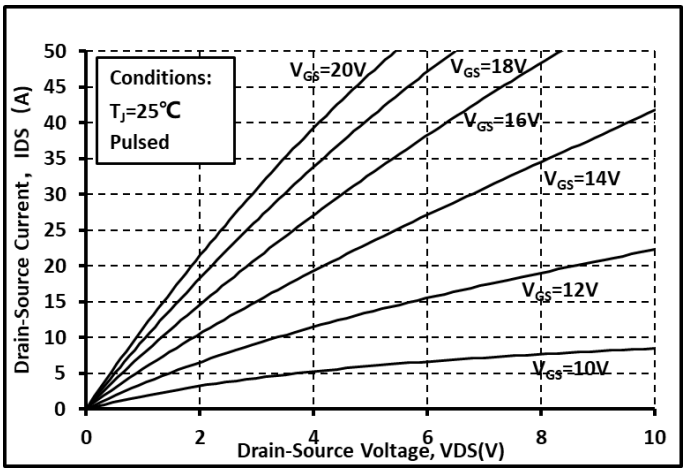


Fig. 2 Output Curve @ T_J=25℃

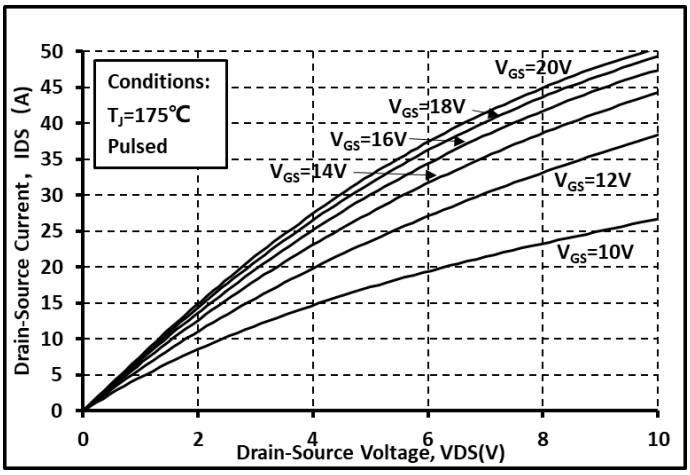


Fig. 3 Output Curve @ T_J=175℃

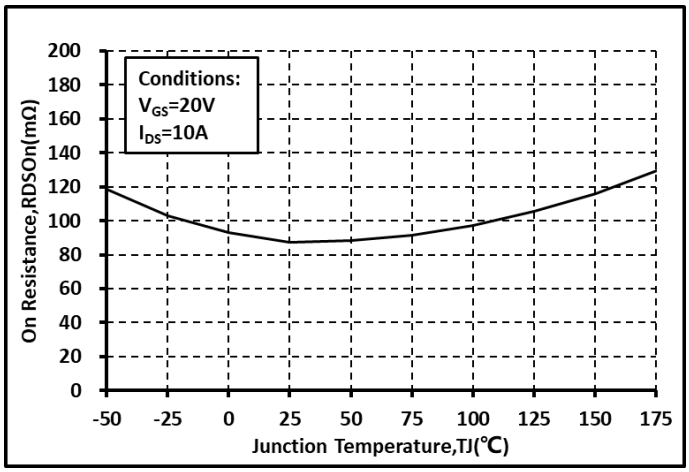


Fig. 4 Ron vs. Temperature

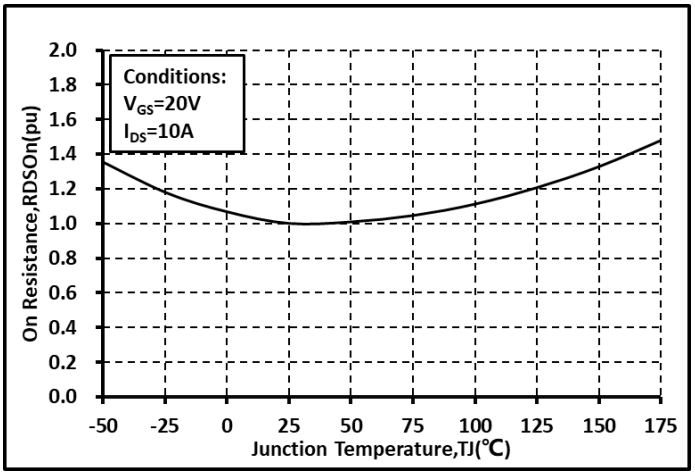


Fig. 5 Normalized Ron vs. Temperature

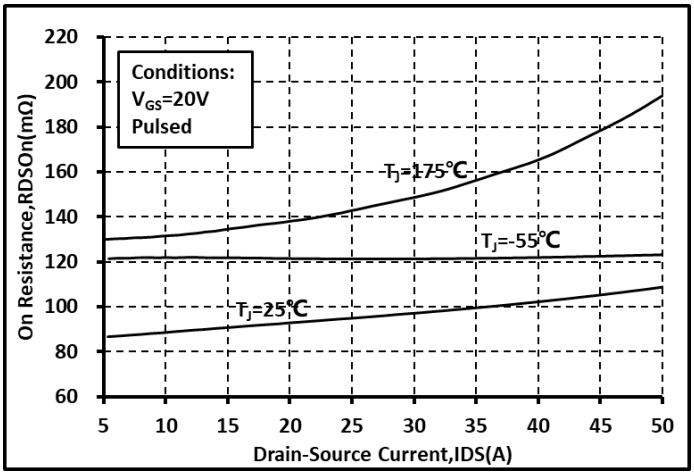


Fig. 6 Ron vs. I_{DS} @ Various Temperature

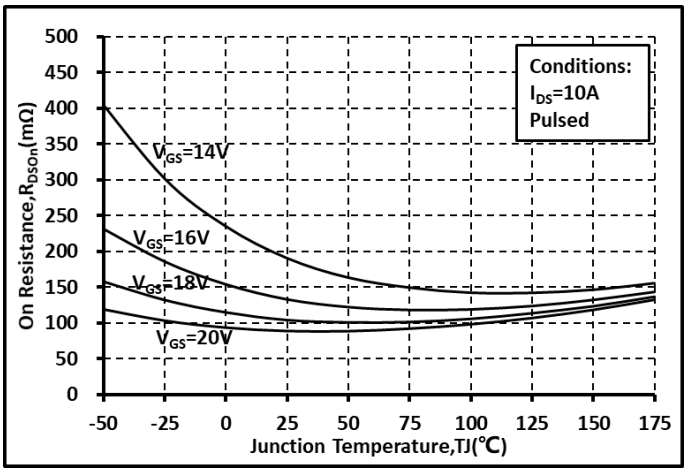


Fig. 7 Ron vs. Temperature @ Various V_{GS}

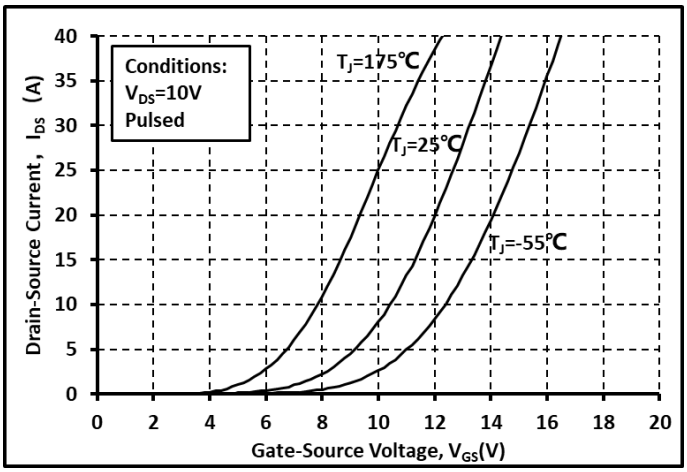


Fig. 8 Transfer Curves @ Various Temperature

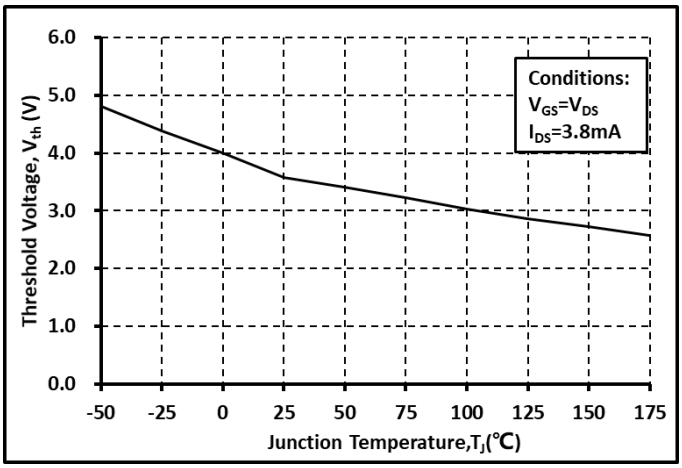


Fig. 9 Threshold Voltage vs. Temperature

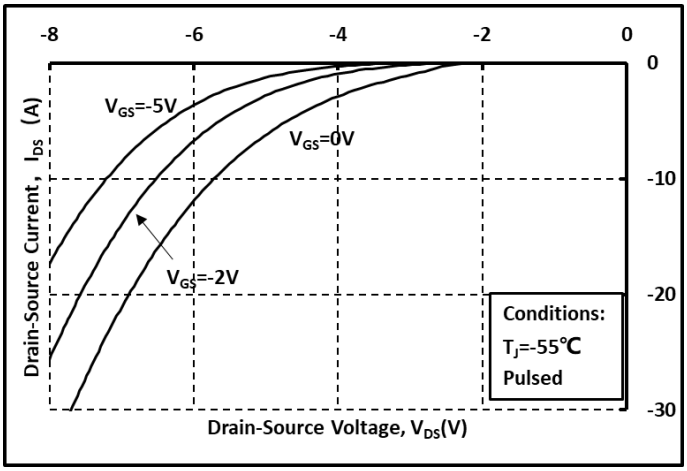


Fig. 10 Body Diode curves @ T_J=-55°C

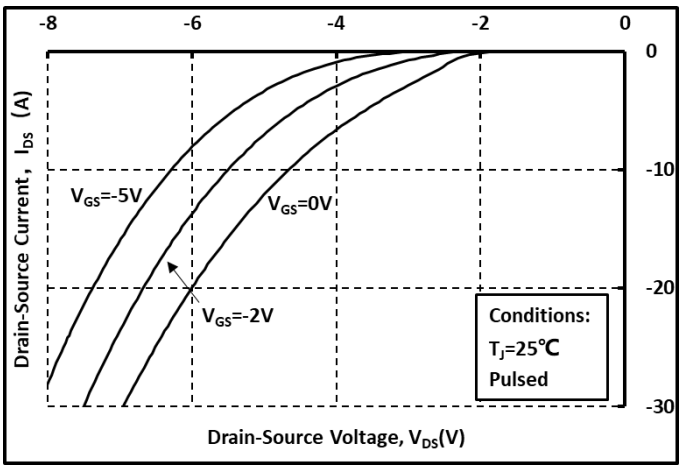


Fig. 11 Body Diode curves @ T_J=25°C

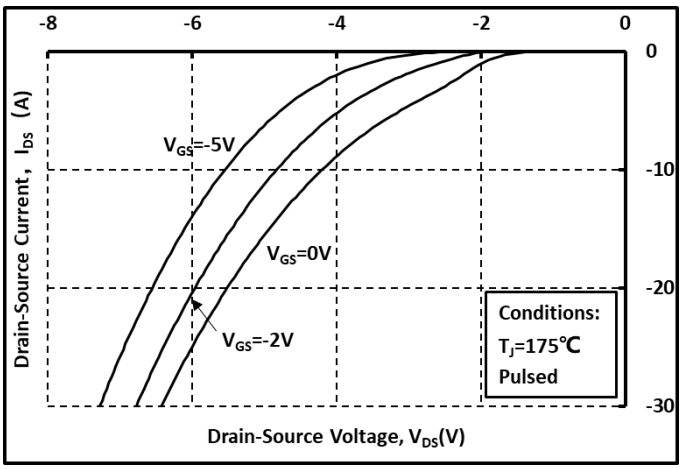


Fig. 12 Body Diode curves @ T_J=175°C

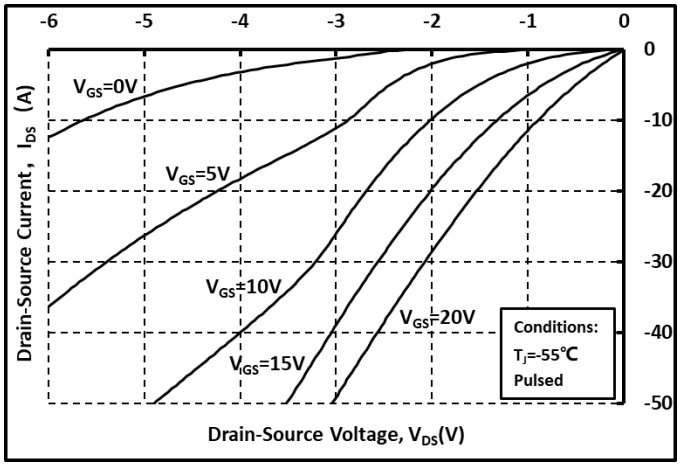


Fig. 13 3rd Quadrant curves @ T_J=-55°C

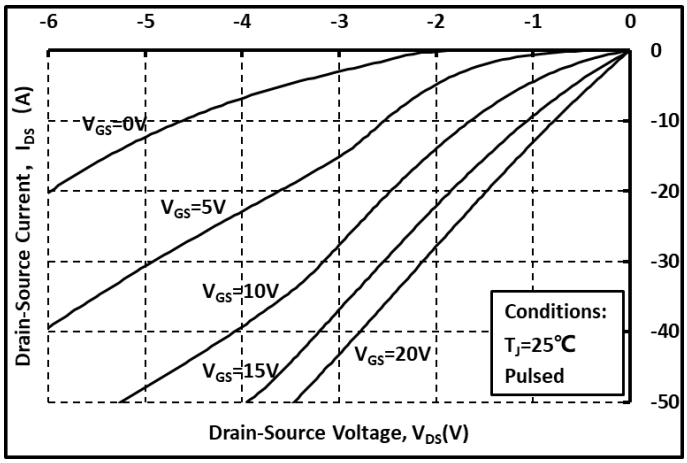


Fig. 14 3rd Quadrant curves @ T_J=25°C

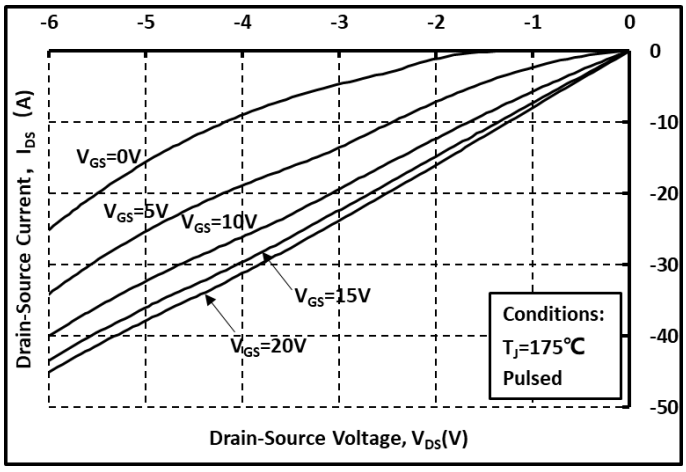


Fig. 15 3rd Quadrant curves @ T_J=175°C

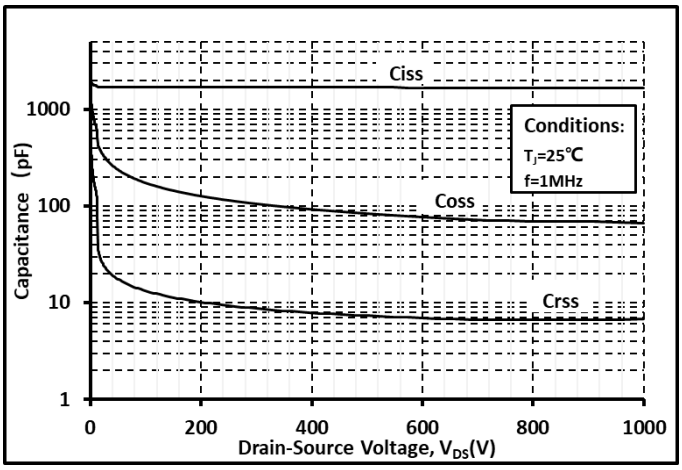


Fig. 16 Capacitance vs. V_{DS}

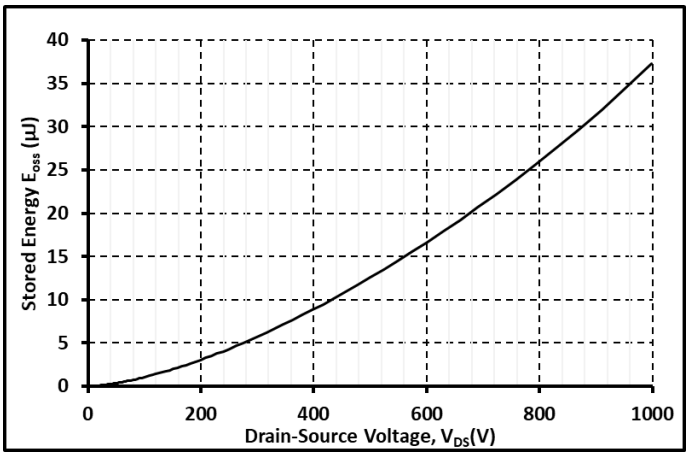


Fig. 17 Output Capacitor Stored Energy

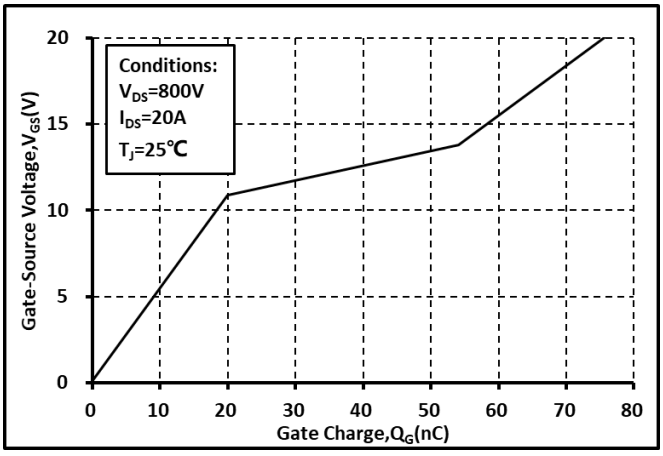


Fig. 18 Gate Charge Characteristics

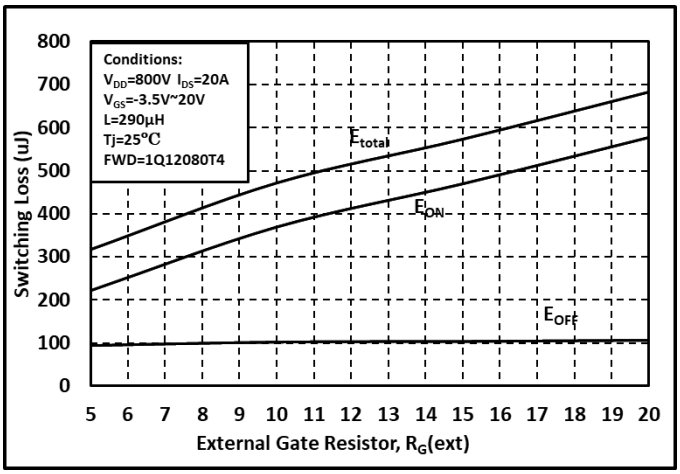


Fig. 19 Switching Energy vs. $R_{G(ext)}$

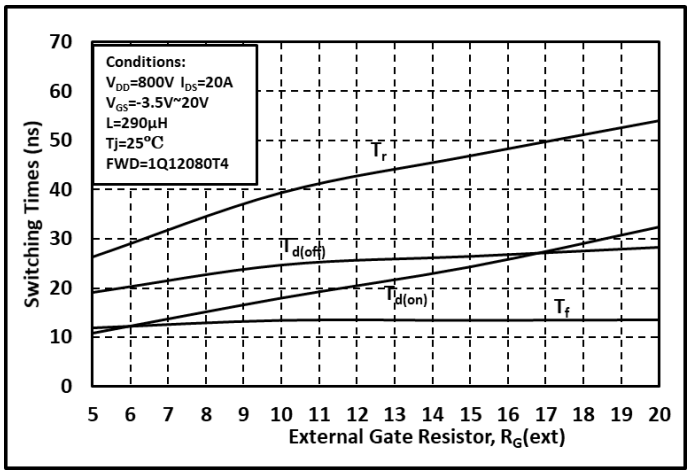


Fig. 20 Switching Times vs. $R_{G(ext)}$

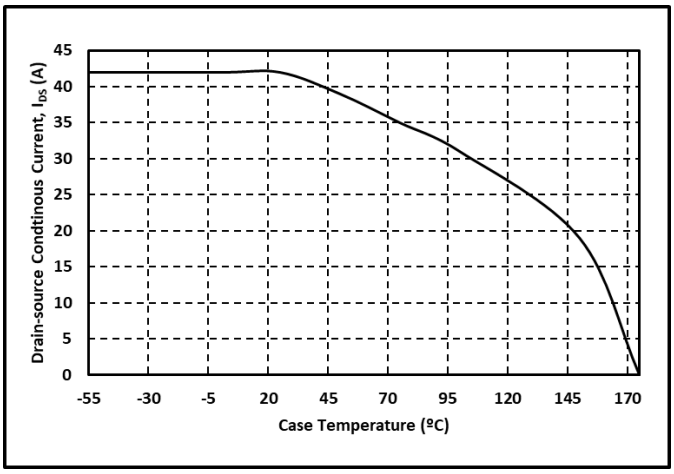


Fig. 21 Continuous Drain Current vs. Case Temperature

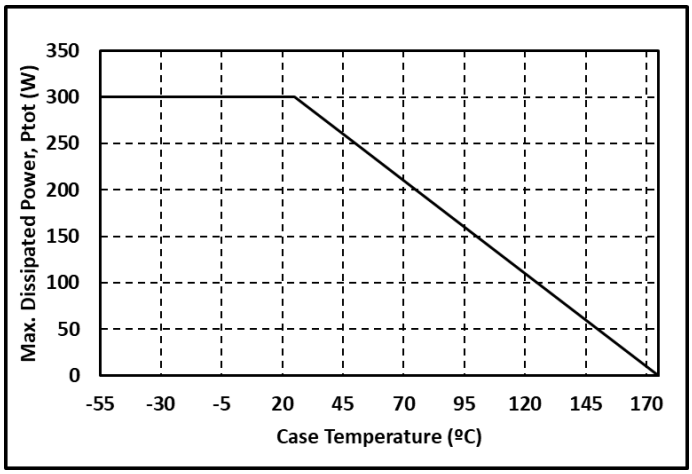


Fig. 22 Max. Power Dissipation Derating vs. Case Temperature

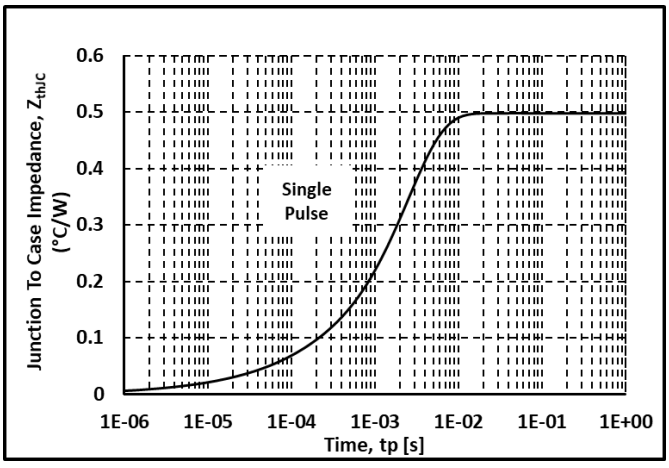


Fig. 23 Thermal impedance

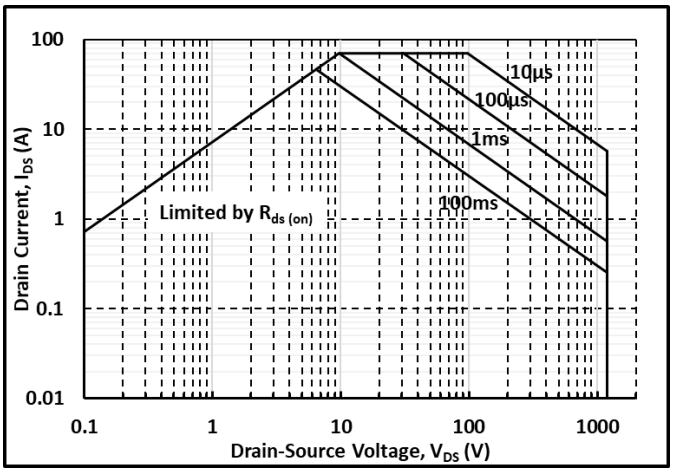
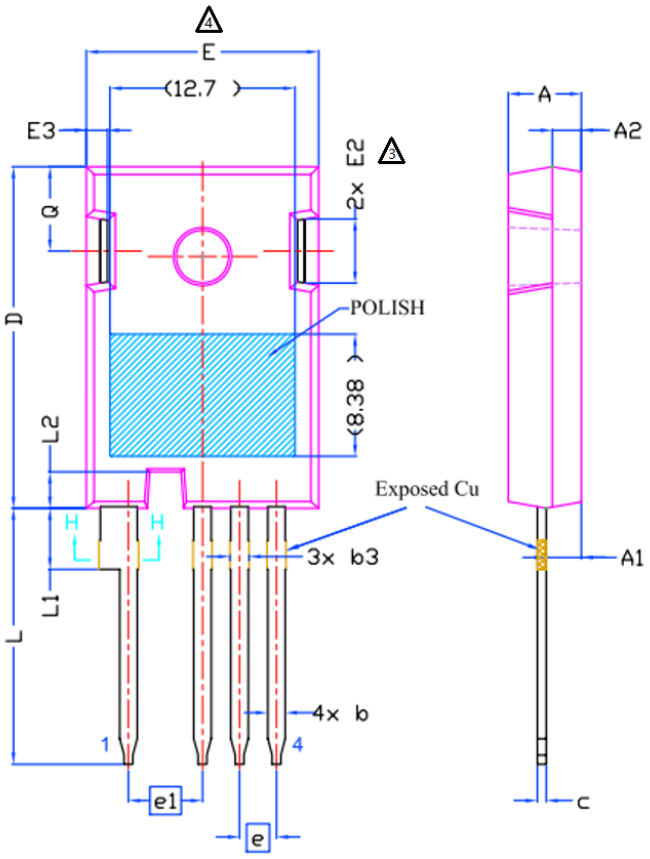
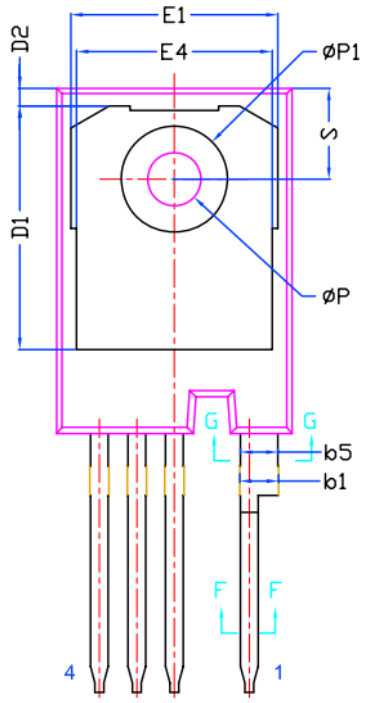


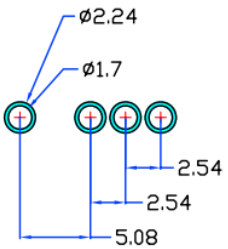
Fig. 24 Safe Operating Area

Package Dimensions

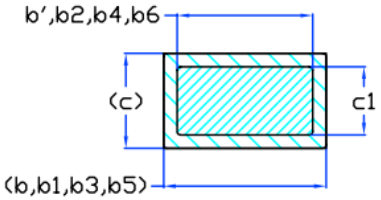


Dimensions In Millimeters		
SYMBOL	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b'	1.07	1.28
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
c	0.55	0.68
c1	0.55	0.65
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
N	4	
ϕP	3.51	3.65
ϕP1	7.18 REF.	
Q	5.49	6
S	6.04	6.3





Recommended Solder Pad Layout



Section F--F, G--G, H--H

Note:

1. Package Reference: JEDEC TO247, Variation AD
2. All Dimensions are in mm
3. Slot Required, Notch May Be Rounded
4. Dimension D&E Do Not Include Mold Flash
5. Subject to Change Without Notice

Notes

For further information please contact IVCT's office.

The Information in this document is subject to change without notice.

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