IVCO1A01/2 10A Isolated Single Channel Gate Driver

1. Features

- Split Outputs (IVCO1A01) or Miller Clamp (IVCO1A02)
- Industry standard SOIC-8 pinout supports 3.75kVrms isolation voltage with Narrow Body (D) and 5.7kVrms isolation voltage with Wide Body (DW) options
- 10A peak source and sink drive current
- Wide driver VCC2 range up to 36V
- VCC2 UVLO protection
  - 8.4V UVLO (IVCO1A01)
  - 12V UVLO (IVCO1A02)
- 100V/ns minimum CMTI
- CMOS inputs
- 50ns typical propagation delays
- Outputs held low when floating inputs
- Safety and regulatory certifications:
  - UL (pending)
  - VDE (pending)
  - CQC (pending)
- Operating temperature range -40°C to 125°C

2. Applications

- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- UPS
- Motor Control
- Emerging Wide Band-Gap Power Devices

3. Description

The IVCO1A01/2 is a 10A single-channel isolated gate driver with 3.75kVrms (D) and 5.7kVrms (DW) isolation. It is capable of effectively and safely driving SiC/Si MOSFETs and Si IGBTs. Low propagation delay and compact SOIC-8 package enables MOSFETs to switch at hundreds of kHz.

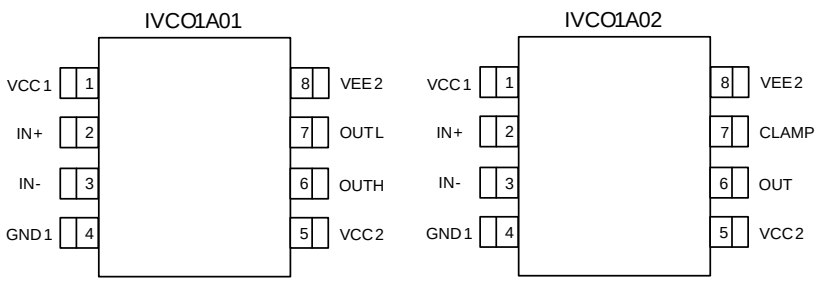
Wide output VCC2 operating range from 9.5V to 33V enables effective driving with Si or SiC MOSFET and IGBT power switches. Integrated UVLO protection ensures output held at low under abnormal conditions. The input VCC1 operates from 2.5V to 5.5V, which supports most digital controllers.

With integrated isolation barrier, IVCO1A01/2 can support isolation up to 3.75kVrms (D) and 5.7kVrms (DW). It is very convenient to control MOSFET/IGBT gate drive across isolation barrier or with level shifting.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCO1A01DR	NB SOIC-8	Tape and Reel
IVCO1A01DWR	WB SOIC-8	Tape and Reel
IVCO1A02DR	NB SOIC-8	Tape and Reel
IVCO1A02DWR	WB SOIC-8	Tape and Reel

Pin Configuration



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4. Pin Configuration and Functions

IVCO1A01	IVCO1A02	NAME	I/O	DESCRIPTION
1	1	VCC1	P	Input Power Supply
2	2	IN+	I	Positive Input
3	3	IN-	I	Negative Input
4	4	GND1	G	Input Ground
5	5	VCC2	P	Output Power Supply
6	/	OUTH	O	Pull High Output
7	/	OUTL	O	Pull Low Output
/	6	OUT	O	Output
/	7	CLAMP	I/O	Active Miller Clamp
8	8	VEE2	G	Output Ground

Truth Table

VCC1	IN+	IN-	VCC2	OUTH (IVCO1A01)	OUTL (IVCO1A01)	OUT (IVCO1A02)
X	X	X	below UVLO	High impedance	L	L
below UVLO	X	X	X	High impedance	L	L
above UVLO	L or floating	X	above UVLO	High impedance	L	L
above UVLO	X	H or floating	above UVLO	High impedance	L	L
above UVLO	H	L	above UVLO	H	High impedance	H

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC1}	Input supply voltage (reference to GND1)	-0.3	7	V
IN+, IN-	Signal input voltage	-0.3	V_{CC1}+0.3	V
V_{CC2}	Output supply voltage (reference to VEE2)	-0.3	36	V
OUTH, OUTL	Gate driver output voltage	-0.3	V_{CC2}+0.3	V
OUT	Gate driver output voltage	-0.3	V_{CC2}+0.3	V
CLAMP	Miller Clamp input voltage	-0.3	V_{CC2}+0.3	
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-2000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{CC1}	Input supply voltage	2.5	5.5	V
V_{INx}	Input voltage	0	V_{CC1}	V
V_{CC2}	Output supply voltage	9.5	33	V
T_A	Ambient temperature	-40	125	°C

5.4 Thermal Information

		D	DW	UNIT
$R_{\theta JA}$	Junction-to-Ambient	110	100	°C/W
ψ_{JT}	Junction-to-Top characterization parameter	18	16	°C/W

5.5 Electrical Specifications

Unless otherwise noted, V_{CC1} = 3.3 V, V_{CC2} = 15 V, T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT					
I_{CC1q} V_{CC1} quiescent current	IN+=0V, IN-=5V, output logic LOW.		0.3	0.5	mA
I_{CC2q} V_{CC2} quiescent current	IN+=0V, IN-=5V, output logic LOW.		1.6	2.5	mA
UVLO (VCC1)					
V_{ON}	VCC1 Rising threshold	2.0	2.2	2.4	V
V_{OFF}	VCC1 Falling threshold	1.9	2.07	2.25	V
IVCO1A01 UVLO (VCC2)					
V_{ON} Under voltage	VCC2 Rising threshold		8.4	9.2	V
V_{OFF} thresholds	VCC2 Falling threshold	7.2	7.8		V
IVCO1A02 UVLO (VCC2)					
V_{ON}	VCC2 Rising threshold		12		V
V_{OFF}	VCC2 Falling threshold		11		V
INPUT					
V_{INH} Input rising threshold			0.5*V_{CC1}	0.6*V_{CC1}	V
V_{INL} Input falling threshold		0.3*V_{CC1}	0.35*V_{CC1}		V
OUTPUTS					
I_{PK} (*) Peak source and sink currents	C_{LOAD} = 0.22uF, with external current limiting resistors, 1kHz switching frequency		10		A
V_{OH} Output high voltage	I_{OUTH} = -20mA		V_{CC2}-0.1	V_{CC2}-0.2	V
V_{OL} Output low voltage	I_{OUTL} = 20mA		8		V
R_{OH} Output static pull-up resistance			5	10	Ω
R_{OL} Output pull-down resistance			0.4		Ω
IVCO1A02 ACTIVE MILLER CLAMP					
I_{CLAMP} (*) Clamp current	VCLAMP = VEE2+2V		10		A
V_{CLAMP} Clamp low voltage	I_{CLAMP} = 20mA		7		V
$V_{CLAMP-TH}$ Clamp threshold voltage			2.1		V
Timing					
TD_r Output rising delay TD_f Output falling delay	C_{LOAD} = 1.8nF		50 50	65 65	ns
T_r Rise time T_f Fall time	C_{LOAD} = 1.8nF		7 6		ns
T_{PWD} Pulse Width Distortion	C_{LOAD} = 1.8nF		1		ns
CMTI (*)		100			V/ns
ACTIVE PULLDOWN					
V_{OPD} Active Pull Down	I_{OUT} = 0.1*I_{OUTL} , V_{CC2}=open		2	2.5	V

(*) Guaranteed by design

5.6 Insulation and Safety Related Specifications

PARAMETER		TEST CONDITIONS	D	DW	UNIT
	Rated Dielectric Insulation Voltage	1-minute duration	3750	5000	V_{RMS}
CLR	External Clearance	Measured from input terminals to output terminals, shortest distance through air	≥4	≥8	mm
CPG	External Creepage	Measured from input terminals to output terminals, shortest distance alone body	≥4	≥8	mm
	Internal Clearance	Insulation distance through insulation	≥21	≥21	μm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	>400	>400	V
	Material Group	IEC 60664-1	II	II	
R_{IO}-R_S	Isolation Resistance (Input to Output)		10^{12}	10^{12}	Ω
C_{IO}	Barrier Capacitance (Input to Output)	Freq = 1 MHz	1.5	1.5	pF
	Installation Classification per DIN VDE 0110	For rated mains voltage < 150 VRMS	I to IV	I 至 IV	
		For rated mains voltage < 300 VRMS	I to IV	I 至 IV	
		For rated mains voltage < 600 VRMS	NA	I 至 III	
		For rated mains voltage <1000 VRMS	NA	I 至 II	
	Climatic Classification		40/125/21	40/125/21	
	Pollution Degree per DIN VDE 0110, Table 1		2	2	
V_{IORM}	Maximum Working Insulation Voltage		1200	1200	
V_{IOTM}	Maximum Transient Isolation Voltage		5300	7071	
V_{IOSM}	Maximum Surge Isolation Voltage	Basic isolation, 1.2/50 μs combination wave	5300	5000	
$V_{pd(m)}$	Input to Output Test Voltage, Method B1	V_{IORM} x 1.5 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 s, partial discharge < 5 pC	1800	1800	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method A: After Environmental Tests Subgroup 1	V_{IORM} x 1.3 = $V_{pd(m)}$, 100% production test, t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	1560	1560	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method A: After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} x 1.2 = $V_{pd(m)}$, 100% production test, t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	1440	1440	V_{PK}
T_S	Maximum Safety Temperature		150	150	°C
R_S	Isolation Resistance at T_S	V_{IO} = 500 V	> 10^9	> 10^9	Ω

5.7 Regulatory Information

Regulatory	D	DW
UL	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 3750 V_{RMS} Isolation Voltage	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5000 V_{RMS} Isolation Voltage
VDE	DIN EN IEC 60747-17 (VDE 0884-17):2021-10[2] Basic Insulation, V_{IORM}=1200 V_{PK}, V_{IOSM} = 5000 VPK	DIN EN IEC 060747-17(VDE 0884-17):2021-10[2] Basic insulation, VIORM = 1200V_{PK}, VIOSM = 5000 V_{PK}
CQC	Certified under GB4943.1-2022 Basic insulation at 557 V_{RMS} (787 V_{PK})	Certified under GB4943.1-2022 Basic insulation at 1118 V_{RMS} (1580 V_{PK}) Reinforced insulation at 557 V_{RMS} (787 V_{PK})

(1) In accordance with UL 1577, each IVCO1A0xD is proof tested by applying an insulation test voltage ⩾ 4500 V rms for 1 sec, and IVCO1A0xDW is proof tested by applying an insulation test voltage ⩾6000V rms for 1 sec.

(2) In accordance with VDE 0884-17, each IVCO1A0x is proof tested by applying an insulation test voltage ⩾ 1800V rms for 1 sec.

6. Typical Characteristics

VCC1=2.5VDC±3% or 3.3VDC±10% or 5VDC±10%, 0.1uF capacitor from VCC1 to GND1, VCC2 = 15VDC±10%, 1uF capacitor from VCC2 to VEE2, CLOAD =1nF. TA = –40°C to 125°C (Unless otherwise noted).

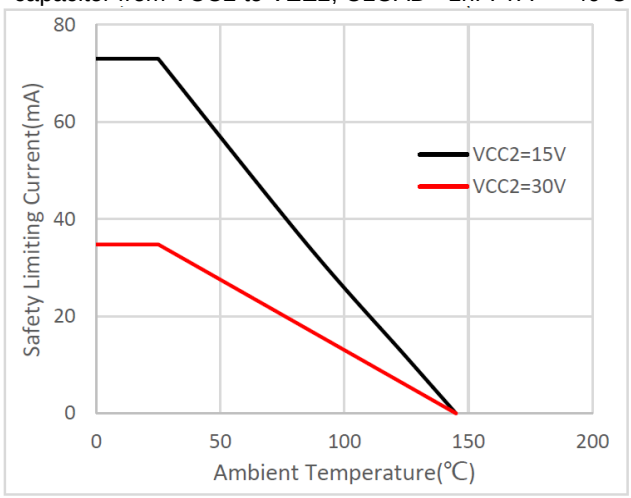


Figure 1. Thermal Derating Curve for Limiting Current with Ambient Temperature per VDE (NB SOIC-8)

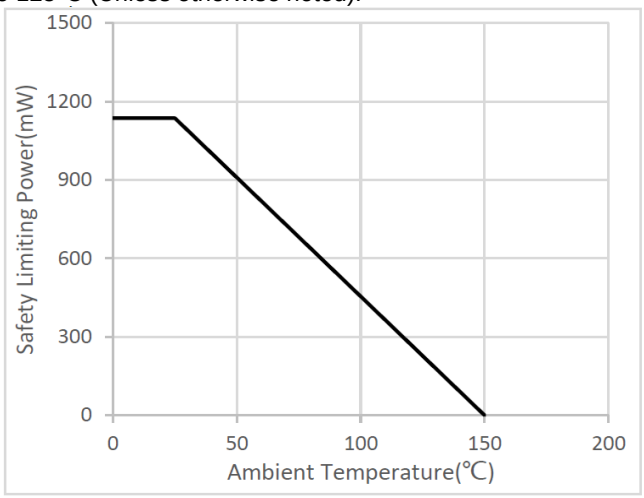


Figure 2. Thermal Derating Curve for Limiting Power with Ambient Temperature per VDE (NB SOIC-8)

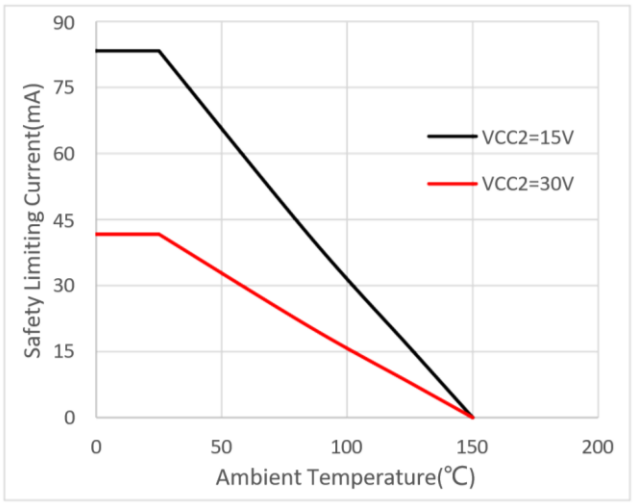


Figure 3. Thermal Derating Curve for Limiting Current with Ambient Temperature per VDE (WB SOIC-8)

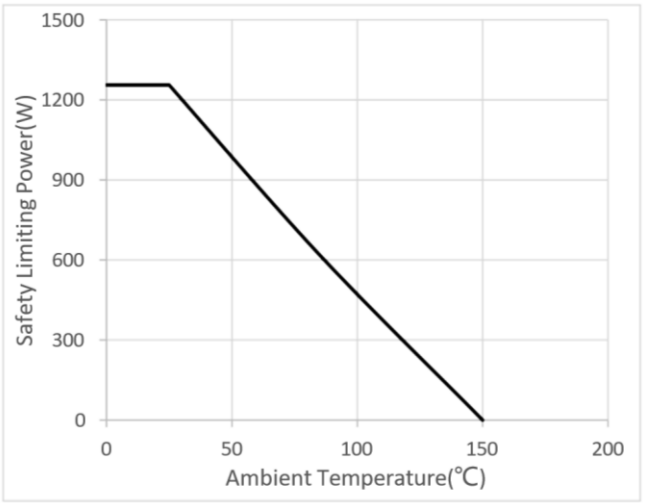


Figure 4. Thermal Derating Curve for Limiting Power with Ambient Temperature per VDE (WB SOIC-8)

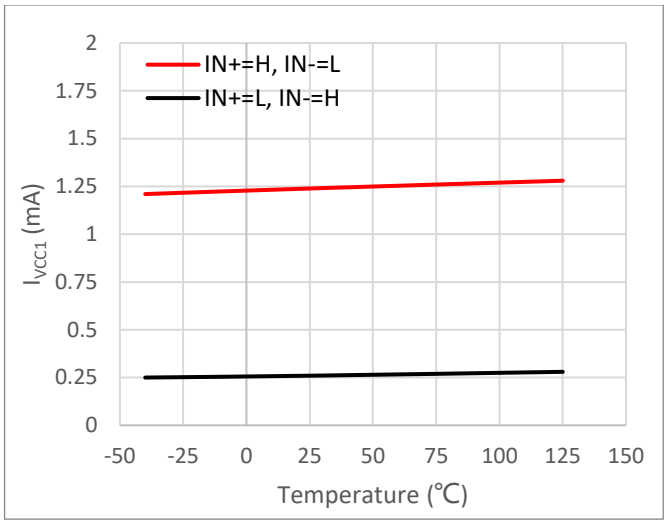


Figure 5. I_{VCC1} Supply Current vs Temperature

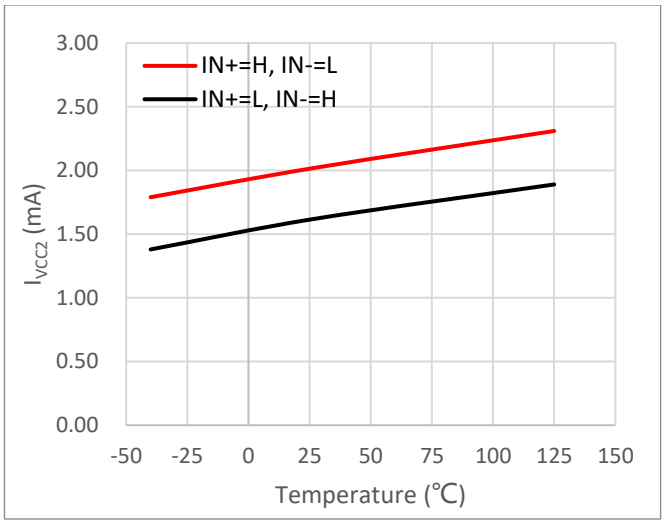


Figure 6. I_{VCC2} Supply Current vs Temperature

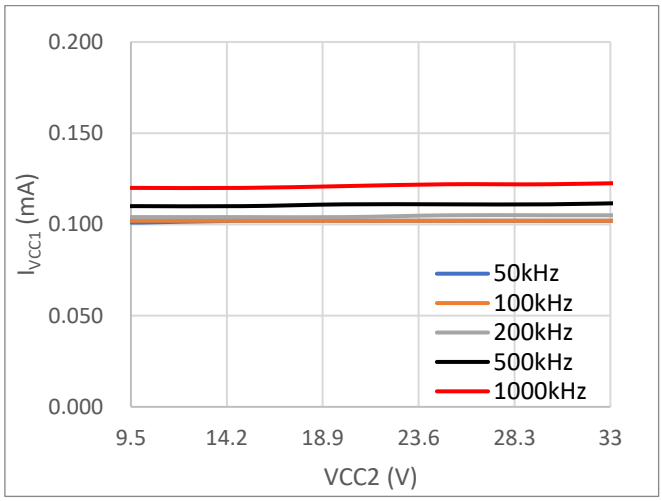


Figure 7. I_{VCC1} Supply Current vs Input Frequency

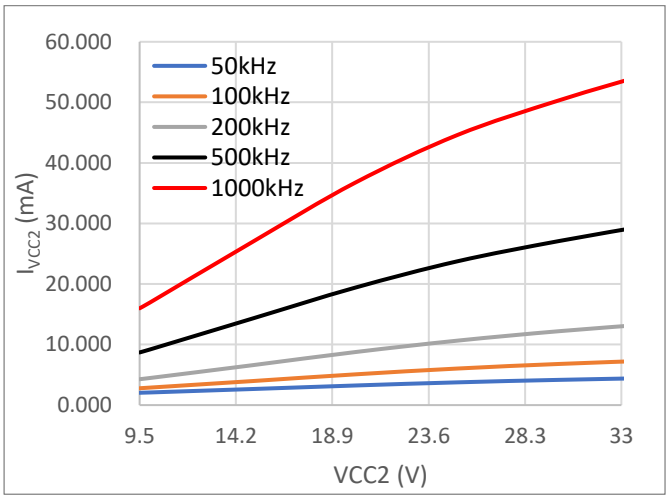


Figure 8. I_{VCC2} Supply Current vs Input Frequency

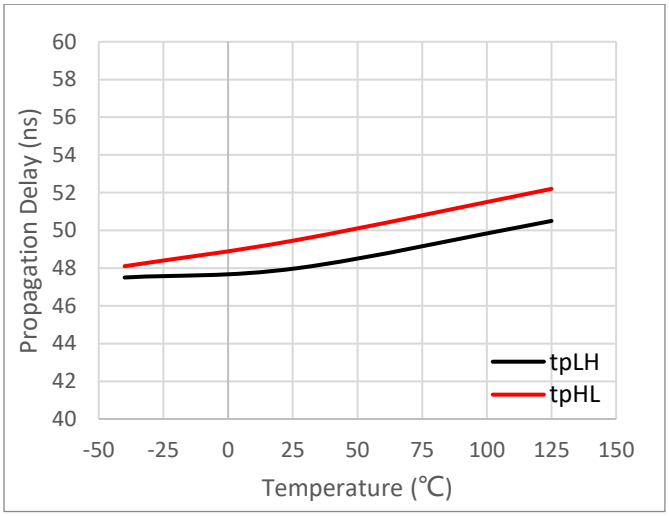


Figure 9. Propagation Delay vs Temperature

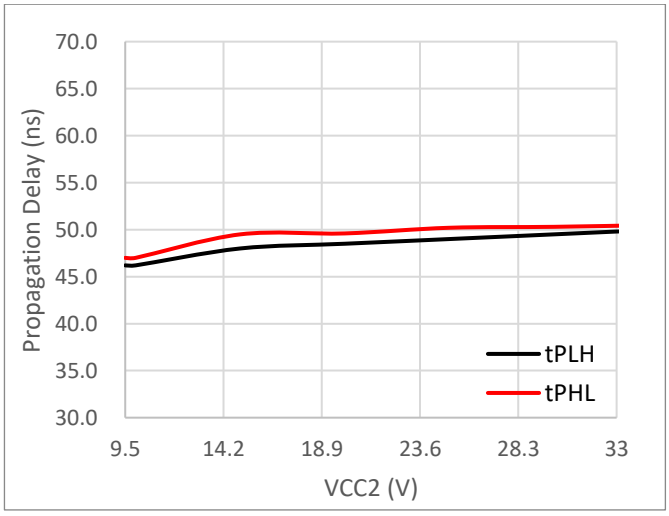


Figure 10. Propagation Delay vs VCC2

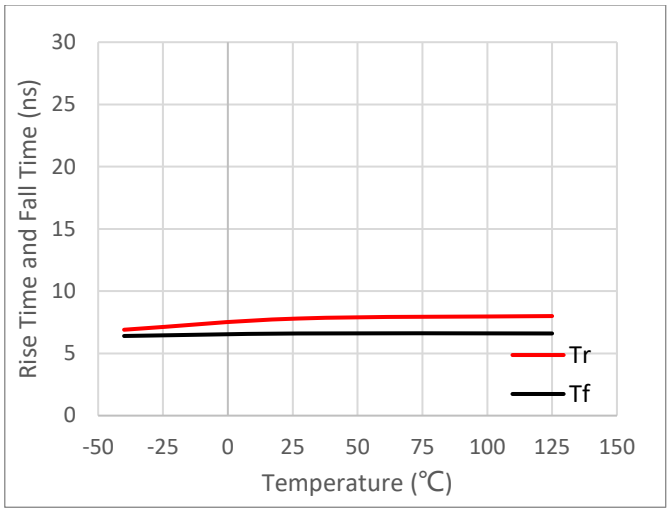


Figure 11. Rise Time and Fall Time vs Temperature

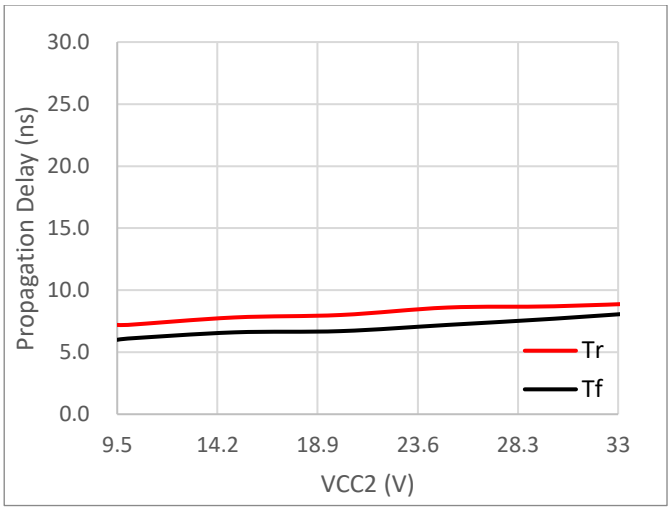


Figure 12. Rise Time and Fall Time vs VCC2

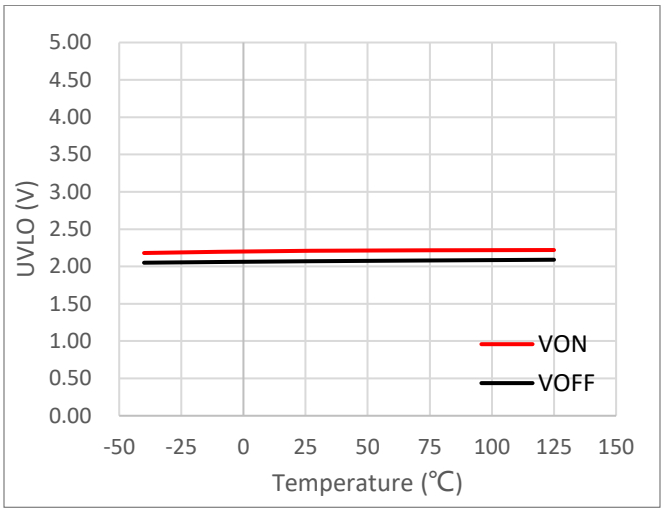


Figure 13. UVLO of VCC1 vs Temperature

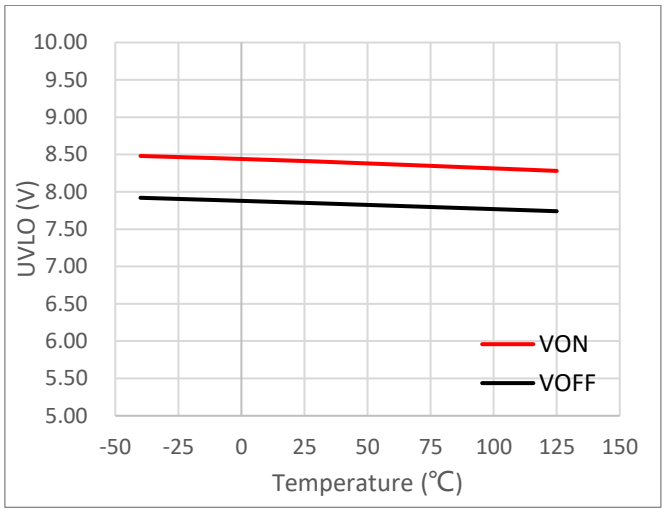


Figure 14. UVLO of VCC2 vs Temperature

7. Detail Descriptions

IVCO1A01/2 driver is single-channel isolated gate driver with 3750Vrms (D) and 5700Vrms (DW) insulation voltage. IVCO1A01 features split outputs which make pull-up and pull-down capabilities independently adjustable. IVCO1A02 features active miller clamp.

7.1 Input Signals

IN+ and IN- are non-inverting and inverting logic gate driver inputs. The pins have a weak pulldown or pullup. When left floating, outputs are pulled to VEE2. The input is a TTL and CMOS logic level with maximum 7V input tolerance.

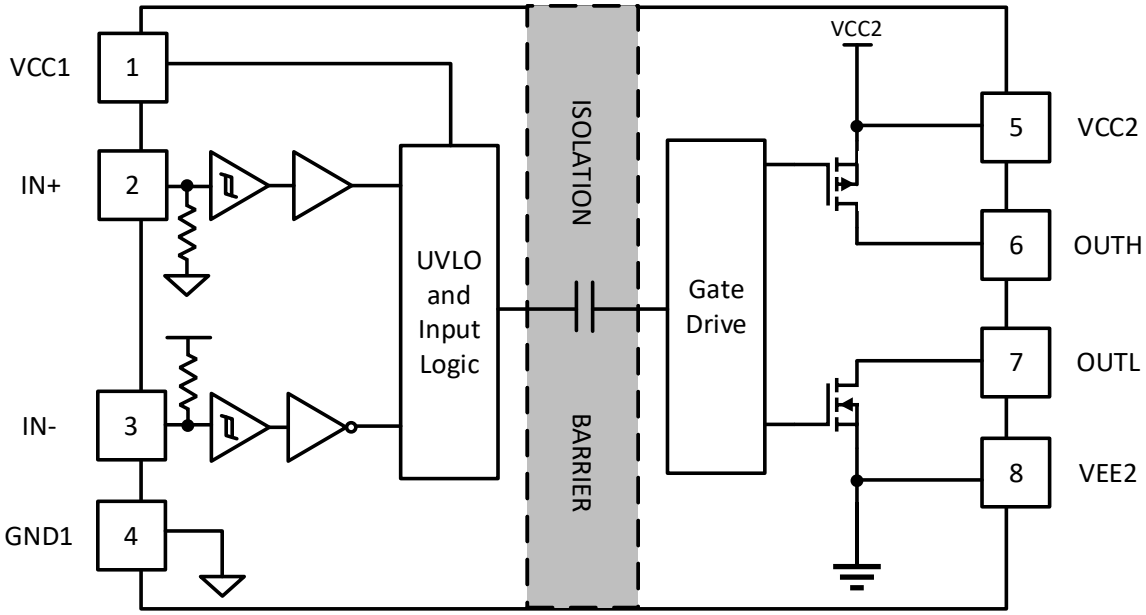


Figure 15. IVCO1A01 Function Block Diagram

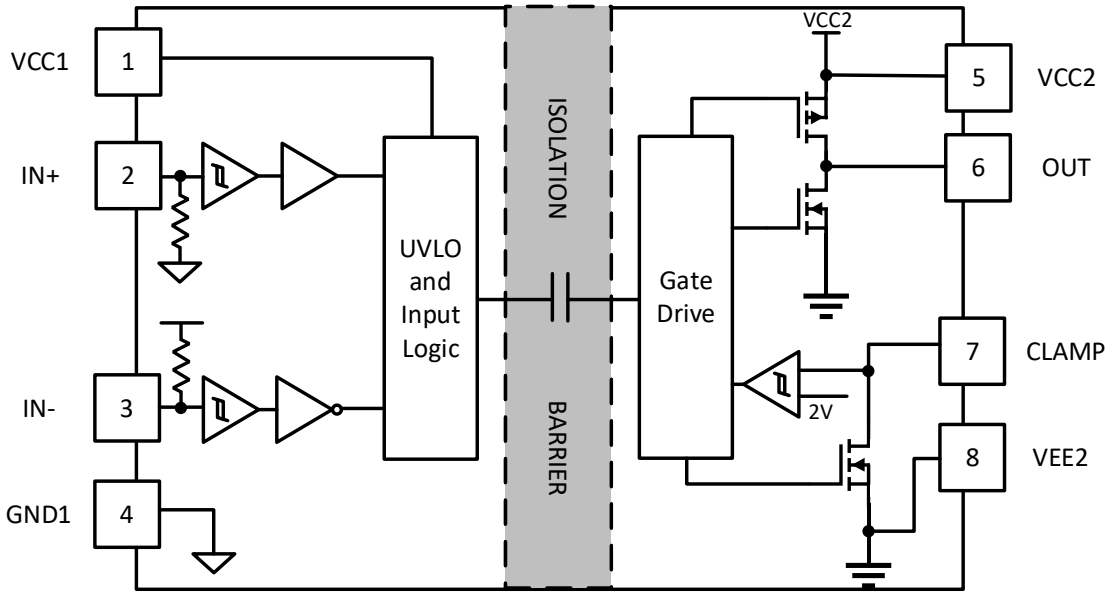


Figure 16. IVCO1A02 Function Block Diagram

7.2 Output Signals

OUTH and OUTL are split outputs. OUTH consists of a hybrid pullup and OUTL consists an N-channel MOSFET for pulldown. Each output stage in IVCO1A01/2 can supply 10A peak source and 10A peak sink current pulses. The output voltage swings between VCC2 and VEE2 providing rail-to-rail operation. The presence of the MOSFET body diodes also offers voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

7.3 VCC and Under Voltage Protection

IVCO1A01/2 maximum VCC1 voltage rating is 7V. The VCC1 internal under voltage lockout (UVLO) protection threshold voltage is 2.2V typical, which enables the input stage working with 2.5V, 3.3V or 5V supply voltages. When VCC1 level is below UVLO (VCC1) threshold, this device holds the output LOW, regardless of the status of the inputs.

IVCO1A01/2 maximum VCC2 voltage rating is 36V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The output stage has VCC2 internal under voltage lockout (UVLO) protection feature. When VCC2 level is below UVLO (VCC2) threshold, this circuit holds the output LOW, regardless of the status of the inputs.

7.4 Isolation and CMTI

IVCO1A01/2 provides insulation withstand voltage 3.75kVrms (D) and 5.7kVrms (DW) with SOIC-8 narrow body package. This device is designed with capacitive isolation technique. The common-mode transient immunity (CMTI) 100V/ns ensures error-free operation when high dv/dt is present.

7.5 CMTI Measurement

Common mode transient immunity (CMTI), which can be distinguished between static and dynamic CMTI, is defined as the maximum tolerable rate of rise and fall of the common mode voltage applied between two isolated circuits. The measurement principle of the CMTI test is shown in figure 17.

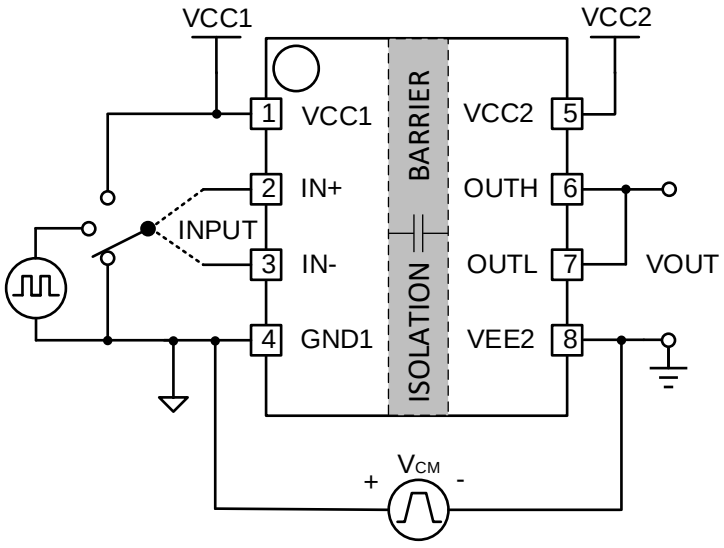


Figure 17. Common-mode transient immunity (CMTI) measurement

8. Application Implementation

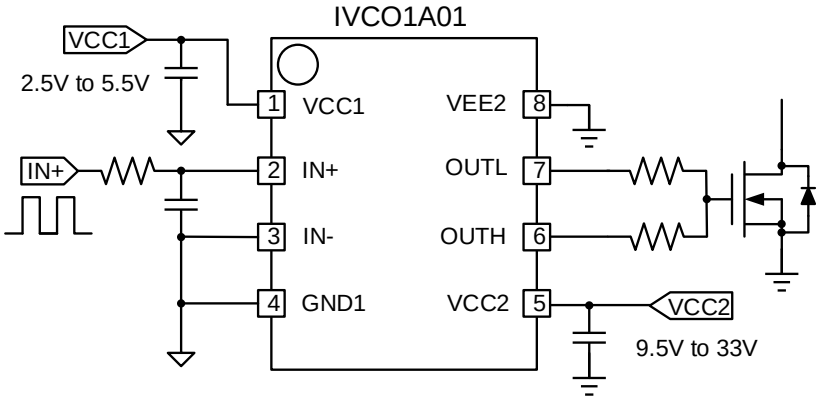


Figure. 18 Typical application circuit with IN+ input (IVCO1A01)

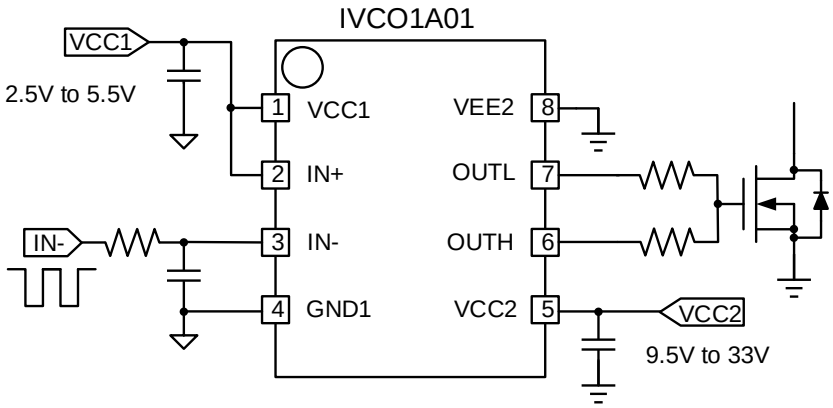


Figure. 19 Typical application circuit with IN- input (IVCO1A01)

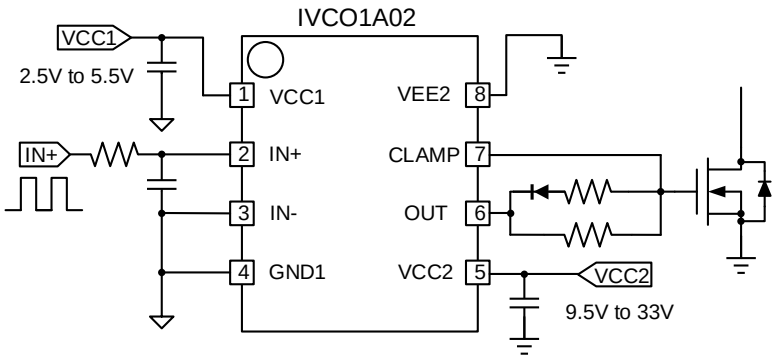


Figure. 20 Typical application circuit with IN+ input (IVCO1A02)

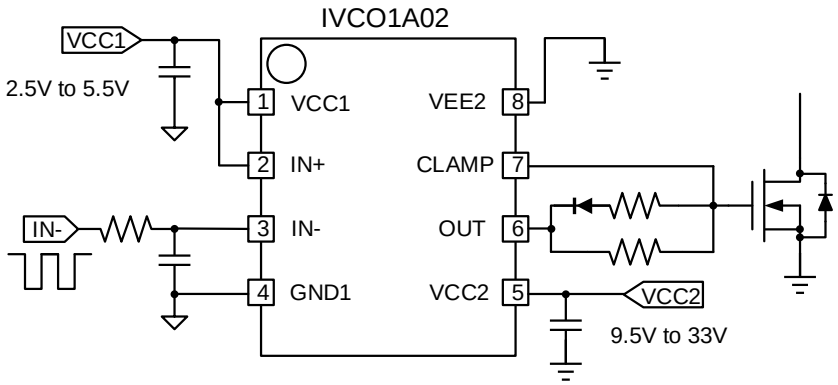


Figure. 21 Typical application circuit with IN- input (IVCO1A02)

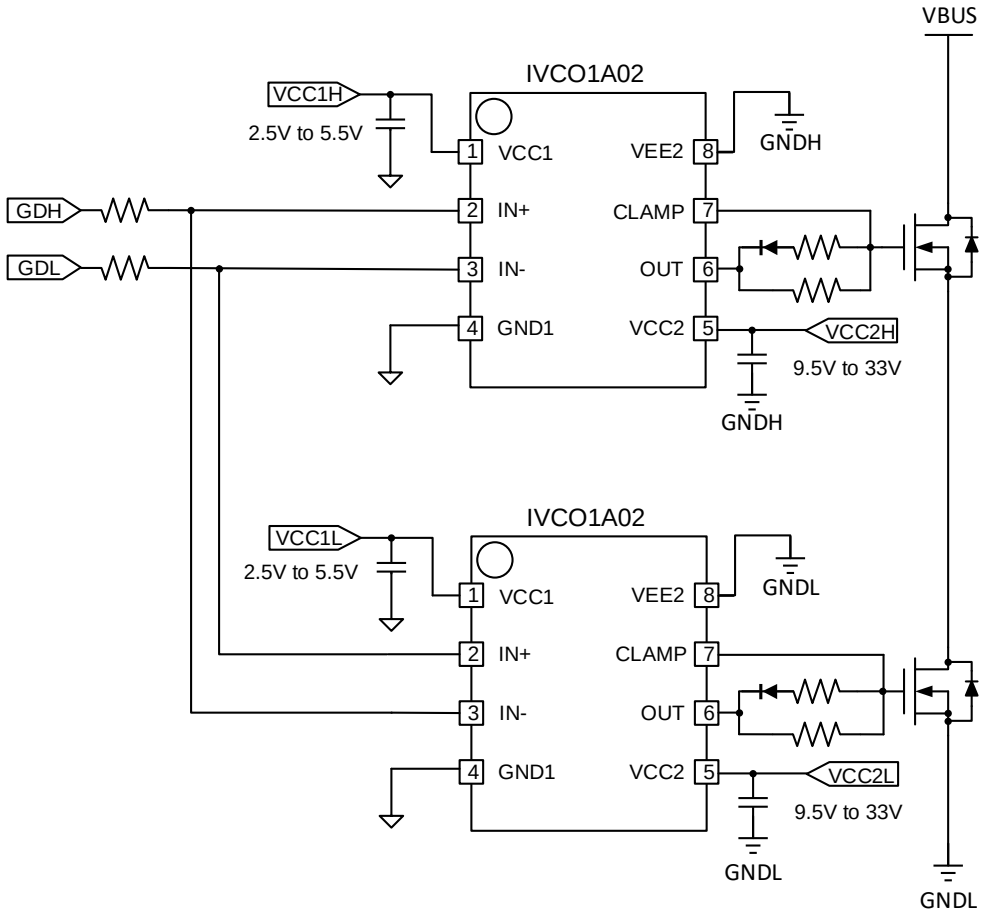


Figure. 22 Typical half bridge application circuit

9. Layout

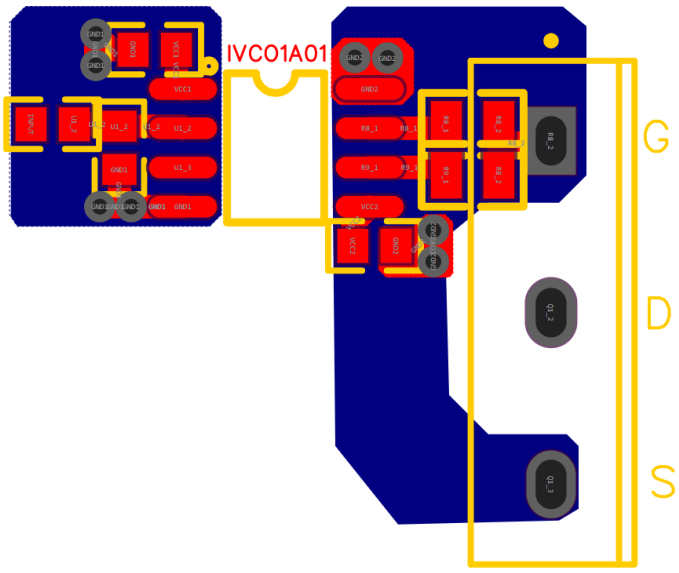


Figure. 23 Layout Example for IVCO1A01 (NB)

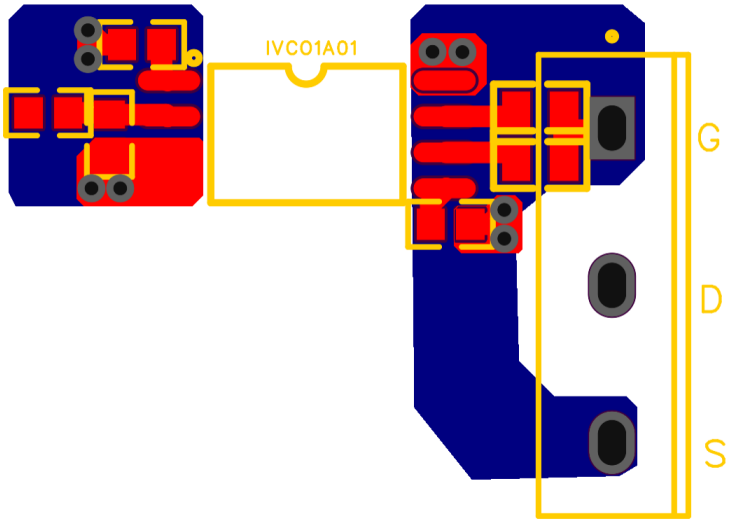
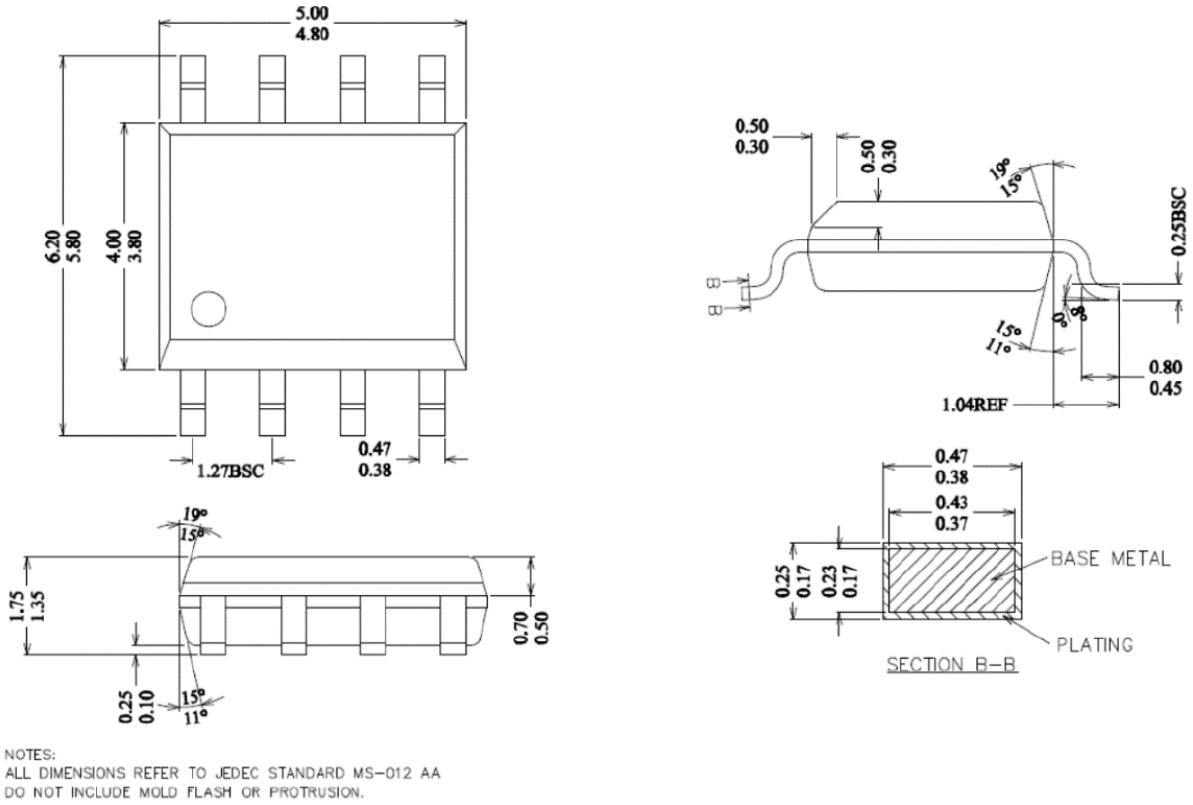


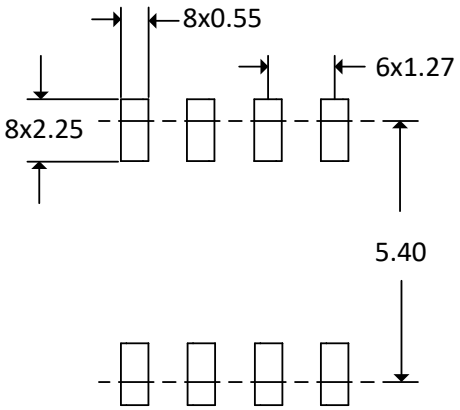
Figure. 24 Layout Example for IVCO1A01 (WB)

10. Package Information

8-Lead Narrow Body SOIC [NB SOIC-8]

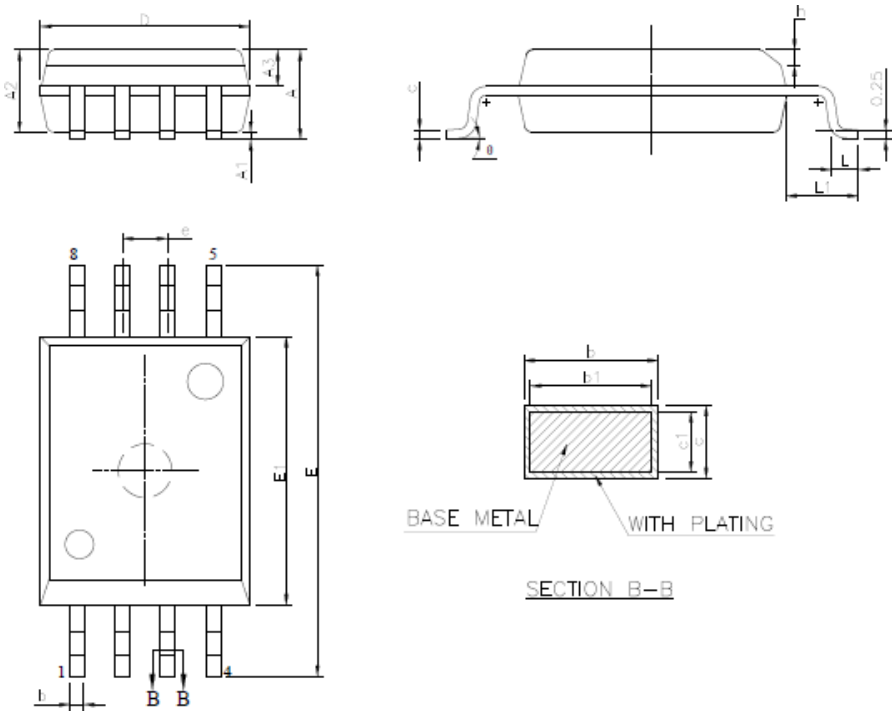


NB SOIC-8 Package Dimensions (mm)



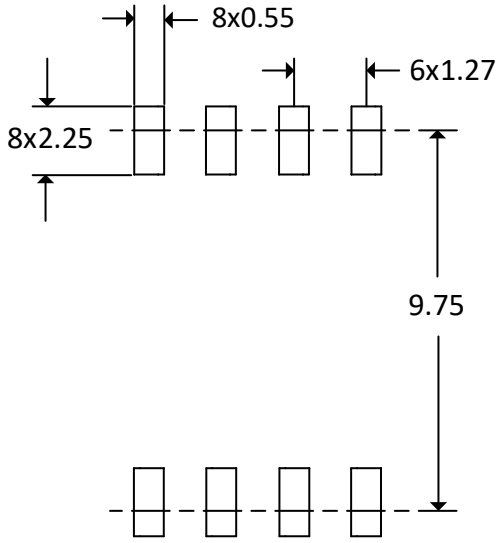
NB SOIC-8 Recommended Soldering Dimensions (mm)

8-Lead Wide Body SOIC [WB SOIC-8]



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	1.00
L1	2.00REF		
θ	0	-	8°

WB SOIC-8 Package Dimensions (mm)



WB SOIC-8 Recommended Soldering Dimensions (mm)

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IV1B12013HA1L IV1D06004F5 IV1D06004O2 IV1D06004P3 IV1D06006F5 IV1D06006O2 IV1D06006P3 IV1D06010O2 IV1D06010T2 IV1D06020U3 IV1D12005O2 IV1D12010O2 IV1D12010P2Z IV1D12020T3 IV1D12020U2 IV1D12030T2 IV1D12030U3 IV1D12030V2 IV1D12040T2 IV1D12040U2 IV1D12040U3 IV1D12040U3Z IV1Q06040L1 IV1Q06040T3 IV1Q06040T4 IV1Q06060T3G IV1Q07015T4G IV1Q12030T4G IV1Q12050D7Z IV1Q12050T4 IV1Q12050T4Z IV1Q12080T3 IV1Q12080T3Z IV1Q12080T4 IV1Q12080T4Z IV1Q12160D7Z IV1Q12160T3 IV1Q12160T4 IV1Q12750O3 IV1Q12750T3 IV2D12002O2 IV2D12002P2 IV2D12020T2 IV2Q06025L1 IV2Q06025T4Z IV2Q06040D7Z IV2Q06040L1 IV2Q06040T4Z IV2Q06060D7Z IV2Q06060L1