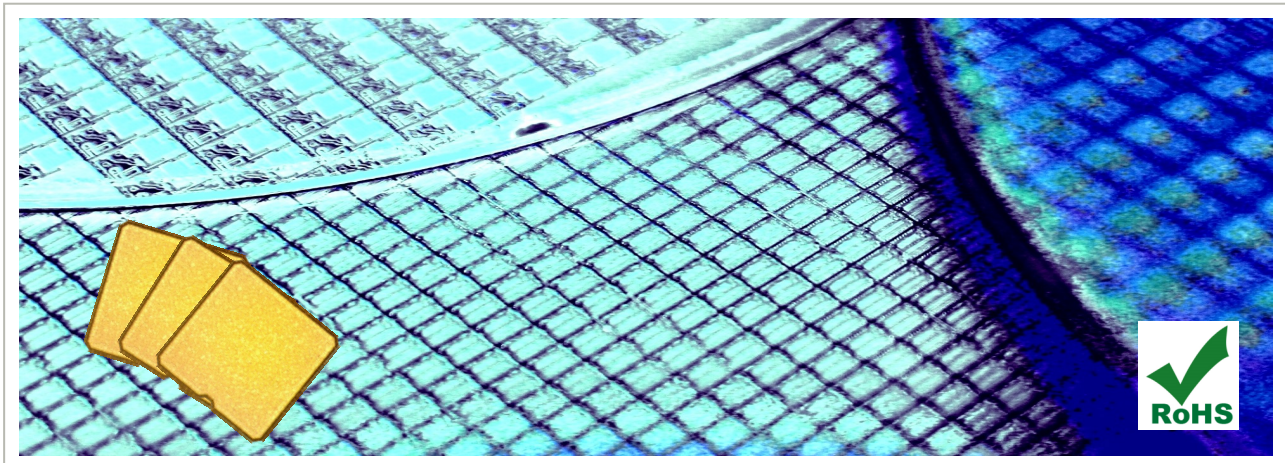




UWSC – Ultra large-band Wire bonding Silicon Capacitor – Wire Bondable Vertical

Rev 1.5



Key Features

- Ultra largeband performance up to 26 GHz
- Resonance free
- Phase stability
- Unique capacitance value of 1nF in 0101
- Ultra high stability of capacitance value over:
 - Temperature $< \pm 0.5\%$ (-55°C to $+150^{\circ}\text{C}$)
 - Voltage $< 0.02\%$ /V
 - Aging $< 0.001\%$ /1000 hours
- Ultra low ESR and ESL
- High reliability (FIT < 0.017 parts/billion hours)
- Compatible with standard wire bonding assembly (ball and wedge)*

* Please refer to our Assembly Application Note for more details

Key Applications

- Optoelectronics/high-speed data
- Trans-Impedance Amplifiers (TIA)
- Receive-and-Transmit Optical Sub-Assembly (ROSA/TOSA)
- Synchronous Optical Networking (SONET)
- High speed digital logic
- Broadband test equipment
- Broadband microwave/millimeter wave
- Replacement of X7R and NP0
- Low profile applications (250 μm , 100 μm on request)

UWSC Capacitors target **optical communication systems** (ROSA/TOSA, SONET and all optoelectronics) as well as **high speed data systems** or products. The UWSC are designed for DC decoupling and bypass applications. The unique technology of integrated passive devices in silicon developed by IPDiA, offers **high rejection up to 26GHz**. The UWSC capacitors are manufactured with both deep trench and MOS semiconductor processes to cover low and high capacitance requirements.

The UWSC capacitors provide **very high reliability** and capacitance stability over temperature ($\pm 0.5\%$) and voltage. They have an extended operating temperature range from -55 to 150°C . **Reliable and repeatable performances** are obtained thanks to a fully controlled production line with high temperature curing (above 900°C) generating a highly pure oxide. These capacitors are compatible with standard wire bonding assembly (ball and wedge). They are RoHS-compliant and are available with thick gold terminations.

Electrical Specifications

Part number	Product description	Case Size	Thickness
UWSC.xxx	Ultra largeband Wire bondable vertical Silicon Capacitor, from -55 to 150°C, 26GHz with Au termination		
935 153 622 410	Ultra largeband Wire bondable vertical Si Cap 1nF, BV>50V	0101	250µm
935 153 620 510	Ultra largeband Wire bondable vertical Si Cap 10nF, BV>50V	0303	250µm
935 153 624 522	Ultra largeband Wire bondable vertical Si Cap 22nF, BV>50V	0504	250µm
935 153 821 510	Ultra largeband Wire bondable vertical Si Cap 10nF, BV>30V	0202	250µm
935 154 622 410	Ultra largeband low profile Wire bondable vertical Si Cap 1 nF, BV>50V	0101	100µm
935 154 620 510	Ultra largeband low profile Wire bondable vertical Si Cap 10nF, BV>50V	0303	100µm
935 154 821 510	Ultra largeband low profile Wire bondable vertical Si Cap 10nF, BV>30V	0202	100µm

Parameters	Value
Capacitance range	10pF to 100 nF ^(**)
Capacitance tolerance	± 15 % ^(**)
Operating temperature range	-55 °C to 150 °C
Storage temperature	- 70 °C to 165 °C
Temperature coefficient	<±0.5 %, from -55 °C to +150 °C
Breakdown voltage (BV)	11, 30, 50, 150, 450 V ^(**)
Capacitance variation versus RVDC	0.02 %/V (from 0 V to RVDC)
Equivalent Serial Inductance (ESL)	typ 6 pH ^(**) @SRF
Equivalent Serial Resistance (ESR)	typ. 14 mΩ ^(**)
Insulation resistance	100 GΩ min @ RVDC & +25°C
Aging	Negligible, < 0.001 % / 1000h
Reliability	FIT<0.017 parts / billion hours.
Capacitor height	Max 250 µm or 100 µm

(**) Other values on request

(**) e.g. 10nF/0303/BV 50V

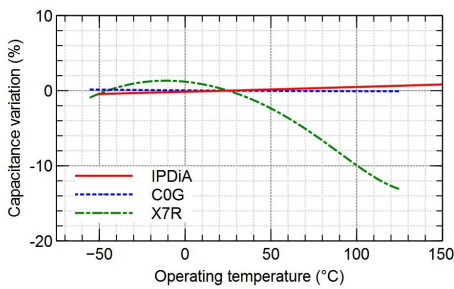


Fig.1: Capacitance variation vs temperature (for UWSC and MLCC technologies)

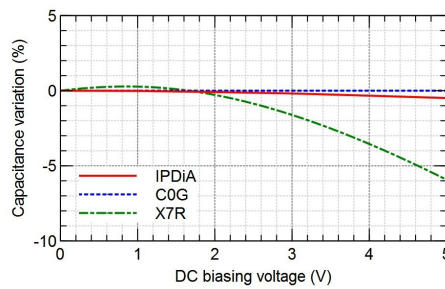


Fig.2: Capacitance variation vs DC biasing voltage (for UWSC and MLCC technologies)

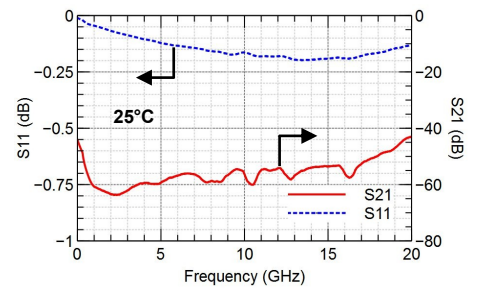
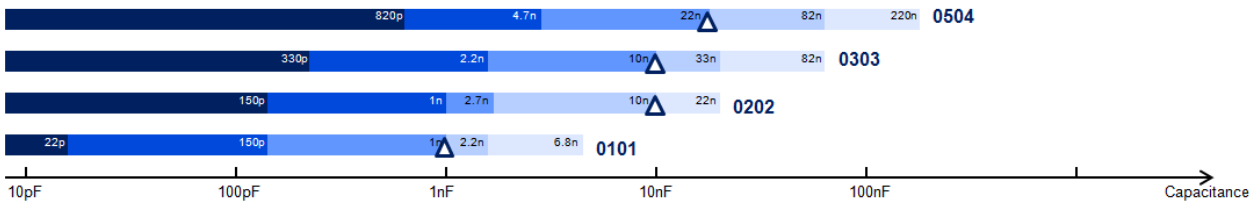


Fig.3: 10 nF/0303 UWSC measurement results (S-parameters in shunt mode)

UWSC Capacitance Range



△ Available parts – see table above
For other values, contact your IPDiA sales representative

BV 450V BV 50V BV 11V
BV 150V BV 30V

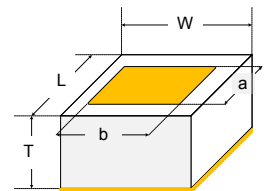
Termination and Outline

Termination

Can be directly mounted on the PCB using die bonding and wire bonding. Bottom electrode in Ti/Ni/Au and top electrode in Ti/Cu/Ni/Au. Other top finishings available on request (ex: 3µm Al/Si/Cu). Compatible with standard wire bonding assembly (ball and wedge).

Package Outline

(mm)	Pad dimension		Case size (typ. ±0.01mm)		
	a	b	L	W	T
0101	>0.15	>0.15	0.25 ⁽¹⁾	0.25 ⁽¹⁾	0.25 (standard profile) or 0.10 (low profile)
0201	>0.40	>0.15	0.50	0.25	
0202	>0.40	>0.40	0.50	0.50	
0303	>0.70	>0.70	0.80	0.80	
0404	>0.94	>0.94	1.04	1.04	
0503	>1.17	>0.72	1.27	0.82	
0504	>1.28	>0.92	1.38	1.02	



Packing

Tape and reel, waffle pack, film frame carrier or raw wafer delivery.

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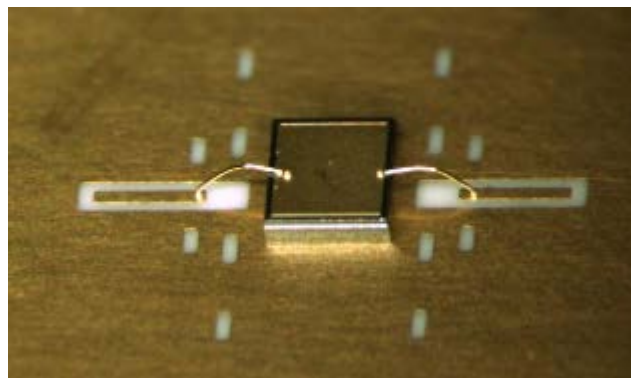
For more information, please visit: <http://www.ipdia.com>
To contact us, email to: sales@ipdia.com



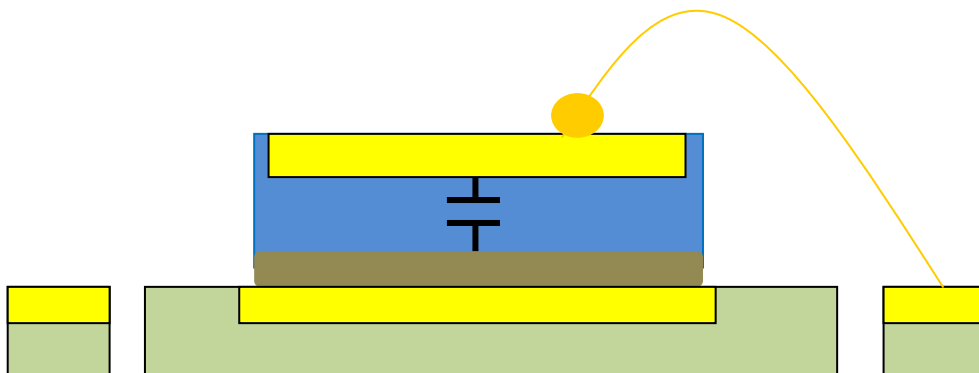
Date of release: 30th January 2015
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 Revision 8



IPDiA Silicon capacitor W type



Introduction

This document describes the attachment techniques recommended by IPDiA for their vertical capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact IPDiA.

Handling Precautions and Storage

Silicon dies must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices do not need to be handled in this type of environment since the product is already well packed. The remaining quantities must be repacked immediately after any process step, under the same conditions as before opening (ESD bag + N2).

Store the capacitors in the manufacturer's package under the following conditions, with no rapid temperature change in an indoor room:

- Temperature: -10 to 40 °C
- Humidity: 30 to 70 % RH

Avoid storing the capacitors under the following conditions:

- (a) Ambient air containing corrosive gas: (chlorine, hydrogen sulfide, ammonia, sulfuric acid, nitric oxide, etc.)
- (b) Ambient air containing volatile or combustible gas
- (c) In environments with a high concentration of airborne particles
- (d) In liquid (water, oil, chemical solution, organic solvents, etc.)
- (e) In direct sunlight
- (f) In freezing environments

To avoid contamination and damage such as scratches and cracks, we recommend the following:

- Never handle the die with the bare hands
- Avoid touching the active face
- Do not store or transport die outside protective bags, tubes, boxes, sawing tape
- Work only in ESD environments
- Use plastic tweezers or a soft vacuum tool to remove the silicon die from the packing.

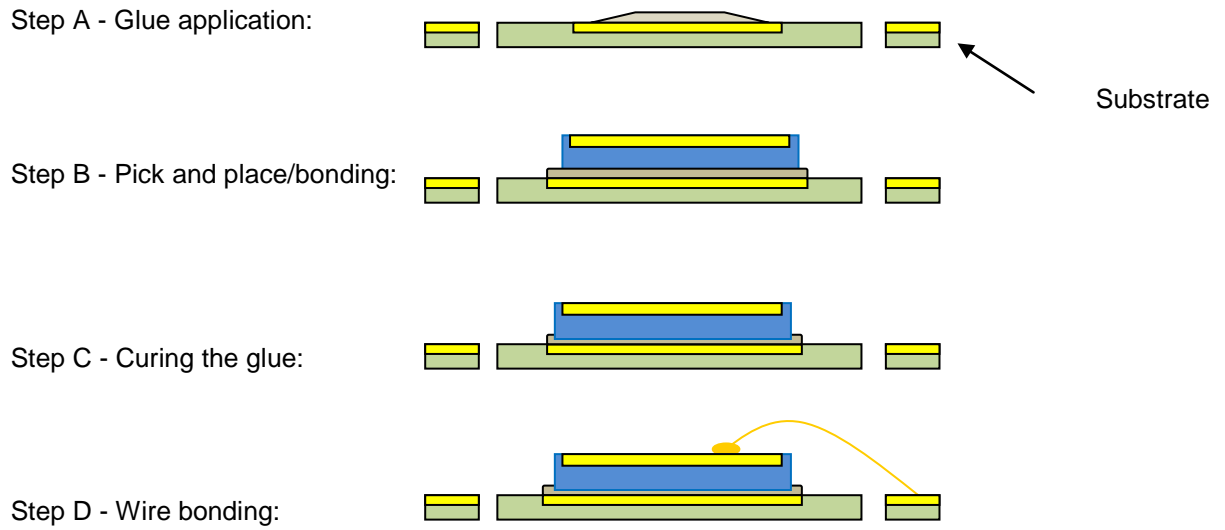
Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided in waffle pack, gelpak or sawing frame. Please contact the IPDiA sales contact for drawing and references (sales@ipdia.com).

Pad Finishing

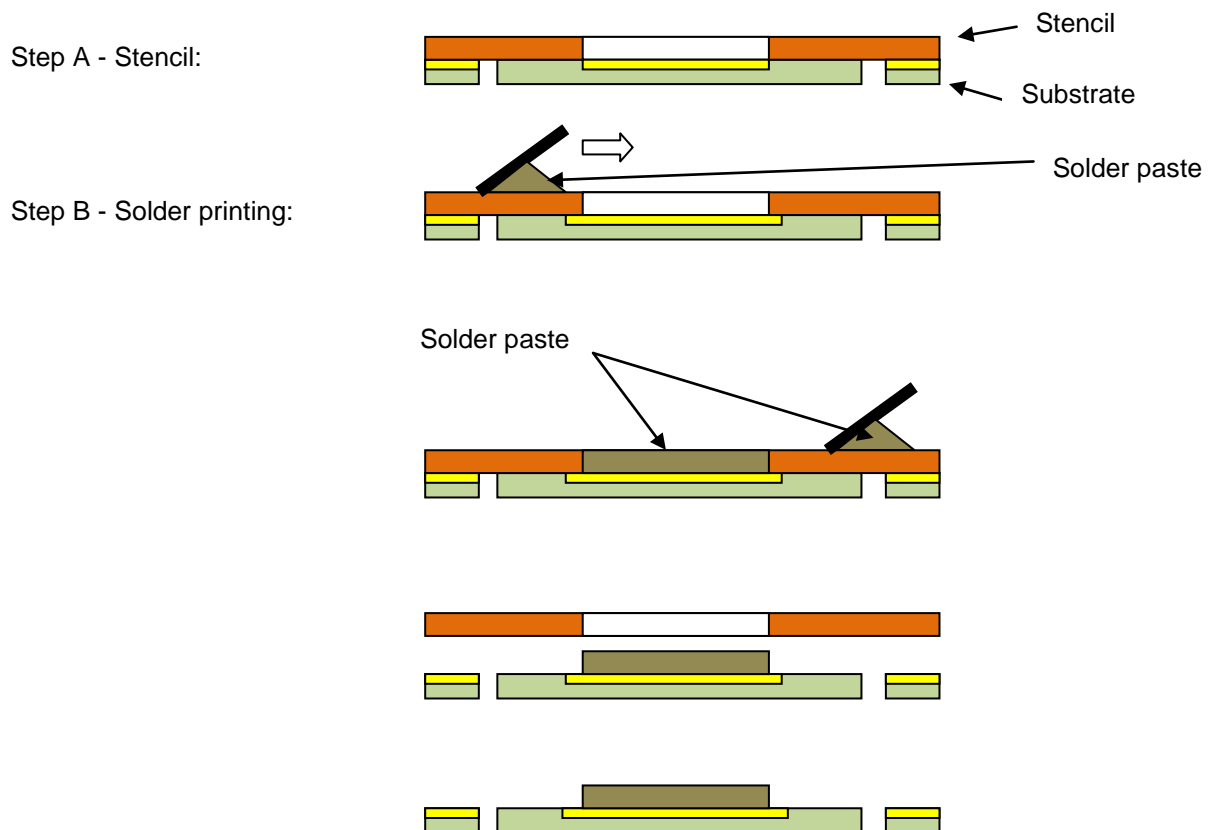
The finishing could be:

- For top electrode(s):
 - TiCuNiAu electroplating: Ti(0.2 µm)/Cu(3.4 µm)/Ni(3 µm)/Au(1.5 µm), recommended for gold wiring.
 - 3 µm aluminium (Al/Si/Cu: 98.96 %/1 %/0.04 %) (finishing recommended for aluminium wire bonding)
 - Other finishes are available upon request
- Bottom electrode: Ti(0.1 µm)/Ni(0.3 µm)/Au(0.2 µm)

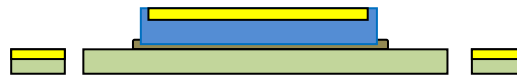
Process Flow with Glue



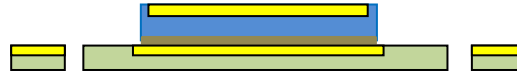
Process Flow with Solder Paste



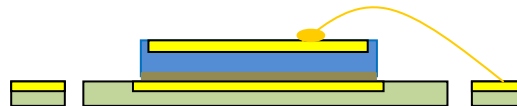
Step C - Die bonding:



Step D - Reflow soldering:



Step E - Wire bonding:



Recommendations concerning the Glue for Die Attachment

An electrical conductive glue must be used. IPDiA often uses the following type of glue:

TYPICAL PROPERTIES OF UNCURED MATERIAL

Thixotropic Index (0.5/5 rpm)	4.0
Viscosity, Brookfield CP51, 25 °C, mPa-s (cP):	
Speed 5 rpm	30,000
Work Life @ 25°C, weeks	2
Shelf Life (from date of manufacture):	
@ 5°C, months	3
@ -10°C, months	6
@ -40°C, year	1

TYPICAL CURING PERFORMANCE

Cure Schedule

1 hour @ 150°C

Alternative Cure Schedule

2 hours @ 125°C

TYPICAL PERFORMANCE OF CURED MATERIAL

Die Shear Strength:

2 X 2 mm Si die, kg-f,

Substrate	@25°C
Ag/Cu leadframe	19

Lap Shear Strength @ 25°C:

Substrate	MPa	psi
Al to Al	12	1500

Landing Pad Opening

IPDiA recommends that the length and width of the landing pad should be 400 µm greater than those of the die pad.

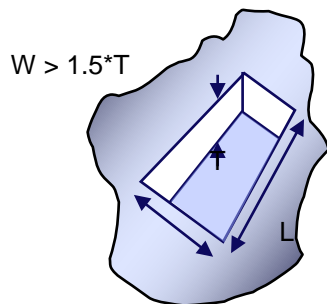
Solder Print Material and Stencil Printing Recommendations

Solder pastes SnPb63/37 and SAC305 are generally used by IPDiA. AuSn 80/20 and SnPb 95/5 can be also used, although they are more expensive. The powder size can be adjusted depending on the die back side size.

ALLOY	COMPOSITION	SOLIDUS	LIQUIDUS	COMMENTS
Sn63	63Sn, 37Pb	183 °C	183 °C	Eutectic
SAC305	96.5Sn, 3Ag, 0.5Cu	217 °C	217 °C	Eutectic
AuSn	80Au20Sn	280 °C	280 °C	Eutectic
SnPb	95Sn5Pb	308 °C	312 °C	Eutectic

Water soluble flux or no-clean flux can be used. If water soluble flux is used, cleaning must be carried out immediately after reflow.

Stencil design rules depending on the quality:



STAINLESS STEEL LASER: $[(L*W)/(2*(L+W)*T)] > 0.66$ &

NICKEL LASER: $[(L*W)/(2*(L+W)*T)] > 0.53$ & $W > 1.2*T$

Die Picking

The most common approach is with automatic equipment using vision inspection to correct die placement after picking and before placement. Manual picking can also be carried out. Use of a rubber or Torlon® tip is strongly recommended for the die picking. A metal tip could damage the capacitor. A minimum picking force (about 100 grams) is recommended.

Die Bonding

If automatic equipment is used, it is best to use the same tool as for picking. The placement force will depend on the die size. A minimum placement force is required in order to cover all the die back side with glue. Too much force can damage the die. In case of die bonding with stencil printing application, IPDiA recommends using the minimum of force, around 50-100 g.

Recommended forces with recommended glue:

Silicon Capacitor Type	Capacitor size (μm^2)	Capacitor thickness	Placement force (grams)
W0101	250x250	100 μm minimum	100
W0202	500x500		200
W0303	800x800		300
W0402	1000x700		350
W0504	1400x1000		450

Reflow Soldering

IPDiA recommends convection reflow but vapor phase reflow and infrared reflow can be also used. Reflow must be carried out in accordance with the JEDEC standard.

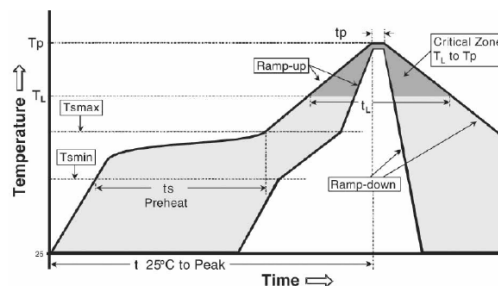
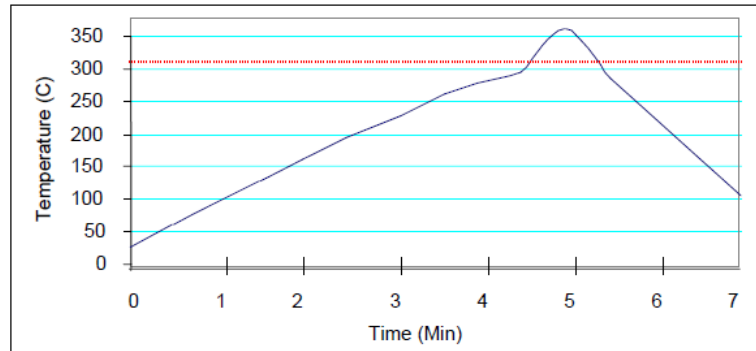


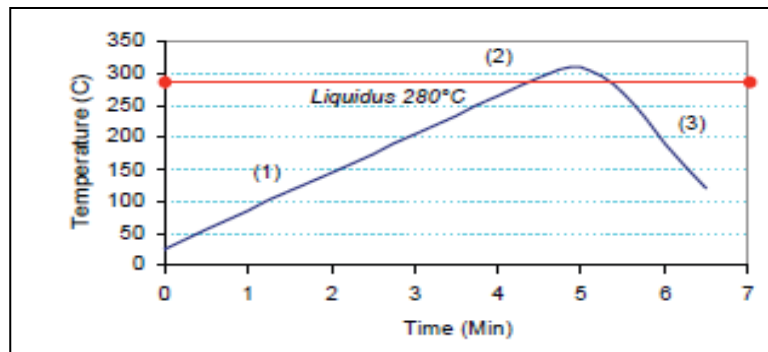
Figure 2: Generic reflow profile according to JEDEC J-STD-020-C

PROFILE FEATURE	SnPb 63/37	SAC305 (Lead-Free Assembly)
Preheat/soak		
Min. temperature (Ts min)	100 °C	150 °C
Max. temperature (Ts max)	150 °C	200 °C
Time (ts) from (Ts min to Ts max)	60 to 120 s	60 to 120 s
Ramp-up		
Ramp-up rate (tL to tp)	maximum 3 °C/s	maximum 3 °C/s
Liquidus temperature (TL)	183 °C	217 °C
Time (tL) maintained above TL	60 to 150 s	60 to 150 s
Peak temperature (Tp)	220 °C	260 °C
Time from 25 °C to peak temperature	maximum 6 minutes	maximum 8 minutes
Ramp-down		
Ramp-down rate (Tp to TL)	maximum 6 °C/s	maximum 6 °C/s

SnPb profile: (IPDiA uses Indalloy Sn95Pb5 from Indium – Indalloy ref. #171)



AuSn profile: (IPDiA uses Indalloy Au80Sn20 from Indium – Indalloy ref. #182)



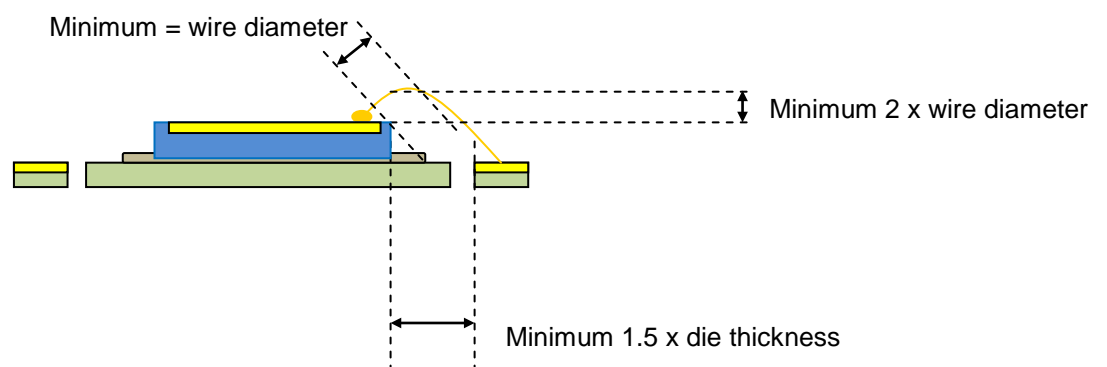
Flux removes tarnish films, maintains surface cleanliness and facilitates solder spreading during the attachment operations. The flux must be compatible with the soldering temperature and soldering times. Please refer to the solder paste supplier for the cleaning and flux removal. Flux residues could be responsible for current leakage or short circuits. For optimum results, clean the circuits immediately after reflow.

Wire Bonding

Materials used and bonding conditions

- Wire lead: diameter 20 to 25 microns, Au/Al wire
- Wire bonding temperature for gold wire bonding: 150 to 200 °C
- Wire bonding methods: Ball bonding or wedge bonding

Wire bonding specifications:

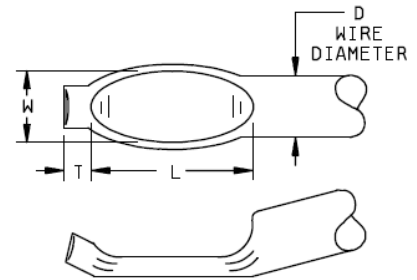


Ball bonding specifications

- The gold ball diameter must be between 2 and 5 times the wire diameter.
- The wire exit must be completely within the periphery of the ball.
- 100 % of the ball must be on the die pad metallization.

Wedge bonding specifications

- The wedge bond on die pad must be between 1.2 and 3 times the gold wire diameter in width.
- The wedge bond must be between 1.5 and 6 times the gold wire diameter in length.
- The bond width must be between 1 and 3 times the aluminium wire diameter.
- The tool impression on wedge bond must cover the entire width of the wire.
- 100 % of the wedge (tail not included) must be on the die pad metallization.



Revision

Version	Author	Date	Description
1.1	Samuel YON	15/06/2015	Creation of the document
1.2	Samuel YON	18/06/2015	Modification

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[02013J3R0ABSTR](#) [02015J1R2ABSTR](#) [04021JR05Z4STR\500](#) [400Z0R1AT100T](#) [400Z0R1PT100T](#) [400Z100FT16T](#) [400Z150FT16T](#)
[400Z170FT16T](#) [400Z180FT16T](#) [400Z1R8QT25T](#) [400Z2R0QT25T](#) [400Z2R4QT25T](#) [400Z3R0AT25T](#) [400Z4R7AT25T](#) [400Z5R6BT25T](#)
[400Z8R2BT16T](#) [04023J4R6ABSTR](#) [02013J1R8PBSTR](#) [02015J0R9PBSTR](#) [02015J1R0PBSTR](#) [0201ZK8R2BBWTR](#) [04021JR65PBSTR](#)
[04021J0R4ZBSTR\500](#) [04023J0R6PBSTR\500](#) [04021J1R4PBSTR\500](#) [02011JR25ZBSTR\500](#) [02015J1R5PBSTR\500](#)
[04025J2R2QBWTR\500](#) [06035J2R2QBSTR](#) [06033J6R8BBSTR](#) [04023J5R6ABSTR](#) [100B300GT500XT](#) [100B1R0CT500XT](#)
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