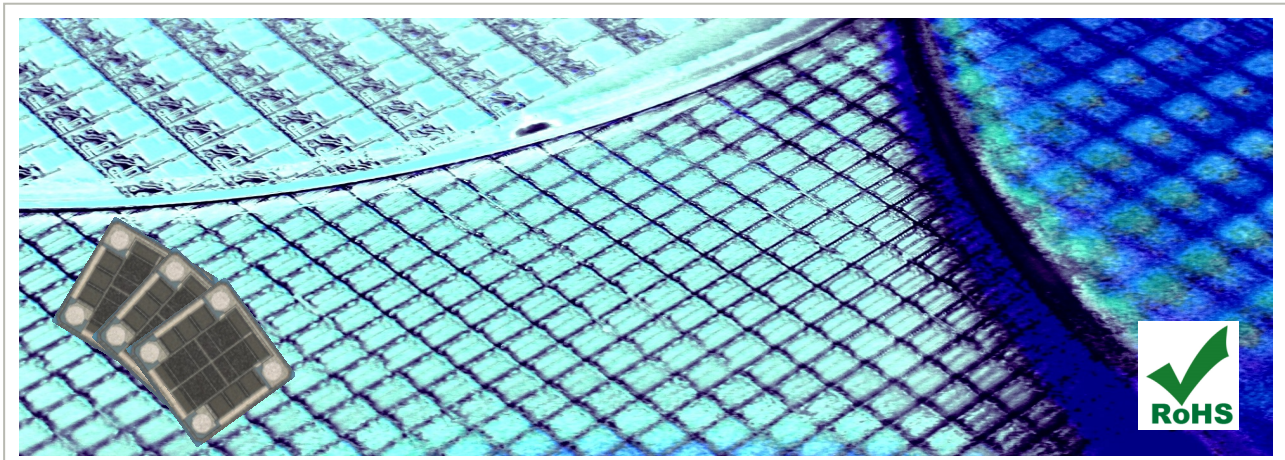




UBEC/ULEC – 60⁺GHz Ultra Broadband Embedding silicon Capacitor – Wire Bondable

Rev 1.5



Key Features

- Ultra broadband performance > 60⁺GHz
- Resonance free
- Phase stability
- Ultra high stability of capacitance value over:
 - Temperature < $\pm 0.5\%$ (-55°C to +150°C)
 - Voltage < 0.1%/V
 - Aging < 0.001%/1000 hours
- Low ESL
- High reliability (FIT < 0.017 parts/billion hours)
- Compatible with standard wire bonding assembly (ball and wedge)*

* Please refer to our Assembly Application Note for more details

Key Applications

- Optoelectronics/high-speed data
- Trans-Impedance Amplifiers (TIA)
- Receive-and-Transmit Optical Sub-Assembly (ROSA/TOSA)
- Synchronous Optical Networking (SONET)
- High speed digital logic
- Broadband test equipment
- Broadband microwave/millimeter wave
- Replacement of X7R and NP0
- Low profile applications (100 μm)

UBEC/ULEC Capacitors target **optical communication systems** (ROSA/TOSA, SONET and all optoelectronics) as well as **high speed data systems** or products. The UBEC/ULEC are designed for DC decoupling and bypass applications. The unique technology of integrated passive devices in silicon developed by IPDiA, offers **high rejection** up to 60 GHz for the UBEC and up to 20 GHz for the ULEC. These deep trench silicon capacitors have been developed with a semiconductor MOS process.

The UBEC/ULEC capacitors provide **very high reliability** and capacitance stability over temperature ($\pm 0.5\%$) and voltage. They have an extended operating temperature range from -55 to 150°C . **Reliable and repeatable performances** are obtained thanks to a fully controlled production line with high temperature curing (above 900°C) generating a highly pure oxide. These capacitors are compatible with standard wire bonding assembly (ball and wedge). They are RoHS-compliant and are available with thick Aluminum terminations.

Electrical Specifications

Part number	Product description	Case Size	Thickness
UBEC.xxx	Ultra Broadband Embedding/Wire bonding Silicon Capacitor from -55 to 150°C, 60GHz with Al termination		
935 157 42F 610	Ultra Broadband Embedding/Wire bonding Silicon Capacitor 100nF, 60GHz, BV>11V	0404	100µm
ULEC.xxx	Ultra Largeband Embedding/Wire bonding Silicon Capacitor, from -55 to 150°C, 20GHz with Al termination		
935 158 42F 610	Ultra Largeband Embedding/Wire bonding Silicon Capacitor 100nF, 20GHz, BV>11V	0404	100µm

Parameters	Value
Capacitance range	10nF to 220 nF ^(**)
Capacitance tolerance	± 15 % ^(**)
Operating temperature range	-55 °C to 150 °C
Storage temperature	- 70 °C to 165 °C
Temperature coefficient	<±0.5 %, from -55 °C to +150 °C
Breakdown voltage (BV)	11, 30 V ^(**)
Capacitance variation versus RVDC	0.1 %/V (from 0 V to RVDC)
Equivalent Serial Inductance (ESL)	Max 100 pH ^(**)
Equivalent Serial Resistance (ESR)	Max 400 mΩ ^(**)
Insulation resistance	100 GΩ min @ RVDC & +25°C
Aging	Negligible, < 0.001 % / 1000h
Reliability	FIT<0.017 parts / billion hours
Capacitor height	Max 100 µm

(**) Other values on request.

(***) e.g. 100nF/0404/BV 11V

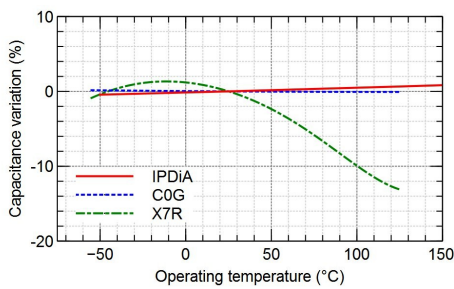


Fig.1: Capacitance variation vs temperature (for UBEC and MLCC technologies)

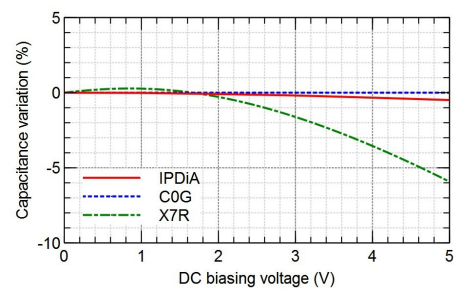
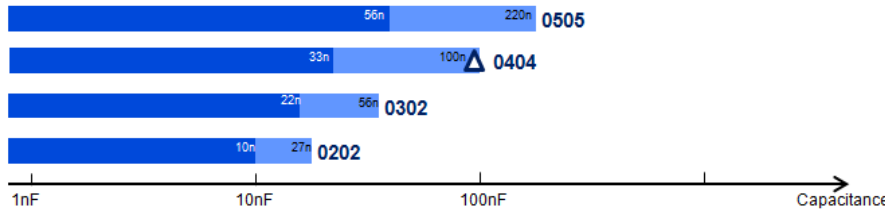


Fig.2: Capacitance variation vs DC biasing voltage (for UBEC and MLCC technologies)

Part Number



△ Available parts – see table above
For other values, contact your IPDiA sales representative

■ BV 30V ■ BV 11V

Termination and Outline

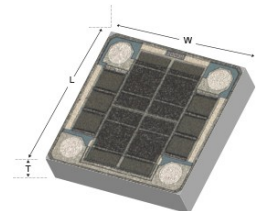
Termination

Can be directly mounted on the PCB using die bonding and wire bonding. Capacitors with top electrodes in 3µm Aluminum (Al/Si/Cu). Other top finishings available on request (ex: Ti/Cu/Ni/Au). Compatible with standard wire bonding assembly (ball and wedge).

Package Outline

For landing pad dimensions on your PCB layout, please refer to IPDiA assembly application note.

(mm)	Case size (typ. ±0.01mm)		
	L	W	T
0202	0.62	0.62	0.10 (low profile)
0302	0.89	0.62	
0404	1.06	1.06	
0505	1.29	1.29	



Packing

Tape and reel, waffle pack, film frame carrier or raw wafer delivery.

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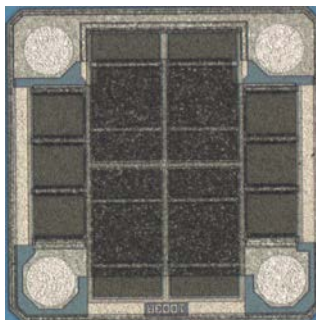
For more information, please visit: <http://www.ipdia.com>
To contact us, email to: sales@ipdia.com



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Document identifier: CL

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IPDiA Silicon capacitor E type

Introduction

This document describes the attachment techniques recommended by IPDiA for their high temperature silicon capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact IPDiA.

Handling Precautions and Storage

Silicon dies must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices do not need to be handled in this type of environment since the product is already well packed. The remaining quantities must be repacked immediately after any process step, under the same conditions as before opening (ESD bag + N2).

Store the capacitors in the manufacturer's package under the following conditions, with no rapid temperature change in an indoor room:

- Temperature: -10 to 40 °C
- Humidity: 30 to 70 % RH

Avoid storing the capacitors under the following conditions:

- (a) Ambient air containing corrosive gas: (chlorine, hydrogen sulfide, ammonia, sulfuric acid, nitric oxide, etc.)
- (b) Ambient air containing volatile or combustible gas
- (c) In environments with a high concentration of airborne particles
- (d) In liquid (water, oil, chemical solution, organic solvents, etc.)
- (e) In direct sunlight
- (f) In freezing environments

To avoid contamination and damage such as scratches and cracks, we recommend the following:

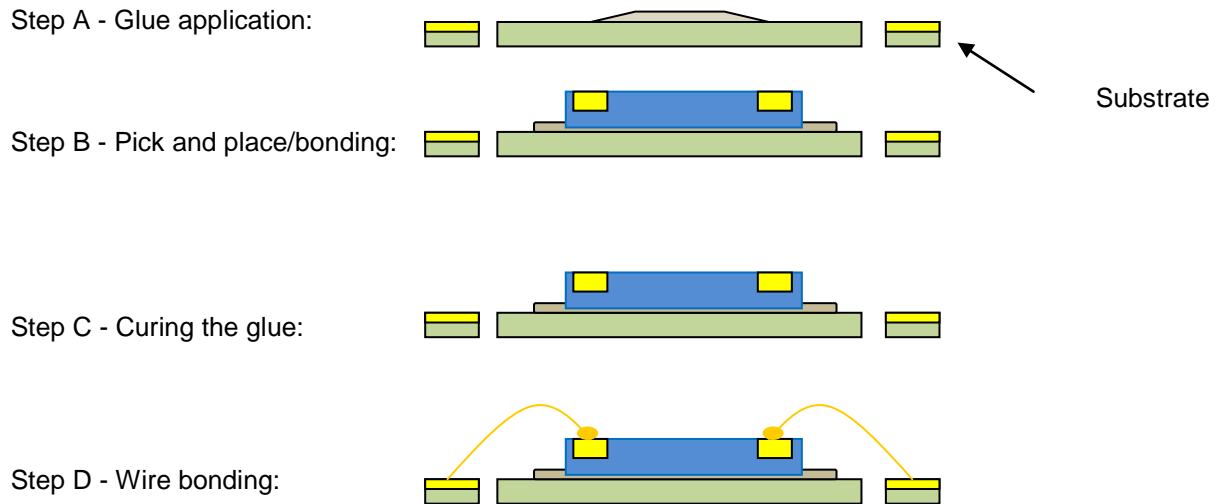
- Never handle the die with the bare hands
- Avoid touching the active face
- Do not store or transport die outside protective bags, tubes, boxes, sawing tape
- Work only in ESD environments
- Use plastic tweezers or a soft vacuum tool to remove the silicon die from the packing.

Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided in waffle pack, gelpak or sawing frame. Please contact the IPDiA sales contact for drawing and references (sales@ipdia.com).

Pad Finishing

- TiCuNiAu electroplating: Ti(0.2 µm)/Cu(3.4 µm)/Ni(3 µm)/Au(1.5 µm)
- 3 µm aluminium (Al/Si/Cu: 98.96 %/1 %/0.04 %) (finishing recommended for aluminium wire bonding)
- Other finishes are available upon request

Process Flow



Recommendations concerning the Glue for Die Attachment

Using an electrical conductive glue could result in capacitor leakage in case of glue overflow on die front side chipping. IPDiA recommends and often uses the following non-conductive glue:

Technology	Bismaleimide Resin
Cure	Heat cure

TYPICAL PROPERTIES OF UNCURED MATERIAL

Specific Gravity @ 25 °C	1.37
Viscosity @ 25 °C, cps	10,000
Thixotropic Index (Speed 0.5/speed 0.5)	5
Pot Life @ 25 °C, hours	12
Ionic Contaminants, ppm:	
Na+, K+	<20
Cl-, F-	<20

Flash Point - See MSDS

TYPICAL PROPERTIES OF CURED MATERIAL

Physical Properties:

Glass Transition Temperature (Tg) °C	-30
Coefficient of Thermal Expansion ppm/°C:	
Below Tg, ppm/°C	80
Above Tg, ppm/°C	150
DMA modulus @ 25°C, GPa	0.3

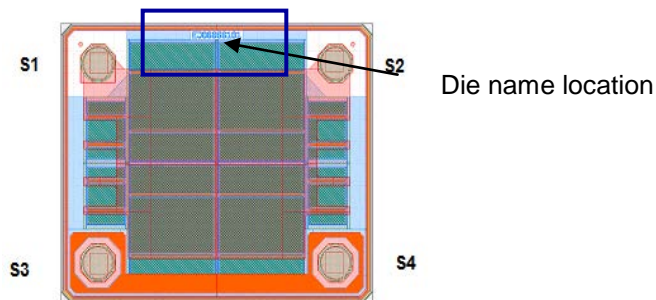
TYPICAL PERFORMANCE OF CURED MATERIAL

Die Shear Strength:

- 1 mil BLT, 300x300 mil die
- Average kgf @25°C on Ceramic
- >100 Average kgf @275°C on Ceramic 15

Special care must be taken when using, for example, thermally conductive glues.

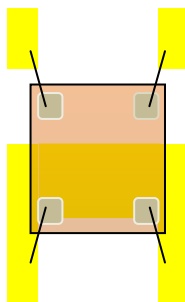
Use of Conductive Glue - Substrate Design



Pin #	Symbol	Description
1, 2	Signal 1	Signal 1
3, 4	Signal 2	Signal 2

Pin description

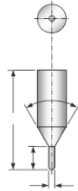
If conductive glue is used on the backside of the silicon cap, it is strongly recommended not to connect the backside to the electrical signal. If the backside is connected to the electrical signal, this signal will be exactly the same as pads 3-4.



Glue Application Tools

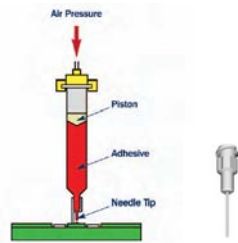
The glue can be dispensed with stamping, air pressure valve, auger or jetting method. The choice will depend on the die size.

Stamping:



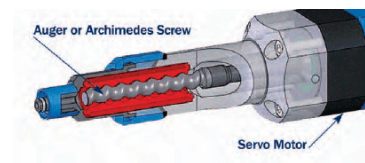
The tool is mounted on the bonding head. It is plunged into a dipping cavity filled with glue and pressed on the bonding position before capacitor bonding.

Air pressure valve:



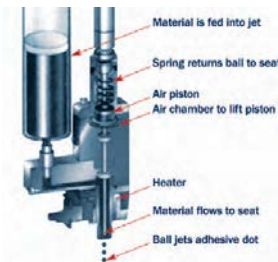
Tool used: needle

Auger:



Tool used: needle

Jetting:



Tool used: nozzle

Silicon Capacitor Type	Capacitor size (µm ²)	Capacitor thickness	Recommended glue dispensing process	Recommended pattern
E0202	580 x 580	100 µm minimum	Stamping/jetting	DOT
E0302	850 x 580		Stamping/time pressure valve/jetting	DOT
E0404	1000 x 1000		Stamping/auger/time pressure valve	DOT
E0505	1250 x 1250		Stamping/auger/time pressure valve	DOT/CROSS
E0605	1520 x 1250		Stamping/auger/time pressure valve	DOT/CROSS
E1208	3000 x 2000		auger	CROSS
E1612	4000 x 3000		auger	CROSS
E1616	4000 x 4000		auger	CROSS
E2016	5000 x 4000			

Die Picking

The most common approach is with automatic equipment using vision inspection to correct die placement after picking and before placement. Manual picking can also be carried out. Use of a rubber or Turlon® tip is strongly recommended for the die picking. A metal tip could damage the capacitor. A minimum picking force (about 100 grams) is recommended.

Die Bonding

If automatic equipment is used, it is best to use the same tool as for picking. The placement force will depend on the die size. A minimum placement force is required in order to cover all the die back side with glue. Too much force can damage the die.

Recommended forces with recommended glue:

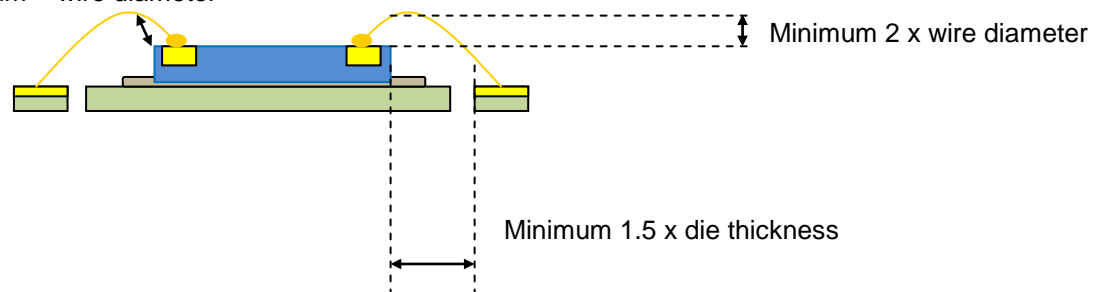
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Wire Bonding

Materials used and bonding conditions

- Wire lead: diameter 20 to 25 microns, Au/Al wire
- Wire bonding temperature for gold wire bonding: 150 to 200 °C
- Wire bonding methods: Ball bonding or wedge bonding

Minimum = wire diameter

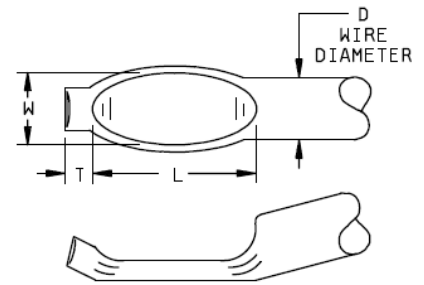


Ball bonding specifications

- The gold ball diameter must be between 2 and 5 times the wire diameter.
- The wire exit must be completely within the periphery of the ball.
- 80 % of the ball must be on the die pad metallization.

Wedge bonding specifications

- The wedge bond on die pad must be between 1.2 and 3 times the gold wire diameter in width.
- The wedge bond must be between 1.5 and 6 times the gold wire diameter in length.
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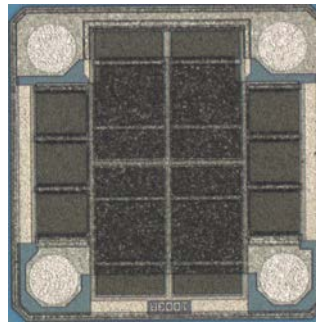


Revision

Version	Author	Date	Description
1.1	Samuel YON	15/06/2015	Creation of the document
1.2	Samuel YON	02/11/2015	Amendment

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IPDiA Silicon capacitor E type

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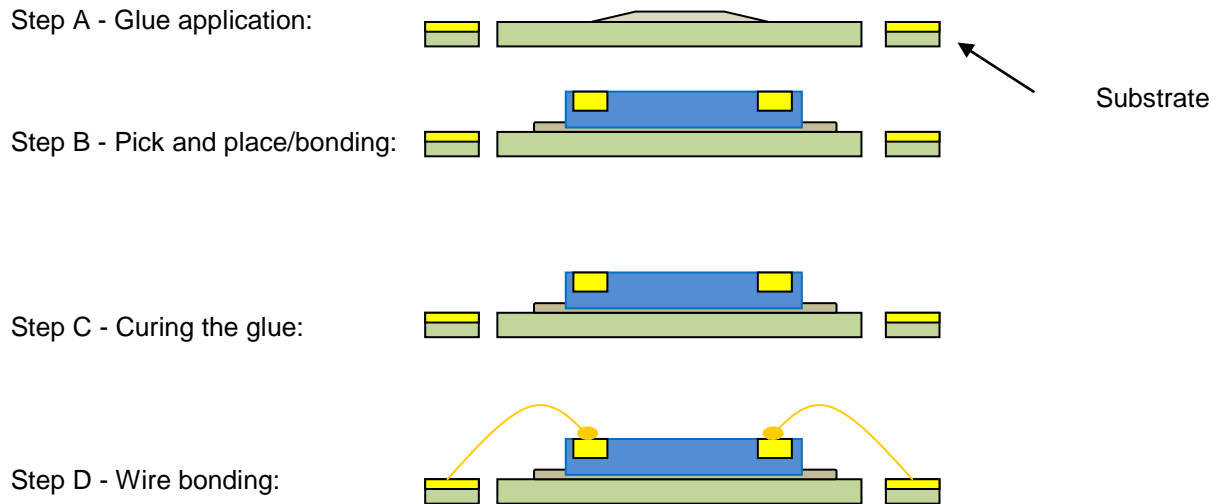
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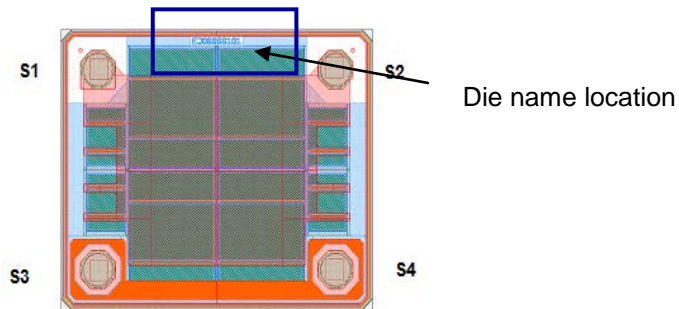
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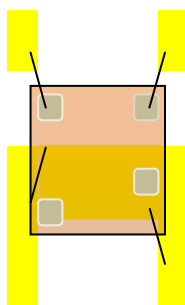
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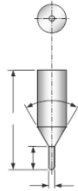
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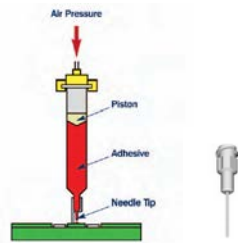
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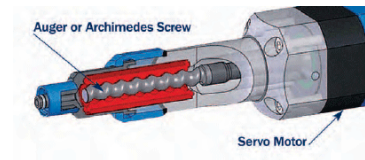
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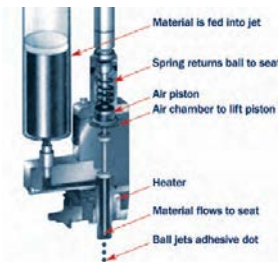
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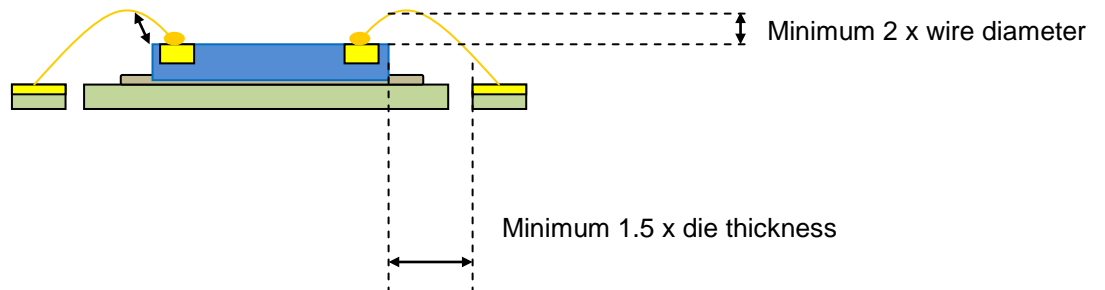
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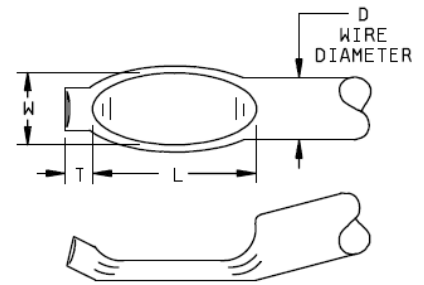


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[02013J3R0ABSTR](#) [02015J1R2ABSTR](#) [04021JR05Z4STR\500](#) [400Z0R1AT100T](#) [400Z0R1PT100T](#) [400Z100FT16T](#) [400Z150FT16T](#)
[400Z170FT16T](#) [400Z180FT16T](#) [400Z1R8QT25T](#) [400Z2R0QT25T](#) [400Z2R4QT25T](#) [400Z3R0AT25T](#) [400Z4R7AT25T](#) [400Z5R6BT25T](#)
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[04025J2R2QBWTR\500](#) [06035J2R2QBSTR](#) [06033J6R8BBSTR](#) [04023J5R6ABSTR](#) [100B300GT500XT](#) [100B1R0CT500XT](#)
[02015J2R0PBSTR\500](#) [100B470GT500XT](#) [700B271JT200XT](#) [100B5R1DT500XT](#) [100B0R6DT500XT](#) [100B160FT500XT](#)
[100B3R3DT500XT](#) [100B180FT500XT](#) [100B2R0DT500XT](#) [04021J0R8P4STR\500](#)