MIMO/SISO Differential Line Driver

GENERAL DESCRIPTION

The CG1110 is a high-performance MIMO/SISO dual port differential line driver designed to work in broadband PLC system. It contains two pairs of wideband, high-voltage, current mode feedback amplifiers.

The line driver can operate on single supply from +10V to +13.2V and retains its bandwidth and linearity over the complete full-scale supply range.

The supply current can be set using a resistor on the IBIAS pin. The device has two separate disable control pins (ENB_AB and ENB_CD) for each differential amplifier to allow TDM operation. These logic pins are internally pulled high, so floating these inputs will put the device in shut down mode.

An internal input VCM generator maximizes the dynamic range and reduces the number of PCB components in the application circuit.

The device has built-in reliable thermal shut-down protection circuit and will be forced into shut-down mode typically when the internal junction temperature reaches +165°C.

The CG1110 is available in 4mmx4mm thermally enhanced 20 pin QFN package. The device is specified for operation over the full -40°C to +85°C ambient temperature range.

FEATURES

- Single +10V to +13.2V supply
- Fixed voltage gain of 25dB (A_V=18 V/V)
- 100MHz -3dB closed-loop signal bandwidth
- High linearity MTPR of 50dBc
- 350mA max. output driver capability
- 16.4$V_{pp\text{-}diff}$ linear output drive into 34Ω
- 25mA quiescent current per port
- Control pins for enable/disable
- Internal V_{CM} for input signal biasing
- Fast shut down / power up – less than 1us
- Thermal shut-down & output short protection
- Supports 20-pin, 4mmx4mm QFN Package
- -40°C to +85°C operating ambient temperature

APPLICATIONS

- Power Line Communications (PLC)
- Smart Grid application
- Smart Home applications (IPTV, Security Cameras, etc.)
- High Voltage and High Current Driving

BLOCK DIAGRAM

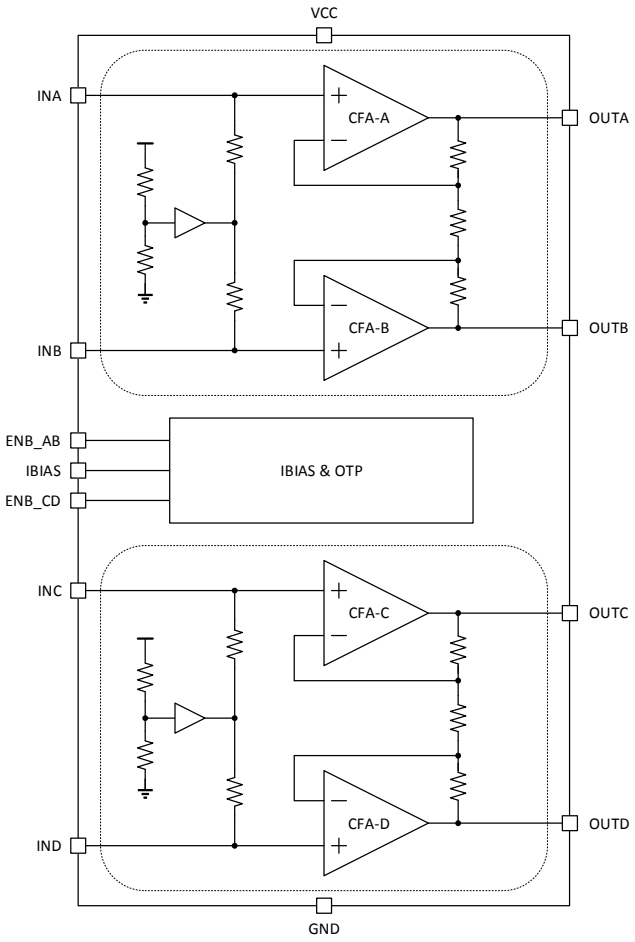
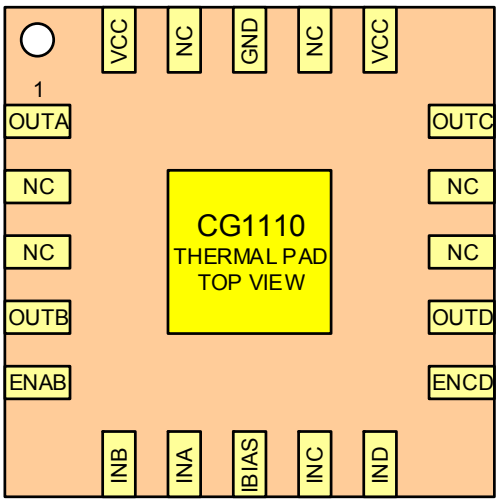


Figure 1 Block diagram

PIN OUT (TOP VIEW)



PIN DESCRIPTION

PIN NUMBER	NAME	I/O	DESCRIPTION
1	OUTA	O	Amplifier-A output
2, 3, 13, 14, 17, 19	NC	-	No internal connection
4	OUTB	O	Amplifier-B output
5	ENB_AB	I	Port-AB enable/disable control
6	INB	I	Amplifier-B non-inverting input
7	INA	I	Amplifier-A non-inverting input
8	IBIAS	O	Bias current adjustment pin
9	INC	I	Amplifier-C non-inverting input
10	IND	I	Amplifier-D non-inverting input
11	ENB_CD	I	Port-CD enable/disable control
12	OUTD	O	Amplifier-D output
15	OUTC	O	Amplifier-C output
16, 20	VCC	PW	Power supply
18	GND	PW	Ground
EPAD	THERMAL PAD	I/O	Connect to the ground

1. Operating Ranges

1.1 Absolute Maximum Ratings

Symbol	Characteristics	Rating	Unit
V_{CC}	Supply Voltage VCC to GND	-0.3 to +13.5	V
V_{INA}, V_{INB}, V_{INC}, V_{IND}	Voltage on input pins	GND+3 to VCC-3	V
V_{ENB_AB}, V_{ENB_CD}	Voltage on control pin	-0.3 to +6	V
V_{IBIAS}	Voltage on BIAS pin	-0.3 to +4	V
I_{INA}, I_{INB}, I_{INC}, I_{IND}	Current into any input pins	-5 to +5	mA
I_{OUTA}, I_{OUTB}, I_{OUTC}, I_{OUTD}	DC continuous output current	100	mA
$T_{Ambient}$	Operating ambient temperature	-40 to 85	˚C
$T_{Junction}$	Operating junction temperature	150	˚C
$I_{Latch-up}$	Latch up current	300	mA

1.2 ESD Ratings

ESD Rating	Value	Unit
Human Body Model (Tested per JESD22-A114F).	±2000	V
Charge Device Model (Tested per JESD22-C101E)	±1000	V

1.3 Typical Operating Ranges

Symbol	Characteristics	Rating	Unit
V_{CC}	Supply Voltage	+10 to +13.2	V
V_{INABD}, V_{INCDD}	Differential input voltage at Av=18 V/V	0 to ±1	V
V_{ENB_AB}, V_{ENB_CD}	Control pin to GND	0 to +6	V
$T_{Ambient}$	Operating temperature	-40 to 85	˚C
$T_{Junction}$	Junction temperature	-40 to 150	˚C

2. Electrical Characteristics

DC Characteristics

V_{CC} = 12V, Ta = 25˚C, A_V = 18 V/V, R_T = 3.9Ω, R_{L-DIFF} = 34Ω, C_L = 50pF, R_{IBIAS} = 0Ω, ENB_AB = ENB_CD = 0V, unless otherwise specified. Referred to typical test and application circuit.

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Supply Characteristics						
Supply Voltage	VCC		10	12	13.2	V
Quiescent Current – MIMO (Dual output port enable, 4X CFA)	I_{MIMO}	ENB_AB = 0V, ENB_CD = 0V	-	46	TBD	mA
Quiescent Current – SISO (Single output port enable, 2X CFA)	I_{SISO}	ENB_AB = 3.3V, ENB_CD = 0V, or ENB_AB = 0V, ENB_CD = 3.3V	-	24	TBD	mA
Quiescent Current - Shut Down	I_{SD}	ENB_AB = 3.3V, ENB_CD = 3.3V	-	1.5	TBD	mA
Input Characteristics						
Input Offset Voltage	V_{OS_IN}	Voltage difference from INA to INB or from INC to IND	-5	0	5	mV
Output Offset Voltage	V_{OS_OUT}	Voltage difference from OUTA to OUTB or OUTC to OUTD	-100	0	-100	mV
Non-inverting Input Voltage Noise	e_N	f_c = 1MHz *Note 1	-	8	-	nV/√Hz
Non-inverting Input Current Noise	i_{N+}	f_c = 1MHz *Note 1	-	4.5	-	pA/√Hz
Differential Input Impedance	R_{INP}	Measured at VCC/2	10	12.5	15	KΩ
Logic Input High Voltage	V_{IH}	ENB_AB, ENB_CD inputs	2.2	-	-	V
Logic Input Low Voltage	V_{IL}	ENB_AB, ENB_CD inputs	-	-	0.8	V
Logic Input High Current	I_{IH}	ENB_AB = ENB_CD = 3.3V	-	-3.5	-	µA
Logic Input Low Current	I_{IL}	ENB_AB = ENB_CD = 0V	-	30	-	µA
Common-mode Input Range Non-Inverting Input Pins	VCM_{IN}	Referenced to + VCC/2	-3	0	+3	V
Output Characteristics						
Differential Voltage Gain	A_V	(OUTA-OUTB)/(INA-INB), (OUTC-OUTD)/(INC-IND)	17	18	19	V/V
Output Short Current	I_{OS}	R_S = 1Ω shorts to VCC or GND	-	-	1.5	A
Common-mode Rejection Ratio (Differential Output referred)	$CMRR_{DM}$	f_c = 1MHz, 0.1V_{PP}	TBD	65	-	dB
PSRR to Differential Output (Output referred)	$PSRR_{DMO}$	f_c = 1MHz, 0.1V_{PP}	TBD	65	-	dB
PSRR to Common-mode Output (Output referred)	$PSRR_{CM}$	f_c = 1MHz, 0.1V_{PP}	TBD	45	-	dB
Thermal Protection						
Thermal Shut-down Temperature *Note 1	T_{SD}		-	165	-	˚C

Note 1: Obtained from design simulation and characterization, not tested.

AC Characteristics

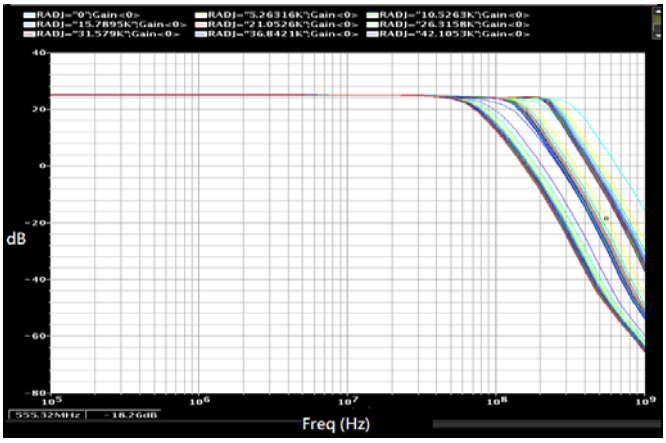
V_{CC} = 12V, Ta = 25˚C, AV = 18 V/V, RT = 3.9Ω, RL-DIFF = 34Ω, CL = 50pF, R_{BIAS} = 0Ω, ENB_AB = ENB_CD = 0V, unless otherwise specified. Referred to typical test and application circuit.

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Output AC Characteristics						
-3dB Small-signal Bandwidth	SSBW	V_{IN} = 0.2 $V_{PP-DIFF}$	-	100	-	MHz
-3dB Large-signal Bandwidth	LSBW	V_{IN} = 0.8 $V_{PP-DIFF}$	-	80	-	MHz
Slew Rate	SR	V_{IN} = 2.0 $V_{PP-DIFF}$	-	1600	-	V/µs

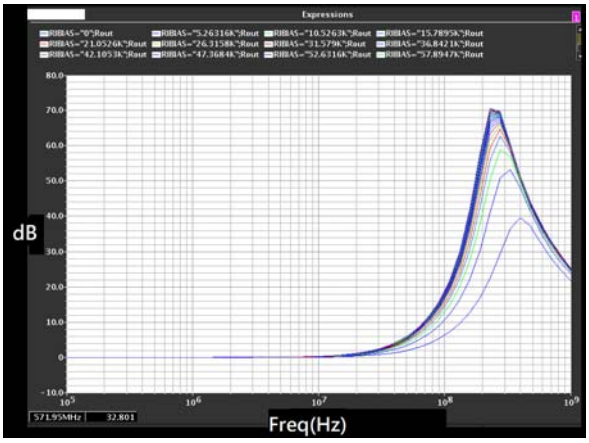
2nd Harmonic Distortion	HD2	f_C = 10MHz, V_{IN} = 0.2 $V_{PP-DIFF}$	-	-66	-	dBc
		f_C = 10MHz, V_{IN} = 0.8 $V_{PP-DIFF}$	-	-60	-	dBc
3rd Harmonic Distortion	HD3	f_C = 10MHz, V_{IN} = 0.2 $V_{PP-DIFF}$	-	-60	-	dBc
		f_C = 10MHz, V_{IN} = 0.8 $V_{PP-DIFF}$	-	-51	-	dBc
Multi-Tone Power Ratio	$MTPR_{STEP}$	Full power from 1MHz to 30MHz, 100kHz tone spacing, P_{LINE} = 15.5dBm, PAR = 15dB	-50	-	-	dB
		30dB power back off from 30MHz to 50MHz, 100kHz tone spacing, P_{LINE} = 15.5dBm, PAR = 15dB	-20	-	-	dB
	$MTPR_{FLAT}$	20dB power back off from 1MHz to 50MHz, 100kHz tone spacing, P_{LINE} = 15.5dBm, PAR = 15dB	-50	-	-	dB

3. Typical Performance Characteristics

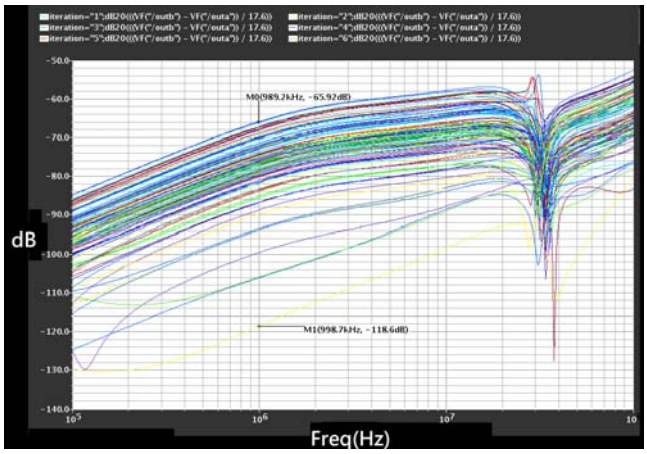
V_{CC} = 12V, Ta = 25˚C, AV =18 V/V, RT = 3.9Ω, RL-DIFF = 34Ω, CL = 50pF, R_{IBIAS} = 0Ω, ENB_AB = ENB_CD = 0V, unless otherwise specified. (See typical test circuit).



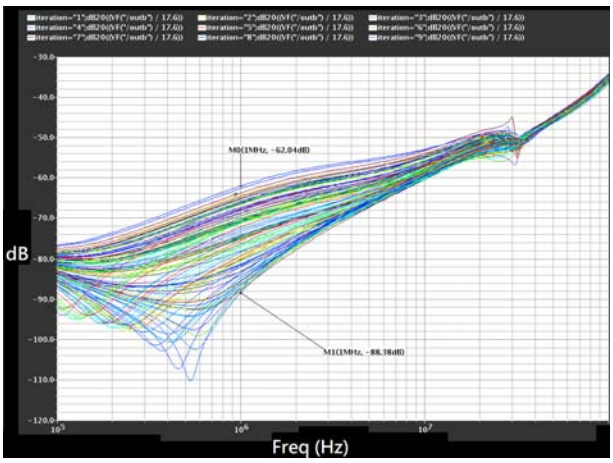
Frequency Response vs R_{IBIAS}



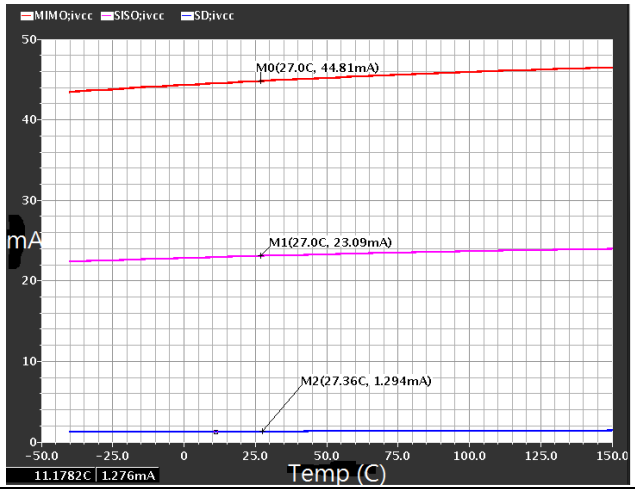
Output Impedance Frequency Response vs R_{IBIAS}



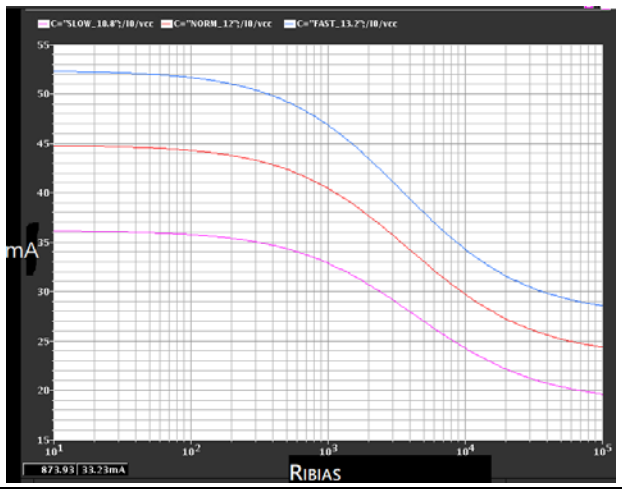
PSRR to Common-mode Output



PSRR to Differential Output



Quiescent Current vs Temperature

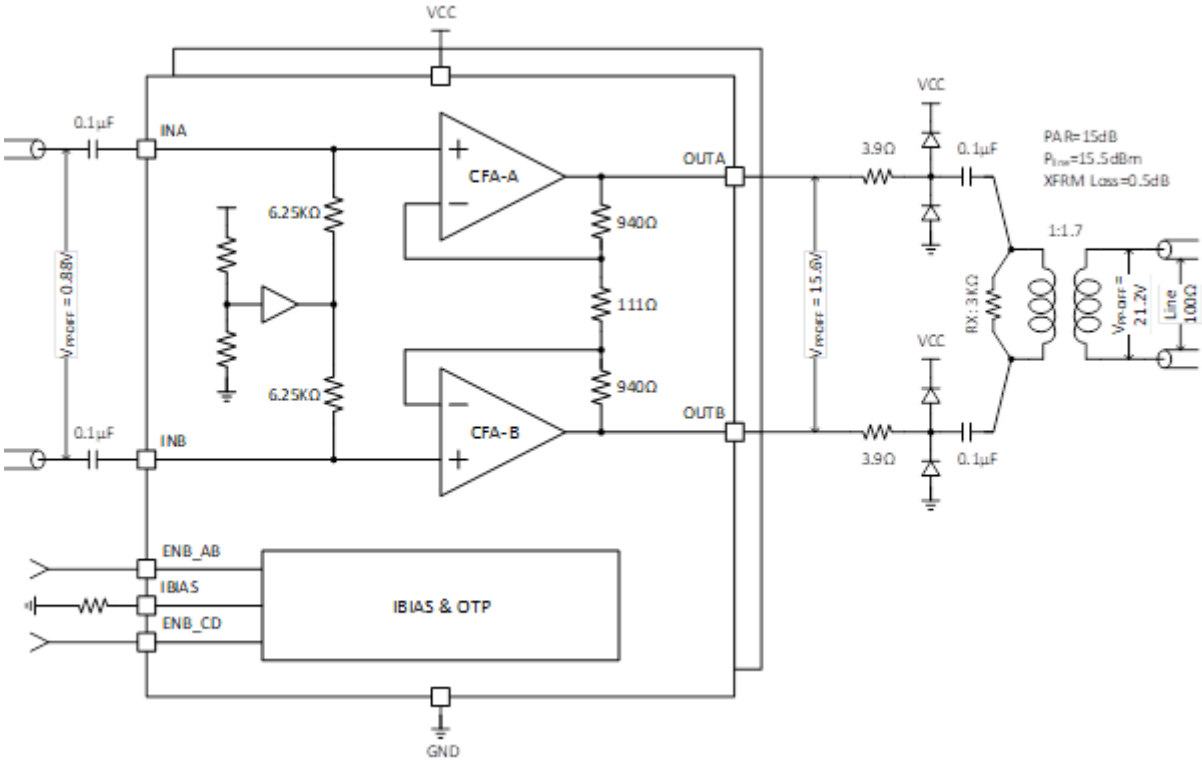


Quiescent Current vs R_{IBIAS}

4. Application Information

The CG1110 is a differential line driver designed for PLC line driver application. The core architecture comprises dual-pairs (four CFAs) high speed current feedback amplifiers.

4.1 Typical Applications



Typical Application and Test Circuit

4.2 Input Common Mode Voltage

The analog inputs of the CG1110 are internally dc biased to VCM=VCC/2 and therefore input pins to CG1110 must be AC coupled using serial 0.1µF ceramic capacitors.

4.3 Bias Current Control

The CG1110 is designed with a biasing current adjustment that lowers the quiescent operating current using an off-chip resistor (R_{IBIAS}) that must be placed between IBIAS pin and GND. Using a resistor larger than 0Ω can reduce the quiescent current of the line driver and improve efficiency. To ensure optimized performance, it is recommended to connect the IBIAS pin to ground.

4.4 Operation State Control

ENB_AB and ENB_CD pins are used as logic inputs to control the line driver operating states. These logic pins are designed to pull high initially, so floating these inputs will put the device in power down mode.

ENB_AB	ENB_CD	Description
0	0	Port AB enable, port CD enable, MIMO mode
0	1	Port AB enable, port CD disable, SISO mode
1	0	Port AB disable, port CD enable, SISO mode
1	1	Port AB disable, port CD disable, Shut down

the various power modes and associated logic states. In the power-down mode, the output of the amplifier goes into a high impedance state.

4.5 Thermal Shutdown

The device has thermal shutdown circuitry that protects the amplifier from damage. The thermal protection circuitry disables the device when the junction temperature reaches approximately 165°C and forces the device to cool. When the junction temperature cools to approximately 140°C, the device is automatically re-enabled.

4.6 Power Dissipation and Thermal Resistance

In order to avoid performance degeneration and device damage, the junction temperature of the device is not allowed to be higher than 150°C for long time. The junction temperature given the ambient temperature is:

$$T_J = T_A + \theta_{JA} \cdot P_D$$

Where, T_J is the absolute junction temperature (°C), T_A is the ambient temperature (°C), θ_{JA} is thermal resistance for junction to ambient (+44°C/W), P_D is the power dissipation in the line driver (W).

4.7 PCB Design Guidelines

4.7.1 Input Considerations:

It is recommended to keep PCB trace length as short as possible and minimize the input parasitic capacitance as much as possible to avoid any ringing or oscillation.

4.7.2 Output Considerations:

The line driver has internal simple current limit protection mechanism but using 3.9Ω series output termination resistors is still recommended to limit output short current. To avoid DC current flow between the two outputs, the AC coupling capacitors are needed in series with the output.

Minimize parasitic capacitance to any ground and power plane for output pins and traces to prevent oscillation.

TVS diodes connected to VCC and GND should be used to absorb the transient energy and clamp the transient voltages of the line driver outputs. To maintain stability, the capacitance of these diodes should be less than 150pF.

4.7.3 IBIAS Considerations:

The bias resistor R_{IBIAS} connected to the IBIAS pin must be routed far away from the components of the signal input network in order to avoid any high frequency signal coupling into the IBIAS pin.

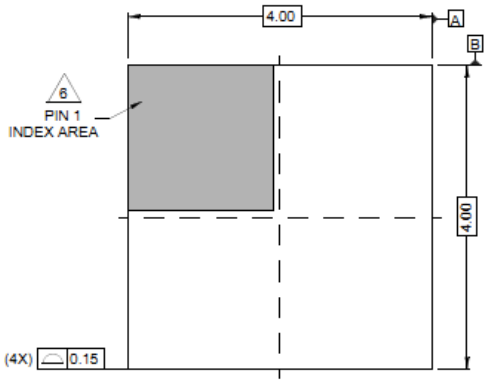
4.7.4 Thermal pad Considerations:

The thermal pad, EPAD, must be soldered to the PCB pad and enough vias need to be used connecting to the bottom plane to dissipate heat out of the package.

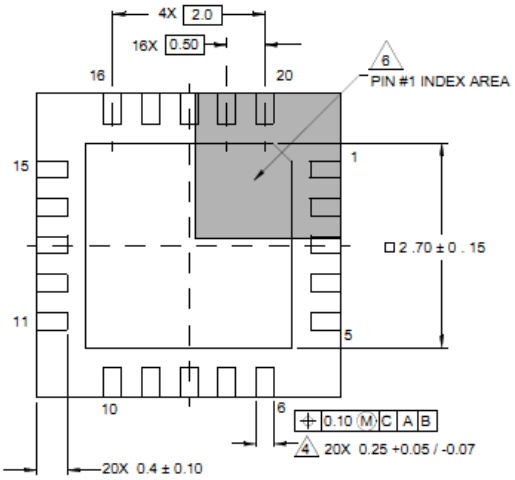
4.7.5 Power Supply

Use 10μF and 0.1μF paralleling decoupling capacitors between power supply and ground. These decoupling capacitors must be close to the power supply pins; minimizing the distance from the pins to high frequency 0.1μF decoupling capacitors.

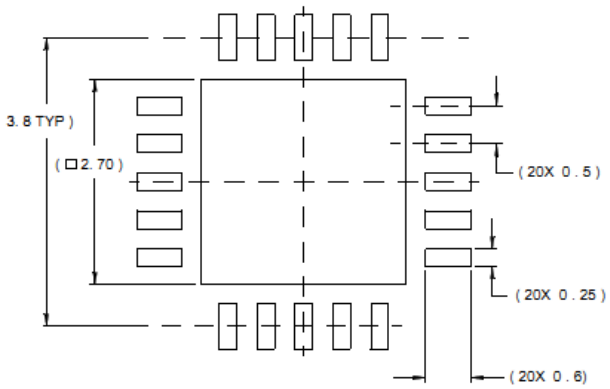
5. Package Outline



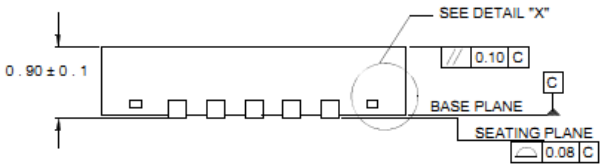
TOP VIEW



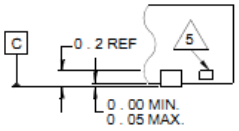
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

Note: The dimension is specified in mm.

6. Ordering Information

Order Part No.	Package	QTY/Reel	Remark
IS31CG1110-QFLS2-TR	QFN-20	2500	

7. Revisions History

Revision	Detail Information	Date
0A	Initial release	2021.02.02

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