

IS31FL3208

18-CHANNEL LED DRIVER; SELECTABLE PWM FREQUENCY

Preliminary Information
March 2018

GENERAL DESCRIPTION

IS31FL3208 is comprised of 18 constant current channels each with independent PWM control, designed for driving LEDs, PWM frequency can be 23kHz (default) or 3.45kHz. The output current of each channel can be set at up to 38mA (Max.) by an external resistor and independently scaled by a factor of 1, 11/12, 9/12 and 7/12. The average LED current of each channel can be changed in 256 steps by changing the PWM duty cycle through an I2C interface.

The chip can be turned off by pulling the SDB pin low or by using the software shutdown feature to reduce power consumption.

IS31FL3208 is available in QFN-28 (4mm × 4mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Four selectable I2C addresses
- Internal reset register
- Modulate LED brightness with 256 steps PWM
- Each channel can be controlled independently
- Each channel can be scaled independently by 1, 11/12, 9/12 and 7/12
- PWM frequency selectable
 - 23kHz (default)
 - 3.45kHz
- -40°C to +125°C temperature range
- QFN-28 (4mm × 4mm) package

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

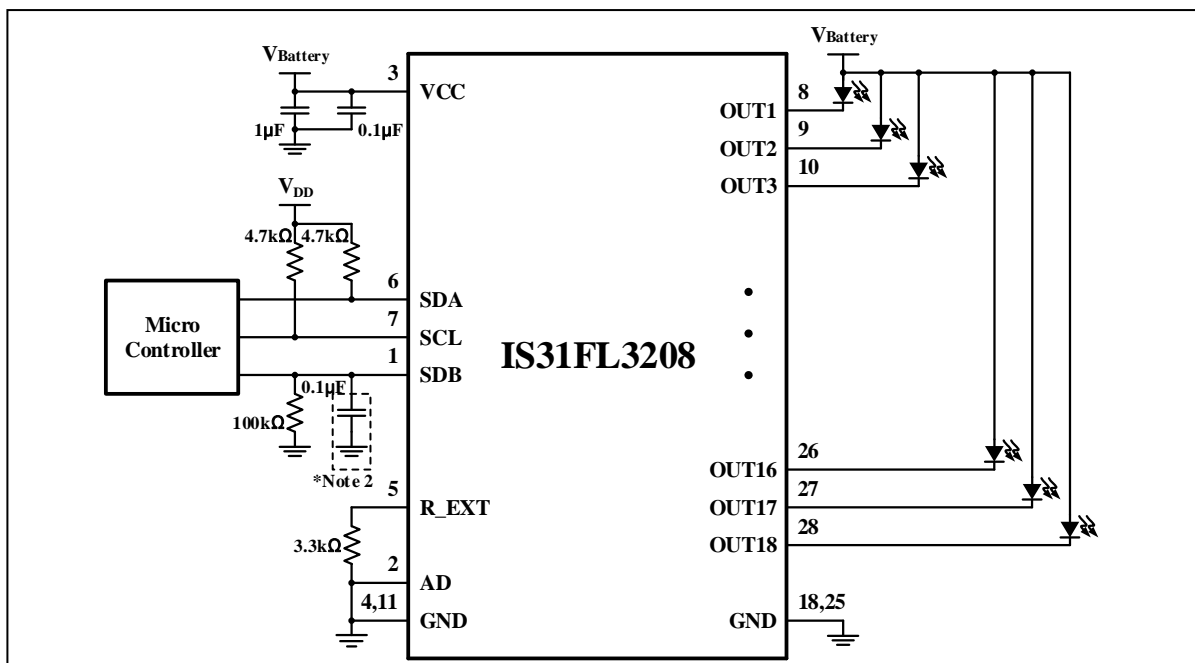


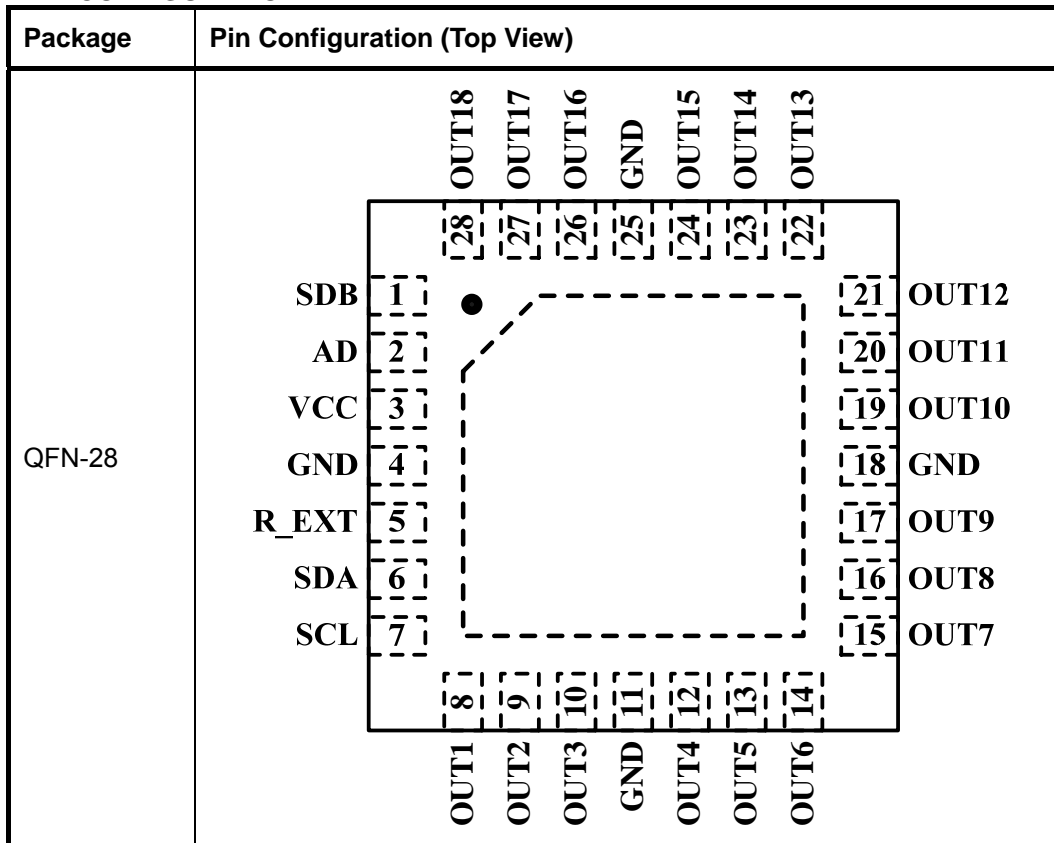
Figure 1 Typical Application Circuit

Note 1: The maximum output current is set to 38mA when $R_{EXT} = 2k\Omega$. Please refer Page 10 for setting LED current.

Note 2: A 0.1µF capacitor is necessary for passing the EFT test.

IS31FL3208

PIN CONFIGURATION



PIN DESCRIPTION

| No. | Pin | Description |
|----------------|---------------|--|
| 1 | SDB | Shutdown the chip when pulled low. |
| 2 | AD | I2C address setting. |
| 3 | VCC | Power supply. |
| 4,11, 18,25 | GND | Ground. |
| 5 | R_EXT | Input terminal used to connect an external resistor. This regulates the global output current. |
| 6 | SDA | I2C serial data. |
| 7 | SCL | I2C serial clock. |
| 8~10 | OUT1~OUT3 | Output channel 1~3 for LEDs. |
| 12~17 | OUT4 ~ OUT9 | Output channel 4~9 for LEDs. |
| 19~24 | OUT10 ~ OUT15 | Output channel 10~15 for LEDs. |
| 26~28 | OUT16 ~ OUT18 | Output channel 16~18 for LEDs. |
| | Thermal Pad | Connect to GND. |



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ORDERING INFORMATION

Industrial Range: -40°C to +125°C

| Order Part No. | Package | QTY/Reel |
|---------------------|-------------------|----------|
| IS31FL3208-QFLS4-TR | QFN-28, Lead-free | 2500 |

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ABSOLUTE MAXIMUM RATINGS

| | |
|--|-----------------------|
| Supply voltage, V_{CC} | -0.3V ~ +6.0V |
| Voltage at SCL, SDA, SDB, OUT1 to OUT18 | -0.3V ~ $V_{CC}+0.3V$ |
| Maximum junction temperature, T_{JMAX} | +150°C |
| Storage temperature range, T_{STG} | -65°C ~ +150°C |
| Operating temperature range, $T_A=T_J$ | -40°C ~ +125°C |
| Package thermal resistance (Mounted on JEDEC standard 4 layer(2s2p) PCB test board), θ_{JA} | 51.4°C/W |
| ESD (HBM) | ±8kV |
| ESD (CDM) | ±1kV |

Note:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values are $T_A = 25^\circ\text{C}$, $V_{CC} = 3.6V$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------------------|--|---|------|------------|------|---------------|
| V_{CC} | Supply voltage | | 2.7 | | 5.5 | V |
| I_{MAX} | Maximum global output current | $V_{CC} = 4.2V$, $V_{OUT} = 0.8V$ $R_{EXT} = 2k\Omega$, SL = “010000” (Note 1) | | 38 | | mA |
| I_{OUT} | Output current | $V_{OUT} = 0.6V$ $R_{EXT} = 3.3k\Omega$, SL = “010000” | | 23 | | mA |
| ΔI_{MATCH} | Output current mismatch between channels | $V_{OUT} = 0.6V$ $R_{EXT} = 3.3k\Omega$, SL = “010000” (Note 2) | -6 | | 6 | % |
| V_{HR} | Headroom voltage | $R_{EXT} = 3.3k\Omega$, $I_{OUT}=20mA$ SL = “010000” | | 0.4 | 0.6 | V |
| I_{CC} | Quiescent power supply current | $R_{EXT} = 3.3k\Omega$ | | 9 | | mA |
| I_{SD} | Shutdown current | $V_{SDB} = 0V$ or software shutdown $T_A = 25^\circ\text{C}$, $V_{CC} = 3.6V$ | | 3 | 5 | μA |
| f_{OUT} | PWM frequency of output | 0x27=0x00 0x27=0x01 | | 23 3.45 | | kHz |
| I_{OZ} | Output leakage current | $V_{SDB} = 0V$ or software shutdown, $V_{OUT} = 5.5V$ | | | 0.2 | μA |
| T_{SHDN} | Thermal shutdown | (Note 2) | | 160 | | °C |
| $T_{SHDNHYST}$ | Hysteresis | (Note 2) | | 20 | | °C |
| V_{EXT} | Output voltage of R-EXT pin | | | 1.3 | | V |

Logic Electrical Characteristics (SDA, SCL, SDB)

| | | | | | | |
|----------|-------------------------|-------------------------------|-----|---|-----|----|
| V_{IL} | Logic “0” input voltage | $V_{CC} = 2.7V\sim 5.5V$ | | | 0.4 | V |
| V_{IH} | Logic “1” input voltage | $V_{CC} = 2.7V\sim 5.5V$ | 1.4 | | | V |
| I_{IL} | Logic “0” input current | $V_{INPUT} = 0V$ (Note 2) | | 5 | | nA |
| I_{IH} | Logic “1” input current | $V_{INPUT} = V_{CC}$ (Note 2) | | 5 | | nA |

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DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 2)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---------------|--|-----------|------|-------------|------|---------|
| f_{SCL} | Serial-Clock frequency | | | | 400 | kHz |
| t_{BUF} | Bus free time between a STOP and a START condition | | 1.3 | | | μ s |
| $t_{HD, STA}$ | Hold time (repeated) START condition | | 0.6 | | | μ s |
| $t_{SU, STA}$ | Repeated START condition setup time | | 0.6 | | | μ s |
| $t_{SU, STO}$ | STOP condition setup time | | 0.6 | | | μ s |
| $t_{HD, DAT}$ | Data hold time | | | | 0.9 | μ s |
| $t_{SU, DAT}$ | Data setup time | | 100 | | | ns |
| t_{LOW} | SCL clock low period | | 1.3 | | | μ s |
| t_{HIGH} | SCL clock high period | | 0.7 | | | μ s |
| t_R | Rise time of both SDA and SCL signals, receiving | (Note 3) | | $20+0.1C_b$ | 300 | ns |
| t_F | Fall time of both SDA and SCL signals, receiving | (Note 3) | | $20+0.1C_b$ | 300 | ns |

Note 1: The recommended minimum value of R_{EXT} is 2k Ω , or it may cause a large current.

Note 2: $\Delta I_{MATCH} = (I_{OUT} - I_{AVG}) / I_{AVG} \times 100\%$. $I_{AVG} = (I_{OUT1} + I_{OUT2} + \dots + I_{OUT18}) / 18$.

Note 3: Guaranteed by design.

Note 4: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

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DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3208 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3208 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Since IS31FL3208 only supports write operations, A0 must always be "0". The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write only):

| Bit | A7:A3 | A2:A1 | A0 |
|-------|-------|-------|----|
| Value | 11011 | AD | 0 |

AD connected to GND, AD = 00;
 AD connected to VCC, AD = 11;
 AD connected to SCL, AD = 01;
 AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3208.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3208's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3208 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3208, the register address byte is sent, most significant bit first. IS31FL3208 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3208 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3208, load the address of the data register that the first data byte is intended for. During the IS31FL3208 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3208 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3208 (Figure 5).

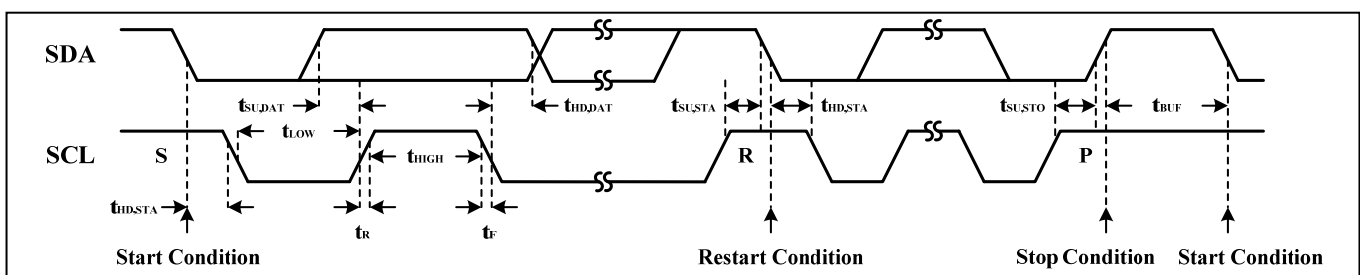


Figure 2 Interface Timing

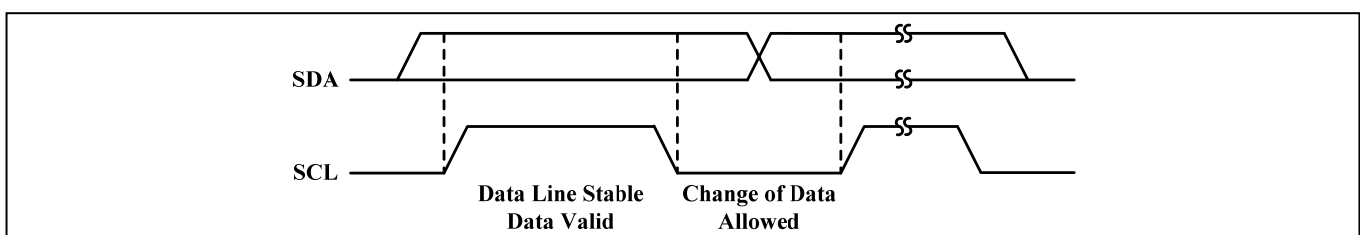


Figure 3 Bit Transfer

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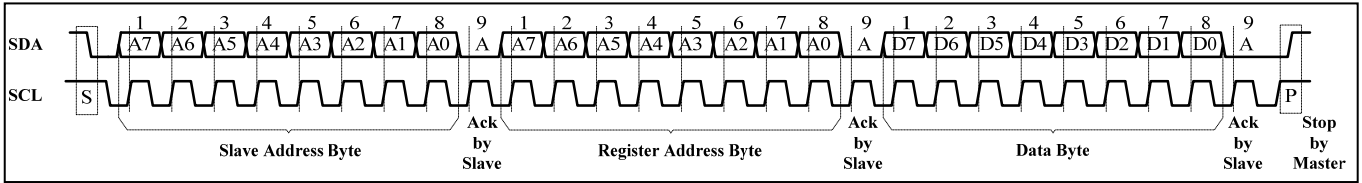


Figure 4 Writing to IS31FL3208 (Typical)

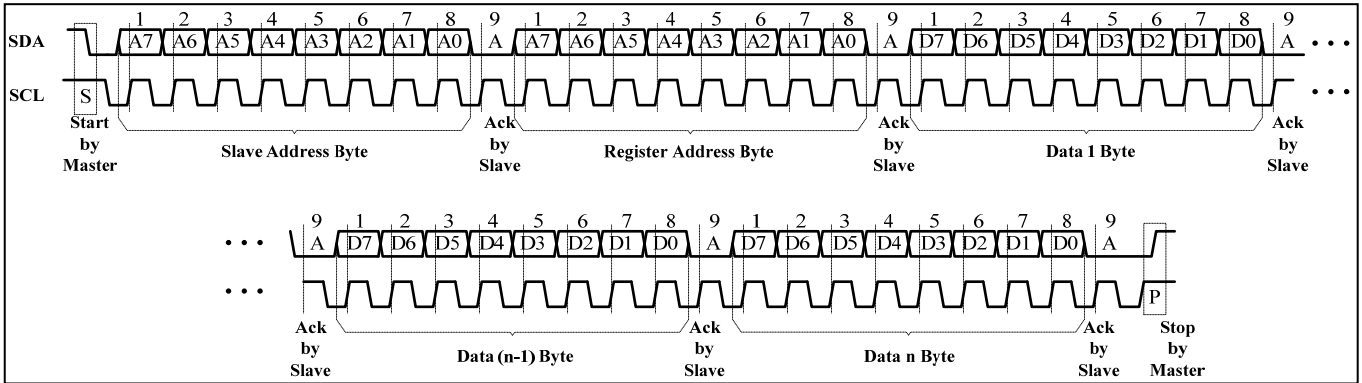


Figure 5 Writing to IS31FL3208 (Automatic Address Increment)

REGISTERS DEFINITIONS

Table 2 Register Function

| Address | Name | Function | Table | Default |
|---------|-----------------------------------|---|-------|-----------|
| 00h | Shutdown Register | Set software shutdown mode | 3 | 0000 0000 |
| 01h~12h | PWM Register | 18 channels PWM duty cycle data register | 4 | |
| 13h | Update Register | Load PWM Register and LED Control Register's data | - | 0000 0000 |
| 14h~25h | LED Control Register | Channel 1 to 18 enable bit and current setting | 5 | 0000 0000 |
| 26h | Global Control Register | Set all channels enable | 6 | |
| 27h | Output Frequency Setting Register | Set all channels operating frequency | 7 | |
| 2Fh | Reset Register | Reset all registers into default value | - | 0000 0000 |

Table 3 00h Shutdown Register

| Bit | D7:D1 | D0 |
|---------|----------|-----|
| Name | - | SSD |
| Default | 0000 000 | 0 |

The Shutdown Register sets software shutdown mode of IS31FL3208.

| | |
|------------|--------------------------|
| SSD | Software Shutdown Enable |
| 0 | Software shutdown mode |
| 1 | Normal operation |

Table 4 01h~12h PWM Register (OUT1~OUT18)

| Bit | D7:D0 |
|---------|-----------|
| Name | PWM |
| Default | 0000 0000 |

The PWM Registers adjusts LED luminous intensity in 256 steps.

The value of a channel's PWM Register decides the average output current for each output, OUT1~OUT18. The average output current may be computed using the Formula (1):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^7 D[n] \cdot 2^n \quad (1)$$

Where "n" indicates the bit location in the respective PWM register.

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For example: D7:D0 = 10110101,

$$I_{OUT} = I_{MAX} (2^0 + 2^2 + 2^4 + 2^5 + 2^7) / 256$$

The I_{OUT} of each channel is setting by the SL bit of LED Control Register (14h~25h). Please refer to the detail information in Page 10.

13h PWM Update Register

The data sent to the PWM Registers and the LED Control Registers will be stored in temporary registers. A write operation of "0000 0000" value to the Update Register is required to update the registers (01h~12h, 14h~25h).

Table 5 14h~25h LED Control Register (OUT1~OUT18)

| Bit | D7:D6 | D5:D0 |
|---------|-------|---------|
| Name | - | SL |
| Default | 00 | 00 0000 |

The LED Control Registers store the on or off state of each LED and set the output current.

| SL | HEX | Output Current (I_{OUT}) |
|--------|------|------------------------------|
| 010000 | 0x10 | $I_{OUT} = I_{MAX}$ |
| 010001 | 0x11 | $I_{OUT} = 11/12 I_{MAX}$ |
| 010010 | 0x12 | $I_{OUT} = 9/12 I_{MAX}$ |
| 010011 | 0x13 | $I_{OUT} = 7/12 I_{MAX}$ |
| 00xxxx | 0x0x | $I_{OUT} = 0$ |
| Others | | Not allowed |

Table 6 26h Global Control Register

| Bit | D7:D1 | D0 |
|---------|----------|------|
| Name | - | G_EN |
| Default | 0000 000 | 0 |

The Global Control Register set all channels enable.

G_EN Global LED Enable

| | |
|---|-------------------|
| 0 | Normal operation |
| 1 | Shutdown all LEDs |

Table 7 27h Output Frequency Setting Register

| Bit | D7:D1 | D0 |
|---------|---------|-----|
| Name | - | OFS |
| Default | 0000000 | 0 |

The Output Frequency Setting Register selects a fixed PWM operating frequency for all output channels.

OFS Output Frequency Setting

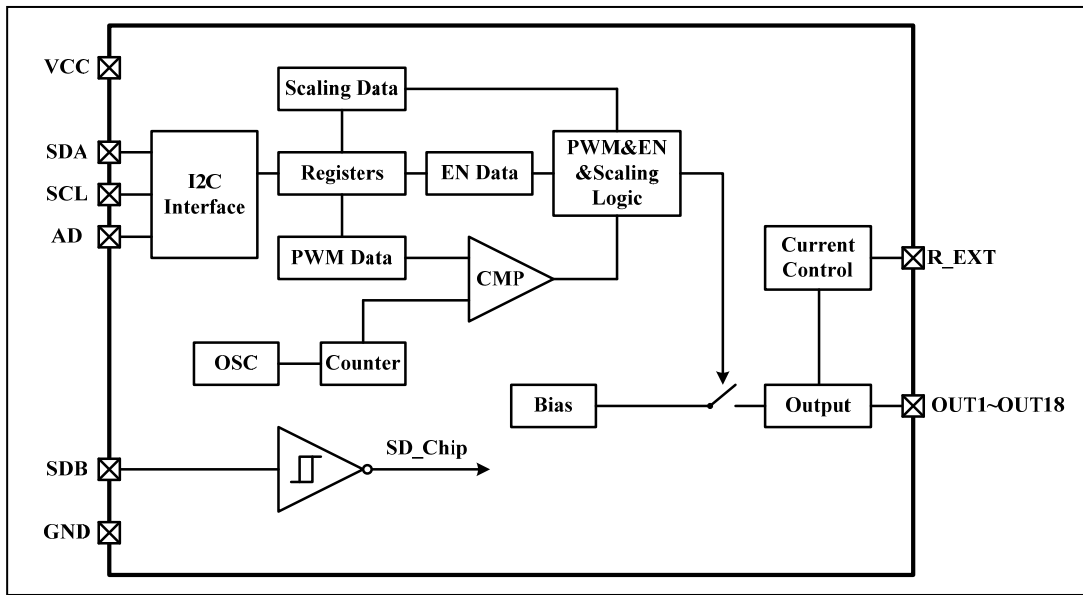
| | |
|---|---------|
| 0 | 23kHz |
| 1 | 3.45kHz |

2Fh Reset Register

Once user writes "0000 0000" data to the Reset Register, IS31FL3208 will reset all registers to default value. On initial power-up, the IS31FL3208 registers are reset to their default values for a blank display.

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FUNCTIONAL BLOCK DIAGRAM



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TYPICAL APPLICATION INFORMATION

PWM CONTROL

The PWM Registers (01h~12h) can modulate LED brightness of 18 channels with 256 steps. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

R_{EXT}

The maximum output current of OUT1~OUT18 can be adjusted by the external resistor, R_{EXT}, as described in Formula (2).

$$I_{MAX} = x \cdot \frac{V_{EXT}}{R_{EXT}} \quad (2)$$

x = 58.5, V_{OUT} = 0.8V, V_{EXT} = 1.3V.

The recommended minimum value of R_{EXT} is 2kΩ.

CURRENT SETTING

The current of each LED can be set independently by the SL bit of LED Control Register (14h~25h). The maximum global current is set by the external register R_{EXT}.

When channels drive different quantity of LEDs, adjust maximum output current according to quantity of LEDs to ensure average current of each LED is the same.

For example, set R_{EXT}= 3.3kΩ then I_{MAX}= 23mA.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3208 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 8 32 Gamma Steps With 256 PWM Steps

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
| 0 | 1 | 2 | 4 | 6 | 10 | 13 | 18 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 22 | 28 | 33 | 39 | 46 | 53 | 61 | 69 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 78 | 86 | 96 | 106 | 116 | 126 | 138 | 149 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 161 | 173 | 186 | 199 | 212 | 226 | 240 | 255 |

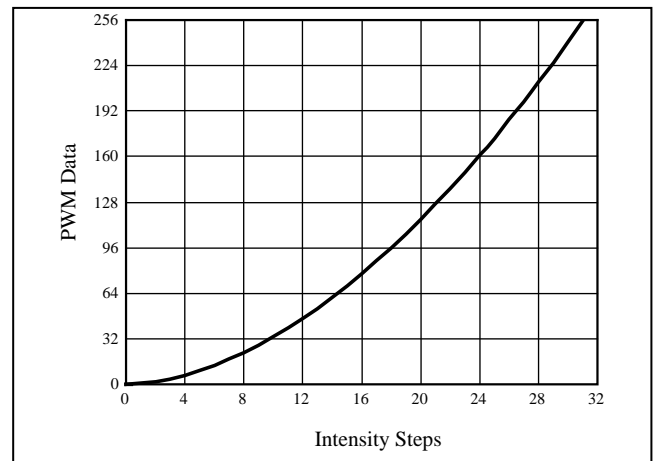


Figure 6 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 9 64 Gamma Steps With 256 PWM Steps

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 24 | 26 | 29 | 32 | 35 | 38 | 41 | 44 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 47 | 50 | 53 | 57 | 61 | 65 | 69 | 73 |
| C(32) | C(33) | C(34) | C(35) | C(36) | C(37) | C(38) | C(39) |
| 77 | 81 | 85 | 89 | 94 | 99 | 104 | 109 |
| C(40) | C(41) | C(42) | C(43) | C(44) | C(45) | C(46) | C(47) |
| 114 | 119 | 124 | 129 | 134 | 140 | 146 | 152 |
| C(48) | C(49) | C(50) | C(51) | C(52) | C(53) | C(54) | C(55) |
| 158 | 164 | 170 | 176 | 182 | 188 | 195 | 202 |
| C(56) | C(57) | C(58) | C(59) | C(60) | C(61) | C(62) | C(63) |
| 209 | 216 | 223 | 230 | 237 | 244 | 251 | 255 |

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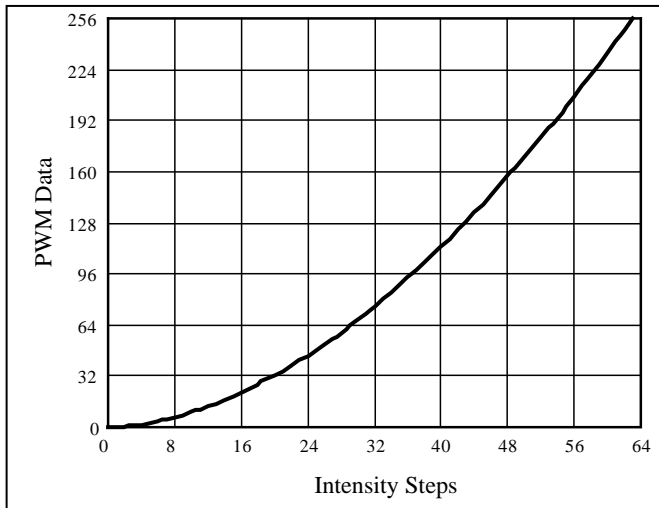


Figure 7 Gamma Correction (64 Steps)

Note, the data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (00h) to “0”, the IS31FL3208 will operate in software shutdown mode. When the IS31FL3208 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low.

PWM FREQUENCY SELECT

The IS31FL3208 output channels operate with a default PWM frequency of 23kHz. Because all the OUTx channels are synchronized, the DC supply will

experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors.

When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, To avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3208’s output PWM frequency above the audible range. The Output Frequency Setting Register 27h bit D0 can be used to set the switching frequency to 23kHz (Default), which is beyond the audible range. Figure 8 below shows the variation of output PWM frequency across supply voltage and temperature.

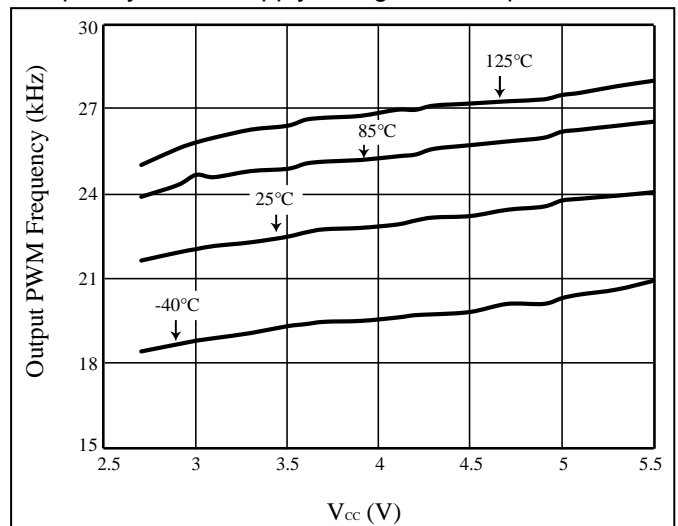


Figure 8 Output PWM Frequency vs. Vcc

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CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|------------------|
| Preheat & Soak | |
| Temperature min (T _{smin}) | 150°C |
| Temperature max (T _{smax}) | 200°C |
| Time (T _{smin} to T _{smax}) (t _s) | 60-120 seconds |
| Average ramp-up rate (T _{smax} to T _p) | 3°C/second max. |
| Liquidous temperature (T _L) | 217°C |
| Time at liquidous (t _L) | 60-150 seconds |
| Peak package body temperature (T _p)* | Max 260°C |
| Time (t _p)** within 5°C of the specified classification temperature (T _c) | Max 30 seconds |
| Average ramp-down rate (T _p to T _{smax}) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

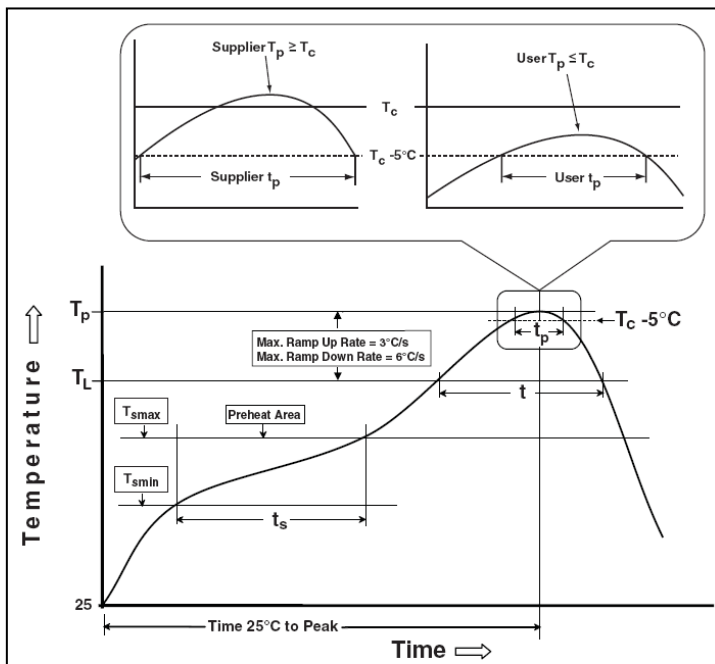
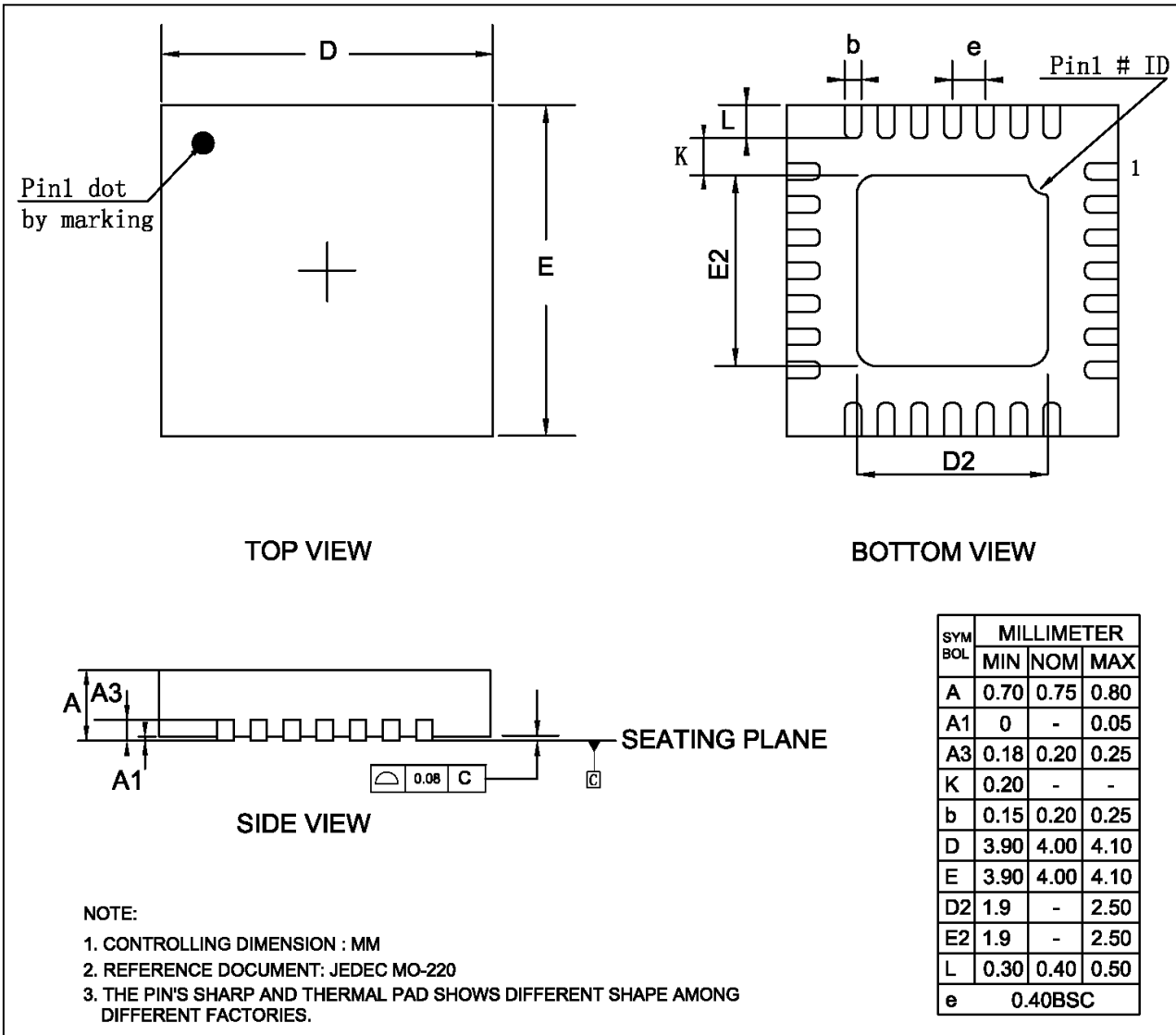


Figure 9 Classification Profile

IS31FL3208

PACKAGE INFORMATION

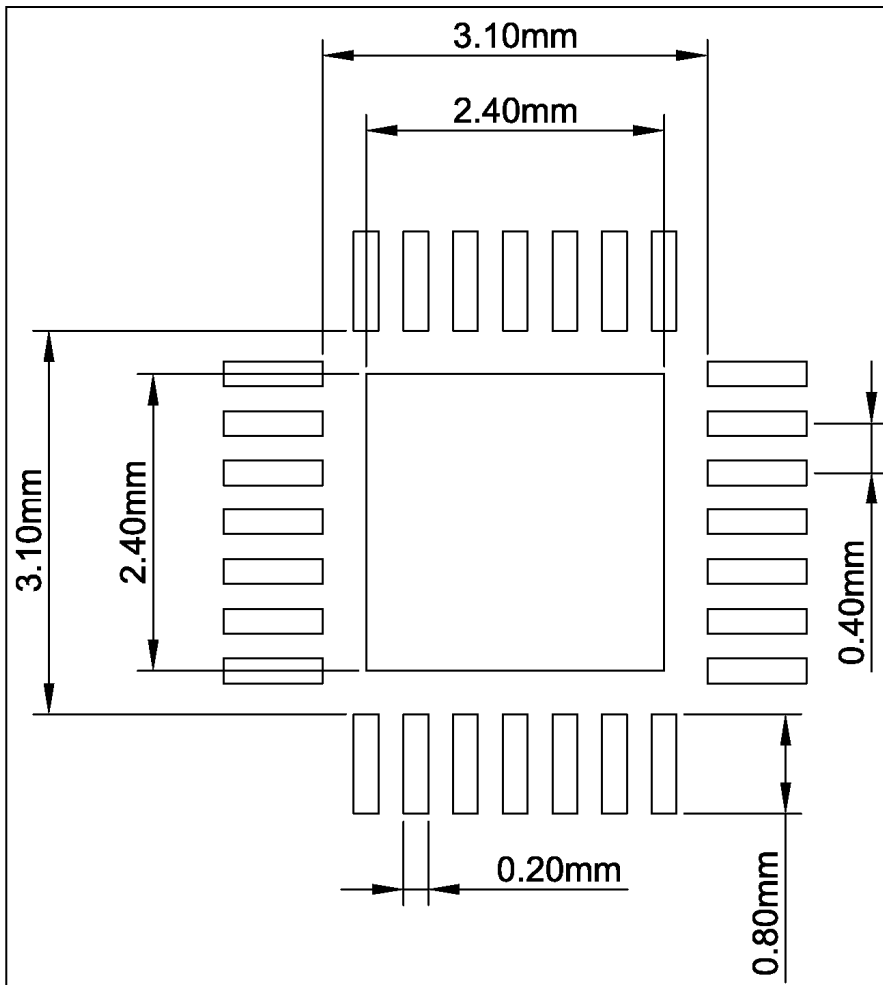
QFN-28



IS31FL3208

RECOMMENDED LAND PATTERN

QFN-28



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.



IS31FL3208

REVISION HISTORY

| Revision | Detail Information | Date |
|----------|---|------------|
| 0A | Initial release. | 2017.09.11 |
| 0B | <ol style="list-style-type: none">1. Update Figure 1 ($R_{EXT}=3.3k\Omega$).2. Add ΔI_{MATCH} item in EC table.3. Change the V_{IH}, V_{IL} test condition to $V_{CC} = 2.7V\sim 5.5V$ in EC table.4. Add ESD value | 2018.02.08 |

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