8×8/7×9 MATRIX LED DRIVER

January 2021

GENERAL DESCRIPTION

The IS31FL3739 is a general purpose 8×8 or 7×9 matrix LED driver programmed via a 1MHz I2C bus compatible interface. Each LED can be dimmed individually with 8-bit PWM data, and each CSx has 8-bit DC current scaling for color calibration. The combination enables 256 steps of linear PWM dimming for each dot and 256 steps of DC current adjustment for each CSx.

Additionally, the open or short state of each LED can be detected and stored in Open-Short Registers. The MCU can then read the Open-Short Registers via the I2C bus and identify which LED in the array is open or short.

The IS31FL3729 features a very low shutdown and quiescent (operational) current. It also supports selectable noise reduction features such as PWM clock spread spectrum and 180 degree phase shifting.

IS31FL3739 is available in SOP-24 package. It operates from 2.7V to 5.5V over the full temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 8 current sinks
- Support 8×n (n=1~8), 7×9 LED matrix configurations
- Individual 256 PWM control steps
- 256 DC current steps for each CSx
- 64 global current steps
- SDB rising edge resets the I2C interface
- Register programmable PWM frequency - 0.25kHz to 80kHz
- 1MHz I2C-compatible interface
- Individual open and short error detect function
- PWM 180 degree phase shift
- Spread spectrum
- De-ghost
- SOP-24 package

APPLICATIONS

- White goods LED display panel.
- IOT device

TYPICAL APPLICATION CIRCUIT

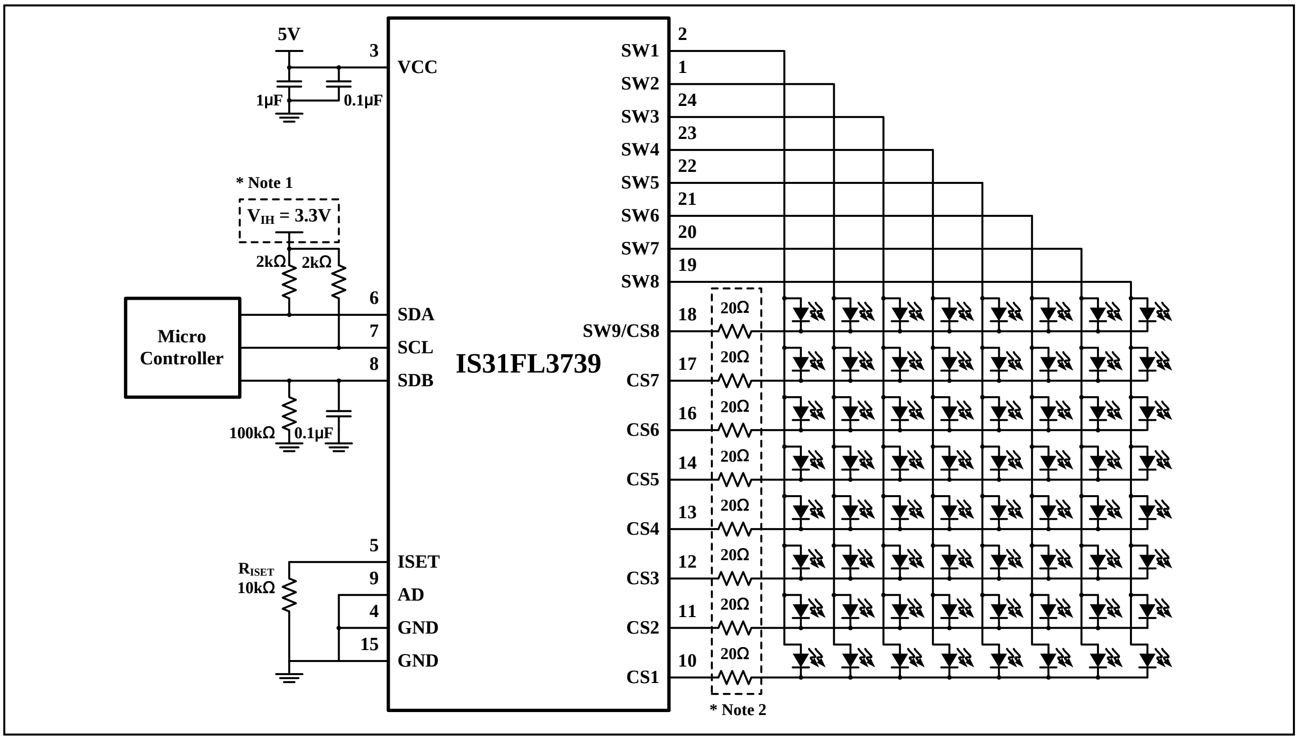


Figure 1 Typical Application Circuit (8×8)

Note 1: The VIH of I2C bus should be smaller than VCC. And if VIH is lower than 3.0V, it is recommended add a level shift circuit to avoid extra shutdown current.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3729, for mono red/yellow/orange LED, if $PV_{CC}=V_{CC}$=3.3V, don't need these resistors.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

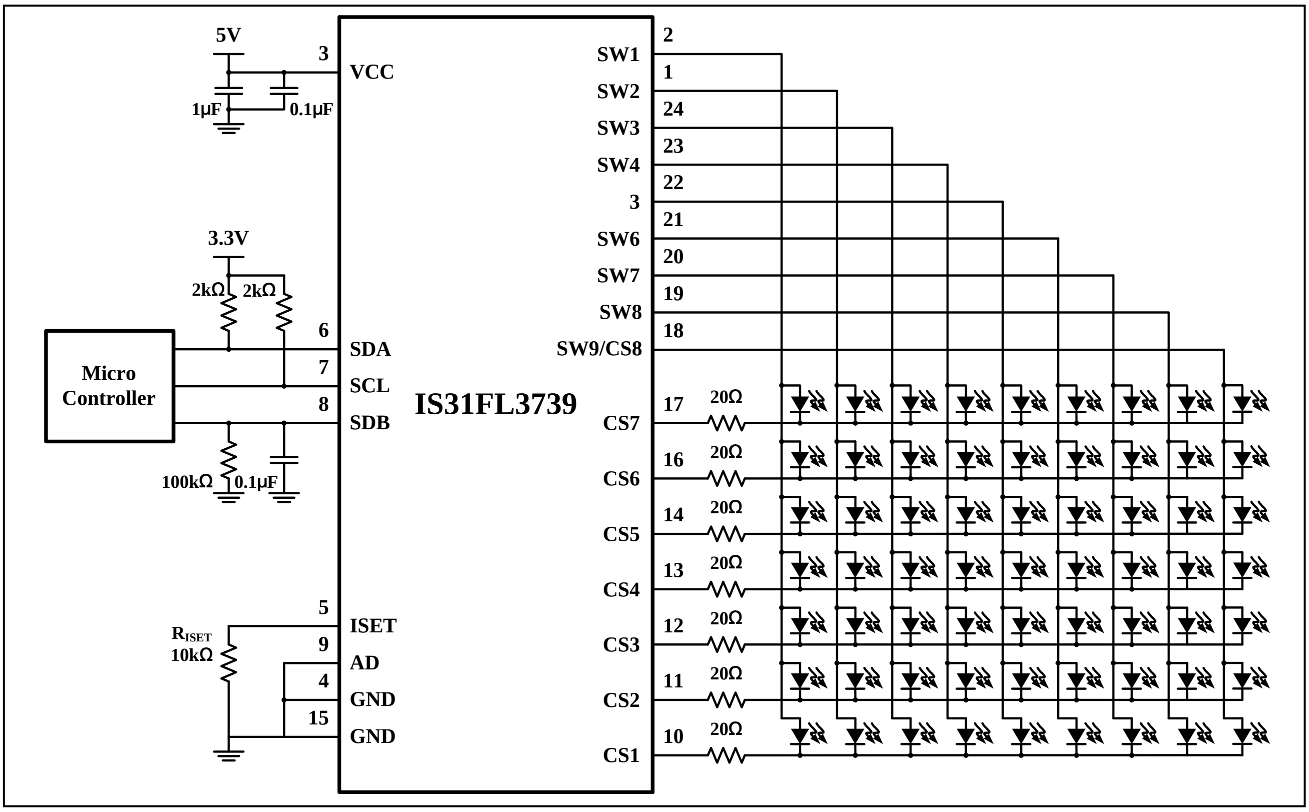


Figure 2 Typical Application Circuit (7×9)

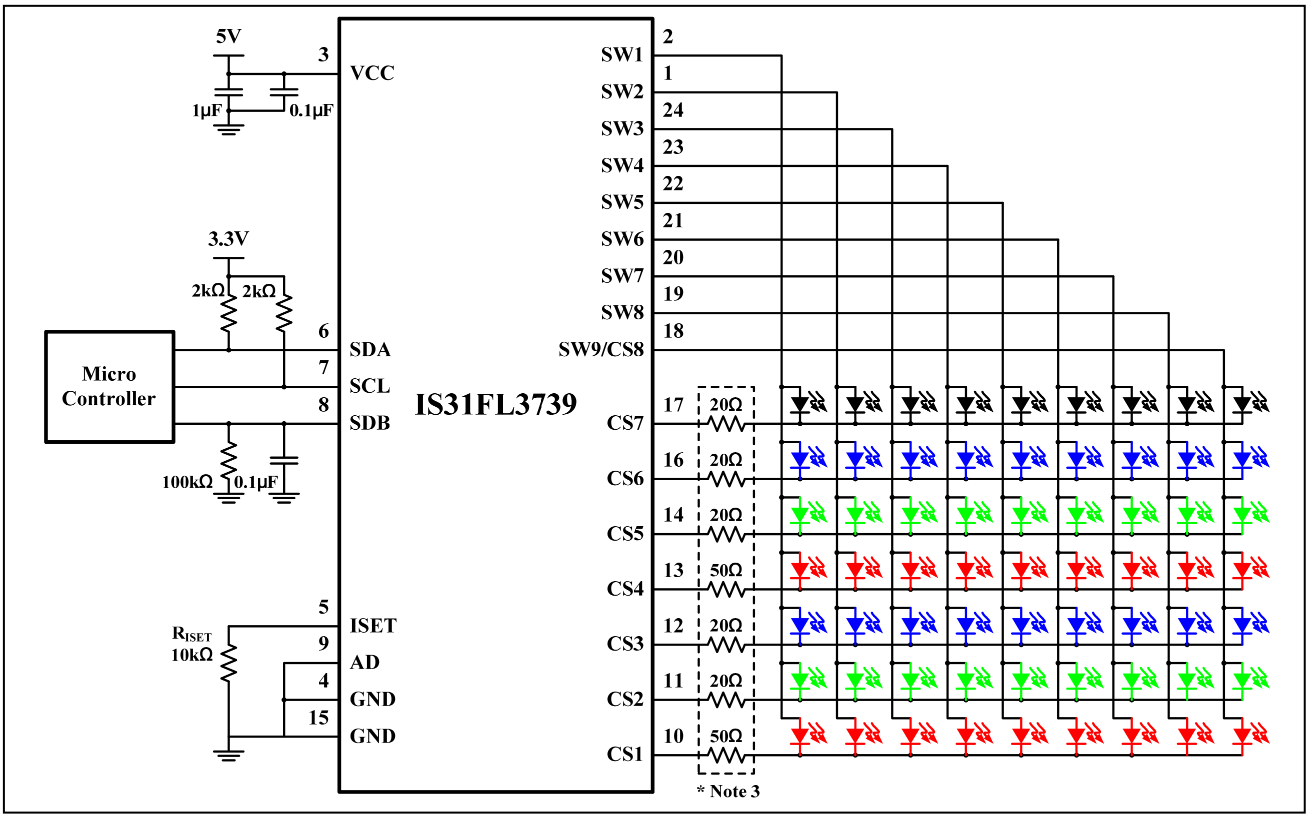
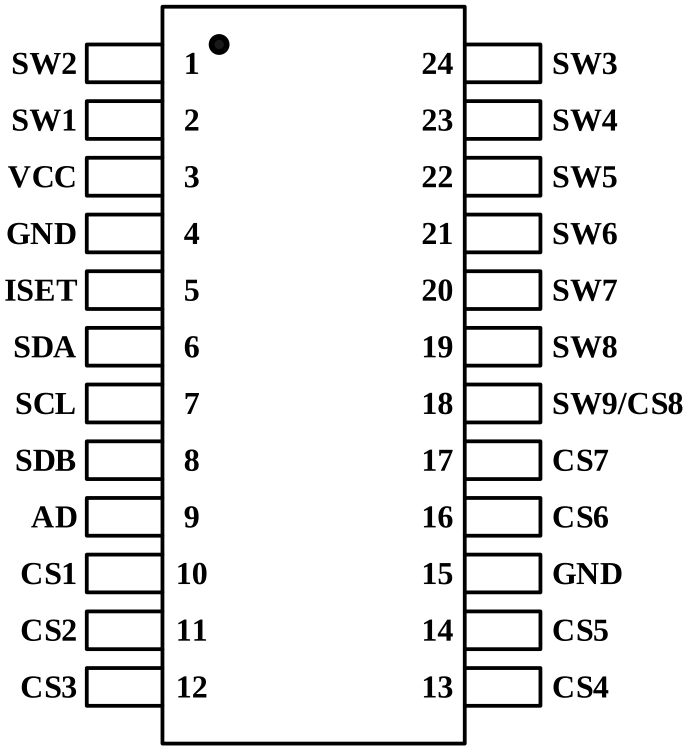


Figure 3 Typical Application Circuit (18 RGBs)

Note 3: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3729, for red LED, it is recommended to use about 30Ω more than blue/green LED, to offload more extra voltage due to lower forward voltage of red LED.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-24	



PIN DESCRIPTION

No.	Pin	Description
1, 2	SW2, SW1	Switch power source.
3	VCC	Power supply.
4, 15	GND	Ground.
5	ISET	Current setting pin.
6	SDA	Serial data.
7	SCL	Serial clock.
8	SDB	Shutdown the chip when pull to low.
9	AD	I2C Address setting.
10~14	CS1~CS5	Current sinks output.
16, 17	CS6, CS7	Current sinks output.
18	SW9/CS8	Switch power source or current sink output.
19~24	SW8~SW3	Switch power source.
	Thermal Pad	Need to connect to GND pins.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3739-GRLS4-TR	SOP-24, Lead-free	1500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	41°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

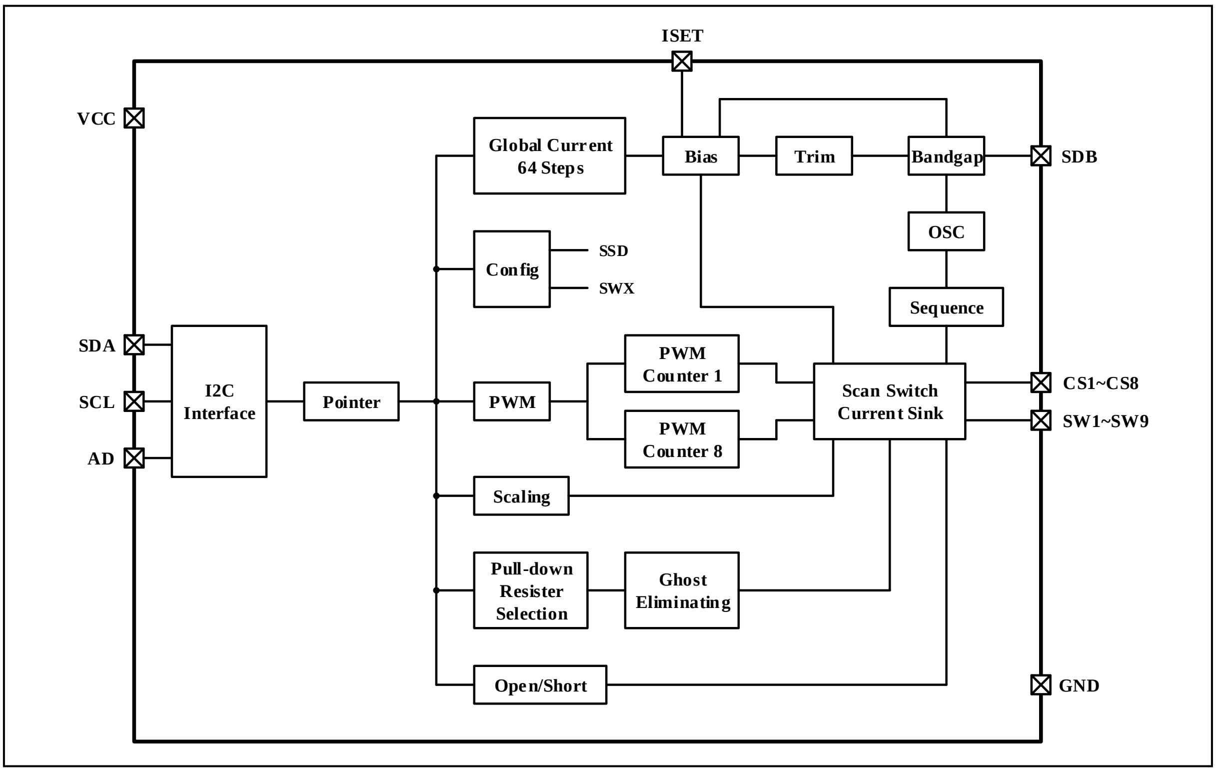
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= $V_{CC,}$ all LEDs off		2	3	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		3	5	μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000"		3	5	
I_{OUT}	Maximum constant current of CSx	R_{ISET}= 10kΩ, GCC= "100 0000" SL= 0xFF	31.5	35	38.5	mA
I_{LED}	Average current on each LED I_{LED} = $I_{OUT(PEAK)}$/Duty	R_{ISET}= 10kΩ, GCC= "100 0000" SL= 0xFF, n= 8, Duty= 1/8.29		4.22		mA
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}= 600mA R_{ISET}= 10kΩ, GCC= "100 0000", SL= 0xFF		500	550	mV
	Current sink headroom voltage CSx	I_{SINK}= 34mA, R_{ISET}= 10kΩ, GCC= "100 0000", SL= 0xFF		400	500	
t_{SCAN}	Period of scanning	B2h= "0x01" (PWM frequency= 32kHz)	22	30	46	μs
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	B2h= "0x01" (PWM frequency= 32kHz)	0.3	0.8	1.2	μs
t_{NOL2}	Delay total time for CS1 to CS8, during this time, the SWx is on but CSx is not all turned on	B2h= "0x01" (PWM frequency= 32kHz)	0.1	0.27	0.4	μs
Logic Electrical Characteristics (SDA, SCL, AD, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V, LGC= "0"	GND		0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V, LGC= "0"	1.4		V_{CC}	V
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V, LGC= "1"	GND		0.6	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V, LGC= "1"	2.4		V_{CC}	V
V_{HYS}	Input schmitt trigger hysteresis	V_{CC}= 3.6V, LGC= "0", LGC= "1"		0.2		V
I_{IL}	Logic "0" input current	SDB= L, V_{INPUT}= L (Note 5)		5		nA
I_{IH}	Logic "1" input current	SDB= L, V_{INPUT}= H (Note 5)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 5: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3739 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3739 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

Table 1 Slave Address

AD	A7:A3	A2:A1	A0
GND	01101	00	0/1
SCL		01	
SDA		10	
VCC		11	

AD connected to GND, A2:A1=00;
AD connected to VCC, A2:A1=11;
AD connected to SCL, A2:A1=01;
AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3739.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3739's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3739 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3739, the register address byte is sent, most significant bit first. IS31FL3739 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3739 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3739, load the address of the data register that the first data byte is intended for. During the IS31FL3739 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3739 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3739 (Figure 7).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3739 device address with the $R/\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3739 device address with the $R/\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3739 to the master (Figure 8).

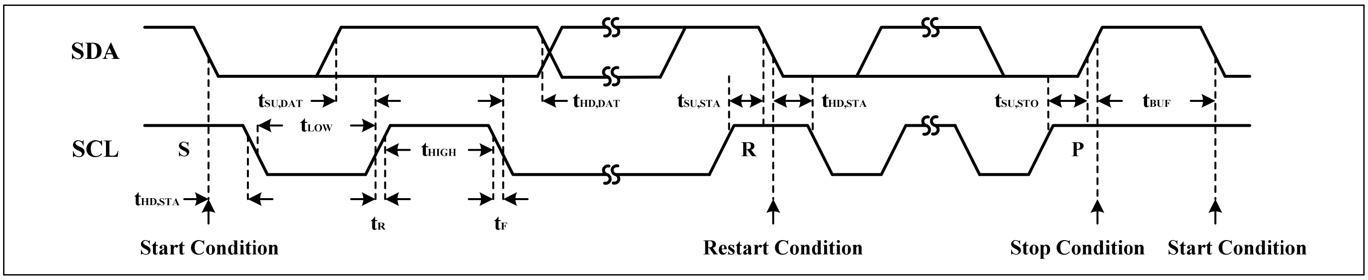


Figure 4 I2C Interface Timing

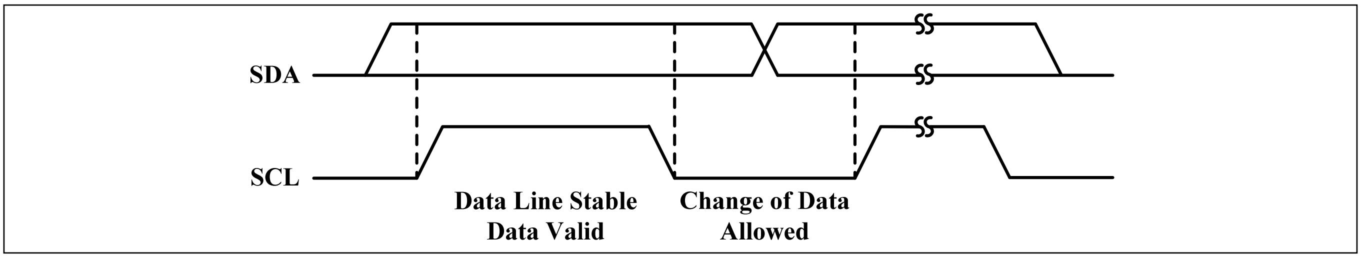


Figure 5 I2C Bit Transfer

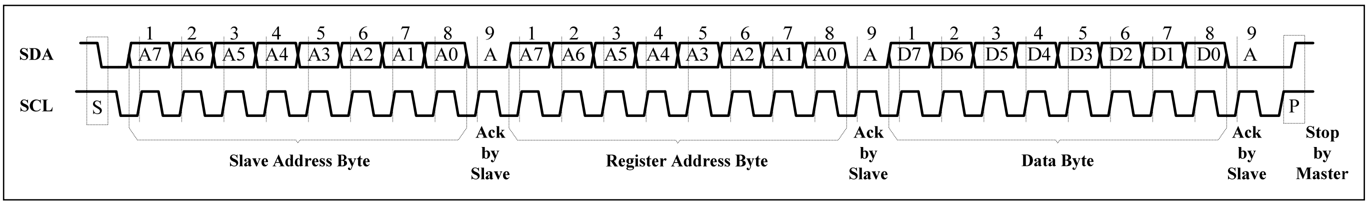


Figure 6 I2C Writing to IS31FL3739 (Typical)

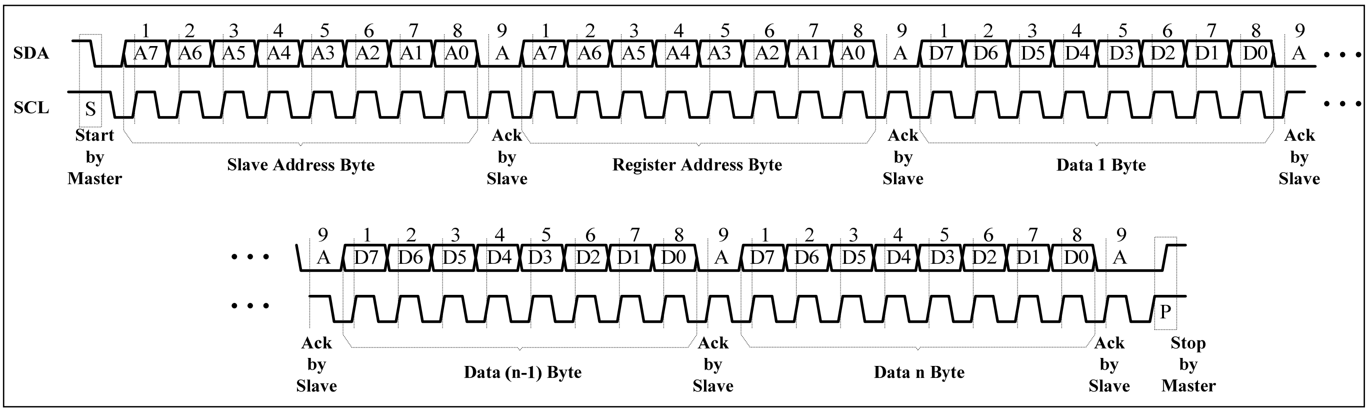


Figure 7 I2C Writing to IS31FL3739 (Automatic Address Increment)

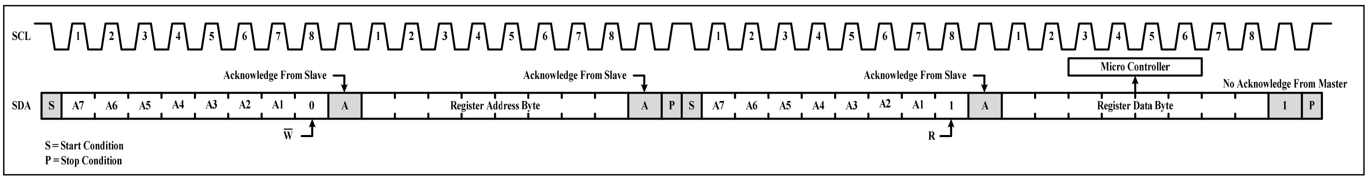


Figure 8 I2C Reading from IS31FL3739

Table 5 Register Definition

Address	Name	Function	Table	R/W	Default
03h~8Fh	PWM Register	Set PWM value for LED	6	R/W	0000 0000
92h~9Fh	Scaling Register	Control the DC output current of each CSy	7	R/W	0000 0000
A0h	Configuration Register	Configure the operation mode	8	R/W	0001 0000
A1h	Global Current Control Register	Set the global current	9	R/W	0000 0000
B0h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and pull up resistor for CSy	10	R/W	0011 0011
B1h	Spread Spectrum Register	Spread spectrum function enable	11	R/W	0000 0000
B2h	PWM Frequency Register	Set the PWM frequency	12	R/W	0000 0001
B3h~C4h	Open/Short Register	Store the open or short information	13-1	R/W	x000 00xx
			13-2	R/W	000x xxxx
CFh	Reset Register	Reset all register to POR state	-	W	0000 0000

PWM Register

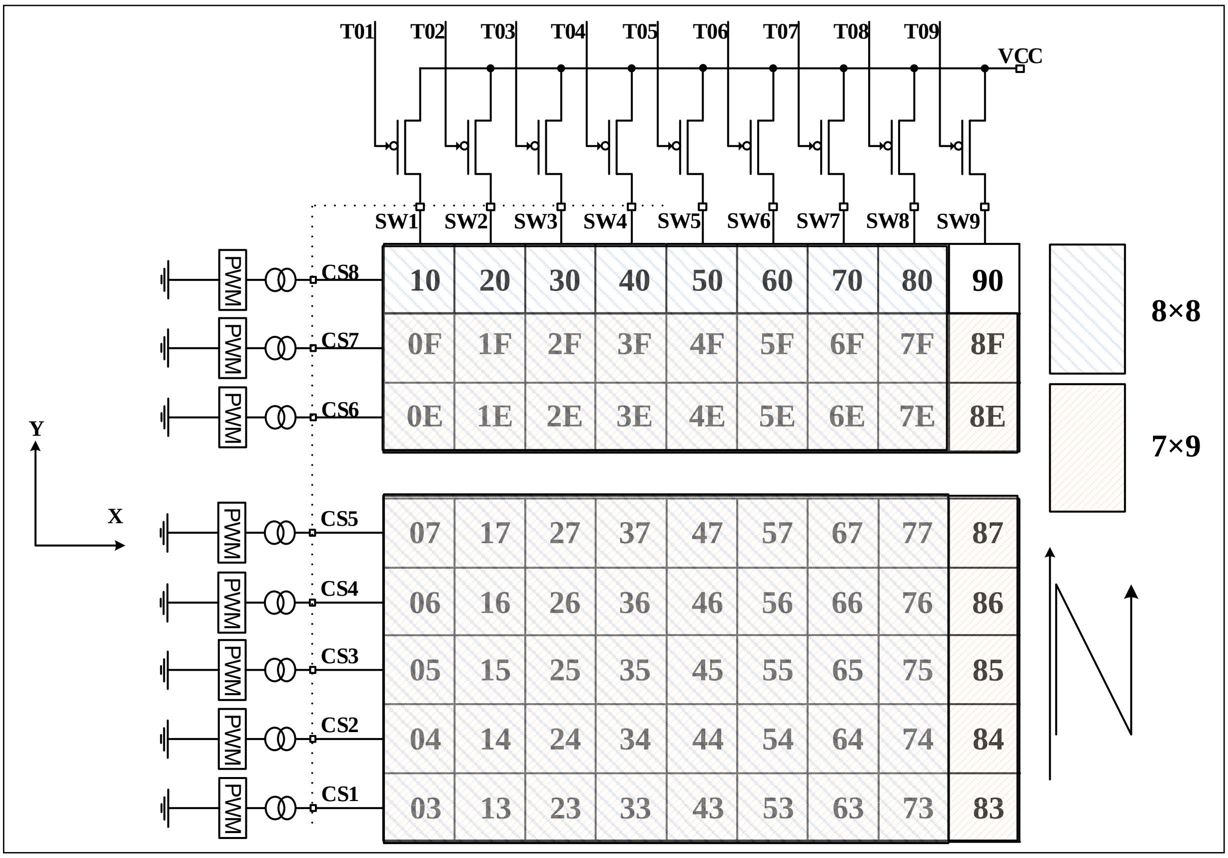


Figure 9 PWM Register

Note 6: The above register address is in hexadecimal format.

Table 6 03h~8Fh PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has a byte to modulate the PWM duty in 256 steps. The PWM clock frequency is set by the PWM Frequency Register (B2h). The following calculations assume B2h is configured for 32kHz PWM, B2h= "0x01" for t_{SCAN}=30μs, the period of scanning and 0.8μs is t_{NOL1}, the non-overlap time and 0.27μs is the CSx delay time.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \qquad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx, when n=9,

$$Duty = \frac{30\mu s}{(30\mu s + 0.8\mu s + 0.27\mu s)} \times \frac{1}{9} = \frac{1}{9.32} \qquad (2)$$

When n=8,

$$Duty = \frac{30\mu s}{(30\mu s + 0.8\mu s + 0.27\mu s)} \times \frac{1}{8} = \frac{1}{8.29} \qquad (2)$$

I_{OUT} is the output current of CSy (y=1~8),

$$I_{OUT(PEAK)} = \frac{342}{R_{ISET}} \times \frac{GCC}{64} \times \frac{SL}{256} \qquad (3)$$

GCC is the Global Current Control Register (A1h) value, SL is the Scaling Register value as Table 9 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC= 100 0000, R_{ISET}=10kΩ, SL=1111 1111:

$$I_{LED} = \frac{342}{10k\Omega} \times \frac{64}{64} \times \frac{255}{256} \times \frac{1}{9.32} \times \frac{181}{256}$$

Scaling Register

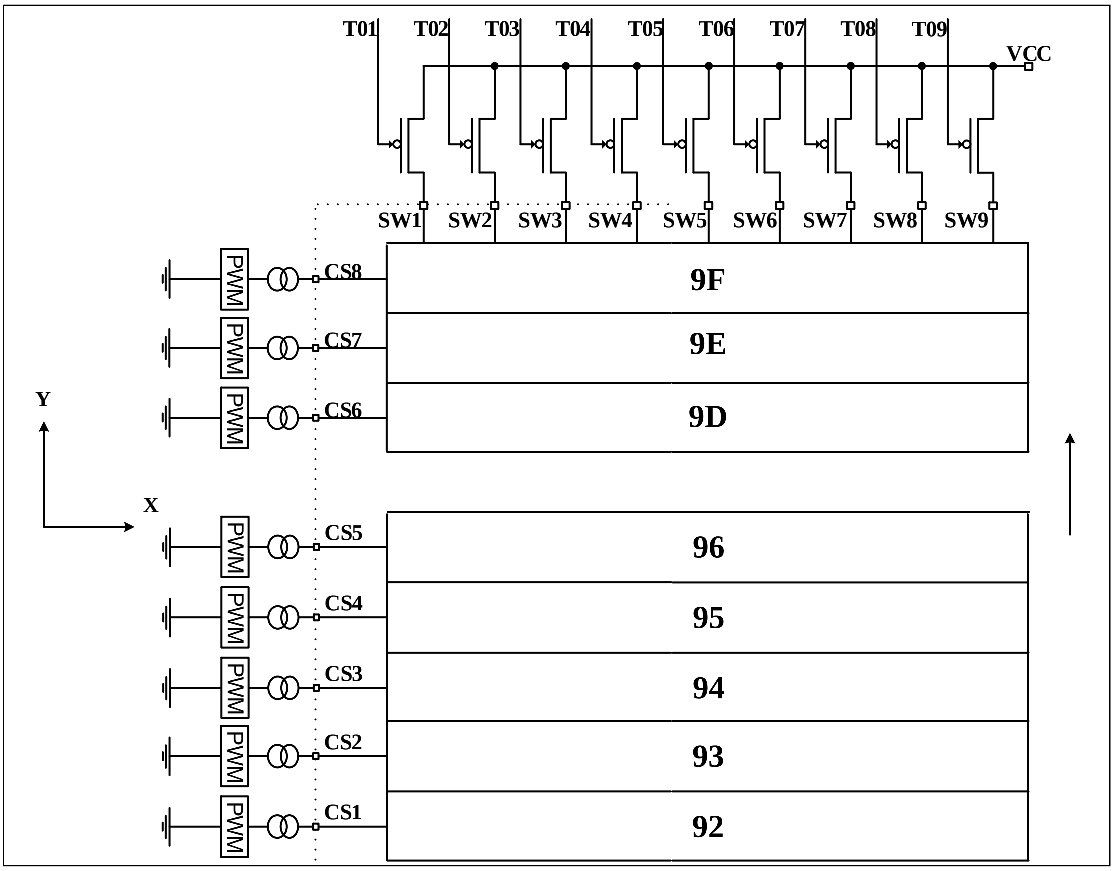


Figure 10 Scaling Register

Note 7: The above register address is in hexadecimal format.

Table 7 92h ~ 9Fh Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Scaling register control the DC output current of each CSy. Each CSy has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{342}{R_{ISET}} \times \frac{GCC}{64} \times \frac{SL}{256} \quad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~8), GCC is the Global Current Control Register (A1h) value and R_{ISET} is the external resistor of R_{ISET} pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if R_{ISET}=10kΩ, GCC=100 0000, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = \frac{342}{10k\Omega} \times \frac{64}{64} \times \frac{127}{256} = 16.9mA$$

$$I_{LED} = 16.9mA \times \frac{1}{9.27} \times \frac{PWM}{256}$$

Table 8 A0h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	LGC	OSDE	SSD
Default	0001	0	00	0

The Configuration Register sets operating mode of IS31FL3739.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

OSDE Open Short Detection Enable
00 Disable open/short detection
01/11 Enable open detection
10 Enable short detection

LGC H/L logic
0 1.4V/0.4V
1 2.4V/0.6V

SWS SWx Setting
0000 n=9, SW1~SW9, 9SW×7CS matrix
0001 n=8, SW1~SW8, 8SW×8CS matrix
0010 n=7, SW1~SW7, 7SW×8CS matrix, SW8 no-active
0011 n=6, SW1~SW6, 6SW×8CS matrix, SW7~SW8 no-active
0100 n=5, SW1~SW5, 5SW×8CS matrix, SW6~SW8 no-active
0101 n=4, SW1~SW4, 4SW×8CS matrix, SW5~SW8 no-active
0110 n=3, SW1~SW3, 3SW×8CS matrix, SW4~SW8 no-active
0111 n=2, SW1~SW2, 2SW×8CS matrix, SW3~SW8 no-active
1000 SW1~SW9 with same phase, all on.
Others SW1~SW9, SW1~SW9, 9SW×7CS matrix

When OSDE set to “01”, open detection will be trigger once, the user could trigger open detection again by set OSDE from “00” to “01”.

When OSDE set “10”, short detection will be trigger once, the user could trigger short detection again by set OSDE from “00” to “10”.

When SSD is “0”, IS31FL3739 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

SWS control the duty cycle of the SWx, default mode is 1/9.

Table 9 A1h Global Current Control Register

Bit	D7	D6:D0
Name	-	GCC
Default	0	000 0000

The Global Current Control Register modulates all CSy (y=1~8) DC current which is noted as I_{OUT} in 65 steps, maximum GCC is “100 0000’, if GCC> “1000000”, GCC= “100 0000”.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{342}{R_{ISET}} \times \frac{GCC}{64} \times \frac{SL}{256}$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 10 B0h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	SWPDR	-	CSPUR
Default	0	011	0	011

Set pull down resistor for SWx and pull up resistor for CSy.

PHC Phase choice
0 0 degree phase delay
1 180 degree phase delay

SWPDR SWx Pull down Resistor Selection Bit
000 No pull down resistor
001 0.5kΩ only in SWx off time
010 1.0kΩ only in SWx off time
011 2.0kΩ only in SWx off time
100 1.0kΩ all the time
101 2.0kΩ all the time
110 4.0kΩ all the time
111 8.0kΩ all the time

CSPUR CSy Pull up Resistor Selection Bit
000 No pull up resistor
001 0.5kΩ only in CSx off time
010 1.0kΩ only in CSx off time
011 2.0kΩ only in CSx off time
100 1.0kΩ all the time
101 2.0kΩ all the time
110 4.0kΩ all the time
111 8.0kΩ all the time

Table 11 B1h Spread Spectrum Register

Bit	D7:D6	D4	D3:D2	D1:D0
Name	-	SSP	RNG	CLT
Default	00	0	00	00

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function.

SSP Spread spectrum function enable
0 Disable
1 Enable

RNG Spread spectrum range
00 ±5%
01 ±15%
10 ±24%
11 ±34%

CLT Spread spectrum cycle time
00 1980μs
01 1200μs
10 820μs
11 660μs

Table 12 B2h PWM Frequency

Bit	D7:D3	D2:D0
Name	-	PWMF
Default	00000	001

Set the PWM frequency, default is 32kHz. In order to avoid LED display flicker, it is recommended PWM frequency ÷ n is higher than 100Hz, so when PWM frequency is 0.5kHz, n cannot be more than 4, when PWM frequency is 0.25kHz, n cannot be more than 2.

PWMF PWM frequency setting
000 55kHz
001 32kHz
010 4kHz
011 2kHz
100 1kHz
101 0.5kHz, (n≤4)
110 0.25kHz, (n≤2)
111 80kHz

Table 13-1 B3h/B5h/B7h/B9h/BBh/BDh/BFh/C1h/C3h Open/Short Register (Read Only)

Bit	D7	D6:D2	D1:D0
Name	-	CS05:CS01	-
Default	x	000 00	xx

Table 13-2 B4h/B6h/B8h/BAh/BCh/BEh/C0h/C2h/C4h Open/Short Register (Read Only)

Bit	D7:D5	D4:D0
Name	CS08:CS06	-
Default	000	x xxxx

When OSDE (A0h) is set to "01", open detection will be trigger once, and the open information will be stored at B3h~C4h.

When OSDE (A0h) set to "10", short detection will be trigger once, and the short information will be stored at B3h~C4h.

Before set OSDE, the GCC should set to 0x01.

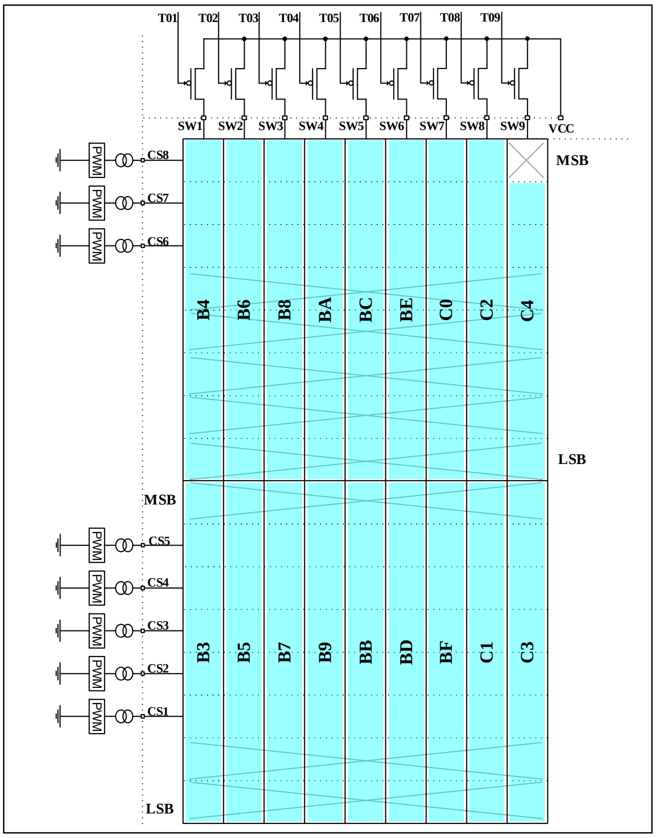


Figure 11 Open/Short Register

CFh Reset Register

Once the Reset Register is updated with 0xAE, all the IS31FL3729 registers will be reset to their default values. Upon initial power-up, the IS31FL3729 registers will also reset to their default values for a blank display.

APPLICATION INFORMATION

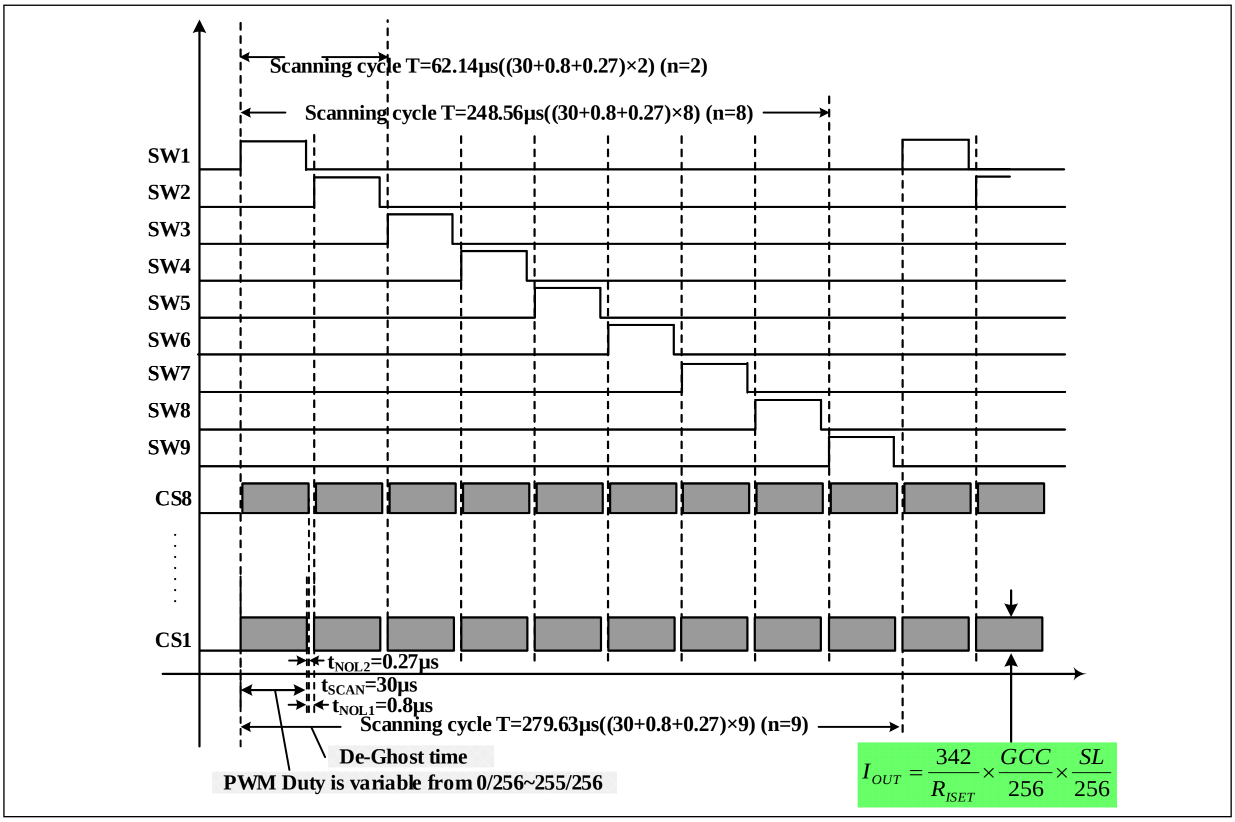


Figure 12 Scanning Timing

SCANNING TIMING

As shown in Figure above, the SW1~SW9 is turned on by serial, LED is driven 15 by 9 within the SWx (x=1~9) on time (SWx, x=1~9 is source and it is high when LED on) , including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~9) is (n=9):

$$Duty = \frac{30\mu s}{(30\mu s + 0.8\mu s + 0.27\mu s)} \times \frac{1}{9} = \frac{1}{9.32} \quad (2)$$

When n=8,

$$Duty = \frac{30\mu s}{(30\mu s + 0.8\mu s + 0.27\mu s)} \times \frac{1}{8} = \frac{1}{8.29} \quad (2)$$

Where PWM Frequency Register B2h= "0x01" (PWM frequency= 32kHz) for t_{SCAN}= 30μs, the period of scanning and 0.8μs is t_{NOL1}, the non-overlap time and 0.27μs is the CSx delay time.

POWER ON SEQUENCE

The IS31FL3739 integrates a power-on reset (POR) feature associated with the input supply voltage VCC. The IS31FL3739 will be initialized when VCC exceeds 2.4V (Typ., 2.7V max.) until then all the control circuits and configuration registers will be held in reset while the internal voltage stabilizes (≥ 2.4V).

The IS31FL3739 enters a hardware shutdown mode when the SDB pin is pulled low. During hardware shutdown the state Function Registers can be accessed but all analog circuits are disabled to conserve power. Once VCC stabilizes > 2.4V, a rising edge of the SDB signal will reset the I2C bus and cause the chip to exit hardware shutdown mode. Since there could be I2C bus transactions prior to the rising edge of the SDB pin, it is recommended to allow 10μs prior to and after the rising edge before beginning any I2C bus transaction.

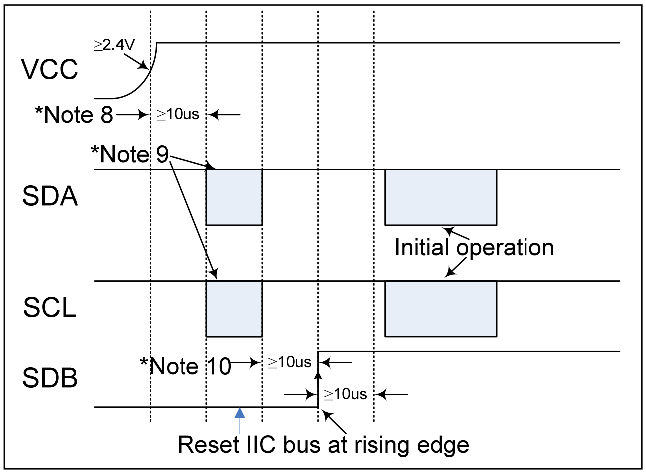


Figure 13 SDB Pin Sequence

Note 8: There should be no I2C operation 10μs before VCC remain ≥2.4V.

Note 9: I2C operation is allowed while SDB is low and VCC ≥2.4V.

Note 10: There should be no I2C operation 10μs before and after SDB rising edge.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \qquad (1)$$

Where PWM is PWM Registers' (03h~8Fh) data showing in Table 6.

For example, in Figure 1, if R_{ISET}= 10kΩ, PWM= 1011 0101 (0xB5, 181), and GCC= 100 0000, SL= 1111 1111, then,

$$I_{OUT(PEAK)} = \frac{342}{R_{ISET}} \times \frac{GCC}{64} \times \frac{SL}{256}$$

$$I_{LED} = \frac{342}{10\,k\Omega} \times \frac{64}{64} \times \frac{255}{256} \times \frac{1}{9.32} \times \frac{181}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3739 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 12 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

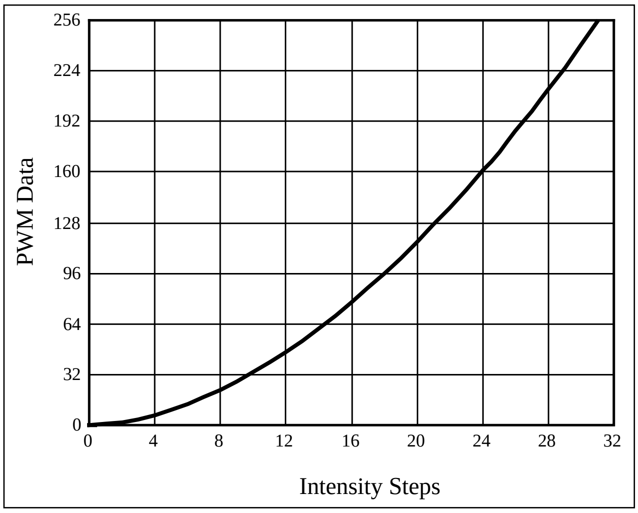


Figure 13 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 13 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

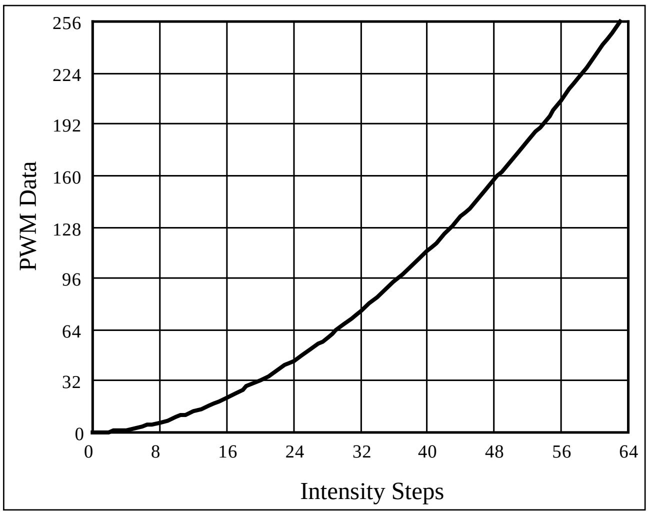


Figure 14 Gamma Correction (64 Steps)

Note 11: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3739 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3729 has individual LED open and short detection capability.

By setting the OSDE bits of the Configuration Register (A0h) from "00" to "01" or "10", the LED Open/short Register will begin storing the open/short information After 2 scan cycles, the MCU can read the open/short information stored in registers B3h~C4h. The open/short data will not get refreshed while setting the OSDE bit of the Configuration Register.

There are two configurations which need to be set prior to configuring the OSDE bits:

1) 0x0F≤A1h≤0x40 adjust LED current

2) B0h=0x00, disable pullup/pulldown resistors

Where A1h is the Global Current Control Register and B0h is the Pull Down/UP Resistor Selection Register.

The detect action is one-time event, so each time before reading out the open/short information, the OSDE bit of the Configuration Register (A0h) needs to be set from "0" to "1" (clear before set operation).

DE-GHOST FUNCTION

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3739 has integrated Pull down resistors for each SWx (x=1~9) and Pull up resistors for each CSy (y=1~8). Select the right SWx Pull down resistor (B0h) and CSy Pull up resistor (B0h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 2kΩ will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (A0h) to "0", the IS31FL3739 will operate in software shutdown mode. When the IS31FL3739 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consumption is 3μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consumption is 3μA.

The chip releases hardware shutdown when the SDB pin is pulled high.

If V_{CC} has a risk of dropping below 1.75V but remain above 0.1V while the SDB pin is pulled low, please re-initialize all Function Registers before SDB is pulled high.

LAYOUT

As described previously, depending on the current set resistor (R_{ISET}) value and current register settings, the chip can consumes lots of power. Please consider the below factors during the PCB layout phase.

1. The V_{CC} capacitors need to be close to the VCC pin 23 with their ground pins well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 9 or 16 vias thru the PCB to the other side's ground area to help radiate the heat. About the

thermal pad size, please refer to the land pattern of each package.

4. The CSy pins will have a maximum current of 35mA (R_{ISET}=10kΩ). However, the SWx pins maximum current is larger since it is the combined current of the CSy pins. Therefore, the width of the SWx trace needs to be much wider than the CSy trace.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

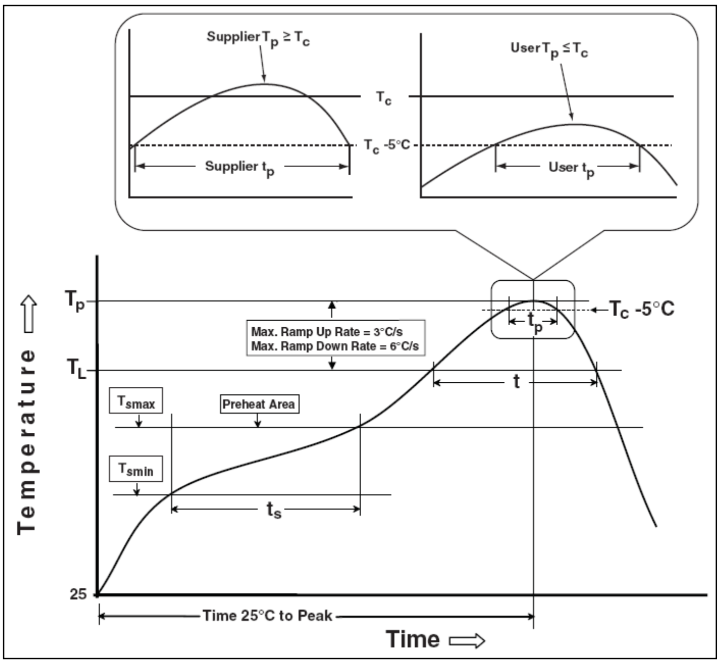
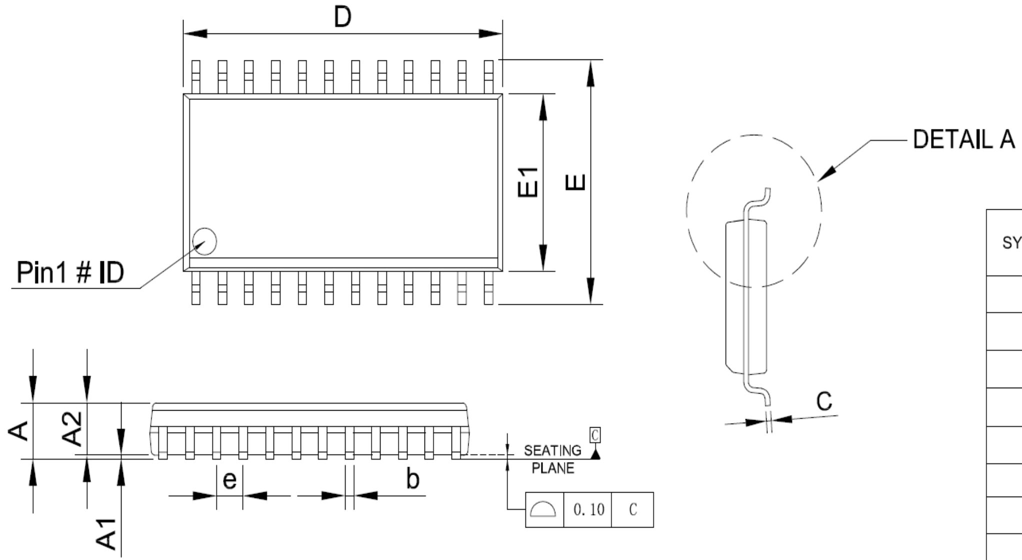
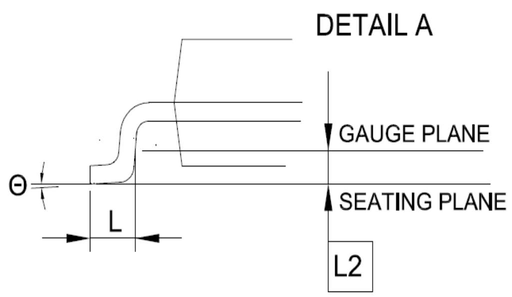


Figure 15 Classification Profile

PACKAGE INFORMATION

SOP-24





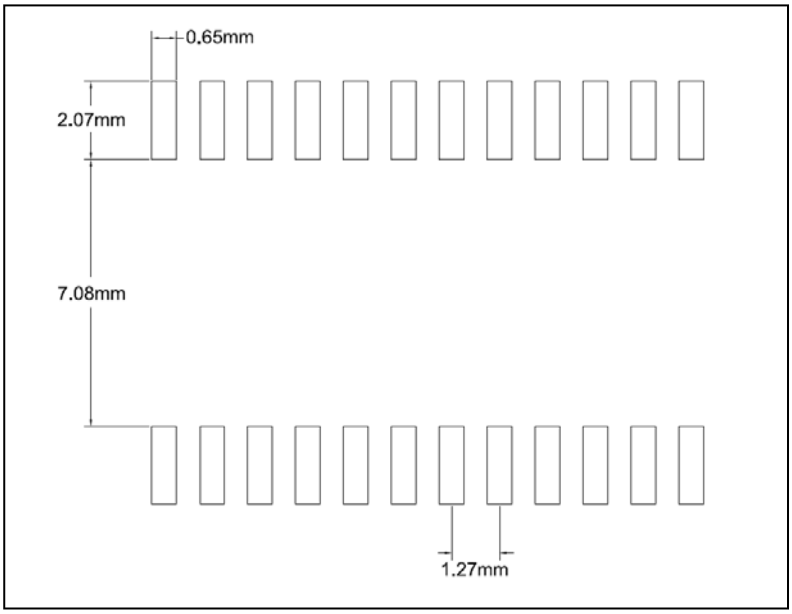
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	–	–
A2	2.05	–	–
E1	7.40	7.50	7.60
E	10.10	10.30	10.61
D	15.2	15.4	15.6
b	0.27	–	0.48
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.20	–	0.33

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-013
5. THE SHAPE OF BODY SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

SOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2019.12.05
A	Release to mass production	2020.01.17
B	Update θ_{JA} value	2020.02.24
C	Update Ordering Information to 1500/Reel	2020.07.10
D	Add POWER ON SEQUENCE section	2021.01.14