

IS31LT3948 AC DEMO BOARD GUIDE

DESCRIPTION

IS31LT3948 is a PFM step-up DC-DC converter designed for driving the white LED arrays for large size LCD panel backlighting applications. With internal OVP circuit, the chip and the system can be safe even if the load is not connected. The device features external PWM dimming or DC dimming, which allows the flexible control of the backlighting luminance. IS31LT3948 incorporates a unique FB scheme which automatically adjusts the integrated DC/DC converter to the optimum output voltage for the system, maximizing the efficiency.

IS31LT3948 general DEMO board is used in general lamp.

FEATURES

- Wide input voltage range: 5V~100V
- Constant Current Output limited only by external component selection (Note)
- No loop compensation required
- Internal over-voltage protection
- Internal over-temperature protection

Note: The maximum output current is determined by Vout/Vin ratio as well as the external components. If output current and Vout/Vin ratio is high, high current components of inductor and NMOS are needed.

QUICK START

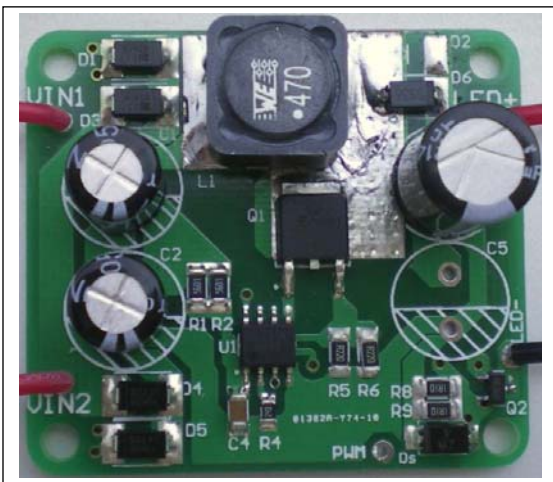


Figure 1: Photo of IS31LT3948 Evaluation Board

ORDERING INFORMATION

| Part No. | Temperature Range | Package |
|-----------------------|----------------------------|---------------------|
| IS31LT3948-GRLS2-EBAC | -40°C ~ +85°C (Industrial) | SOP-8-EP, Lead-free |

Table 1: Ordering Information

For pricing, delivery, and ordering information, please contacts Lumissil's analog marketing team at analog@Lumissil.com or (408) 969-6600.

RECOMMENDED EQUIPMENT

- 30VDC Power supply
- LED panel (1W LED, 12 LEDs in series)
- Multi-meter

RECOMMENDED INPUT AND OUTPUT RATINGS

- Input: 12VAC
- Output: 12LEDs in series/333mA

Note: The input voltage must be lower than the output voltage (total V_F).

ABSOLUTE MAXIMUM RATINGS

- Input voltage \leq 15VDC
- voltage \leq 45VDC

Caution: Do not exceed the conditions listed above, otherwise the board will be damaged or output current will be limited.

PROCEDURE

The IS31LT3948 DEMO Board is fully assembled and tested. Follow the steps listed below to verify board operation.

Caution: Do not turn on the power supply until all connections are completed.

- 1) Connect the terminals of the power supply to the VIN1 and VIN2 pin (If the board don't have the rectifier(D1,D3~D5), connect the positive terminal of the power supply to the VIN1 of the board and the negative terminal of power supply to the VIN2 of the board) .
- 2) Connect the negative of the LED panel (LED arrays) to the LED- terminal.
- 3) Connect the positive of the LED panel (LED arrays) to the LED+ terminal.
- 4) Turn on the power supply and the LED panel (LED arrays) will be light.

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DETAILED DESCRIPTION

COMPONENT SELECTION

The component selection is very important. They have a significant effect on the operating state of the demo board. The output capacitor must be a low ESR capacitor so as to minimize its affect on the line regulation and load regulation.

Please read the datasheet carefully to get more information about the component selection.

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems.

- Wide traces should be used for connection of the high current loop to minimize the EMI and unnecessary loss.
- The external components ground should be connected to IS31LT3948 ground as short as possible. Especially the Rcs and Rfb ground to IS31LT3948 ground connection should be as short

and wide as possible to have an accurate LED current.

- The capacitor C1, C2, C3 should be placed as close as possible to IS31LT3948 for good filtering. Especially the output capacitor C3 connection should be as short and wide as possible.
- NMOS drain is a fast switching node. The inductor and Schottky diode should be placed as close as possible to the drain and the connection should be kept as short and wide as possible. Avoid other traces crossing and routing too long in parallel with this node to minimize the noise coupling into these traces. The feedback pin (e.g. CS, FB, OVP) should be as short as possible and routed away from the inductor, the Schottky diode and NMOS. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

The thermal pad on the back of NMOS package must be soldered to the large ground plane for ideal power dissipation.

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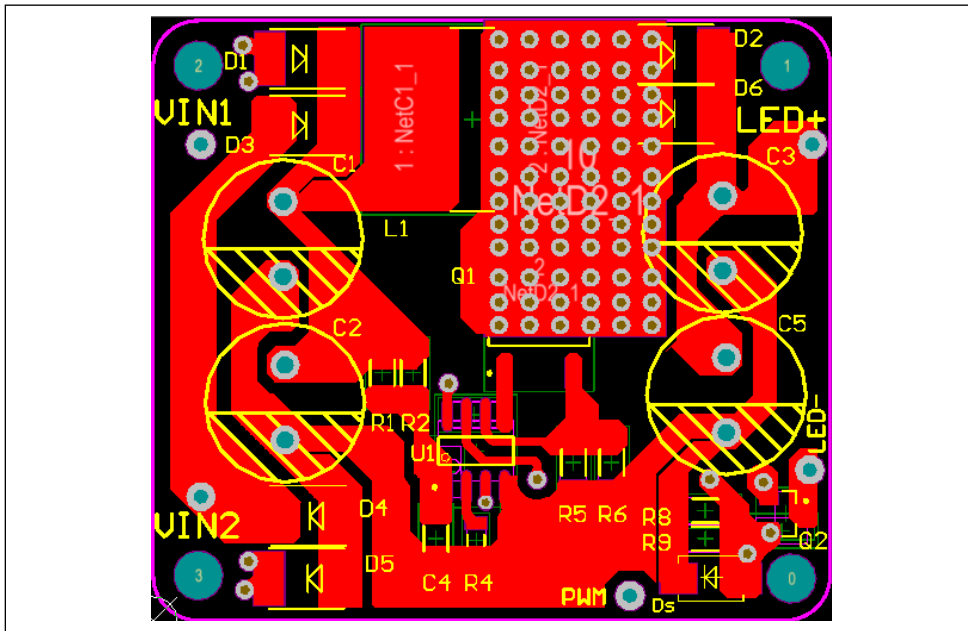


Figure 3: Board PCB Layout - Top Layer

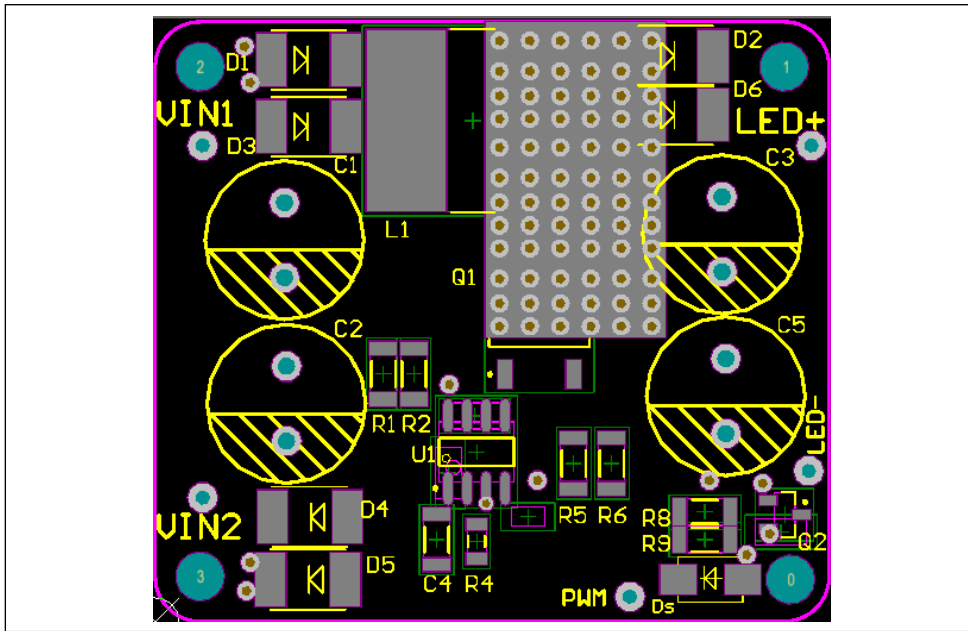


Figure 4: Component Placement Guide - Top Layer

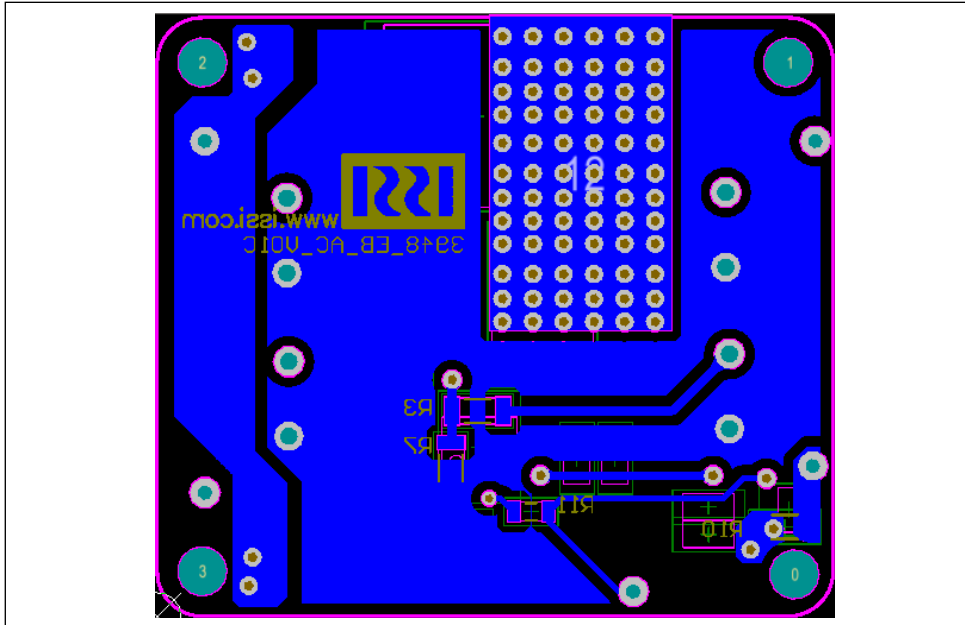


Figure 5: Board PCB Layout - Bottom Layer

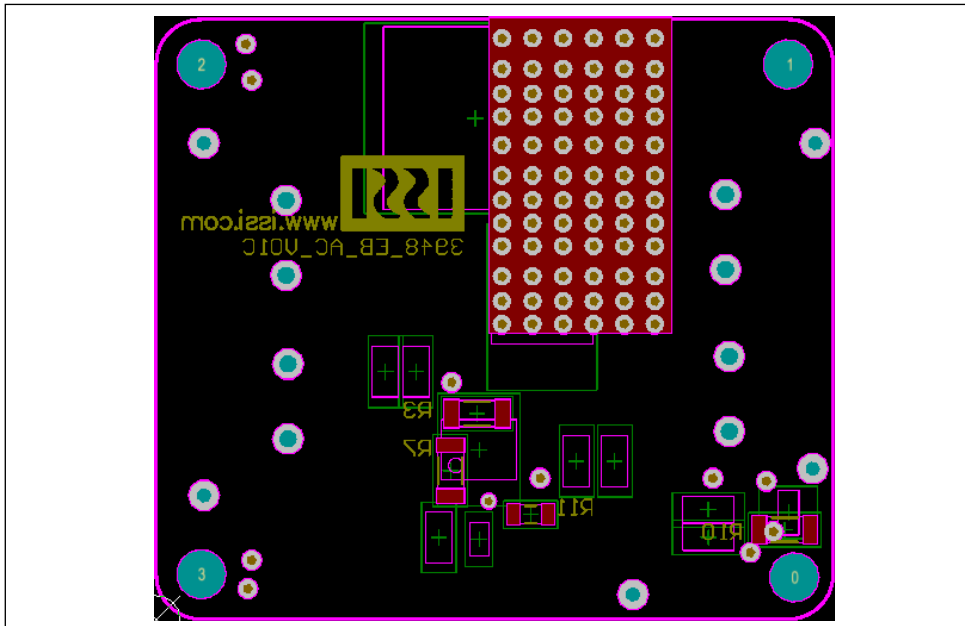


Figure 6: Component Placement Guide - Bottom Layer

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