4-CH CAPACITIVE TOUCH SENSOR WITH AUTO CALIBRATION

August 2015

GENERAL DESCRIPTION

The IS31SE5104 is a low power, fully integrated 4-channel solution for capacitive touch button applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic. On-chip calibration logic continuously monitors the environment and automatically adjusts on-and-off threshold levels to prevent false sensor activation.

The IS31SE5104 supports the 400kHz I²C serial bus data protocol and includes a field programmable slave address. An active low interrupt signal is generated on the INTB pin whenever a button event (touched or released) is detected. The triggered and cleared condition can be configured by setting the interrupt register.

IS31SE5104 is available in either a QFN-16 (3mm × 3mm) or SOP-16 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- Four capacitive touch sensor controller
- Auto offset compensation
- Sensitivity adjustable with external capacitor or internal register
- Low power optimized for portable applications
- Interrupt output
- 400kHz fast-mode I²C interface
- 8kV ESD HBM
- Operating temperature T_A = −40°C ~ +85°C
- QFN-16 (3mm × 3mm) and SOP-16 packages

APPLICATIONS

- Mobile phones
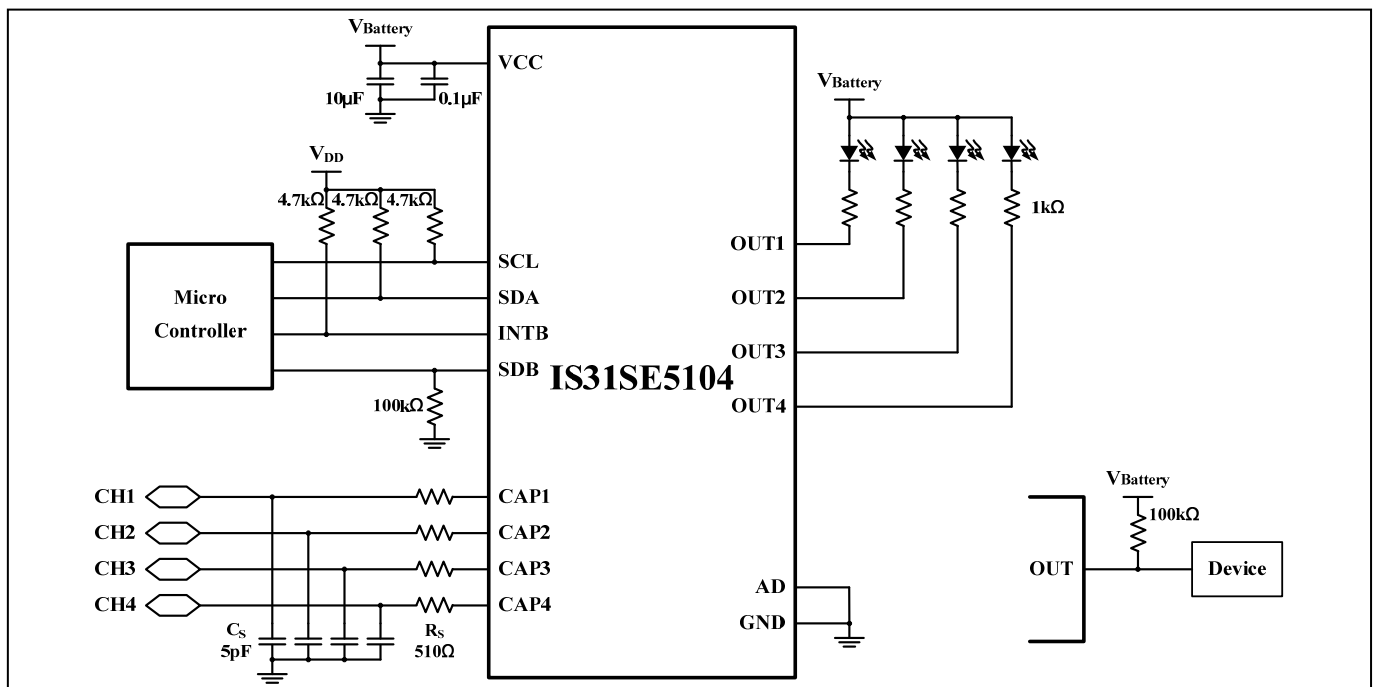- GPS
- PDAs

TYPICAL APPLICATION CIRCUIT

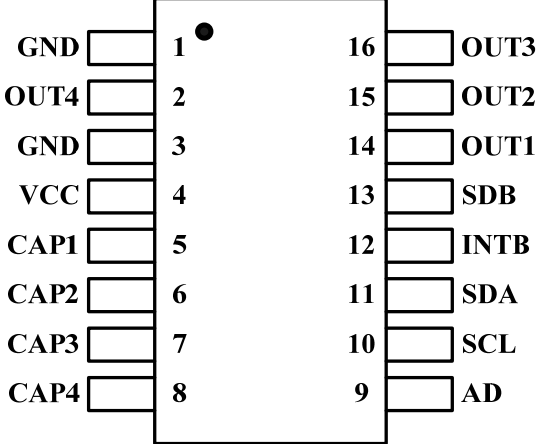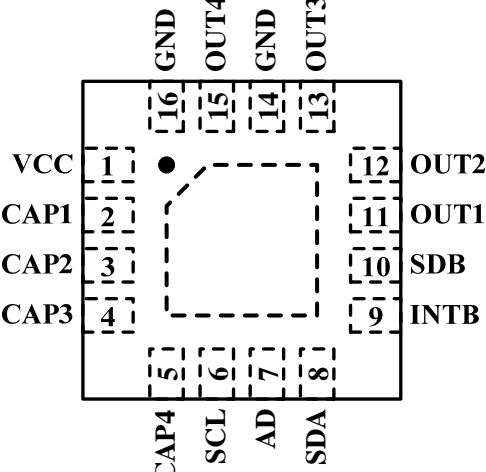**Figure 1** Typical Application Circuit

Note 1: The IC should be placed far away from the mobile antenna in order to prevent the EMI.
Note 2: The R_S resistor should place as close as possible to reduce EMI.
Note 3: The OUTx pin is open drain structure inside. To configure the OUTx pin as a logic signal output use a 100kΩ pull up resistor.

IS31SE5104

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-16	GND — 1 · / 16 — OUT3 OUT4 — 2 / 15 — OUT2 GND — 3 / 14 — OUT1 VCC — 4 / 13 — SDB CAP1 — 5 / 12 — INTB CAP2 — 6 / 11 — SDA CAP3 — 7 / 10 — SCL CAP4 — 8 / 9 — AD
QFN-16	16 GND, 15 OUT4, 14 GND, 13 OUT3 VCC — 1 · / 12 — OUT2 CAP1 — 2 / 11 — OUT1 CAP2 — 3 / 10 — SDB CAP3 — 4 / 9 — INTB 5 CAP4, 6 SCL, 7 AD, 8 SDA

PIN DESCRIPTION

No.		Pin	Description
SOP	QFN		
1,3	14,16	GND	Ground.
2	15	OUT4	Channel 4 outputs. Pulled low when input sense channel is pressed. Leave floating if not used.
4	1	VCC	Power supply.
5~8	2~5	CAP1 ~ CAP4	Input sense channel 1 ~ 4. Each channel should connect to GND if it is not used and disabled by the 01h register (Page 8).
9	7	AD	I2C address setting.
10	6	SCL	I2C serial clock.
11	8	SDA	I2C serial data.
12	9	INTB	Interrupt output, active low.
13	10	SDB	Shutdown the chip when pulled low.
14~16	11~13	OUT1 ~OUT3	Channel 1 ~ 3 outputs. Pulled low when input sense channel is pressed. Unused channel should be left floating.
-		Thermal Pad	Connect to GND.

IS31SE5104

ORDERING INFORMATION
Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY
IS31SE5104-QFLS2-TR	QFN-16, Lead-free	2500/Reel
IS31SE5104-GRLS2-TR	SOP-16, Lead-free	2500/Reel
IS31SE5104-GRLS2		50/Tube

IS31SE5104

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
ESD (HBM)	±8kV
ESD (CDM)	±1kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = -40°C ~ +85°C, V_{CC} = 2.7V ~ 5.5V, unless otherwise noted. Typical value are T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB} = V_{CC} = 3.6V		173	476	µA
I_{SD}	Shutdown current	V_{SDB} = 0V, V_{CC} = 5.5V		1.6	5.8	µA
V_{HR}	Current Sink headroom voltage	I_{OUT} = 20mA, V_{CC} = 3.6V	79	290	467	mV
ΔC_S	Minimum detectable capacitance	C_S = 5pF (Note 1)		0.2		pF
Logic Electrical Characteristics						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V(Note 1)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC}(Note 1)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			µs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			µs
$t_{SU, STA}$	Repeated START condition setup time		0.6			µs
$t_{SU, STO}$	STOP condition setup time		0.6			µs
$t_{HD, DAT}$	Data hold time				0.9	µs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			µs
t_{HIGH}	SCL clock high period		0.7			µs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 2)		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 2)		$20+0.1C_b$	300	ns

Note 1: Guaranteed by design.

Note 2: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31SE5104 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31SE5104 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1   Slave Address

Bit	A7:A3	A2:A1	A0
Value	10001	AD	1/0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31SE5104.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31SE5104's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31SE5104 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5104, the register address byte is sent, most significant bit first. IS31SE5104 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31SE5104 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31SE5104 address with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31SE5104 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31SE5104 to the master (Figure 5).
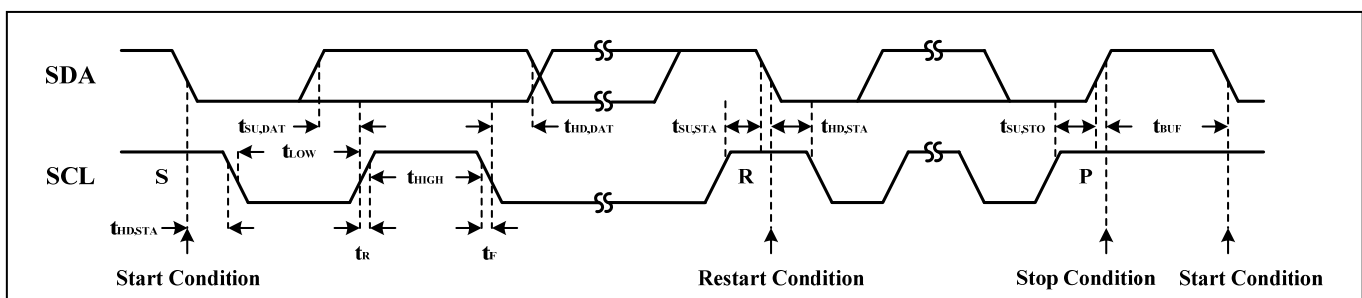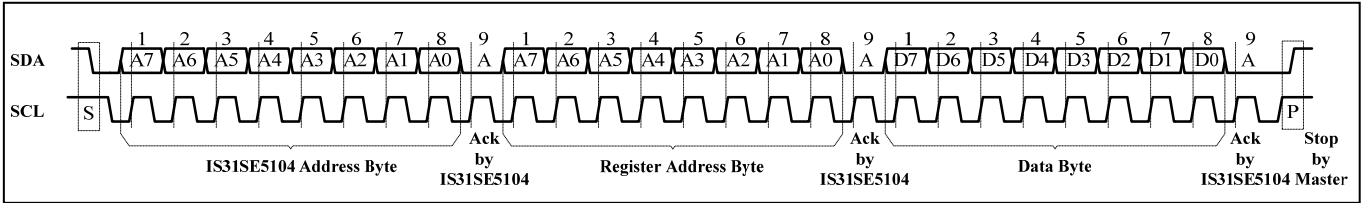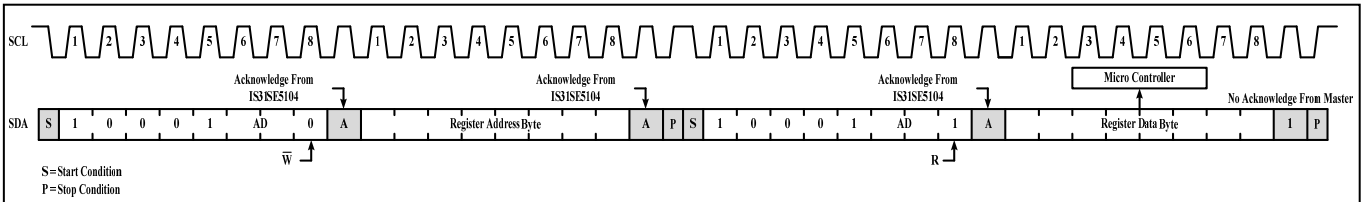

Figure 2   Interface timing
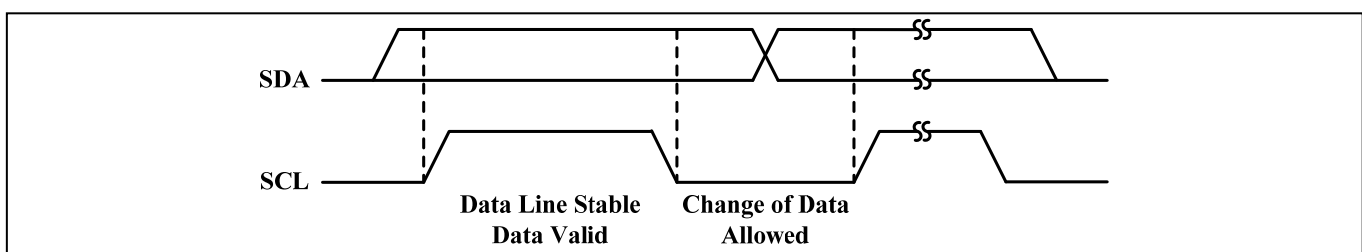
Figure 3   Bit transfer

Figure 4   Writing to IS31SE5104

Figure 5   Reading from IS31SE5104

Table 2   Register Function

Address	Name	Function	Table	Default
00h	Configuration Register	Set software shutdown mode and sensitivity	3	0000 0000
01h	Channel Control Register	Set the 4 channels enable	4	1111 1111
02h	State Register 1	Store state of action for 4 channels	5	
03h	State Register 2	Show state of 4 channels changes or not	6	0000 0000
04h	Interrupt Register	Set interrupt function	7	

Table 3   00h   Configuration Register

Bit	D7	D6:D5	D4:D0
Name	SSD	SS	-
Default	0	00	00000

The Configuration Register sets software shutdown mode and sensitivity.

SSD Software Shutdown Enable
0   Normal operation
1   Software shutdown mode

SS Sensitivity Selection
00   Normal sensitivity
01   High sensitivity
10   Low sensitivity
11   Not a valid state

Table 4   01h   Channel Control Register

Bit	D7:D4	D3:D0
Name	-	CH4: CH1
Default	1111	1111

The Channel Control Register sets the 4 channels enable.

CHx Channel Enable
0   Disable
1   Enable

Table 5   02h   State Register 1 (Read only)

Bit	D7:D4	D3:D0
Name	-	AS4: AS1
Default	0000	0000

The State Register 1 stores state of action for 4 channels.

ASx Action State Bit
0   Button released
1   Button pressed

Table 6   03h   State Register 2 (Read only)

Bit	D7:D4	D3:D0
Name	-	SC4: SC1
Default	0000	0000

The State Register 2 shows state of 4 channels changes or not.

SCx State Change Bit
0   No state change
1   Button touched or released event occurs

Table 7   04h   Interrupt Register

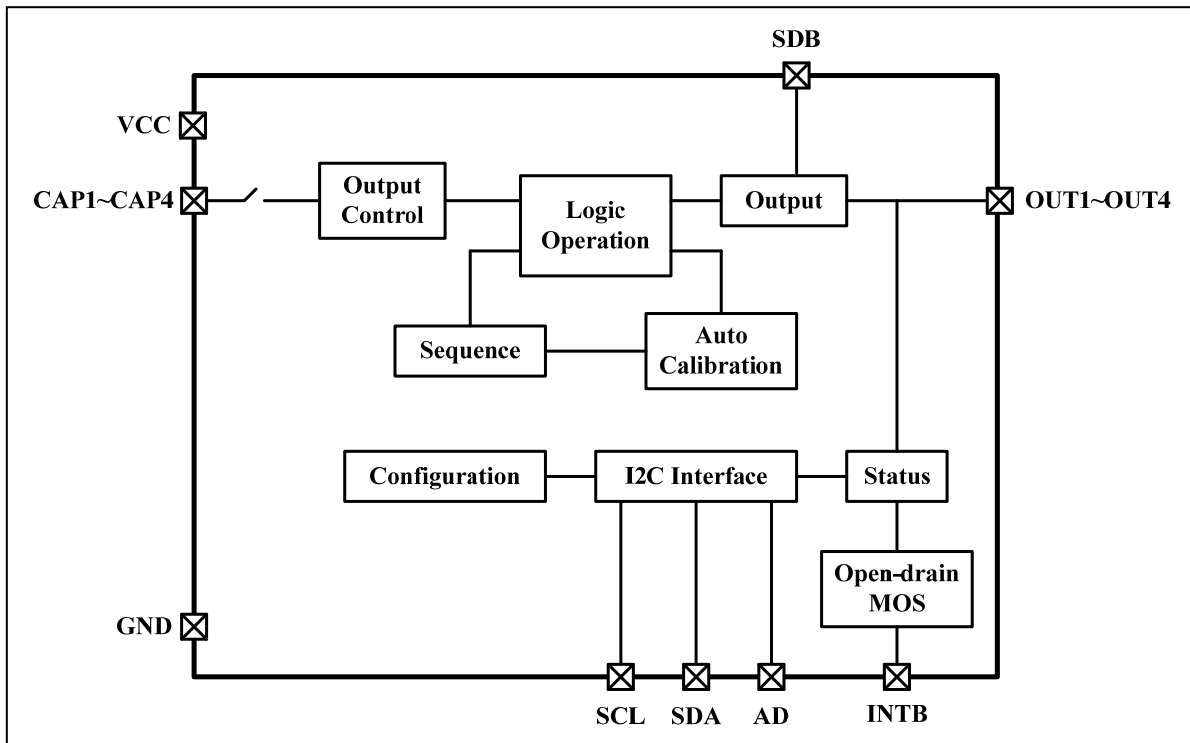| Bit	D7:D6	D5:D0
Name	ACI	-
Default	00	000000

The Interrupt Register sets interrupt function.

ACI Automatically Clear Interrupt
00   No auto clear
01   Auto clear after 8ms
10   Auto clear after 32ms
11   Not a valid state

IS31SE5104

FUNCTIONAL BLOCK DIAGRAM

APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS31SE5104 is an ultra low power, fully integrated 4-channel solution for capacitive touch-button applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic.

SENSITIVITY ADJUSTING

Sensitivity can be adjusted by using an external capacitor (Typical 5pF) or programming an internal register.

A high value of capacitor will lower the sensitivity; while a low value of capacitor will increase sensitivity.

The SS bit of Configuration Register (00h) is used to modulate sensitivity. By setting the SS bit to "00" sensitivity is normal. Sensitivity is high when SS bit is set to "01". Sensitivity is low when SS bit is set to "10". Setting SS bit to "11" is not a valid state.

OUTPUT CONTROL

There are 4 output ports (OUT1~OUT4) and 4 capacitive sensor input channels (CAP1~CAP4). The output port will be pulled low to drive an externally connected LED (with current limiting resistor) or other device when a capacitance change is detected on the corresponding input channel.

The OUT1~OUT4 ports are open drain type which require a 100kΩ pull up resistor when used for logic signaling.

For example, in Figure 1, when a sensitivity channels detects a capacitance change, the corresponding LED is driven by current set by the limiting resistor.

ACTION INFORMATION

The action information is stored in the State Register (02h, 03h). If the AS bit is set to "0", the corresponding channel is released. If the AS bit is set to "1", the corresponding channels is pressed. If the SC bit is set to "0", the corresponding channel has no status changing. If the SC bit is set to "1", the corresponding channel has status changing.

INTERRUPT SIGNAL

A detected capacitance change on any of the CAP1~CAP4 inputs will cause the INTB pin to be pulled low. The INTB signal is used for notifying the MCU that a capacitance disturbance has been detected. The MCU through the I2C bus can identify which input experienced they capacitance change by reading the Status Register (02h, 03h). The INTB will return to high state once the MCU has accessed the Status Register 2 (03h).

The ACI bit of Interrupt Register (04h) is used to configure the automatic interrupt clear function. If the ACI bit is set to "00", the automatic interrupt clear

function is disabled. If the ACI bit is set to "01", the function is enabled and the INTB pin will be automatically cleared after remaining low for 8ms. If the ACI bit is set to "10", the INTB pin will be automatically cleared after staying low for 32ms. Setting ACI bit to "11" is not a valid state.

AUTOMATIC CALIBRATION FUNCTION

The IS31SE5104 integrates an auto-calibration logic block to continuously update the reference capacitance register to compensate for slow changes in the environment. Very low capacitive changes are neutralized by the auto-calibration logic. The advantage of auto-calibration is capacitive changes due to dirt, humidity, or temperature will not affect this device. However, extremely fast changes will not be detected because the capacitance disturbance is digitally filtered out.

An auto-calibration cycle is performed every 2 seconds. CAP1~CAP4 capacitance is measured and the reference capacitance value in the hidden registers are updated. A detection cycle is performed every 16ms. The CAP1~CAP4 capacitance is measured and compared to the stored reference capacitance. A valid detection is when the CAP1~CAP4 capacitance differs from the stored reference capacitance value for two (2) detection cycles

The device can be programmed to 3 sensitivity detection levels: Normal, High and Low. An interrupt is generated if over two detection cycles the measured capacitance exceeds the stored reference value. A detection of 32 steps higher difference is recognized as a capacitive change for normal sensitivity, 16 steps higher for high sensitivity and 64 steps higher for low sensitivity.

SHUTDOWN MODE

There are two methods to place the IC in shutdown mode, software or hardware. The shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data but capacitance changes are not detected.

SOFTWARE SHUTDOWN

By setting SSD bit of the Configuration Register (00h) to "1", the IS31SE5104 will operate in software shutdown mode. In this shutdown mode, the device consumes only 1.6µA (typ.) current.

HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein the consumption current is the same as software shutdown, 1.6µA (Typ.).

IS31SE5104

CLASSIFICATION REFLOW PROFILES

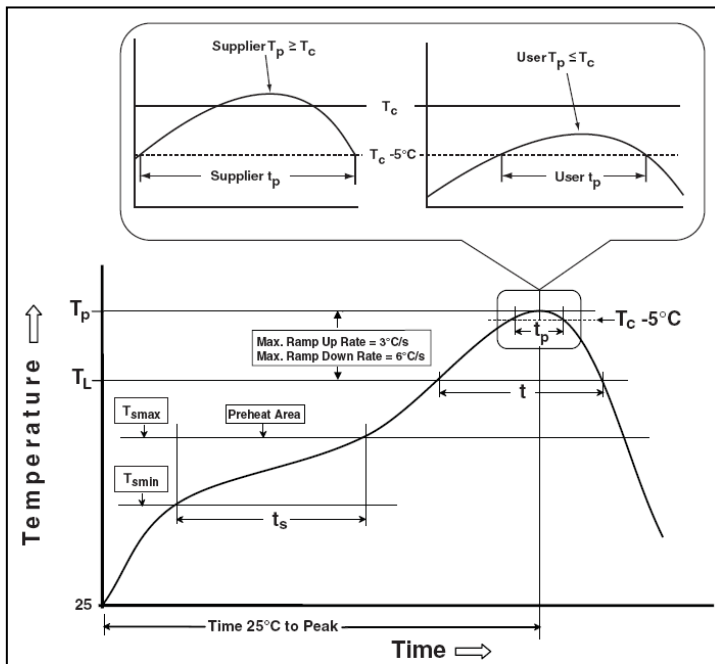| Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Figure 6   Classification profile

PACKAGE INFORMATION

QFN-16

TOP VIEW

Pin1 dot
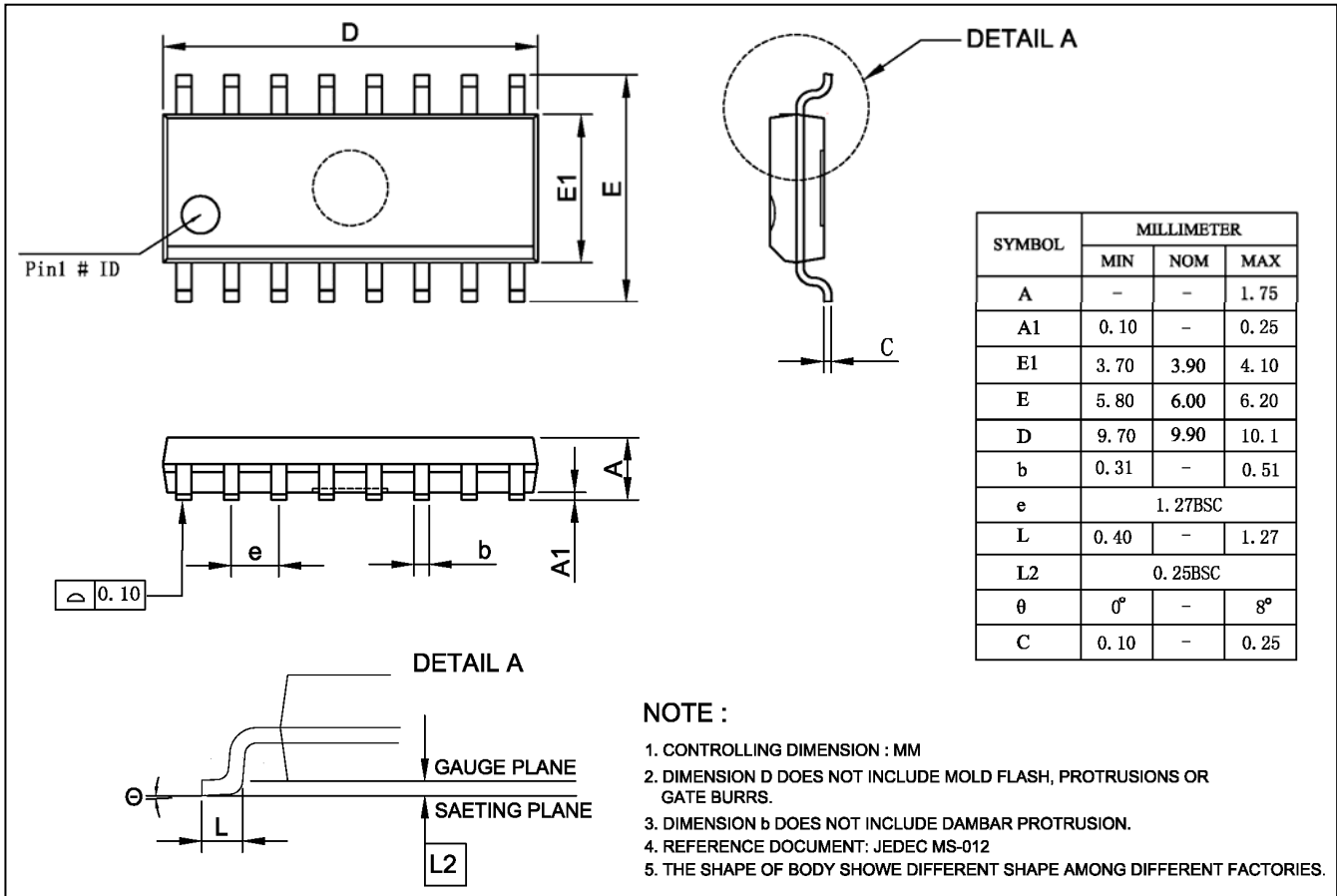by marking

BOTTOM VIEW

Pin1 # ID

SIDE VIEW

SEATING PLANE
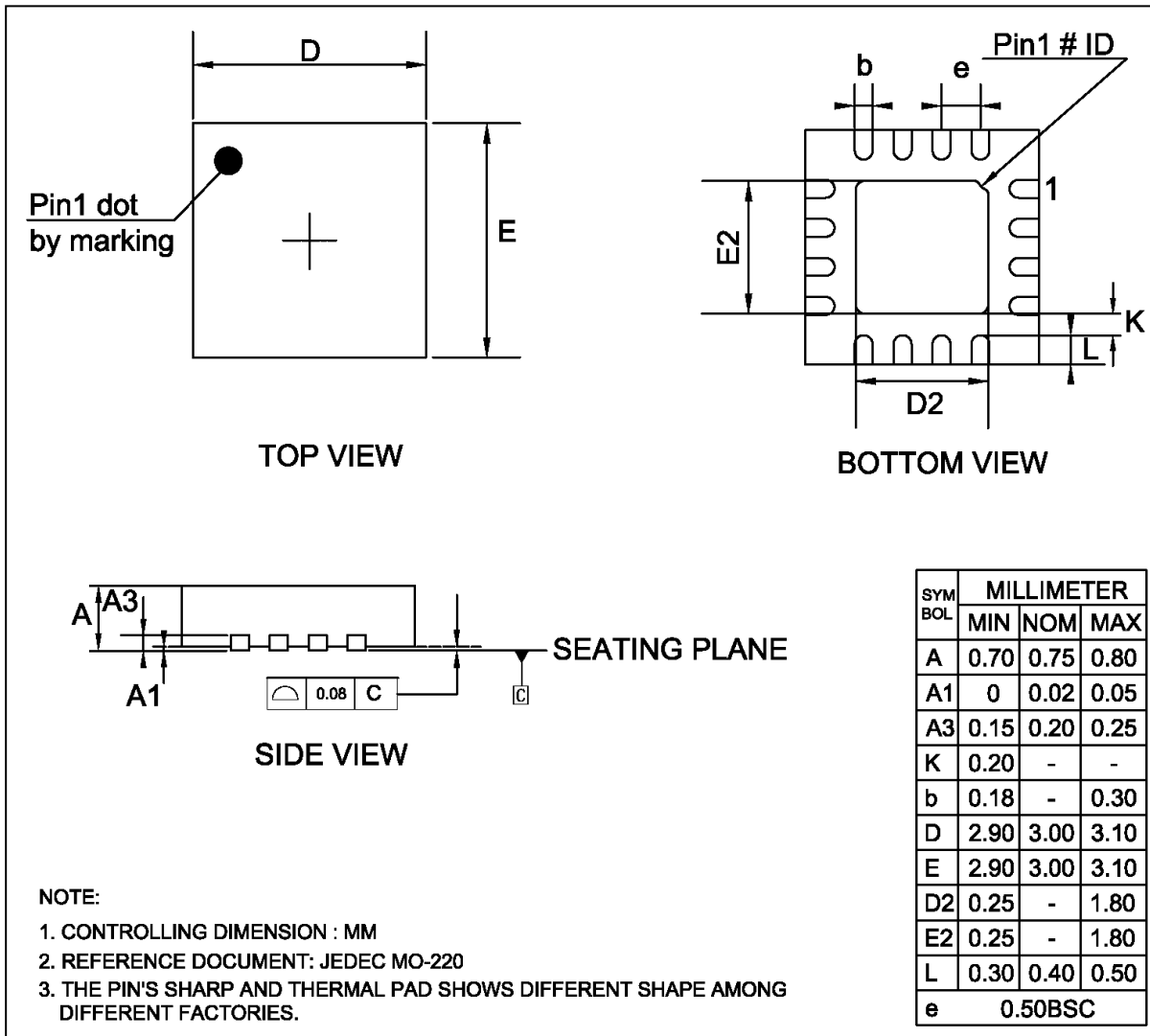
NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.15	0.20	0.25
K	0.20	-	-
b	0.18	-	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	0.25	-	1.80
E2	0.25	-	1.80
L	0.30	0.40	0.50
e	0.50BSC		

SOP-16

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	–	0.25
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
D	9.70	9.90	10.1
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.10	–	0.25

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY SHOWE DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.
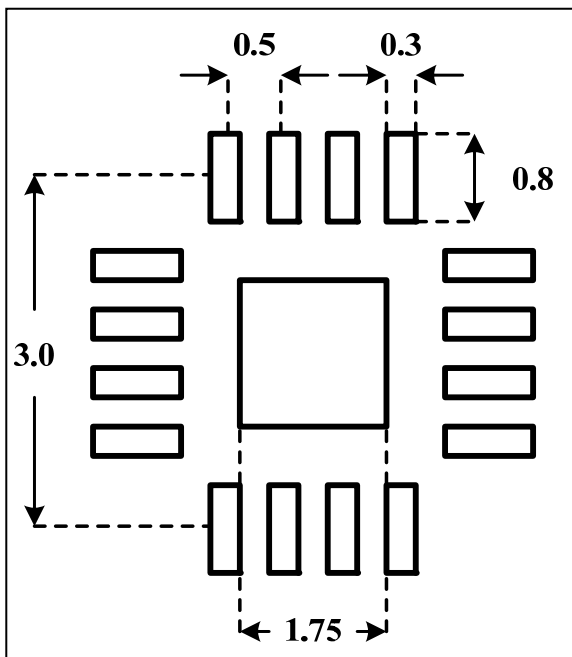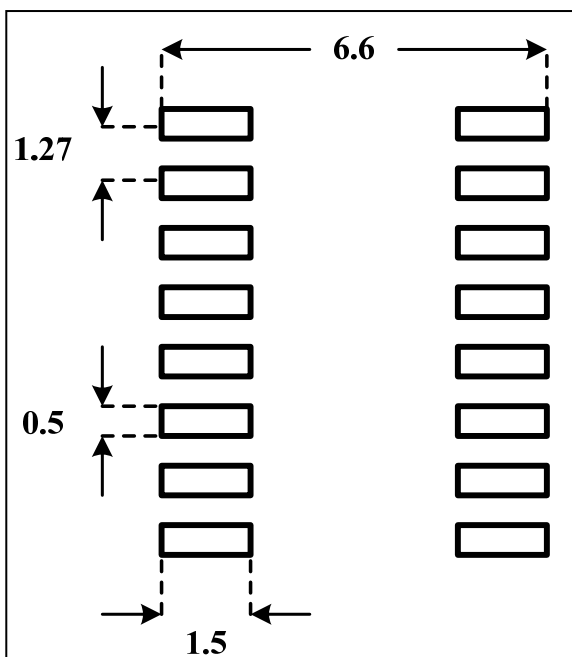
RECOMMENDED LAND PATTERN

QFN-16

SOP-16

Note:

1. Land pattern complies to IPC-7351.

2. All dimensions in MM.

3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2013.12.25
B	1. Add Tape reel packing for SOP (Not release)	2014.11.10
C	1. Add land pattern 2. Add revision history 3. Revise Application Information 4. Update POD	2015.08.05

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